nine bit register is used to calculate the CRC character while writing data on the tape according to the following rules[7]:

(a) Initially the CRC register is clear.

(b) All the data characters (data character includes the vertical parity) are added to the contents of the CRC register without carry (half addition).

(c) Between such additions, the contents of the CRC register are rotated (not normal shifting) one position to the right (CRC P to CRC 0 etc. and CRC 7 to CRC P).

(d) If the rotation in (c) will cause the CRC P bit to become a '1', the bits being rotated into the positions CRC 2, CRC 3, CRC 4 and CRC 5 are inverted.

(e) After the last data character hasbeen added, the CRC register is rotated once more in accordance with the steps (c) and (d).

(f) To write the CRC character on the tape, the contents of all the bit positions except CRC 2 and CRC 4 are inverted.

Drawing 6.16 shows the CRC register configuration together with all the gating necessary for rotating the contents of CRC and communicating with RWB 1.

The signals 0 → CRC to clear the CRC register, RWB → CRC to transfer the data character into the CRC, ROTATE CRC to rotate the contents of the CRC register and CRC → RWB to transfer the contents of the CRC into RWB 1 for writing on the tape, are shown on Drawing 6.17.

5.8.1 CRC register

As can be seen from Drawing 6.16, the flip-flops used to construct the CRC register have 4 DCD gates, two on the set and two on the reset side. The level inputs of the inner set of DCD gates are connected together and are fed from the corresponding bit of the RWB 1,

so that when the common pulse line is excited by the RWB → CRC pulse, the data character will be Exclusively OR'ed into the CRC register. Thus, if the RWB 10 is a '1', the level inputs of the inner set of DCD gates of the CRC 0 will be at ground and when the RWB → CRC pulse occurs, CRC 0 will be complemented (i.e. RWB 10 is half added with CRC 0 and the result is left in CRC 0). The level inputs of the outer set of DCD gates are obtained from the '1' and '0' outputs of the previous bit to perform the rotation except for the CRC 2 through CRC 5 and CRC P. The CRC P is connected to the CRC 7 for rotation, while the others obtain their level inputs from a gating network to comply with rule (d). Because the contents of the CRC 7 will appear in CRC P after rotation, rotation into the CRC 2 through CRC 5 is controlled by the outputs of CRC 7. If this happens to be a '1', the content entered into CRC 2 through CRC 5 is the complement of the previous bit. Thus, if CRC 7 is a '1' and CRC 1 is a '0' before rotation, a '1' will appear in CRC 2 when the rotation is complete. On the other hand, if CRC 7 is a '0', the preceding bit will be entered into the CRC 2 through CRC 5 positions.

When the CRC control (Drawing 6.17) generates the CRC → RWB pulse, all the CRC bit positions except CRC 2 and CRC 4 are gated in the complement form into the corresponding positions of RWB 1 to obtain the Cyclic Redundancy Check Character.

5.8.2 CRC register control signal generation

When the CLOCK COUNTER overflows (this is the write time), the CRC control generates the RWB → CRC pulse to perform the half addition between the data character and the CRC Register. The RWB → CRC pulse also triggers a 2 microseconds delay. At the end of this delay the ROTATE CRC signal is generated, to rotate the contents of the CRC Register. This delay is provided to allow for the settling of the CRC Register from the half addition performed by the RWB → CRC pulse. After writing the last data character in a record, the real time clock which provides the MASTER CLOCK signals is switched off, by clearing the CLOCK ENABLE flip-flop (see section 5.11).

When the writing is at 800 bpi, resetting the CLOCK ENABLE triggers a 5 microseconds delay. After completing this delay the CRC control generates the CRC → RWB pulse and triggers the CRC delay. The CRC → RWB pulse is used to load the contents of the CRC Register into RWB 1 (see section 5.8.1). The 5 microseconds delay from the time the CLOCK ENABLE flip-flop is cleared and the CRC → RWB pulse is generated, is to ensure that the last data character has been written on the tape and the RWB 1 is cleared before loading the CRC character into it. The CRC delay when complete, generates the WRITE TIME pulse (see Drawing 6.11), which triggers the WRITE PULSER to write the CRC character and clear the RWB 1.

It should be noted that the CRC → RWB pulse is generated only during a 800 bpi operation because the CRC character is required only for IBM compatibility (see section 3.6). The CRC delay is chosen equal

to 95 microseconds so that together with the aforementioned 5 microseconds delay a total of 100 microseconds of delay will be obtained between the last data character and the CRC character. This time is equal to the 4 character spaces required for IBM compatibility of 800 bpi tapes running at a speed of 50 inches per second. Figure 5.4 shows the timing diagram for the CRC control signal generation.

5.9 Data Break Interface and Control:

The Data Break facility of the PDP-8 allows one input-output device to communicate directly with the core memory on a cycle stealing basis. The tape control unit, which can control two transports, is treated as a single device.

5.9.1 Data break interface

Information flow to effect a Data Break transfer with an input-output device, appears in Figure 5.5. In general terms, to initiate a Data Break transfer, the interface must provide the following information:

(a) Specify the affected address in the core memory.

(b) Provide the data word by establishing the proper logic levels at the computer interface.

(c) Provide the necessary gating to receive the word for a transfer from the computer.

(d) Provide a logical signal to indicate the direction of transfer (in or out of the computer).

(e) Provide a logical signal to indicate single cycle or three cycle break operation.

(f) Present a proper signal to request a Data Break.