nine bit register is used to calculate the CRC character while writing data on the tape according to the following rules[7]:

(a) Initially the CRC register is clear.

(b) All the data characters (data character includes the vertical parity) are added to the contents of the CRC register without carry (half addition).

(c) Between such additions, the contents of the CRC register are rotated (not normal shifting) one position to the right (CRC P to CRC 0 etc. and CRC 7 to CRC P).

(d) If the rotation in (c) will cause the CRC P bit to become a '1', the bits being rotated into the positions CRC 2, CRC 3, CRC 4 and CRC 5 are inverted.

(e) After the last data character hasbeen added, the CRC register is rotated once more in accordance with the steps (c) and (d).

(f) To write the CRC character on the tape, the contents of all the bit positions except CRC 2 and CRC 4 are inverted.

Drawing 6.16 shows the CRC register configuration together with all the gating necessary for rotating the contents of CRC and communicating with RWB 1.

The signals 0 → CRC to clear the CRC register, RWB → CRC to transfer the data character into the CRC, ROTATE CRC to rotate the contents of the CRC register and CRC → RWB to transfer the contents of the CRC into RWB 1 for writing on the tape, are shown on Drawing 6.17.

5.8.1 CRC register

As can be seen from Drawing 6.16, the flip-flops used to construct the CRC register have 4 DCD gates, two on the set and two on the reset side. The level inputs of the inner set of DCD gates are connected together and are fed from the corresponding bit of the RWB 1,

so that when the common pulse line is excited by the RWB → CRC pulse, the data character will be Exclusively OR'ed into the CRC register. Thus, if the RWB 10 is a '1', the level inputs of the inner set of DCD gates of the CRC 0 will be at ground and when the RWB → CRC pulse occurs, CRC 0 will be complemented (i.e. RWB 10 is half added with CRC 0 and the result is left in CRC 0). The level inputs of the outer set of DCD gates are obtained from the '1' and '0' outputs of the previous bit to perform the rotation except for the CRC 2 through CRC 5 and CRC P. The CRC P is connected to the CRC 7 for rotation, while the others obtain their level inputs from a gating network to comply with rule (d). Because the contents of the CRC 7 will appear in CRC P after rotation, rotation into the CRC 2 through CRC 5 is controlled by the outputs of CRC 7. If this happens to be a '1', the content entered into CRC 2 through CRC 5 is the complement of the previous bit. Thus, if CRC 7 is a '1' and CRC 1 is a '0' before rotation, a '1' will appear in CRC 2 when the rotation is complete. On the other hand, if CRC 7 is a '0', the preceding bit will be entered into the CRC 2 through CRC 5 positions.

When the CRC control (Drawing 6.17) generates the CRC → RWB pulse, all the CRC bit positions except CRC 2 and CRC 4 are gated in the complement form into the corresponding positions of RWB 1 to obtain the Cyclic Redundancy Check Character.

5.8.2 CRC register control signal generation

When the CLOCK COUNTER overflows (this is the write time), the CRC control generates the RWB → CRC pulse to perform the half addition between the data character and the CRC Register. The RWB → CRC pulse also triggers a 2 microseconds delay. At the end of this delay the ROTATE CRC signal is generated, to rotate the contents of the CRC Register. This delay is provided to allow for the settling of the CRC Register from the half addition performed by the RWB → CRC pulse. After writing the last data character in a record, the real time clock which provides the MASTER CLOCK signals is switched off, by clearing the CLOCK ENABLE flip-flop (see section 5.11).

When the writing is at 800 bpi, resetting the CLOCK ENABLE triggers a 5 microseconds delay. After completing this delay the CRC control generates the CRC → RWB pulse and triggers the CRC delay. The CRC → RWB pulse is used to load the contents of the CRC Register into RWB 1 (see section 5.8.1). The 5 microseconds delay from the time the CLOCK ENABLE flip-flop is cleared and the CRC → RWB pulse is generated, is to ensure that the last data character has been written on the tape and the RWB 1 is cleared before loading the CRC character into it. The CRC delay when complete, generates the WRITE TIME pulse (see Drawing 6.11), which triggers the WRITE PULSER to write the CRC character and clear the RWB 1.

It should be noted that the CRC → RWB pulse is generated only during a 800 bpi operation because the CRC character is required only for IBM compatibility (see section 3.6). The CRC delay is chosen equal

to 95 microseconds so that together with the aforementioned 5 microseconds delay a total of 100 microseconds of delay will be obtained between the last data character and the CRC character. This time is equal to the 4 character spaces required for IBM compatibility of 800 bpi tapes running at a speed of 50 inches per second. Figure 5.4 shows the timing diagram for the CRC control signal generation.

5.9 Data Break Interface and Control:

The Data Break facility of the PDP-8 allows one input-output device to communicate directly with the core memory on a cycle stealing basis. The tape control unit, which can control two transports, is treated as a single device.

5.9.1 Data break interface

Information flow to effect a Data Break transfer with an input-output device, appears in Figure 5.5. In general terms, to initiate a Data Break transfer, the interface must provide the following information:

(a) Specify the affected address in the core memory.

(b) Provide the data word by establishing the proper logic levels at the computer interface.

(c) Provide the necessary gating to receive the word for a transfer from the computer.

(d) Provide a logical signal to indicate the direction of transfer (in or out of the computer).

(e) Provide a logical signal to indicate single cycle or three cycle break operation.

(f) Present a proper signal to request a Data Break.

(12) Generate a post-record delay as specified in Table 2 according to speed.

(13) Subsequent operation can now be performed as desired.

3-3. VERTICAL PARITY GENERATION

The vertical parity bit (VRC) recorded in Channel P on 9-track systems is generated so that the total number of "1" bits in each data character (not the CRCC or LRCC) is always odd. On 7-track systems, even parity is used when writing BCD.

3-4. CRC GENERATION (9-TRACK SYSTEMS ONLY)

The CRCC is based on a modified cyclic code and provides a more rigorous method of error detection than using the VRC or LRC checks only. When reading, it can also be used in conjunction with the VRC and LRCC checks for error correction, provided that the errors are confined to a single channel. For a more detailed description of CRCC refer to PEC Application Note, Document No. 70701.

The CRCC can be generated according to the following rules:

(1) Each data character is added to the contents of a CRC register (CRCR) without carry - each bit being exclusively ORed to the corresponding bit of the CRCR.

(2) This information then undergoes a circular shift right of one place, such that each bit is copied into the adjacent CRCR flip-flop:

(CRCP → CRC0, etc.)

(3) If the bit entering CRCP is a "1", the bits entering CRC2, CRC3, CRC4, and CRC5 are inverted.

(4) Steps (1), (2), and (3) are repeated for each data character of the record.

(5) The contents of all CRCR positions, except CRC2 and CRC4, are inverted and the resultant character is written onto the tape.

Figure 9 shows a block diagram of a CRCR. Note that this circuit requires one clock pulse for each data character, and that no extra shift is required after the last data character.

If it is required to regenerate the CRCC during a Read Reverse command, the significance of the data bits entering the CRCR must also be reversed.

The CRCC has the following properties.

(1) It can be an all-zeroes character.

(2) Its value is such that the LRCC always has odd parity (therefore the LRCC can never be all-zeroes).

(3) It has odd parity if there are an even number of data characters, or even parity for an odd number of data characters.

For compatibility reasons, the correct CRCC should always be written onto tape even though it is intended not to make use of it for read checking.

RECORDING METHODS

Before information is written on tape, tape coating is erased to a specified magnetic flux polarity. Erasure is accomplished by passing tape across a dc erase head before it is written. The erase head magnetizes the entire width of the tape so that the end of tape nearest the beginning-of-tape (BOT) marker is a north-seeking magnetic pole. Interblock gap areas have the same magnetic flux polarity that is produced by the erase head.

Both the nonreturn to zero IBM (NRZI) and the phase-encoded (PE) methods record information by producing magnetic flux reversals in the tape coating. The NRZI method uses a flux reversal in either direction to represent a 1-bit. When writing NRZI tape, flux reversals are written only for 1-bits. When reading NRZI tape, the absence of a flux reversal is interpreted as a 0-bit (Ⓐ, Figure 3).

When writing PE tape, flux reversals are written for both 1- and 0-bits. When tape is moving forward, a flux reversal to the magnetic polarity of "erased" tape at bit-shift time is defined as a 1-bit. A flux reversal to a polarity opposite that of erased tape at bit-shift time is defined as a 0-bit (Ⓑ, Figure 3). The comparison of the flux reversals needed to write a series of bits on tape in both NRZI and PE mode is shown on Ⓒ, Figure 3. The extra shifts that occur at bit-cell-boundary time (phase bits) are necessary to maintain the correct direction of shift for each type of bit, when writing two like PE bits (1 and 1 or 0 and 0) in succession.

Each PE data block is preceded and followed by a burst of all-zeros bytes and an all-ones marker (preamble and postamble). The preamble synchronizes the read detection circuits so that 1's and 0's are identified correctly when reading the data bytes which follow. The postamble indicates the end of the data in a tape block. When reading backward, the functions of the preamble and postamble are reversed.

When tape is read, the bits (flux reversals) are sensed by the read head to produce a waveform similar to the waveform which wrote the bits. The waveform is decoded in a 2803/2804 to 0- and 1-bits by comparing it to reference (clock) pulses. Because the sensing and decoding of a bit depend not only on the magnetic strength of the signal but also on the polarity and timing of the recorded signal, the possibility of an error because of weak or extraneous signals is considerably reduced.

The nine-track tape format used with the System/360 eight-bit code and the seven-track tape format used with the six-bit BCD code are shown in Figures 18-20. To increase nine-track reliability, the bit tracks are arranged to place the most-used bits in the center of the tape.

Error Correction

Nine-track NRZI tapes are written with a cyclic redundancy check (CRC) character at the end of each data block (Figure 18). This character, which is used to correct single-track read errors, is generated in the CRC register in the tape control. The contents of the nine positions of the CRC register are designated CP (parity) and C0 through C7.

The CRC character is formed in the following manner:

1. All data characters in the tape block are added to the CRC register without carry (each bit position n is exclusive ORed to Cn).
2. Between additions the CRC register is shifted one position (CP to C1, etc., and C7 to CP).
3. If shifting will cause CP to become a 1, the bits being shifted into positions C2, C3, C4, and C5 are inverted.
4. After the last data character has been added, the CRC register is shifted once more in accordance with steps 2 and 3.
5. To write the CRC character on tape, the contents of all positions except C2 and C4 are inverted. The parity of the CRC character is odd if the number of data characters within the block is even, and the parity is even if the number of data characters within the block is odd. The CRC character may contain all 0-bits only if the number of data characters is odd.

Additional information on nine-track NRZI error correction is in Field Engineering Theory of Operation, *IBM 2803/2804 Model 1 Tape Control and Tape Controls for 2403/2404 Models 1, 2, and 3,* Form Y22-2853.

OPERATOR'S CONTROLS AND INDICATORS

Operator's Panel

The operator's panel is shown in Figure 4. For convenience, the indicators are all in the upper row and the controls are in the lower row.

Select

The select indicator is turned on to show that the tape unit is the one selected to perform the next tape function. The tape unit must be in ready status.

Ready

When on, the ready indicator shows that the tape unit is in ready status; that is, the tape unit is loaded (tape in the vacuum columns and across read/write head), all interlocks are closed, and tape is not rewinding. This indicator is turned on by pressing the start pushbutton, but it will not turn on unless the two preceding conditions are satisfied. Pressing the start pushbutton while the tape is in motion, as in a load/rewind operation, will not turn on this indicator immediately; but the indicator will turn on when the load/rewind is completed.

successive characters is nominally measured greater than 900 μin.

(2) The timing between the first detected bit and the last detected bit of a character is nominally measured less than 425 μin.

4.4 Erase

4.4.1 Erase Direction. The tape shall be magnetized so that the rim end of the tape is a north-seeking pole.

4.4.2 Erase Width. The full width of the tape is dc erased in the direction specified in 4.4.1.

4.4.3 Erase Function. The erase function, whether by the write head or the erase head, shall ensure that the level of the read-back signal amplitude is below 4% of the Standard Reference Amplitude at 800 frpi.

4.5 Standard Reference Amplitude. The Standard Reference Amplitude is the average peak-to-peak output signal amplitude derived from the NBS Amplitude Reference Tape (SRM 3200) on a measurement system using the 800 CPI recording system with the recording current of 2.1 × I_r. The longitudinal recording pattern in the tracks to be tested shall be 10001000 (200 frpi). The signal amplitude shall be averaged over a minimum of 4000 consecutive flux reversals.

The Standard Reference Current (I_r) is the minimum current applied to the Amplitude Reference Tape which causes an output signal amplitude equal to 95% of the maximum output signal.

4.6 Signal Amplitude

4.6.1 Average Signal Amplitude. The average peak-to-peak output signal amplitude of an interchanged tape at 800 frpi shall deviate no more than + 15%, − 30% from the Standard Reference Amplitude. Averaging shall be done over a minimum of 4000 flux reversals.

4.6.2 Maximum Signal Amplitude. An interchanged tape shall contain no adjacent reversals whose peak-to-peak output signal amplitude exceeds 1.2 times the Standard Reference Amplitude.

4.6.3 Minimum Signal Amplitude. An interchanged tape shall contain no adjacent flux reversals whose peak-to-peak output signal amplitude is less than 0.35 times the Standard Reference Amplitude.

5. Format

See Fig. 2.

5.1 Track Format. The track format shall consist of nine parallel tracks.

5.2 Track Dimensions

5.2.1 Track width on tape is 0.043 inch minimum.

5.2.2 Centerline distance between tracks is 0.055 inch nominal.

5.2.3 Centerline of track 1 is to be 0.029 inch ± 0.003 inch from reference edge.

5.3 Reference Edge. The reference edge of the tape shall be the top edge when viewing the oxide-coated side of the tape with the rim end of the tape to the observer's right.

5.4 Track Identification. Tracks shall be numbered consecutively, beginning at the reference edge with track No. 1, and assigned as follows:

Track:	1	2	3	4	5	6	7	8	9
Environment:	E3	E1	E5	P	E6	E7	E8	E2	E4
Binary weight:	2^2	2^0	2^4	P	2^5	2^6	2^7	2^1	2^3
ASCII bits:	b_3	b_1	b_5	P	b_6	b_7	Z	b_2	b_4

5.4.1 Bits b_1-b_7 correspond to the bit assignments in ASCII.

5.4.2 Bit P is the parity bit. Character parity is odd.

5.4.3 Bit Z shall be zero and treated as a bit of higher order than the ASCII bits.

5.5 Block Length (See Fig. 2)

5.5.1 The data portion of a block shall contain a minimum of 18 ASCII characters. The Tape Mark is excluded from the minimum block length requirements (see 5.8).

5.5.2 The data portion of a block shall contain a maximum of 2048 ASCII characters.

5.6 Density Identification Area. The identification area shall be fully saturated in the erased direction. This area begins 1.3 inches minimum before the trailing edge of the BOT marker and extends to the initial gap.

5.7 Gaps (See Fig. 2)

5.7.1 Interblock Gap

(1) Nominal – 0.6 inch

(2) Minimum – 0.5 inch

(3) Maximum – 25 feet

(Gap depends upon the number of consecutive erase operations.)

5.7.2 Initial Gap. The gap between the trailing edge of the BOT marker and the first recorded character shall be 3 inches minimum, 25 feet maximum.

5.8 Tape Mark. The Tape Mark shall be a single character block consisting of the Device Control Character, DC3 ("1" bits in tracks 2, 3, and 8 only).

5.9 CRC Character. At the end of each tape block a character shall be written on tape for the possible recovery of single-track errors. This character shall be called the Cyclic Redundancy Check (CRC) character. In Tape Mark blocks, zero bits are written in all tracks for the CRC character.

5.9.1 Consider the contents of a 9-position register

to be C_1 to C_9 with the following track assignments:

Regular position:	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9
Track number:	4	7	6	5	3	9	1	8	2

5.9.2 The CRC character shall be derived as given in 5.9.2.1 through 5.9.2.5.

5.9.2.1 All data characters in the tape block are added to the CRC register without carry (each bit position is exclusive OR'ed to C_n).

5.9.2.2 Between additions, the CRC register is shifted one position C_1 to C_2, etc, and C_9 to C_1.

5.9.2.3 If shifting will cause C_1 to become "1," then the bits being shifted into positions C_4, C_5, C_6, and C_7 are inverted.

5.9.2.4 After the last data character has been added, the CRC register is shifted once more in accordance with 5.9.2.2 and 5.9.2.3.

5.9.2.5 To write the CRC character on tape, the contents of all positions except C_4 and C_6 are inverted. The parity of the CRC character will be odd, if the number of data characters within the block is even, and even, if the number of data characters within the block is odd. The CRC character may contain all zero bits, in which case the number of data characters was odd.

5.10 LRC Character. Following the CRC character a check character shall be written for the possible detection of read errors. This character shall be called the Longitudinal Redundancy Check (LRC) character. A longitudinal redundancy check bit is written in any track if the longitudinal count is otherwise odd.

6. Revision of American National Standard Referred to in This Document

When the following American National Standard referred to in this document is superseded by a revision approved by the American National Standards Institute, Inc, the revision shall apply:

American National Standard Code for Information Interchange, X3.4-1968