problem is to employ a process of repeated half addition (Exclusive OR) on the variables (see (6) for a complete discussion on parity generation).

As the data is always written from RWB 1, the first four Exclusive OR gates monitor the contents of RWB 1. The partial sums of the first two bit pairs are fed into the fifth Exclusive OR gate while the partial sums of the last two bit pairs are fed into the sixth Exclusive OR gate. The seventh Exclusive OR gate monitors the outputs of the 5th and 6th gates to obtain the half added result of the 8 data bits. The ninth gate half adds this result with the Parity bit of the Command Register such that the final result is the odd or even parity bit of the 8 data bits as specified by the Command Word. Whenever the CLOCK COUNTER reaches 3 the parity bit is strobed into a flip-flop from where it will be written onto the tape. It is worthwhile pointing out that writing occurs on every fourth MASTER CLOCK pulse and that the parity information is ready in the flip-flop one clock period before the actual writing. For all practical purposes this parity flip-flop can be considered to be an extension of the RWB 1. At this point it may be pointed out that a flip-flop is used to hold the parity bit instead of writing directly the output of the parity generator, because while writing the CRC character and the EOF character, the data parity generation circuits are bypassed; the appropriate characters (including parity) are loaded directly into the RWB 1 for writing on the tape.

5.8 Cyclic Redundancy Character Generation:

As mentioned previously, the Cyclic Redundancy Character Register is provided in the tape control for the CRC generation. This