

IBM COMPATIBLE 9-TRACK TAPE SYSTEM FOR THE PDP-8 COMPUTER

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in the
Department of Electrical Engineering
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by

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"IBM COMPATIBLE 9-TRACK TAPE SYSTEM FOR THE PDP-8 COMPUTER"

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M.Sc. Thesis presented to College of Graduate Studies

ABSTRACT

A control unit design to operate a 9-track tape system with a PDP-8 computer is described in detail. In addition to providing a local bulk storage facility, the tape system is designed to operate on IBM Compatible 800bpi tapes and hence information interchange with System 360 installations is possible. The formatting scheme is such that data transfers between the PDP-8 and the tape unit always take place as 12 bit parallel words. This not only means full use of the available memory space in the PDP-8, but also makes programming the tape system efficient and easier. An unique by-product of the formatting scheme is that the End-of-File Code is the only record with a single character as data on the tape. This makes it unnecessary to rely on the code read from the tape to identify the End-of-File and correspondingly the End-of-File detection logic is very simple.

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TABLE OF CONTENTS

	Page
Acknowledgements	iii
Abstract	iv
Table of Contents	v
List of Figures	viii
List of Tables	ix
List of Control Flow Charts	x
List of Engineering Drawings	xi
1. <u>INTRODUCTION</u>	1
2. <u>SOME RELEVANT TOPICS ON IBM COMPATIBLE DIGITAL RECORDING</u>	6
2.1 Writing and Reading the Magnetic Tape	6
2.2 Recording Methods	9
2.3 Data Records and Files	10
2.4 Beginning of Tape and End of Tape Markers	10
2.5 Write Lock Ring	13
2.6 Checking Tape Validity	13
2.6.1 Vertical parity	13
2.6.2 Longitudinal parity	14
2.6.3 Cyclic redundancy check	14
2.6.4 Writing LRC in NRZ recording	15
2.7 Self Clocking Data	15
3. <u>SYSTEM REQUIREMENTS</u>	17
3.1 Interface	17
3.2 Capacity	17
3.3 Density	18
3.4 Gap Generation	18
3.5 Data Transfer Format	18
3.6 Parity Generation and Error Checks	18
3.7 Starting and Stopping the Transports	20
3.8 Ready/Not Ready Conditions.	21

TABLE OF CONTENTS

	Page
3.9 Tape Operations	21
3.9.1 Read data	22
3.9.2 Write data	22
3.9.3 Read/Compare	22
3.9.4 Space forward	22
3.9.5 Space reverse	22
3.9.6 Rewind	22
3.9.7 Write EOF	23
3.10 Normal and Continuous Modes of Operations	23
4. PROGRAMMING THE MAGNETIC TAPE SYSTEM	24
4.1 Command Word Format	24
4.2 Status Word Format	24
4.3 Data Format	31
4.4 Tape Operations	33
4.4.1 Read data	35
4.4.2 Write data	37
4.4.3 Read/Compare	38
4.4.4 Spacing operations	40
4.4.5 Write End of File	41
4.4.6 Rewind	41
5. LOGICAL ORGANIZATION AND IMPLEMENTATION OF THE CONTROL UNIT	44
5.1 Major Functional Sub-units	44
5.2 Device Selector Logic	47
5.2.1 Read status and load command pulses.	47
5.2.2 Skip pulse generation	48
5.3 Command Register and Associated Control	49
5.4 Pinch Roller Control	50
5.5 Rewind Control	54
5.6 Read Clock and Data Clock Control	58
5.6.1 Suppressing the undesired data	61
5.6.2 Separating the desired data from the check characters	62
5.7 Read/Write Buffer and its Associated Control	65
5.7.1 Character counter	68
5.7.2 Clock counter and event counter	69
5.7.3 Read/Write buffer control signal generation	71
5.7.4 Vertical parity generation	75
5.8 Cyclic Redundancy Character Generation	77
5.8.1 CRC register	78
5.8.2 CRC register control signal generation	80

TABLE OF CONTENTS

	Page
5.9 Data Break Interface and Control	81
5.9.1 Data break interface	81
5.9.2 Break count flip-flop and its control	85
5.9.3 Data flag and its control	88
5.10 Read/Compare Control	93
5.11 Density and Clock Control	99
5.12 Write Control and Gap Generation	103
5.13 IRG Detection Control	106
5.14 Status Register and Associated Control	107
5.14.1 Illegal condition detection	107
5.14.2 Parity error detection	108
5.14.3 EOF detection	110
5.14.4 Rewind in progress condition	111
5.14.5 BOT and EOT marker detection	112
5.14.6 Error and Job Done flags	112
5.15 Writing EOF	116
5.16 Conclusions	117
6. <u>ENGINEERING DRAWINGS</u>	119
<u>REFERENCES</u>	148
<u>APPENDICES</u>	149
Appendix 1	150
Appendix 2	151
Appendix 3	154

LIST OF FIGURES

Figure Number	Title	Page
2.1	Typical Transport Layout	7
2.2	Nine Track Data Format	8
2.3	IRG and EOF Specifications	11
2.4	EOT and BOT Marker Specifications	12
4.1	Command Word Format	26
4.2	Status Word Foramt	28
4.3	Data Format Illustration: one 12 bit word written on the Tape	32
4.4	Data Format Illustration: two 12 bit words written on the Tape	34
5.1	Erase, Write and Read Head Locations when tape is at Load Point	60
5.2	RWB Control during Read	74
5.3	RWB Control during Write	76
5.4	CRC Register Control Timing	82
5.5	Data Break Transfer Interface: Block Diagram	84
5.6	Data Break and Break Count Flip-flop Timing	89

LIST OF TABLES

Table Number	Title	Page
4.1	Instruction List for PTC-1	25
4.2	Function and Density Codes	27
4.3	Status Bit Assignments	29
4.4	Programming Summary	42
5.1	Truth Table for Pinch Roller Control	53
A.1.1	MT-36 Tape Transport Specification	150
A.2.1	Transport Interface Signals	151
A.2.2	Data Electronics Interface Signals	152
A.3.1	Logic Signal Symbols	155

LIST OF CONTROL FLOW CHARTS

Flow Chart Number	Title	Page
5.1	Pinch Roller Control	55
5.2	Rewind Control	59
5.3	Data Clock Control	64
5.4	Data Flag Control during Read	94
5.5	Data Flag Control during Write	96
5.6	Read-Compare Control	100
5.7	Error Status Management	113

LIST OF ENGINEERING DRAWINGS

Drawing Number	Title	Page
6.1	Functional Block Diagram	119
6.2	Device Selectors	120
6.3	Command Register and Associated Control	121
6.4	Density Control Package	122
6.5	Function Decoding	123
6.6	Pinch Roller Control	124
6.7	Rewind Control	125
6.8	Read Clock and Data Clock Control	126
6.9	Read/Write Buffer	127
6.10	RWB Control Part I	128
6.11	RWB Control Part II	129
6.12	Write Events Decoder	130
6.13	WRT CLK and LRC Pulse Cable Driver	131
6.14	Parity Generator Package	132
6.15	IN-OUT Data MPXING	133
6.16	CRC Register	134
6.17	CRC Control	135
6.18	Data Break	136
6.19	RWB-MB Interface	137
6.20	BRK CNT Control	138
6.21	Data Flag	139

LIST OF ENGINEERING DRAWINGS

Drawing Number	Title	Page
6.22	Read/Compare Control	140
6.23	IRG Detection Control	141
6.24	Write Control and Gap Generators	142
6.25	Status Register	143
6.26	LRC Buffer	144
6.27	Illegal Condition Detection and Parity Error Control	145
6.28	Interrupt and Skip Gating	146
6.29	EOF Control	147

1. INTRODUCTION

Although it is only in recent years that magnetic recording has come into widespread general use, the invention is generally credited to Valdemar Poulsen, a Danish engineer who applied for a patent on a "Method of Recording Sound or Signals" in 1899.

The activities that heralded the definitive introduction of magnetic recording for data storage were started around 1947⁽⁸⁾. This was in direct response to the needs of the digital computers that were entering an explosive growth stage.

Digital magnetic recording is generally accomplished by magnetising small areas of ferromagnetic material deposited on a moving medium. Though media like drums and discs are widely used because of their unique advantages, magnetic tape has enjoyed extreme popularity for digital applications as a result of its economical mass storage characteristics⁽⁸⁾. Significant achievements have been made both in recording techniques and associated equipment since the introduction of tape recording for computer applications.

Data is stored on a tape as a number of bits recorded simultaneously across the width of the tape to form a "character" or "frame". Each bit location on the tape is called a "track". The storage capability of a tape system is usually expressed in terms of "storage density"; where the storage density is defined as the product of the number of tracks per inch (tpi) and characters per inch (cpi) and is

expressed in bits/sq. inch. The storage density in the earlier tape systems was about 1400 bits/sq. in., compared with the 14,000 bits/sq. inch available on recent tape systems.

Until recently, nearly all the computer manufacturers adopted their own tape formats in the absence of any accepted standards. These have ranged from 1/2 inch wide tapes with 7 tracks to 3 inch wide tapes with 36 tracks. However, only the format introduced by IBM which has 7 tracks on a 1/2 inch wide tape at recording densities of 200, 556 and 800 bpi, found widespread use. As a result of constant efforts to improve the recording densities, tape systems capable of handling 9 tracks on 1/2 inch wide tapes at 800 and 1,600 bpi have been developed⁽⁷⁾ and are now becoming widely accepted. Fortunately, a recent standard for 9 track recording has been proposed and it resembles very closely the IBM 9 track format.

The Automatic Cartographic System being developed for the Canadian Hydrographic Service is centered around the PDP-8, a small general purpose computer. This system has to organise, handle and maintain large amounts of data related to hydrographic charts and understandably a data bank on magnetic tape is planned for this purpose. Services of an IBM System 360 as a back-up computer, on those occasions when the capabilities of the PDP-8 are inefficient or inadequate, is also envisaged. In view of the economics and convenience, magnetic tape has been chosen as a communication medium between the PDP-8 and System 360 installations.

Though the data transfer rates from a tape unit are generally slow compared with the internal operating speeds of a computer, they are normally fast enough to make program controlled transfers inefficient. The PDP-8 as with many other contemporary machines has facilities to enable high speed peripheral equipment such as magnetic tape units to communicate directly with the core memory for transfers, without any program intervention on a cycle stealing basis. The very fact that these magnetic tape units communicate directly with the core memory points the need for a control unit located between them and the computer to synchronise the tape and computer operations.

The thesis describes such a control unit to operate an IBM compatible 9 track tape system with a PDP-8. In simple terms a tape control unit performs the following operations.

- a) Accepts data from the computer and transmits it to the tape.
- b) Transmits data from the tape to the computer.
- c) Executes the commands issued by the computer.
- d) Monitors the current status of the tape system and conveys it to the computer on demand.
- e) Checks the validity of the data before transmitting it to the computer.
- f) Encodes and decodes the data in terms of the tape recording and the computer requirements.

As a suitable commerical unit for the PDP-8 computer was not available, a project to develop the PTC-1, a 9 track tape control unit was initiated for use in the Automatic Cartographic System, with two

goals in mind:

- a) to provide communication facility with the System 360 installation, and
- b) to provide a convenient back up storage facility for the PDP-8.

As this project was nearing completion a suitable commercial unit was announced⁽³⁾ which could satisfy the first requirement but only partly fill the second need, in the sense that transfers between the computer and the tape take place as 8 bit parallel words, while the computer is a 12 bit parallel machine. This requires the program to preformat the data prior to writing on the tape, and post-format the data after obtaining it from the tape.

A tape control unit can be treated for all practical purposes as a special purpose computer and the same techniques used in digital logic system design are also applicable in this case. The exact requirements and organisation of a tape control unit depend to a large extent on the application of the tape system and on the computer it is intended to work with. For example, the requirements of a control unit to run an efficient back-up store alone would differ greatly from the one that is intended to provide compatibility with two different computer installations.

In the past few years digital magnetic tape recording has become a well organised discipline and this is shown by the attention given to this category of computer hardware in several special symposia.

Inclusion in such a general category as input-output equipment is no longer sufficient. The first comprehensive book on digital tape recording was published only in 1965⁽¹⁾. A second book⁽⁸⁾ followed in 1967 which covered both analogue and digital tape recording in considerable detail.

Though some attempt is made in the first book to introduce necessary concepts useful in modern tape control unit design, the amount of information published in other readily available literature is very limited because of its commercial and proprietary implications. This scarcity of published literature to some extent annoyed and motivated the writer to compile the necessary information and techniques for a tape control unit design. Although it is hard to support the claim by documented evidence, the tape control unit described in the following pages is believed to be unique because of the following features:

- a) Data transfers between the 9-track tape units and the PDP-8 always take place as 12 bit parallel words.
- b) The formatting scheme chosen makes it unnecessary to rely on the accuracy of code read for detecting the End of File.

2. SOME RELEVANT TOPICS ON IBM COMPATIBLE DIGITAL RECORDING

This chapter contains brief information useful in understanding some of the terms and concepts used in IBM compatible tape recording.

2.1 Writing and Reading the Magnetic Tape:

Figure 2.1 shows the layout of a typical digital tape transport. The tape supply reel is mounted on the upper motor spindle and the tape is threaded under the upper vacuum tank through the assemblies of EOT/BOT sensor, upper capstan/pinch roller, erase head, read/write head, lower capstan/pinch roller and over the lower vacuum tank. The free end is wrapped several times around the hub of the lower reel which serves as the take-up member. When the power is applied, a vacuum pump begins to exhaust air from the vacuum tanks drawing the tape into them to form loops. At the same time, photo-electric sensing circuits come into action to determine the location of the tape loop in each tank and drive the reel servos such that a nominal amount of tape is always maintained in these tanks. The tape loops act as buffers during rapid start/stop motions of the tape. They also act as a speed converter while the high inertia tape reels attain the running speed or continue to coast momentarily before stopping. Because the inertia associated with the tape loops in the vacuum tanks is small, acceleration and deceleration at a high rate are possible.

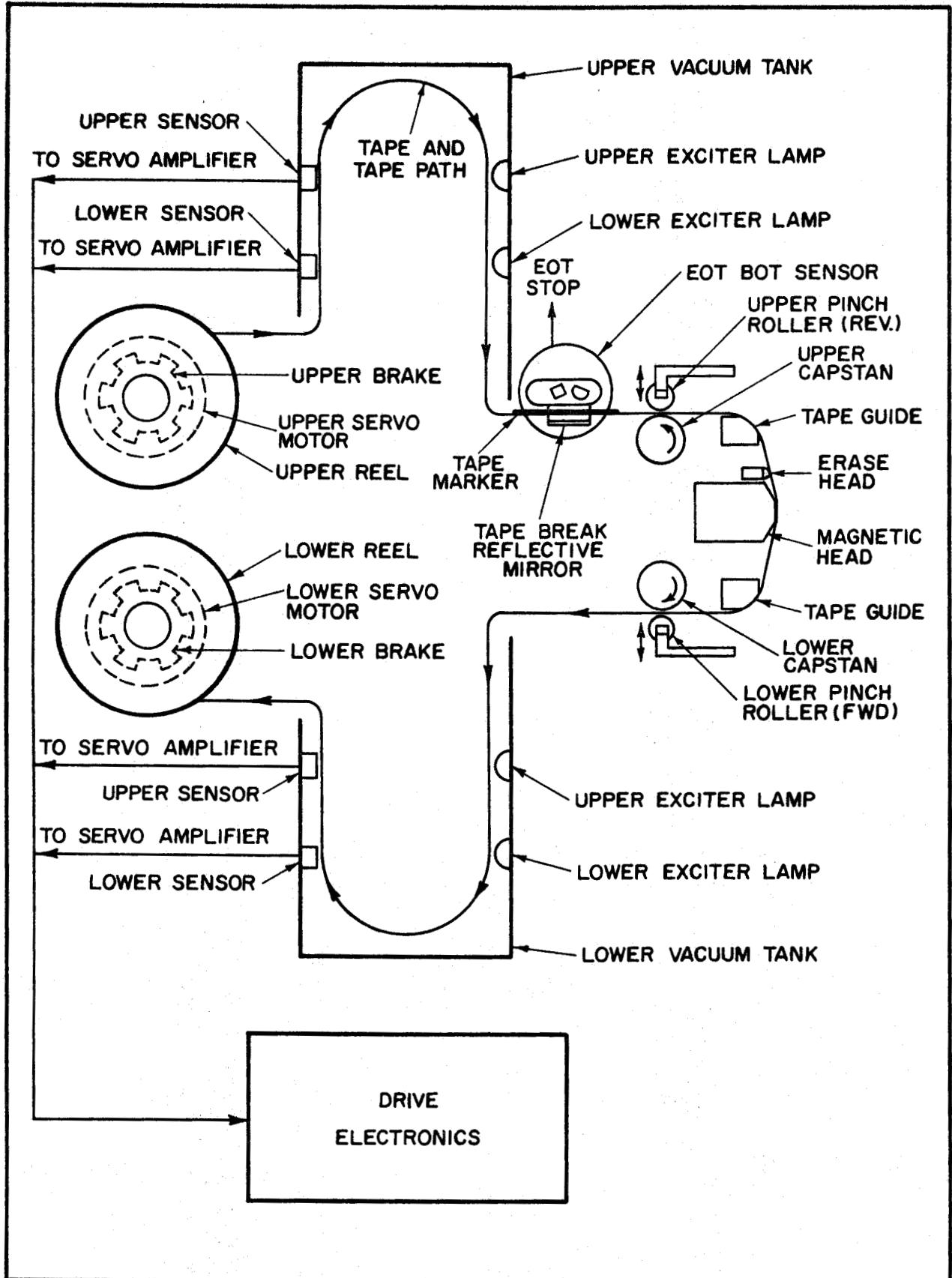


FIGURE 2.1 TYPICAL TRANSPORT LAYOUT

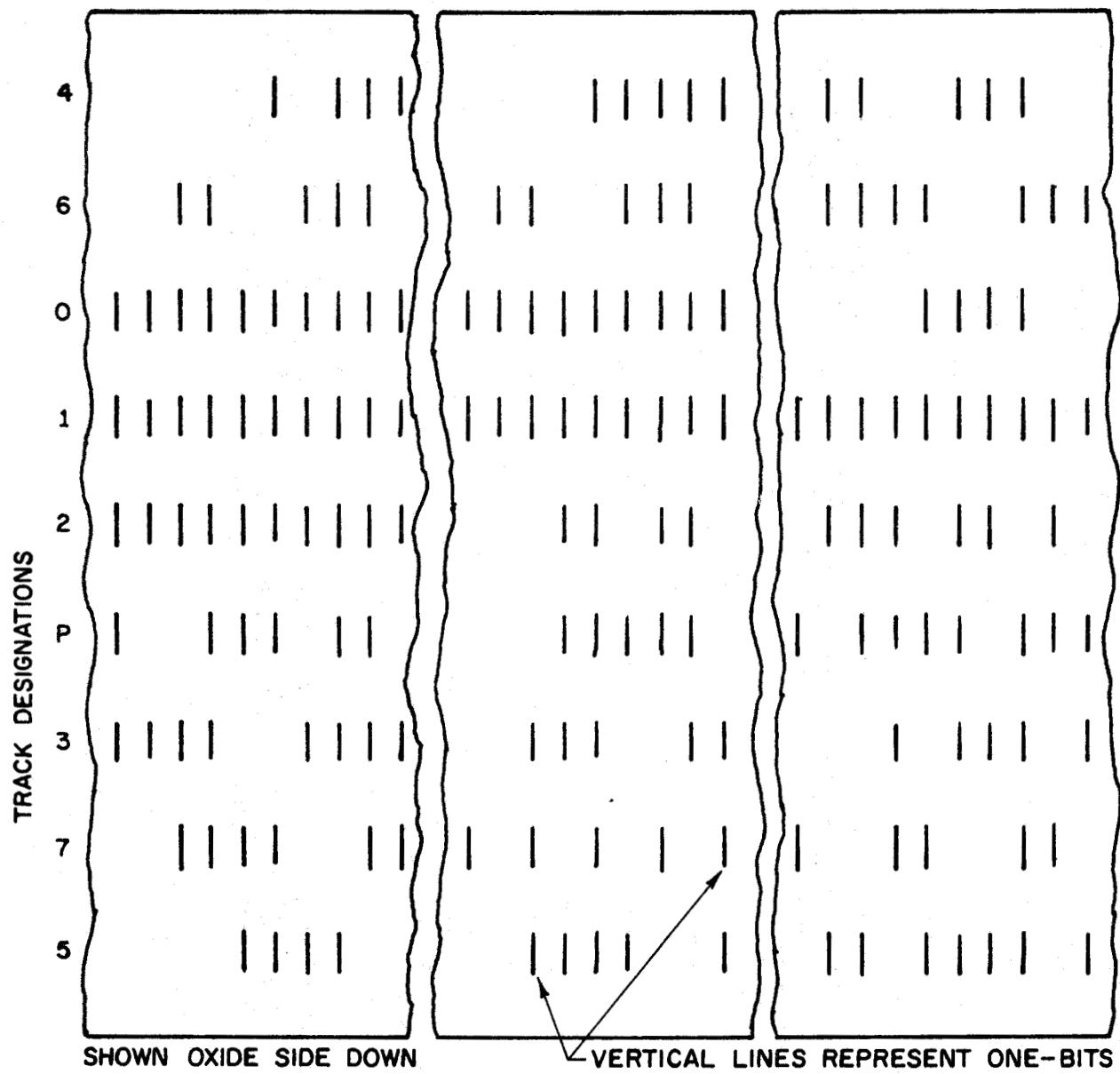


FIGURE 2.2 NINE-TRACK TAPE DATA FORMAT

Reading or writing occurs as the tape moves past the read/write head gaps. Writing is accomplished by magnetising small discrete areas of the tape in nine parallel tracks across the width using a head assembly with nine write gaps. During the read operation, these magnetised areas induce voltage in the read head which is representative of data on the tape. Before the tape reaches the read/write head assembly, it passes over the erase head. The erase head is excited only during write operations to erase any previous information on the tape.

The magnetised spots or bits in nine track positions constitute a character. In IBM 9-track format, eight tracks contain data bits and the other track carries the vertical parity information (see section 2.6.1). Figure 2.2, shows track designations for IBM compatibility on a 1/2 inch wide tape.

2.2 Recording Methods:

There are a number of recording methods proposed for digital applications⁽¹⁾. However, only Non-Return to Zero (NRZ) and Phase Encoding (PE) methods are widely used. IBM compatible 800 bpi tapes require the NRZ method of recording.

In the NRZ method enough current always flows through the write winding to saturate the tape. Whenever a binary '1' is to be written, the write current direction is reversed. Hence in this method, flux reversal of either polarity represents a '1' and absence of such reversal a '0'.

The NRZ method of recording can readily be implemented using a complementing flip-flop. The write winding is connected through appropriate buffering across the outputs of the flip-flop, which can be complemented every time a '1' is to be written; thus reversing the direction of current flow in the write head (see section 2.6.4).

2.3 Data Records and Files:

Data is stored as a series of characters along the length of a tape. A collection of characters logically grouped together constitute a record. These records are separated from each other by a length of blank tape, called the Inter Record Gap (IRG). The length of a record may vary depending on the data storage requirements.

A file consists of a number of records. It is possible to arrange more than one file on a reel of tape. Files are separated from one another by a special record called End of File (EOF). Figure 2.3 shows the IRG and EOF format specifications for IBM compatibility.

2.4 Beginning of Tape and End of Tape Markers:

Magnetic tape must have some blank tape at the beginning and end to allow threading through the transport. Small optically reflective strips called markers are placed on the base (uncoated) side of the tape to identify the Beginning of Tape (BOT) and End of Tape (EOT) areas. Digital tape transports in general are equipped with a lamp-photocell arrangement to sense these markers. Figure 2.4 shows locations of the tape markers on an IBM compatible tape.

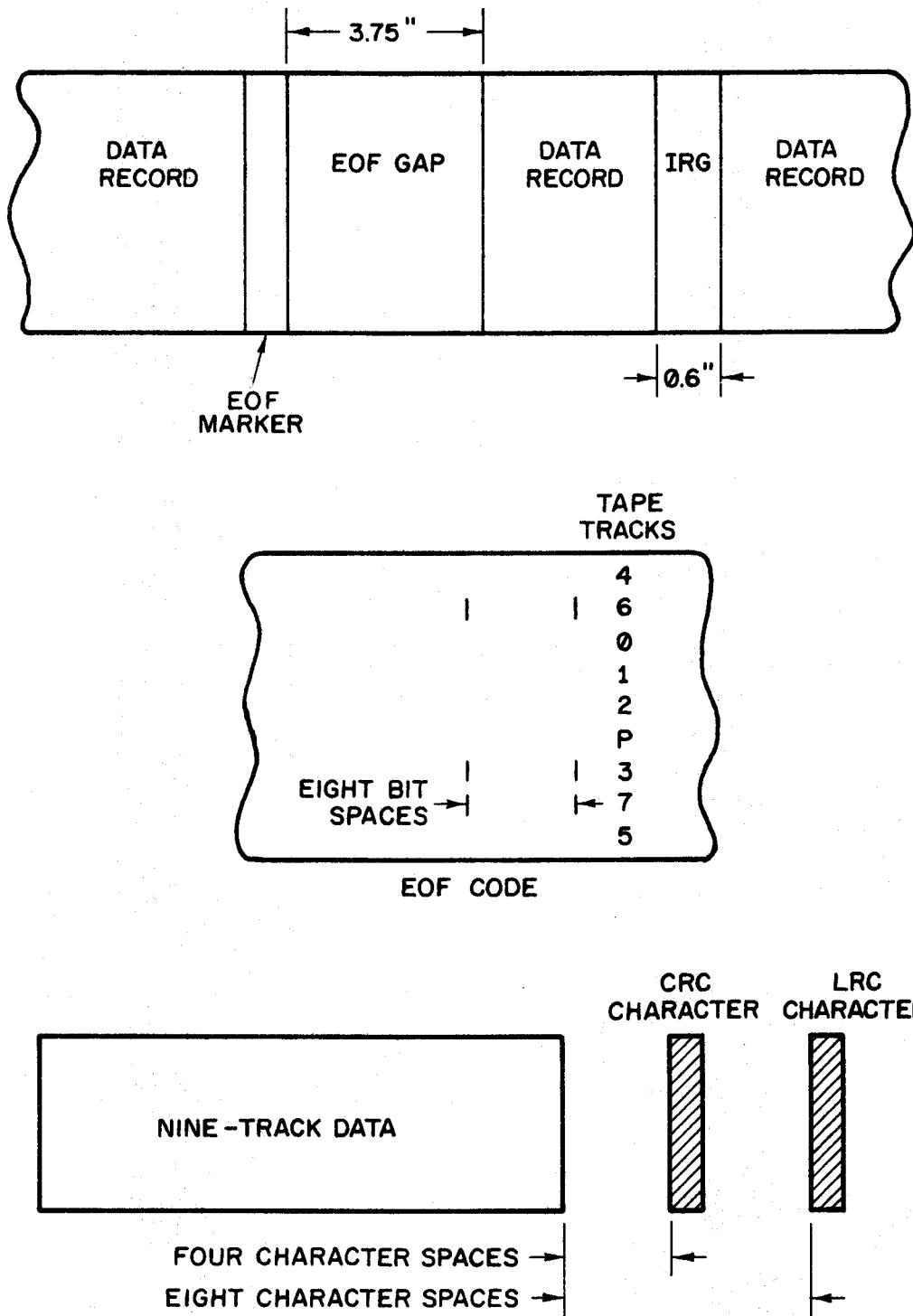


FIGURE 2.3 IRG & EOF SPECIFICATIONS

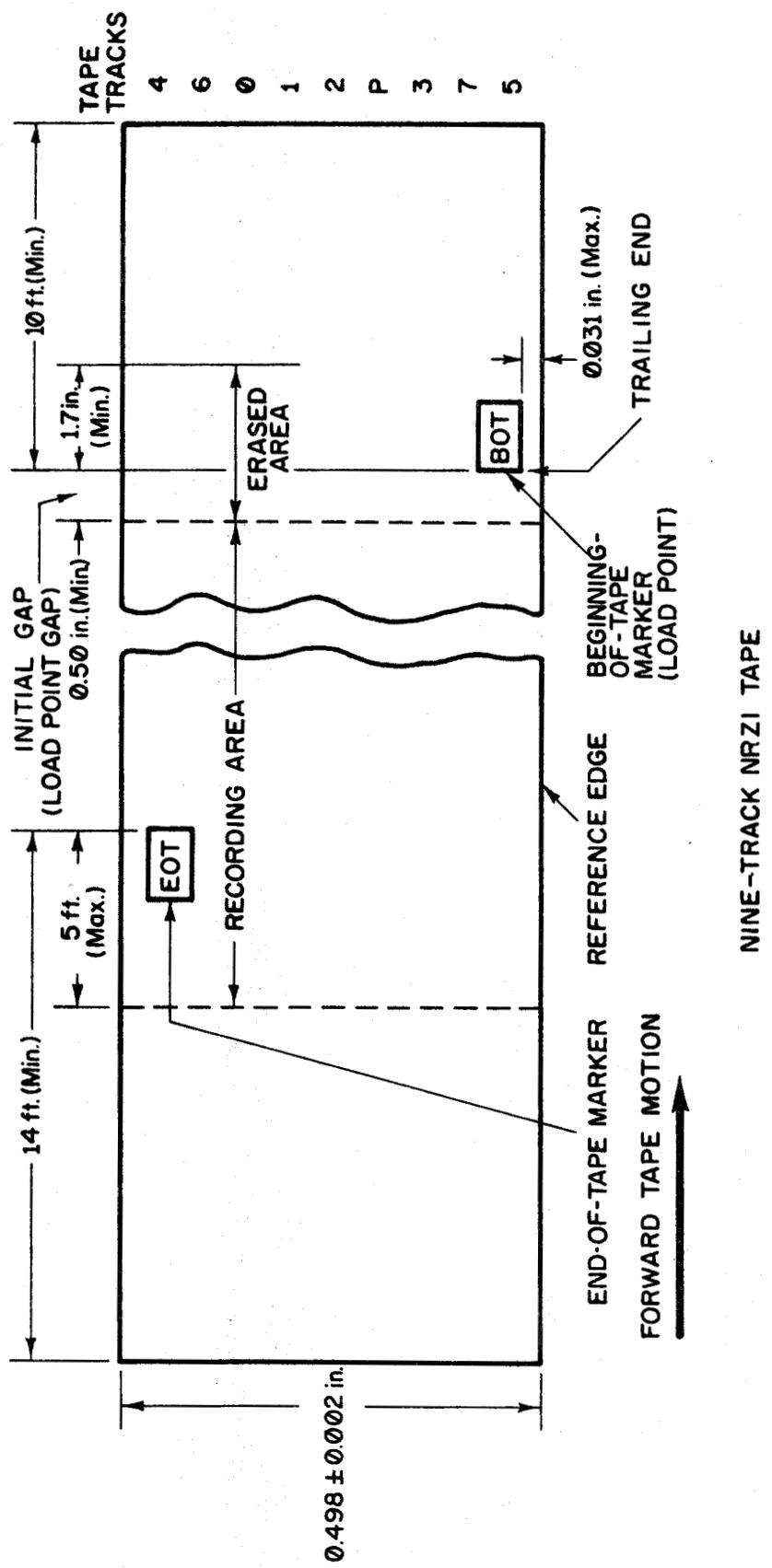


FIGURE 2.4 EOT AND BOT MARKER SPECIFICATIONS

2.5 Write Lock Ring:

Because a write operation always erases previous information on the tape, all IBM compatible tape reels are provided with a Write Lock Ring or File Protect to prevent accidental erasures. This plastic ring fits into a groove moulded into the reel carrying the tape. All IBM reel compatible transports are equipped to sense the presence of this ring. When not in place, the write circuits cannot be energized.

2.6 Checking Tape Validity:

Though the highest possible regard is paid to the materials and equipment used in digital recording, their operation is not always perfect, and errors still do occur. There are several possible methods for detecting and correcting errors in digital systems⁽⁹⁾. On nine track 800 bpi tape systems IBM uses parity and Cyclic Redundancy Checks (CRC) for detecting and correcting errors⁽⁷⁾.

2.6.1 Vertical parity

The vertical parity or vertical redundancy provides a means of checking for the proper number of '1' bits in each character. The parity track carries information about the total number (odd or even) of 1's in that character. During a read operation, the parity is calculated from the 8 data bits obtained from the tape and checked against the parity bit as read from the tape. Provided they agree, the character read is assumed correct.

2.6.2 Longitudinal parity

The vertical parity check inherently lacks the capability of error correction, because it cannot identify the track in which an error has occurred. However, if it is given some means of locating the error in the second magnetic dimension, some degree of correction can be achieved. This is accomplished in IBM format using a Longitudinal parity or Longitudinal Redundancy (LRC) character. A longitudinal parity check involves monitoring all tracks to ensure the presence of an even number of 1's in each track of a record. Figure 2.3 shows the location of the LRC in a record.

2.6.3 Cyclic redundancy check

In IBM 9-track format the Cyclic Redundancy Check (CRC) scheme is used to correct single track read errors. As a record is written, a special check character (CRC) is calculated automatically from the data characters. The CRC character is written after the body of the record (expecting EOF) and before the LRC character (see Figure 2.3). During a read operation, the CRC character is again calculated and compared with the written CRC character. If they disagree, a CRC error is indicated, and an error pattern character is calculated using the vertical parity indications and their positions within the record. Single track errors may be corrected by implementing an error correcting routine; multiple track errors cannot be corrected.

2.6.4 Writing LRC in NRZ recording

In section 2.2 it was mentioned that NRZ recording can be readily implemented using a complementing flip-flop. This also provides an easy way for generating and writing LRC on the tape. If a flip-flop was initially '0' and complemented every time a '1' is written, the total number (odd or even) of 1's written can be assessed by its final state; if the total number of times complemented is even, the flip-flop will contain a '0', otherwise a '1'. As the LRC is a count of the number of 1's in a record, it can be written on to the tape simply by resetting all the write flip-flops, to make the total number of 1's (including the LRC) along each track even.

2.7 Self Clocking Data:

In order to facilitate interchange of tapes inspite of small variations from unit to unit in packing density and speed, digital tape systems employ some form of clocking scheme to locate the characters on the tape. Three types of clocking schemes are in wide use:

- a) systems having a separate clock track recorded along with the information tracks,
- b) systems using NRZ recording but having no separate clock track, and
- c) systems which are independently self clocking in each recorded track.

IBM 800 bpi tape units employ the second system despite the fact that the NRZ method of recording is inherently not self clocking, because by adopting the convention of excluding "all-zero" codes (parity bit included) character timing reference points can be established during

a read operation. It is important to note that with data alone, an "all-zero" LRC character can occur (see 2.6.2). However, the rules for calculating CRC (see section 5.8) take this condition into account and are formulated so that an "all-zero" LRC character will never result.

3. SYSTEM REQUIREMENTS

The first step to take in any complex logic system design is to establish the exact system requirements or performance specifications to achieve the desired final result. These serve a useful purpose apart from formally stating the objectives. For convenience, the system is usually divided for synthesis, into logical subsystems of manageable size. When complete, these subsystems are integrated to obtain the total system. A study of the system requirements in general helps the designer in arriving at suitable subsystem configurations. This chapter is used to formally specify the requirements for the tape control unit.

3.1 Interface:

The control unit shall interface with a PDP-8 computer (manufactured by Digital Equipment Corporation) and MT-36 tape transports fitted with MA315-4 data electronics (manufactured by Potter Instruments Company). It is designated as Type PTC-1 for convenient future referencing.

The 3 cycle data break facility of the PDP-8 is to be used for data transfers into and out of the computer.

3.2 Capacity:

The control shall be capable of handling two program selectable tape transports. Though it should handle two units, data trans-

fers may be taking place from only one unit at any given time.

3.3 Density:

Because the tape units selected are equipped to handle nine track tapes at 200, 556 and 800 bpi, the control unit shall be designed to operate at all these three densities. However, IBM compatibility demands only 800 bpi. The normal tape speed will be 50 inches per second.

3.4 Gap Generation:

The control unit shall be capable of generating all the necessary gaps automatically to produce IBM compatible tapes (see Figure 2.3).

3.5 Data Transfer Format:

Data transfers between the computer and the control unit shall always be as 12 bit parallel words. The control should be capable of unpacking 12 bit words to write as 8 bit tape characters and pack 8 bit tape characters into 12 bit words.

3.6 Parity Generation and Error Checks:

The control shall be capable of writing and reading data with even or odd vertical parity. The desired parity will be selected by program.

As the MA315-4 unit is equipped with a vertical parity checking circuit, the control need not generate parity for the characters read from the tape for checking; it is sufficient if it can accept the "Parity Indication" signal furnished by the MA315-4 and in the event of an error to inform the computer.

The control unit need not generate the LRC character for writing on the tape. The write amplifiers can be made to do this by pulsing the "Compensated Reset" line of the MA315-4 when the LRC character is to be written (refer to section 2.6.4).

Though the control unit is not responsible for checking the vertical parity for the characters read from the tape, the task of checking the longitudinal parity is assigned to the control unit. If an error occurs the control should be capable of conveying this fact to the computer.

The control unit shall generate the CRC character to be written on the tape. This is required only for IBM format compatibility and no error correcting schemes are contemplated in the PDP-8 computer.

Like many other contemporary units, the MT-36 transports are equipped with dual gap (separate read and write gaps) heads. The character just written can be echoed using the read gaps during a write operation. The control need not compare the data with the echo; it is sufficient to monitor the "Parity Indication" line for possible parity errors during a write operation. If there is no parity error in the echo, the character will be assumed to be written correctly.

Because the check characters (LRC and CRC) are calculated from the bit patterns of the data characters, the vertical parity of these characters may not necessarily comply with the specified parity for the data. The control should take this into account and suppress the parity error indications due to vertical parity failure when dealing with the check characters.

3.7 Starting and Stopping the Transports:

On account of the finite times taken to start and stop the tape, it is not permitted to stop during normal tape operations except in the Inter Record Gaps.

After a rewind, the tape shall stop on the BOT marker. Local control in the MT-36 transport automatically terminates the rewind when the BOT marker is sensed. However, as the rewinding is done at a high speed, the tape cannot stop exactly on the BOT marker but over runs it before coming to a halt. The control unit shall position the tape back on the marker before the rewind operation is assumed complete.

When under program control, the transport should not halt immediately on sensing the EOT marker. There is usually enough tape left beyond the EOT marker to complete the current operation. The control unit shall remember the fact that the EOT has been sensed to request program attention upon completion of the current operation.

The control unit shall not allow the transport to start if an error from a previous operation has not been attended to by the program.

Any attempt by a program to initiate any tape operation involving motion in the reverse direction when the tape is at the BOT shall not be allowed to succeed. The control unit is expected to raise an error flag to inform the program that the selected operation is illegal.

3.8 Ready/Not Ready Conditions:

The tape system is not expected to accept and implement commands at all times. This might arise due to the control being busy or the transports being physically unable to implement them.

To initiate a new tape function on the control, a previously selected operation in progress must be completed. It is the responsibility of the control unit to see that this is not violated. Facilities shall be provided to see if it is ready to initiate a new operation.

Facilities shall also be provided to interrogate the control to find if the selected transport is capable of accepting commands. The transport cannot accept commands if the power to the transport is not switched on, the mode control switch on the transports is left in "Manual" position (possibly after loading the tape) or the vacuum has collapsed either due to a fault or in preparation for a high speed rewind.

Should any program insist on issuing a command under system "Not Ready" condition, the control shall protest by setting an error status. Issuing such illegal commands should not interfere with any tape operation that may be in progress.

3.9 Tape Operations:

The tape control unit shall provide the following operations and the computer is to be informed after completion:

1. Read Data

The control unit reads data from the tape, assembles it as a 12 bit word and transfers these words into a computer. The program specifies the number of words required to be read and the locations they should go into in the core memory.

2. Write Data

The control obtains data from the program specified core locations and writes on the tape as 8 bit data characters.

3. Read/Compare

The control reads data from the tape and compares with the data in specified core locations. If there is a discrepancy, the control raises a Read/Compare Failed status.

4. Space Forward

The control unit advances the tape in the forward direction for a specified number of records. No data transfers occur during the spacing operation and encountering an EOF marker terminates it.

5. Space Reverse

This operation is very similar to Space Forward; except that the spacing is done in the reverse direction. Encountering the BOT marker or EOF code during a space reverse terminates the operation.

6. Rewind

This operation rewinds the tape at a high speed to position the tape on the BOT marker.

7. Write EOF

When this operation is selected, the control unit writes the appropriate EOF code on the tape (refer to section 2.3).

3,10 Normal and Continuous Modes of Operation:

The control unit shall provide facilities to operate the tape system in two modes: (a) Normal Mode (NM), and (b) Continuous Mode (CM). Normal Mode is used whenever operating the system on one record at a time basis. In this mode the tape is stopped at the end of each record, whereas in CM the tape is allowed to run through the IRG to avoid start-stop delays after each record.

4. PROGRAMMING THE MAGNETIC TAPE SYSTEM

From a study of the system requirements, the instructions necessary to program the PDP-8 for PTC-1 are classified into the following three categories.

- a) Skip instructions to interrogate the status of the tape system.
- b) Command instructions to initiate a desired operation.
- c) Read status instructions to analyze the type of error, if any, after completion of an operation.

Table 4.1 lists the instructions provided to operate the tape system.

4.1 Command Word Format:

To conserve the number of input-output (IOT) instructions, all the necessary information for a tape operation is transferred from the accumulator (AC) of the computer into the control unit as a command word. Figure 4.1 shows the command word format containing the tape unit number, desired mode, function, density and parity information. The command word is decoded in the control as shown in Table 4.2 to obtain the desired function and density.

4.2 Status Word Format:

All the status information is encoded by the control as one status word which can be transferred into the accumulator on demand. Figure 4.2 shows the status word format. Table 4.3 lists the status bit assignments for the status word.

TABLE 4.1 INSTRUCTION LIST FOR PTC-1

Mnemonic	Octal Code	Operation
MTSF	6701	Skip on error flag or job done flag. This instruction samples the status of the error and job done flags. If either (or both) is set the contents of the program counter (PC) is incremented once to skip the next sequential instruction.
MTCR	6711	Skip on tape control Ready. This instruction causes the program counter to be incremented once, if the tape control is ready to accept a command.
MTTR	6721	Skip on selected tape transport Ready. This instruction causes the next sequential instruction in the program to be skipped if the selected transport is ready.
MTAF	6712	Clear command and status registers.
MTCW	6714	The contents of the accumulator are exclusively OR'ed into the command register (see command word format).
MTLC	6716	Load command register. This instruction is a combination of the previous two instructions. This instruction <u>clears</u> the command and status registers and <u>transfers</u> contents of the accumulator into the command register.
MTGO	6722	This GO instruction initiates the operation as indicated by the command register, if the command is legal.
MTRC	6724	Inclusive OR of the command register into the accumulator. If the accumulator was clear prior to this instruction, the accumulator will hold the command register contents after execution of this instruction.
MTSR	6704	Inclusive OR of the status register into the accumulator. If the accumulator was clear before issuing this instruction, this instruction loads the status register into the accumulator.
MTCM	6702	This change Mode command always sets the mode bit in the command bit to the Normal mode.

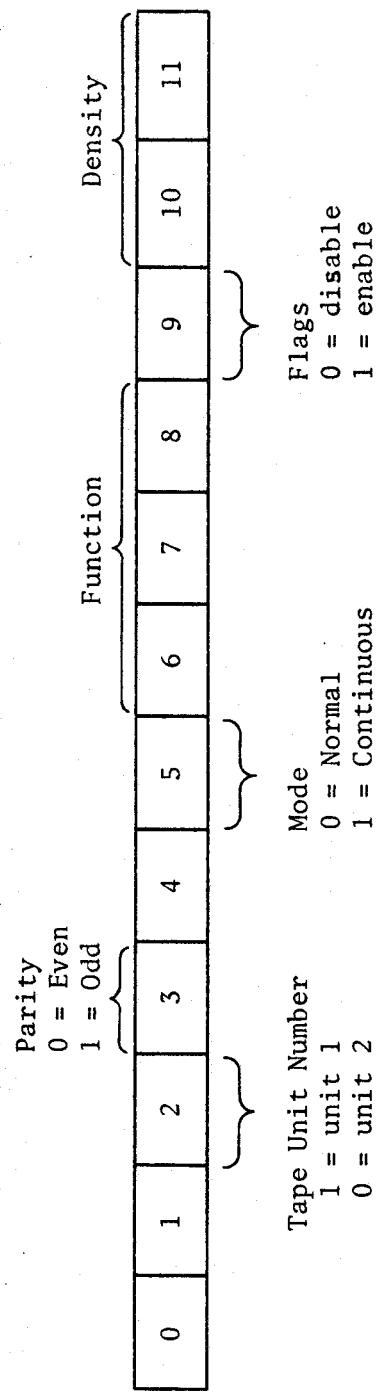


Figure 4.1: Command Word Format

TABLE 4.2 FUNCTION AND DENSITY CODES

FUNCTION	Bits			DENSITY	Bits	
	6	7	8		10	11
No operation	0	0	0	200 BPI	0	0
Rewind	0	0	1	556 BPI	0	1
Read	0	1	0	800 BPI	1	0
Read/Compare	0	1	1	Not used	1	1
Write	1	0	0			
Write EOF	1	0	1			
Space Forward	1	1	0			
Space Reverse	1	1	1			

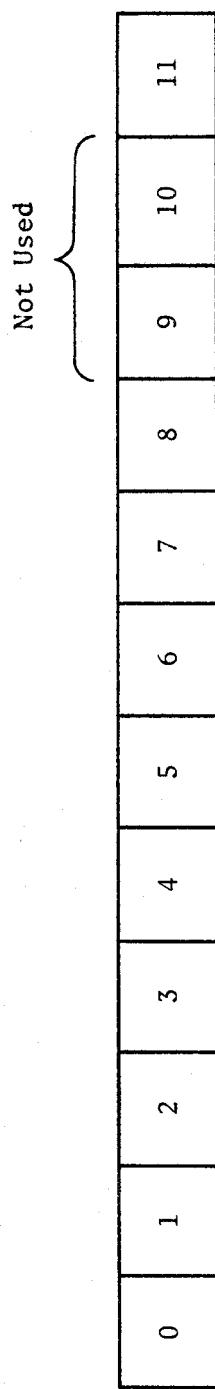


Figure 4.2: Status Word Format

TABLE 4.3 STATUS BIT ASSIGNMENTS

Bit	
0	Error Flag. This flag is set whenever the operation is not successfully completed. However, if the function selected is illegal, this flag is set without initiating the operation.
1	Tape Rewinding. This bit is set whenever a Rewind command has been issued to the control and the function is in progress.
2	Beginning of Tape (BOT). This bit is set whenever the reflective BOT marker is sensed.
3	Illegal Command. This bit is set whenever an illegal operation is selected. The following are illegal: (a) Command issued when control is not ready. (b) Trying to initiate an operation on a tape unit which is not ready. (c) Attempting to write without Write Lock Ring in position. (d) Trying to execute a Space Reverse or Rewind operation when the tape is at BOT. (e) Trying to initiate an operation with status register uncleared from a previous error condition. (f) Specifying an unused code in the command register.
4	Parity Error. This bit is set whenever there is a parity error detected. Both vertical and horizontal parity failures can set this bit. The program cannot identify which parity failure has occurred. However, the operator can determine if a horizontal parity failure has occurred by examining the control panel indicators.
5	End of File (EOF). This bit is set whenever an EOF code is encountered as a single character record by the control. This can happen during all valid tape functions; except Rewind, Write or Write EOF.
6	End of Tape (EOT). End of Tape detection occurs during any forward command and this bit is set whenever EOT is sensed. Sensing EOT does not terminate the function in progress.
7	Read/Compare Failure. When a Read/Compare function is selected, data from the tape is compared with data in the core. Should any time the comparison disagree this status bit is set.

Table 4.3 continued

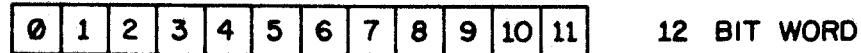
Bit	
8	Not used.
9	Not used.
10	Not used.
11	Job Done Flag. This bit is set whenever a desired operation has been completed successfully.

4.3 Data Format:

According to the system requirements (refer to section 3.5), the transfers between the PDP-8 and the tape are to be as 12 bit parallel words. As a 9-track tape has only 8 data bits in a character, the control has to assemble data from more than one character into a 12 bit word before transfer. Similarly while writing, the control must unpack 12 bit words received from the computer to form 8 bit data characters. The following observations can be made when formatting 12 bit words into 8 bit tape characters:

1. The smallest amount of data that can be written on the tape from the computer is never less than two characters. This is obvious because the smallest amount of data information the computer transmits is a 12 bit word which takes more than one character space on the tape.
2. Whenever a record to be written contains an even number of computer words, the number of characters in that record will be a multiple of three.
3. Whenever a record to be written contains an odd number of computer words, the formatting results in a fractional last character.

Figure 4.3 illustrates the format on the tape when one 12 bit word is written. The most significant 8 bits of the data word appear on the tape as the first character. The remaining 4 bits occupy half of the second character on the tape. To fill up the remaining 4 bit positions in the second character, the control inserts zeros. When these two characters are read from the tape the zeros inserted by the control are not transferred into the computer.



	FIRST CHARACTER	SECOND CHARACTER
TRACK 4	4	*
TRACK 6	6	*
TRACK 0	0	8
TRACK 1	1	9
TRACK 2	2	10
TRACK P	P	P
TRACK 3	3	11
TRACK 7	7	*
TRACK 5	5	*

* CONTROL INSERTS ZEROS IN THESE POSITIONS

FIGURE 4.3 DATA FORMAT ILLUSTRATION :
ONE 12 BIT WORD WRITTEN ON THE TAPE

Figure 4.4 illustrates the format when two 12 bit words are written on to the tape. The most significant 8 bits from the first data word form the first tape character, while the remaining 4 bits of the first data word and the most significant 4 bits of the second data word form the second tape character. The third character on the tape contains the remaining 8 bits of the second data word. During a read operation, the control assembles these three characters into two 12 bit words in the same order.

The formatting scheme just described can be extended to any number of 12 bit words. If "n" number of 12 bit words are to be written as a record, the number "N" of tape characters generated by the control can be expressed by the following relations:

$$N = \frac{3n}{2} \quad n \text{ is even} \quad \dots (4.1)$$

$$N = \frac{3(n - 1)}{2} + 2 \quad n \text{ is odd} \quad \dots (4.2)$$

4.4 Tape Operations:

The tape control PTC-1 is capable of implementing the following operations on selected tape unit according to the bit patterns of the function bits in the command word (see Table 4.2). The following is a detailed description of the functions.

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11
----	----	----	----	----	----	----	----	----	----	-----	-----

1 st. 12 BIT WORD

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
----	----	----	----	----	----	----	----	----	----	-----	-----

2nd. 12 BIT WORD

	FIRST CHARACTER	SECOND CHARACTER	THIRD CHARACTER
TRACK 4	A4	B0	B8
TRACK 6	A6	B2	B10
TRACK 0	A0	A8	B4
TRACK 1	A1	A9	B5
TRACK 2	A2	A10	B6
TRACK P	P	P	P
TRACK 3	A3	A11	B7
TRACK 7	A7	B3	B11
TRACK 5	A5	B1	B9

FIGURE 4.4 DATA FORMAT ILLUSTRATION:
TWO 12 BIT WORDS WRITTEN ON THE TAPE

4.4.1 Read data

Data may be read on the PTC-1 for transfers into the computer only in the forward direction. It is required that both Current Address (CA) and Word Count (WC) registers located in the core memory of the computer be loaded prior to initiating this function. For reading data, the CA is loaded with $(SA - 1)$ where SA is the starting address of the location into which the first data word assembled by the tape control is to be transferred. The WC is loaded with the 2's complement of the number of words to be transferred. The PTC-1 uses locations $(7752)_8$ and $(7753)_8$ in the core memory as WC and CA respectively. Before each transfer, the contents of the CA are incremented by one by the data break control circuits in the PDP-8. This facilitates the loading of successive words assembled by the tape control into consecutive core locations starting from SA. After each transfer, the contents of WC are also incremented by one. The control circuits in the PDP-8 provide a "Word Count Overflow" signal when the WC reaches zero to indicate that the required number of transfers have been completed. The tape control uses this signal to inhibit further transfers.

Reading of data can be accomplished in two modes: (a) Normal, and (b) Continuous. The desired mode is specified by bit 5 in the command word (see Figure 4.1).

(a) Normal Mode (NM).

In the NM, data from one record on the tape is read by the control and the transport is halted in the IRG. Though a complete record is read from the tape, the number of words transferred into

the computer is determined by the WC. If the WC is set to less than the number of words (not characters) in a record, transfers occur only until the WC reaches zero. On the other hand, setting the WC to equal or more than the number of words in the record, a complete record will be transferred before the transport is halted. In the former case the control reads the complete record for checking the longitudinal parity and stopping the transport in the IRG.

During the read operation, every character (except the check characters) is checked for vertical parity failure. If there is an error, the "Parity Error" bit in the status word is set (see Table 4.3). When the tape reaches the IRG, the status word is checked by the control to see if any error has occurred in the record just read. If so the Error Flag (bit 0 in the status word) is set; if not the reading is successful and the Job Done (bit 11 in the status word) is set. Whether the operation is successful or not, the transport halts in the IRG. If the flags are Enabled (bit 9 in the command word is '1'), either flag can cause a program interrupt.

(b) Continuous Mode (CM).

Whenever more than one record is to be transferred into the computer, reading in CM eliminates the intermediate start-stop delays as the transport is not halted at the end of each record. The control will set the Job Done flag after reading one record but the transport is allowed to run. The program can reset the WC and CA registers as desired and issue a MTGO instruction to transfer the next record. The

program is expected to change the Mode bit (bit 5 in the command word) to NM using a MTCM instruction before the last desired record transfer is completed. When the control accomplishes the last record transfer, the transport will be stopped in the IRG with the Job Done flag set as usual. In the event of an error during Read Continuous Mode of operation, the transport will stop in the IRG at the end of the record in which the error has occurred, with the Error Flag set in the status word.

4.4.2 Write data

Writing data on the PTC-1 may be achieved only in the forward direction. This operation also requires the setting of CA and WC registers prior to its initiation. The CA is loaded again with (SA - 1) where SA this time is the address of the location from which the control will obtain the first data word in the core. The WC is loaded with the 2's complement of the number of words to be written. The control obtains data from consecutive locations starting from SA and writes as one record until the WC reaches zero.

As in the case of reading data, writing of data can also be accomplished in two modes.

(a) Normal Mode.

In this mode words are transferred from the computer into the control until the WC reaches zero. The control inserts the computed Cyclic Redundancy Check and Longitudinal Redundancy Check characters after the data characters and stops the transport. If there are no

errors detected in the data written (characters are echo-checked during write), the Job Done flag will be set, otherwise the transport will stop with the Error Flag and Parity Error bits set in the status word.

(b) Continuous Mode.

Writing in Continuous Mode is useful if the data is to be written as more than one record without encountering the start-stop delays in the intermediate records. After completion of writing one record, the control will set the Job Done flag but leave the transport running. The program can reset the WC and CA registers as desired for the next record and issue a MTGO instruction. At some time during the last record, the program must change the mode to Normal Mode using a MTCM instruction. After finishing the last record, the transport will halt with the Job Done flag set. If there is an error during Write Continuous Mode of operation, the control stops the tape after the record in which the error has occurred with the appropriate flags set in the status word.

4.4.3 Read/Compare

The Read/Compare operation facilitates the comparison of data on a tape with that in specified core locations for equality, with minimal programming assistance.

As in the case of read or write operations, Read/Compare can be accomplished only in the forward direction. It also requires the proper setting of the CA and WC registers prior to initiation.

The CA is again loaded with (SA - 1), where SA is the address of the location in which the first data word for comparison is stored. The WC is loaded with the 2's complement of the number of comparisons required.

The control assembles the first 12 bit word from the tape and checks against the first data word in the core for equality. If they match, it proceeds to the next consecutive word. If the data on the tape disagrees with a corresponding word in the core, the comparison is immediately discontinued. The tape, however, proceeds to the IRG for longitudinal parity checking and stops with the error flag and Read/Compare Failed (bit 7) set in the status word. Since the comparison is discontinued immediately after a failure, examining the contents of the CA will reveal the address of the word where the first failure has occurred. As no actual transfers occur into the core or on to the tape during Read/Compare operation, data is left undisturbed in both these places.

Read/Compare operation can be accomplished in two modes.

(a) Normal Mode.

In this mode an attempt is made to compare data from only one record. However, if the WC is set to less than the number of words in a record, comparison will take place only until the WC reaches zero. The transport will be stopped in the IRG irrespective of the WC. If the operation is successful the Job Done flag will be set, otherwise the Error flag and the corresponding status bits are set.

(b) Continuous Mode.

Read/Compare in Continuous Mode facilitates comparison of more than one record without stopping the transport in the intermediate Inter Record Gaps. After each record the control sets the Job Done flag and leaves the transport running. The program can issue a MTGO instruction after resetting the CA and WC registers as desired to continue comparison. To terminate this operation, the program must change the Mode bit in the command word using a MTCM instruction before the end of the last record. If there is an error during the continuous mode of operation, the transport will halt at the end of the record in which the error has occurred.

4.4.4 Spacing operations

To position the tape in a desired record, two functions, Space Forward and Space Reverse are provided in the tape system. In either of these two operations data transfers do not occur and hence setting of the CA is not necessary. However, the program must declare the number of records to be spaced by loading the WC with the 2's complement of the number prior to initiating a spacing operation. After spacing the desired number of records, the transport will halt with the Job Done flag set in the status word. Because Continuous Mode of operation in spacing operations is meaningless, any attempt to space in Continuous Mode will be ignored and the control spaces the tape in Normal Mode.

4.4.5 Write End of File

This command writes the EOF characters in IBM compatible format. Setting of the CA and WC registers is not necessary for this function. The Continuous Mode of operation is meaningless for this function and hence the control implements this function in the Normal Mode. IBM compatibility requires that EOF be written with odd parity. The tape will stop after writing the EOF marker with the Job Done flag set in the status word.

4.4.6 Rewind

This function causes the tape to rewind at a high speed. At the end of this operation, the tape will stop on the BOT marker with the Job Done flag set. This function does not require the setting of WC and CA registers. As long as this function is in progress Tape Rewinding (bit 1) in the status word will be set and the control is not ready.

Table 4.4 is a summary of the tape operations and possible errors.

TABLE 4.4 PROGRAMMING SUMMARY

FUNCTION	CHARACTERISTICS	STATUS OR POSSIBLE ERRORS
REWIND	CA: Ignored WC: Ignored DENSITY: Must be selected MODE: Ignored. Always will be Normal Mode PARITY: Ignored ENABLE: Must be set if a Program FLAGS: Interrupt is desired	Illegal Rewind in progress BOT Job Done
READ	CA: Must be loaded with one less than the starting address WC: Must be loaded with the 2's complement of number of words required DENSITY: Must be selected MODE: Must be selected PARITY: Must be selected ENABLE: Must be set if a Program FLAGS: Interrupt is desired	Illegal EOF Parity Job Done EOT
WRITE	Same as READ	Same as READ except no EOF

Table 4.4 continued

FUNCTION	CHARACTERISTICS	STATUS OR POSSIBLE ERRORS
SPACE FORWARD	CA: Ignored WC: 2's complement of number of records to be spaced DENSITY: Must be selected MODE: Ignored. Always will be Normal Mode PARITY: Ignored ENABLE: Must be set if a Program FLAGS: Interrupt is desired	Illegal EOF Job Done EOT
SPACE REVERSE	Sames as SPACE FORWARD	Illegal EOF BOT Job Done
READ/COMPARE	Same as READ	Illegal EOF EOT Read/Compare Fail Job Done
WRITE EOF	CA: Ignored WC: Ignored DENSITY: Must be selected MODE: Ignored. Always will be Normal Mode PARITY: Ignored. Always will be odd parity ENABLE: Must be set if a Program FLAGS: Interrupt is desired	Illegal Job Done

5. LOGICAL ORGANIZATION AND IMPLEMENTATION OF THE CONTROL UNIT

The information contained in this chapter is a detailed description of the tape control unit operations and control flow diagrams and timing diagrams are included wherever necessary to facilitate understanding.

The relevant engineering drawings are located in Chapter 6 and are referenced by the last number of the drawing designation (hence, Drawing Number PTC-01-3 will be called Drawing 6.3). The signal and module locations on the drawing are referenced according to the co-ordinates on the margins of the drawings. Appendix 3 describes the conventions used in preparing these drawings.

Familiarity with the input-output facilities of the PDP-8⁽⁴⁾ and signal specifications for the tape units^(10,11) aid considerably in understanding the control unit operations. For convenience Appendix 2 tabulates the signal details of the tape units as the referenced documents may not be readily accessible.

5.1 Major Functional Sub-units:

Drawing 6.1 shows the basic functional block diagram of the tape control unit depicting the major registers and various interfaces between the computer and the tape transports.

(a) Device Selectors

The Device Selectors decode the input-output (IOT) instructions and generate the necessary pulses to load and clear the Command Register, read and clear the Status Register and skip when the program interrogates the tape system status. See chapter 4 for a complete list of IOT instructions.

(b) Command Register.

The Command Word specifying the desired tape operation is received and held in this register. The contents of the Command Register are decoded in the control to implement the desired operation (see chapter 4 for the Command Word format).

(c) Status Register

The control unit uses this register to assemble and hold the Status Word, containing all the necessary information regarding the tape system status. The Status Word is transferred into the computer on demand (see Table 4.3 for the status bit assignment).

(d) Longitudinal Redundancy Character Buffer (LRCB)

The control loads this register with the characters read from the tape to calculate the longitudinal parity and check the calculated parity with the LRC character recorded on the tape.

(e) Cyclic Redundancy Character Register (CRCR)

This register is used to calculate the CRC character to be written on the tape.

(f) Read/Write Buffer (RWB)

The control uses this register to hold the data obtained from the computer to format into 8 bit characters for writing on the tape and assemble characters read from the tape into twelve bit words while reading from the tape.

This register is also used by the control to compare the data on the tape with the data in the core during a Read/Compare operation.

(g) Input-Output data Multiplexing

These circuits are used to route the data between the computer and the tape control unit as dictated by the selected operation.

(h) Transport Data Multiplexing

These circuits route data between the Read/Write Buffer and the data electronics in the transports.

(i) Transport Control Signal Multiplexing

These circuits accept and deliver the control signals between the local control in the transports and the PTC-1

(j) Skip Gating

The Skip gating logic generates a pulse from the Job Done, Error flags and the Skip instruction to increment the program counter in the PDP-8 by one.

(k) Fixed Memory Address

The twelve bits specified by this "hard wired" register indicate the location of the WC register in the core memory (see section 5.9).

(l) Interrupt Gating

The interrupt logic generates a signal from the Error, Job Done flags and the Enable (bit 9) in the Command Word to request a program interrupt.

(m) Data Flag

The control requests access to the PDP-8 through this flip-flop whenever the data is ready for a transfer.

(n) Control

The control is a collection of logic and timing circuits scattered throughout the PTC-1 to co-ordinate the various operations to implement a desired tape operation.

5.2 Device Selector Logic:

The Device Selector Logic as shown in Drawing 6.2 decodes the output of the Memory Buffer bits 3 through 8 and generates the IOT pulses used to implement the instructions listed in Table 4.1.

5.2.1 Read status and load command pulses

When the program specifies a MTSR or MTCM instruction, the Memory Buffer contains an octal code of 70 in bits 3 through 8. The Device Selector module⁽²⁾ (see location A1, A2, B1, B2 and C1) responds to this code. If the instruction issued is MTCM, IOP 2 pulse generated by the PDP-8 at event time 2 is gated with the decoded output to generate the IOT 702 pulse. This pulse is used to clear the Mode bit in the Command Register thus changing the mode of operation into Normal Mode. Similarly, when a MTSR instruction is issued IOP 4 pulse from the computer is used to generate the IOT 704 pulse. This pulse gates the status information to produce the outputs (IM 0 through IM 8 on Drawing 6.25) which are loaded into the PDP-8 accumulator.

When a MTAF or MTCW instruction is issued the second device selector generates the IOT 712 or IOT 714 pulses respectively. The IOT 712 pulse is used to generate the $0 \rightarrow CR$ signal which clears the Command and Status Registers (see Drawing 6.3). The IOT 714 pulse is used to generate the $AC \rightarrow CR$ signal which transfers the Command Word from the accumulator into the Command Register as an exclusive OR transfer.

The IOT 724 pulse generated by the third device selector when a MTRC instruction is issued, is gated with the Command Register outputs to generate IM2, IM3, and IM4 through IM 11 signals which load the accumulator with the Command Register contents.

The IOT 722 pulse is generated when a MTGO instruction is issued.

5.2.2 Skip pulse generation:

When a skip instruction is issued by the program (MTSF or MTTR, or MTCR) the device selectors receive the IOP 1 pulse at event time 1 of the computer. This pulse is gated with the specified device code (octal 70, 71 or 72) to generate the IOT 701 or IOT 711 or IOT 721 signals. The IOT 701 pulse is gated with the Error and Job Done flag outputs on to the skip bus of the PDP-8. The IOT 711 and IOT 721 pulses are also gated with the SELECTED UNIT READY and RUN/STOP signals respectively on to the skip bus (see Drawing 6.28). If the conditioning inputs permit these IOT pulses drive the skip bus to ground, thus causing the program counter in the PDP-8 to be incremented by one to skip the next sequential instruction in the program.

5.3 Command Register and Associated Control:

As mentioned earlier, the tape control receives the Command Word and holds it in this nine bit register. Drawing 6.3 shows the seven command bits specifying the Unit Number (UNIT NO), desired parity (PITY), Mode (MODE), Function desired (FR 0 -FR 2) and Enable Flags (ENABLE FLGS). The remaining two bits specifying the tape density (DENSITY 0 and DENSITY 1) are located on Drawing 6.4. The signals $0 \rightarrow CR$ and $AC \rightarrow CR$ (derived from the IOT 712 and IOT 714 pulses) are used to clear and load the Command Register respectively. The Command Register is wired such that if an accumulator bit is a '1' the corresponding bit in the Command Register will be complemented (exclusive OR) by the $AC \rightarrow CR$ signal. Two signals, UN1 EVEN/ODD SELECT and UN2 EVEN/ODD SELECT are also derived from the PITY bit in the Command Register. These signals specify the desired parity to the data electronics in the transports.

At this stage, it is necessary to recall the system requirement (see section 3.8) which specifies that the issuing of an illegal command should not interfere with any current operation that may be in progress. This emphasises that changing (clearing or loading) the Command Register when a tape operation is in progress is illegal. The control protects the Command Register from such illegal operations by inhibiting the generation of $0 \rightarrow CR$ and $AC \rightarrow CR$ signals whenever the RUN/STOP signal is true. For the present it will be assumed that whenever the RUN/STOP signal is true, some tape operation is in progress and the control is busy. Apart from protecting the CR, the control also takes note of such illegal attempts to inform the program on conclusion of the current operation.

It is interesting to consider the case when a MTCW instruction with "all-zero" accumulator is issued and the control is busy. Though this would not affect the Command Register (because all the accumulator bits are zero), the control faithfully protects the Command Register and instead of appreciating the subtle difference of the program issuing a harmless instruction, presents back an error status.

The function bits (FR 0 through FR 2) of the Command Register are decoded using an octal to binary decoder module (see Drawing 6.5) to determine the selected function.

5.4 Pinch Roller Control:

The MT-36 tape transports are equipped with two pinch rollers to drive the tape in either direction; the motion of the tape is determined by the pinch roller control logic centered around the RUN/STOP flip-flop as shown in Drawing 6.6.

The signals UN1 RUN/STOP and UN2 RUN/STOP are derived by gating the UNIT NO. bit of the Command Register with the RUN/STOP flip-flop output. These signals, when true, energize the appropriate pinch roller through the local control in the transports.

When a MTGO instruction is received from the program to initiate a desired operation, the control triggers a delay called GO DELAY using the IOT 722 pulse. This delay time allows the control to check for the possible error conditions (see section 5.14.1) that may exist before initiating the operation. If there are no errors, the RUN/STOP flip-flop is set at the termination of the GO DELAY. This engages the appropriate pinch roller; tape on the selected transport

begins to move and the desired operation has begun.

Stopping the tape is slightly more involved for the following reasons:

- (a) During the normal tape operation, it can be stopped only in an Inter Record Gap and while stopping, consideration must be given to the selected mode of operation (NM or CM) and errors in the Status Register. If the selected operation is performed in CM, and the control has successfully operated on a record, then the tape need not stop but the Job Done flag is to be set. On the other hand, the tape should be stopped and the Error flag is to be set in the event of an unsuccessful operation by the control (see chapter 4).
- (b) If a spacing operation (Space Forward or Space Reverse) is selected then the total number of records spaced must also be taken into account.
- (c) While stopping the tape, the final position of the read head in the Inter Record Gap is an important consideration⁽¹¹⁾. When the tape does finally come to a halt, the read head must be located far enough in the IRG, so that if a Space Reverse operation is attempted from this position, enough time should be available to accelerate the tape to the rated speed before entering the actual record.
- (d) While writing in CM, as the tape does not stop after a record, the IRG specifications should be kept in mind.
- (e) The command repetition rate specifications of the transports should not be exceeded.

In the design of the pinch roller control logic, a method involving two delay times, STOP DELAY and SHUTDOWN DELAY is employed. The STOP DELAY is triggered whenever an attempt to stop the tape is to be made. If the transport is allowed to stop by the other conditions, it will stop only after this delay (Rewind is an exception, see section 5.5). This delay will be chosen long enough to satisfy the tape acceleration requirements mentioned earlier.

begins to move and the desired operation has begun.

Stopping the tape is slightly more involved for the following reasons:

- (a) During the normal tape operation, it can be stopped only in an Inter Record Gap and while stopping, consideration must be given to the selected mode of operation (NM or CM) and errors in the Status Register. If the selected operation is performed in CM, and the control has successfully operated on a record, then the tape need not stop but the Job Done flag is to be set. On the other hand, the tape should be stopped and the Error flag is to be set in the event of an unsuccessful operation by the control (see chapter 4).
- (b) If a spacing operation (Space Forward or Space Reverse) is selected then the total number of records spaced must also be taken into account.
- (c) While stopping the tape, the final position of the read head in the Inter Record Gap is an important consideration⁽¹¹⁾. When the tape does finally come to a halt, the read head must be located far enough in the IRG, so that if a Space Reverse operation is attempted from this position, enough time should be available to accelerate the tape to the rated speed before entering the actual record.
- (d) While writing in CM, as the tape does not stop after a record, the IRG specifications should be kept in mind.
- (e) The command repetition rate specifications of the transports should not be exceeded.

In the design of the pinch roller control logic, a method involving two delay times, STOP DELAY and SHUTDOWN DELAY is employed. The STOP DELAY is triggered whenever an attempt to stop the tape is to be made. If the transport is allowed to stop by the other conditions, it will stop only after this delay (Rewind is an exception, see section 5.5). This delay will be chosen long enough to satisfy the tape acceleration requirements mentioned earlier.

Whether the tape is stopped or not, the SHUTDOWN DELAY will be triggered at the end of the STOP DELAY. The sum of these two delays will be equal to that necessary to generate the 0.6 inch of blank tape to meet the IRG specification when writing in the Continuous Mode. Setting of the flags (Job Done, and Error) will occur at the end of the SHUTDOWN DELAY. If the SHUTDOWN DELAY alone does not permit meeting the command repetition rate specification, the GO DELAY can be increased to satisfy this requirement.

Assuming that a signal is available to indicate that the tape is in an IRG and this signal will not be generated during a Rewind operation, a truth table as shown in Table 5.1 can be prepared depicting the possible conditions under which the SHUTDOWN DELAY is to be triggered and the tape is to be stopped.

From an analysis of the truth table, the following logic equations are obtained.

$$\text{SHUTDOWN} = [\text{SPACE FWD} + \text{SPACE REV} + (\text{SPACE FWD} + \text{SPACE REV}).\text{WCO} + \text{EOF}]\text{IRG} \quad \dots(5.1)$$

$$0 \rightarrow \text{RUN/STOP} = (\text{ERROR} + \text{NORMAL MODE}).\text{SHUTDOWN} \quad \dots(5.2)$$

where WCO indicates the Word Count Overflow.

The control generates a signal called IRG from the EOB IND signal provided by the data electronics (see section 5.13). This signal is a negative going pulse of about 1 msec width. The positive-going edge (trailing edge) of this signal tries to trigger the STOP DELAY in

TABLE 5.1: TRUTH TABLE FOR PINCH ROLLER CONTROL

Write	Read	Read Comp	Space FWD	Space REV	Write EOF	Shut Down	Mode	Error	WCO	$0 \rightarrow$ Run/Stop
0	0	0	0	0	1	1	0	0	0	1
0	0	0	0	0	1	1	0	1	0	1
0	0	0	0	1	0	0	0	0	0	0
0	0	0	0	1	0	1	0	0	1	1
0	0	0	0	1	0	1	0	1	0	1
0	0	0	0	1	0	1	0	1	1	1
0	0	0	0	1	0	1	0	1	1	1
0	0	0	1	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0	0	1	1
0	0	0	1	0	0	1	0	1	0	1
0	0	0	1	0	0	1	0	1	1	1
0	0	1	0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0	0	1	1
0	0	1	0	0	0	1	0	1	0	0
0	0	1	0	0	0	1	1	0	1	0
0	0	1	0	0	0	1	1	1	0	1
0	0	1	0	0	0	1	1	1	1	1
0	1	0	0	0	0	1	0	0	0	1
0	1	0	0	0	0	1	0	0	1	1
0	1	0	0	0	0	1	0	1	0	1
0	1	0	0	0	0	1	1	0	1	0
0	1	0	0	0	0	1	1	1	0	1
1	0	0	0	0	0	1	0	0	0	1
1	0	0	0	0	0	1	0	0	1	1
1	0	0	0	0	0	1	0	1	0	1
1	0	0	0	0	0	1	1	0	0	0
1	0	0	0	0	0	1	1	0	1	0
1	0	0	0	0	0	1	1	1	0	1
1	0	0	0	0	0	1	1	1	1	1

Drawing 6.6. The conditioning input to this delay is the expression

$$[\overline{\text{SPACE FWD}} + \overline{\text{SPACE REV}} + (\overline{\text{SPACE FWD}} + \overline{\text{SPACE REV}}) \cdot \text{WCO} + \text{EOF}]$$

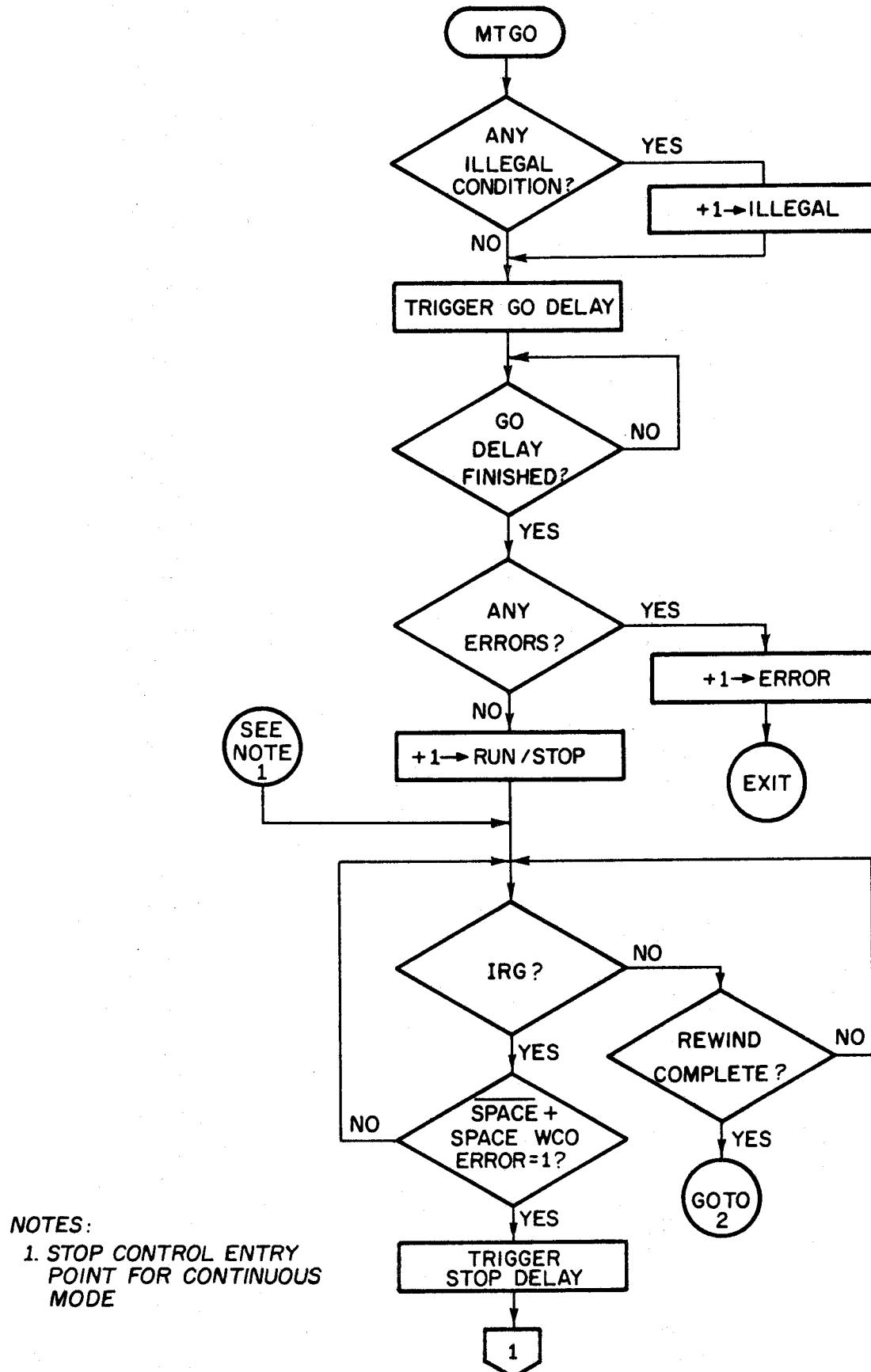
When this expression is '1', the delay is triggered and the $0 \rightarrow \text{RUN/STOP}$ pulse is generated at the end of the STOP DELAY. The ENABLE $0 \rightarrow \text{RUN/STOP}$ is nothing but the first term of the equation (5.2).

Apart from trying to clear the RUN/STOP flip-flop, the $0 \rightarrow \text{RUN/STOP}$ pulse also triggers the SHUTDOWN DELAY (see Drawing 6.27). At the termination of the SHUTDOWN DELAY, if there are no errors in the Status Register, the Job Done flag is set, otherwise the Error flag is set.

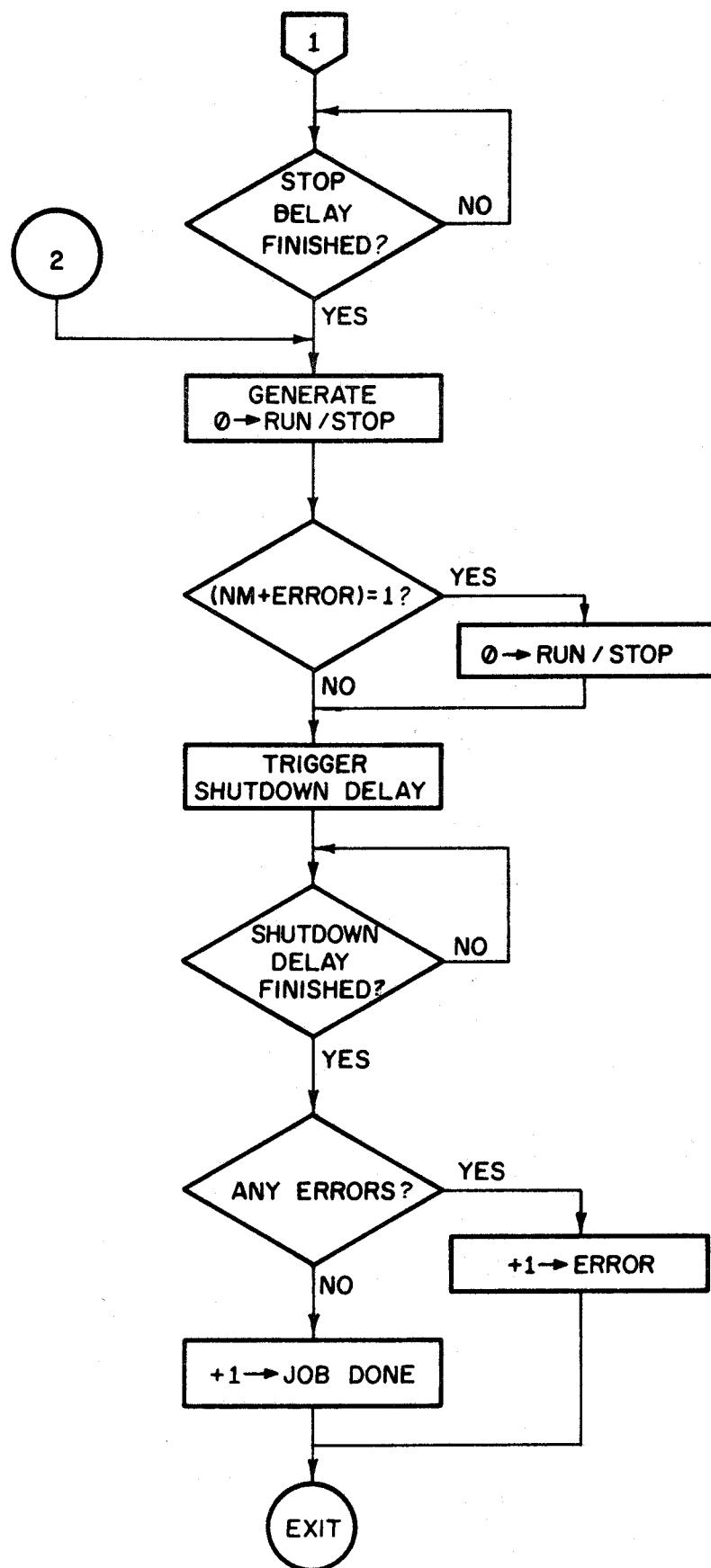
As can be seen from the Drawing 6.6, the $0 \rightarrow \text{RUN/STOP}$ pulse is also generated by the REWIND COMPLETE signal. This signal comes from the Rewind control logic (see section 5.5) when the BOT marker is sensed after completing a rewind. This signal is also generated when the BOT marker is sensed during a Space Reverse operation, and serves to terminate it. Flow Chart 1 summarizes the roller control logic.

5.5 Rewind Control:

The tape control has to specify "high Speed" on the NORMAL/HIGH SPEED line and "REVERSE" on the FORWARD/REVERSE line of the transports (see appendix 2) to initiate a Rewind operation. Under these conditions the local control in the transport performs the following operations⁽¹⁰⁾:



FLOW CHART 5.1 PINCH ROLLER CONTROL (CONT'D)



FLOW CHART 5.1

- (a) Removes the READY signal and switches off the vacuum pump.
- (b) Pauses briefly to allow the vacuum to collapse and starts the reel servos to rewind the tape.
- (c) When the BOT marker is sensed, stops rewinding and switches on the vacuum pump.
- (d) When the vacuum is re-established, provides the READY signal back.

The control sequence performed by the tape control for a Rewind operation is shown in Drawing 6.7. This sequence is entered when the Command Register specifies a Rewind operation and the MTGO command is issued to initiate it.

When the MTGO command is received the control proceeds to check the usual error conditions before initiating the command as shown in Flow Chart 7. If there are no errors, two signals, ENABLE FWD/REV and ENABLE NORMAL/HI SPEED are generated. These two signals are used as the conditioning inputs to two flip-flops, FWD/REV and NORMAL/HI SPEED respectively. When the GO DELAY period is complete, these two flip-flops are set if the conditioning inputs are true. The outputs of these flip-flops are gated with the UNIT NO. bit of the Command Register to obtain the UN1 FWD/REV, UN2 FWD/REV, UN1 NORMAL/HI SPEED and UN2 NORMAL/HI SPEED signals which are used by the local control in the transports.

The Rewind operation on the selected tape transports starts when both these flip-flops are set. Upon sensing the BOT marker while rewinding, the local control automatically stops rewinding the tape and the control generates the BOT signal (see Drawing 6.25). This

signal clears both the FWD/REV and NORMAL/HI SPEED flip-flops, in preparation to drive the tape at normal speed to position it back on the BOT marker (see section 3.7). At this time though the BOT marker is sensed, the tape control does not generate the REWIND COMPLETE signal. As mentioned earlier, the local control removes the READY signal normally available to the tape control unit. However, when the vacuum has been re-established, the READY signal becomes true.

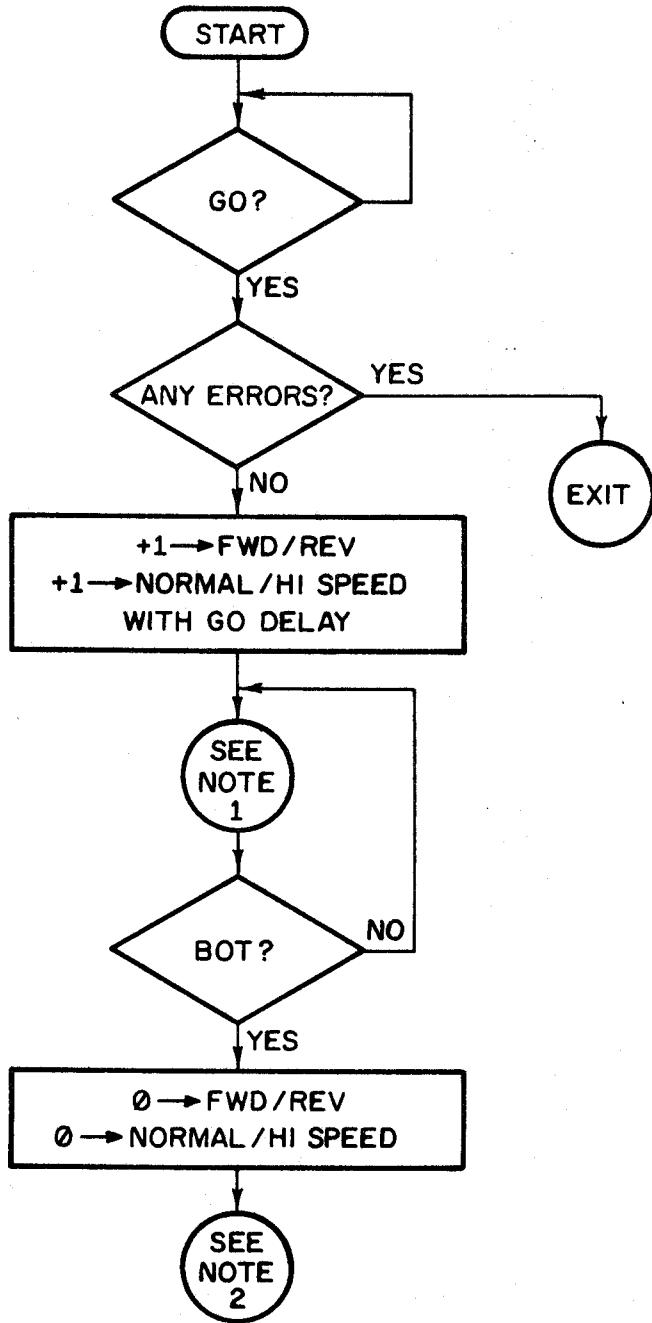
Though, the RUN/STOP flip-flop has been set during all this time, the pinch roller is prevented from engaging as a result of removing the READY signal by the local control. However, as soon as the local control indicates a READY status again, the pinch roller engages and the tape begins to move forward. If the BOT marker is sensed now, the tape control generates the REWIND COMPLETE signal. This signal produces $0 \rightarrow$ RUN/STOP pulse (see Drawing 6.6) which clears the RUN/STOP flip-flop because the Rewind operation is always implemented in the Normal mode.

Apart from clearing the RUN/STOP flip-flop, $0 \rightarrow$ RUN/STOP pulse also triggers the SHUTDOWN DELAY which sets the Job Done flag signifying a successful Rewind operation.

Flow Chart 2 is a summary of the Rewind control logic.

5.6 Read Clock and Data Clock Control:

The data electronics provided in the transport are always monitoring the read head output and whenever a non-zero character



NOTES:

1. REWIND IN PROGRESS
2. ENTER FLOW CHART 5.1 AT STOP CONTROL ENTRY POINT FOR CONTINUOUS MODE

FLOW CHART 5.2 REWIND CONTROL

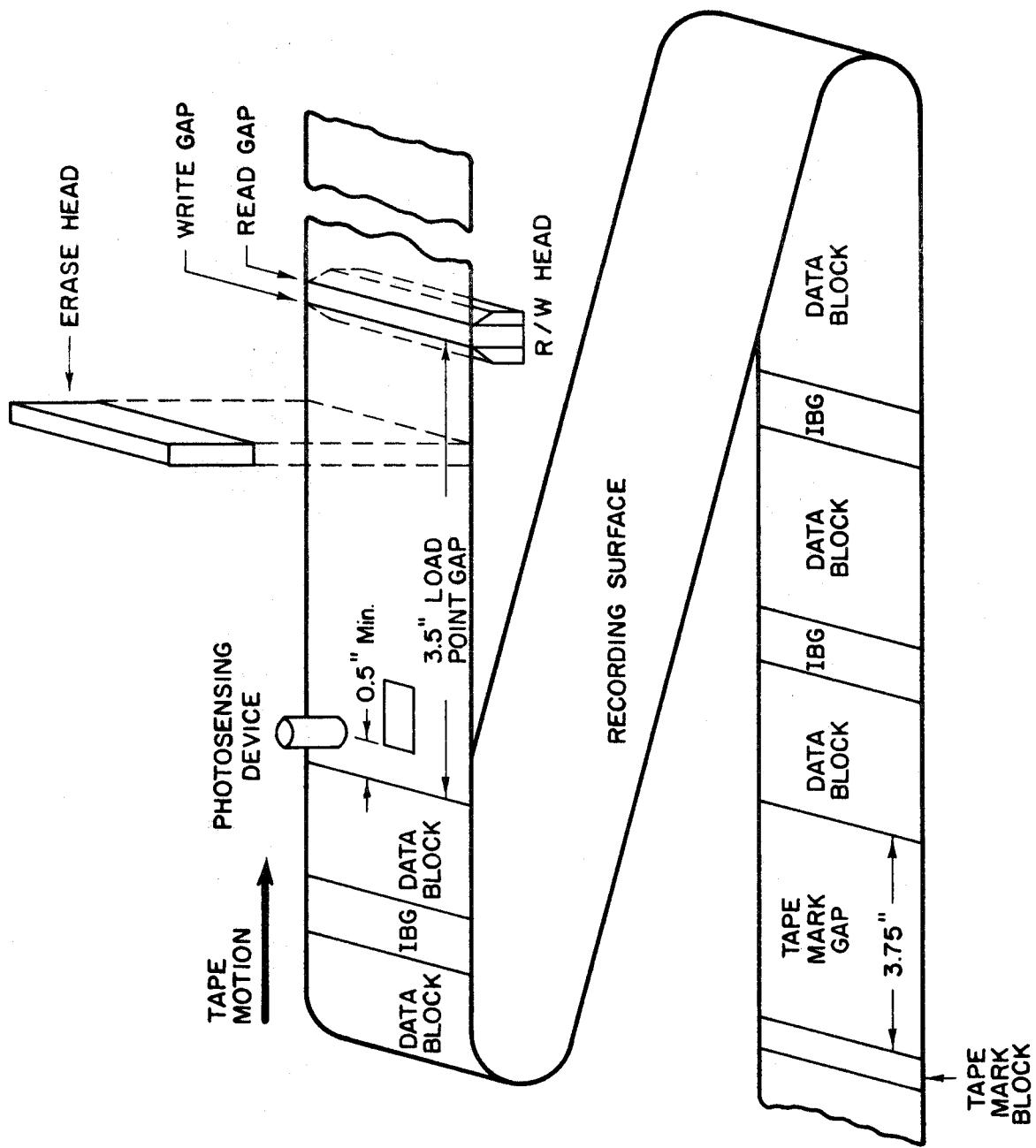


FIGURE 5.1 ERASE, WRITE AND READ HEAD LOCATIONS WHEN TAPE IS AT LOAD POINT

passes over the read head, they generate a Read Clock pulse. However, all the pulses appearing on the Read Clock line do not represent data. These pulses can be classified into three categories:

- (a) Undesired data.
- (b) Check characters.
- (c) Desired data.

The control logic shown on Drawing 6.8 prevents the occurrence of the Read Clock pulses representing undesired data, while separating the desired data from the check characters for internal use.

5.6.1 Suppressing the undesired data

The tape control inhibits the generation of the Read Clock pulses in the data electronics by enabling the "Read Reset" line under the following conditions:

- (a) During a Rewind operation: when a Rewind operation is in progress there are no data transfers or checks involving the recorded information on the tape.
- (b) While initiating a tape operation when the tape is at the BOT marker: for IBM compatibility, certain length of tape (load point gap) has to be erased before the first physical character begins (see chapter 2).

Figure 5.1 shows schematically the positioning of the tape when loaded with respect to the erase, write and read heads. During normal operations of the tape system, the length of tape from the physical beginning to the erase head can never be erased. However, if any tape operation is attempted from this position, the length of tape between the read and erase heads has to pass over the read head. Any information

that may exist on this length of tape is invalid because the actual data does not start until about 1/2" beyond the BOT marker. To prevent this invalid information from affecting the tape system, the control triggers a delay called "Load Point Delay" whenever a tape operation is started from the BOT marker. The Read Reset line is kept enabled for the duration of this delay to inhibit reading any invalid information. The adjustment of this delay is such that by the time the Load Point Delay is complete, the read head is located well in the Load Point Gap and any data passing over the read head after this will be read as usual.

5.6.2 Separating the desired data from the check characters.

Once the possibility of invalid clock pulses is eliminated, any clock pulse occurring on the Read clock line must represent valid data or check characters. The remainder of the logic is used to separate the clock pulses representing data from those representing the check characters.

Characters on the tape are regularly spaced at the selected density, so that if the tape is moving at a constant speed, the Read Clock pulses will be occurring at regular intervals. However, the CRC and LRC characters violate this; the CRC is about four spaces away from the last data character in a record and the LRC is four more spaces away from the CRC. The data electronics in the transports are equipped to monitor the spacing between the characters (see EOB detection in⁽¹¹⁾). Whenever two or more clock pulses are missing after encountering a clock pulse, a signal called EOB INDICATION is generated. This signal indicates

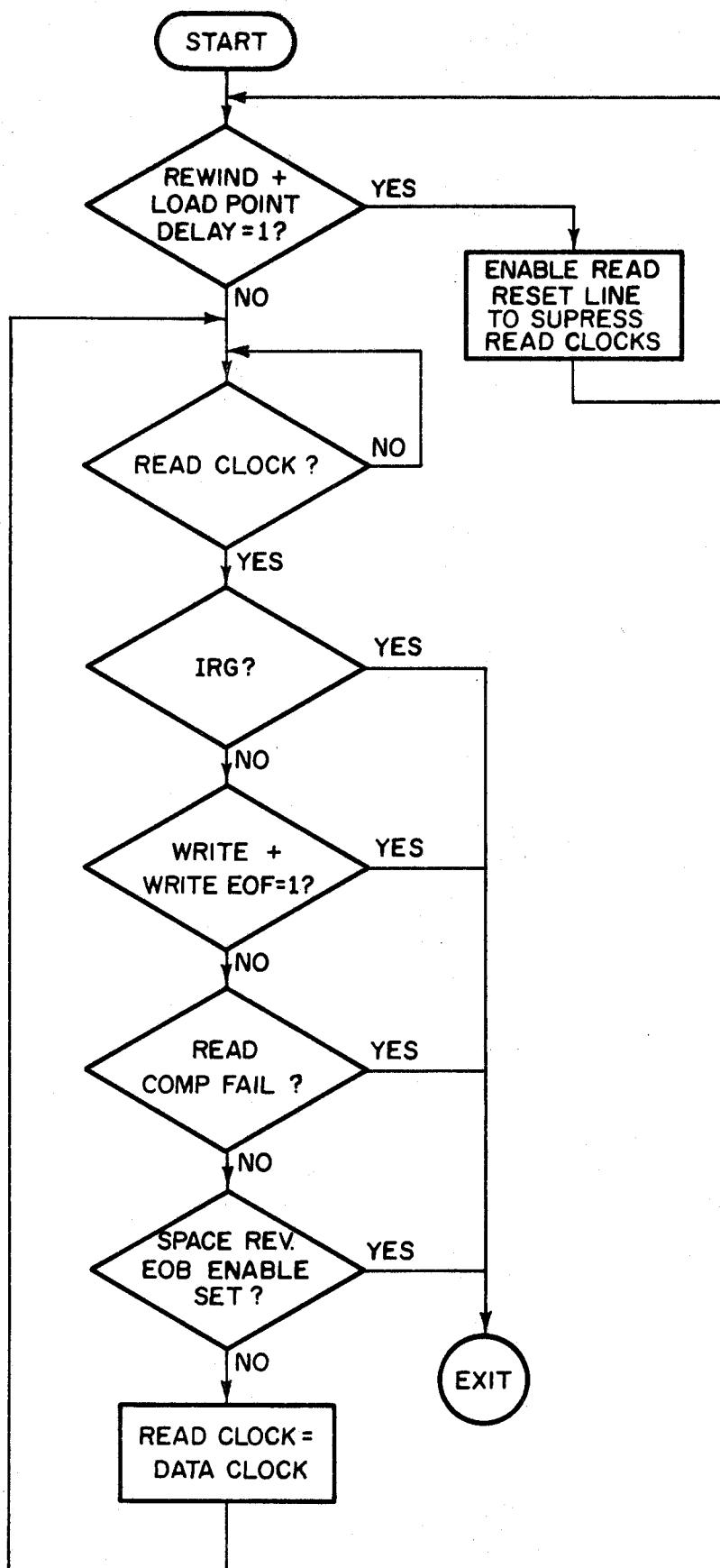
the control that the tape is about to enter an Inter Record Gap. To distinguish between the data and the check characters, the control makes use of the fact that the two clock pulses occurring immediately after receiving an EOB INDICATION signal are the check characters, except during a Space Reverse operation.

The Read Clock pulses received by the control (UN1 RDCLK and UN2 RDCLK) are multiplexed using an OR gate and shaped by a Schmitt trigger. The shaped output is power amplified to increase the drive capability and is used by the tape control as READ CLOCK signal.

The tape control needs the DATA CLOCK signals whenever the following logic equation is satisfied:

$$\begin{aligned} \text{READ.IRG} + \text{READCOMPARE} (\overline{\text{IRG}} + \overline{\text{READCOMPFAIL}}) + \text{SP.FWD.IRG} \\ + \text{SP.REV}(\text{IRG ENABLE}(1)) = 1 \end{aligned} \quad \dots (5.3)$$

If the tape is being read for either data transfers or comparisons, all the clock pulses received by the control before receiving the IRG signal (derived from the EOB INDICATION) represent data. During a READ COMPARE operation the generation of the DATA CLOCK signals is controlled not only by the IRG signal but also by the result of comparisons; DATA CLOCK is generated as long as there is no comparison failure. Once a comparison failure is detected, the present operation is unsuccessful and the comparison is discontinued (see section 4.4.3). This facilitates the finding of the address of the location whose contents failed to compare, by examining the contents of the CA register in the core memory.



FLOW CHART 5.3 DATA CLOCK CONTROL

During any spacing operation (Forward or Reverse), data transfers are not needed. Still the DATA CLOCK signals are generated by the control for the explicit purpose of indentifying the EOF on the tape during these operations. In a Space Forward operation, two characters received immediately after an IRG signal are the check characters. However, while spacing in the reverse direction, control encounters the check characters before data. The tape control design uses a different strategy to extract data from the check characters during a Space Reverse operation (see section 5.13). For the present it will be assumed that the READ CLOCK signals received whenever the EOB ENABLE signal is true during a Space Reverse operation represent data.

For implementation, the conditions for DATA CLOCK signal generation mentioned earlier can be re-stated by the following propositions:

DATA CLOCK pulses are not generated whenever:

- (a) IRG signal is true, or
- (b) opeation selected is Write or Write EOF, or
- (c) Read comparison has failed, or
- (d) Operation selected is Space Reverse and EOB ENABLE signal is false.

5.7 Read/Write Buffer and Its Associated Control:

Some form of temporary storage is required to implement the formatting scheme described in section 4.3, and the Read/Write Buffer with a capacity of twenty four bits is provided for this purpose. The logical organization is such that the computer treats these twenty four

bits as two 12 bit registers, while the data electronics in the transports treat them as three 8 bit registers. The individual bits in this buffer are marked RWB 10 through RWB 37 in octal code (see Drawing 6.9) to emphasize the point that the Read/Write Buffer consists of three sections, RWB 1, RWB 2 and RWB 3 with 8 bits in each section.

The following register operations are assumed to implement the desired formatting scheme:

- (a) Writing on to the tape will always take place from the RWB 1.
- (b) Transfers from the RWB 2 to RWB 1 and RWB 3 to RWB 2 are possible.
- (c) Data characters from the tape will always be received into the RWB 3 first.
- (d) RWB 10 through RWB 23 and RWB 24 through RWB 37 will have two-way communication with the Memory Buffer (MB) of the computer to receive and transmit data as twelve bit words.

The illustration used in section 4.3 where two computer words are formatted as three tape characters is recalled to explain the role played by the Read/Write Buffer in the data formatting. The first and the second word are loaded into RWB 10 through RWB 23 through RWB 37 by gating the Memory Buffer outputs (BMB signals on Drawing 6.9) using the BMB \rightarrow RWB 1-2 and BMB \rightarrow RWB 2-3 pulses respectively. The following sequence of operations are performed in the control to write these two words as three tape characters:

- (a) The contents of the RWB 1 are loaded into the write buffer of the selected tape unit and the RWB 1 is cleared using the 0 \rightarrow RWB 1 pulse.
- (b) The contents of the RWB 2 are transferred into the RWB 1 using the RWB 2 \rightarrow RWB 1 pulse and the RWB 2 is cleared using the 0 \rightarrow RWB 2 pulse.

- (c) The contents of the RWB 3 are transferred into the RWB 2 using the RWB 3 → RWB 2 pulse and the RWB 3 is cleared using the 0 → RWB 3 pulse.
- (d) Operations (a) and (b) above are repeated until the three characters are written on the tape.

If a selected operation involves reading of data from the tape, the characters read from the tape are received into the RWB 3 by gating the Data Output lines of the selected tape unit with the DATA CLOCK (see section 5.6 where this signal generation is described). To assemble two 12 bit words prior to a transfer into the computer the following operations are performed:

- (a) The first character is transferred from the RWB 3 into the RWB 1 via the RWB 2 using the RWB 3 → RWB 2 and RWB 2 RWB 1 pulses and both RWB 3 and RWB 2 are cleared.
- (b) The second character received into the RWB 3 is transferred into RWB 2 using the RWB 3 → RWB 2 pulse and RWB 3 is cleared.
- (c) The third character is left in the RWB 3.
- (d) The contents of RWB 10 through RWB 23 are transferred as the first twelve bit word and the contents of RWB 24 through RWB 37 are transferred as the second 12 bit word into the computer.

The prime function of the RWB control logic is to generate all the necessary signals to clear and effect transfers between the three sections of the Read/Write buffer in a pre-determined sequence. The sequence in which these signals are to be generated depends not only on the tape operation in progress but also on the number of characters that have been operated upon. For example, during a Read operation, the signal sequence necessary to operate on the RWB while manipulating the first character is different from that needed for the second or third characters.

5.7.1 Character counter

As the tape control has to deal with a maximum of three characters at any given time, a two bit binary counter called CHARACTER COUNTER (CHAR CNTR) is maintained. The state of the control depends on the count in this counter. The pulse INC → CHAR CNTR advances the count every time a character is read or written. This signal is generated whenever the CLOCK COUNTER overflows (see section 5.7.2) or a DATA CLOCK pulse occurs. For the present it will be assumed that the CLOCK COUNTER overflow indicates writing of a character on the tape. The outputs of the CHARACTER COUNTER are decoded (see Drawing 6.10) to obtain the CHAR CNTR 1, CHAR CNT2 and CHAR CNT 3 signals whenever the count is 1, 2 and 3 respectively.

During a write operation, the CHARACTER COUNTER also helps to determine whether two or three characters are to be written on the basis of the number of words (one or two) supplied by the computer during a transfer. The reasoning behind this is as follows:

Whenever a transfer is allowed, the control tries to extract two words from the computer. Whether this is allowed or not depends on the contents of the Word Count register. During a transfer one of these three things can happen:

- (a) The computer supplies two words without a Word Count Overflow.
- (b) The computer supplies two words but the Word Count Overflow occurs.
- (c) The computer supplies only one word and the Word Count Overflow occurs.

If two words are available without a Word Count Overflow, the Read/Write buffer is loaded with these two words as explained earlier in this section. Occurrence of the BMB → RWB 2-3 pulse during a Write operation forces the CHARACTER COUNTER to hold a count of 1 (see Drawing 6.10, Location D3). As 1 is the two's complement of 3, if the CHARACTER COUNTER is incremented once every character written, it will reach zero after the third character. Because the Word Count did not overflow, request for more data is made. On the other hand, if two words are received with a Word Count Overflow, the control still writes three characters but does not request for more data from the computer.

Now consider the case when only one word is received and the Word Count Overflows. The control keeps an account of the number of words received during a transfer in the BREAK COUNT (BRK CNT) flip-flop. This flip-flop will hold a '1' whenever only one word is received (see section 5.9.2). If the BRK CNT is 1 and the Word Count Overflow occurs, a signal called SET CHAR CNTR 0 is generated (see Drawing 6.11 Location C5). This signal forces the CHARACTER COUNTER to hold a count of 2 (see Drawing 6.10, Location D3). As 2 is the two's complement of 2, it will reach zero only after writing two characters.

5.7.2 Clock counter and Event counter

Assuming that the tape is running at a constant speed, all the data characters are written under a real time clock control to obtain the desired recording density. There are three clocks provided

in the tape control unit to obtain the required three densities (see section 3.3). The outputs from these clocks (200 bpi CLK, 556 bpi CLK and 800 bpi CLK signals) are multiplexed to obtain the signal called MASTER CLOCK (see Drawing 6.11). All the signals necessary to manipulate the Read/Write buffer during a Write operation (see section 5.7) are derived from the MASTER CLOCK signal by running each clock at 4 times the frequency necessary to obtain the desired packing density. A two bit counter called CLOCK COUNTER (CLK CNTR) divides the MASTER CLOCK signal frequency by four to obtain the desired write timing. The required timing for the RWB control signal generation is obtained by counting the MASTER CLOCK pulses in a three bit EVEN COUNTER (EVE CNTR). A flip-flop called EVENT COUNT ENABLE (EVE CNT ENABLE) is used for synchronizing the EVE CNTR chain with the CHAR CNTR and the CLK CNTR. Whenever the CHAR CNTR reaches zero, a signal called $0 \rightarrow$ EVE CNT ENABLE is generated. This signal when true, pulses the reset line of the EVE CNT ENABLE flip-flop to reset it. The zero output line of the EVE CNT ENABLE flip-flop holds the common reset line of the EVE CNTR chain to ground. This forces the EVE CNTR bits to assume zero state and does not allow the counting to proceed even if the MASTER CLOCK signals are present. The EVE CNT ENABLE flip-flop is set whenever the CLOCK COUNTER reaches 3 by the decoded output of the CLK CNTR.

The fourth MASTER CLOCK pulse will increment the EVE CNTR. This pulse also makes the CLK CNTR to overflow and when this happens, two signals $INC \rightarrow$ CHAR CNTR and WRITE TIME are generated. The first signal increments the CHAR CNTR and the second signal triggers the

delay module called WRITE CLOCK PULSER. The output of this delay is the WRITE CLOCK (WRT CLK), which actually excites the Write Clock line of the selected transport to write the contents of the RWB 1 on the tape. All the MASTER CLOCK pulses occurring from the time EVE CNT ENABLE is set and the CHAR CNTR signifies that the required number of characters have been written on the tape in the present cycle and more data is to be obtained before further writing can proceed. If this happens to be the end of a record (then the Word Count Overflow must have already occurred), the clock will be switched off (see section 5.11).

5.7.3 Read/Write Buffer control signal generation

As mentioned in section 5.7.1, 0 → RWB 2, 0 → RWB 3, RWB 2 → RWB 1, and RWB 3 → RWB2 signals are necessary to manipulate the data in the Read/Write Buffer to obtain the desired formatting. There are two basic timing signals in the tape system, DATA CLOCK and MASTER CLOCK from which the Read/Write Buffer control signals are generated. Though the same signals are used to control the Read/Write Buffer while reading and writing, the sequence in which they occur is not necessarily the same in both cases.

If the operation selected is READ or READ COMPARE, then a delay chain consisting of three delay circuits READ DELAY 1, READ DELAY 2 and READ DELAY 3 is enabled. The DATA CLOCK signals trigger the chain to provide the three signals RD DELAY 1, RD DELAY 2 and RD DELAY 3 for every DATA CLOCK pulse received. The DATA CLOCK signals also increment

the CHARACTER COUNTER (see section 5.7.1). When the CHAR CNTR holds a count of 1 or 2, RWB 3 → RWB 2 is generated at the termination of the READ DELAY 1. When the first DATA CLOCK occurred, the data has been received into the RWB 3 (see section 5.7) and the CHAR CNTR is holding 1. By generating the RWB 3 → RWB 2 and RWB 2 → RWB 1 the control is transferring the first data character into the RWB 1 and clearing the RWB 3 using the 0 → RWB 3 in preparation to receive the next data character into RWB 3. At the end of the READ DELAY 3, the 0 → RWB 2 pulse is generated to clear RWB 2. When the second character is read from the tape, the second DATA CLOCK loads the character into RWB 3 which has been cleared before hand and increments the CHAR CNTR to two. At the termination of READ DELAY 1, the RWB 3 → RWB 2 pulse is again generated which transfers the second character into RWB 2. At the end of READ DELAY 2, only the 0 → RWB 3 pulse will be generated. This clears RWB 3 and the second character is left in RWB 2. When the third character is read from the tape, the DATA CLOCK once more increments the CHAR CNTR to three and none of the register control signals are generated, thus leaving the third character in RWB 3. The receipt of the third character indicates that the buffer is full and the control sets the DATA FLAG flip-flop to request access to the computer for a transfer. This will be explained in more detail in section 5.9. To ensure an all-zero Read/Write Buffer, the CLEAR ALL signal is generated whenever a MTGO command is received (this is the beginning of an operation) and after completing the data transfer into the computer (see section 5.9.3).

The timing diagram shown in Figure 5.2 summarizes the discussion on the RWB control signal generation when data is being read from the tape.

While writing the RWB control signal generation is controlled by the contents of the EVE CONTR. The decoding circuits shown on Drawing 6.12 decode the contents of the EVE CNTR to obtain the signals EVE 1 through EVE 6. As mentioned before, the EVE CNT ENABLE flip-flop is set after the occurrence of the third MASTER CLOCK pulse and the data character is written on the fourth pulse. The fourth clock pulse also increments the EVE CNTR because the EVE CNT ENABLE is set. The WRT CLK pulse which writes the data, generates the $0 \rightarrow$ RWB 1 signal using its trailing edge to clear RWB 1. When the fifth MASTER CLOCK pulse occurs, the EVE 1 signal is true and the RWB 2 \rightarrow RWB 1 signal is generated to transfer the contents of the RWB 2 into RWB 1, which was previously cleared after writing the first character. When the sixth MASTER CLOCK pulse arrives, the EVE 2 signal is true and the $0 \rightarrow$ RWB 2 signal will be generated to clear RWB 2 in preparation to receive the third character from RWB 3. At the seventh clock pulse, the EVE 3 signal will be true and the RWB 3 \rightarrow RWB 2 signal is generated to load the contents of RWB 3 into RWB 2. Now the third character is in RWB 2. On the eighth clock pulse the CLK CNTR overflows and the contents of RWB 1 are written on the tape. This is the second character. At the same time, the eighth pulse also advances the CHAR CNTR. When the eighth clock pulse occurs, the EVE 4 signal is true and the $0 \rightarrow$ RWB 3 signal is generated. This is in preparation for leaving an all-zero Read/Write Buffer when all the three characters are written. When the next clock pulse occurs (this will be the 9th pulse), EVE 5 signal is true and the

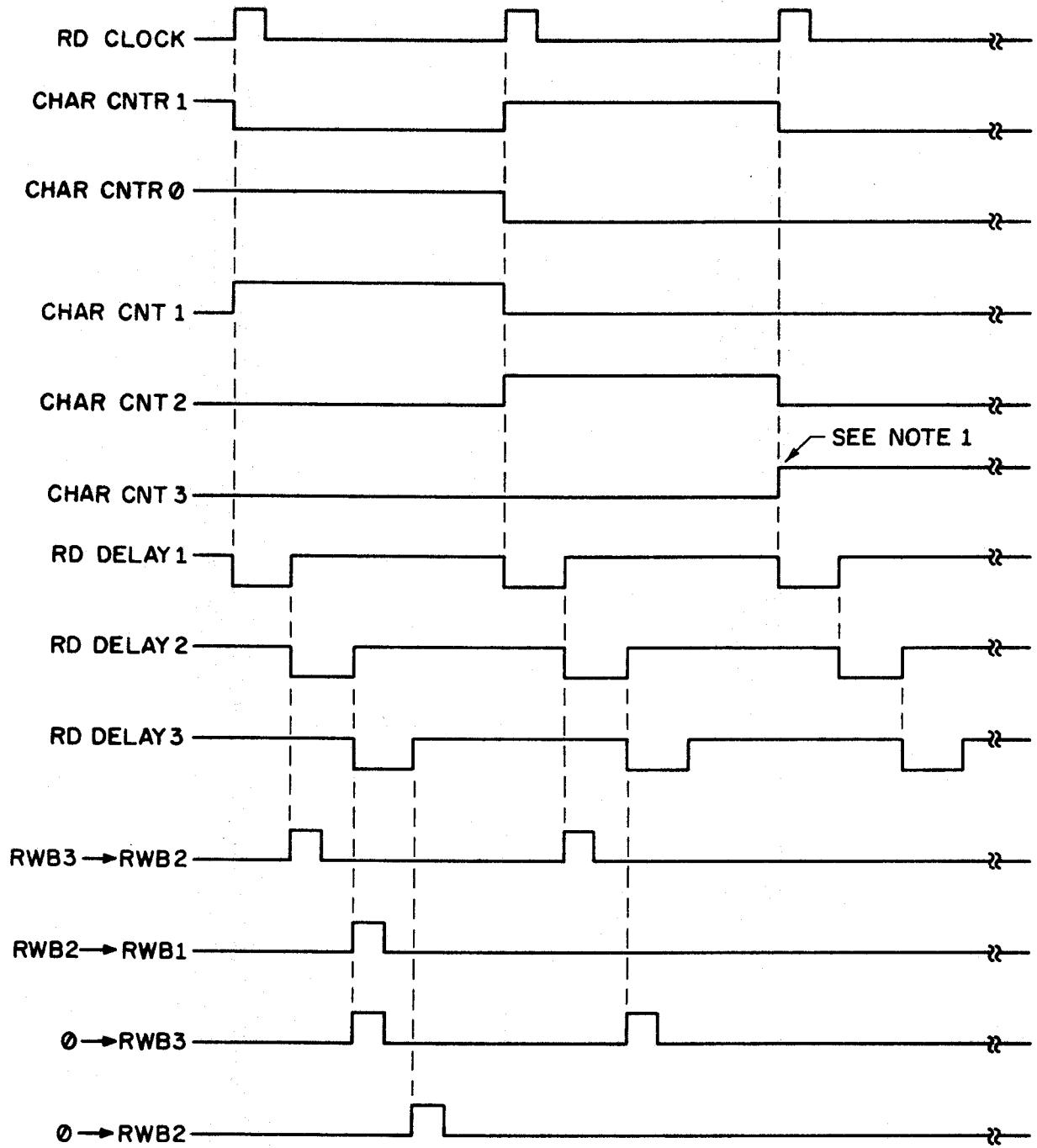


FIGURE 5.2 RWB CONTROL DURING READ

NOTES:

1. DATA FLAG IS SET HERE TO REQUEST ACCESS INTO THE COMPUTER.
2. DIAGRAM IS NOT TO SCALE.

RWB 2 → RWB 1 signal is generated once more. This transfers the third character from RWB 2 into RWB 1. At the time of the tenth clock pulse EVE 6 signal will be true and the 0 → RWB 2 signal is generated to clear RWB 2. This once again is in preparation for leaving an all-zero RWB. On the eleventh clock pulse no control signals are generated and hence the Read/Write buffer is left undisturbed. When the 12th MASTER CLOCK pulse occurs, the CLK CNTR will overflow once again and the third character which is in RWB 1 will be written on the tape. The CHAR CNTR which was loaded with the 2's complement of 3 at the time of transferring data into the tape control from the computer, would have reached zero when the third character is written. Reaching zero in the CHAR CNTR generates the 0 → EVE CNT ENABLE signal which clears the EVE CNT ENABLE flip-flop, which in turn clears the EVE CNTR chain in preparation for a next cycle of operation which will start when the CLK CNTR reaches 3. The timing diagram shown in Figure 5.3 summarizes the RWB control signal generation when data is being written on to the tape.

5.7.4 Vertical parity generation

Because the responsibility of generating the vertical parity bit to be written on the tape is assigned to the tape control unit, a parity generator package is provided as shown in Drawing 6.14.

The Boolean function for generating the parity is the classic example of a function which is not efficiently realized in two-level gating. A two-level parity generator over eight variables would require 129 NAND gates! A more economical approach to the parity generation

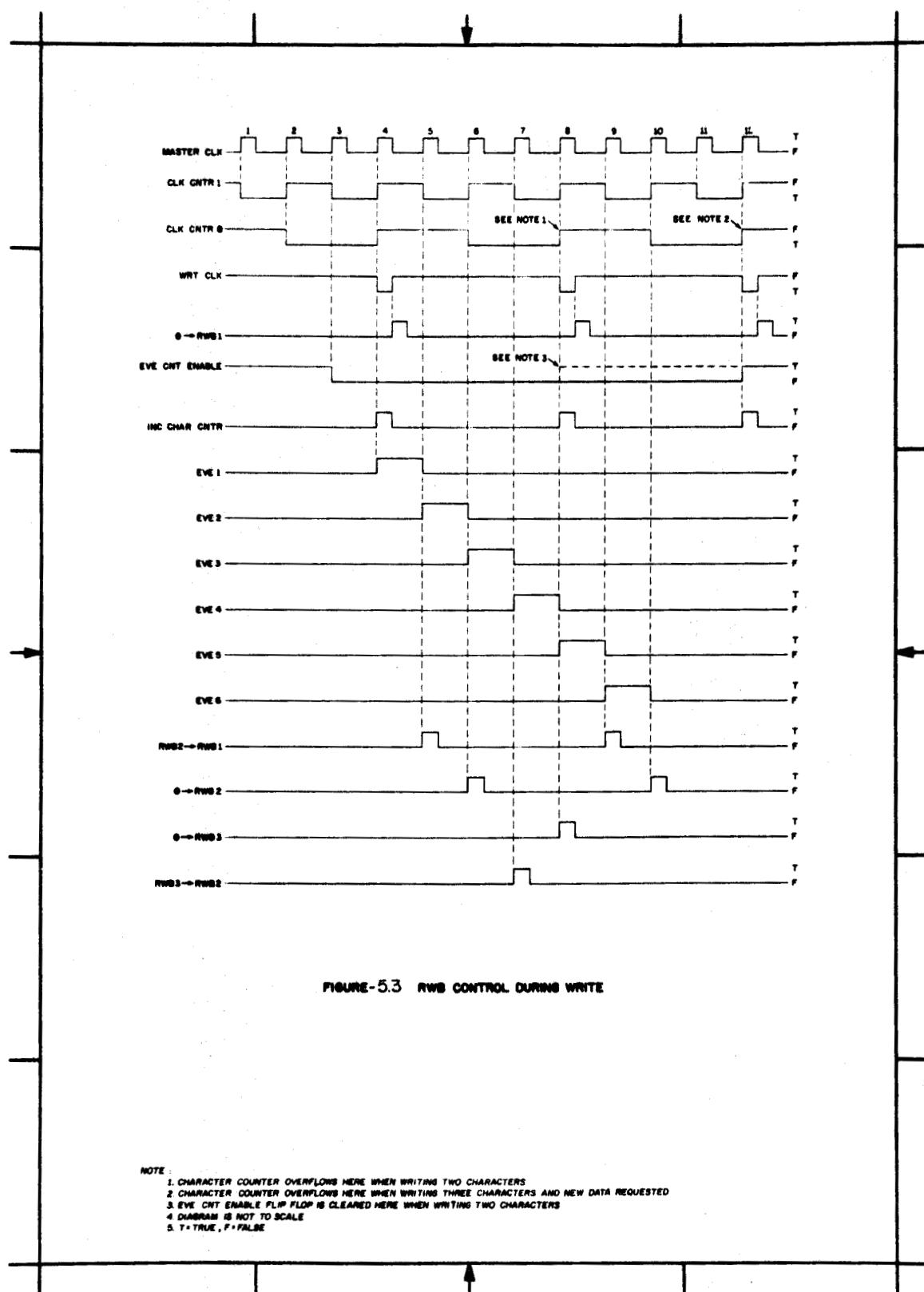


FIGURE-5.3 RWB CONTROL DURING WRITE

NOTE

1. CHARACTER COUNTER OVERFLOWS HERE WHEN WRITING TWO CHARACTERS
2. CHARACTER COUNTER OVERFLOWS HERE WHEN WRITING THREE CHARACTERS AND NEW DATA REQUESTED
3. EVE CNT ENABLE FLIP FLOP IS CLEARED HERE WHEN WRITING TWO CHARACTERS
4. DIAGRAM IS NOT TO SCALE
5. T = TRUE, F = FALSE

problem is to employ a process of repeated half addition (Exclusive OR) on the variables (see (6) for a complete discussion on parity generation).

As the data is always written from RWB 1, the first four Exclusive OR gates monitor the contents of RWB 1. The partial sums of the first two bit pairs are fed into the fifth Exclusive OR gate while the partial sums of the last two bit pairs are fed into the sixth Exclusive OR gate. The seventh Exclusive OR gate monitors the outputs of the 5th and 6th gates to obtain the half added result of the 8 data bits. The ninth gate half adds this result with the Parity bit of the Command Register such that the final result is the odd or even parity bit of the 8 data bits as specified by the Command Word. Whenever the CLOCK COUNTER reaches 3 the parity bit is strobed into a flip-flop from where it will be written onto the tape. It is worthwhile pointing out that writing occurs on every fourth MASTER CLOCK pulse and that the parity information is ready in the flip-flop one clock period before the actual writing. For all practical purposes this parity flip-flop can be considered to be an extension of the RWB 1. At this point it may be pointed out that a flip-flop is used to hold the parity bit instead of writing directly the output of the parity generator, because while writing the CRC character and the EOF character, the data parity generation circuits are bypassed; the appropriate characters (including parity) are loaded directly into the RWB 1 for writing on the tape.

5.8 Cyclic Redundancy Character Generation:

As mentioned previously, the Cyclic Redundancy Character Register is provided in the tape control for the CRC generation. This

nine bit register is used to calculate the CRC character while writing data on the tape according to the following rules⁽⁷⁾:

- (a) Initially the CRC register is clear.
- (b) All the data characters (data character includes the vertical parity) are added to the contents of the CRC register without carry (half addition).
- (c) Between such additions, the contents of the CRC register are rotated (not normal shifting) one position to the right (CRC P to CRC 0 etc. and CRC 7 to CRC P).
- (d) If the rotation in (c) will cause the CRC P bit to become a '1', the bits being rotated into the positions CRC 2, CRC 3, CRC 4 and CRC 5 are inverted.
- (e) After the last data character has been added, the CRC register is rotated once more in accordance with the steps (c) and (d).
- (f) To write the CRC character on the tape, the contents of all the bit positions except CRC 2 and CRC 4 are inverted.

Drawing 6.16 shows the CRC register configuration together with all the gating necessary for rotating the contents of CRC and communicating with RWB 1.

The signals $0 \rightarrow$ CRC to clear the CRC register, RWB \rightarrow CRC to transfer the data character into the CRC, ROTATE CRC to rotate the contents of the CRC register and CRC \rightarrow RWB to transfer the contents of the CRC into RWB 1 for writing on the tape, are shown on Drawing 6.17.

5.8.1 CRC register

As can be seen from Drawing 6.16, the flip-flops used to construct the CRC register have 4 DCD gates, two on the set and two on the reset side. The level inputs of the inner set of DCD gates are connected together and are fed from the corresponding bit of the RWB 1,

so that when the common pulse line is excited by the RWB → CRC pulse, the data character will be Exclusively OR'ed into the CRC register. Thus, if the RWB 10 is a '1', the level inputs of the inner set of DCD gates of the CRC 0 will be at ground and when the RWB → CRC pulse occurs, CRC 0 will be complemented (i.e. RWB 10 is half added with CRC 0 and the result is left in CRC 0). The level inputs of the outer set of DCD gates are obtained from the '1' and '0' outputs of the previous bit to perform the rotation except for the CRC 2 through CRC 5 and CRC P. The CRC P is connected to the CRC 7 for rotation, while the others obtain their level inputs from a gating network to comply with rule (d). Because the contents of the CRC 7 will appear in CRC P after rotation, rotation into the CRC 2 through CRC 5 is controlled by the outputs of CRC 7. If this happens to be a '1', the content entered into CRC 2 through CRC 5 is the complement of the previous bit. Thus, if CRC 7 is a '1' and CRC 1 is a '0' before rotation, a '1' will appear in CRC 2 when the rotation is complete. On the other hand, if CRC 7 is a '0', the preceding bit will be entered into the CRC 2 through CRC 5 positions.

When the CRC control (Drawing 6.17) generates the CRC → RWB pulse, all the CRC bit positions except CRC 2 and CRC 4 are gated in the complement form into the corresponding positions of RWB 1 to obtain the Cyclic Redundancy Check Character.

5.8.2 CRC register control signal generation

When the CLOCK COUNTER overflows (this is the write time), the CRC control generates the RWB → CRC pulse to perform the half addition between the data character and the CRC Register. The RWB → CRC pulse also triggers a 2 microseconds delay. At the end of this delay the ROTATE CRC signal is generated, to rotate the contents of the CRC Register. This delay is provided to allow for the settling of the CRC Register from the half addition performed by the RWB → CRC pulse. After writing the last data character in a record, the real time clock which provides the MASTER CLOCK signals is switched off, by clearing the CLOCK ENABLE flip-flop (see section 5.11).

When the writing is at 800 bpi, resetting the CLOCK ENABLE triggers a 5 microseconds delay. After completing this delay the CRC control generates the CRC → RWB pulse and triggers the CRC delay. The CRC → RWB pulse is used to load the contents of the CRC Register into RWB 1 (see section 5.8.1). The 5 microseconds delay from the time the CLOCK ENABLE flip-flop is cleared and the CRC → RWB pulse is generated, is to ensure that the last data character has been written on the tape and the RWB 1 is cleared before loading the CRC character into it. The CRC delay when complete, generates the WRITE TIME pulse (see Drawing 6.11), which triggers the WRITE PULSER to write the CRC character and clear the RWB 1.

It should be noted that the CRC → RWB pulse is generated only during a 800 bpi operation because the CRC character is required only for IBM compatibility (see section 3.6). The CRC delay is chosen equal

to 95 microseconds so that together with the aforementioned 5 microseconds delay a total of 100 microseconds of delay will be obtained between the last data character and the CRC character. This time is equal to the 4 character spaces required for IBM compatibility of 800 bpi tapes running at a speed of 50 inches per second. Figure 5.4 shows the timing diagram for the CRC control signal generation.

5.9 Data Break Interface and Control:

The Data Break facility of the PDP-8 allows one input-output device to communicate directly with the core memory on a cycle stealing basis. The tape control unit, which can control two transports, is treated as a single device.

5.9.1 Data break interface

Information flow to effect a Data Break transfer with an input-output device, appears in Figure 5.5. In general terms, to initiate a Data Break transfer, the interface must provide the following information:

- (a) Specify the affected address in the core memory.
- (b) Provide the data word by establishing the proper logic levels at the computer interface.
- (c) Provide the necessary gating to receive the word for a transfer from the computer.
- (d) Provide a logical signal to indicate the direction of transfer (in or out of the computer).
- (e) Provide a logical signal to indicate single cycle or three cycle break operation.
- (f) Present a proper signal to request a Data Break.

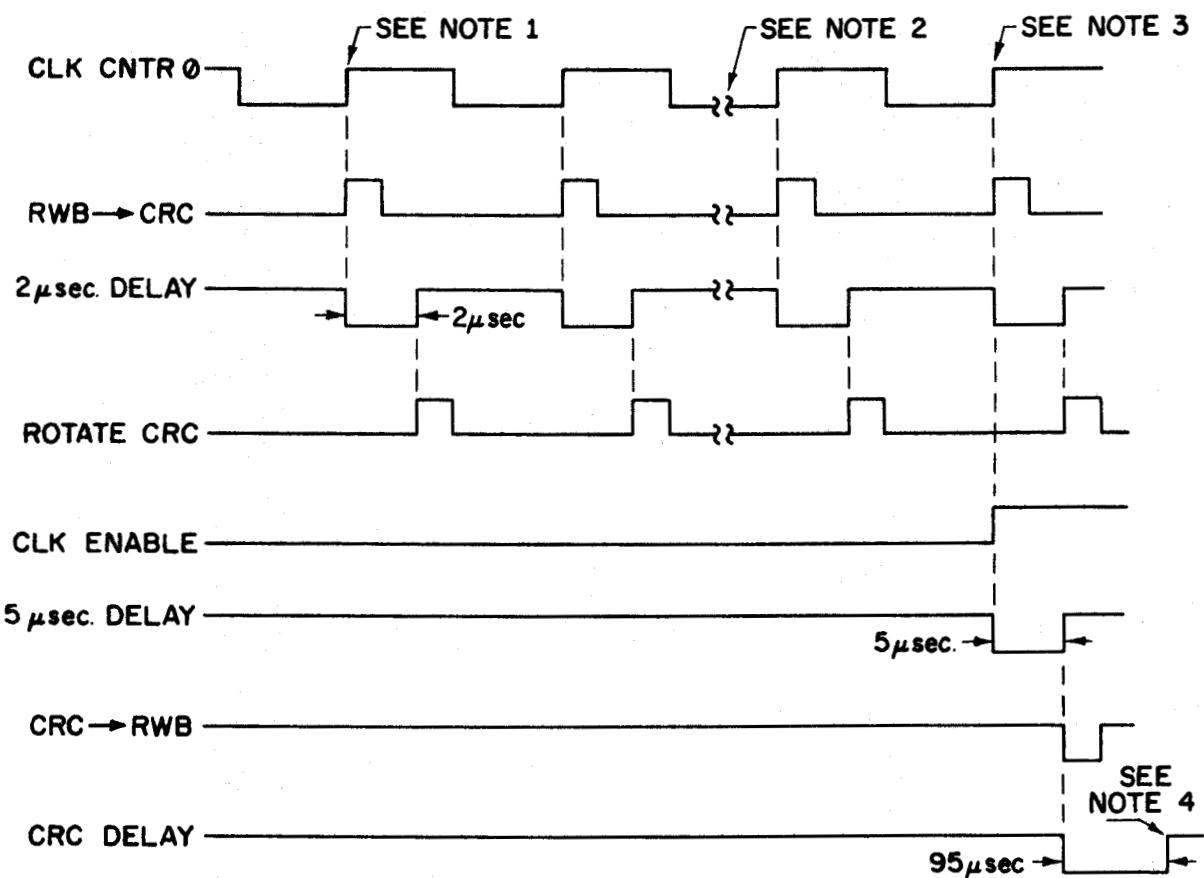


FIGURE 5.4 CRC REGISTER CONTROL TIMING

NOTE:

1. INDICATES CLK CNTR OVERFLOW
2. BREAK TO INDICATE WRITING IN PROGRESS
3. LAST DATA CHARACTER IS WRITTEN
4. CRC IS WRITTEN AT THIS TIME
5. DIAGRAM IS NOT TO SCALE

Because the tape control unit uses the three cycle Data Break, only the sequence of operations performed by the three cycle Data Break facility of the PDP-8 is listed here.

- (a) An address is read from the device to indicate the locations of the Word Count (WC) register and an Address Accepted pulse is generated. This register is always the same for a given device; thus it can be "hard-wired" instead of using a flip-flop register.
- (b) The contents of the specified address is read from the core memory and a 1 is added before rewriting. If the result of this addition happens to be a zero, a WC overflow signal will be generated. To transfer a block of N words, the WC is loaded with the 2's complement of N during programmed initialization of the device (see chapter 4). After the block has been transferred, this pulse is generated to signify the completion of the required transfers.
- (c) The next sequential core memory location is read as the Current Address (CA) register. Although the contents of this register are incremented by 1 before rewriting, an Increment CA Inhibit ($+1 \rightarrow CA\ INH$) signal may inhibit the incrementation. To transfer a block of data beginning at location SA, this register is program initialized by loading (SA - 1).
- (d) The content of the previously read Current Address is loaded into the Memory Address Register to serve as the address for the data transfer in the specified direction.

Drawing 6.18 shows the Data Break control signal interfacing. As mentioned earlier, the address specifying the location of the WC register in the core memory is hard-wired. The appropriate DATA ADDRESS bits (DATA ADD 0 through DATA ADD 11) are connected to ground to obtain 7752 in octal code (see section 4.4.1). Because the tape control unit always uses the three cycle Data Break, the CYCLE SELECT signal is also connected to ground. As the data transfers into the computer are needed only during a Read operation, the DIRECTION signal is obtained from the READ output of the function decoder (see Drawing 6.5). The $+1 \rightarrow CA\ INH$

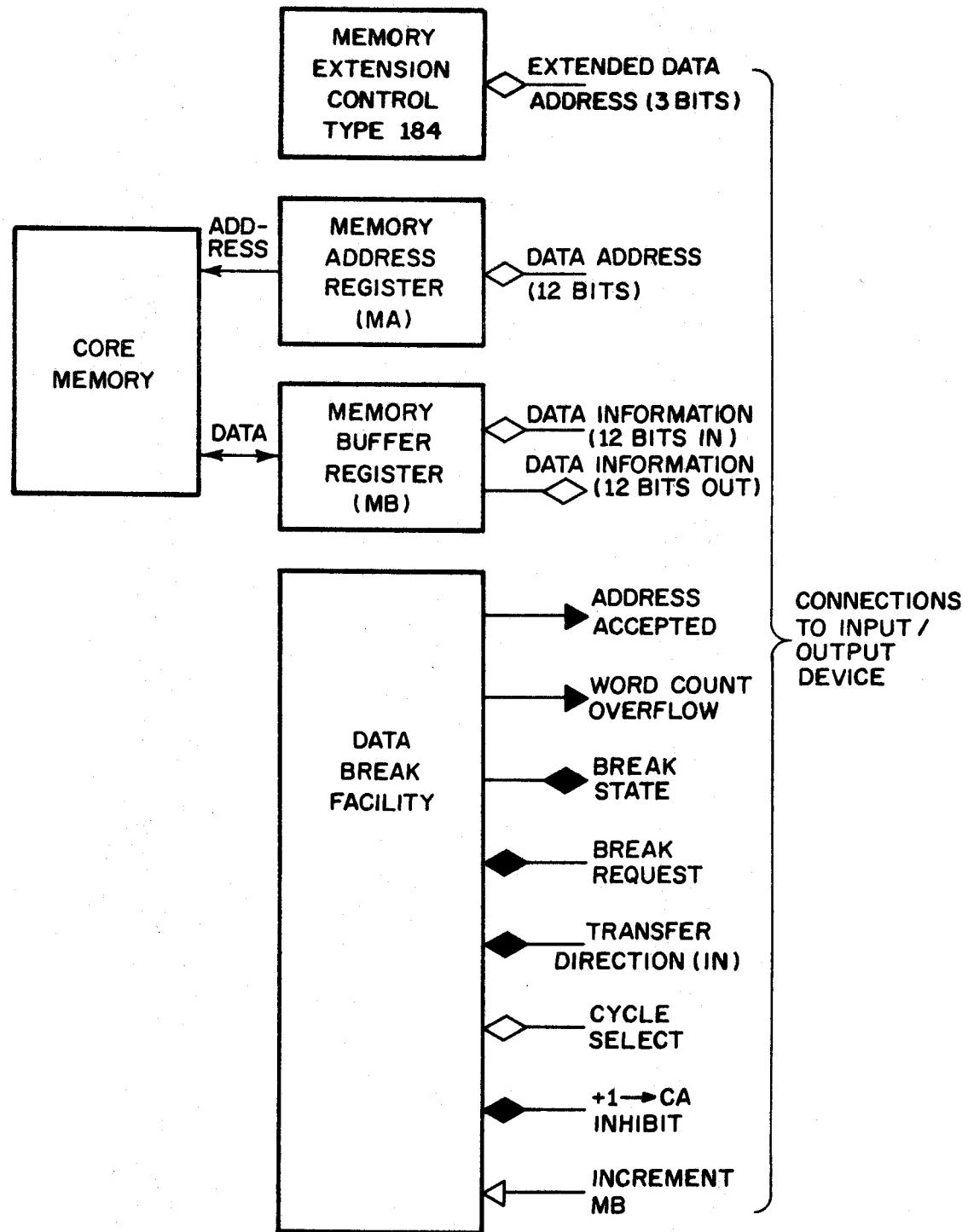


FIGURE 5.5 DATA BREAK TRANSFER INTERFACE
BLOCK DIAGRAM

signal is made false during a Write or Read or Read Compare operation so that transfers will take place from the successive core memory locations. The pulse ADDRESS ACCEPTED (ADD ACC) and WORD COUNT OVERFLOW (WCO) are inverted to make these signals available to the other parts of the control in either polarity. The BREAK REQUEST (BRK REQ) signal is generated from the DATA FLAG (DF) flip-flop output. This flip-flop is set whenever a request is to be conveyed to the computer. The control of the DATA FLAG is explained in detail in section 5.9.3.

Drawing 6.19 shows the interface to present data to the computer. As mentioned in section 5.7, data is transferred into the computer from a 24 bit Read/Write Buffer as two 12 bit words. There is a BREAK COUNT (BRK CNT) flip-flop in the tape control to determine the number of transfers taking place (see section 5.9.2). This flip-flop will be '1' for the first word transfer and a '0' for the second word. The outputs of RWB 10 through RWB 23 are gated with the '1' side of the BRK CNT flip-flop and the outputs of RWB 24 through RWB 37 are gated with the '0' side to obtain the signals DATA BIT 0 through DATA BIT 11. These are the inputs to the Memory Buffer of the computer so that the computer will read RWB 10 through RWB 23 as the first word, and RWB 24 through RWB 37 as the second word, during a Read operation.

5.9.2 Break count flip-flop and its control

The tape control is designed to operate normally on a "two words at a time" basis, i.e. when obtaining data from the computer it always tries to extract two words, and while feeding data tries to

supply two words into the computer. The contents of the WC and the number of characters in a record on the tape determine whether two transfers desired by the control can be allowed or not. The BREAK COUNT (BRK CNT) flip-flop shown on Drawing 6.20 is used to keep an account of the number of transfers (one or two) taking place. This flip-flop is inactive and remains cleared while rewinding or spacing the tape, as no data transfers take place during these operations.

First, consider the role played by the BRK CNT flip-flop during a Read operation. When the data from the tape is assembled in the Read/Write Buffer and ready for a transfer, the DATA FLAG is set (see section 5.9.3). The computer senses this and responds with an ADD ACC pulse, which triggers a 1 microsecond delay to generate the DELAYED ADD ACC signal. Because the operation selected is assumed to be Read (i.e. not a spacing operation), the level inputs of the BRK CNT flip-flop input gates are at ground and the DELAYED ADD ACC signal complements the flip-flop, thus setting it. This enables the gates that transfer the contents of RWB 10 through RWB 23 on to the computer input lines. The computer goes through the WC and CA cycles (to increment the CA and WC registers). If the Word Count did not overflow during this transfer, the DATA FLAG is left set so that when the computer finishes taking in the first word during the Break cycle (following WC and CA cycles), it re-enters the WC cycle and furnishes another ADD ACC pulse. This generates the DELAYED ADD ACC signal again to complement the BRK CNT flip-flop which will become zero. This enables the second set of gates to transfer the contents of RWB 24

through RWB 37 on to the computer input lines. As two transfers are complete, the DATA FLAG is cleared and the present cycle of operation is complete.

Now, consider the case if a Write or Read Compare operation is selected. The BRK CNT flip-flop is in the complementing mode as before. When the computer transmits the first ADD ACC pulse, the BRK CNT flip-flop is set to 1 by the DELAYED ADD ACC signal. After completing the WC and CA cycles, the computer enters the Break cycle and the signal called BREAK (provided by the computer) becomes true. When the operation selected is Write or Read Compare and the computer is in Break state, the signal called ENABLE BMB \rightarrow RWB is generated. This signal is the conditioning input to a gate driven by the BT2A pulses. These pulses are derived from the computer memory timing control and are available to the user. When the ENABLE BMB \rightarrow RWB signal is true, the BMB \rightarrow RWB pulse is generated using the BT2A pulse. If the control requests data, it is available in the Memory Buffer at BT2A time during the Break cycle. The BMB \rightarrow RWB pulse is gated with the outputs of the BRK CNT flip-flop to obtain the BMB \rightarrow RWB 1-2 and BMB \rightarrow RWB 2-3 pulses. During the first word transfer the BRK CNT flip-flop is in '1' state and hence the first BMB \rightarrow RWB signal generates the BMB \rightarrow RWB 1-2 pulse. This gates the Memory Buffer outputs into RWB 10 through RWB 23. If the Word Count did not overflow during this transfer, the computer re-enters the WC cycle, and transmits a second ADD ACC signal, thus complementing the BRK CNT flip-flop once again, which will become

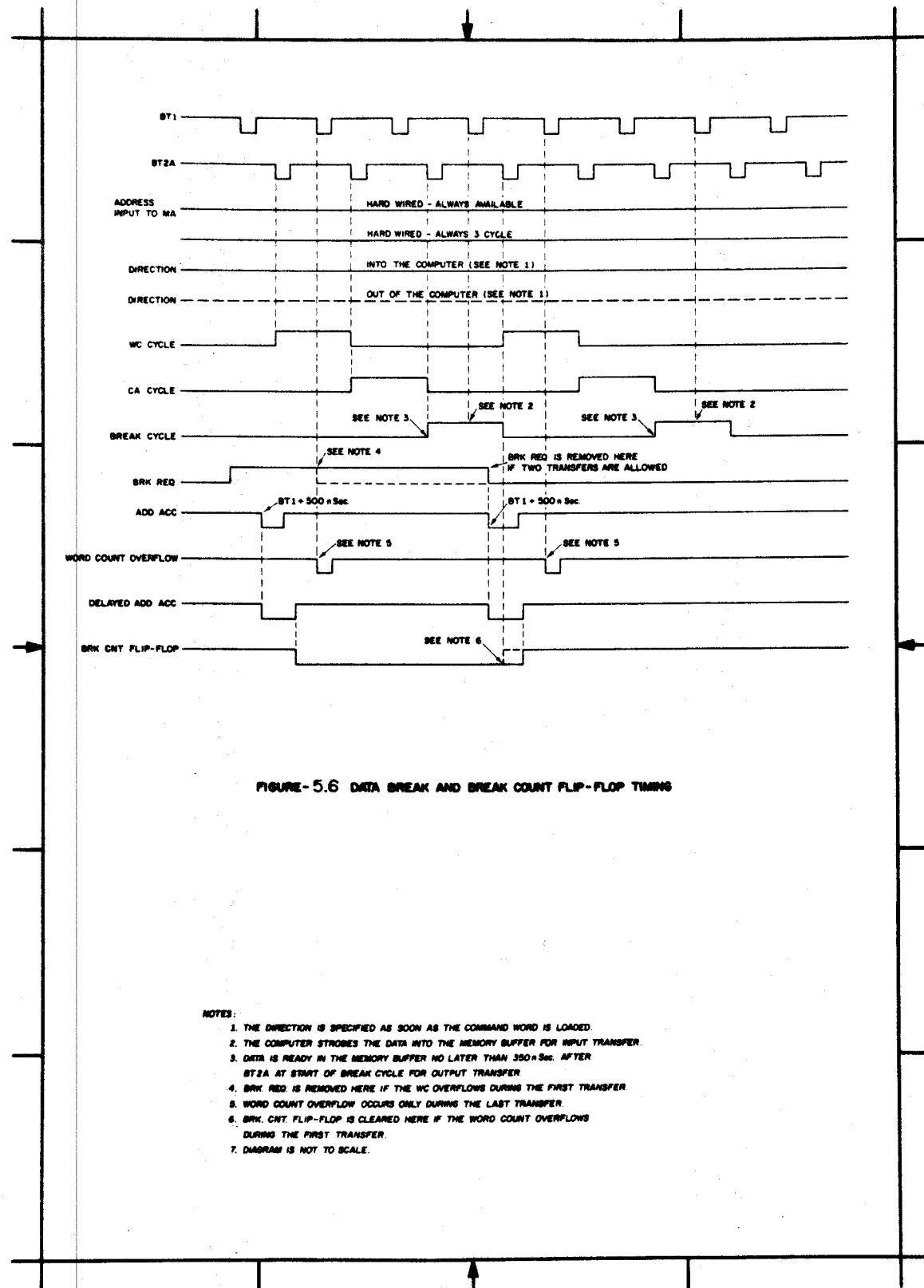
zero. The BRK CNT flip-flop control this time generates the BMB → RWB 2-3 at BT2A time during the Break cycle, to transfer the contents of the Memory Buffer into RWB 24 through RWB 37.

If the Word Count Overflow has occurred (this will be during the WC cycle), the signal called ENABLE 0 → BRK CNT is generated. This gates the BT2A pulse to generate the 0 → BRK CNT signal which clears the BRK CNT flip-flop. Generating the 0 → BRK CNT signal as indicated, ensures that if the Word Count Overflow occurred during the first transfer the BRK CNT flip-flop is left in the '1' state so that transfers occur only between RWB 10 through RWB 23 and the Memory Buffer. Figure 5.6 shows the timing diagram of the BRK CNT flip-flop control. As can be seen on this diagram, the second ADD ACC pulse is generated 500 nanoseconds after the BT1 pulse and the computer is still in the first Break Cycle.

Complementing of the BRK CNT flip-flop is delayed 1 microsecond from the time an ADD ACC is received, to ensure that the BRK CNT flip-flop does not change its state until the Break cycle is complete (it will be approximately 200 nanoseconds after receiving the second ADD ACC pulse). This is necessary because the BMB → RWB is generated from the BT2A pulse occurring at the end of the Break cycle.

5.9.3 Data flag and its control

The tape control requests access to the computer by setting the DATA FLAG (DF). The Word Count Overflow pulse generated by the computer during the Word Count cycle sets the WORD COUNT OVERFLOW (WC OV)



flip-flop which is also shown on the same drawing (see Drawing 6.21).

If the WCOV flip-flop is not set, the level input of the DCD gate on the set input of DF is true and the flag can be set by the $+1 \rightarrow DF$ pulse. The $0 \rightarrow DF$ signal always clears the DATA FLAG.

If the operation selected is Read, three characters from the tape are loaded into the Read/Write Buffer (see section 5.7). The buffer is now full and the control is ready for a transfer. As the CHAR CNTR is counting the number of characters entering the RWB, it will reach a count of 3 as soon as the third character is in the RWB and the CHAR CNT 3 signal becomes true. This triggers a gate to generate the $+1 \rightarrow DF$ pulse to set the DF and request a data break.

In response to this request the computer generates an ADD ACC pulse, which tries to generate the $0 \rightarrow DF$ pulse. At this point the BRK CNT flip-flop is still in zero state, because it is complemented by the delayed ADD ACC signal, and $0 \rightarrow DF$ pulse generation is inhibited. The computer cycles through the WC, CA and Break cycles are explained previously. If the Word Count Overflow signal occurs during this first transfer, the DATA FLAG is cleared. If this did not happen the computer re-enters the WC cycle because the DF is not cleared and transmits the second ADD ACC pulse during the first Break cycle. When the second ADD ACC pulse is received, the BRK CNT is in '1' state and enables the gate to generate the $0 \rightarrow DF$ pulse which clears the DATA FLAG. This is the second character, and the DATA FLAG must once more be set by the CHARACTER COUNTER to request any more access.

At this state, the generation of the CLEAR ALL signal (see section 5.7.3) must be reconsidered. This signal is generated with the BT2A pulse during a Read operation, whenever the computer enters the Break cycle with the DATA FLAG clear. This condition signifies the completion of the required number of transfers during this cycle (that is why the DF is clear) and the CLEAR ALL signal initializes the CHARACTER COUNTER in preparation for the next cycle of operation. The CLEAR ALL signal also clears the RWB in preparation to read more data.

During a Read operation an IRG could have been encountered without the CHARACTER COUNTER reaching a count of 3. This would happen for the last two characters, if the number of characters in a record represents an odd number of words. In that case, the CHARACTER COUNTER will be holding a count of 2 and the IRG signal sets the DATA FLAG. If only two characters are read and IRG is encountered, then only one 12 bit word is to be transferred, thus ignoring the zeros inserted by the control to fill up a character (see section 4.3). The ADD ACC signal generates the $0 \rightarrow DF$ pulse if the CHAR CNTR is 2, thus removing the BRK REQ.

The case when the operation selected is Write should now be considered. The data is not required immediately after initiating the Write operation by the GO command, because appropriate lengths of blank tape must first be generated. There are three type of gap delays in the control for this purpose, which directly affect the DATA FLAG

(see section 5.12).

- (a) When the Write operation is initiated with the tape at the BOT marker, the load point gap must be generated. The BOT DELAY is used to generate this gap.
- (b) When the tape has been stopped after an operation, the read and write heads are located in the IRG (see section 5.12). If writing is initiated from this position, the remainder of IRG must be written and IRG DELAY 1 signal is used to generate this gap.
- (c) When writing in Continuous Mode, the tape is not stopped in an IRG and the IRG DELAY 2 signal is used to identify that the required gap has been generated.

Any of these signals, i.e. BOT DELAY, IRG DELAY 1, or IRG DELAY 2 can trigger the $+1 \rightarrow DF$ pulse and request a break. The control tries to extract two words from the core by not clearing the DF until the second transfer is complete using the BRK CNT flip-flop as explained previously. However, as the number of words supplied by the computer is determined by the WC, the control is forced to generate the $0 \rightarrow DF$ pulse if the Word Count Overflows, thus aborting its attempt to get a second word. In any case the writing proceeds, as explained in the earlier sections. If two words are supplied by the computer without a Word Count Overflow, request for more data is made by setting the DF using the $0 \rightarrow EVE$ CNT ENABLE signal (see section 5.7.2). While obtaining data, the control also loads the CHAR CNTR with 2's complement of the number of characters to be written (see section 5.7.1) and the $0 \rightarrow EVE$ CNT ENABLE is generated when the CHAR CNTR reaches zero, signifying that the data from the RWB has been emptied onto the tape.

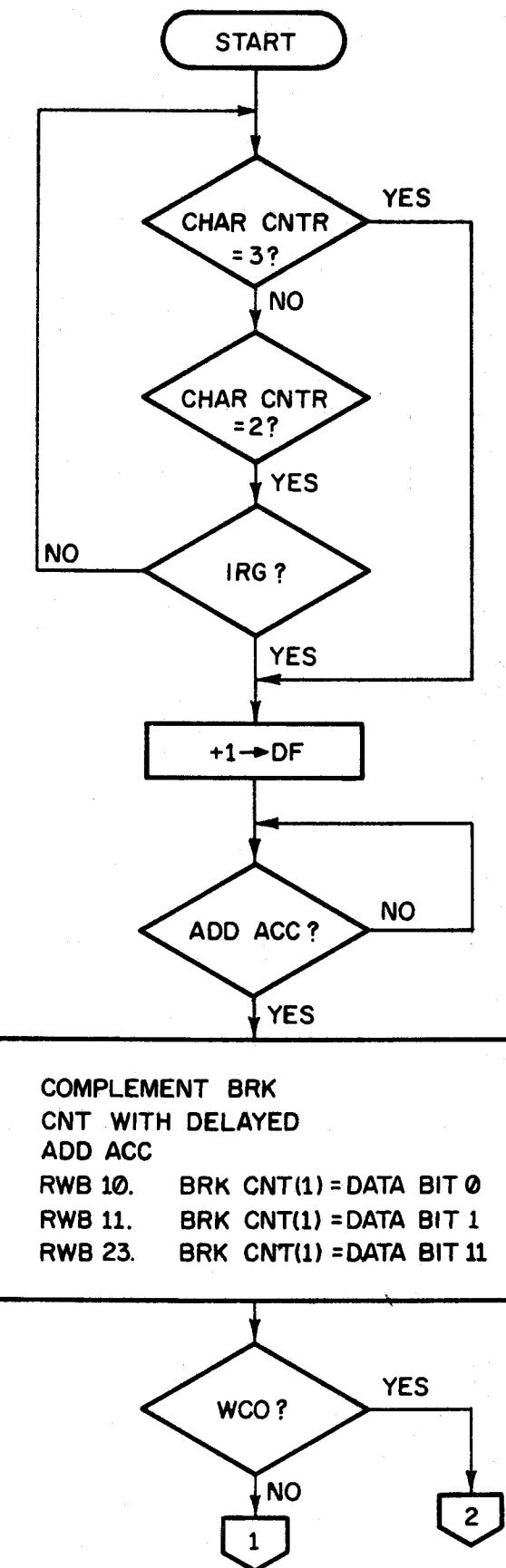
During a spacing operation, no data transfers occur between the tape control and the computer. But the WC register in the core memory is used to count the number of records spaced and hence the $+1 \rightarrow DF$ is generated only by the IRG signal while spacing. The DATA FLAG is cleared immediately after receiving the ADD ACC signal, thus incrementing the WC once for every record spaced.

During a Read-Compare operation, the DATA FLAG is set when the CHAR CNTR reaches 3 or when an IRG is encountered when the CHAR CNTR is holding 2. The first ADD ACC pulse clears the DATA FLAG. This is in preparation for discontinuing comparisons in case there is a comparison failure. During the Break cycle, the control obtains the first word from the computer and compares it with the contents of RWB 10 - RWB 23. Because the DATA FLAG is already cleared, the computer does not re-enter the WC cycle. If the first comparison is successful, another request is made by the Read-Compare control logic (see section 5.10).

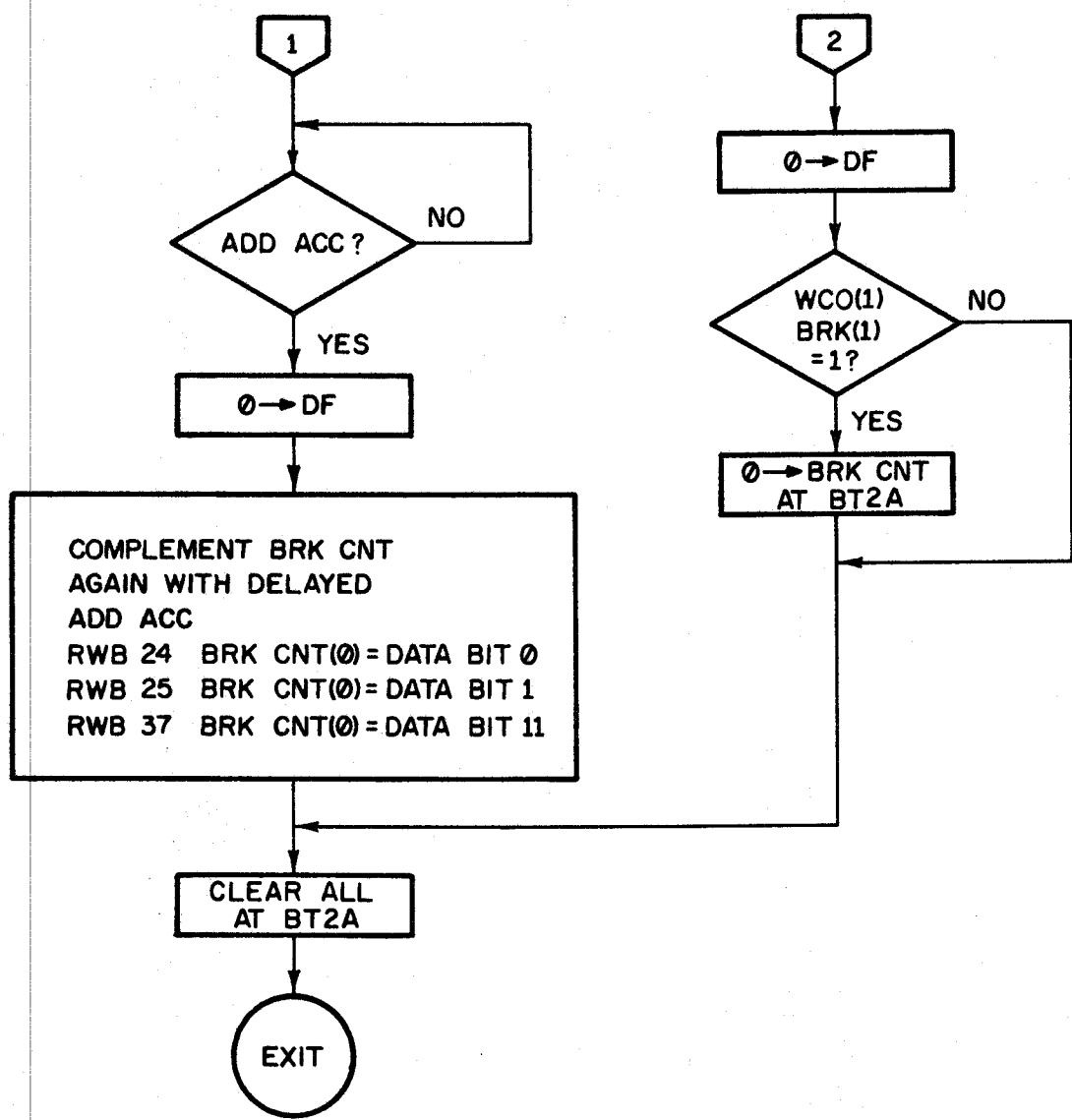
Flow charts 4 and 5 summarize the Data Break control during Read, Write operations respectively. Refer to section 5.10 for Data Break control during a Read Compare operation.

5.10 Read/Compare Control:

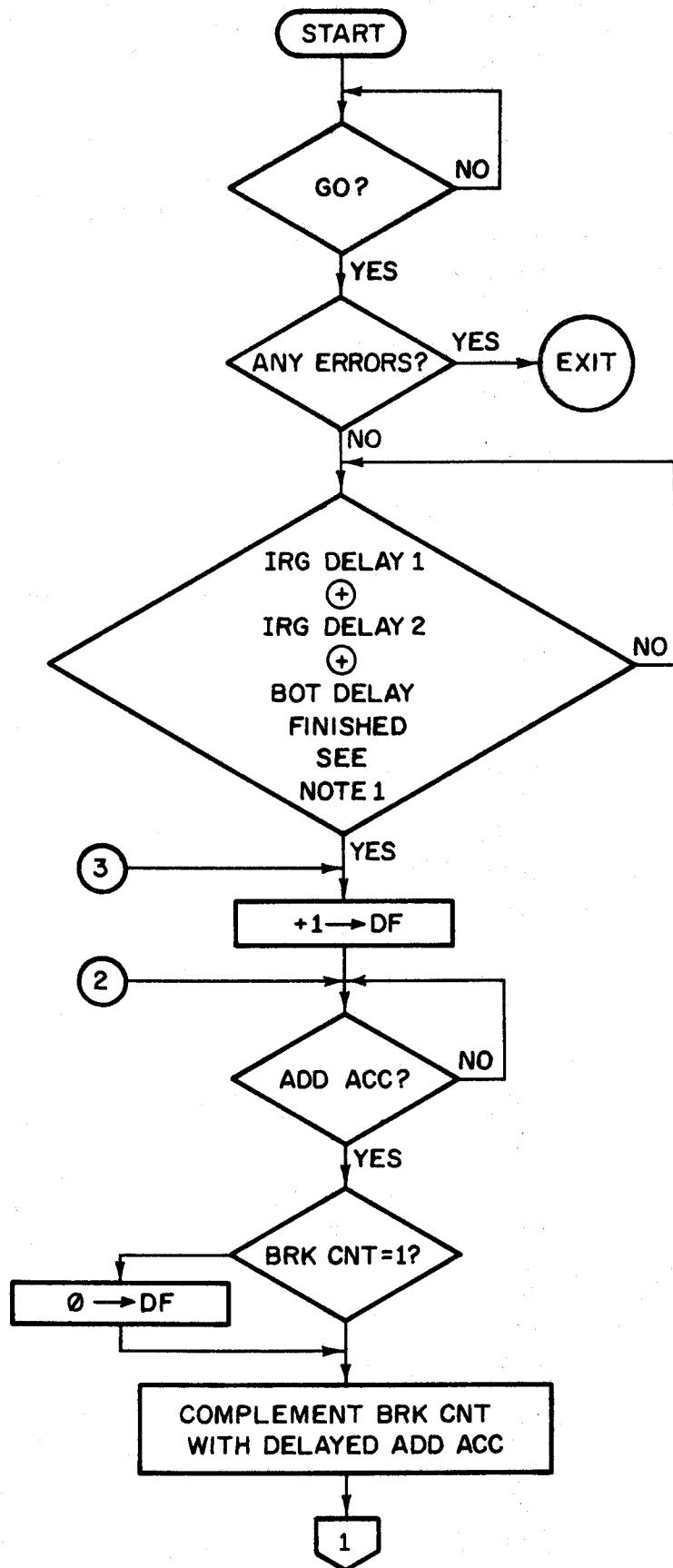
The Read/Compare operation described in section 4.4.3 can be treated as a combination of the Read and Write operations in the sense that data is read from the tape as in a Read operation, and data is obtained from the computer as in a write operation.



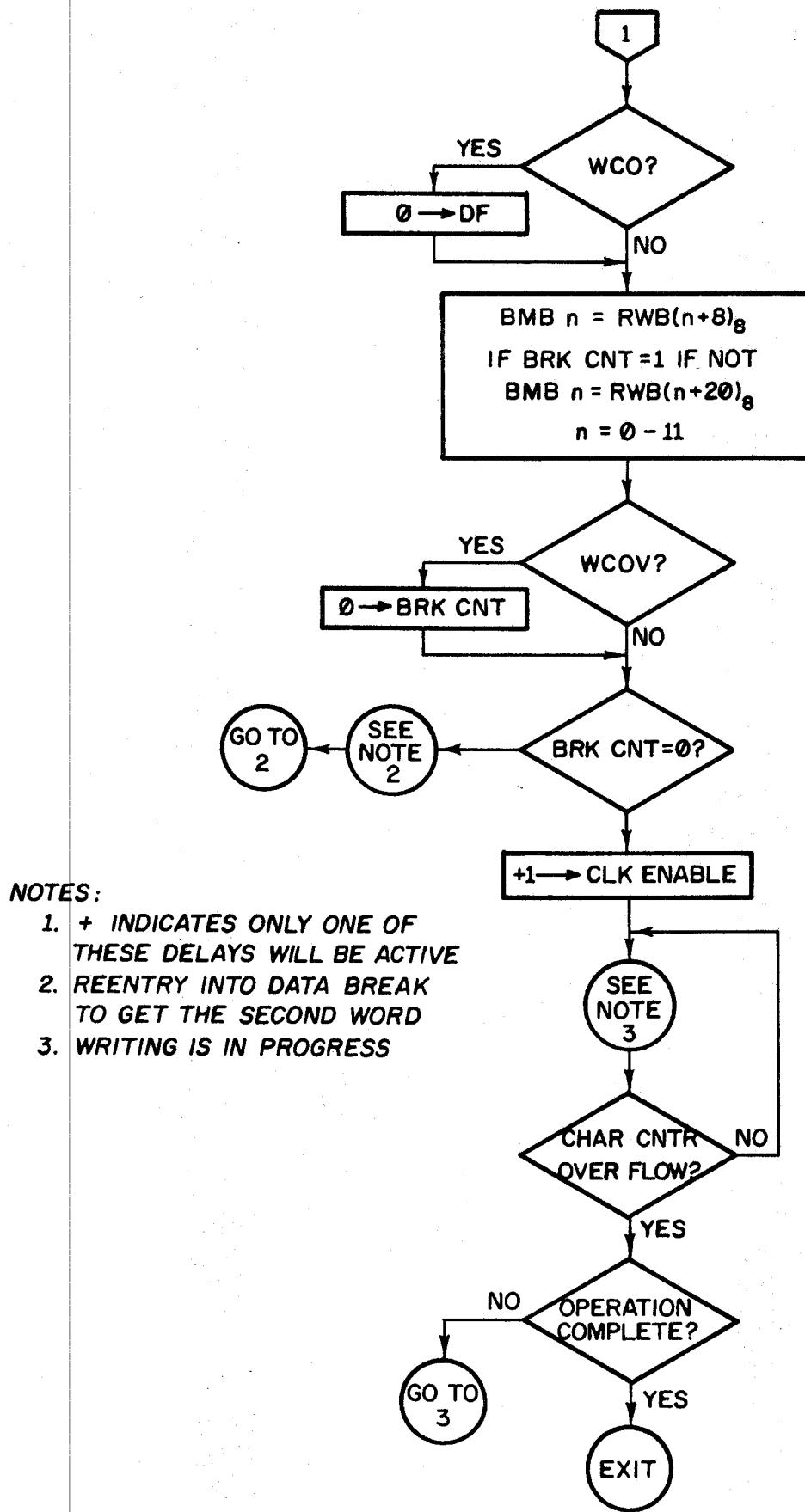
FLOW CHART 5.4 DATA FLAG CONTROL DURING READ (CONT'D)



FLOW CHART 5.4



FLOW CHART 5.5 DATA FLAG CONTROL DURING WRITE(CONT'D)



FLOW CHART 5.5

The comparison makes use of the fact that the half addition of two equal binary numbers will always result in a zero. In other words

$$A \oplus B = 0 \quad \text{if } A = B \quad \dots (5.3)$$

Where A and B are the binary numbers, and

\oplus indicates the half-addition.

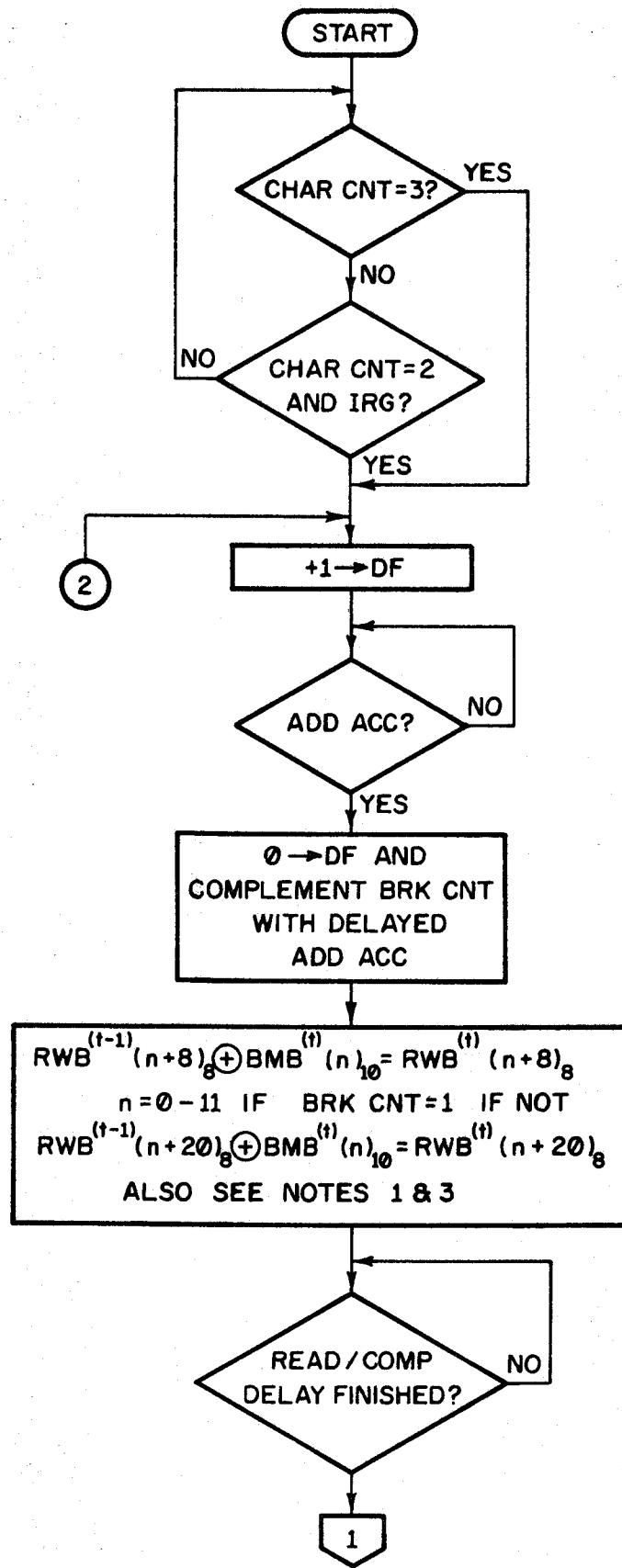
During a Read Compare operation, the data is read from the tape and when the Read/Write Buffer is loaded with the first three characters, the DATA FLAG is set (see section 5.9). The computer responds with the ADD ACC pulse and the DATA FLAG is cleared. During the Break cycle, the control generates the BMB \rightarrow RWB 1-2 pulse as explained in section 5.9.2. This pulse half adds the contents of the Memory Buffer with RWB 10 - RWB 23 and leaves the result in the latter (note that during a Write operation RWB is clear before the data is loaded). By virtue of (5.3), the contents of RWB 10 - RWB 23 should be zero, if the first word assembled from the tape and the computer agree. There is a 13 input gate which monitors the outputs of RWB 10 - RWB 23 for zero when the BRK CNT flip-flop is set, and a signal called COMPARES OK is generated (see Drawing 6.22). During a Read Compare operation, the BMB \rightarrow RWB pulse (from which the BMB \rightarrow RWB 1-2 pulse is obtained) also triggers the COMPARE DELAY. This delay is to allow time for the half addition to be completed before the result is examined for zero. If the comparison is not successful, then the signal COMPARES OK is true and the signal +1 \rightarrow READ/COMPARE FAILED is generated, to set the appropriate bit in the Status Register. On the other hand

if the first comparison is successful, the control generates the +1 → DF signal instead of +1 → READ/COMPARE FAILED after the COMPARE DELAY, to request for the second word.

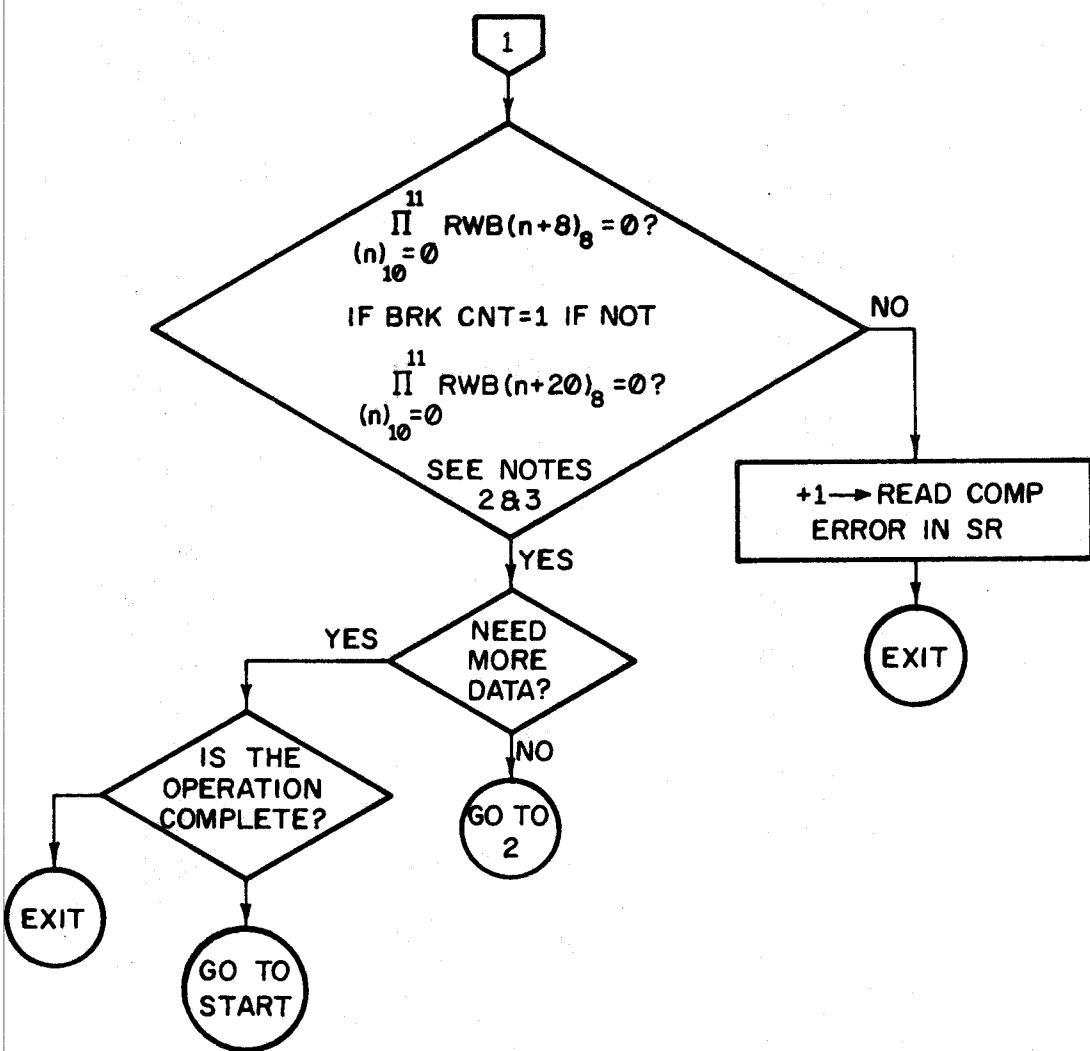
When the second word is received, it is half added with the contents of RWB 24 - RWB 37 using the BMB → RWB 2-3 pulse and the COMPARE DELAY is triggered once again. The contents of RWB 24 through RWB 37 are examined for zero using another 13 input gate, one of its input being the reset side of the BRK CNT flip-flop. If the second word comparison is unsuccessful, the +1 → READ/COMPARE FAILED pulse is generated as before. In any case, the control does not generate the +1 → DF pulse because this is the second word comparison and more data should come from the tape before the comparison can proceed. It is worthwhile remembering that once a comparison failure is detected, the DATA CLOCK generation is inhibited (see section 5.6), so that no more data breaks are requested by the CHARACTER COUNTER. The flow chart 5.6 summarizes the control functions performed during a Read Compare operation.

5.11 Density and Clock Control:

The desired density of operation is specified by the Command Word and the bits specifying the selected density are loaded into the density flip-flops (DENSITY 0 and DENSITY 1) as shown in Drawing 6.4. The contents of these flip-flops are decoded to obtain the signals 200 bpi SELECT, 556 bpi SELECT and 800 bpi SELECT which are delivered to the data electronics in the tape transports.



FLOW CHART 5.6 READ COMPARE CONTROL (CONT'D)



NOTES :

1. SUPER SCRIPT (t) INDICATES PRESENT
SUPER SCRIPT (t-1) INDICATES PREVIOUS
 \oplus INDICATES HALF ADDITION
2. \prod DENOTES REPEATED AND OPERATION
3. SUBSCRIPT DENOTES THE RADIX.

FLOW CHART 5.6

Drawing 6.4 also shows the three real time clocks (200 bpi CLOCK, 556 bpi CLOCK and 800 bpi CLOCK), which generate the actual timing pulses for writing. Whenever the corresponding ENABLE (200 bpi CLOCK ENABLE, 556 bpi CLOCK ENABLE or 800 bpi CLOCK ENABLE) signal is true, the selected clock becomes active and starts delivering the clock pulses until the ENABLE signal is removed. As mentioned in section 5.7.2 the clocks are adjusted to run at four times the frequency necessary to obtain the desired packing density. For example, the clock frequency should be 40,000 pulses per second to obtain 800 bits per inch packing, when the tape is running at 50 inches per second. Hence the 800 bpi CLOCK is adjusted to run at 160,000 pulses per second. The ENABLE signals for the clocks are derived from the density flip-flop outputs and the CLOCK ENABLE (CLK ENABLE) flip-flop as shown in Drawing 6.4.

The sole purpose of the CLOCK ENABLE flip-flop is to start the writing only after the data from the computer is received and stop the clocks only after writing the last data character on the tape. The CLOCK ENABLE is set by the BMB → RWB pulse (see section 5.9.2 where this signal generation is discussed) during a Write operation when the DATA FLAG is zero (zero DF indicates that the Read/Write Buffer is loaded for the present cycle). Setting this flip-flop enables the selected clock. The 0 → EVE CNT ENABLE signal is generated whenever the required number of characters is written in the present cycle (see section 5.7.3). If the Word Count Overflow has occurred during a Write operation (signifying that data for one complete record has been

received) the $0 \rightarrow$ EVE CNT ENABLE signal clears the CLOCK ENABLE flip-flop, thus disabling the clocks.

5.12 Write Control and Gap Generation:

To implement the Write or Write EOF operation, the tape control must specify the WRITE ENABLE signal to the data electronics. The erase head is energized in preparation for writing only when this signal is true in conjunction with the Write Lock Ring. Two signals UN1 WRT ENABLE and UN2 WRT ENABLE (see Drawing 6.24) are generated by gating the UNIT NO. bit of the Command Register with the WRITE + WRITE EOF signals from the function decoder, such that the WRITE ENABLE is specified on the selected tape unit when a Write or Write EOF operation is desired.

While writing, some blank tape must be generated to satisfy the various gap length requirements.

If an operation which involves writing on the tape is attempted from the BOT marker, the BOT DELAY is triggered using the GO DELAY. This delay is chosen to generate the required Load Point Gap, and requests for data are made only after completing this delay (see section 5.9.3), so that writing does not start until the required length of blank tape is generated.

When the tape is stopped in an IRG, the read head is located approximately in the middle of the gap due to the STOP DELAY (i.e. approximately 0.3 inches from the previous record). The write head is about 0.1 inches further from the read head (dual gap head), so that if writing is initiated from this position, approximately 0.2 inches

of blank tape must be generated to obtain the required 0.6 inches for an IRG. The IRG DELAY 1 is triggered by the GO DELAY whenever writing is attempted from a position other than the BOT marker to ensure that no data requests are made until the appropriate length of IRG is generated.

When the writing is done in Continuous Mode, the sum of the STOP and SHUTDOWN delays was chosen to be equal to the required IRG length (see section 5.4). The IRG DELAY 2 is triggered by the IOT 722 pulse when writing in Continuous Mode. The reason for providing this delay is not to generate any gaps, because the actual length of tape travel during this 1 microsecond delay is negligible (about 50 micro-inches). When the tape control has completed writing a record in Continuous Mode, the Job Done flag is presented at the end of the SHUTDOWN DELAY and the program issues a MTGO command to proceed with the writing (see chapter 4). The IOT 722 pulse generated by the MTGO command is used to reset the flags (see Drawing 6.25) and the Word Count Overflow flip-flop (see Drawing 6.21). Because the DF cannot be set by the +1 → DF pulse if the WCOV flip-flop is set, the IRG DELAY 2 is used to ensure that no attempt to set the DF is made until the WCOV flip-flop is reset.

There is a gap of approximately 4 character spaces between the last data character and the CRC character in a record. This gap is generated by the CRC DELAY as explained in section 5.8.2. A four character space gap is also required between the CRC and LRC characters in a record, thus locating the LRC about 8 spaces away from the last

data character. Three delay circuits (200 bpi LRC DELAY, 556 bpi LRC DELAY and 800 bpi LRC DELAY) are provided to generate the gap of 8 character spaces as shown on Drawing 6.24. When the CLOCK ENABLE flip-flop is cleared to switch off the real time clocks, one of these delays is triggered depending on the selected density of operation. These delays are adjusted to be equal to the required 8 character spaces at the selected tape density when the tape is moving at a speed of 50 inches per second. The LRC PULSER circuit is triggered at the end of the selected LRC DELAY, to drive the reset line of the selected tape unit (see Drawing 6.13) to clear the write flip-flops, thus writing the LRC on the tape (see section 2.6.4).

The delay required for an EOF gap is generated by the EOF writing control logic (see section 5.15). After writing the EOF code, the appropriate LRC DELAY is triggered once again to write the LRC character for the EOF code, thus making the EOF a single character record.

It is interesting to note that the LRC DELAY is chosen 8 character spaces from the last data character instead of 4 character spaces from the CRC character in a record for the following reasons:

- (a) The CRC character is not written in a record when operating the tape system at a density other than 800 bpi.
- (b) The CRC character is not required for the EOF record.
- (c) The same LRC DELAY modules can be used in writing the LRC character for the EOF record if the last data character is chosen as a reference point instead of the CRC character.

5.13 IRG Detection Control:

Detection of an IRG by the data electronics can be controlled by the EOB INHIBIT signal, the data electronics are prevented from generating a signal to indicate when IRG encountered, if this signal is true. Drawing 6.23 shows the IRG detection control logic centered around the EOB ENABLE flip-flop. Two signals UN1 EOB INH and UN2 EOB INH are derived from the EOB ENABLE flip-flop output and the data electronics are conditioned to signal an IRG when these signals are false. If either transport detects an Inter Record Gap, the corresponding signal (UN1 EOB IND or UN2 EOB IND) will be true. These two signals are multiplexed by an OR gate and shaped by a Schmitt trigger. The Schmitt trigger output is used by the tape control as the IRG signal.

The IRG detection control sequence is as follows:

- (a) The EOB ENABLE flip-flop is initially clear.
- (b) The first READ CLOCK pulse sets the EOB ENABLE flip-flop if the operation selected is not Space Reverse. This marks the beginning of a record.
- (c) The first two characters read will be the check characters if the operation selected is a Space Reverse. During this operation, the first READ CLOCK pulse (this will be the LRC) triggers one of the three CHECK CHARACTER DELAYS, depending on the selected density.
- (d) These delays are adjusted such that by the time the selected delay is complete, the CRC character has moved past the read head. The EOB ENABLE flip-flop is set at the end of the CHECK CHARACTER DELAY, and marks the beginning of data. This fact is used in the generation of DATA CLOCK pulses during a Space Reverse operation (see section 5.7.2).
- (e) The EOB ENABLE flip-flop is cleared when an IRG is detected in preparation for the next cycle of operation.

Setting of the EOB ENABLE flip-flop after the CHECK CHARACTER DELAY during a Space Reverse operation accomplishes the following objectives:

- (a) Prevents the data electronics from identifying the blank tape between the LRC and CRC as an IRG.
- (b) Supplies the DATA CLOCK generating logic a means of distinguishing the check characters from data.

5.14 Status Register and Associated Control:

As mentioned before, the control uses the Status Register to assemble the Status Word, which can be transferred into the computer on demand. The signals generated in the control to load the status information into the computer have already been explained (see section 5.2.1). This section contains details on how the current status of the tape system is monitored by the tape control.

5.14.1 Illegal condition detection

For a proper operation of the tape system, the control must ensure that a selected tape operation is legal before it is initiated.

There are a number of conditions in which a tape operation should not be initiated:

- (a) The Command Register specifies a Rewind or Space Reverse operation when the tape is at the BOT marker.
- (b) The Command Register specifies a Write or Write EOF operation but the Write Lock Ring is not in place (see section 2.5).
- (c) The Command Register specifies an unused density code.
- (d) The selected tape unit is not ready.
- (e) The errors from the previous operation are not cleared by the program.

If any of these conditions exist, the Illegal condition detection logic (see Drawing 6.27) generates the ENABLE ILLEGAL signal. When this signal is true, the IOT 722 pulse sets the ILLEGAL error bit in the Status Register (see Drawing 6.25).

Although the Command Register is protected from change when an operation is in progress (see section 5.3), the program should be made aware of such illegal attempts. The ILLEGAL error bit in the Status Register is also set whenever the RUN/STOP signal is true and the IOT 712 or IOT 714 pulses are generated (see Drawing 6.27).

5.14.2 Parity error detection

There are two types of parity errors that can occur in the tape system, vertical parity failure and horizontal parity failure.

(a) Vertical parity failure detection

The tape control receives the vertical parity failure indication from the data electronics (see section 3.6), as the UN1 PARITY IND and UN2 PARITY IND signals. Whenever either of these two signals is true, the signal SET PITY ERROR is generated to set the PARITY ERROR bit in the Status Register. To take into account the fact that the check characters may differ from the specified parity (see section 3.6), the SET PARITY signal generation is inhibited whenever the IRG signal is true, as shown on Drawing 6.27. As explained in section 5.13, the IRG signal is generated when the read head is located between the last data character and the CRC. The control ignores the parity failures indicated during the IRG signal period.

The PARITY ERROR bit in the Status Register can never be set whenever a spacing operation is selected, or when an EOF is detected. This can be appreciated by noting the fact that during a spacing operation, the accuracy of data is not important and when the EOF is detected, the parity error indication is not necessarily an indication of error in reading (the EOF is always written with odd parity and the CR might be specifying even parity).

It is important to note that the EOF code read during a spacing operation cannot be relied upon because the parity errors are ignored; the design of the tape control uses the fact that the EOF is a single character record (see section 5.14.3) instead of relying on the actual code for detecting the EOF.

(b) Horizontal parity

The tape control uses the LONGITUDINAL REDUNDANCY BUFFER (LRCB) for detecting any horizontal parity failures as shown in Drawing 6.26. The fact that every binary number representing an even decimal integer contains a '0' in its least significant position, has been used to design the horizontal parity checking scheme. The control treats the bits in the 9 bit LRCB as the least significant bit positions of 9 binary counters. Initially the buffer is clear and the control complements a LRCB bit whenever the bit read from the corresponding tape track is a '1'. If the LRCB is checked after reading all the characters (including the LRC) in a record, it should be zero if there are no errors.

To ensure that the buffer is checked only after reading the LRC character, the CHECK COUNTER flip-flop is used. The READ CLOCK pulses complement the flip-flop, if the IRG signal is true. When operating at 800 bpi tape density, this flip-flop will be zero after reading the LRC; if the selected density is other than 800 bpi, then it will contain a '1' after reading the LRC character (because there is no CRC if the density is not 800 bpi). The CHECK LRCB signal will be true after reading the LRC, thus enabling the gate monitoring the LRCB for zero. Concurrently with generating the CHECK LRCB signal, the CHECK DELAY is also triggered. If the LRCB is not zero, then the LRCB \neq 0 signal will be true. This signal enables the set side of the PARITY ERROR flip-flop in the Status Register (see Drawing 6.25). After the CEHCK DELAY of the LRCB \neq 0 signal is true, the PARITY ERROR bit in the Status Register is set.

5.14.3 EOF detection

The EOF is a single character record and is used to separate the data files from one another on the tape (see section 2.3). For IBM compatibility, the EOF character is written only with odd parity and if any tape operation specifies even parity in the Command Register, a Parity Error will be detected, when the control encounters the EOF code. To avoid this, the parity error is suppressed when the tape encounters the EOF. But the fact that the error checking scheme is ignored, makes the accuracy of the character read for EOF detection questionable. To avoid these problems, a scheme which does not involve relying on the

actual code for EOF detection is used, by making use of the property that EOF is the only record on the tape which has a single character as data. By virtue of the formatting scheme chosen, there are no single character data records (see section 4.3) to conflict with the EOF detection scheme.

The EOF bit of the Status Register is set whenever an Inter Record Gap is encountered and the CHAR CNTR is holding a count of 1. (see Drawing 6.25).

To initialize the CHARACTER COUNTER during spacing operations, the signal called $0 \rightarrow \text{CHAR CNTR}$ is generated. If a spacing operation is selected, this signal is generated whenever the CHARACTER COUNTER reaches 3 or an IRG is detected when the CHARACTER COUNTER is holding 2.

5.14.4 Rewind in progress condition

To maintain an appropriate current status when a Rewind operation is in progress, the control generates the REWIND IN PROG signal by gating the RUN/STOP flip-flop output with the REWIND output of the function decoder (see Drawing 6.25 location C2). As explained in section 5.5, the RUN/STOP flip-flop is set immediately after initiating a Rewind operation and is not cleared until the tape is positioned back on the BOT marker. It may be pointed out here that the RUN/STOP flip-flop is set immediately after initiating a Rewind only to obtain the appropriate status; the RUN/STOP flip-flop cannot actuate the pinch roller until tape has been rewound and the vacuum is re-established.

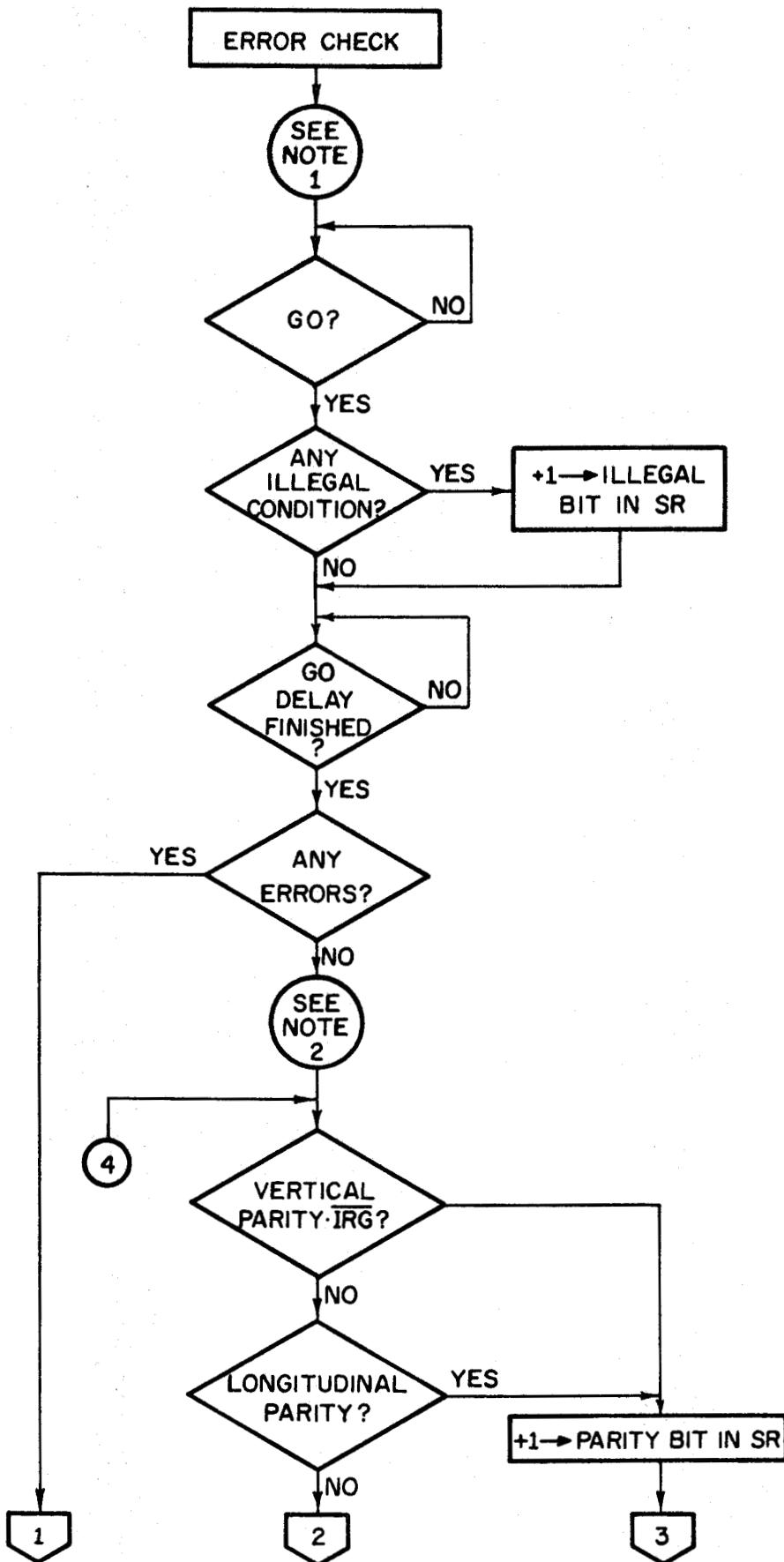
5.14.5 BOT and EOT detection

Whenever the transports encounter the BOT or EOT marker, the local control generates the appropriate signal (UN1 BOT, UN2 BOT, UN1 EOT or UN2 EOT on Drawing 6.25) from the photo-electric sensor outputs. The BOT and EOT signals thus obtained are gated with the UNIT NO bit of the Command Register to find if the selected tape unit is at the BOT or EOT. If the tape is the BOT marker the signal called BOT becomes true (see Drawing 6.25, Location C3). This signal is used by the Rewind Control logic to terminate the Rewind operation in conjunction with the READY signal (see section 5.5).

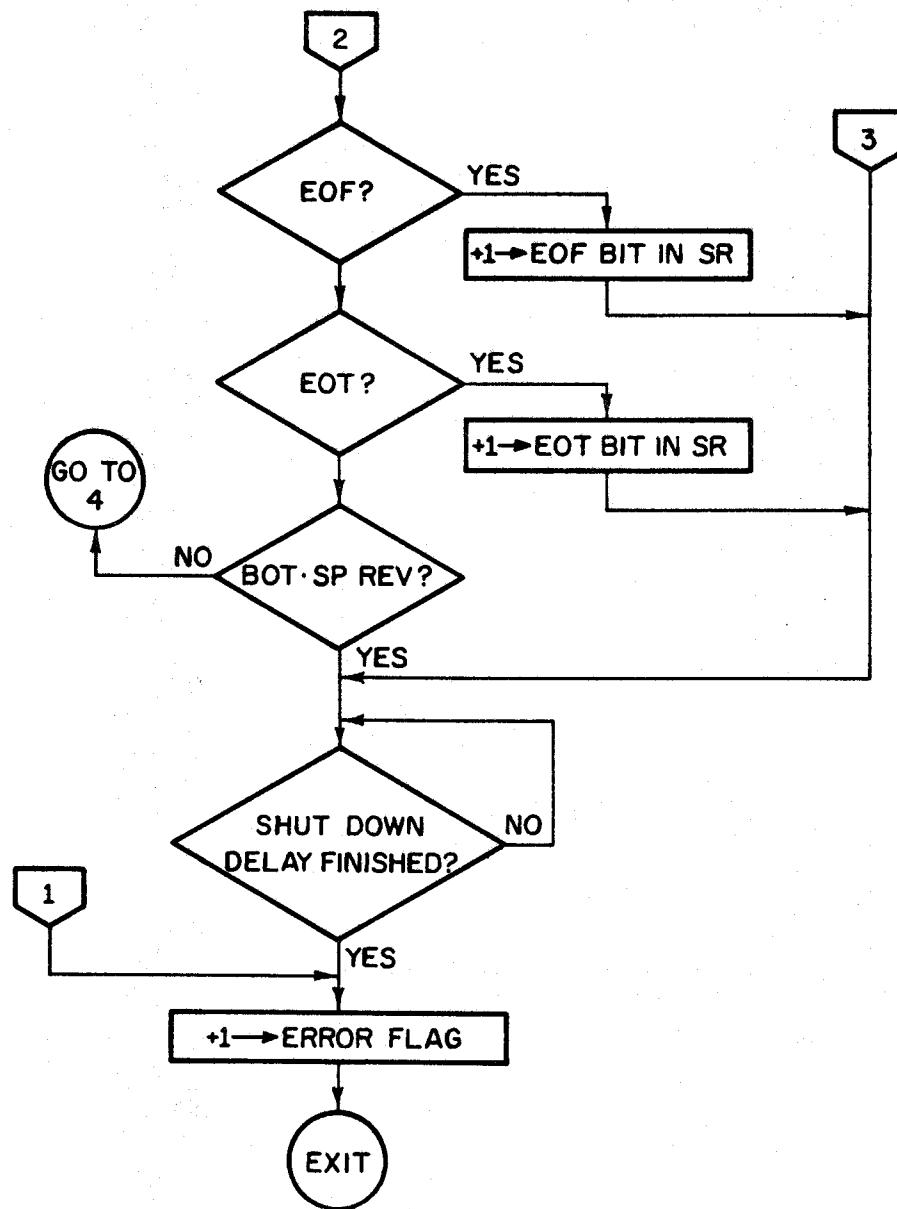
Unlike in the case of the BOT detection, a flip-flop is used to determine the EOT marker status. This is to allow a tape operation to proceed till the end of the current record after sensing the EOT marker (see section 3.7). When the EOT marker is sensed, the control sets the EOT flip-flop in the Status Register (see Drawing 6.25). This makes the ERROR signal true (see Drawing 6.24). When the IRG is encountered, the control interrogates the tape system status to set the ERROR flag if the ERROR signal is true. It is interesting to note the EOT is set only if the FWD/REV flip-flop which controls the direction of tape travel is set for forward direction.

5.14.6 Error and Job Done flags

The error input conditions that initiate a specific type of error signal are shown in Flow Chart 5.7. The possible errors in the tape system can be classified into two categories; pre-initiation and



FLOW CHART 5.7 ERROR STATUS MANAGEMENT (CONT'D)

**NOTES :**

1. PRE-INITIATION ERROR CHECK FLOW START
2. POST-INITIATION ERROR CHECK FLOW START

FLOW CHART 5.7

post-initiation errors depending upon whether they occur before or after initiating a tape operation. The conditions described in section 5.14.4 are the possible pre-initiation errors. The control sets the ILLEGAL bit in the Status Register if the pre-initiation error condition exists using the IOT 722 (GO) pulse. This makes the ERROR signal true (see Drawing 6.24) and the control sets the ERROR bit in the Status Register instead of the RUN/STOP flip-flop at the end of the GO DELAY period, thus preventing the tape to start with a pre-initiation error condition. If any post-initiation error occurs (e.g. parity error), the appropriate bit in the Status Register is set immediately to maintain the current status of the tape system. However, the ERROR flag is not set until the SHUTDOWN DELAY is complete so that the current operation is not affected until the end of the record has been reached. At this time, if there are no errors, the Job Done flag is set to signify successful conclusion of the current operation. If the ENABLE bit in the Command Register is set either of these two flags can cause a program interrupt (see Drawing 6.28). In addition to gating the flag outputs on to the program interrupt bus, the flag outputs are also gated on to the skip bus of the PDP-8 to increment the Program counter by one, so that the next sequential instruction in the program is skipped on the MTSF instruction.

It should be recalled now that during Continuous Mode of tape operations, the Job Done flag is set after operating successfully on a record and the program issues a MTGO instruction to proceed (see chapter 4) with the next record. The IOT 722 (GO) pulse clears the Job Done flag so that the flag is initialized properly during Continuous Mode operations.

5.15 Writing EOF:

As mentioned on earlier occasions the EOF is a special single character record to separate data files from one another on the tape. The control has to perform the following operations to write the EOF code on the tape.

- (a) Generate the required length of blank tape (EOF gap) that precedes the EOF code. This is generally 3.5 inches, though not mandatory for IBM compatibility.
- (b) Write the appropriate EOF code on the tape.
- (c) Write the appropriate LRC character 8 spaces from the EOF code. It is worthwhile reminding here that there is no CRC character for the EOF.

When the Command Word specifies a Write EOF operation, the control energizes the WRITE ENABLE line (see section 5.12) to excite the erase head of the selected tape unit. If there are no pre-initiation error conditions the GO DELAY triggers the EOF DELAY 1 (see Drawing 6.29).

At the end of this delay the EOF code is loaded into RWB 1 by the LOAD EOF signal and the EOF DELAY 2 is triggered. At the end of this delay the EOF → TAPE pulse is generated. This pulse triggers the WRT CLK PULSER (see Drawing 6.11) which writes the EOF code on the tape. The WRITE TIME pulse, apart from triggering the WRT CLK PULSER, also triggers the appropriate LRC DELAY depending on the selected density of operation (see Drawing 6.24) so that the LRC is written after 8 character spaces from the EOF code. The sum of the EOF DELAY 1 and EOF DELAY 2 is equal to the delay necessary to create 3.5 inches of blank tape for the EOF gap.

5.16 Conclusion:

The tape control unit whose operations have been described in the preceding sections was built and is in use with the Automatic Cartographic System for nearly a year in its proto-type form.

The basic subroutines to operate the tape system were developed and these were also used to test the tape system by writing known data patterns on the tape and reading back for checking by the PDP-8. These tapes were also run on the System 360 to produce a line printer dump of the data to check the tape compatibility. Tapes written with known data patterns by the System 360 were read on the PDP-8 to establish the interchangeability of the data tape between the two installations, thus fulfilling the aims of the project.

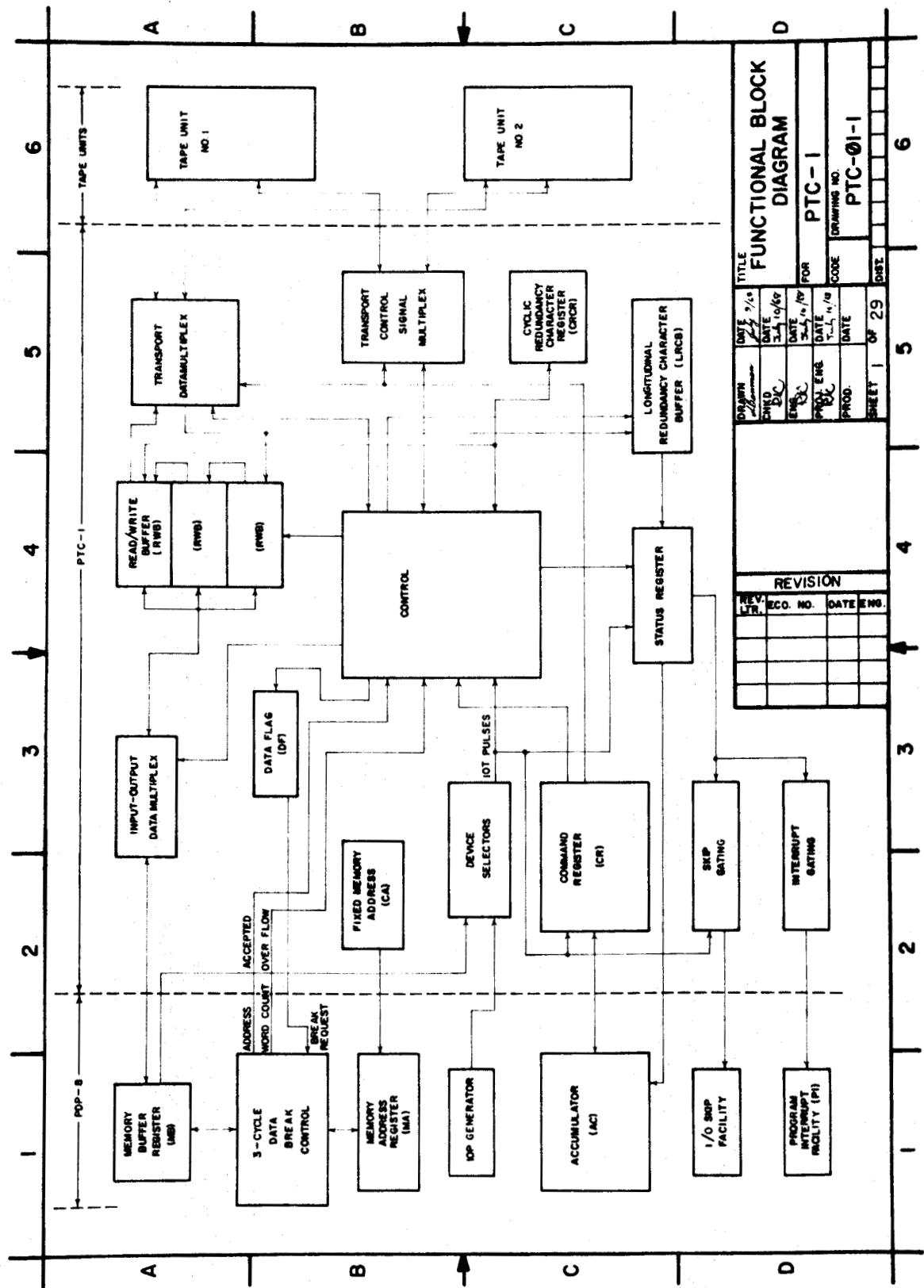
When updating the prototype tape control unit to the finished form, the following modifications may result in a more elegant design:

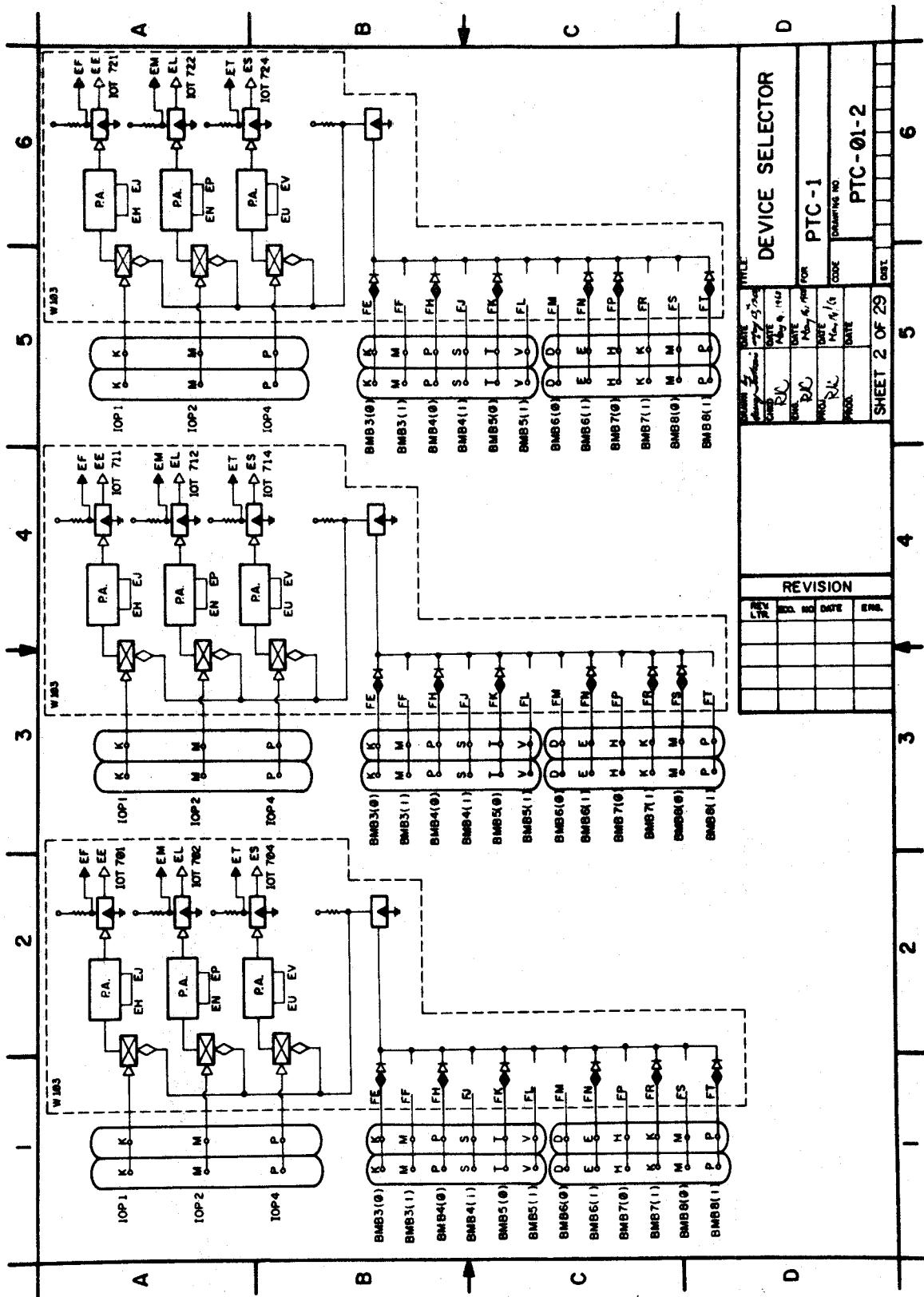
- (a) CRC and LRC gap generation: As can be seen from Drawings 6.17 and 6.24, delay modules were used to generate the required 4 character spaces before the CRC and LRC characters. Instead of using different delays depending on the selected density, a more elegant approach would have been to generate these gaps by using a binary counter to count the MASTER CLOCK pulses. Although the control will be more complex, one could intuitively sense that the CLK CNTR might be used to serve this purpose.
- (b) Elimination of Redundancy: Although every effort was made to eliminate redundancy in the first design, one cannot be sure of complete minimal implementation in a system of this complexity. It

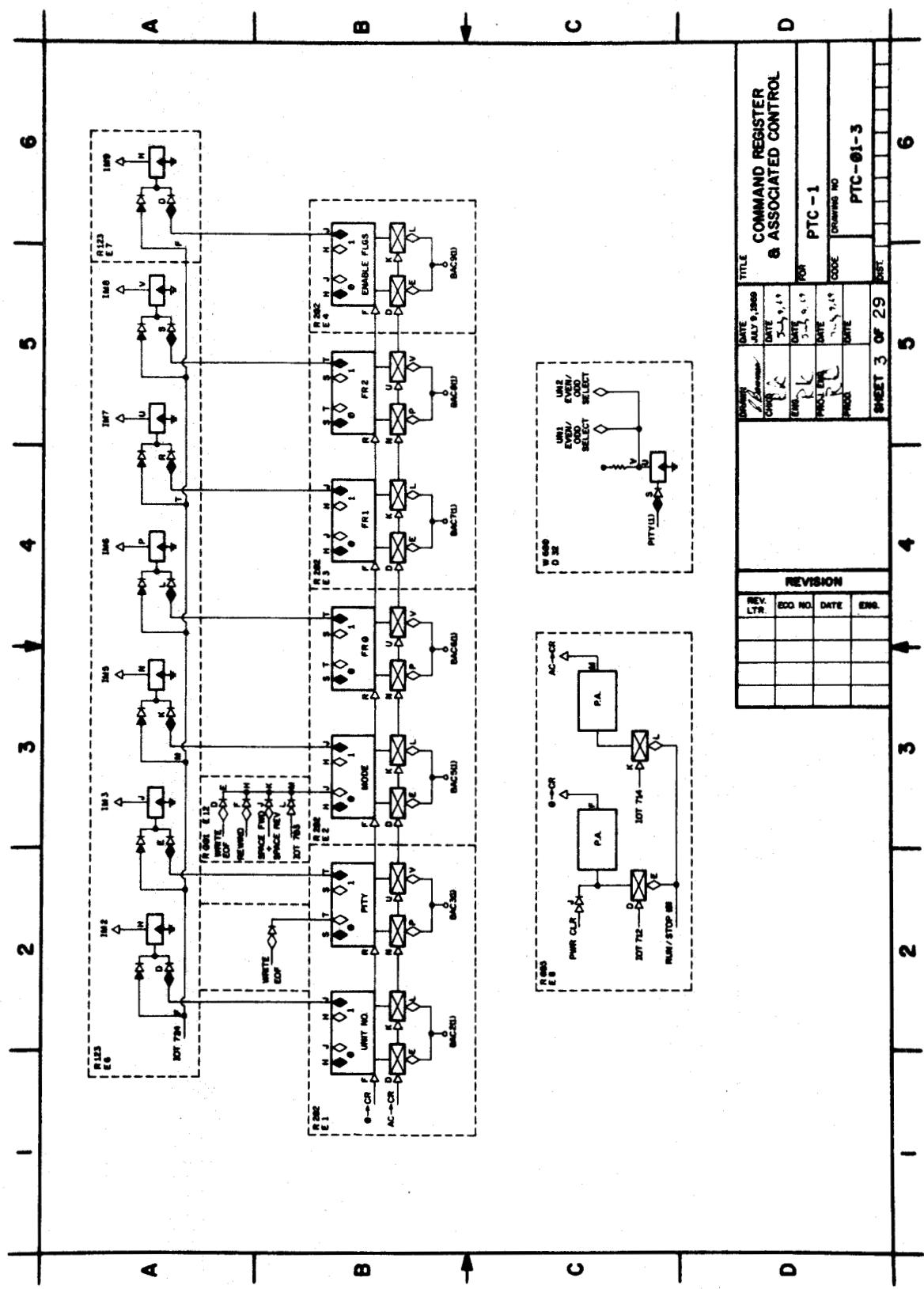
is safe to assume that this redundancy will be mostly in the form of signal duplication (i.e the same signal is generated in more than one place), which can usually be best eliminated by a careful review and listing of each signal in the control by a person other than the designer.

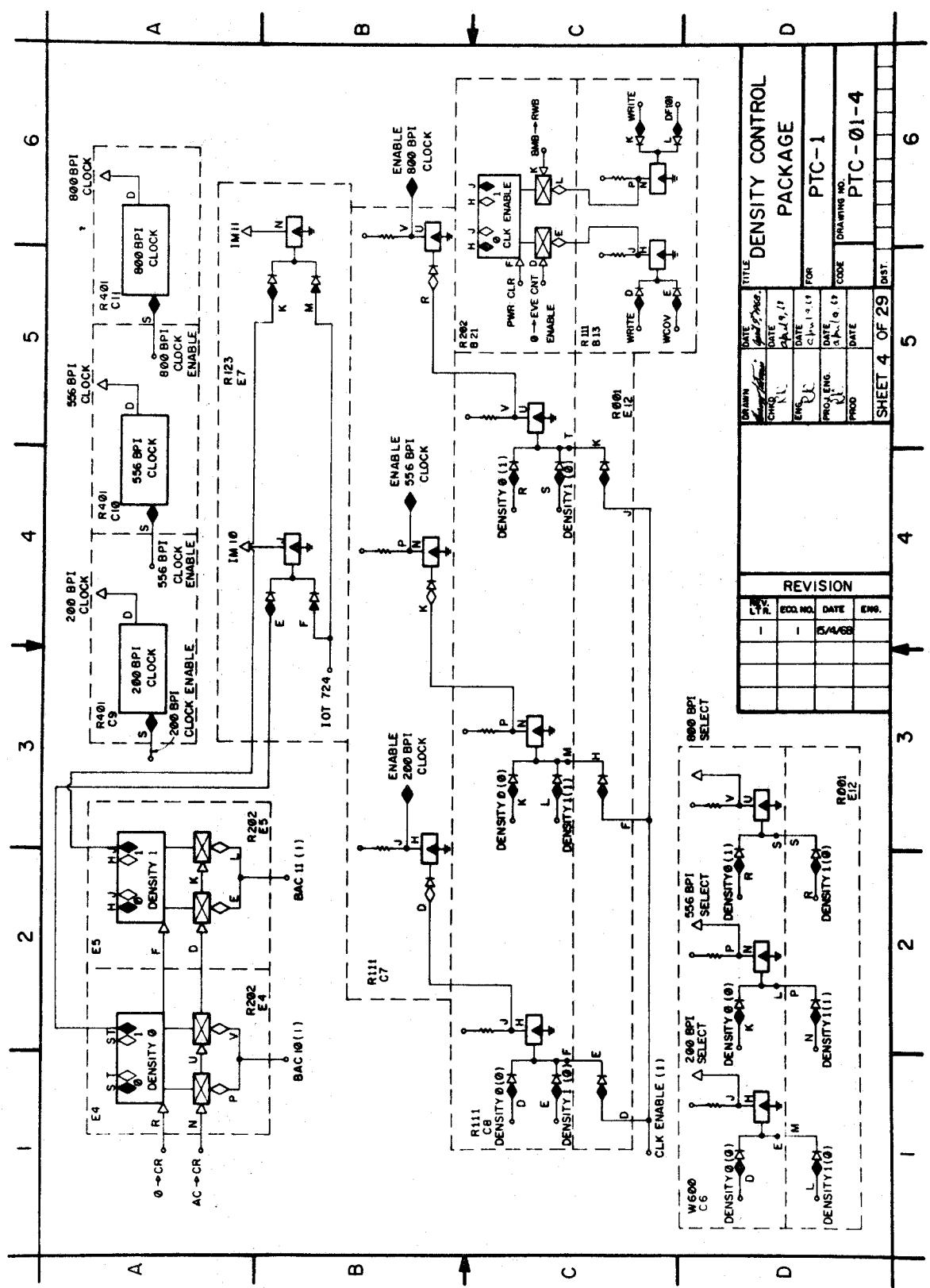
The EVE CNTR is the only subsystem in the control where redundancy is deliberately left in because of its conceptual simplicity in understanding the operations. A slight thought is enough to reveal that the CLK CNTR and CHAR CNTR outputs could have been used to generate the write event signals.

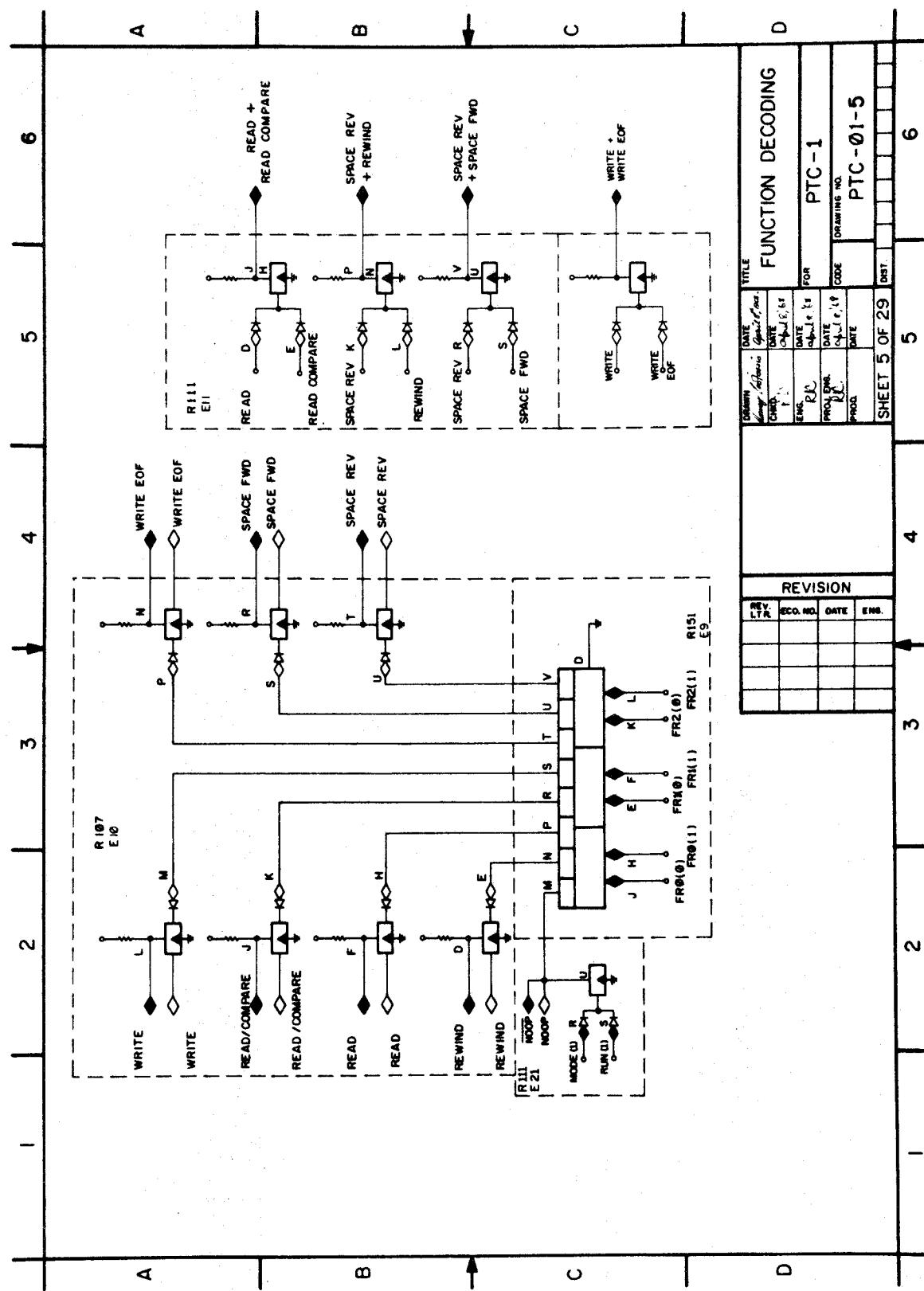
ENGINEERING DRAWINGS

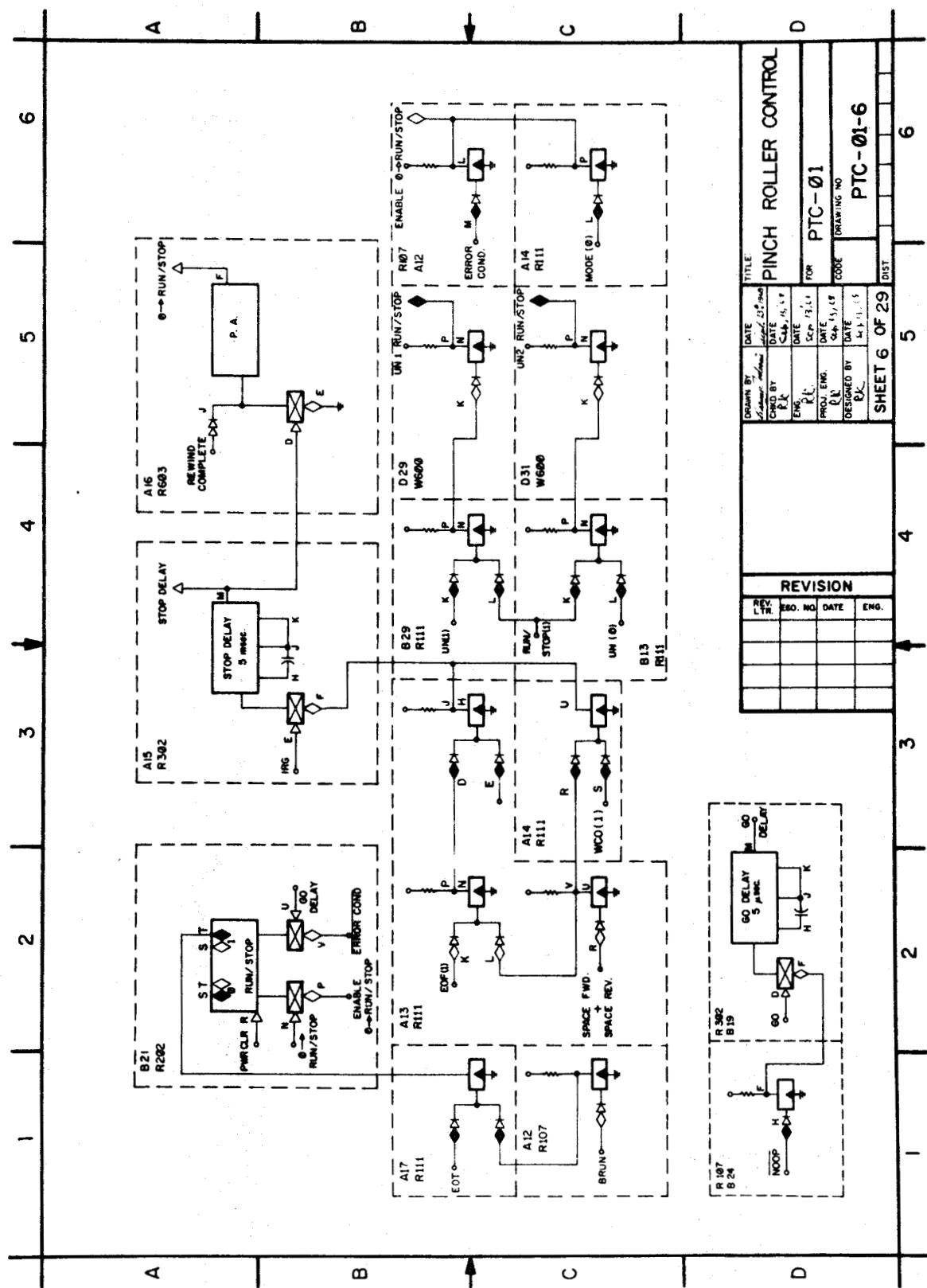


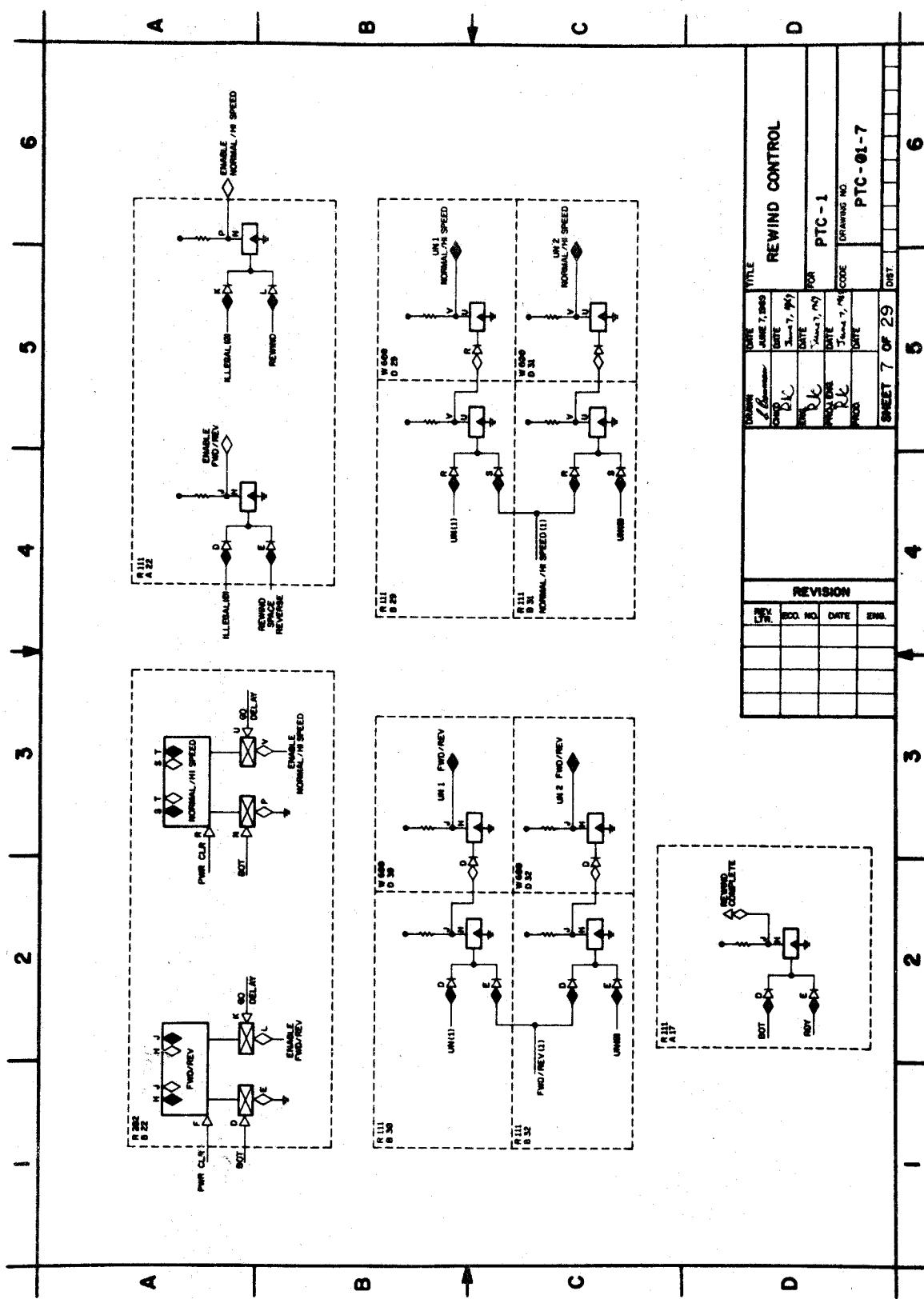


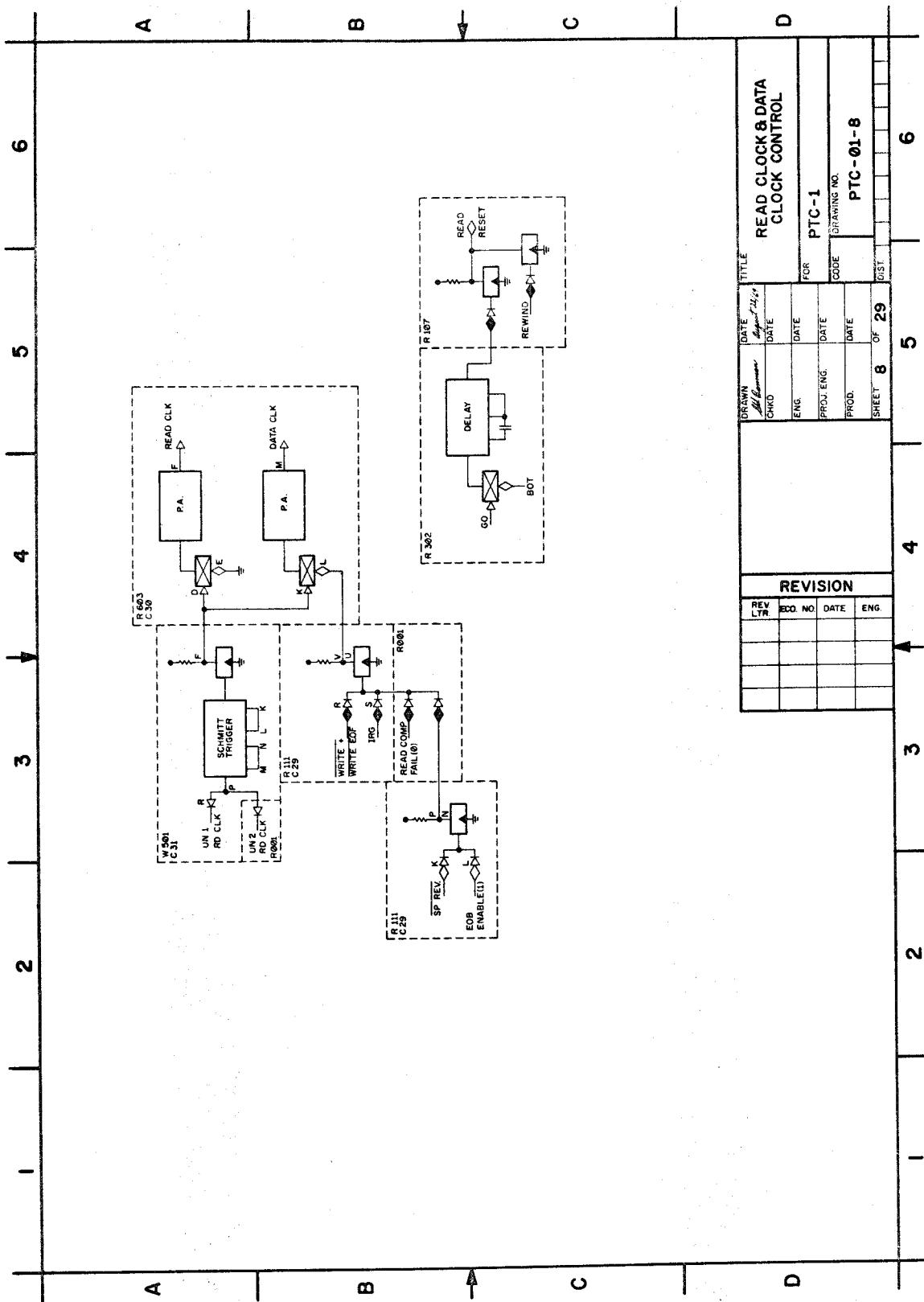


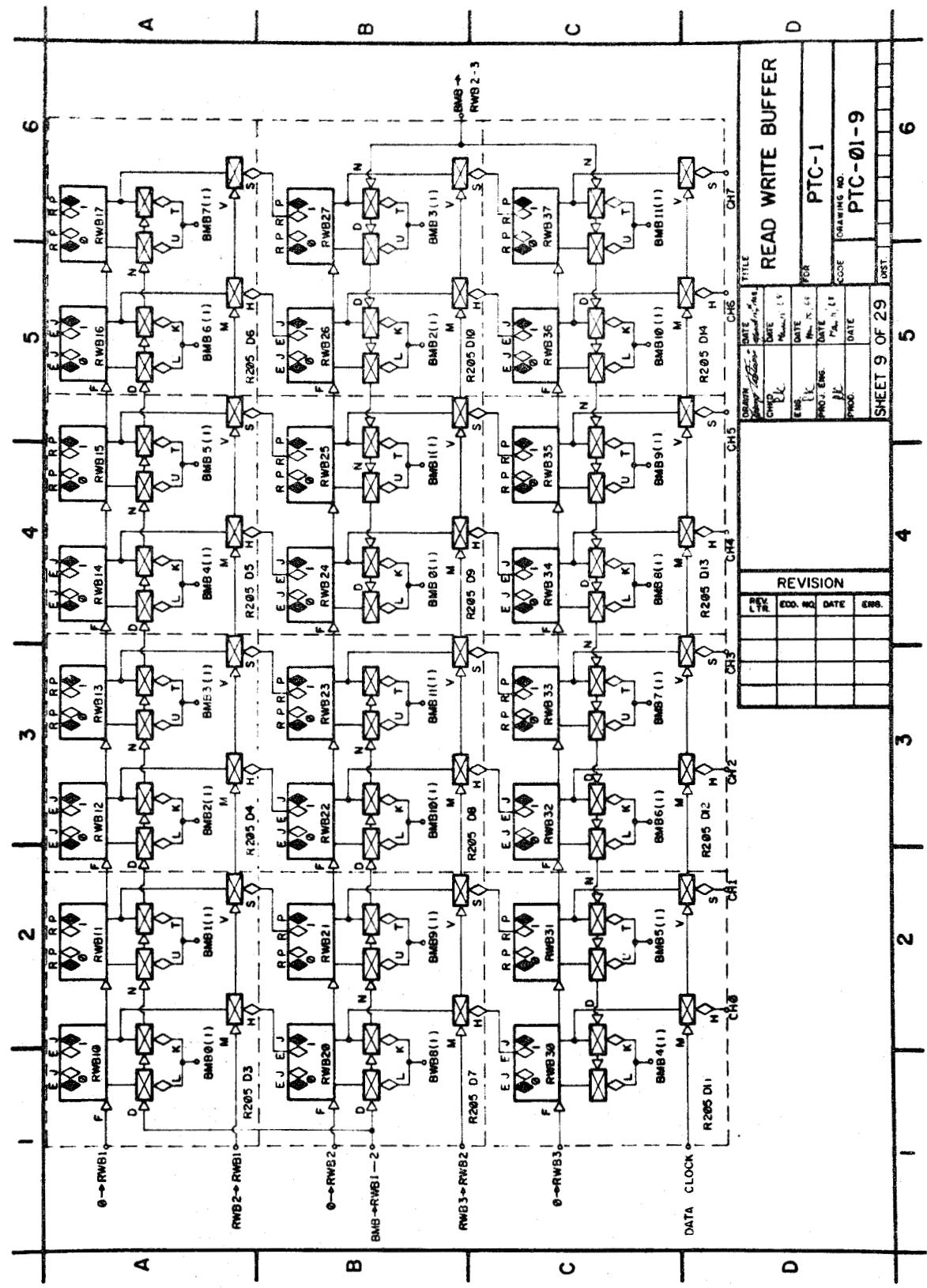


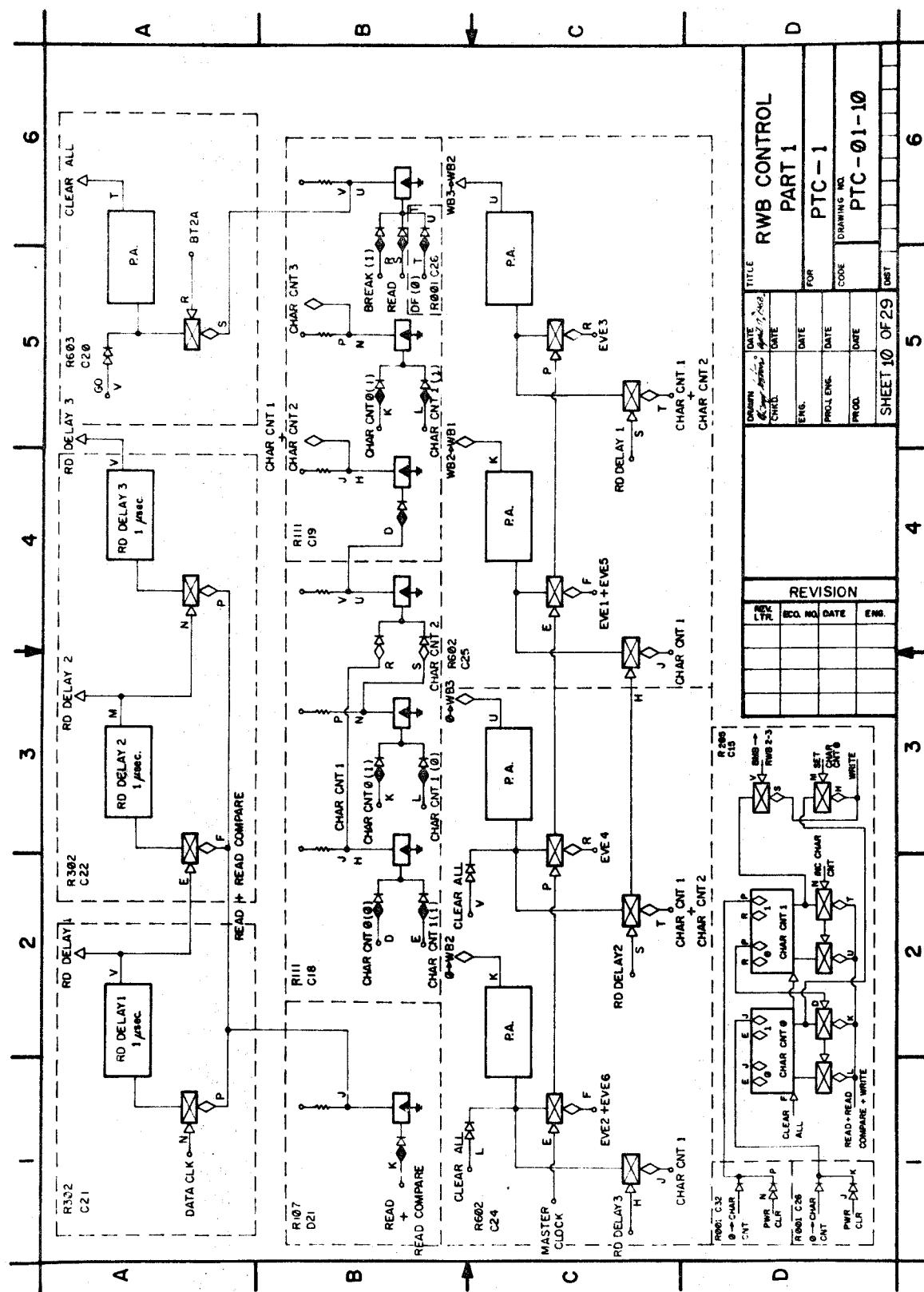


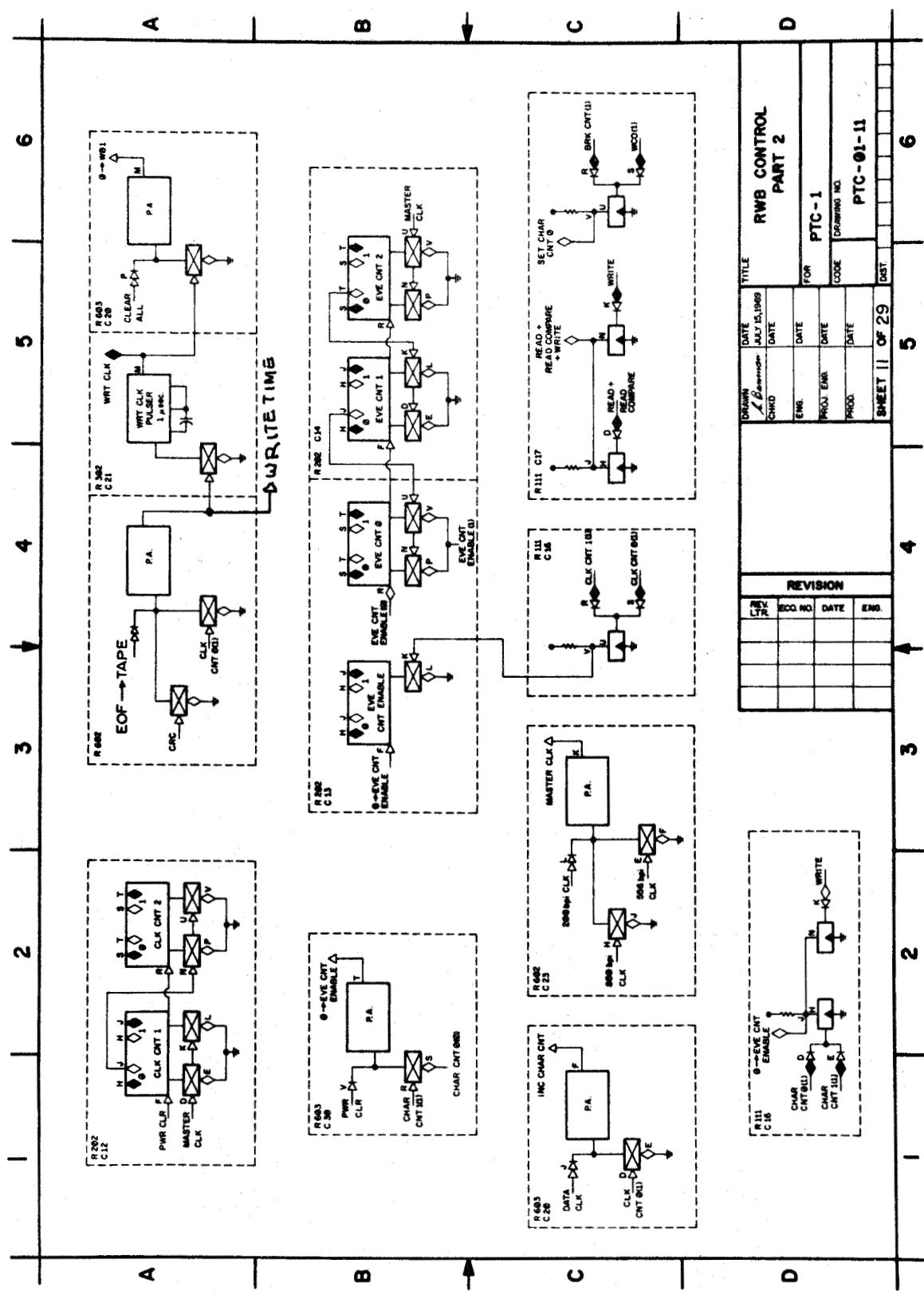


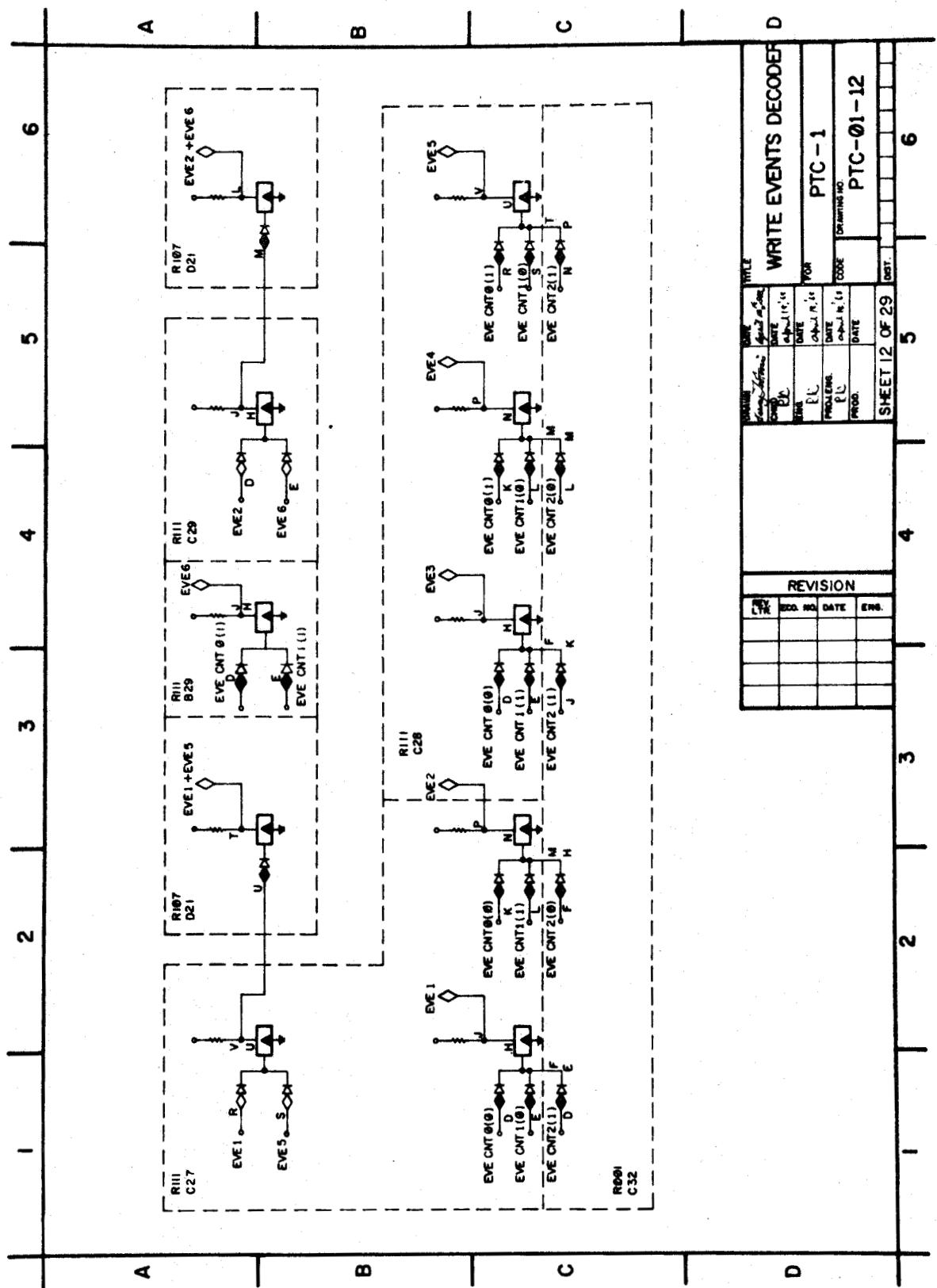


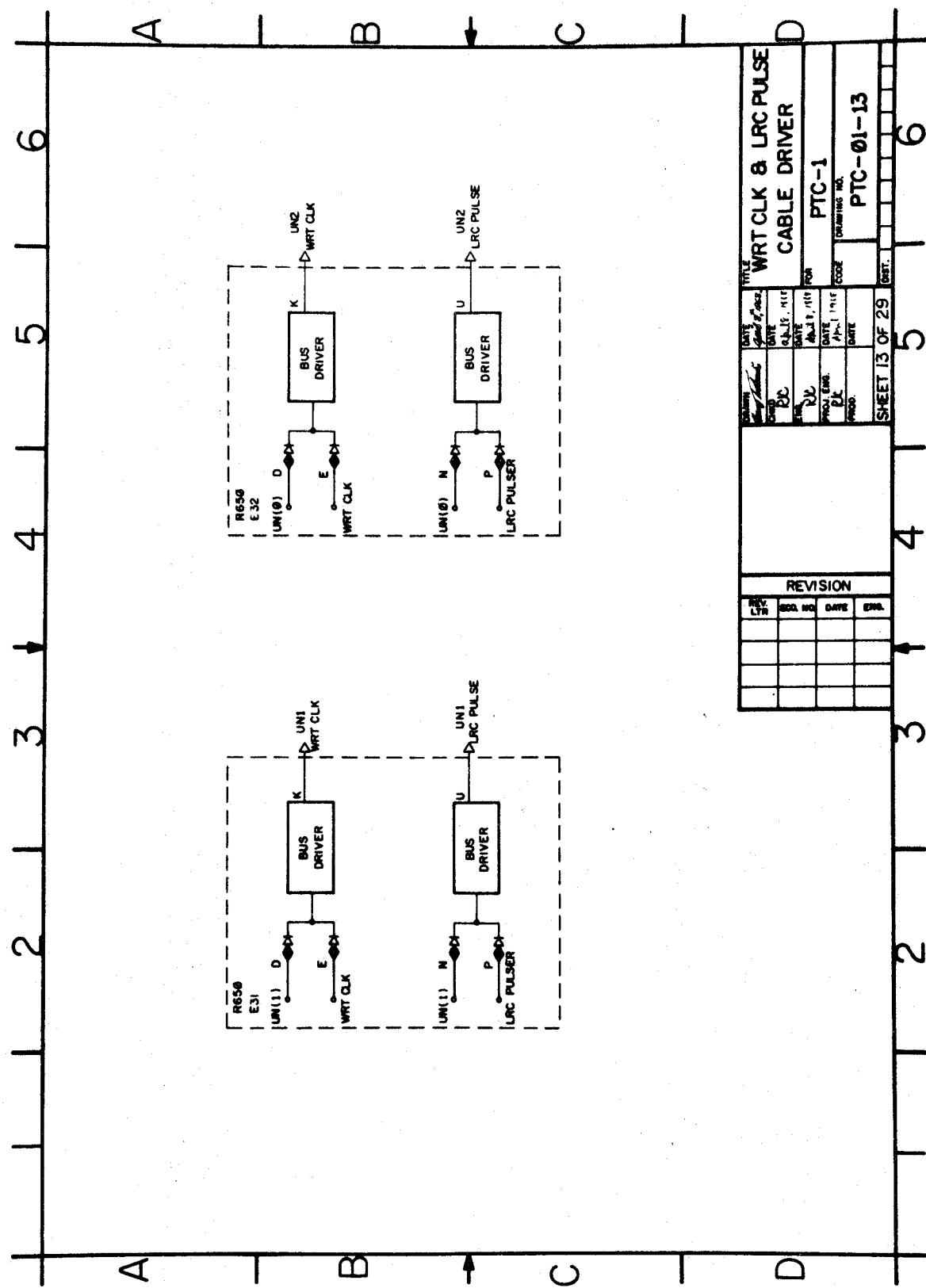


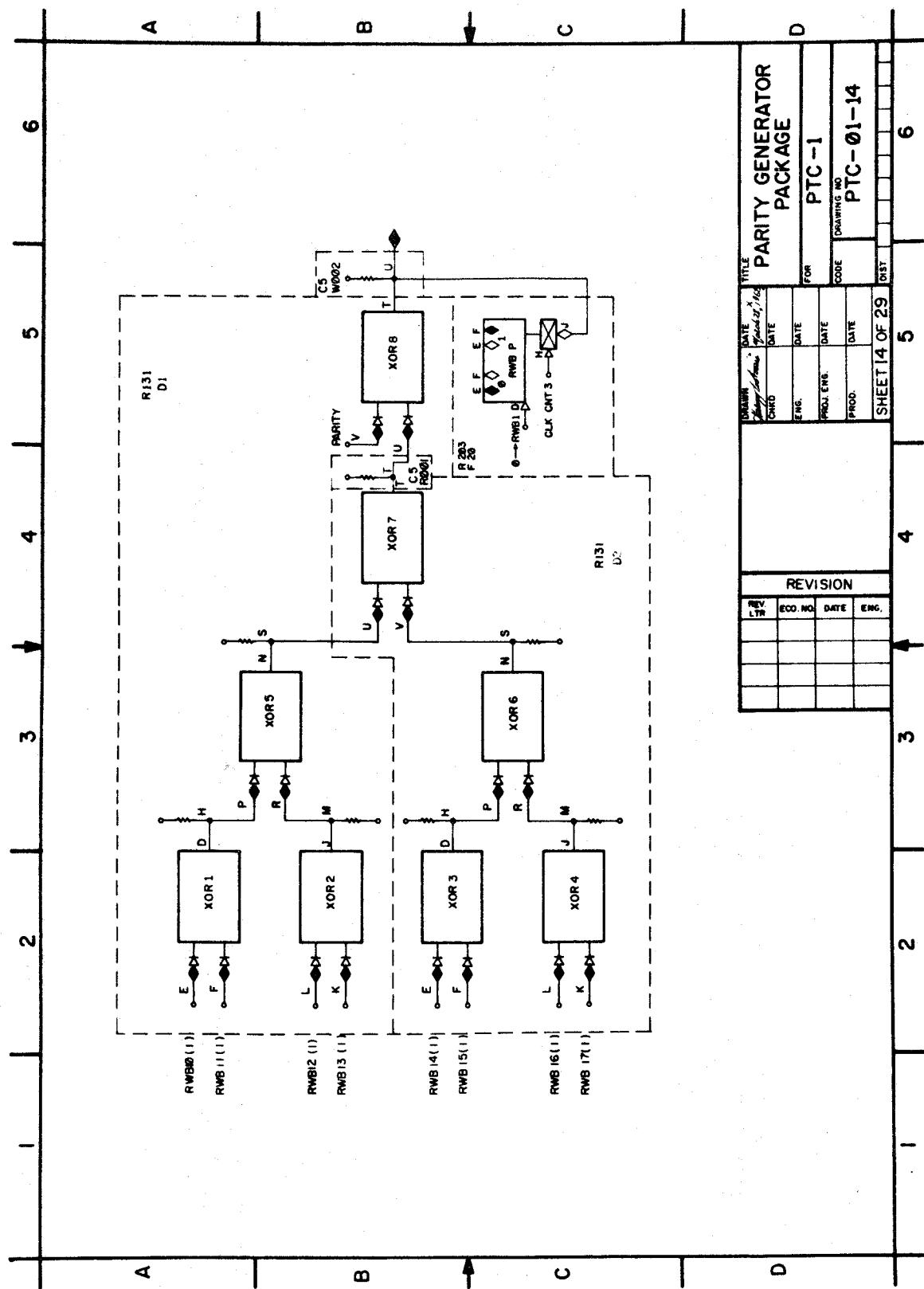


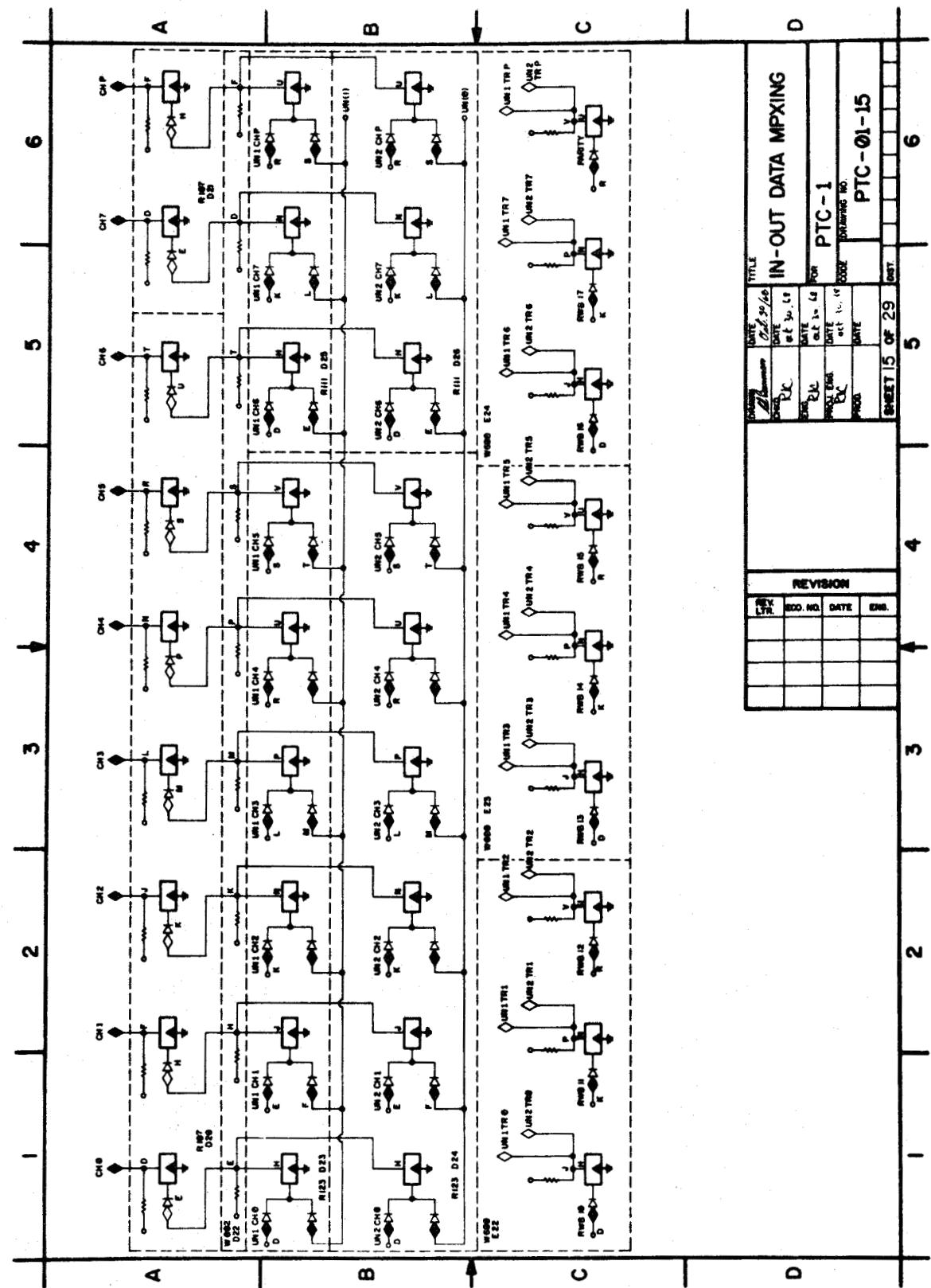












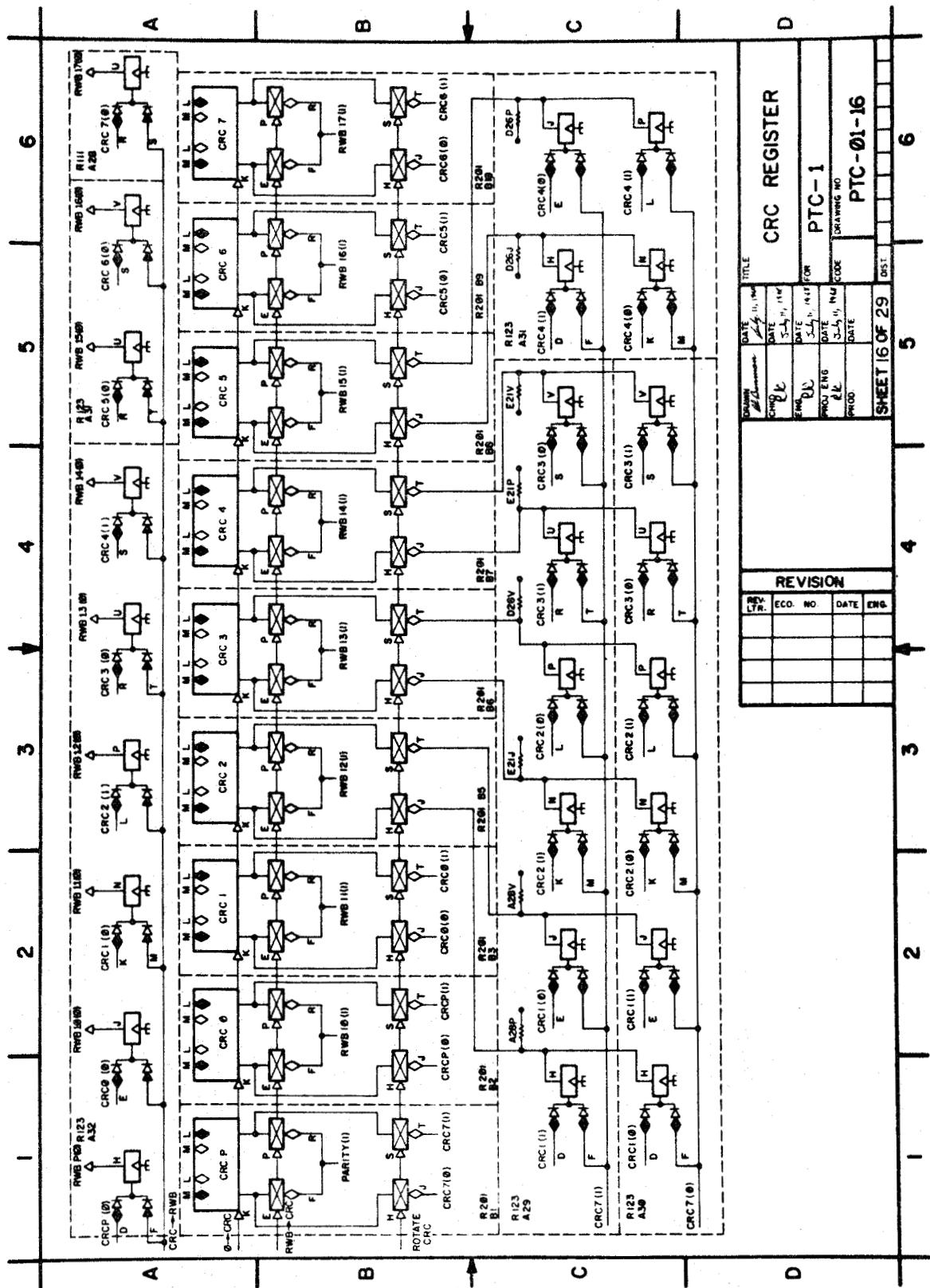
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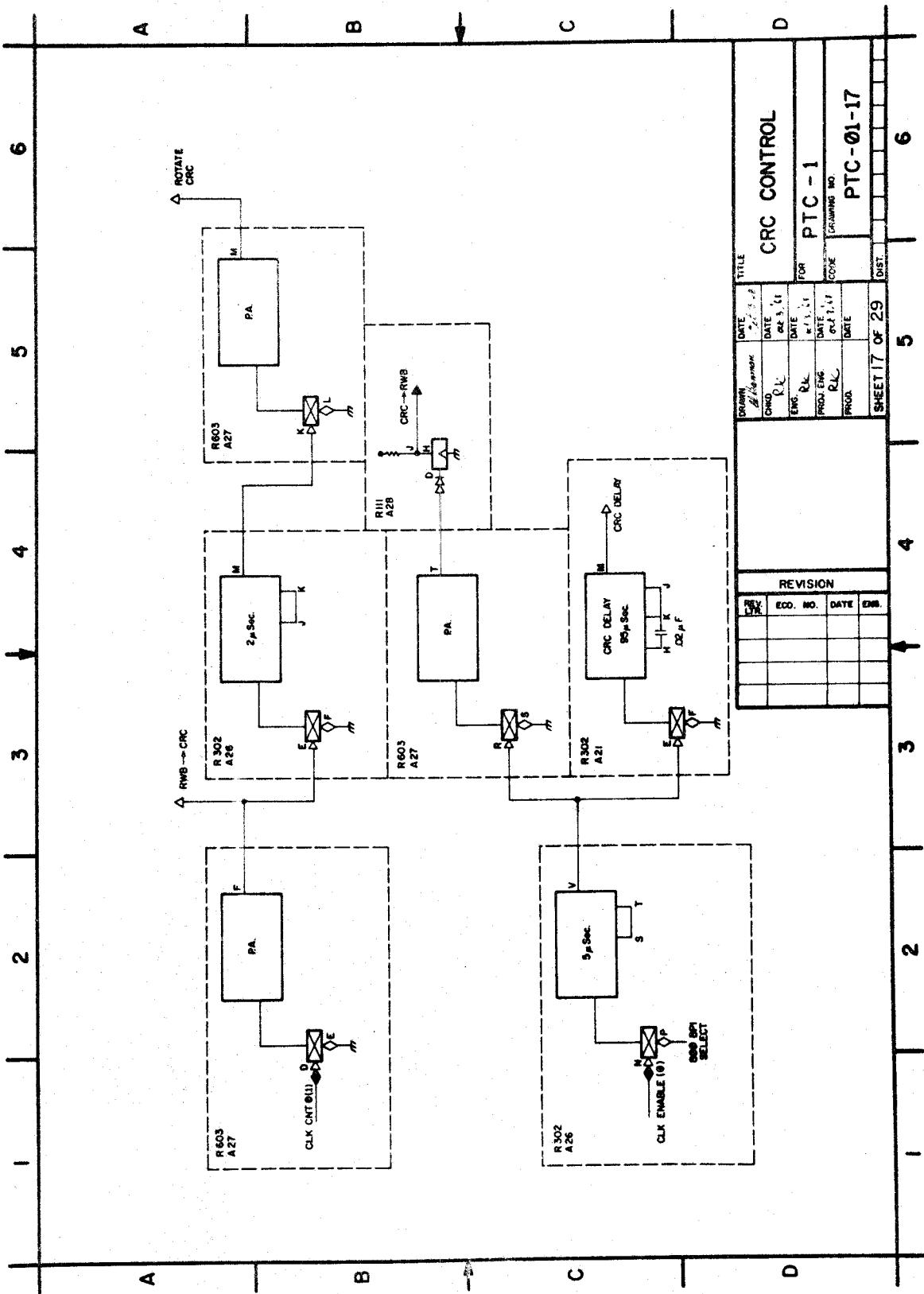
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REVISION			
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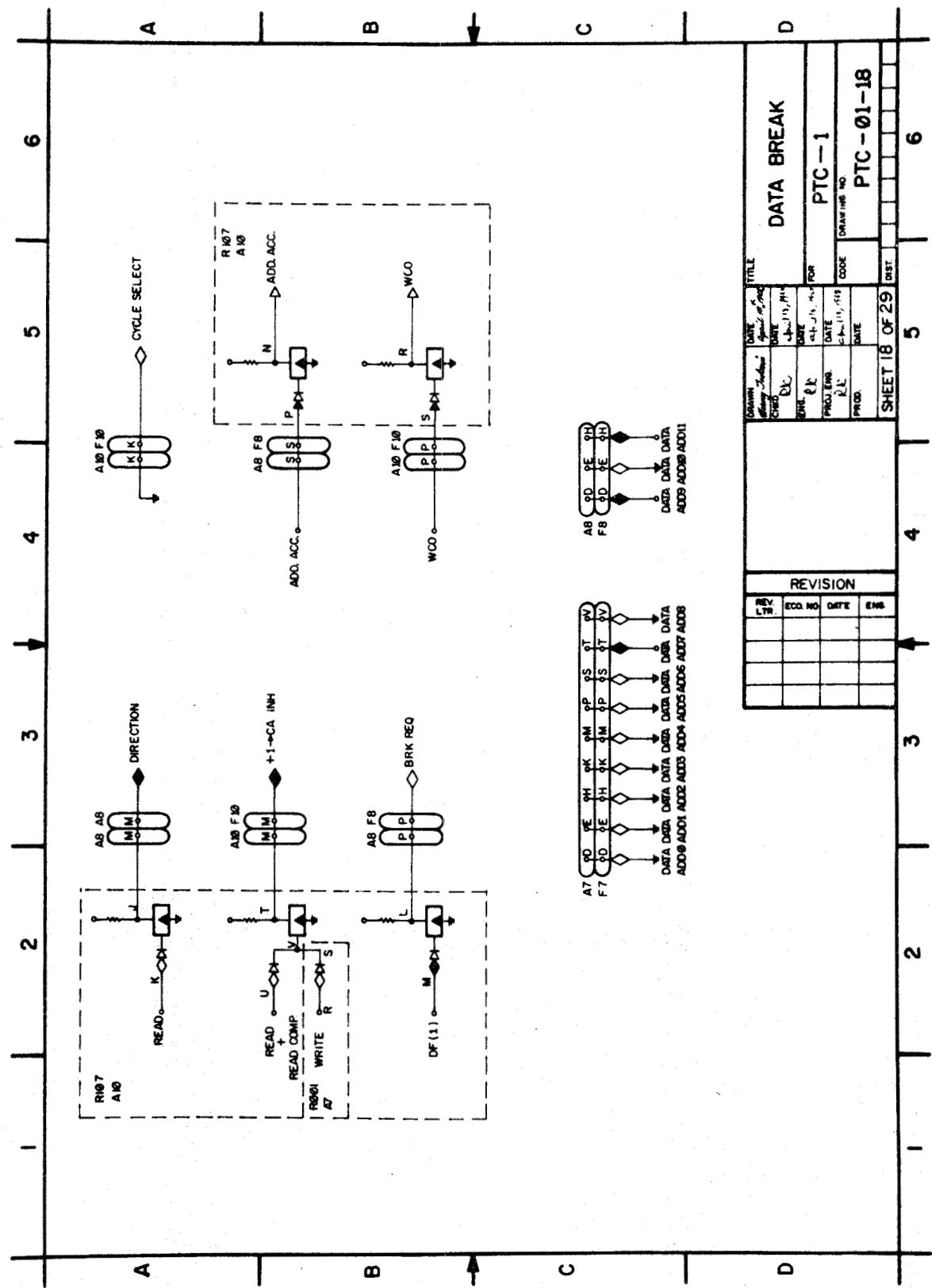
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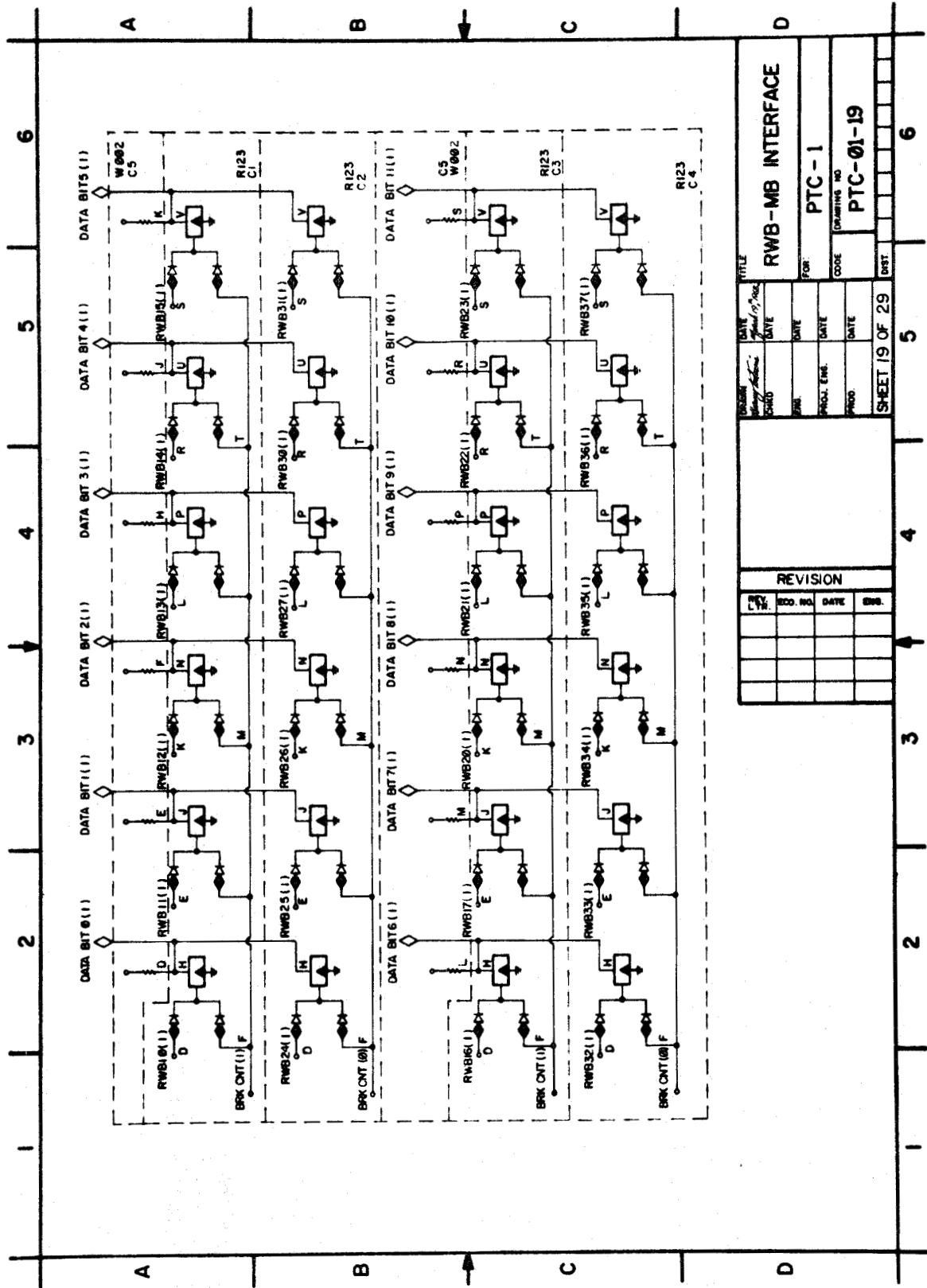
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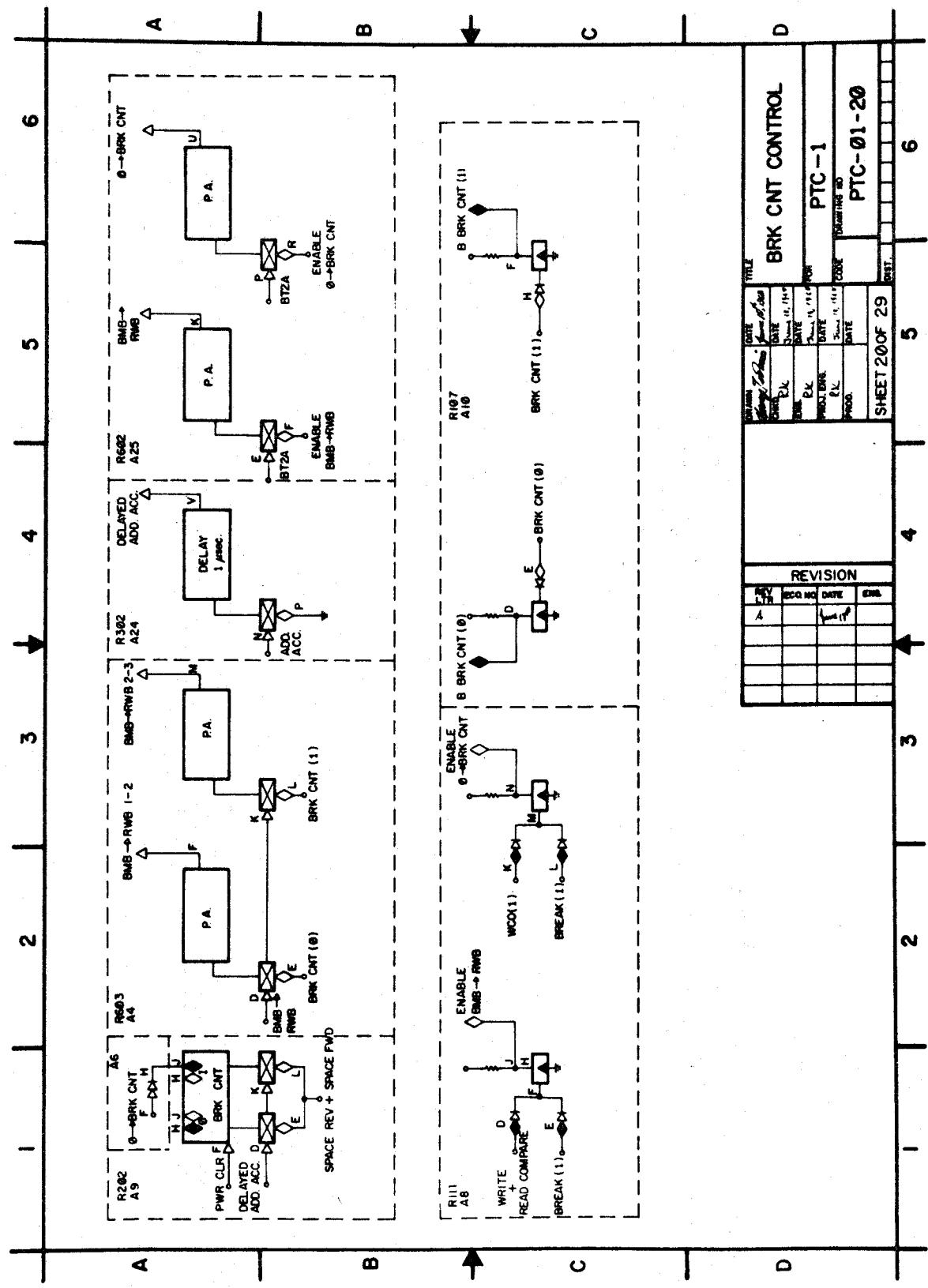
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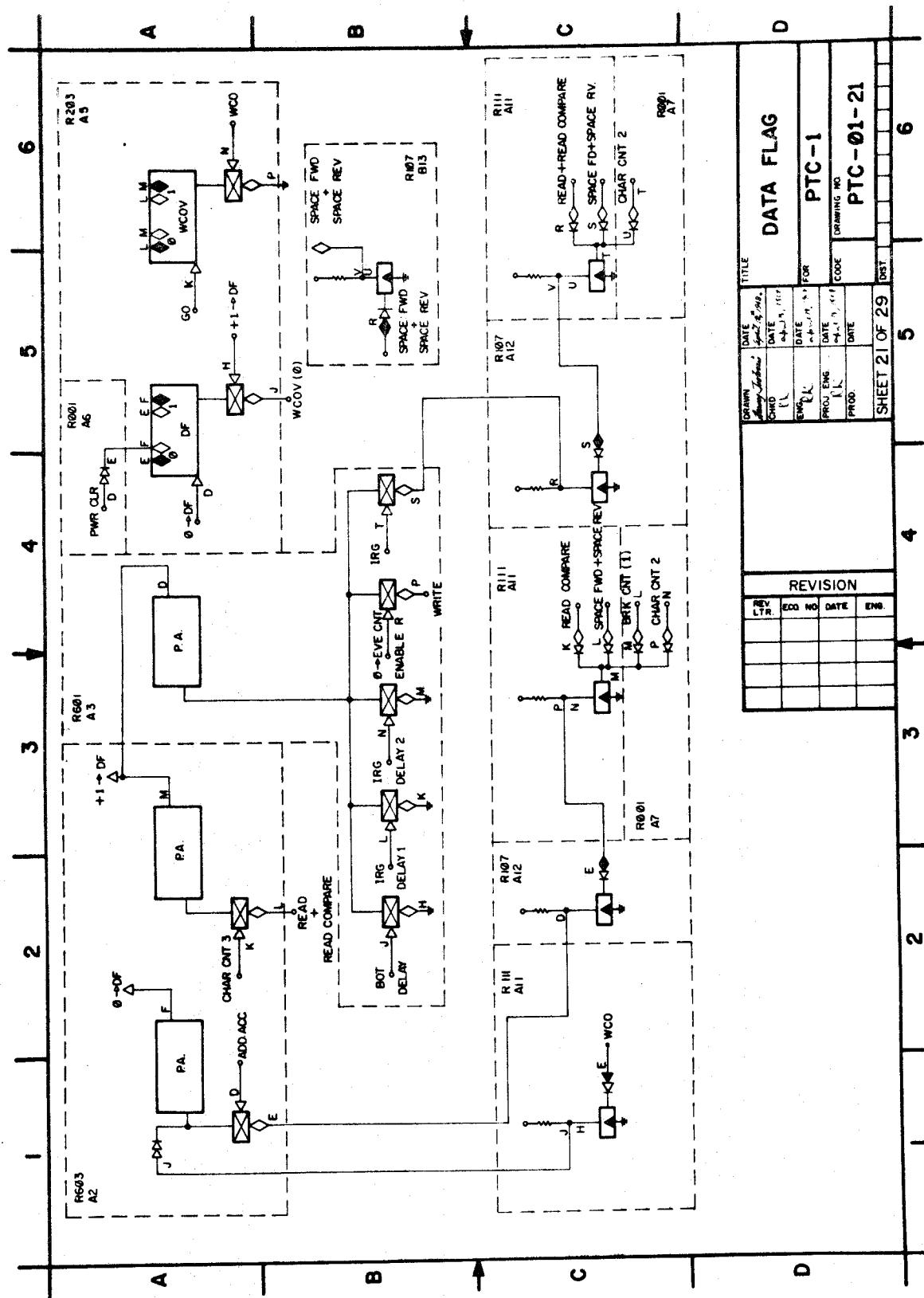


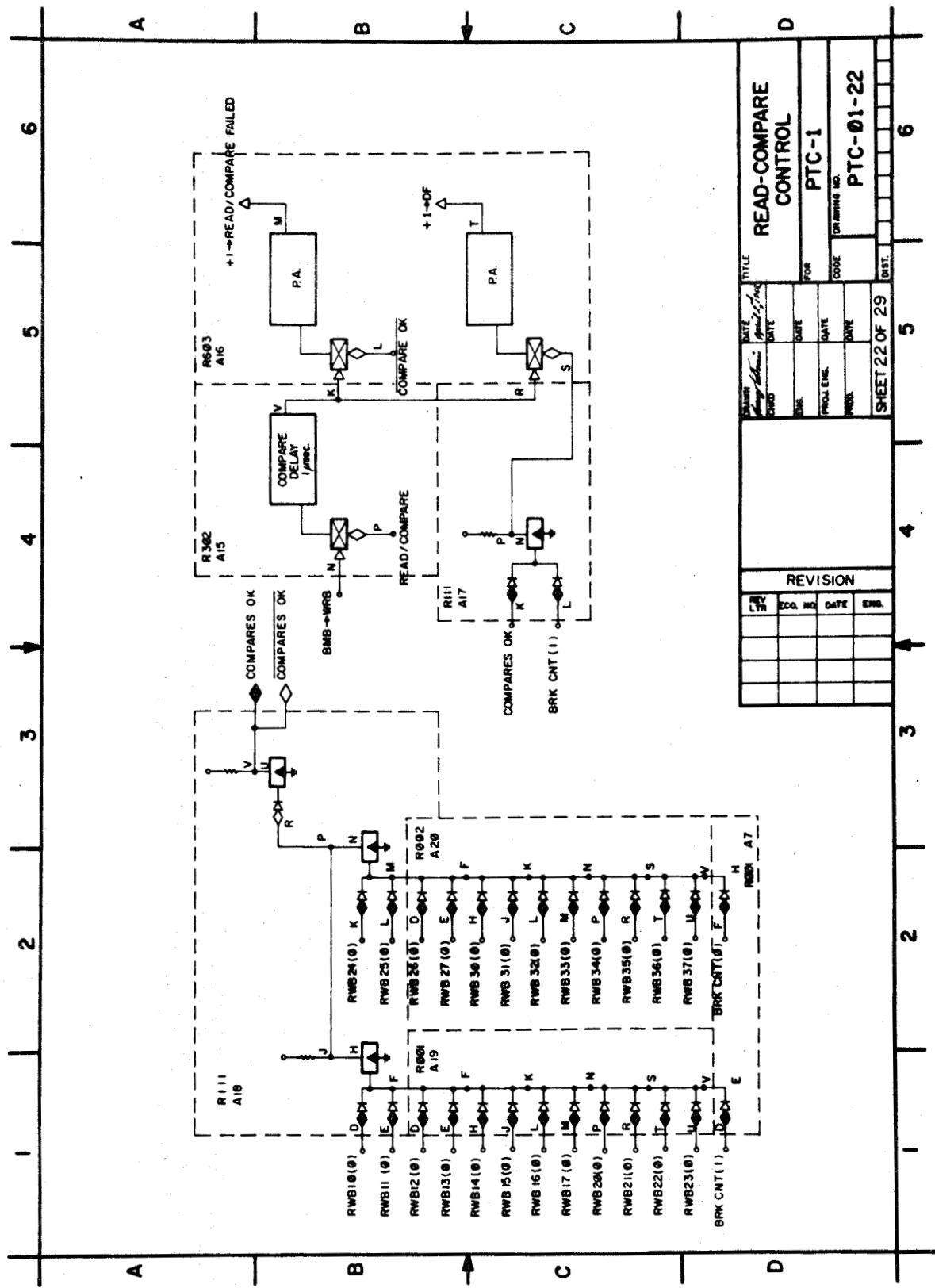


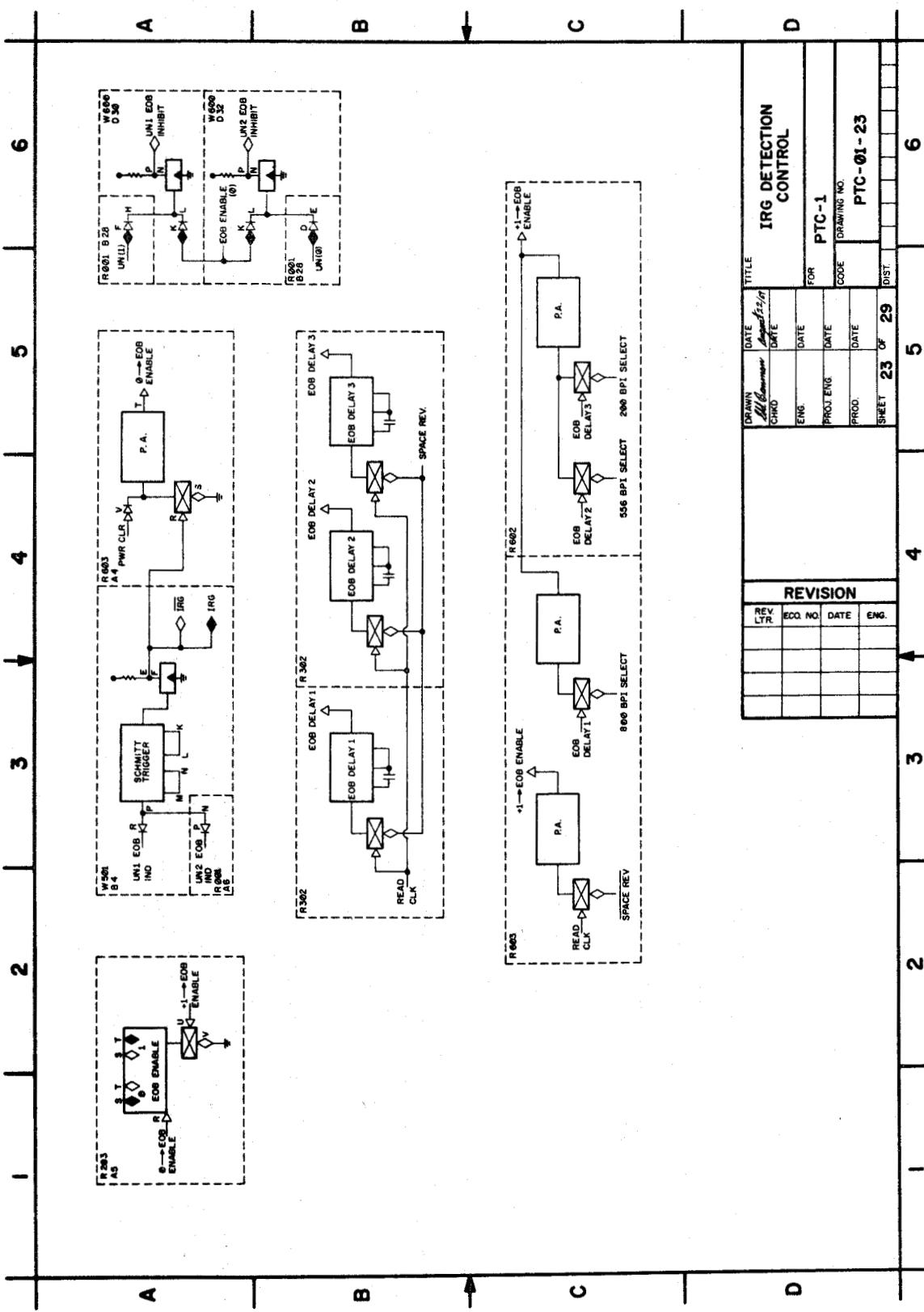


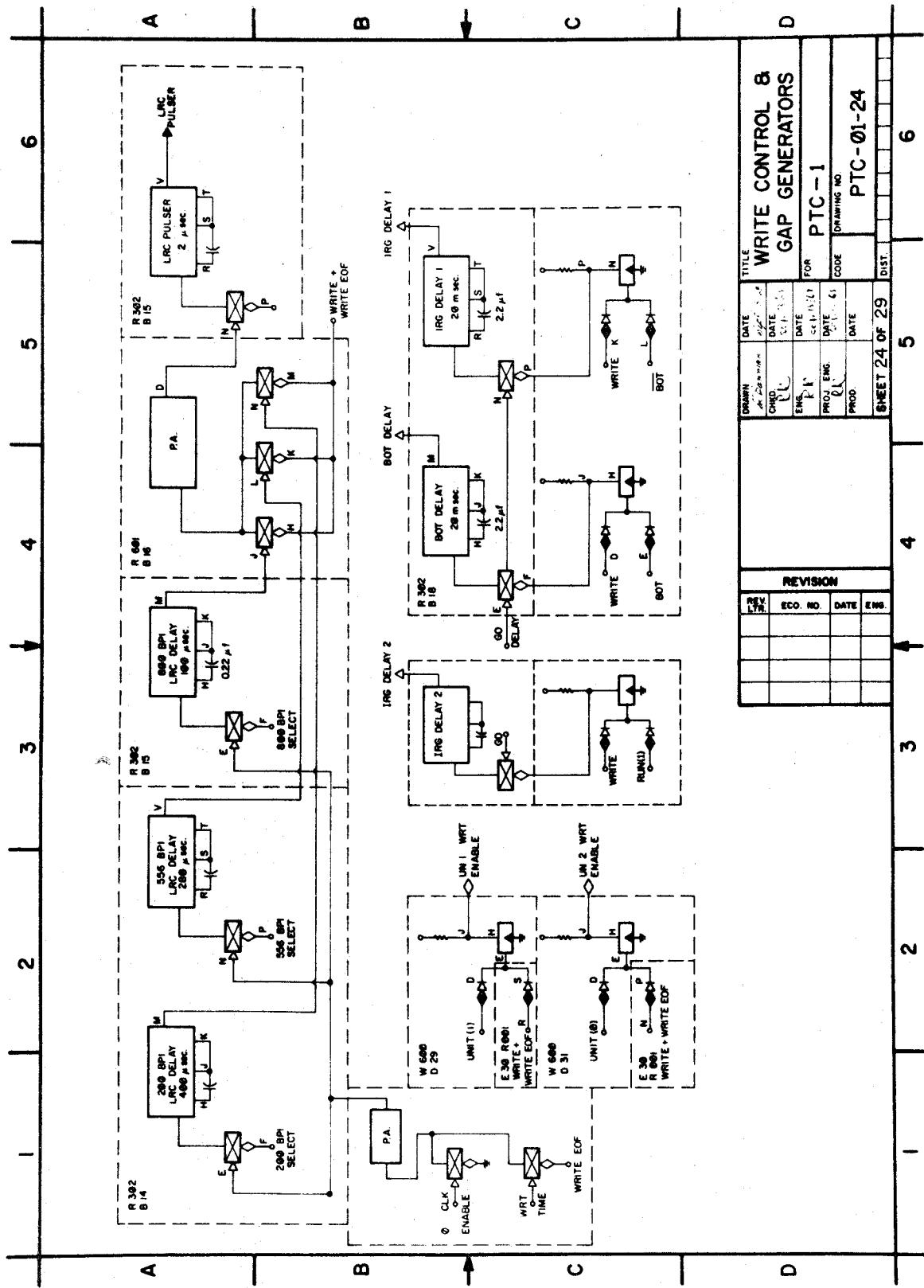


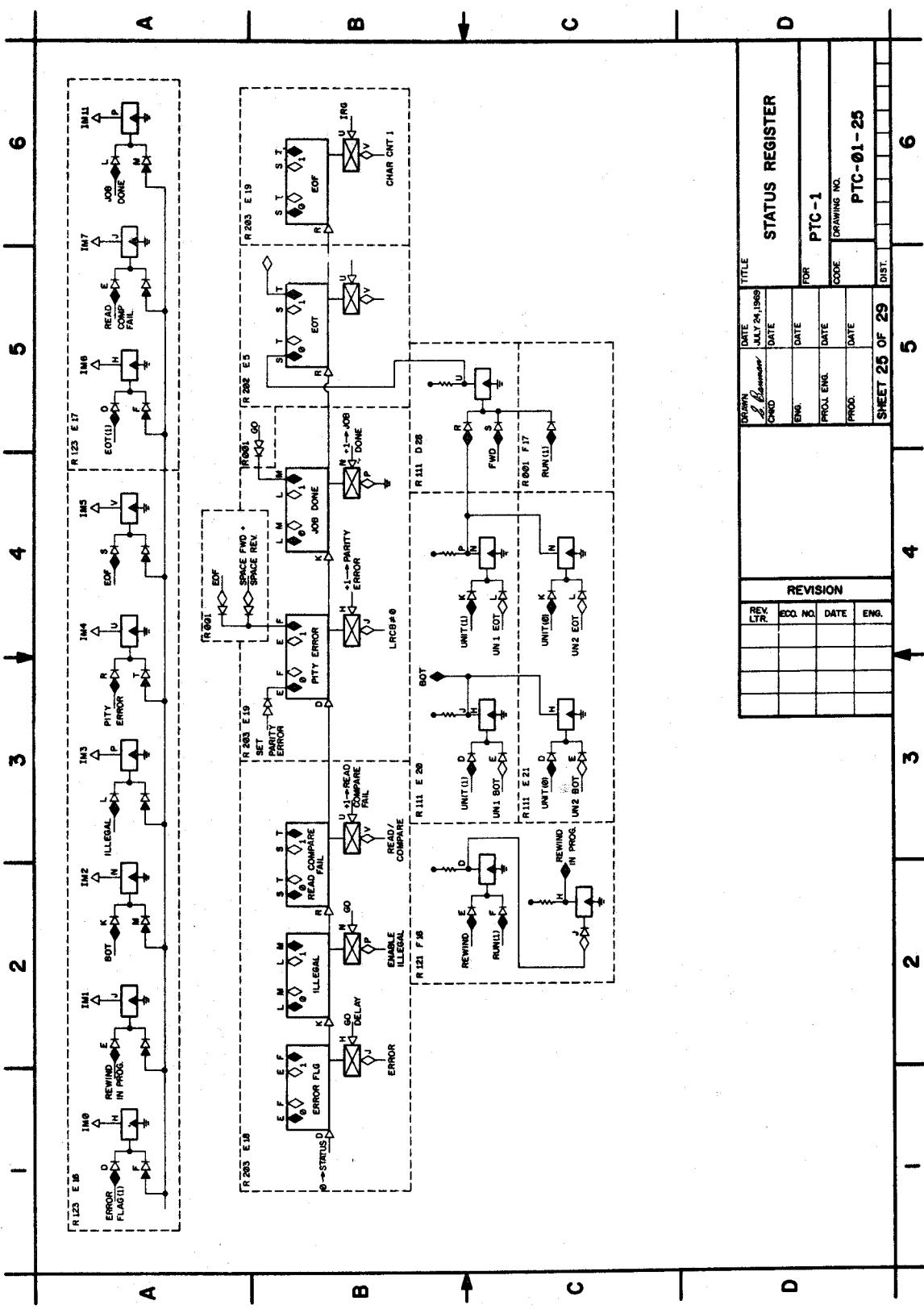


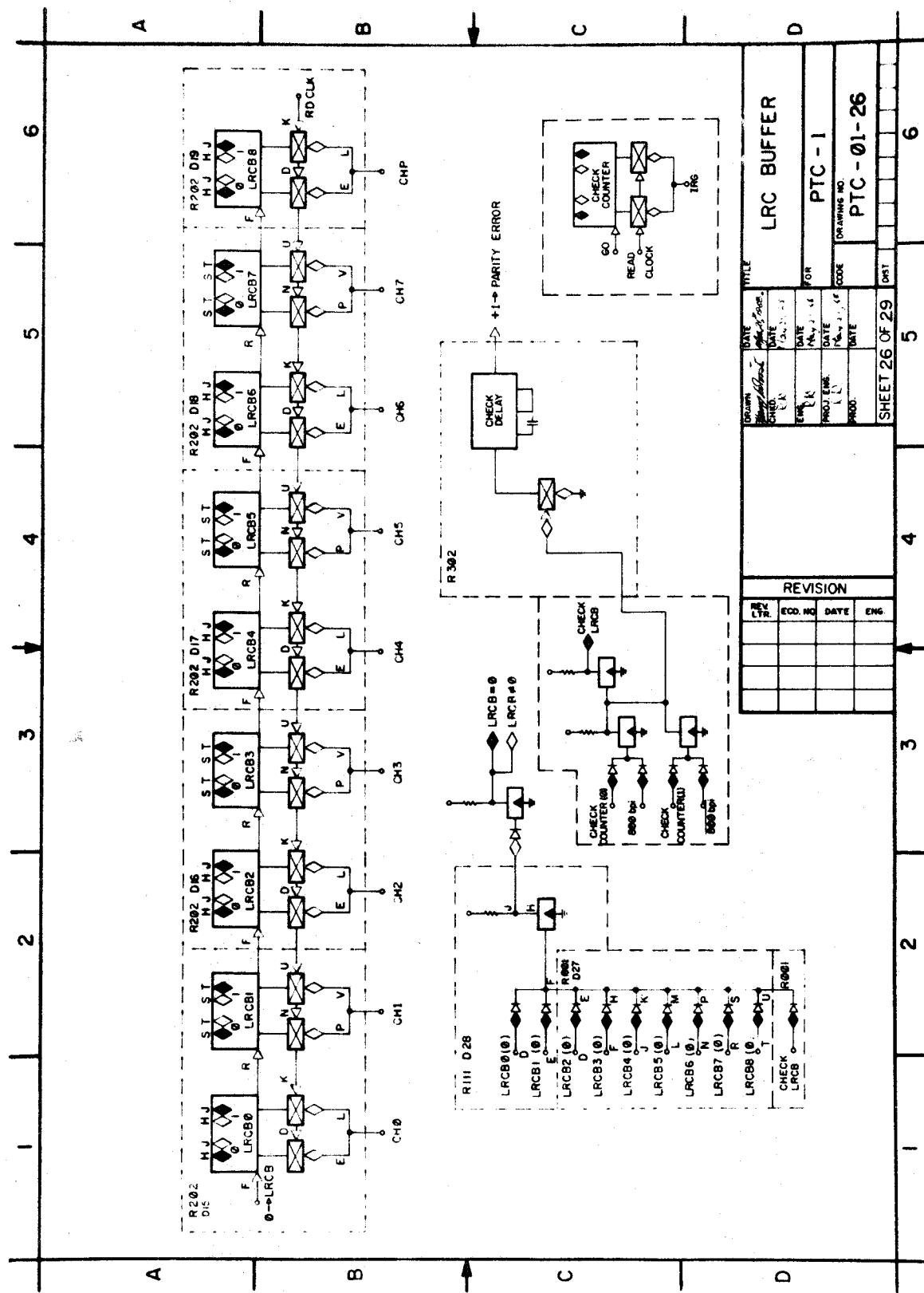


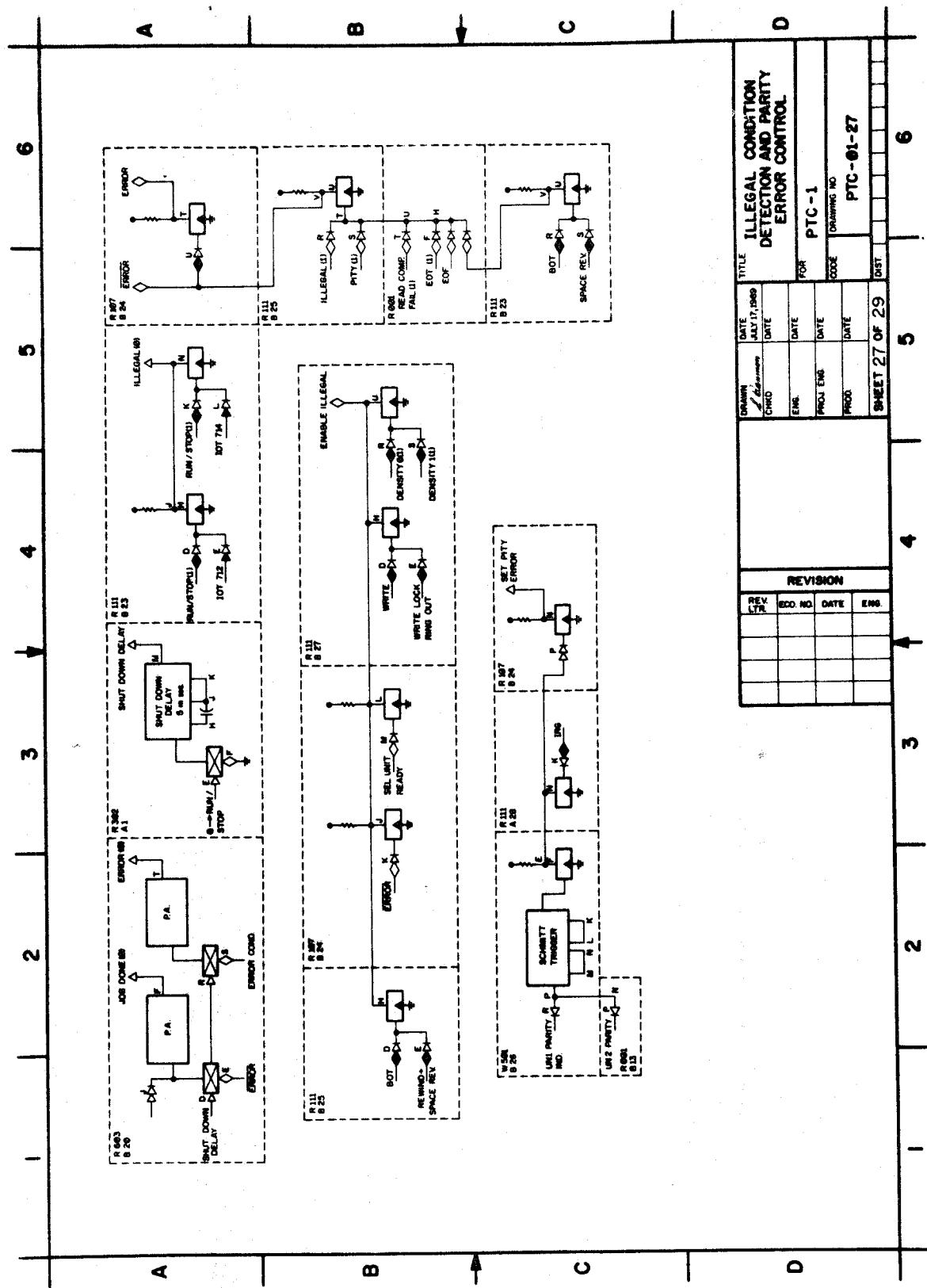


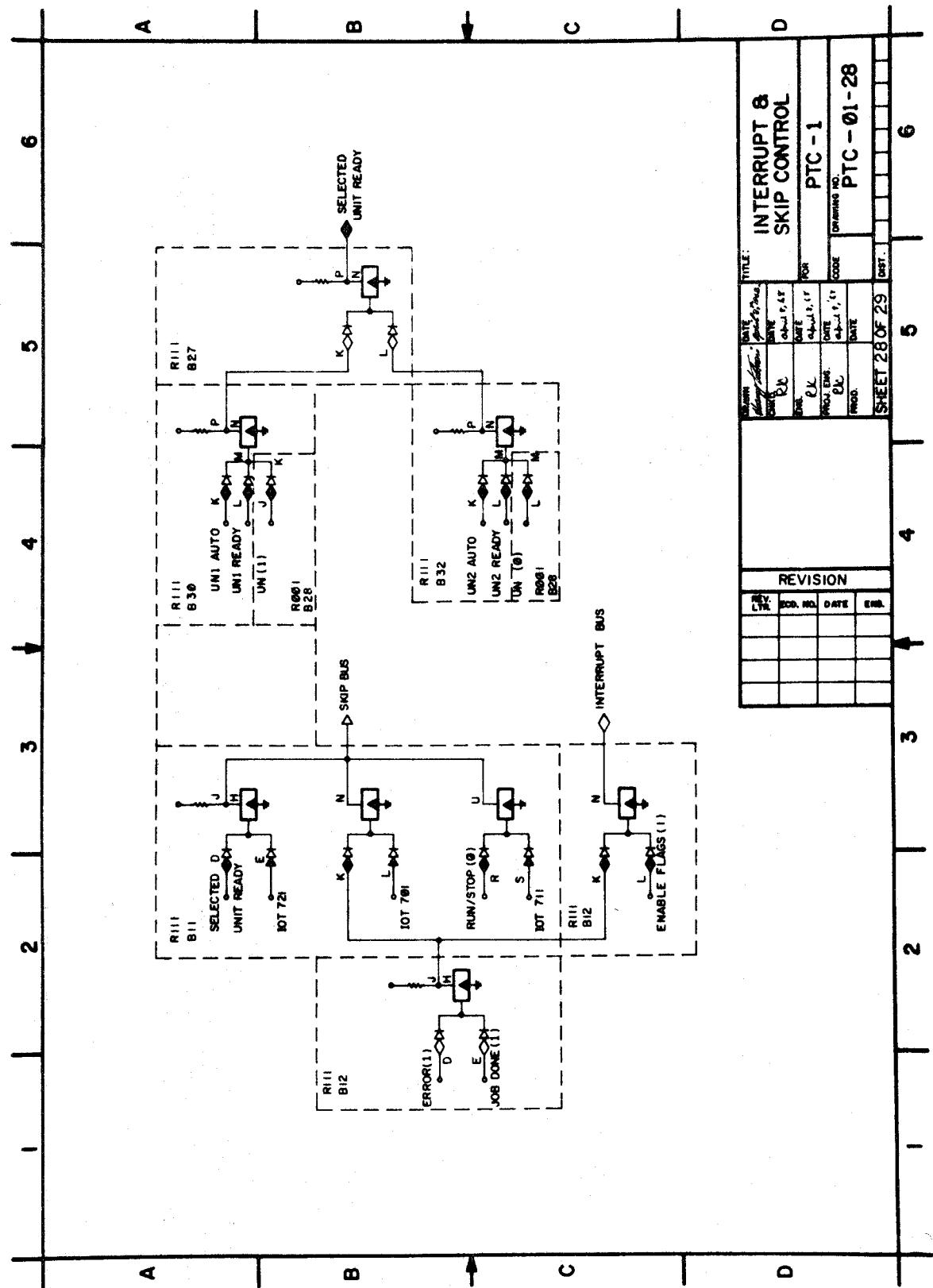


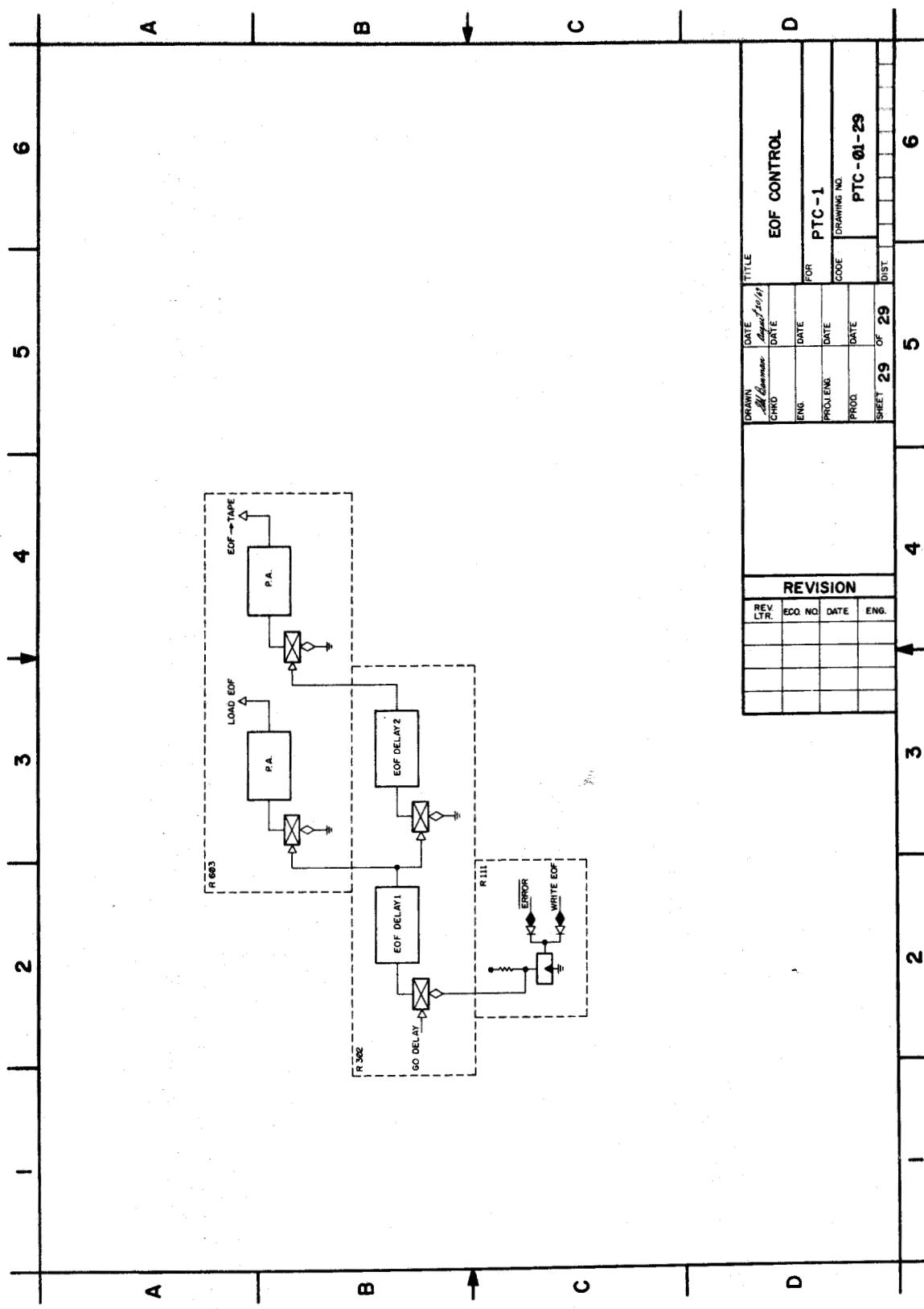












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APPENDICES

APPENDIX 1

EQUIPMENT SPECIFICATIONS

TABLE A.1.1. MT-36 TAPE TRANSPORT SPECIFICATIONS

Characteristic	Specification
Tape Speed	50 inches per second
Tape Speed Accuracy	2% at any speed above 15 inches per second
Rewind Time	Less than 3 minutes for a full 2400 feet of 1/2 inch 1.5 mil Mylar tape
Start Time	5 milliseconds from receipt of command to within 10% of rated speed
Start Distance	Over cycling range of 0 - 200 commands per second, tape travels 0.110 inches 5 milliseconds after receipt of command
Start Distance Accuracy	0.020 inches
Stop Time	3 milliseconds
Stop Distance	0.054 ±0.020 inches
Command Repetition Rate	0 - 200 commands per second, 5 milliseconds between commands for performance within specification
Wow and Flutter	Less than 2% rms
Interchannel Time Displacement (any two channels of 1/2" tape)	Static 8 microseconds (maximum) Dynamic 6 microseconds (maximum)
Tape Width	1/2 inch
Tape Reels and Hubs	IBM type 10-1/2 inch reels and hubs

APPENDIX 2

This appendix lists the details necessary to interface the transports and data electronics with the tape control unit.

TABLE A.2.1. TRANSPORT INTERFACE SIGNALS

Designation	Interface Details
Run/Stop	- 5V RUN input at 6ma sink enables the pinch roller drive, OV STOP signal inhibits the pinch roller drive
FWD/REV	- 5V REV input at 6ma sink initiates the operation in the reverse direction. OV FWD input initiates forward operation. This signal operates in conjunction with NORMAL/HIGH SPEED signal
NORMAL/HIGH SPEED	- 5V HIGH SPEED input at 5ma sink selects high speed. OV NORMAL selects normal speed operations
READY	- 10V READY output signal at 5ma source signifies tape transport ready for operation
EOT	- OV output when the tape is at the EOT marker and -15V at 5ma indicates the tape is not at EOT
BOT	- OV output when the tape is at BOT - 15V at 5ma indicates that the tape is not at BOT
AUTO INDICATION	- 7.5V at 2ma source signifies that transport is in automatic mode
W.L.O. SW N.C.	- Write Lock out switch normally closed contact
W.L.O. SW COM	- Write Lock out switch common contact
W.L.O. SW N.O.	- Write Lock out switch normally open contact

TABLE A.2.2. DATA ELECTRONICS INTERFACE SIGNALS

Function	Description	Number of Lines	Signals
Write	Write Data Input Lines	9	Level: 1=0V at 1.5ma 0=-3.5V to -15V
Write	Write Clock	1	Pulse (1 microsecond) 1=0V at 1.5ma 0=-3.5V to -15V
Control	Write Enable	1	Level 1=0V at 1.5ma 0=-3.5V to -15V
Control	Write LRC	1	Pulse (2 microseconds) 1=0V at 1.5ma 0=-3.5V to -15V
Control	Read Reset	1	Pulse (2 microseconds) or level 1=0V at 1.5ma 0=-3.5V to -15V
Control	Low Threshold Level Select	1	Level 1=0V at 1.5ma 0=-3.5V to -15V
Control	FWD/REV Select FWD = 1	1	Level 1=0V at 1.5ma 0=-3.5V to -15V
Control	End-of-Block (EOB) Inhibit	1	Level 1=0V at 1.5ma 0=-3.5V to -15V
Control	Even/Odd Parity Select Even = 1	1	Level 1=0V at 1.5ma 0=-3.5V to -15V
Control	200 BPI Select	1	Level 1=0V at 1.5ma 0=-3.5V to -15V
	556 BPI Select	1	Level 1=0V at 1.5ma 0=-3.5V to -15V

Table A.2.2. continued

Function	Description	Number of Lines	Signals
Control	800 BPI Select	1	Level 1=0V at 1.5ma 0=-3.5V to -15V
Read	Read Data Output	9	Pulse (0.5 to 20 μ secs.) 1=0V 0=-10V
Read	Read Clock Output	1	Pulse (0.5 to 2.0 μ secs.) 1=0V 0=-10V
Control	Parity Indication	1	Pulse (0.5 to 2.0 μ secs.) 1=0V 0=-10V
Control	End of Block Indication	1	Pulse (1 millisecond) 1=0V 0=-10V

APPENDIX 3

LOGIC SYMBOLS

In order to achieve maximum compatibility with the overall cartographic system, the tape control unit has been designed using Digital Equipment Corporation (DEC) logic modules and documented using the DEC symbols.

A.3.1 Standard Logic Levels:

The standard logic voltage level used by the DEC logic modules is "ground" (0 to -0.3 volts) or -3 volts (-2.5 to -3.5 volts). All logic signals in general, are identified by their names (mnemonic or otherwise) and shown in asserted condition on the drawings. An open diamond ($\text{---}\diamond\text{---}$) indicates a standard logic level of ground on the line represents assertion. On the other hand, a solid diamond ($\text{---}\blacklozenge\text{---}$) represents a standard negative level is the asserting condition.

A.3.2 Standard Pulses:

Standard pulses used by the DEC logic are about 3 volts in amplitude and 100 or 400 nanoseconds wide as required by a specific circuit configuration. Positive going pulses (-3 volts to ground) are represented by an open arrow ($\text{---}\rightarrow\text{---}$) and negative going pulses are represented by a solid arrow ($\text{---}\blacktriangleright\text{---}$).

A.3.3 Level Transitions:

On many occasions where diode-capacitor-diode (DCD) gates are present, the transition of a level is used at an input where a pulse is

expected. The DCD gates respond to the level transitions because of their differentiating configuration (see A.3.4.2). A composite symbol (such as ) is used to indicate a level transition usage. The arrow head in the composite symbol is drawn open or solid depending on whether a positive or negative transition triggers the circuit action. Also, the shading of the diamond is either the same as the arrow head to indicate triggering on the leading edge or opposite to indicate triggering on the trailing edge of the level transition. When triggering with the output of a delay module (see section A.3.4.4), it is common to show only the arrow instead of the composite symbol with the explicit understanding that the delay modules provide only level transitions.

Table A.3.1 summarizes the logic symbols used in preparing the engineering drawings for this thesis.

TABLE A.3.1.

Symbol	Significance
	Ground level
	-3V level
	Positive going pulse
	Negative going pulse
	Negative level transition and triggering on the trailing edge

A.3.4 Logic Circuits and Symbols:

This section is a brief account and functional description of the logic circuits available in DEC modules together with the symbols used to represent them.

A.3.4.1 Diode gates

Inverting diode gates are the extensively used circuits to generate the desired logic signals. Figure A.3.1 shows the symbol used for the basic gate configuration. These gates perform a NAND function for negative signals at the input and NOR function for ground signals.

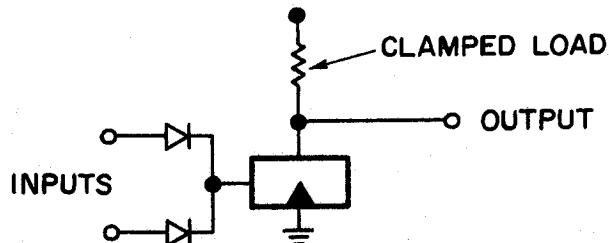


Figure A.3.1: Diode Gate

A.3.4.2 Diode-Capacitor-Diode gates

The Diode-Capacitor-Diode (DCD) gates are used in DEC logic circuits to standardize inputs for various circuits such as flip-flops, single shots and pulse amplifiers. Figure A.3.2 shows the symbol used to represent a DCD gate.

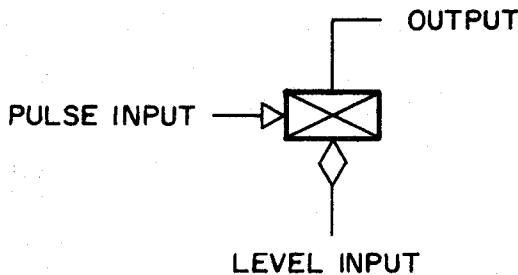


Figure A.3.2: DCD Gate Symbol

For a signal to appear at the output as a result of the pulse input in a DCD gate, the level input must be held at the ground level for a specified time (typically 400 nanoseconds) before the pulse is applied. The gate remains enabled for approximately the same period after removing the enabling level input. Because of the presence of a capacitor, the DCD gate can differentiate the pulse input; thus making it possible to use level transitions to obtain an output.

The DCD gates are useful in practice for three reasons:

- (a) They provide logical isolation between the pulse and level inputs.
- (b) They provide a logical delay or temporary memory action.
- (c) They provide a logical AND function as long as their memory action is taken into account.

Since many DCD gates may be driven by the same pulse input, the side of the rectangle opposite the pulse input is used to show the continuation of the same line as shown in Figure A.3.3.

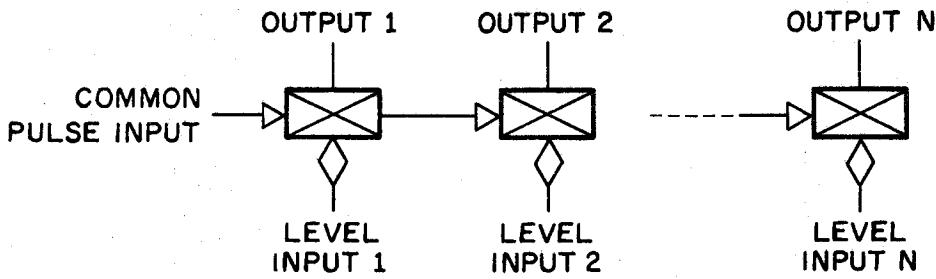


Figure A.3.3: Representing a Number of DCD Gates Driven by the Same Pulse

A.3.4.3 Flip-flops

Flip-flops in DEC modules are packaged using two diode gates and Figure A.3.4 shows the symbol used. The flip-flops may be set or reset by driving the appropriate input to ground; when the flip-flop is set, the '1' output is at -3 volts. In addition to the direct set and reset inputs flip-flops are usually provided with one or more DCD gates. The DCD gates provide sufficient delay so that information from one flip-flop may be transferred into another flip-flop such that the first flip-flop can receive a command to change state at the same time as the transfer command. The flip-flops can be operated in a complementing mode simply by holding the level inputs of the set and reset DCD gates at ground level. The flip-flops can also be set and reset from the output side by driving the appropriate output to ground momentarily. The outputs from a flip-flop are usually identified by its names and the contents are shown in parentheses following the name. For example, BRK CNT (0) means the flip-flop called BRK CNT is in zero state.

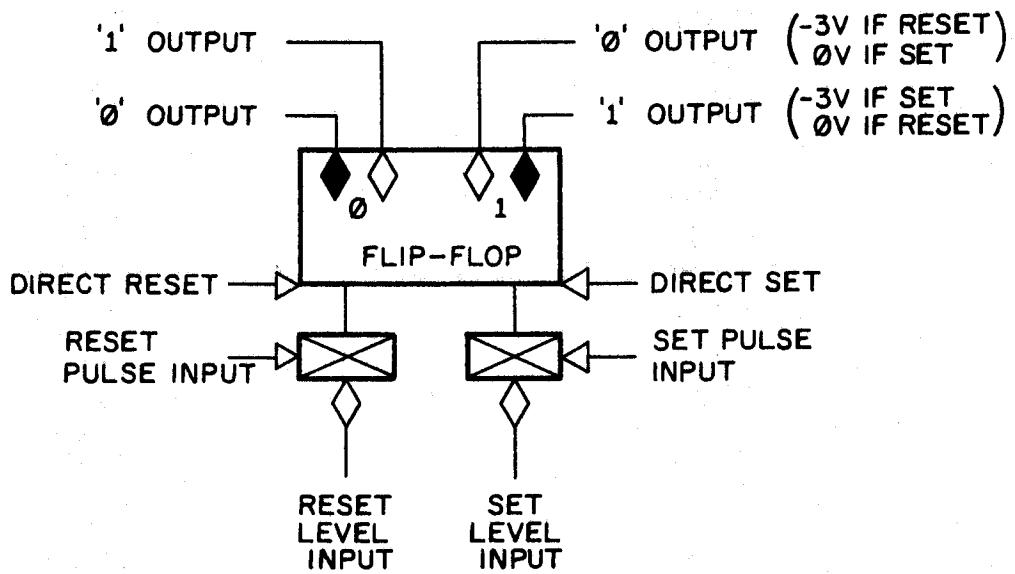


Figure A.3.4: Flip-flop Symbol

A.3.4.4 Delay modules

The input to the delay circuits in DEC modules is always through a DCD gate and Figure A.3.5 shows the symbol used to represent the delay circuits. There are provisions made to connect an external capacitor to obtain the desired delay when the internal capacitor value is not sufficient. When a pulse is applied after applying the proper enabling level input, the output level changes from its normal ground to -3 volts for a fixed, but adjustable length of time.

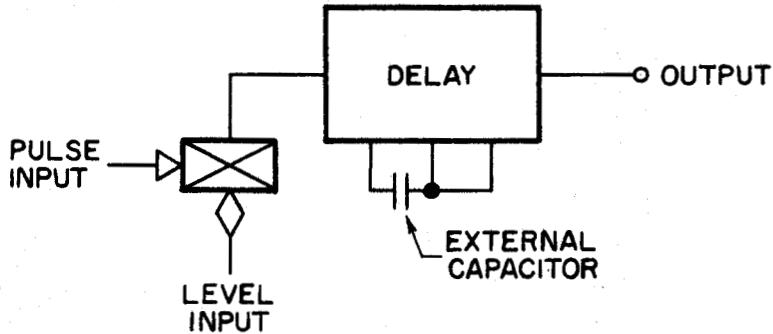


Figure A.3.5: Symbol Used for a Delay Circuit

A.3.4.5 Pulse amplifiers

Pulse amplifiers shown symbolically in Figure A.3.6 are very versatile elements because they not only amplify and standardize various signals into positive going pulse but also can be used to perform logic using the DCD gates on the inputs.

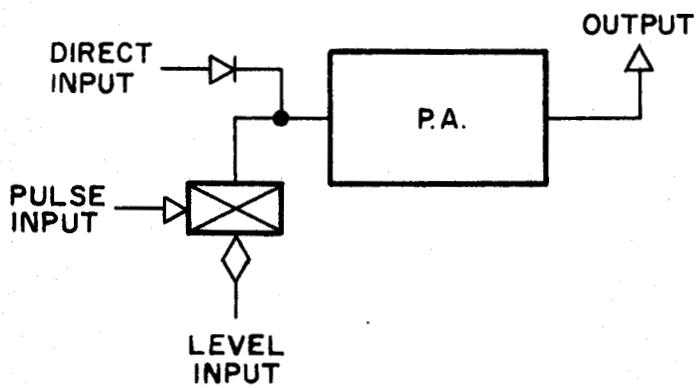


Figure A.3.6: Pulse Amplifier Representation