A General Technique for Derivation of Average Current Mode Control Laws for Single-Phase Power-Factor-Correction Circuits Without Input Voltage Sensing

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***Abstract*— This paper presents a general technique to derive average current mode control (CMC) laws without input voltage sensing to achieve high power factor for single-phase topologies operating in continuous conduction mode (CCM). The control laws are derived based on the steady-state input–output voltage relationships and the CCM large-signal averaged pulsewidth modulation (PWM)-switch model. Using this methodology, average CMC laws with linear PWM waveforms are discovered for commonly used single-phase power stage topologies such as boost, flyback, SEPIC, and buck+boost. Conventional three-loop-controlled average CMC converters can now be controlled with a two-loop architecture. Hardware results for a boost power factor correction (PFC) and simulation results for flyback, SEPIC, and buck+boost topologies verify operation. The small-signal models of the current loop and voltage loop are derived for the boost topology and are used for control loop design. Input current harmonic distortion measurements demonstrate improved performance compared to the conventional three-loop control technique.**

***Index Terms*— Feedback control, power factor correction, single-phase.**

I. Introduction

AVERAGE current mode-controlled (ACMC) power-factor-correction (PFC) techniques utilizing converters operating in continuous conduction mode (CCM) are the primary choice for many medium- and high-power applications. A very popular control technique to implement ACMC is the three-loop architecture as implemented in [1]. The current programming signal sets the reference for a high-bandwidth fast-acting current loop. The amplitude of the current programming signal is slowly modulated by the low-bandwidth output voltage error signal and the low-pass-filtered line voltage rms signal to ensure steady-state input–output power balance. The need for a squarer–divider–multiplier circuit in the control integrated circuit (IC) to ensure power balance under changes in load and line rms voltage is explained in [2]. If the current programming signal is not derived from the line explicitly, the advantages in eliminating the squarer, divider, and multiplier circuitry in the integrated circuit (IC) and reduction in external passive components are obvious.

Methods for achieving high power factor without input voltage sensing for converters operating in CCM have been recently reported in [3]–[5]. In [3] and [4], the steady-state input–output voltage relationships of the boost and flyback topologies along with the average switch current information were utilized to derive "nonlinear" pulsewidth modulation (PWM) waveforms that provide high power factor. This paper presents a simple and general technique to utilize current information in various branches in the power stage to implement PFC laws without input voltage sensing. Based on ease of implementing the PWM waveforms, current sensing, and current-loop small-signal stability a suitable PWM scheme can then be chosen. The control laws of [3] and [4] are a subset of the possible control laws discovered in this work. The use of certain branch currents along with a suitable averaging circuit implementation enables "linear" PWM carrier waveforms and is the main topic of this paper. Linear PWM waveforms are in general much more easier to implement on chip and reproduce consistently over temperature and process; the methodology presented here utilizes a very simple procedure based on the CCM large-signal averaged PWM switch model. In [5] "linear" PWM waveforms for peak current mode control are presented for the boost and buck–boost topologies. An extension to provide linear ACMC PFC by injecting an external ramp signal so as to cancel the ripple component of inductor current is also presented in [5].

The first objective of this paper is to present a general procedure to derive linear PWM waveforms that provide PFC without input voltage sensing. The key step is to derive a set of possible PWM waveforms using the large-signal averaged CCM PWM-switch model for a given power stage topology

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and then choose the branch currents that yield a suitable PWM waveform. Use is made of the fact that there is a significant time-scale separation between the switching frequency and variation of the full-wave rectified line voltage. The approach is to design a pulse width modulation control law based on the steady-state relationships and then ensure that the control law is being satisfied by using a suitably designed fast control loop. The second objective is to verify its feasibility and performance through hardware implementation. In Section II, the general technique to derive PWM strategies is presented and applied to commonly used single-phase power stage topologies such as the boost, flyback, SEPIC, and buck+boost topologies. It is shown that linear PWM waveforms yield ACMC PFC for all of these topologies. The key features of operation, use of an integrate-and-hold scheme, and the hardware performance results for the boost PFC using the new PWM waveform are detailed in Section II. Section III presents the small-signal model and current loop gain characteristics for the PFC scheme using a boost topology. The harmonic performance of this control technique is presented in Section IV. The model for voltage-loop design is presented in Section V. This technique of performing PFC without input voltage sensing has been filed as a patent application by Virginia Tech and SGS-Thomson [10].

II. A General Technique for Linear PWM Waveform Derivation

The general four-step procedure to derive PFC control laws can be stated as follows.

Step 1): The objective of PFC is expressed as

$$\langle i_{\rm in}\rangle = \frac{V_{\rm in}}{R_{eq}}$$

where R_{eq} is the load impedance magnitude reflected to the input terminals of the power stage. Transformation of the load impedance to the input terminals can be easily performed with the use of equivalent circuits models such as the PWM-switch model [6].

Step 2): The CCM steady-state input–output voltage relationship for the given topology is determined and substituted for $V_{\rm in}$ in the above equation.

Step 3): Using the PWM-switch model, the relationships between the various branch currents and input current is determined for the given topology.

Step 4): Substituting the results of Steps 2) and 3) in Step 1), a set of solution candidates are obtained.

A. Application to Boost Family of Topologies

The technique to derive linear PWM waveforms for ACMC PFC is illustrated in detail using the boost topology as an example.

Fig. 1 shows the schematic of the boost topology with the three terminals active, passive, and common marked to facilitate application of the large-signal averaged PWM-switch model [6] relationships.

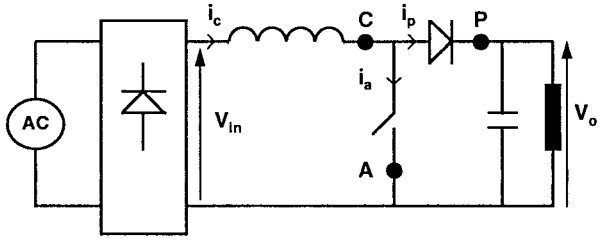


Fig. 1. Boost power stage with the PWM-switch model terminals A, C, and P.

The main objectives of the application of this circuit are: 1) to provide high power factor at the input (resistor emulation) and 2) regulate the output voltage V_o. The first objective, using average current mode control can be mathematically expressed as

$$\langle i_{\rm in}\rangle = \frac{V_{\rm in}}{R_{eq}} \tag{1}$$

where $\langle i_{\rm in}\rangle$ is the average value of input current over a switching period $T_s, V_{\rm in}$ is the instantaneous value of line voltage, and R_{eq} is an equivalent resistance whose magnitude is that of load, reflected to the input terminals of the boost power stage. By application of the large-signal-averaged PWM-switch model [6], CCM relationships

$$\langle i_{\rm in}\rangle = \langle i_c\rangle = \frac{\langle i_a\rangle}{D} = \frac{\langle i_p\rangle}{(1-D)} \tag{2}$$

where $\langle . \rangle$ refers to switching frequency averages and D is the duty ratio of the main switch. The branch currents are as defined in Fig. 1. In this analysis it is assumed that the input voltage is constant over a switching period (quasi-static approach). Given the significant time-scale separation between the switching frequency and the line frequency this assumption is well justified. The steady-state input–output conversion ratio of the boost topology is

$$V_{\rm in} = V_o.(1-D). \tag{3}$$

Substituting (2) and (3) in (1), we can derive a set of equations, each of which satisfies the two objectives

$$\langle i_{\rm in}\rangle = \frac{V_o}{R_{eq}}.(1-D) \tag{4a}$$

$$\langle i_a\rangle = \frac{V_o}{R_{eq}}.(1-D).D \tag{4b}$$

$$\langle i_p\rangle = \frac{V_o}{R_{eq}}.(1-D)^2. \tag{4c}$$

Let us first examine (4a). The physical meaning of this equation is as follows. In every switching cycle, if the power switch is turned ON/OFF (in the conventional trailing edge modulation sense, with a duty ratio D), when the average value of the input current over an entire switching cycle is equal in value to a waveform whose time variation is given by $(V_o/R_{eq}).\ (1 - t/T_s)$, then resistor emulation is obtained. The graphical interpretation of the above statement is shown in Fig. 2.

The switch is turned ON at the beginning of the switching cycle and turned OFF when the average value of input current

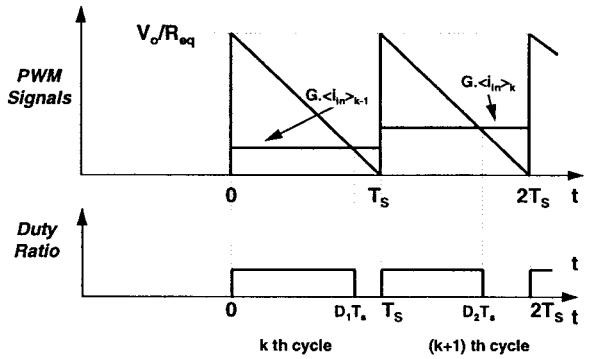


Fig. 2. Graphical interpretation of the PFC control law PWM strategy.

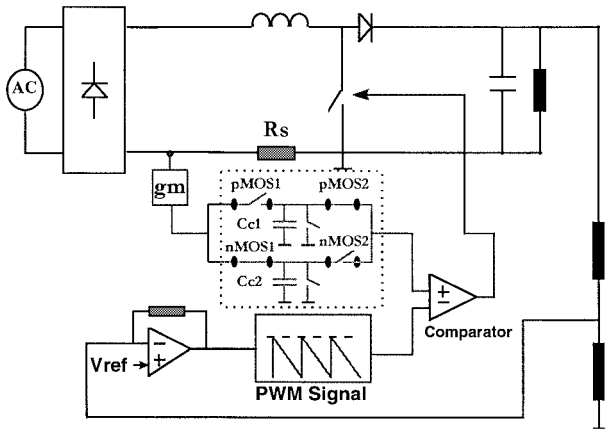


Fig. 3. Simplified schematic of power stage and control circuit.

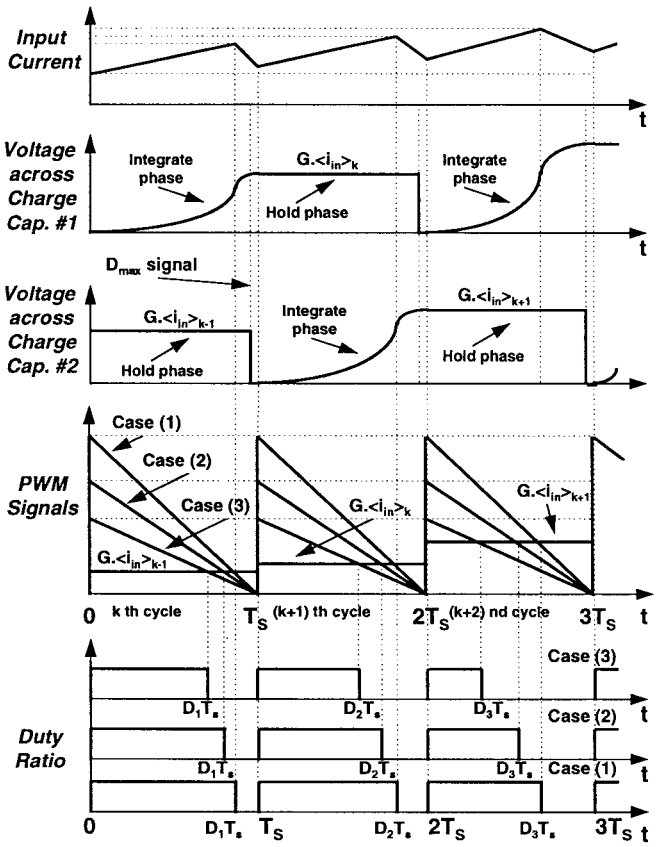


Fig. 4. Key waveforms of the new linear average CMC PWM technique for PFC using the boost power stage.

equals the PWM ramp. An important point which may not be readily obvious needs clarification. The control law that we have just described, requires the duty ratio during one switching period to be determined by the average value of current during the entire period. This is not possible in a causal system. However, due to fact that the input voltage varies very slowly between two consecutive switching cycles, use of the average value of input current during one switching period to determine duty ratio in the next period is justified. This is implemented by holding the average value of current in one cycle and using it from PWM in the next cycle as shown in Fig. 2. The simplified schematic of the power stage and control circuit is shown in Fig. 3. The key waveforms associated with operation are shown in Fig. 4.

Prior to $t = 0$, C_{c1} has been fully discharged and its voltage $V_{c1} = 0$. The reset switch is open after the discharge operation and continues to remain so until $t = 2.T_s$. From $t = 0$ to $t = T_s$, the input (inductor) current is used to charge capacitor Cc1. A resistive sensing network provides a voltage proportional to input current, and is the input to a voltage-to-current (V2I) converter circuit (transconductance amplifier) in the current loop. The V2I converter circuit produces a charging current that drives the charge capacitor. The voltage across the charge capacitor C_{c1} is given by

$$V_{c1} = \frac{R_s.g_m}{C_{c1}} \int_0^{T_S} i_{\text{in}}.\,dt = \frac{R_s.g_m}{C_{c1}}.\langle i_{\text{in}}\rangle \qquad (5)$$

where R_s is the current sense resistor (Fig. 3) and g_m is the gain of the V2I converter. At $t = D_{\max}.T_s$, the charge control circuit discharges charge capacitor C_{c2} and sets the initial conditions correct for the charging and averaging operation from $t = T_s$ to $t = 2.T_s$. At $t = T_s$, the charge control circuit "holds" the voltage across C_{c1} by causing the gate signals to pMOS1 and pMOS2 to go high and low, respectively. Simultaneously the gate signals to nMOS1 and nMOS2 are commanded high and low, respectively. During the time interval $t = T_s$ to $t = 2.T_s$, the held value of voltage across C_{c1} is compared with the PWM ramp waveform to determine the duty ratio. While the waveshape of the PWM ramp signal was established in (4a), the dynamics of the signal are shown for three cases of output voltage error in Fig. 4. These three cases correspond to: 1) a large-output voltage error; 2) a smaller output voltage error; and 3) an even smaller output voltage error. In the hardware implementation, a signal proportional to the output voltage, the output voltage-loop error amplifier signal is used to determine the ramp amplitude. This enables the use of a voltage-loop amplifier to obtain the required voltage-loop gain. The dynamics of the output voltage error signal are determined by the conventionally designed output voltage control loop whose unity gain crossover frequency is about 10–20 Hz.

The PWM technique described above uses PWM ramp amplitude modulation to achieve the output voltage regulation. The PWM waveshape, together with the a suitable

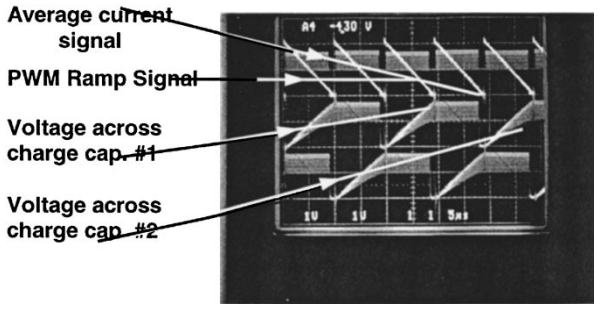


Fig. 5. Key waveforms for boost PFC control.

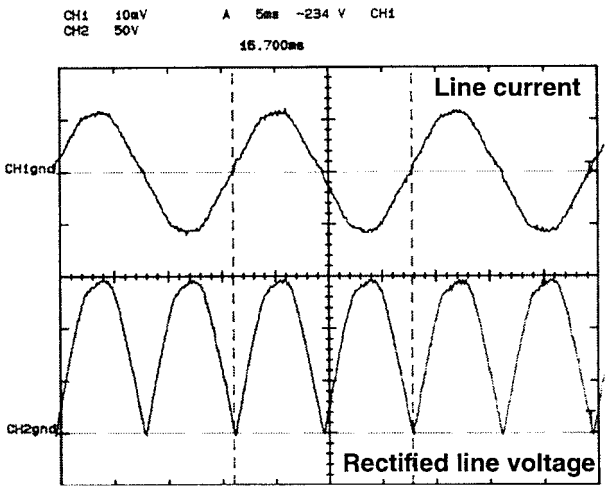


Fig. 6. Line current and full-wave rectified line voltage with the new PFC control technique with boost topology.

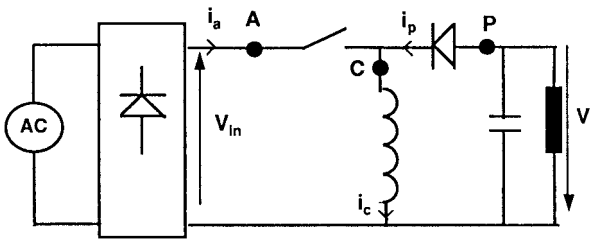


Fig. 7. Buck–boost power stage with the PWM-switch model terminals A, C, and P.

branch current sensing and toggled capacitors averaging circuit, enables PFC.

Fig. 5 is a snapshot of the PWM ramp signal, the average of input current, and the integrate-and-hold operation of the two charge capacitors. This photograph of operation of the control board prototype captures the variations of the four quantities over part of an ac line voltage cycle. Fig. 6 shows the current drawn from the line and the full-wave rectified line voltage.

B. Application to Buck–Boost Family of Topologies

The general four-step procedure outlined in Section II is now applied to derive PFC control laws for the buck–boost family of topologies, such as the flyback and SEPIC topologies which are used for PFC. Fig. 7 shows a simple buck–boost topology with the three PWM-switch terminals marked.

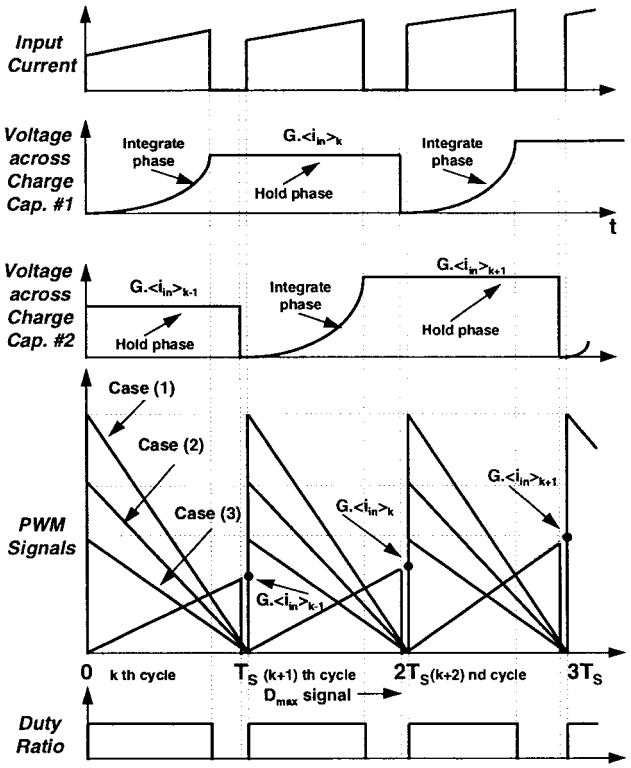


Fig. 8. Key waveforms of the new linear average CMC PWM technique for PFC using the flyback power stage.

The application of the control law derivation procedure is outlined below

$$\text{Step 1:}\quad \langle i_{\text{in}}\rangle = \frac{V_{\text{in}}}{R_{eq}} \tag{6}$$

$$\text{Step 2:}\quad \langle i_{\text{in}}\rangle = \langle i_a\rangle = D.\langle i_c\rangle = \frac{D}{(1-D)}\,\langle i_p\rangle \tag{7}$$

$$\text{Step 3:}\quad V_{\text{in}} = V_o\frac{(1-D)}{D} \tag{8}$$

$$\text{Step 4:}\quad \langle i_{\text{in}}\rangle = \frac{V_o}{R_{eq}}\,\frac{(1-D)}{D} \tag{9a}$$

$$\langle i_c\rangle = \frac{V_o}{R_{eq}}\,\frac{(1-D)}{D^2} \tag{9b}$$

$$\langle i_p\rangle = \frac{V_o}{R_{eq}}\,\frac{(1-D)^2}{D^2}. \tag{9c}$$

The control law chosen is (9a). A simple manipulation yields a simplified control law

$$\frac{t}{T_s}\langle i_{\text{in}}\rangle = \frac{V_o}{R_{eq}}\left(1-\frac{t}{T_s}\right). \tag{10}$$

Fig. 10 shows all the key waveforms associated with the control action. The top figure is the input current whose average value is computed by charging the capacitors. As in the case of the boost PFC control strategy, the charge capacitors operate in tandem and the capacitor voltage waveforms are shown in Fig. 8.

The right-hand side (RHS) of (10) is the linearly decreasing ramp voltage waveform $(V_o/R_{eq}).(1-t/T_s)$ and is similar to the boost topology. The left-hand side (LHS) of (10),

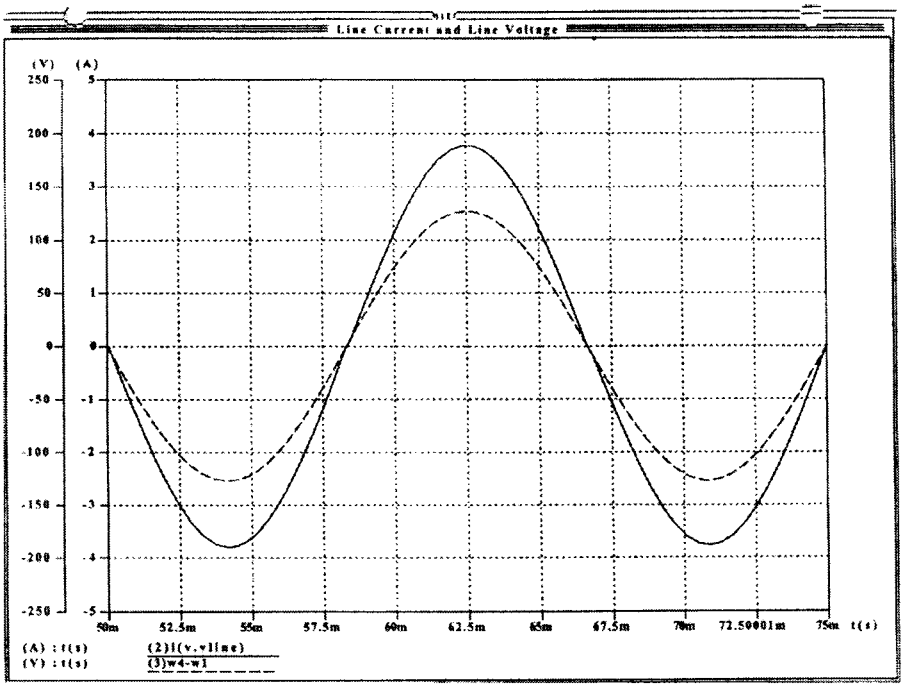


Fig. 9. Simulation results for a flyback PFC with the new control strategy using a large-signal averaged model; waveforms are line voltage and input current.

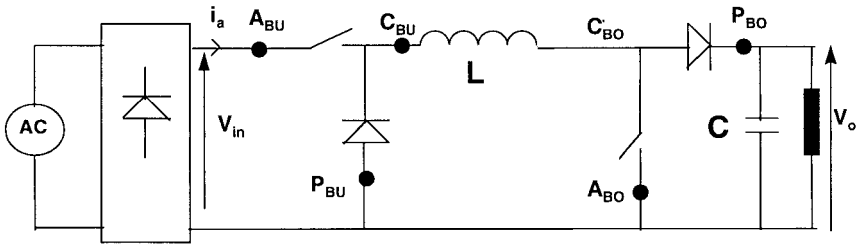


Fig. 10. Buck+boost power stage with PWM-switch terminals.

$t/T_s.\langle i_{\rm in}\rangle$ is a linearly increasing ramp waveform whose slope is proportional to the average value of input current during the previous switching cycle (held value of capacitor voltage). These two ramp waveforms are the inputs to the PWM comparator that determines the duty ratio.

A large-signal averaged model based on the PWM switch model that automatically discriminates between discontinuous conduction mode (DCM) and CCM modes of operation is a very useful tool in simulating PFC circuits that operate with average current mode control. Such a model was developed to investigate the PFC requirements of this new scheme as applied to the flyback topology. The use of the large-signal averaged model requires derivation of the large-signal averaged circuit of the PWM modulator. From the control law (9a), $D = V_C/(\langle i_{\rm in}\rangle + V_C)$. Waveforms of input current and line voltage for a flyback topology are shown in Fig. 9. In the SEPIC topology, the average value of input and switch current are the same in steady state. Based on sensing requirements either of the currents can be sensed and used to close the current loop.

C. Application to Buck+Boost Family of Topologies

The buck+boost topology [9] (Fig. 10) provides input current shaping and a low-voltage output in a single stage. The PWM-switch terminals active (A), passive (P), and common (C) are shown with subscripts BU (buck) and BO (boost), respectively. The circuit operates in boost mode when the instantaneous value of line voltage is less than the output voltage; the boost part of the circuit (S2, D2, L, C) provides high power factor and output voltage regulation; switch S1 is always ON during this mode. During the portion of the line cycle when the line voltage is greater than the output voltage, the buck part of the circuit (S1, D1, L, C) provides high power factor and output voltage regulation; switch S2 is always open during this mode. A PWM strategy that provides high power factor can be derived using the general four-step procedure:

Step 1): To achieve resistor emulation

$$\langle i_{\rm in}\rangle = V_{\rm in}/R_{eq}. \tag{11}$$

Step 2): For the buck topology operating in CCM, the input-voltage conversion voltage conversion ratio

$$V_{\rm in} = V_o/D. \tag{12}$$

Step 3): Applying the large-signal PWM switch relationships

$$\langle i_{\rm in}\rangle = \langle i_a\rangle = D.\langle i_c\rangle \tag{13a}$$

$$\langle i_{\rm in}\rangle = D/(1-D).\langle i_p\rangle. \tag{13b}$$

Step 4): Substituting the results of Steps 2 and 3 in Step 1, the possible PWM control laws are

$$\langle i_{\rm in}\rangle = \frac{V_o}{D.R_{eq}} \tag{14a}$$

$$\langle i_c\rangle = \frac{V_o}{D^2.R_{eq}} \tag{14b}$$

$$\langle i_p\rangle = \frac{(1-D)V_o}{D^2.R_{eq}}. \tag{14c}$$

Equations (14b) and (14c) are nonlinear in D. A simple manipulation of (14a) yields

$$D.\langle i_{\rm in}\rangle = \frac{V_o}{R_{eq}}.$$

Substituting the time variable for D, the control law for the buck topology is

$$\frac{t}{T_S}.\langle i_{\rm in}\rangle = \frac{V_o}{R_{eq}}. \tag{15}$$

The graphical interpretation of the control law is shown in Fig. 11. A signal whose slope is proportional to the average value of input (switch) current is compared with the voltage-loop error amplifier output. The switch is turned ON at the beginning of the switching period and is turned OFF at the intersection of the two signals. Duty ratio determined by this scheme thus implements control law (15). For the boost mode, the control law (4a) is implemented. The same input current which is sensed for buck mode operation is used for the boost mode; the switch current in buck mode is the input current for boost mode as switch S1 is always closed. Simulation results based on the large-signal averaged PWM model are shown in Fig. 12. Shown are the waveforms of input current and line voltage and the duty ratios of the buck and boost switches.

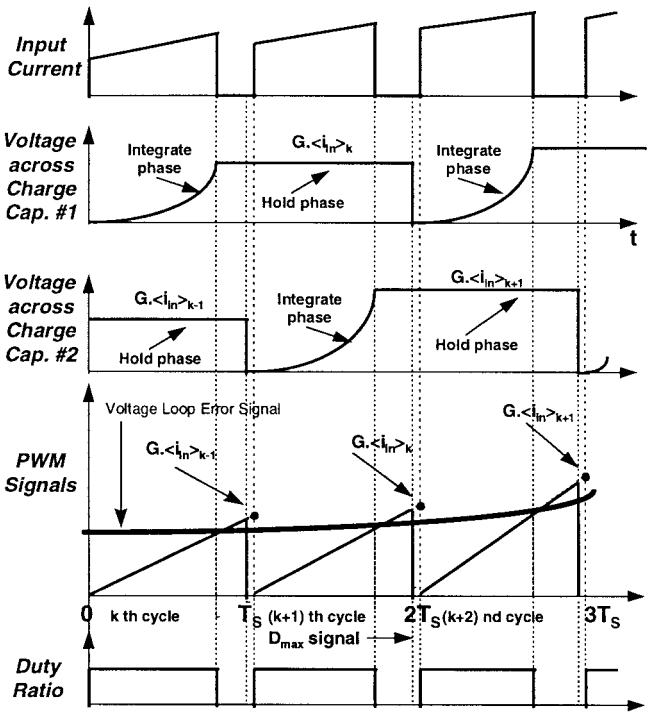


Fig. 11. Salient control waveforms for PFC strategy as applied to buck–boost family of topologies.

III. Characteristics and Small-Signal Model of the Current Loop for the Boost Topology

The small-signal model of the proposed PFC scheme for purposes of current loop design is shown in Fig. 13. The current loop gain is given by $Ti = (il/d).R_i.g_m.(T_s/C_c).He(s).F_m$, where il/d is the duty ratio to inductor current transfer function, R_i is the input current sense resistor, g_m is the transconductance of the amplifier which converts the voltage across R_i to a current which charges the integration capacitor C_c, T_s is the switching time period, $He(s)$ is the continuous-time expression for the sampling effect [7], and F_m is the small-signal gain of the PWM modulator. For the linear PWM waveform used in the boost topology, from geometric considerations, the small-signal gain magnitude of F_m can be derived to be $-1/V_m$, where V_m is the amplitude of the PWM ramp. The phase lag introduced by action of the "hold" circuit is equivalent to the action of an uniformly sampled modulator. The phase lag is given by $F_m = D.f/fs{*}360°$ [8]. The gain k is determined by the magnitude of the output voltage error. For a current converter with $L = 1$ mH, $C = 450$ uF, $V_o = 400$ V, $R_i.g_m = 1$ m, $C_c = 10$ nF, $fs = 100$ kHz, a current loop with a phase margin of 40° (measured with respect to −360°), a unity gain crossover frequency of 10 kHz was designed.

The current loop gain T_i is given by

$$T_i = \frac{V_o.(s+2/C.R_L)}{D_p^2.L_e.(1+s/Q\omega_n+s^2/\omega_n^2)} .R_i.g_m.\frac{T_s}{C_c}.He(s).\frac{1}{V_m}.e^{-2.\pi.D.f/fs}. \tag{16}$$

The notation used is as in [11] and in the previous paragraph. Fig. 14(a) and (b) shows the current loop gain plot as measured from a prototype; the magnitude and phase from (16) are marked in the figure. It can be seen that the theoretical predictions are quite accurate and can be used to design the current loop.

As in conventional three-loop-controlled [1], [2] converters, the current loop gain varies with line; however, the characteristics of current loop gain for the new PFC scheme are different. In the region of crossover frequency, the dominant term that determines the magnitude of current loop gain is V_m. The basic strategy of this control scheme is to control V_m to regulate output voltage. This variation of V_m with load causes the magnitude of current loop gain to vary with load as shown in Fig. 15(a). At light loads (small V_m), the increase in current loop gain crossover frequency may cause insufficient phase margin leading to current loop instability. This instability can be eliminated by addition of an external ramp to the averaged current information.

For a given load, the phase of current loop gain varies with instantaneous value of line voltage. This is because of the action of the uniformly sampled modulator. Near the zero crossings of the line voltage, the value of duty ratio is the highest. This causes a proportionally longer delay as given by

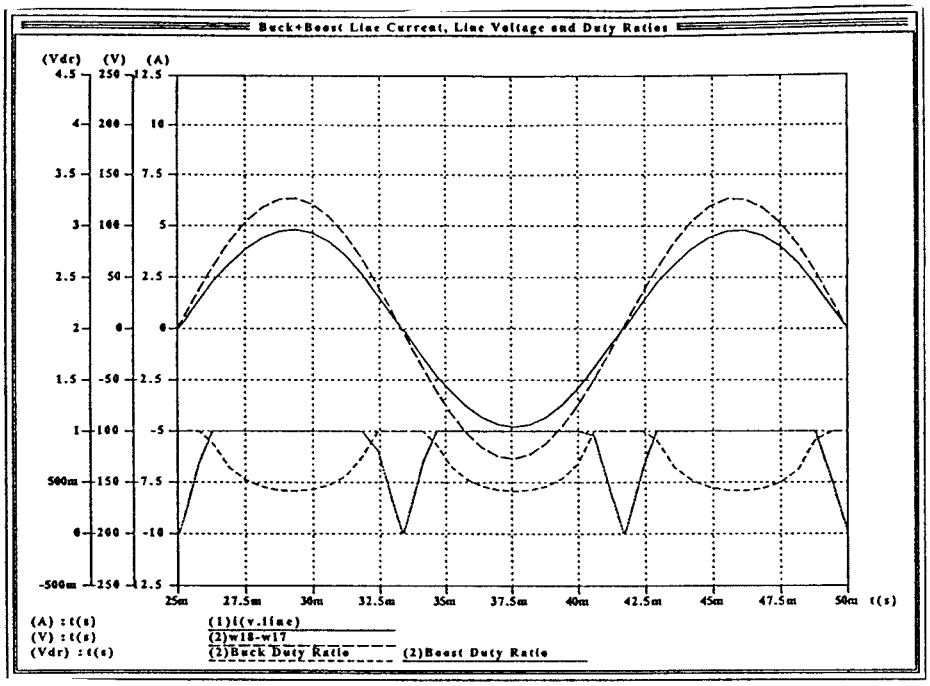


Fig. 12. Input voltage, input current, and duty ratios of buck+boost topology. Simulation results from a large-signal averaged PWM switch model.

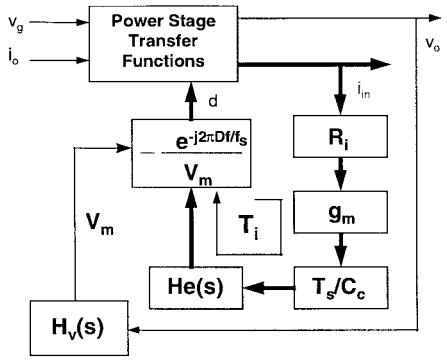


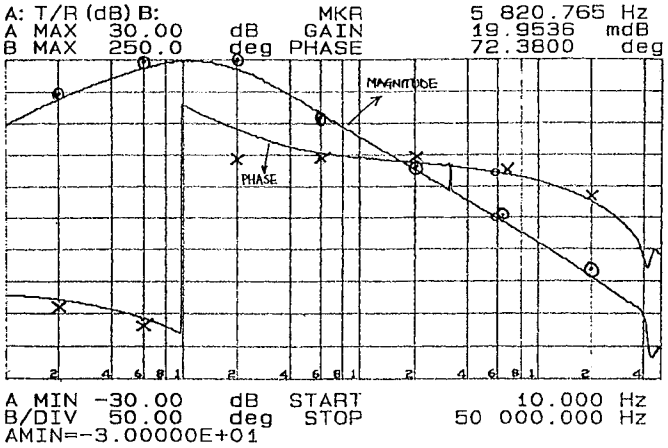
Fig. 13. Small-signal model for the proposed control scheme.

the phase-lag term $e^{-2\pi Df/fs}$. The variation of current loop phase with instantaneous value of line voltage is shown in Fig. 15(b).

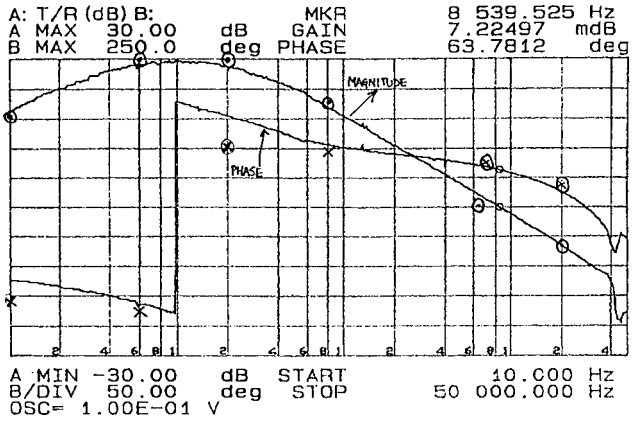
The current loop gain was designed at rms value of line voltage and nominal load for the prototype hardware. Parameters for the design of the current loop are R_i, C_c, and the addition of an external stabilizing ramp. Design of the low-crossover frequency outer voltage loop can be performed as outlined in [1]. The current loop gain has been verified experimentally at various operating points and is useful for design of the current loop and external stabilizing ramp.

IV. Current Distortions and Harmonics

The low-frequency harmonic components in line current with the new power factor control scheme and the conventional three-loop control scheme were measured. To isolate and identify the harmonic sources, the measurements were performed with and without the voltage loop open. By performing measurements with the voltage loop open, the 120-Hz ripple from the voltage loop does not enter the current loop. For the

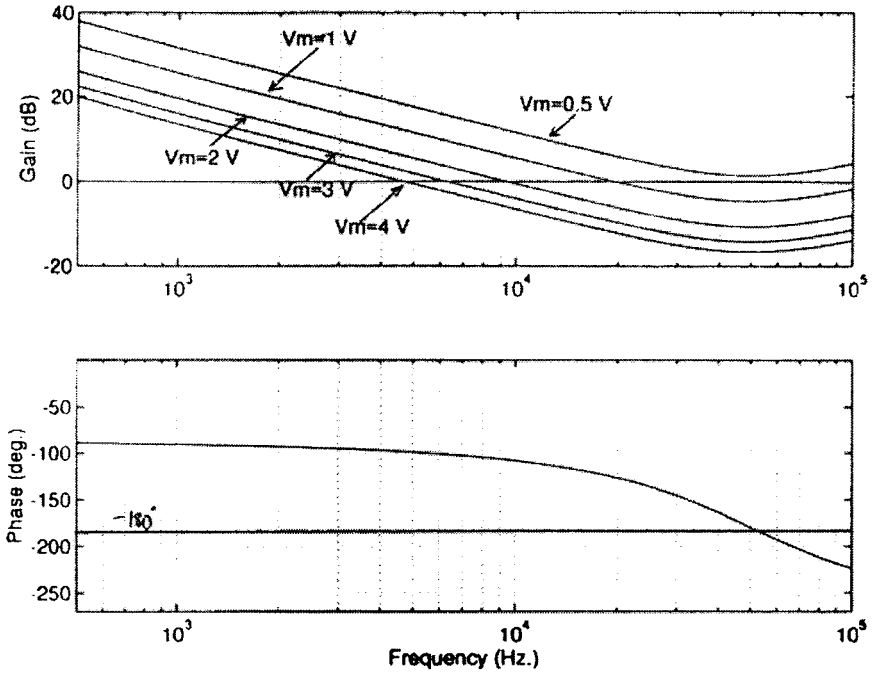


(a)

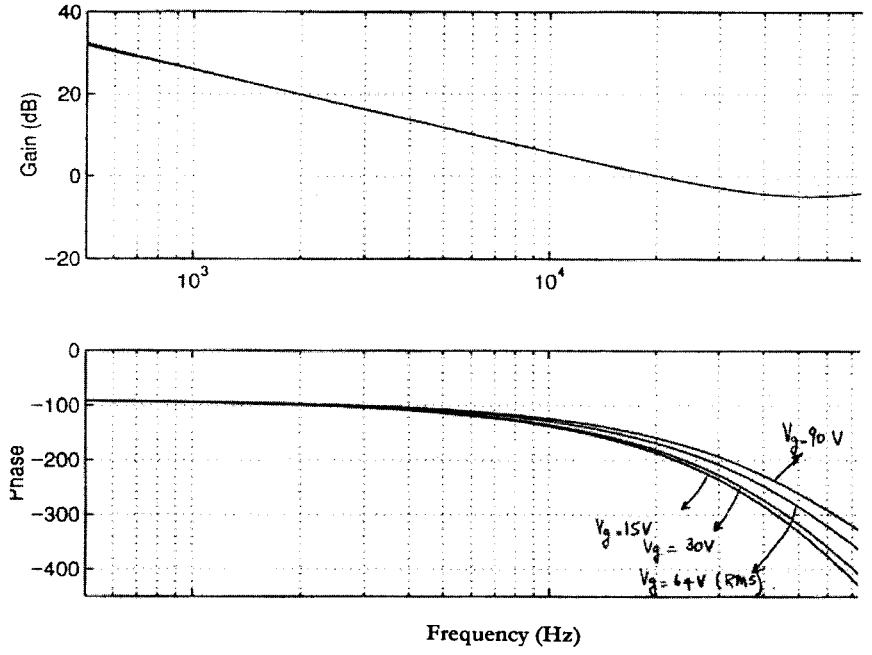


(b)

Fig. 14. (a) Current loop gain prototype measurement and theoretical predictions: $V_{\rm in} = 90$ V (rms), $V_o = 181$ V, $I_{\rm load} = 0.44$ A, $V_m = 2.005$ V, and $T_s = 9.5$ μs and (b) current loop gain prototype measurement and theoretical predictions: $V_{\rm in} = 90$ V (rms), $V_o = 181$ V, $I_{\rm load} = 0.62$ A, $V_m = 3$ V, and $T_s = 9.5$ μs.



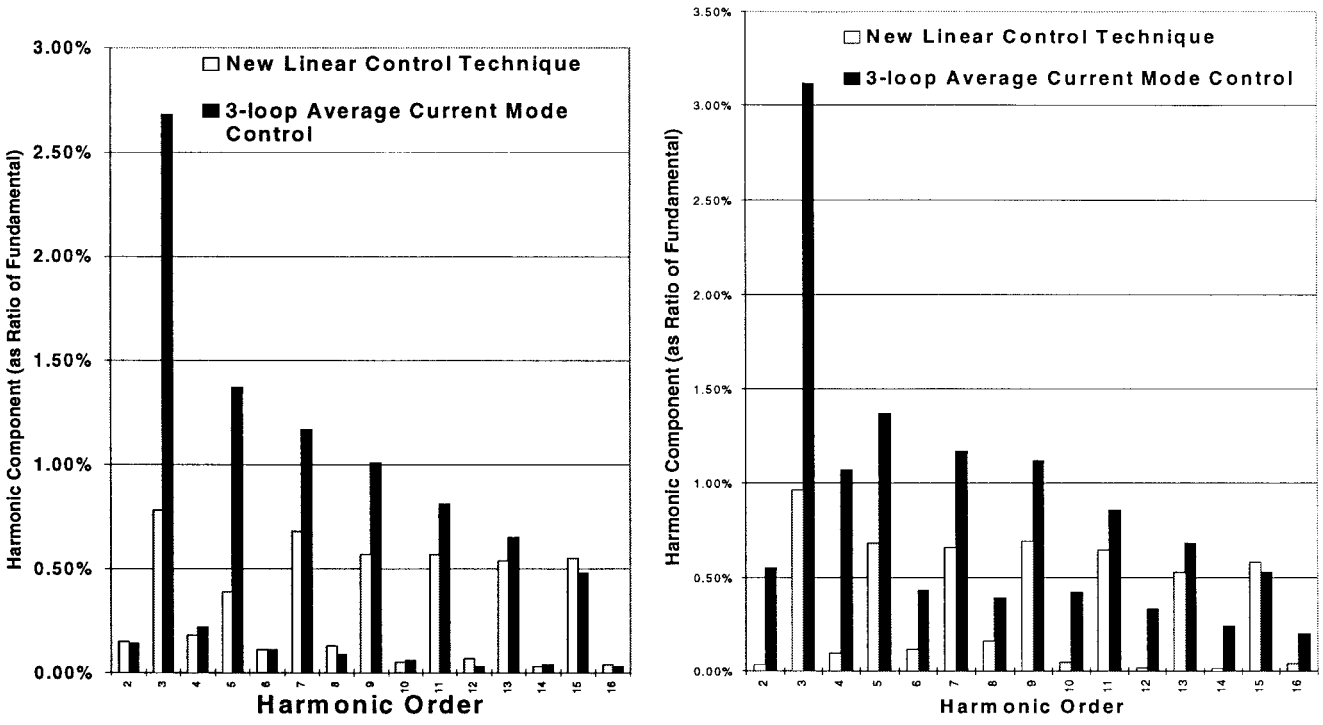
(a)



(b)

Fig. 15. (a) Variation of current loop gain of boost PFC with load of the proposed control scheme. (b) Variation of current loop gain with line voltage for a boost PFC.

three-loop-controlled PFC, the feedforward path was opened to avoid a source of distortion [13]. Fig. 16(a) shows the harmonic components in input current using the two control schemes using a high-quality sine-wave voltage generated using a high-power linear amplifier-based voltage source. The current loops in either control scheme had almost identical crossover frequencies; it is seen that the harmonics in the new control scheme had less lower order harmonics. A reason is that the new pulsewidth modulator has a significantly higher linearity than the multiplier–divider–squarer circuit. Integrated circuit multipliers have an inherent nonlinearity error. An IC multiplier produces an output $Y = K.A.B$. The variation in K with the signal ranges of A and B is termed nonlinearity error. Dividers are designed using a multiplier in the feedback path on an opamp and consequently have a nonlinearity error. A squarer may be implemented using a multiplier. Alternatively squarers can be designed with a smaller transistor count than a multiplier if the inputs are current signals rather than voltage



(a) (b)

Fig. 16. (a) Input current harmonics of new control scheme and conventional three-loop control scheme; voltage loop for both schemes and feedforward loop for the three-loop control are open. (b) Input current harmonics of new control scheme and conventional three-loop control scheme; voltage loop closed and feedforward loop for the three-loop control are open.

signals. Depending on the implementation there is a different nonlinearity error involved. It is possible to implement with a smaller linearity error a linear PWM ramp signal.

The harmonics in input current with voltage loop closed are shown in Fig. 16(b). It is shown that the overall harmonic performance of this new scheme is better than the conventional three-loop control scheme.

Equations (4b) and (4c) are possible solutions of PWM waveforms that provide PFC for a boost topology. In [3], (4b) was the resultant "nonlinear" PWM waveform for PFC. A disadvantage of this nonlinear waveform is the change in slope depending on $D > 0.5$ or < 0.5 and its implications on small-signal stability. PFC control laws based on (4c) are also nonlinear waveforms and have additional current sensing requirements.

V. Modeling for Voltage-Loop Design

The model of the power stage with the current loop closed is required for design of the voltage loop. The approach to model and design as presented in [12] is adopted for this control scheme. The important steps toward the derivation of the small-signal model are as follows. The control law governing input current is

$$\langle i_{\rm in}\rangle . R_i . g_m . \frac{T_s}{C_C} = V_m . (1 - D). \tag{17}$$

Based on power balance in every 120-Hz time scale

$$V_{\rm in}^{\rm rms} . i_{\rm in}^{\rm rms} = V_O . I_O. \tag{18}$$

Substituting (17) in (18)

$$i_{\rm in}^{\rm rms} = V_m . \frac{V_{\rm in}^{\rm rms}}{V_o . R_i . g_m . T_s / C_C}. \tag{19}$$

Perturbation and linearization of (19) gives the small-signal model equations

$$\hat{i}_o = \frac{(V_{\rm in}^{\rm rms})^2}{R_i . g_m . T_s / C_c . V_O^2} . \hat{v}_m + \frac{2 . (V_{\rm in}^{\rm rms}) . V_m}{R_i . g_m . T_s / C_c . V_O^2} . \hat{v}_{\rm in} - \frac{2 . I_o}{V_o} . \hat{v}_o \tag{20}$$

$$\hat{i}_{\rm in} = \frac{V_C}{R_i . g_m . T_s / C_c . V_O} . \hat{v}_{\rm in} + \frac{(V_{\rm in}^{\rm rms})}{R_i . g_m . T_s / C_c . V_O} . \hat{v}_m - \frac{I_{\rm in}^{\rm rms}}{V_o} . \hat{v}_o. \tag{21}$$

It is important to note that from the above (20) that the output resistance $\hat{v}_o / \hat{i}_o$ is $V_o / 2 . I_o$, half the value of conventional three-loop control for the same topology. A similar result has been reported in [5]. This helps is providing better regulation, with a nonintegral voltage loop. The voltage loop can be designed in a straightforward manner as done with conventional three-loop control. The voltage-loop model as expressed by (20) and (21) has been verified experimentally.

VI. Conclusion

This work presents a general and unified technique for derivation of ACMC laws to achieve high power factor. Using this methodology average CMC laws which provide high

power factor without the need for input voltage sensing are discovered. Small-signal models for the current and voltage loop which aid feedback design are presented. Hardware results for a boost PFC and simulation results for flyback buck+boost verify operation.

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