



An Assignment on

Hexadecimal to Seven-Segment Displays on the Nexys2 Board Using Verilog

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Objectives

The objectives of this assignment are the following:

- I. To become familiar with the seven-segment displays on the Nexys2 board.
- II. To design a circuit using decoders and multiplexers that drives the seven-segment displays on the Nexys2 board.
- III. To implement a 4-digit hex-to-7-segment decoder on the Nexys2 FPGA prototyping board.

What is a seven-segment LED?

A seven-segment LED is a digital display module that specializes in displaying numerical information. Digital light-emitting diodes (leds) provide an easy-to-see display. These are sometimes called "seven segment indicators" or "seven segment indicators".

Seven-segment displays are commonly used as alphanumeric displays in logic and computer systems. The seven-segment display consists of 7 leds (see below), which can be used to display any hexadecimal number between 0000 and 1111 by lighting combinations of these leds. For example, the red numbers on a digital clock use 2-segment LED displays. There are two types of 7-segment displays: common anode and common cathode. A standard 7-segment display has all the anodes connected together, while a standard 7-segment display has all the cathodes connected together.

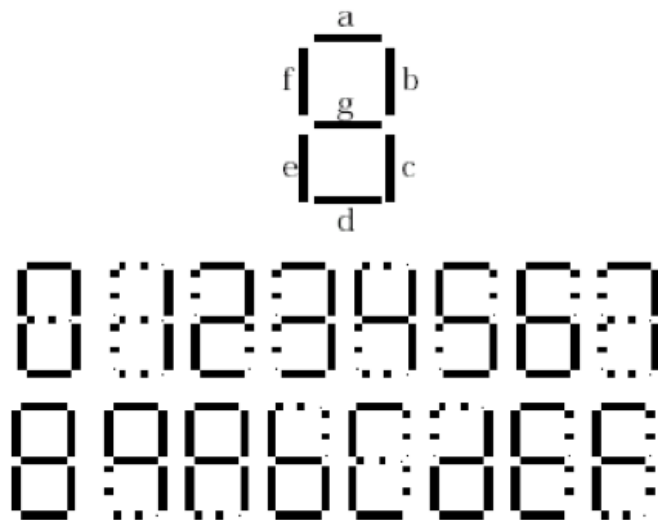


Fig: A 7-segment display contains seven light emitting diodes (LEDs)

Seven-Segment Displays on the Nexys2 Board

The Nexys2 board has four 7-segment displays. Each seven-segment display consists of seven LED bars and a single LED round (for the decimal point), as shown in the figure below. For more information, we can refer to the Digilent Nexys2 board manual.

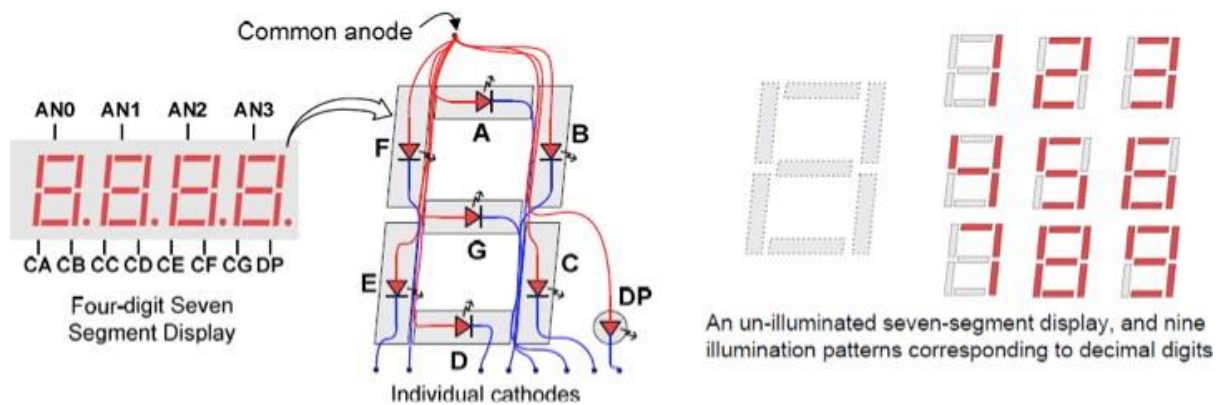


Fig-2: Nexys2 seven-segment displays

The Nexys2 board uses the common anode method in its displays. This means that all the anodes are interconnected and connected to 3.3 V via a pnp transistor as shown in Figure 7.3. A different FPGA output pin is connected to each cathode a - g plus decimal via a 100 Ω current limiting resistor. Control signal 0 turns on the LED segment and signal 1 turns it off. A hexadecimal-7-segment decoder takes a 4-bit input (a hexadecimal number) and creates a corresponding 8-bit pattern to illuminate the corresponding LED segments on the display.

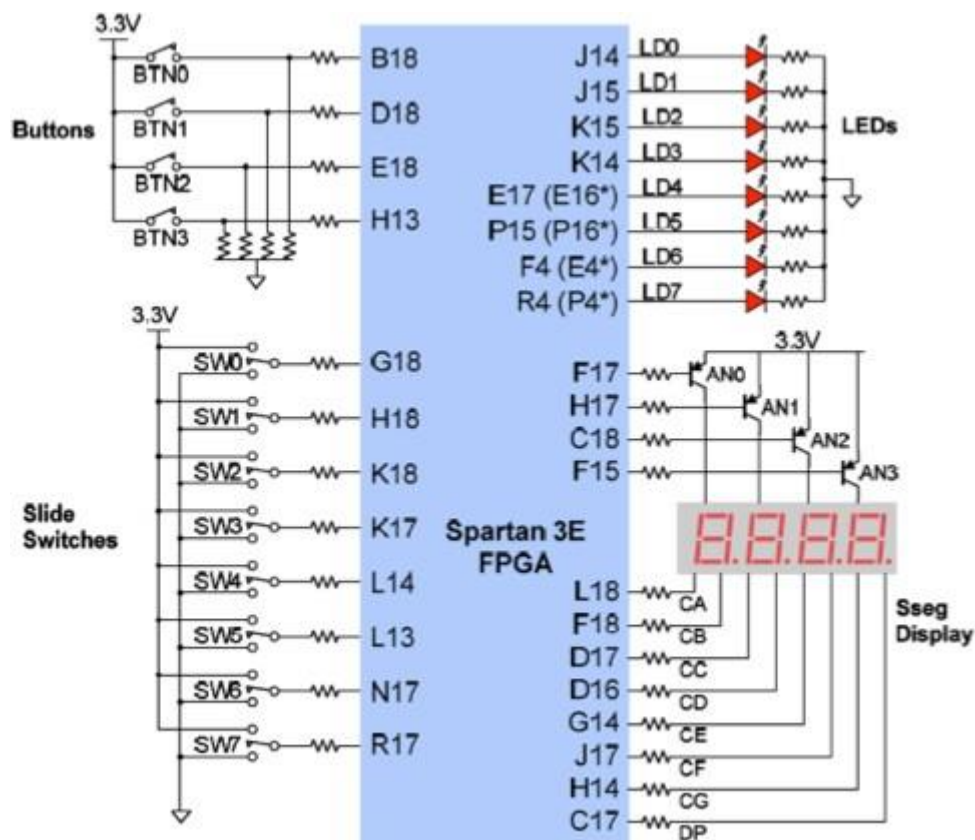


Fig-3: Nexys2 I/O devices and circuits

Multiplexing 4 Hex-to-7-Segment Displays

As described in the Nexys2 user manual, the Nexys2 board designers mapped the FPGA pins connecting the four seven-segment displays to the same control lines. The user can "simultaneously" display four different characters by high-speed time-division multiplexing the control lines of the seven-segment display.

enough speed for the human eye to see all four screens on and display the correct value. Each number illuminates only a quarter of the time, but since the eye cannot detect a darkening of a number until it lights up again, the number appears continuously illuminated. If you slow down the "refresh" to about 45 hertz, the screen will flicker. In order for all four digits to be bright and continuously lit, all four digits must be used at least once every 16 ms with a refresh rate of 60 Hz. In a 60 Hz refresh system, the entire display is refreshed every 16 ms, and each digit flashes for $\frac{1}{4}$ of the refresh period, or 4 ms. The controller must move the cathode in the correct pattern when the corresponding anode signal is moved. To illustrate the process, when AN0 is asserted, when CB and CC are asserted, "1" will be displayed in number 1 (left of the four screens). Then, when AN1 is asserted, when CA, CB and CC are asserted, number 2 will show "7". If AN0 with CB and CC is applied for 4ms and then A1 with CA, CB and CC is moved in sequence for 4ms, the display will show "17" with the first two digits. The figure below shows the timing diagram of a four digit controller.

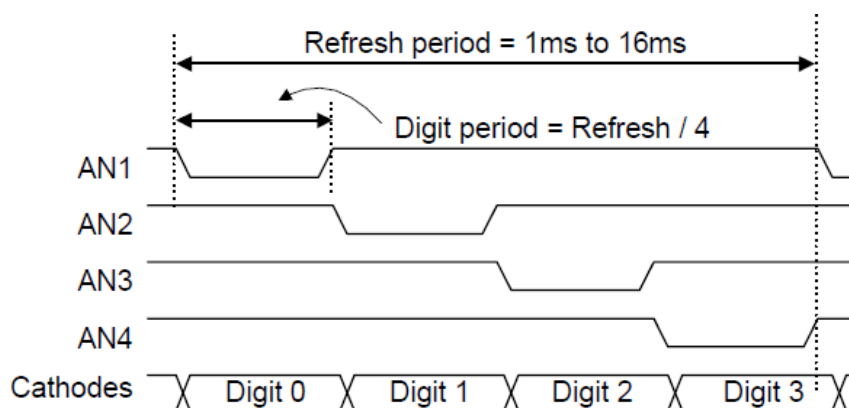


Fig-4: Seven-segment display timing diagram

Counters and Clock Dividers

A 4-digit seven-segment controller inputs a clock and four characters (4-bit each) and writes seven-segment control signals and four anode signals to display all four characters simultaneously. The figure below shows a block diagram of a possible implementation of this controller.

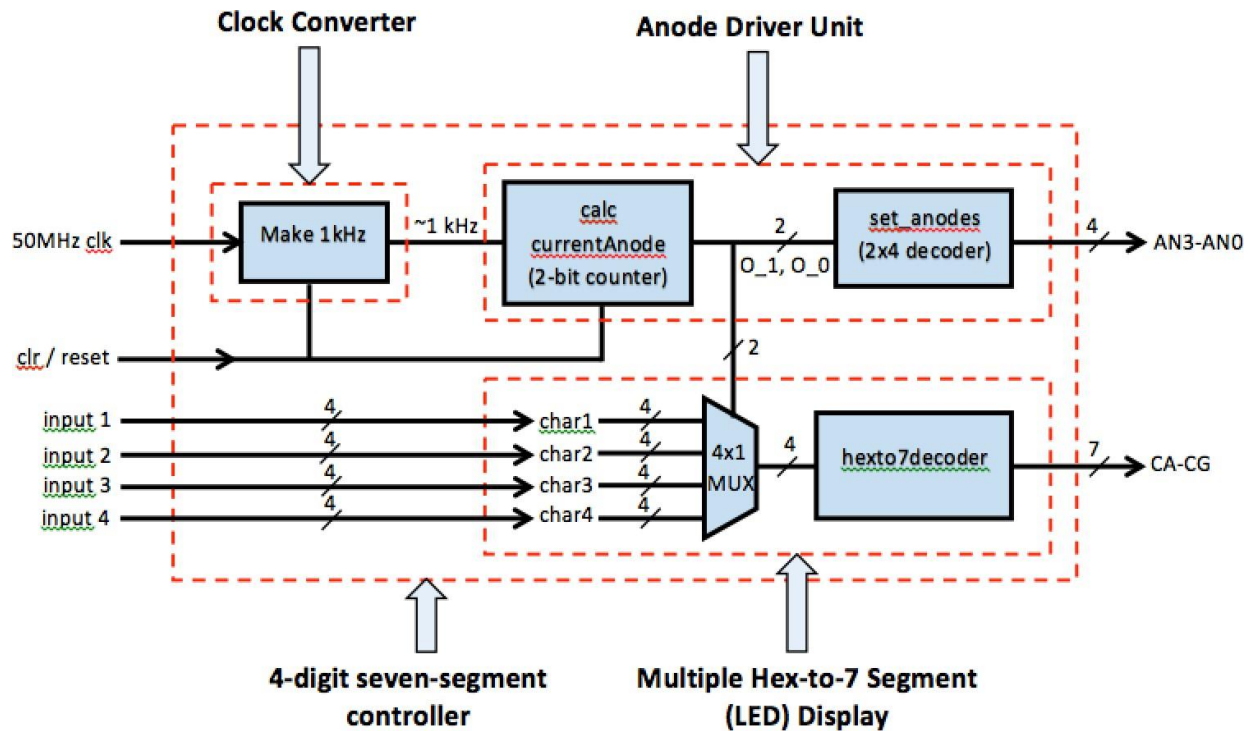


Fig-5: A block diagram of a possible implementation of the seg7_driver

Hex-to-7-Segment Decoder: Logic Equations

To display hexadecimal numbers on a 7-segment display, we need to build a hexadecimal decoder (called hex7seg) whose input is a 4-bit number ($x[3:0]$) and whose outputs are 7-segment values. - g from the truth table above. We can make a Karnaugh map for each segment and then develop logic equations for segments a - g. For example, the logical equation of segment e is:

$$e = \sim x[3] \& x[0] \mid \sim x[3] \& x[2] \& \sim x[1] \mid \sim x[2] \& \sim x[1] \& x[0]$$

We can similarly develop equations for the other six segments and then write the Verilog program for the 7-segment decoder.

VERILOG CODE DESIGN

```
module hexto7segment(
    input [3:0]x,
    output reg [6:0]z
);
always @*
case (x)
```

```

4'b0000    z = 7'b11111110;    //Hexadecimal 0
4'b0001    z = 7'b0110000;    //Hexadecimal 1
4'b0010    z = 7'b1101101 ;    // Hexadecimal 2
4'b0011    z = 7'b1111001 ;    // Hexadecimal 3
4'b0100    z = 7'b0110011 ;    // Hexadecimal 4
4'b0101    z = 7'b1011011 ;    // Hexadecimal 5
4'b0110    z = 7'b1011111;    // Hexadecimal 6
4'b0111    z = 7'b1110000;    // Hexadecimal 7
4'b1000    z = 7'b1111111;    //Hexadecimal 8
4'b1001    z = 7'b1111011;    //Hexadecimal 9
4'b1010    z = 7'b1110111;    // Hexadecimal A
4'b1011    z = 7'b0011111;    // Hexadecimal B
4'b1100    z = 7'b1001110;    // Hexadecimal C
4'b1101    z = 7'b0111101;    // Hexadecimal D
4'b1110    z = 7'b1001111;    // Hexadecimal E
4'b1111    z = 7'b1000111 ;    // Hexadecimal F
endcase

endmodule

```

Test Bench

```

`timescale 1ns / 1ps
module test_hexto7segment;
    // Inputs
    reg [3:0] x;
    // Outputs
    wire [6:0] z;
    // Instantiate the Unit Under Test (UUT)
    hexto7segment uut (
        .x(x),
        .z(z)
    );

    initial begin
        $dumpfile("dump.vcd");
        $dumpvars;
        // Initialize Inputs
        x = 0;
        #20 x = 1;
    end
endmodule

```

```

#20 x = 2;
#20 x = 3;
#20 x = 4;
#20 x = 5;
#20 x = 6;
#20 x = 7;
#20 x = 8;
#20 x = 9;
#20 x = 10;
#20 x = 11;
#20 x = 12;
#20 x = 13;
#20 x = 14;
#20 x = 15;
#40 $finish;
end

endmodule

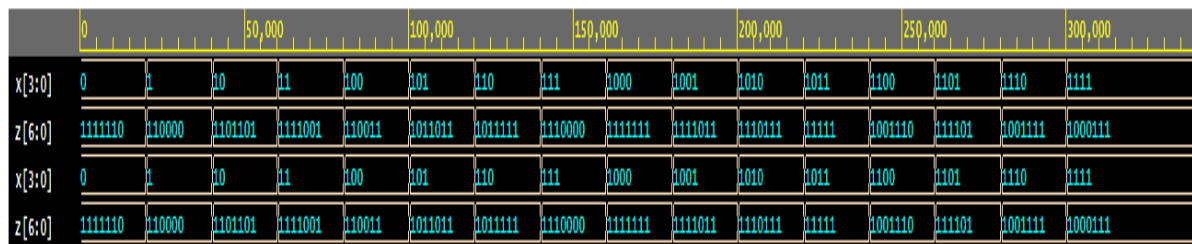
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OUTPUT:

The table below shows output cathode values for each segment a – g needed to display all hex values from 0 – F.

X	a	b	c	d	e	f	g
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1
A	1	1	1	0	1	1	1
B	0	0	1	1	1	1	1
C	1	0	0	1	1	1	0
D	0	1	1	1	1	0	1
E	1	0	0	1	1	1	1
F	1	0	0	0	1	1	1

WAVEFORM



CONCLUSION

Seven-segment displays are very commonly used in low-power electronic devices such as remote controls, watches, clocks, digital meters, etc. From the previous discussion, we can conclude that a seven-segment display consists of seven LEDs (Light Emitting Diode). segments lit up in a pattern to show the numbers 0-9. The seven-segment display is also used to display some key characters.

REFERENCES

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2. <https://www.rohm.com/electronics-basics/leds/seven-segment-led#:~:text=A%20seven%2Dsegment%20LED%20is,%22seven%2Dsegment%20indicators.%22>
3. <https://goldunicfirst.weebly.com/7-segment-display-using-common-anode-verilog.html>