FET3576-C Hardware Manual

Release 1.0

Forlinx Embedded Technology Co., Ltd

Jul 21, 2025

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PDF [1]

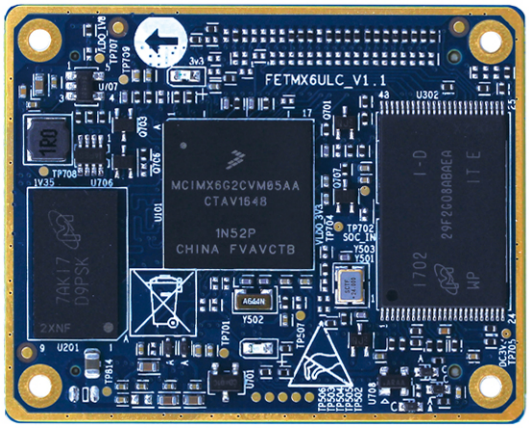
[1] https:docs.forlinx.net/_static/abc.pdf

CHAPTER

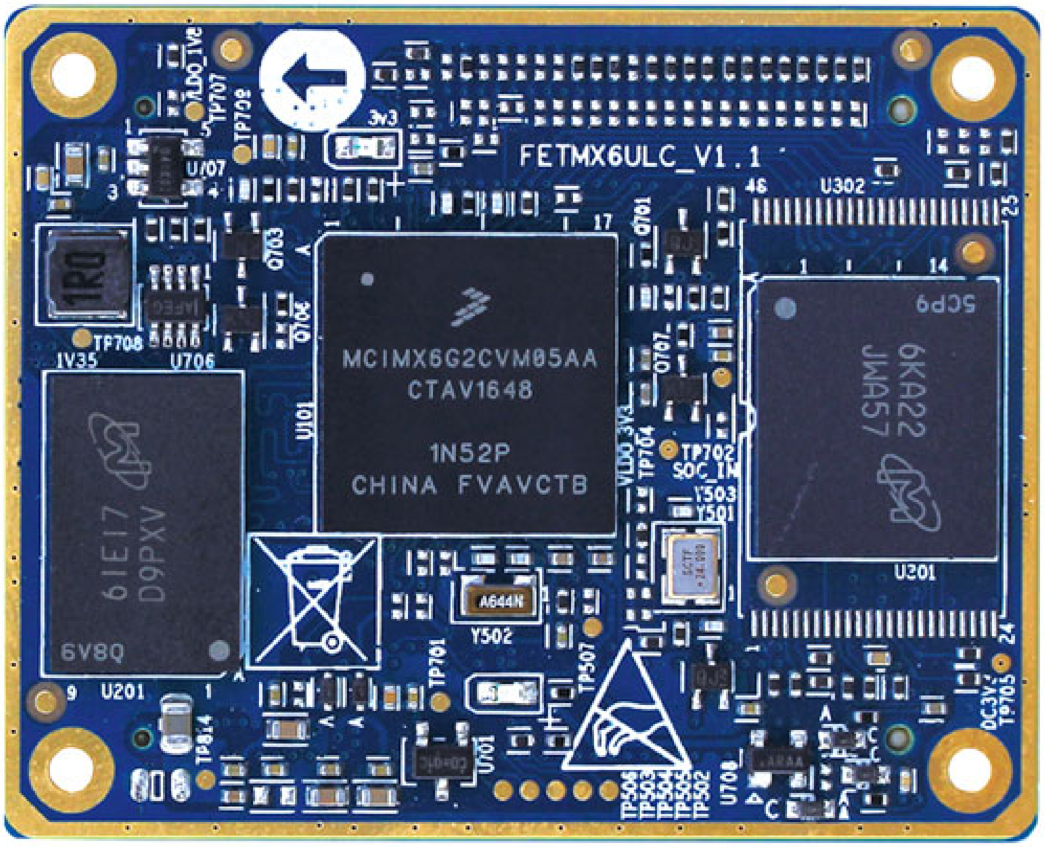
ONE

2.1 FETMX6UL-C

Nand Flash□□□



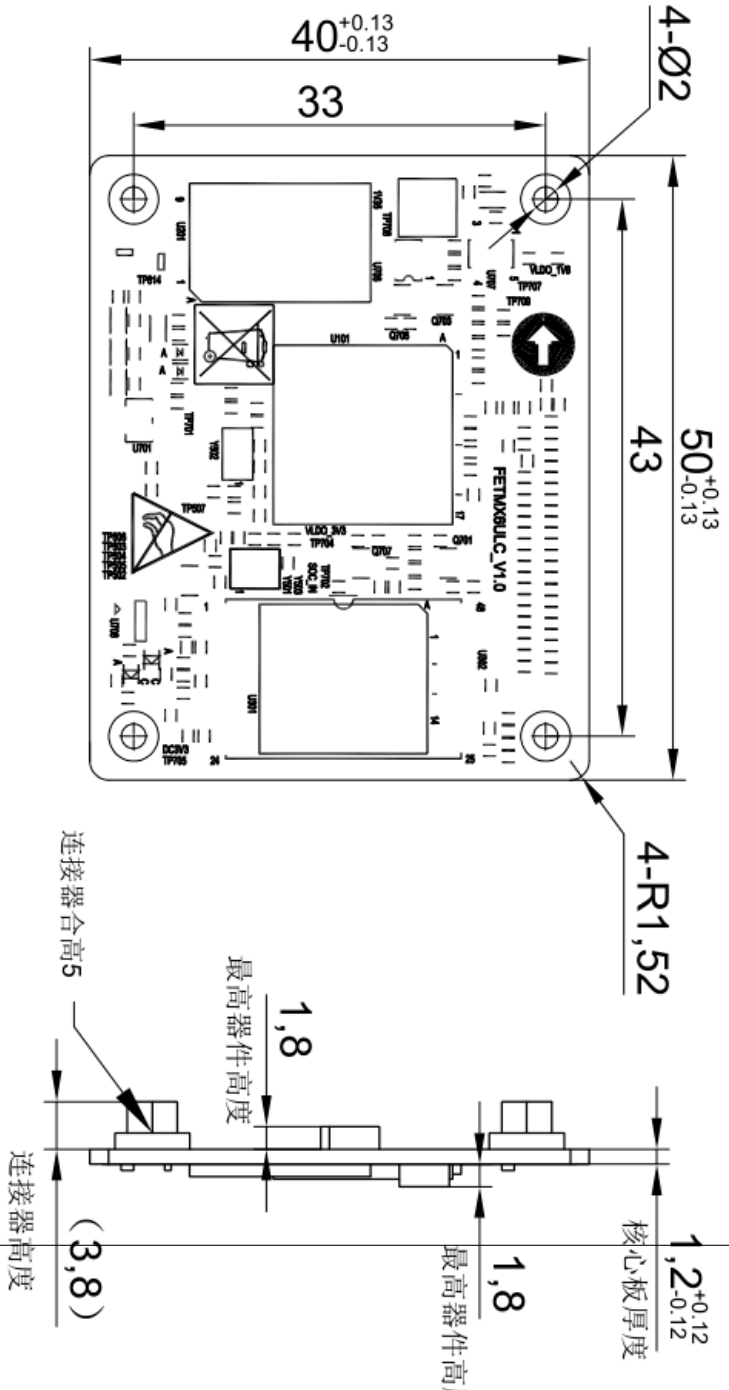
eMMC□□□


FETMX6ULC_V1.1
MCIMX6G2CVM05AA
CTAV1648
1N52P
CHINA FVAVCTB

CHAPTER

TWO

2.2 FETMX6UL-C



40mm×50mm ±0.15mm

1.15mm 6 PCB

0.8mm 80pin

M2*5mm* *M2*4mm

CHAPTER

THREE

2.3

2.3.1

	—	—	528	MHz	—
RTC	—	32.768	—	KHz	—

2.3.2

	VSYS	4.5	5	5.5	V	—
	—	63.1	—	85	mA	—
	—	113	—	160	mA	

2.3.3

	0	25	+70	℃
	-40	25	+125	℃
	-40	25	+85	℃
	-40	25	+125	℃
	10	—	90	RH
	5	—	95	RH

2.3.4

	—	115200	—	bps	—
SPI	—	—	52	MHz	—
IIC	—	100	400	Kbps	—
CAN	—	—	1	Mbps	—
SD/MMC/SDIO	—	—	104	Mbps	—
USB	—	—	480	Mbps	—
AD	0.7	—	1.25	us	Fadc=40 MHz

2.3.5 ESD

ESD HBM(ESDA/JEDEC JS-001-2017)	2000	V
ESD CDM(ESDA/JEDEC JS-002-2018)	500	V

CHAPTER

FOUR

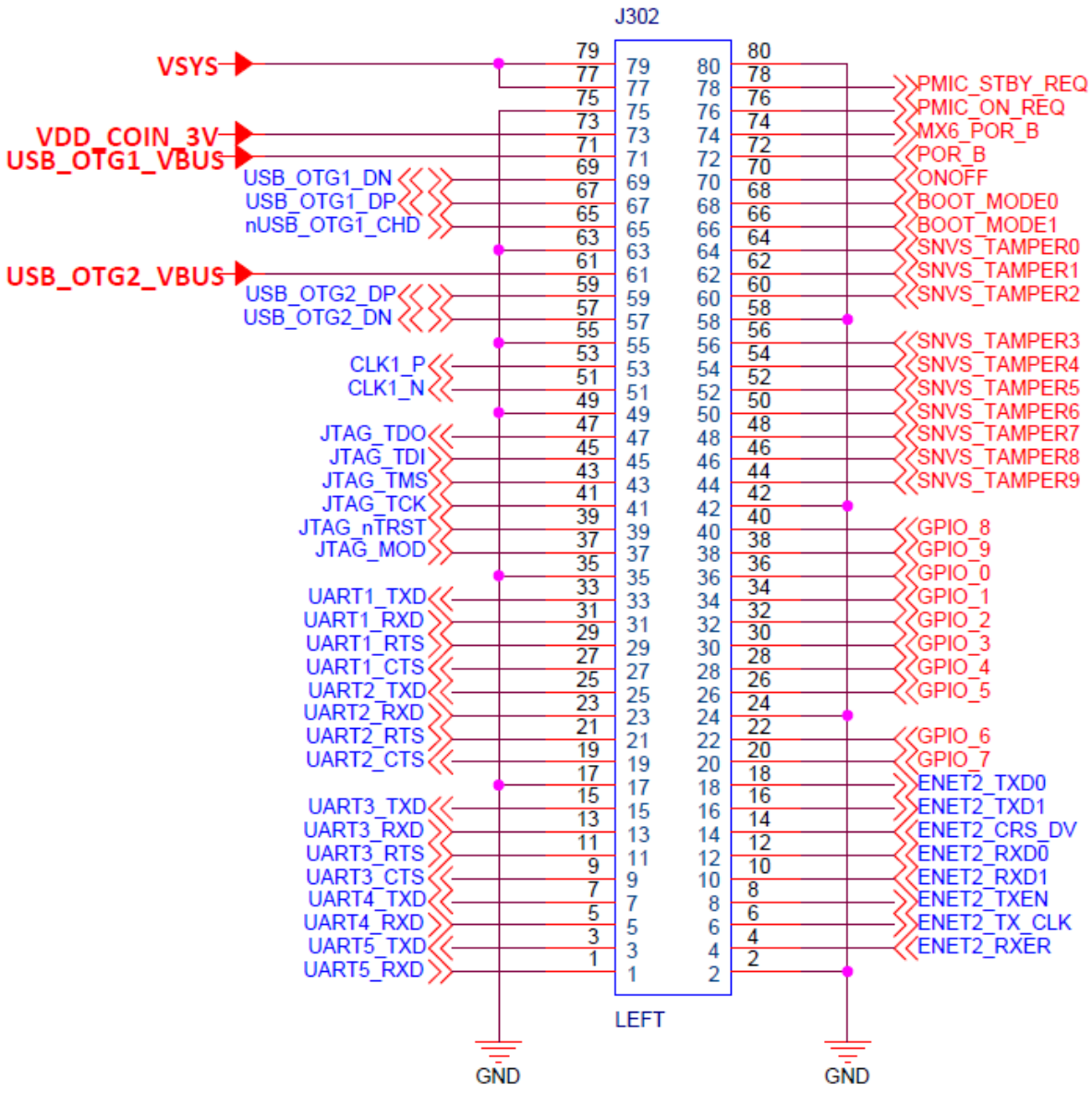
2.4

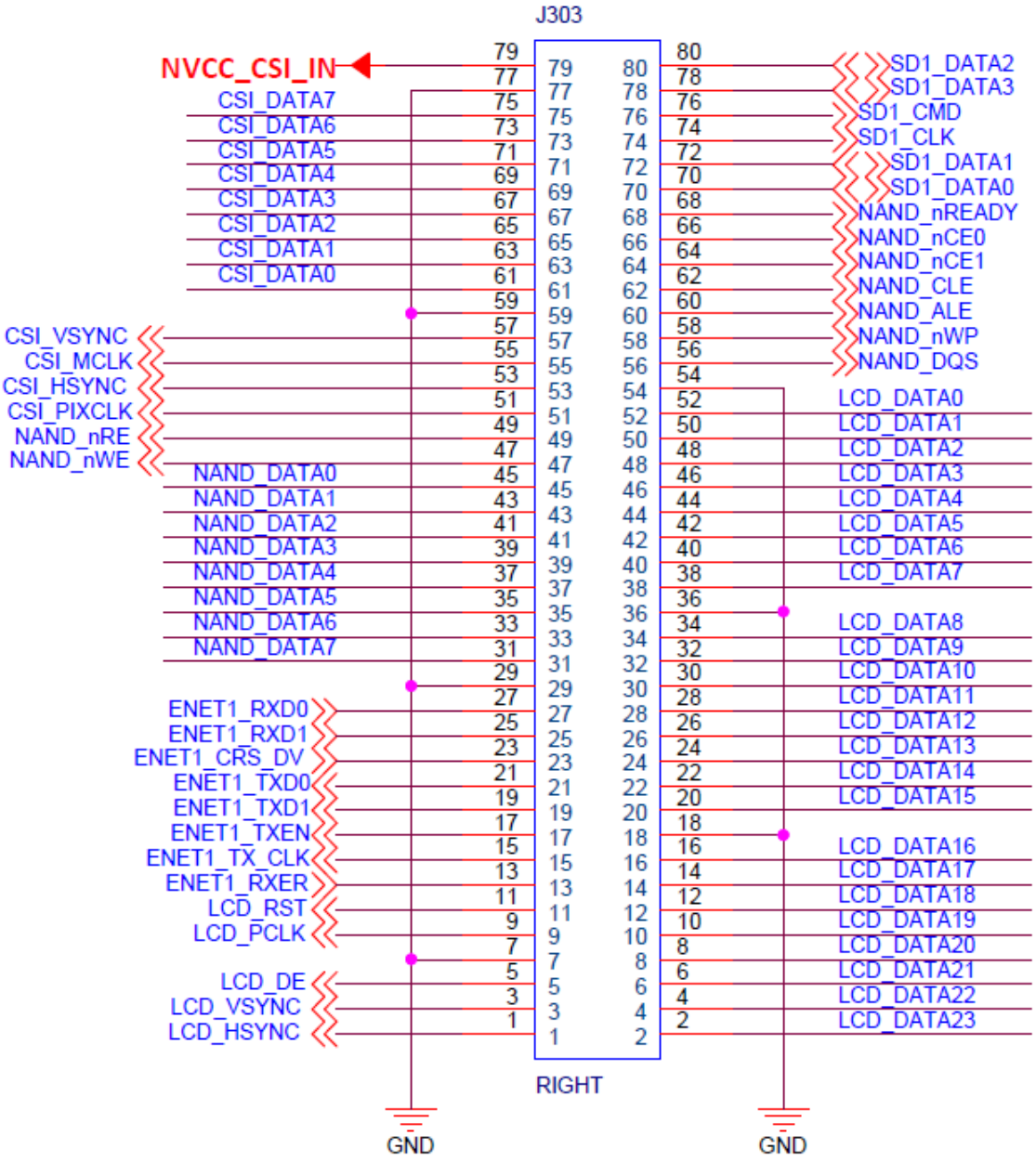
LCD	1	RGB888 24 WXGA (1366 x 768) (60 Hz
CAMERA	1	8 DVP 5-Megapixel
SD/MMC/SDIO	2	UHS-I SDR104 SD SDIO 1 4 104 MB/s
USB	2	USB 2.0 480 Mbps HS USB Phy
SAI	3	I2S Audio
SPDIF	1	
UART	8	5.0 Mbps
eCSPI	4	52 Mbit/s /
IIC	4	
Ethernet	2	10/100Mbps
PWM	8	16
JTAG		
KeyPad Port		8*8
QSPI	1	
CAN	2	CAN 2.0B
ADC	10	12 (ADC) 10
ISO7816-3	2	
EBI BUS	1	16

CPU

2.5 FETMX6UL-C

2.5.1 FETMX6UL-C





2.5.2 FETMX6UL- C

1

** Num —— **

** Ball —— **CPU

** GPIO —— **CPU I/O

** Vol ——**

2

** ——**

** ____**

** ____** “ ”

□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□

3: “ ” “ ”

1 LEFT J302

Num	Ball		GPIO	Vol		
L_1	G13	UART5_RXD	gpio1.IO[31]	3.3V	UART5	IIC2_SDA
L_3	F17	UART5_TXD	gpio1.IO[30]	3.3V	UART5	IIC2_SCL
L_5	G16	UART4_RXD	gpio1.IO[29]	3.3V	UART4	IIC1_SDA
L_7	G17	UART4_TXD	gpio1.IO[28]	3.3V	UART4	IIC1_SCL
L_9	H15	UART3_CTS	gpio1.IO[26]	3.3V	UART3	CAN1_TX
L_11	G14	UART3_RTS	gpio1.IO[27]	3.3V	UART3	CAN1_RX
L_13	H16	UART3_RXD	gpio1.IO[25]	3.3V	UART3	UART3_RXD
L_15	H17	UART3_TXD	gpio1.IO[24]	3.3V	UART3	UART3_TXD
L_17	—	GND	—	—		GND
L_19	J15	UART2_CTS	gpio1.IO[22]	3.3V	UART2	CAN2_TX
L_21	H14	UART2_RTS	gpio1.IO[23]	3.3V	UART2	CAN2_RX
L_23	J16	UART2_RXD	gpio1.IO[21]	3.3V	UART2	UART2_RXD
L_25	J17	UART2_TXD	gpio1.IO[20]	3.3V	UART2	UART2_TXD
L_27	K15	UART1_CTS	gpio1.IO[18]	3.3V	UART1	UART1_CTS
L_29	J14	UART1_RTS	gpio1.IO[19]	3.3V	UART1	UART1_RTSSD1_CD
L_31	K16	UART1_RXD	gpio1.IO[17]	3.3V	UART1	UART1_RXD
L_33	K14	UART1_TXD	gpio1.IO[16]	3.3V	UART1	UART1_TXD
L_35	—	GND	—	—		GND
L_37	P15	JTAG_MOD	gpio1.IO[10]	3.3V	JTAG	JTAG_MOD
L_39	N14	JTAG_nTRST	gpio1.IO[15]	3.3V	JTAG	JTAG_nTRSTSAI2_TXD
L_41	M14	JTAG_TCK	gpio1.IO[14]	3.3V	JTAG	JTAG_TCKSAI2_RXD
L_43	P14	JTAG_TMS	gpio1.IO[11]	3.3V	JTAG	JTAG_TMSSAI2_MCLK
L_45	N16	JTAG_TDI	gpio1.IO[13]	3.3V	JTAG	JTAG_TDISAI2_BCLK
L_47	N15	JTAG_TDO	gpio1.IO[12]	3.3V	JTAG	JTAG_TDOSAI_SYNC
L_49	—	GND	—	—		GND
L_51	P16	CLK1_N	—	—	—	CLK1_N
L_53	P17	CLK1_P	—	—	+	CLK1_P
L_55	—	GND	—	—		GND
L_57	T13	USB_OTG2_D—	—	—	USB —	USB_OTG2_D—
L_59	U13	USB_OTG2_D+	—	—	USB +	USB_OTG2_D+
L_61	U12	USB_OTG2_VBUS	—	—	USB	USB_OTG2_VBUS
L_63	—	GND	—	—		GND
L_65	U16	nUSB_OTG1_CHD	—	—	USB	USB_OTG1_CHD
L_67	U15	USB_OTG1_D+	—	—	USB OTG +	USB_OTG1_D+
L_69	T15	USB_OTG1_D-	—	—	USB OTG —	USB_OTG1_D—
L_71	T12	USB_OTG1_VBUS	—	—	USB OTG	USB_OTG1_VBUS
L_73	—	VDD_COIN_3V	—	—	RTC	BAT1
L_75	—	GND	—	—		GND
L_77	—	VSYS	—	5V	5V	VDD_5V
L_79	—	VSYS	—	5V	5V	VDD_5V

2 LEFT J302

Num	Ball		GPIO	Vol			
L_2	—	GND	—	—			GND
L_4	D16	ENET2_RXER	gpio2.IO[15]	3.3V	ENET2 RMII		ENET2_RXER
L_6	D17	ENET2_TX_CLK	gpio2.IO[14]	3.3V	ENET2 RMII		ENET2_TX_CL
L_8	B15	ENET2_TXEN	gpio2.IO[13]	3.3V	ENET2 RMII		ENET2_TXEN
L_10	C16	ENET2_RXD1	gpio2.IO[9]	3.3V	ENET2 RMII	1	ENET2_RXD1
L_12	C17	ENET2_RXD0	gpio2.IO[8]	3.3V	ENET2 RMII	0	ENET2_RXD0
L_14	B17	ENET2_CRS_DV	gpio2.IO[10]	3.3V	2		ENET2_CRS_D
L_16	A16	ENET2_TXD1	gpio2.IO[12]	3.3V	ENET2 RMII	1	ENET2_TXD1
L_18	A15	ENET2_TXD0	gpio2.IO[11]	3.3V	ENET2 RMII	0	ENET2_TXD0
L_20	L16	GPIO_7	gpio1.IO[7]	3.3V	I/O		ENET2_MDC
L_22	K17	GPIO_6	gpio1.IO[6]	3.3V	I/O		ENET2_MDIO
L_24	—	GND	—	—			GND
L_26	M17	GPIO_5	gpio1.IO[5]	3.3V	I/O **	**	GPIO_5
L_28	M16	GPIO_4	gpio1.IO[4]	3.3V	I/O		GPIO_4
L_30	L17	GPIO_3	gpio1.IO[3]	3.3V	I/O		GPIO_3
L_32	L14	GPIO_2	gpio1.IO[2]	3.3V	I/O		GPIO_2
L_34	L15	GPIO_1	gpio1.IO[1]	3.3V	I/O		GPIO_1
L_36	K13	GPIO_0	gpio1.IO[0]	3.3V	I/O		USB_OTG1_ID
L_38	M15	GPIO_9	gpio1.IO[9]	3.3V	I/O		LED3SD1_NRS
L_40	N17	GPIO_8	gpio1.IO[8]	3.3V	I/O		BLT_PWM
L_42	—	GND	—	—			GND
L_44	R6	SNVS_TAMPER9	gpio5.IO[9]	3.3V	SNVS TAMPER	9	LED2LCD_DIS
L_46	N9	SNVS_TAMPER8	gpio5.IO[8]	3.3V	SNVS TAMPER	8	SHIFT_NOE
L_48	N10	SNVS_TAMPER7	gpio5.IO[7]	3.3V	SNVS TAMPER	7	SHIFT_STCP
L_50	N11	SNVS_TAMPER6	gpio5.IO[6]	3.3V	SNVS TAMPER	6	ENET2_NINT
L_52	N8	SNVS_TAMPER5	gpio5.IO[5]	3.3V	SNVS TAMPER	5	ENET1_NINT
L_54	P9	SNVS_TAMPER4	gpio5.IO[4]	3.3V	SNVS TAMPER	4	AUD_INT
L_56	P10	SNVS_TAMPER3	gpio5.IO[3]	3.3V	SNVS TAMPER	3	SNVS_TAMPE
L_58	—	GND		3.3V			GND
L_60	P11	SNVS_TAMPER2	gpio5.IO[2]	3.3V	SNVS TAMPER	2	PERI_PWREN
L_62	R9	SNVS_TAMPER1	gpio5.IO[1]	3.3V	SNVS TAMPER	1	TP_INT
L_64	R10	SNVS_TAMPER0	gpio5.IO[0]	3.3V	SNVS TAMPER	0	ACC_INT
L_66	U10	BOOT_MODE1	gpio5.IO[11]	3.3V	1		SHIFT_SHCPB
L_68	T10	BOOT_MODE0	gpio5.IO[10]	3.3V	1		SHIFT_SDIBO
L_70	R8	ONOFF	—	—			ONOFF
L_72	P8	POR_B	—	—	i.MX6UL		POR_B
L_74	—	MX6_POR_B	—	—			MX6_POR_B
L_76	T9	PMIC_ON_REQ	—	—	GEN_5V	GEN_3.3V	PMIC_ON_RE
L_78	U9	PMIC_STBY_REQ	—	—	PMIC Standby	VDD_SOC_IN	PMIC_STBY_
L_80	—	GND	—	—			GND

3 RIGHT J303

Num	Ball		GPIO	Vol		
R_1	D9	LCD_HSYNC	gpio3.IO[2]	3.3V	RGB	LCD_HSYNC
R_3	C9	LCD_VSYNC	gpio3.IO[3]	3.3V	RGB	LCD_VSYNC
R_5	B8	LCD_DE	gpio3.IO[1]	3.3V	RGB	LCD_DE
R_7	—	GND	—	0V		GND
R_9	A8	LCD_PCLK	gpio3.IO[0]	3.3V	RGB	LCD_PCLK

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Table 3 – continued from previous page

Num	Ball		GPIO	Vol				
R_11	E9	LCD_RST	gpio3.IO[4]	3.3V	RGB			LCD_RST
R_13	D15	ENET1_RXER	gpio2.IO[7]	3.3V	ENET1 RMII			ENET1_RXER
R_15	F14	ENET1_TX_CLK	gpio2.IO[6]	3.3V	ENET1 RMII			ENET1_TX_CLK
R_17	F15	ENET1_TXEN	gpio2.IO[5]	3.3V	ENET1 RMII			ENET1_TXEN
R_19	E14	ENET1_TXD1	gpio2.IO[4]	3.3V	ENET1 RMII	1		ENET1_TXD1
R_21	E15	ENET1_TXD0	gpio2.IO[3]	3.3V	ENET1 RMII	0		ENET1_TXD0
R_23	E16	ENET1_CRS_DV	gpio2.IO[2]	3.3V	ENET1 RMII	RX_EN CRS		ENET1_CRS_DV
R_25	E17	ENET1_RXD1	gpio2.IO[1]	3.3V	ENET1 RMII	1		ENET1_RXD1
R_27	F16	ENET1_RXD0	gpio2. .IO[0]	3.3V	ENET1 RMII	0		ENET1_RXD0
R_29	—	GND	—	—				GND
R_31	A5	NAND_DATA7	gpio4.IO[9]	3.3V	NAND	7		NAND_DATA7
R_33	A6	NAND_DATA6	gpio4.IO[8]	3.3V	NAND	6		NAND_DATA6
R_35	B6	NAND_DATA5	gpio4.IO[7]	3.3V	NAND	5		NAND_DATA5
R_37	C6	NAND_DATA4	gpio4.IO[6]	3.3V	NAND	4		NAND_DATA4
R_39	D6	NAND_DATA3	gpio4.IO[5]	3.3V	NAND	3		NAND_DATA3
R_41	A7	NAND_DATA2	gpio4.IO[4]	3.3V	NAND	2		NAND_DATA2
R_43	B7	NAND_DATA1	gpio4.IO[3]	3.3V	NAND	1		NAND_DATA1
R_45	D7	NAND_DATA0	gpio4.IO[2]	3.3V	NAND	0		NAND_DATA0
R_47	C8	NAND_nWE	gpio4.IO[1]	3.3V	NAND			NAND_nWE
R_49	D8	NAND_nRE	gpio4.IO[0]	3.3V	NAND			NAND_nRE
R_51	E5	CSI_PIXCLK	gpio4.IO[18]	3.3V				CSI_PIXCLK
R_53	F3	CSI_HSYNC	gpio4.IO[20]	3.3V				CSI_HSYNC
R_55	F5	CSI_MCLK	gpio4.IO[17]	2.7V				CSI_MCLK
R_57	F2	CSI_VSYNC	gpio4.IO[19]	2.7V				CSI_VSYNC
R_59	—	GND	—	—				GND
R_61	E4	CSI_DAT0	gpio4.IO[21]	2.7V	8bit	0		CSI_DAT0
R_63	E3	CSI_DAT1	gpio4.IO[22]	2.7V	8bit	1		CSI_DAT1
R_65	E2	CSI_DAT2	gpio4.IO[23]	2.7V	8bit	2		CSI_DAT2
R_67	E1	CSI_DAT3	gpio4.IO[24]	2.7V	8bit	3		CSI_DAT3
R_69	D4	CSI_DAT4	gpio4.IO[25]	2.7V	8bit	4		CSI_DAT4
R_71	D3	CSI_DAT5	gpio4.IO[26]	2.7V	8bit	5		CSI_DAT5
R_73	D2	CSI_DAT6	gpio4.IO[27]	2.7V	8bit	6		CSI_DAT6
R_75	D1	CSI_DAT7	gpio4.IO[28]	2.7V	8bit	7		CSI_DAT7
R_77	—	GND	—	—				GND
R_79	—	NVCC_CSI_IN	—	—	CPU			NVCC_CSI_IN

4 RIGHT J303

Num	Ball		GPIO	Vol			
R_2	B16	LCD_DATA23	gpio3.IO[28]	3.3V	7		LCD_DATA23
R_4	A14	LCD_DATA22	gpio3.IO[27]	3.3V	6		LCD_DATA22
R_6	B14	LCD_DATA21	gpio3.IO[26]	3.3V	5		LCD_DATA21
R_8	C14	LCD_DATA20	gpio3.IO[25]	3.3V	4		LCD_DATA20
R_10	D14	LCD_DATA19	gpio3.IO[24]	3.3V	3		LCD_DATA19
R_12	A13	LCD_DATA18	gpio3.IO[23]	3.3V	2		LCD_DATA18
R_14	B13	LCD_DATA17	gpio3.IO[22]	3.3V	1		LCD_DATA17
R_16	C13	LCD_DATA16	gpio3.IO[21]	3.3V	0		LCD_DATA16
R_18	—	GND	—	0V			GND
R_20	D13	LCD_DATA15	gpio2.IO[4]	3.3V	7		LCD_DATA15

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Table 4 – continued from previous page

Num	Ball		GPIO	Vol			
R_22	A12	LCD_DATA14	gpio3.IO[19]	3.3V	6		LCD_DATA14
R_24	B12	LCD_DATA13	gpio3.IO[18]	3.3V	5		LCD_DATA13
R_26	C12	LCD_DATA12	gpio3.IO[17]	3.3V	4		LCD_DATA12
R_28	D12	LCD_DATA11	gpio3.IO[16]	3.3V	3		LCD_DATA11
R_30	E12	LCD_DATA10	gpio3.IO[15]	3.3V	2		LCD_DATA10
R_32	A11	LCD_DATA9	gpio3.IO[14]	3.3V	1		LCD_DATA9
R_34	B11	LCD_DATA8	gpio3.IO[13]	3.3V	0		LCD_DATA8
R_36	—	GND	—	—			GND
R_38	D11	LCD_DATA7	gpio3.IO[12]	3.3V	7( )		LCD_DATA7
R_40	A10	LCD_DATA6	gpio3.IO[11]	3.3V	6		LCD_DATA6
R_42	B10	LCD_DATA5	gpio3.IO[10]	3.3V	5		LCD_DATA5
R_44	C10	LCD_DATA4	gpio3.IO[9]	3.3V	4		LCD_DATA4
R_46	D10	LCD_DATA3	gpio3.IO[8]	3.3V	3		LCD_DATA3
R_48	E10	LCD_DATA2	gpio3.IO[7]	3.3V	2		LCD_DATA2
R_50	A9	LCD_DATA1	gpio3.IO[6]	3.3V	1		LCD_DATA1
R_52	B9	LCD_DATA0	gpio3.IO[5]	3.3V	0		LCD_DATA0
R_54	—	GND	—	—			GND
R_56	E6	NAND_DQS	gpio4.IO[16]	3.3V	NAND		NAND_DQS
R_58	D5	NAND_nWP	gpio4.IO[11]	3.3V	NAND	**Nand**	NAND_nWP
R_60	B4	NAND_ALE	gpio4.IO[10]	3.3V	NAND	**Nand**	NAND_ALE
R_62	A4	NAND_CLE	gpio4.IO[15]	3.3V	NAND	**Nand**	NAND_CLE
R_64	B5	NAND_nCE1	gpio4.IO[14]	3.3V	NAND	1	NAND_nCE1
R_66	C5	NAND_nCE0	gpio4.IO[13]	3.3V	NAND	0 **Nand**	NAND_nCE0
R_68	A3	NAND_nREADY	gpio4.IO[12]	3.3V	NAND	**Nand**	NAND_nREADY
R_70	B3	SD1_DATA0	gpio2.IO[18]	3.3V	SD/MMC1	0	SD1_DATA0
R_72	B2	SD1_DATA1	gpio2.IO[19]	3.3V	SD/MMC1	1	SD1_DATA1
R_74	C1	SD1_CLK	gpio2.IO[17]	3.3V	SD/MMC1		SD1_CLK
R_76	C2	SD1_CMD	gpio2.IO[16]	3.3V	SD/MMC1		SD1_CMD
R_78	A2	SD1_DATA3	gpio2.IO[21]	3.3V	SD/MMC1	3	SD1_DATA3
R_80	B1	SD1_DATA2	gpio2.IO[20]	3.3V	SD/MMC1	2	SD1_DATA2

CHAPTER

SIX

2.6

FETMX6UL-C , 5V , :

3.5 “OKMX6UL-C ”