

Depletion and enhancement modes

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In field-effect transistors (FETs), **depletion mode** and **enhancement mode** are two major transistor types, corresponding to whether the transistor is in an *ON* state or an *OFF* state at zero gate–source voltage.

Enhancement-mode MOSFETs are the common switching elements in most MOS. These devices are off at zero gate–source voltage, and can be turned on by pulling the gate voltage either higher than the source voltage, for NMOS, or lower than the source voltage, for PMOS. In most circuits, this means pulling an enhancement-mode MOSFET's gate voltage towards its drain voltage turns it *ON*.

In a depletion-mode MOSFET, the device is normally *ON* at zero gate–source voltage. Such devices are used as load "resistors" in logic circuits (in depletion-load NMOS logic, for example). For N-type depletion-load devices, the threshold voltage might be about -3 V , so it could be turned off by pulling the gate 3 V negative (the drain, by comparison, is more positive than the source in NMOS). In PMOS, the polarities are reversed.

The mode can be determined by the sign of the threshold voltage (gate voltage relative to source voltage at the point where an inversion layer just forms in the channel): for an N-type FET, enhancement-mode devices have positive thresholds, and depletion-mode devices have negative thresholds; for a P-type FET, enhancement-mode negative, depletion-mode positive.^{[1][2]}

Junction field-effect transistors (JFETs) are depletion mode, since the gate junction would forward bias if the gate were taken more than a little from source toward drain voltage. Such devices are used in gallium-arsenide and germanium chips, where it is difficult to make an oxide insulator.

Alternative terminology

Some sources say "depletion type" and "enhancement type" for the device types as described in this article as "depletion mode" and "enhancement mode", and apply the "mode" terms for which direction the gate–source voltage differs from zero.^[3] Moving the gate voltage toward the drain voltage "enhances" the conduction in the channel, so this defines the enhancement mode of operation, while moving the gate away from the drain depletes the channel, so this defines depletion mode.

Enhancement-load and depletion-load logic families

Depletion-load NMOS logic refers to the logic family that became dominant in silicon VLSI in the latter half of the 1970s; the process supported both enhancement-mode and depletion-mode transistors, and typical logic circuits used enhancement-mode devices as pull-down switches and depletion-mode devices as loads, or pull-ups. Logic families built in older processes that did not support depletion-mode transistors were retrospectively referred to as *enhancement-load* logic, or as *saturated-load* logic, since the enhancement-mode transistors were typically connected with gate to the V_{DD} supply and operated in the saturation region (sometimes the gates are biased to a higher V_{GG} voltage and operated in the linear region, for a better power–delay product, but the loads then take more area).^[4] Alternatively, rather than static logic gates, dynamic logic such as four-phase logic was sometimes used in processes that did not have depletion-mode transistors available.

For example, the 1971 Intel 4004 used enhancement-load silicon-gate PMOS logic, and the 1976 Zilog Z80 used depletion-load silicon-gate NMOS.

References

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