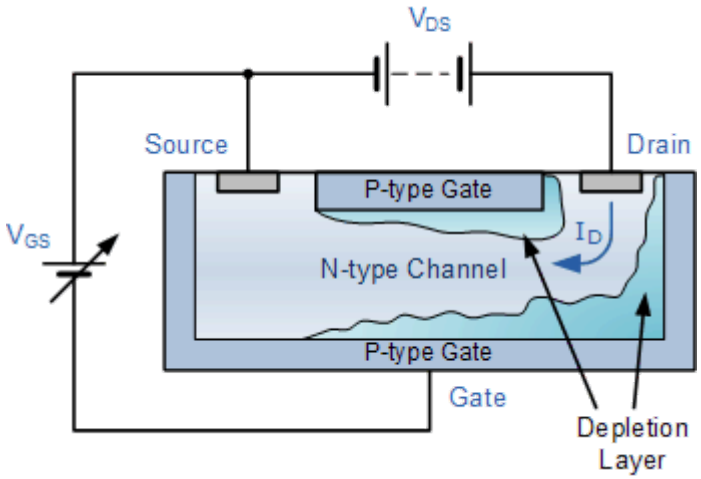


Junction Field Effect Transistor

The Field Effect Transistor

In the Bipolar Junction Transistor tutorials, we saw that the output Collector current of the transistor is proportional to input current flowing into the Base terminal of the device, thereby making the bipolar transistor a "CURRENT" operated device (Beta model) as a smaller current can be used to switch a larger load current.

The **Field Effect Transistor**, or simply **FET** however, uses the voltage that is applied to their input terminal, called the Gate to control the current flowing through them resulting in the output current being proportional to the input voltage. As their operation relies on an electric field (hence the name field effect) generated by the input Gate voltage, this then makes the **Field Effect Transistor** a "VOLTAGE" operated device.

The **Field Effect Transistor** is a three terminal unipolar semiconductor device that has very similar characteristics to those of their *Bipolar Transistor* counterparts ie, high efficiency, instant operation, robust and cheap and can be used in most electronic circuit applications to replace their equivalent bipolar junction transistors (BJT) cousins.

Typical Field Effect Transistor

Field effect transistors can be made much smaller than an equivalent BJT transistor and along with their low power consumption and power dissipation makes them ideal for use in integrated circuits such as the CMOS range of digital logic chips.

We remember from the previous tutorials that there are two basic types of bipolar transistor construction, NPN and PNP, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made. This is also true of FET's as there are also two basic classifications of Field Effect Transistor, called the N-channel FET and the P-channel FET.

The field effect transistor is a three terminal device that is constructed with no PN-junctions within the main current carrying path between the Drain and the Source terminals, which correspond in function to the Collector and the Emitter respectively of the bipolar transistor. The current path between these two terminals is called the "channel" which may be made of either a P-type or an N-type semiconductor material.

Related Products: **RF MOSFET**

The control of current flowing in this channel is achieved by varying the voltage applied to the Gate. As their name implies, Bipolar Transistors are "Bipolar" devices because they operate with both types of charge carriers, Holes and Electrons. The Field Effect Transistor on the other hand is a "Unipolar" device that depends only on the conduction of electrons (N-channel) or holes (P-channel).

The **Field Effect Transistor** has one major advantage over its standard bipolar transistor cousins, in that their input impedance, (Rin) is very high, (thousands of Ohms), while the BJT is comparatively low. This very high input impedance makes them very sensitive to input voltage signals, but the price of this high sensitivity also means that they can be easily damaged by static electricity.

There are two main types of field effect transistor, the **Junction Field Effect Transistor** or **JFET** and the **Insulated-gate Field Effect Transistor** or **IGFET)**, which is more commonly known as the standard **Metal Oxide Semiconductor Field Effect Transistor** or **MOSFET** for short.

The Junction Field Effect Transistor

We saw previously that a bipolar junction transistor is constructed using two PN-junctions in the main current carrying path between the Emitter and the Collector terminals. The **Junction Field Effect Transistor** (JUGFET or JFET) has no PN-junctions but instead has a narrow piece of high resistivity semiconductor material forming a "Channel" of either N-type or P-type silicon for the majority carriers to flow through with two ohmic electrical connections at either end commonly called the Drain and the Source respectively.

There are two basic configurations of junction field effect transistor, the N-channel JFET and the P-channel JFET. The N-channel JFET's channel is doped with donor impurities meaning that the flow of current through the channel is negative (hence the term N-channel) in the form of electrons.

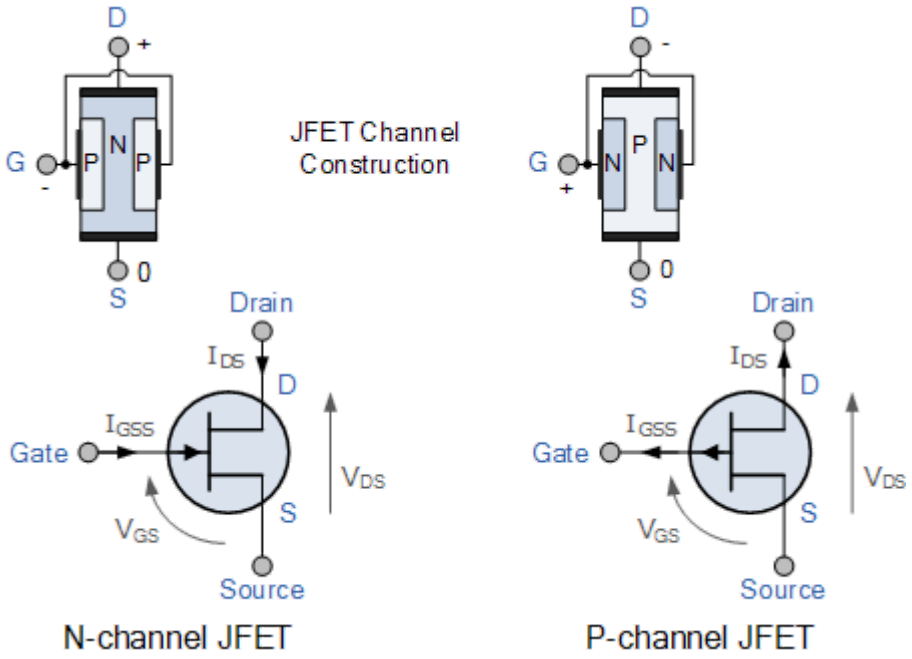
Likewise, the P-channel JFET's channel is doped with acceptor impurities meaning that the flow of current through the channel is positive (hence the term P-channel) in the form of holes. N-channel JFET's have a greater channel conductivity (lower resistance) than their equivalent P-channel types, since electrons have a higher mobility through a conductor compared to holes. This makes the N-channel JFET's a more efficient conductor compared to their P-channel counterparts.

We have said previously that there are two ohmic electrical connections at either end of the channel called the Drain and the Source. But within this channel there is a third electrical connection which is called the Gate terminal and this can also be a P-type or N-type material forming a PN-junction with the main channel. The relationship between the connections of a junction field effect transistor and a bipolar junction transistor are compared below.

Comparison of Connections between a JFET and a BJT

Bipolar Transistor	Field Effect Transistor
Emitter – (E)	>> Source – (S)
Base – (B)	>> Gate – (G)
Collector – (C)	>> Drain – (D)

The symbols and basic construction for both configurations of JFETs are shown below.

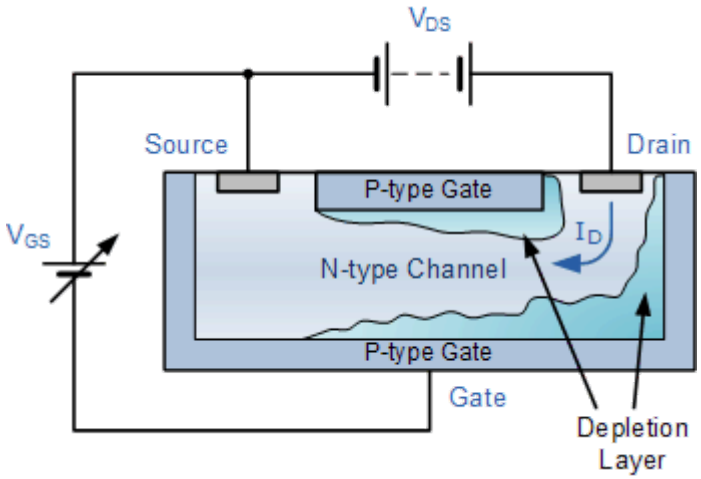


The semiconductor "channel" of the **Junction Field Effect Transistor** is a resistive path through which a voltage V_{DS} causes a current I_D to flow and as such the junction field effect transistor can conduct current equally well in either direction. As the channel is resistive in nature, a voltage gradient is thus formed down the length of the channel with this voltage becoming less positive as we go from the Drain terminal to the Source terminal.

The result is that the PN-junction therefore has a high reverse bias at the Drain terminal and a lower reverse bias at the Source terminal. This bias causes a "depletion layer" to be formed within the channel and whose width increases with the bias.

The magnitude of the current flowing through the channel between the Drain and the Source terminals is controlled by a voltage applied to the Gate terminal, which is a reverse-biased. In an N-channel JFET this Gate voltage is negative while for a P-channel JFET the Gate voltage is positive. The main difference between the JFET and a BJT device is that when the JFET junction is reverse-biased the Gate current is practically zero, whereas the Base current of the BJT is always some value greater than zero.

Biasing of an N-channel JFET



The cross sectional diagram above shows an N-type semiconductor channel with a P-type region called the Gate diffused into the N-type channel forming a reverse biased PN-junction and it is this junction which forms the *depletion region* around the Gate area when no external voltages are applied. JFETs are therefore known as depletion mode devices.

This depletion region produces a potential gradient which is of varying thickness around the PN-junction and restrict the current flow through the channel by reducing its effective width and thus increasing the overall resistance of the channel itself.

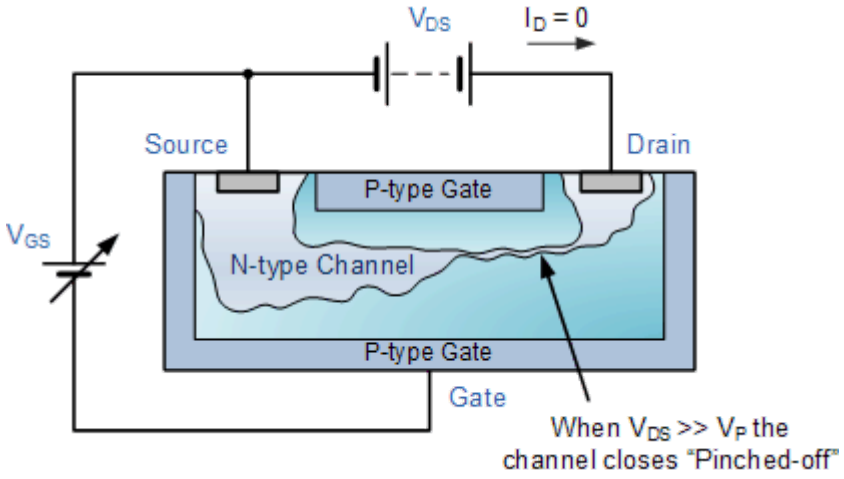
Then we can see that the most-depleted portion of the depletion region is in between the Gate and the Drain, while the least-depleted area is between the Gate and the Source. Then the JFET's channel conducts with zero bias voltage applied (ie, the depletion region has near zero width).

With no external Gate voltage ($V_G = 0$), and a small voltage (V_{DS}) applied between the Drain and the Source, maximum saturation current (I_{DSS}) will flow through the channel from the Drain to the Source restricted only by the small depletion region around the junctions.

If a small negative voltage ($-V_{GS}$) is now applied to the Gate the size of the depletion region begins to increase reducing the overall effective area of the channel and thus reducing the current flowing through it, a sort of "squeezing" effect takes place. So by applying a reverse bias voltage increases the width of the depletion region which in turn reduces the conduction of the channel.

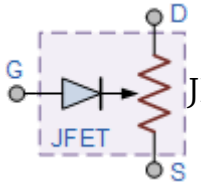
Since the PN-junction is reverse biased, little current will flow into the gate connection. As the Gate voltage ($-V_{GS}$) is made more negative, the width of the channel decreases until no more current flows between the Drain and the Source and the FET is said to be "pinched-off" (similar to the cut-off region for a BJT). The voltage at which the channel closes is called the "pinch-off voltage", (V_P).

JFET Channel Pinched-off



In this pinch-off region the Gate voltage, V_{GS} controls the channel current and V_{DS} has little or no effect.

The result is that the FET acts more like a voltage controlled resistor which has zero resistance when V_{GS} = 0 and maximum "ON" resistance (R_{DS}) when the Gate voltage is very negative. Under normal operating conditions, the JFET gate is always negatively biased relative to the source.



JFET Model

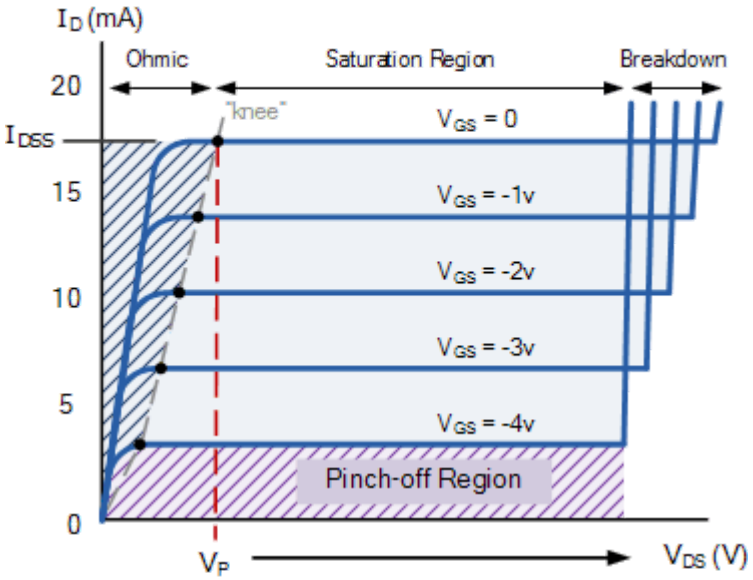
It is essential that the Gate voltage is never positive since if it is all the channel current will flow to the Gate and not to the Source, the result is damage to the JFET. Then to close the channel:

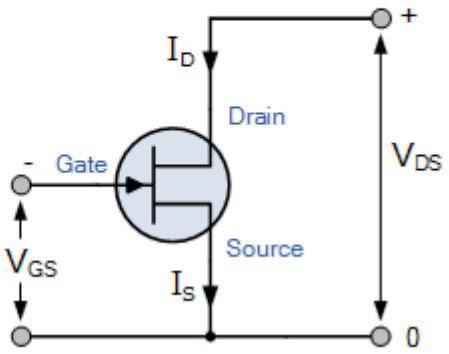
- No Gate voltage (V_{GS}) and V_{DS} is increased from zero.
- No V_{DS} and Gate control is decreased negatively from zero.
- V_{DS} and V_{GS} varying.

The P-channel **Junction Field Effect Transistor** operates the same as the N-channel above, with the following exceptions: 1). Channel current is positive due to holes, 2). The polarity of the biasing voltage needs to be reversed.

The output characteristics of an N-channel JFET with the gate short-circuited to the source is given as

Output characteristic V-I curves of a typical junction FET.





The voltage V_{GS} applied to the Gate controls the current flowing between the Drain and the Source terminals. V_{GS} refers to the voltage applied between the Gate and the Source while V_{DS} refers to the voltage applied between the Drain and the Source.

Because a **Junction Field Effect Transistor** is a voltage controlled device, "NO current flows into the gate!" then the Source current (I_S) flowing out of the device equals the Drain current flowing into it and therefore ($I_D = I_S$).

The characteristics curves example shown above, shows the four different regions of operation for a JFET and these are given as:

Ohmic Region – When V_{GS} = 0 the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.

Cut-off Region – This is also known as the pinch-off region were the Gate voltage, V_{GS} is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.

Saturation or Active Region – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.

Breakdown Region – The voltage between the Drain and the Source, (V_{DS}) is high enough to causes the JFET's resistive channel to break down and pass

uncontrolled maximum current.

The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current I_D decreases with an increasing positive Gate-Source voltage, V_{GS}.

The Drain current is zero when $V_{GS} = V_P$. For normal operation, V_{GS} is biased to be somewhere between V_P and 0. Then we can calculate the Drain current, I_D for any given bias point in the saturation or active region as follows:

Drain current in the active region.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Note that the value of the Drain current will be between zero (pinch-off) and I_{DSS} (maximum current). By knowing the Drain current I_D and the Drain-Source voltage V_{DS} the resistance of the channel (I_D) is given as:

Drain-Source channel resistance.

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m}$$

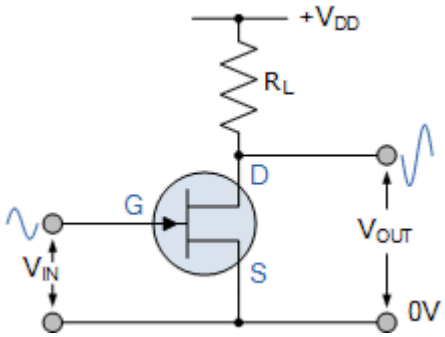
Where: g_m is the "transconductance gain" since the JFET is a voltage controlled device and which represents the rate of change of the Drain current with respect to the change in Gate-Source voltage.

Modes of FET's

Like the bipolar junction transistor, the field effect transistor being a three terminal device is capable of three distinct modes of operation and can therefore be connected within a circuit in one of the following configurations.

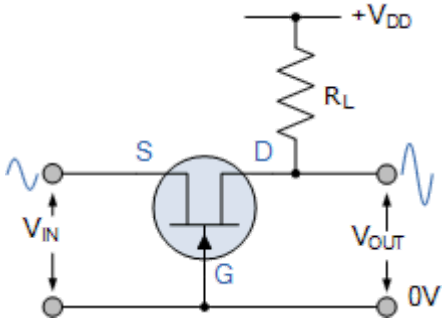
Common Source (CS) Configuration

In the **Common Source** configuration (similar to common emitter), the input is applied to the Gate and its output is taken from the Drain as shown. This is the most common mode of operation of the FET due to its high input impedance and good voltage amplification and as such Common Source amplifiers are widely used.



The common source mode of FET connection is generally used audio frequency amplifiers and in high input impedance pre-amps and stages. Being an amplifying circuit, the output signal is 180° "out-of-phase" with the input.

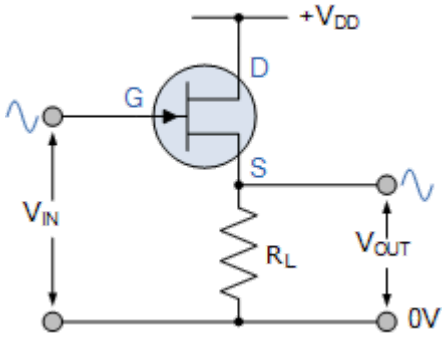
Common Gate (CG) Configuration



In the **Common Gate** configuration (similar to common base), the input is applied to the Source and its output is taken from the Drain with the Gate connected directly to ground (0v) as shown. The high input impedance feature of the previous connection is lost in this configuration as the common gate has a low input impedance, but a high output impedance.

This type of FET configuration can be used in high frequency circuits or in impedance matching circuits were a low input impedance needs to be matched to a high output impedance. The output is "in-phase" with the input.

Common Drain (CD) Configuration



In the **Common Drain** configuration (similar to common collector), the input is applied to the Gate and its output is taken from the Source. The common drain or "source follower" configuration has a high input impedance and a low output impedance and near-unity voltage gain so is therefore used in buffer amplifiers. The voltage gain of the source follower configuration is less than unity, and the output signal is "in-phase", 0° with the input signal.

This type of configuration is referred to as "Common Drain" because there is no signal available at the drain connection, the voltage present, $+V_{DD}$ just provides a bias. The output is in-phase with the input.

The JFET Amplifier

Just like the bipolar junction transistor, JFET's can be used to make single stage class A amplifier circuits with the JFET common source amplifier and characteristics being very similar to the BJT common emitter circuit. The main advantage JFET amplifiers have over BJT amplifiers is their high input impedance which is controlled by the Gate biasing resistive network formed by R1 and R2 as shown.

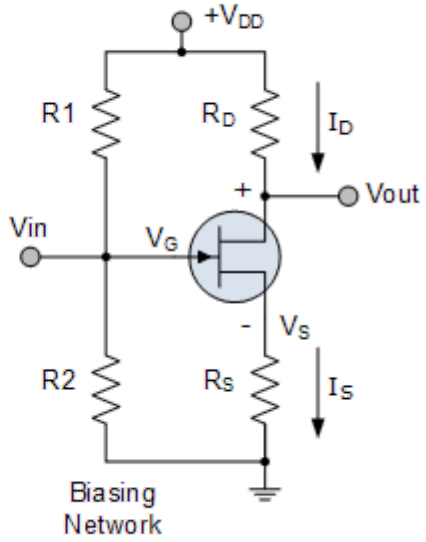
Biasing of JFET Amplifier

$$V_S = I_D R_S = \frac{V_{DD}}{4}$$

$$V_S = V_G - V_{GS}$$

$$V_G = \left(\frac{R2}{R1 + R2} \right) V_{DD}$$

$$I_D = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S}$$



This common source (CS) amplifier circuit is biased in class "A" mode by the voltage divider network formed by resistors R1 and R2. The voltage across the Source resistor R_S is generally set to be about one quarter of V_{DD}, (V_{DD} /4) but can be any reasonable value. The required Gate voltage can then be calculated from this R_S value. Since the Gate current is zero, (I_G = 0) we can set the required DC quiescent voltage by the proper selection of resistors R1 and R2.

The control of the Drain current by a negative Gate potential makes the **Junction Field Effect Transistor** useful as a switch and it is essential that the Gate voltage is never positive for an N-channel JFET as the channel current will flow to the Gate and not the Drain resulting in damage to the JFET. The principals of operation for a P-channel JFET are the same as for the N-channel JFET, except that the polarity of the voltages need to be reversed.

In the next tutorial about **Transistors**, we will look at another type of Field Effect Transistor called a **MOSFET** whose Gate connection is completely isolated from the main current carrying channel.

43 Comments

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Your Name

Email Address

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SUBMIT

s sahana

does jfet helps in increasing the range of detection of radio frequency,if yes plz tell me how?

Posted on September 23rd 2016 | 11:58 am

Reply

H Hashim

please can someone explain how impedance matching is perform using jfet.

Posted on August 28th 2016 | 12:21 pm

Reply

p prathamesh muralidhar sawant

justify that JFET canbe used as a voltage variable resistor

Posted on August 12th 2016 | 8:33 am

Reply

P

Parthy

Thank you so much for the information. It was very useful.

Can you please explain why Vss= Vdd/4?

Posted on August 11th 2016 | 1:56 am

Reply

Wayne Storr

Rs is used in a common-source configuration to set the Q point and raise the quiescent source voltage above zero resulting in greater stability. As its a resistance, ohms law tells us that a current passing through a resistance results in a voltage drop. This current is Is and the voltage (Vs) needs to be sufficiently greater than 0v but less than half Vdd for the Q point to be in the linear part of the characteristics, so a value around one-quarter of Vdd, that is Vdd/4 is a good place to start. From that Rs is calculated as (Vdd/4)/Is. Vs could be any voltage value you want in reality to set the appropriate bias at Vg.

Posted on August 11th 2016 | 7:19 am

Reply

S

Shubham

very clearly explained..thanks

Posted on August 03rd 2016 | 5:20 am

Reply

R

Rashmi

Very clearly explained

Thanks so much

Posted on July 17th 2016 | 3:17 pm

Reply

prajakta

It was a really helpful one. thank you so much!

Posted on July 13th 2016 | 6:24 am

Reply

A

Amina Job

I learned alot from here thank you very much.....but please may you include some worked examples

Posted on June 21st 2016 | 6:25 pm

Reply

D

Devika V S

Thanks!
It really helped me during my exams.

Posted on May 01st 2016 | 3:39 pm

Reply

P

Penversation

Hello, my friend. Very nice article, great job. However, regarding the pinch-off voltage, if you take a look at the characteristics V-I curves, it's not meant to reduce the drain current to zero. Vp(pinch-off) is the drain-to-source voltage which makes the drain current to go into saturation and remain constant until V(breakdown). You didn't mention Vgs(off), which is the gate-to-source voltage that closes the channel and makes the drain current to go to zero.

Thanks

Posted on April 18th 2016 | 9:25 pm

Reply

J

Jaqen

I strongly agree with your comment.

Posted on June 11th 2016 | 9:18 am

Reply

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