

# CrossLink-NX Evaluation Board

Rev - B

- 01 - Title page
- 02 - Block Diagram
- 03 - USB Interface
- 04 - Camera Interface (DPHYs)
- 05 - Raspberry Pi and User I/O Interface (Bank6)
- 06 - SERDES SMAs / Switches / FMC Control (Bank2)
- 07 - I2C LEDs and Push Buttons (Bank1)
- 08 - PMODs (Bank7)
- 09 - Configuration and ADC (Bank0)
- 10 - FMC-LPC (Bank3/4/5)
- 11 - Power CSI and Banks
- 12 - Power Decoupling
- 13 - Power Regulators
- 14 - Power Block Diagram

## Notes:

Resistors size 0402, tolerance 5%, unless otherwise specified.

Ferrite Beads size 0402 unless otherwise specified.

Capacitors  $\geq 4.7\mu\text{F}$  size 0603 unless otherwise specified.

Capacitors  $< 4.7\mu\text{F}$  size 0402 unless otherwise specified.



Lattice Semiconductor Applications  
<http://www.latticesemi.com/Support>

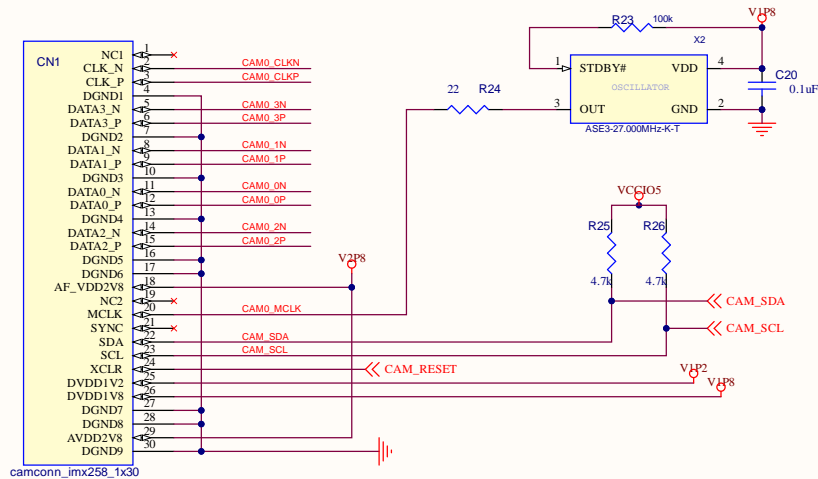
Title			
Title page			
Size	Project	Schematic Rev	
B	CrossLink-NX Evaluation Board	1.0	
Date:		Board Rev	
Friday, Nov 22, 2019		B	
Sheet		1 of 14	



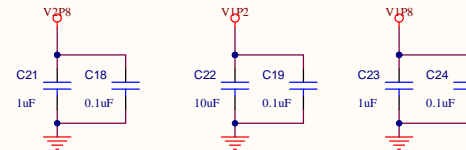
Lattice Semiconductor Applications  
<http://www.latticesemi.com/Support>

Title			
Block Diagram			
Size B	Project		Schematic Rev 1.0
	CrossLink-NX Evaluation Board		Board Rev B
Date: Friday, Nov 22, 2019		Sheet	2 of 14





Keep LEDs away from Camera



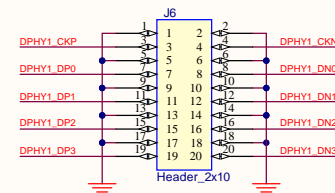
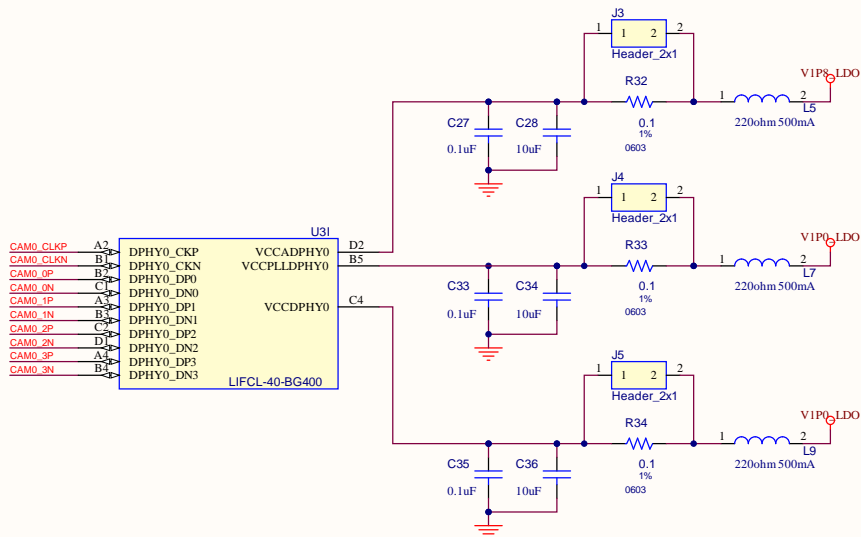
#### LVDS RX Termination Resistors



NOTE: Place close to FPGA

NOTE:

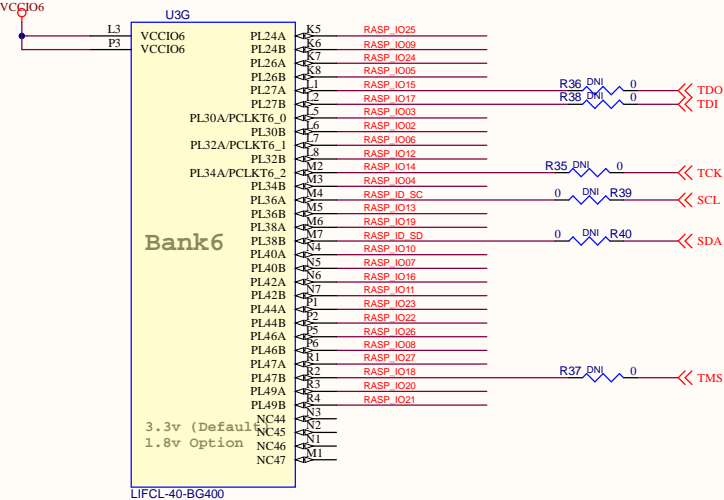
1. Match length within pair  $\leq 0.1\text{mm}$ , match length between pairs  $\leq 1.0\text{mm}$ .
2. Differential impedance should be 100 ohms and 50 ohms as a single ended signal
3. All the power rails should be capable of carrying 1A current



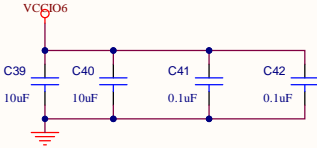
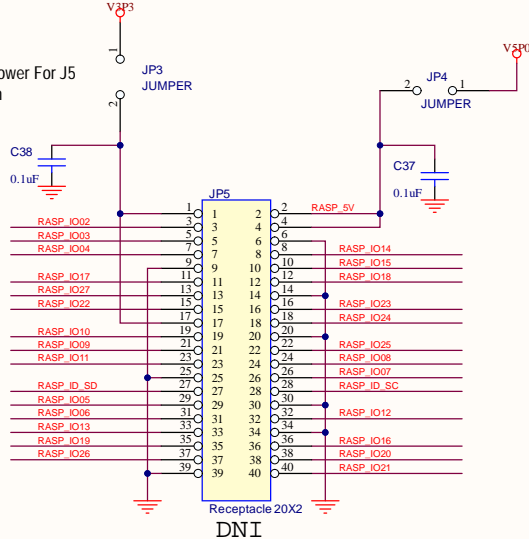
Lattice Semiconductor Applications  
<http://www.latticesemi.com/Support>

Title		
Camera Interface (DPHYs)		
Size	Project	Schematic Rev
B	CrossLink-NX Evaluation Board	1.0
Date:	Friday, Nov 22, 2019	Board Rev
		B
Sheet	4	of 14

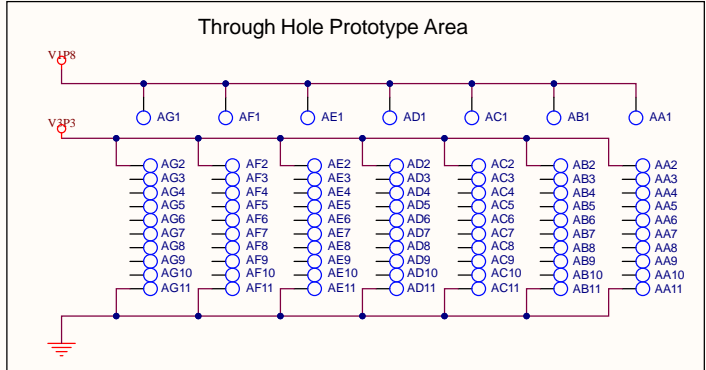
Raspberry PI and User I/O Connector



JP3 & JP4 Power For J5  
Default Open



Layout:  
SS: Put box around Prototype Area  
SS: Row and Column Letters/Numbers  
Close to FMC-LPC and JP5



Lattice Semiconductor Applications  
<http://www.latticesemi.com/Support>

Title

Raspberry Pi and User I/O Interface

Size B

Project

CrossLink-NX Evaluation Board

Schematic Rev 1.0

Board Rev B

Date: Friday, Nov 22, 2019

Sheet 5 of 14

PLL filter with DCR<=0.1 ohm  
DC must be <<5% drop across  
anti-resonance resistor under  
worst case

Place PLL series resistor,  
two caps and r\_ext right  
underneath the chip on the  
reverse side of the board

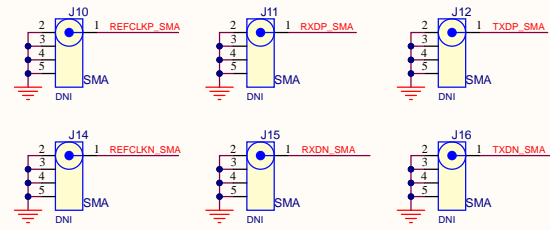
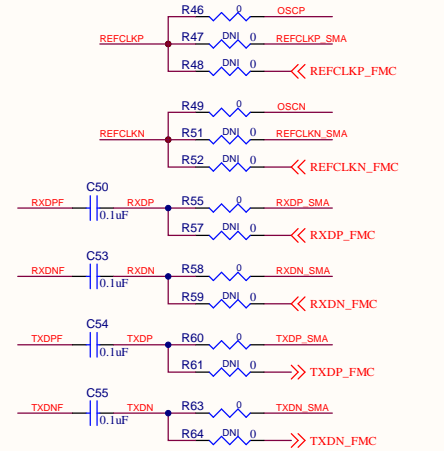
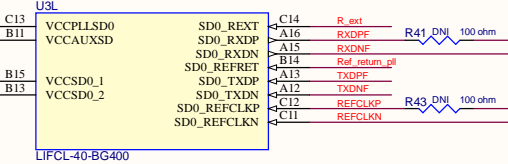
R\_ext is chosen for 100 ohm Diff

Use little to no stub  
between selection  
resistors

Minimize length as short as possible  
short\_stub\_trace. TP close to FPGA

Two 50 ohm Lookbacks Traces: 6 inches and 10 inches  
Place TPs close to FPGA

## Serdes Bank



Route SMA pairs as 100 ohm differential

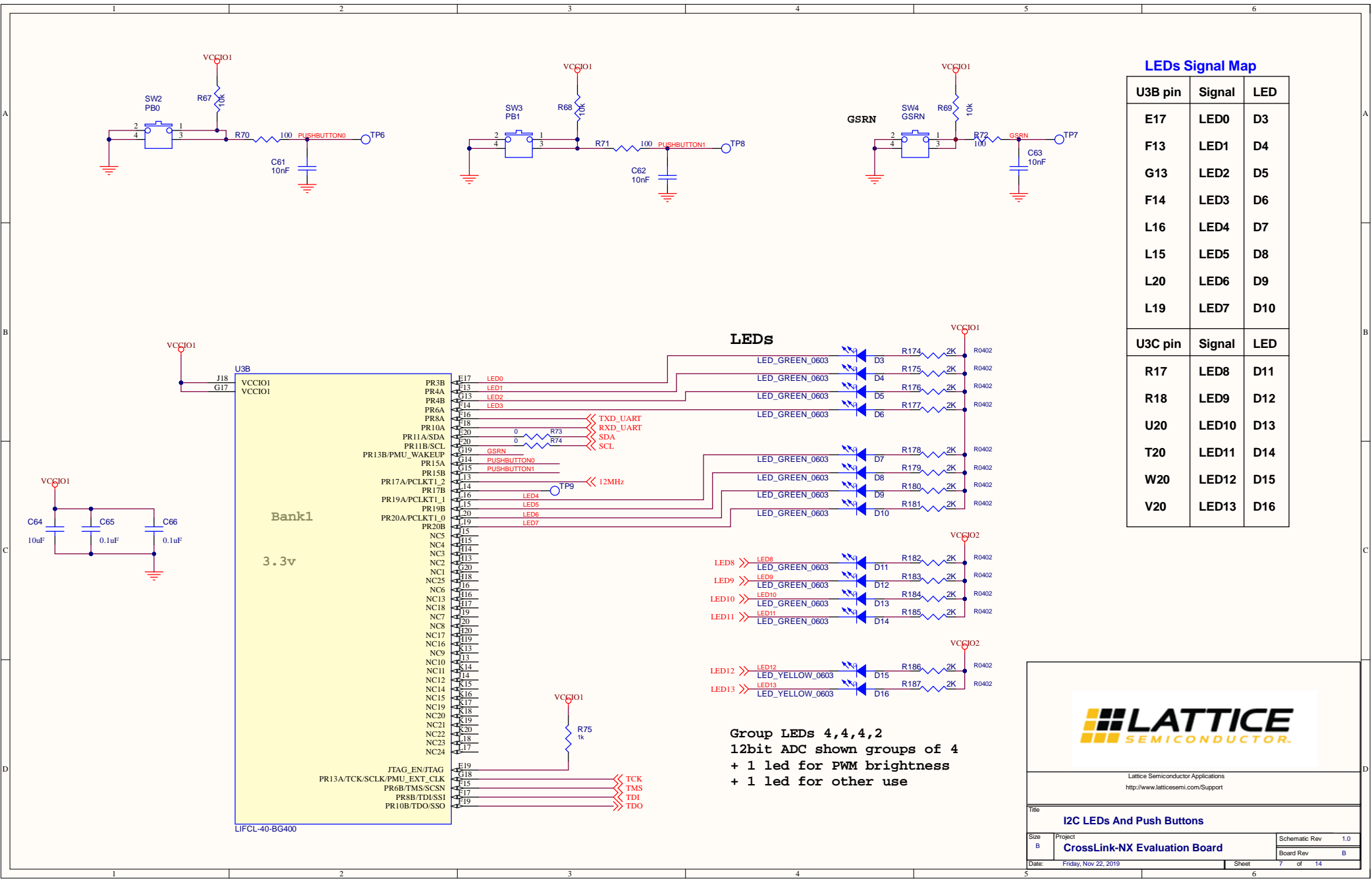
## Switch Signal Map

U3C Pin	Signal	SWITCH
N14	SWITCH0	1
M14	SWITCH1	2
M16	SWITCH2	3
M15	SWITCH3	4
N15	SWITCH4	5
N16	SWITCH5	6
M17	SWITCH6	7
M18	SWITCH7	8



Lattice Semiconductor Applications  
<http://www.latticesemi.com/Support>

Title <b>Serdes SMAs/Switches/FMC Control</b>		
Size B	Project <b>CrossLink-NX Evaluation Board</b>	Schematic Rev 1.0
Date Friday, Nov 22, 2019	Sheet 6 of 14	Board Rev B



Lattice Semiconductor Applications  
<http://www.latticesemi.com/Support>

Title			
I2C LEDs And Push Buttons			
Size	Project	Schematic Rev	
B	CrossLink-NX Evaluation Board	1.0	
Date:	Friday, Nov 22, 2019	Sheet	7 of 14

1	2	3	4	5	6
---	---	---	---	---	---



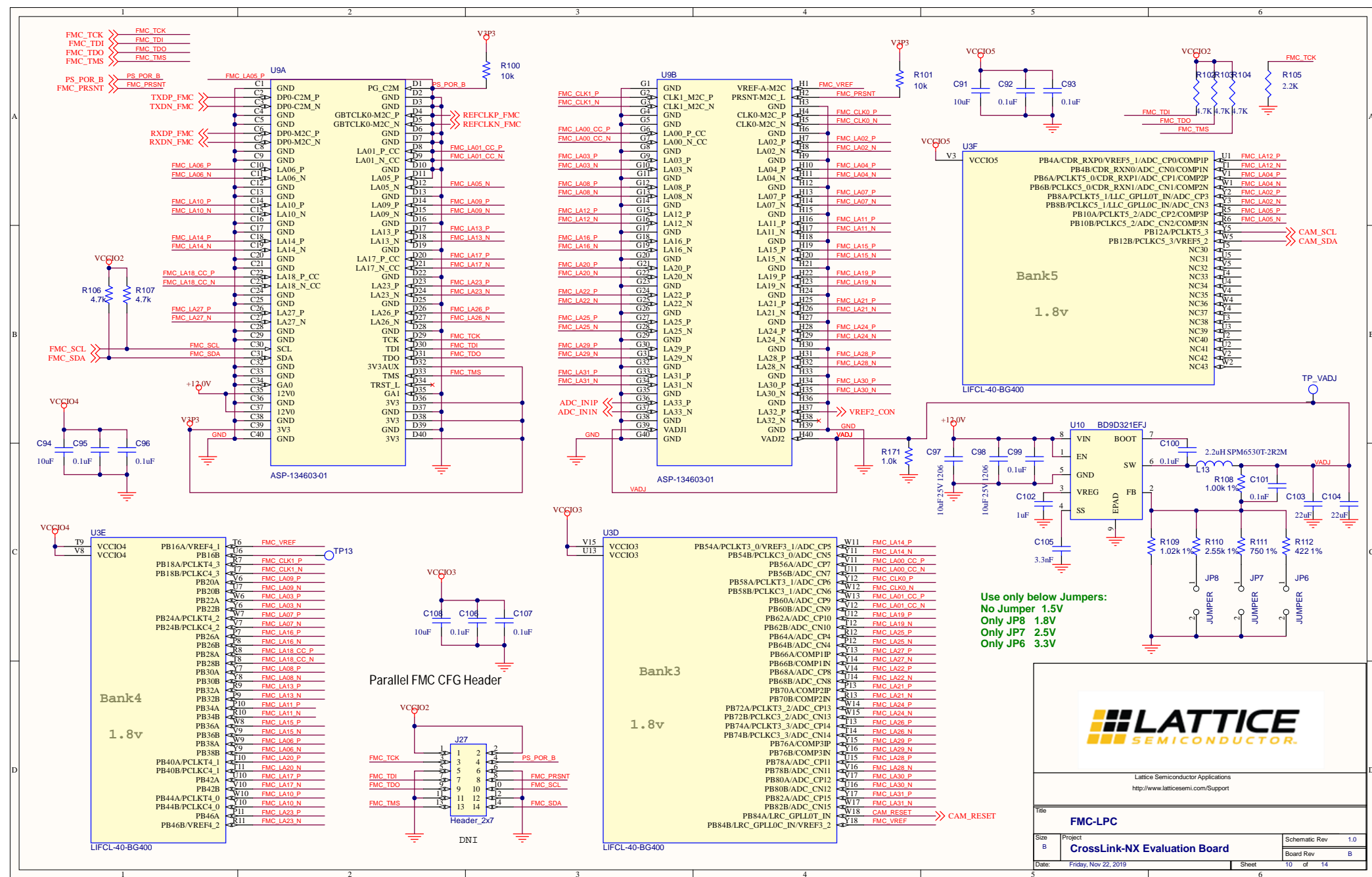
B



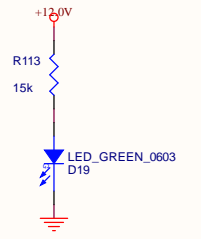
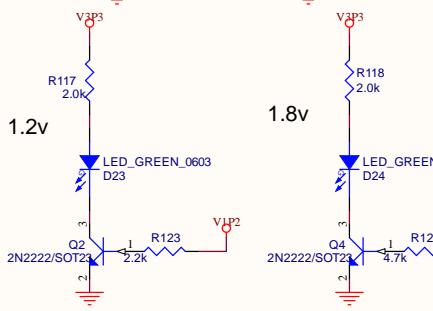
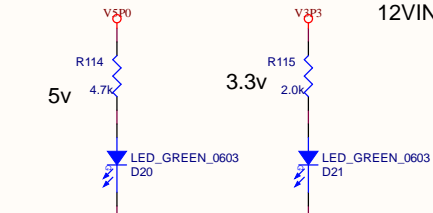
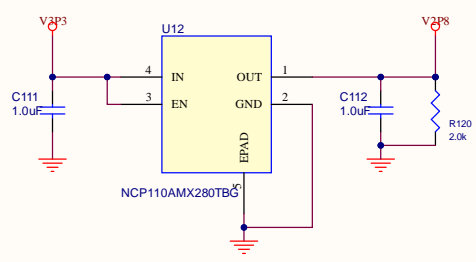
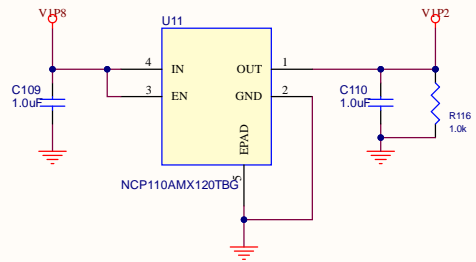
B

1	2	3	4	5	6
---	---	---	---	---	---

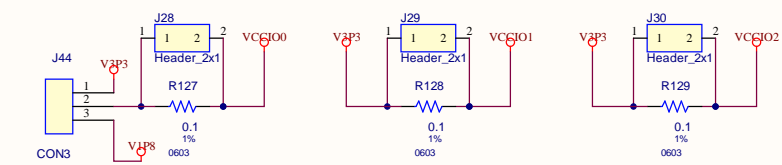
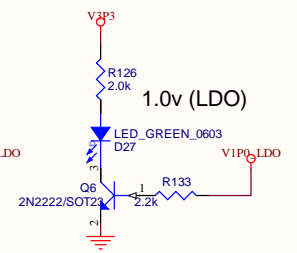
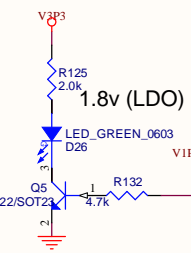
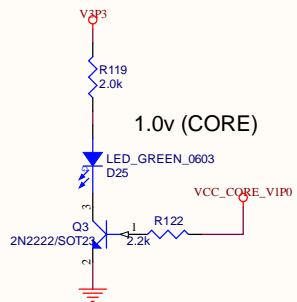
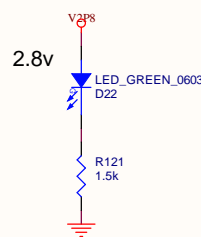




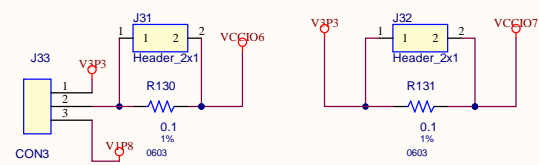
1 2 3 4 5 6



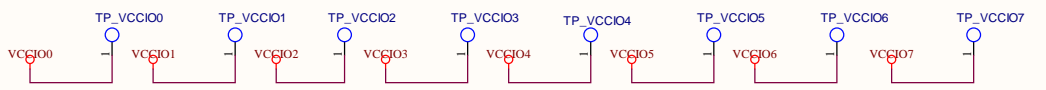
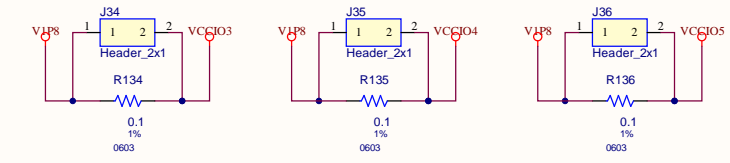
Group LEDs together



Flash Voltage Select  
1-2 3.3V (Default)  
2-3 1.8V (Note PMOD2 unavailable)

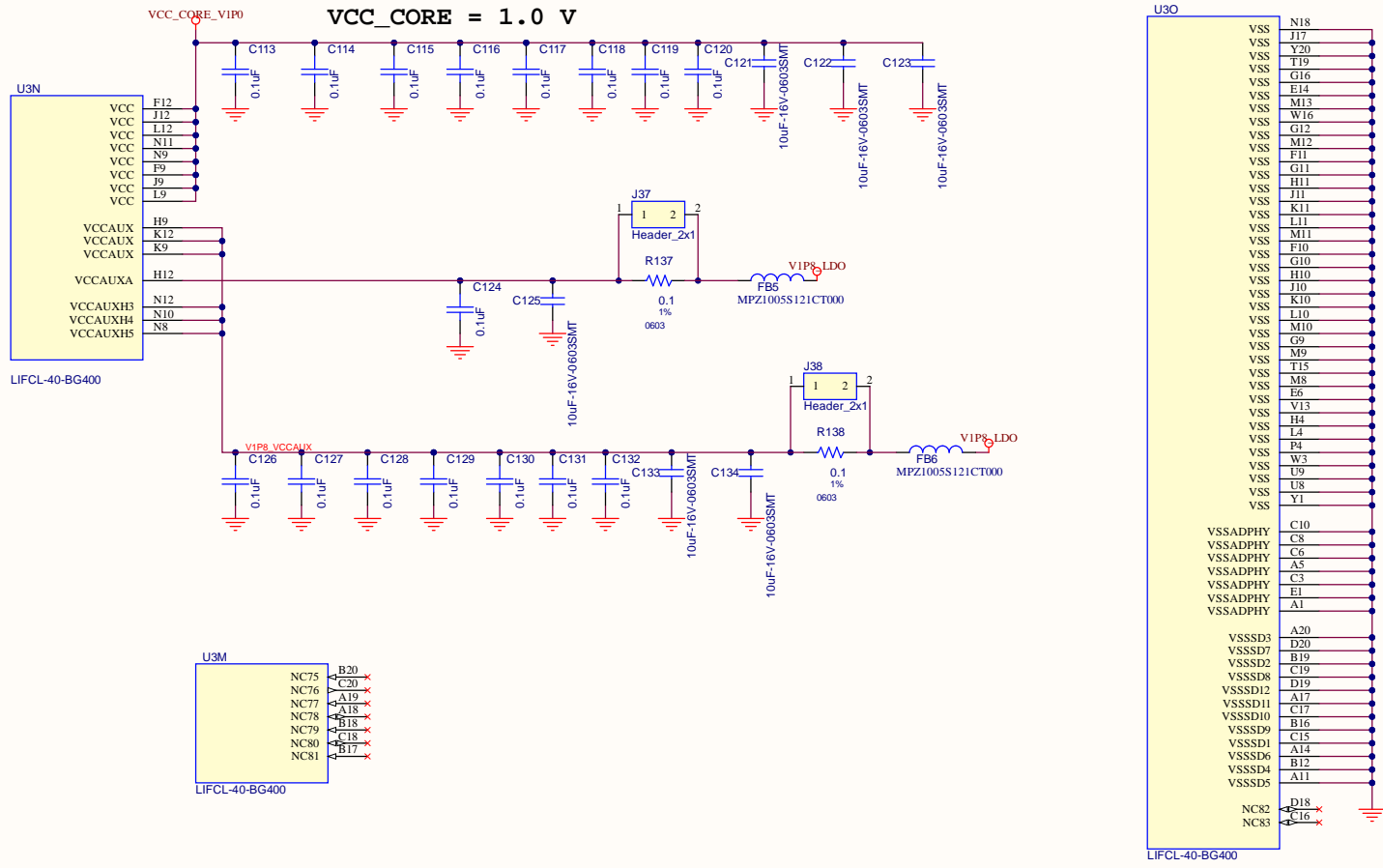


RPI / User I/O Voltage Select  
1-2 3.3V (Default)  
2-3 1.8V



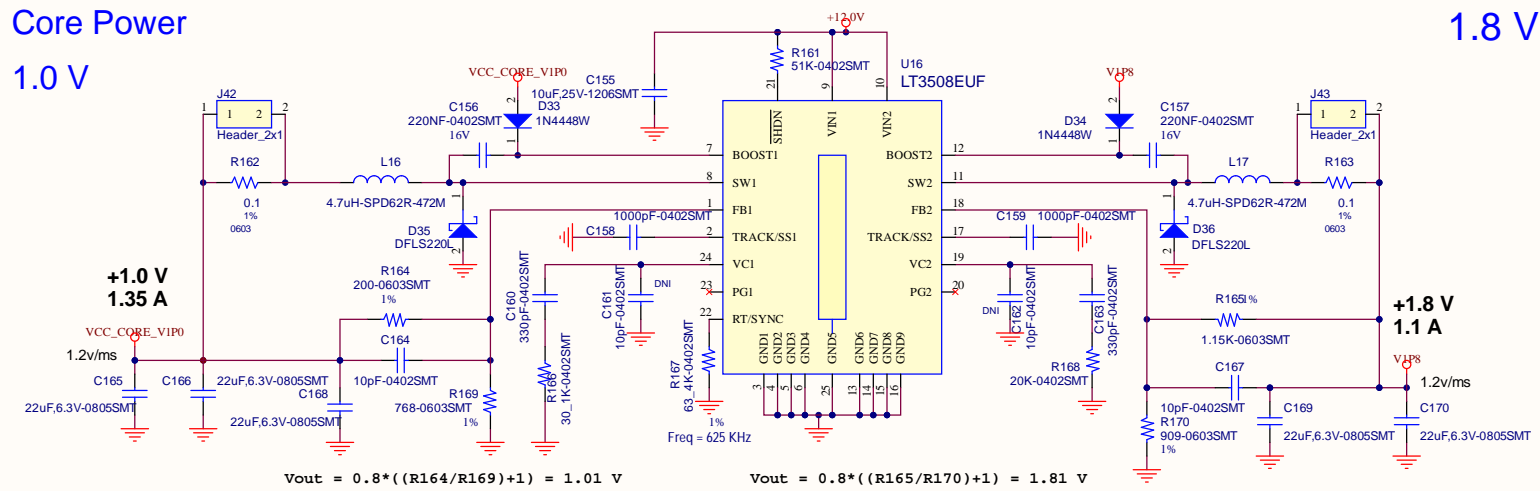
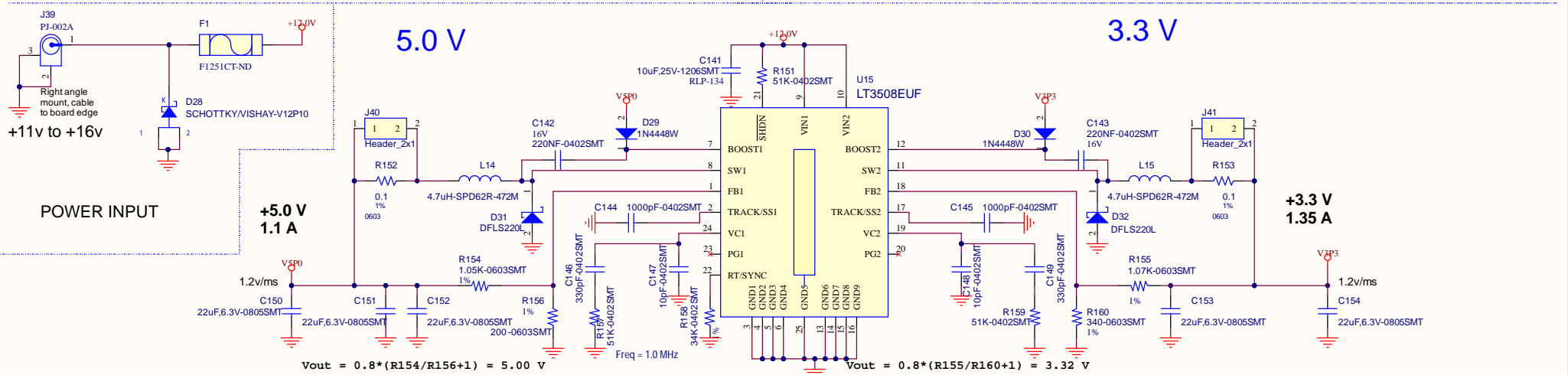
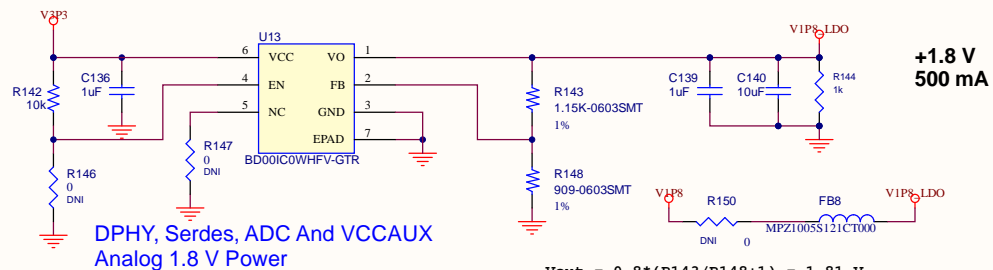
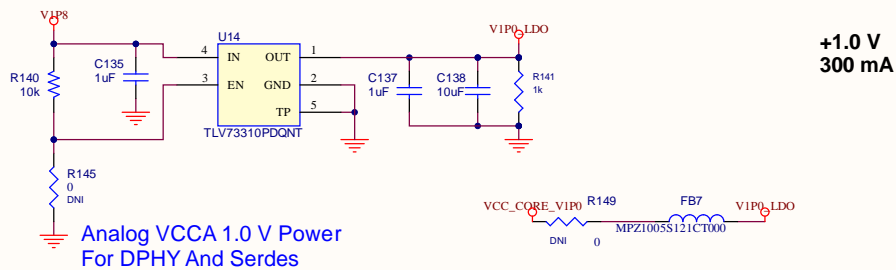
Lattice Semiconductor Applications  
<http://www.latticesemi.com/Support>

Title			
Power CSI and Banks			
Size	Project	Schematic Rev	1.0
B	CrossLink-NX Evaluation Board	Board Rev	B
Date:	Friday, Nov 22, 2019	Sheet	11 of 14



Lattice Semiconductor Applications  
<http://www.latticesemi.com/Support>

Title		
Power Decoupling		
Size	Project	Schematic Rev
B	CrossLink-NX Evaluation Board	1.0
Date:	Friday, Nov 22, 2019	Board Rev
		B
Sheet	12 of 14	



Lattice Semiconductor Applications <a href="http://www.latticesemi.com/Support">http://www.latticesemi.com/Support</a>			
Title: Power Regulators			
Size: B	Project: CrossLink-NX Evaluation Board	Schematic Rev: 1.0	
Date: Friday, Nov 22, 2019	Sheet: 13 of 14	Board Rev: B	



Lattice Semiconductor Applications  
<http://www.latticesemi.com/Support>

Title			
Power Block Diagram			
Size B	Project		Schematic Rev 1.0
	CrossLink-NX Evaluation Board		Board Rev B
Date: Friday, Nov 22, 2019		Sheet	14 of 14