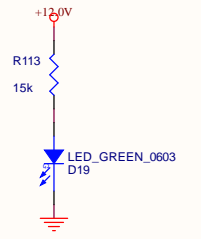
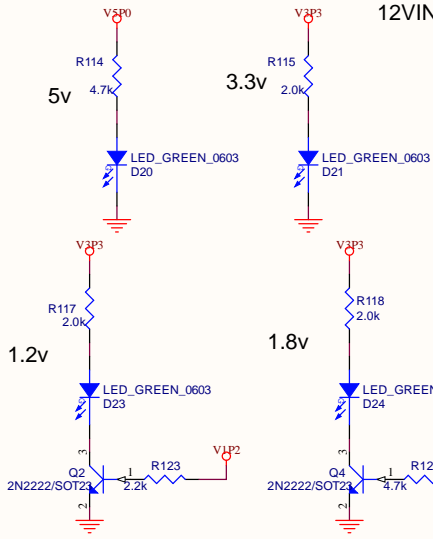
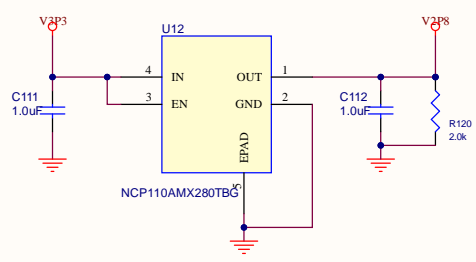
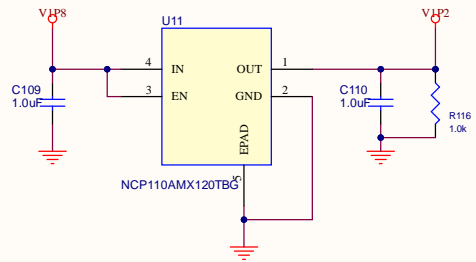


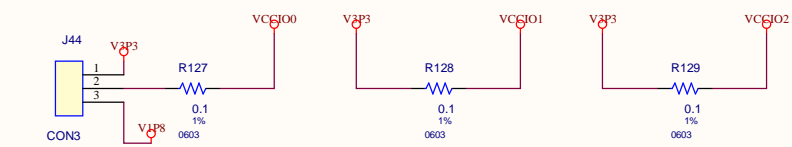
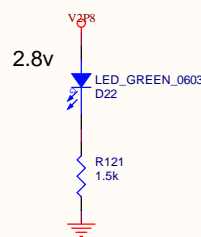
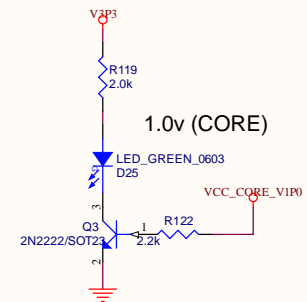
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<http://www.latticesemi.com/Support>

Title			
Power Regulators			
Size	Project	Schematic Rev 1.0	
B		Board Rev	B
Date:		Sheet	1 of 12

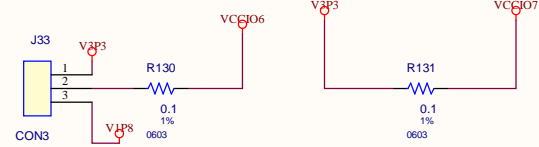
1 2 3 4 5 6



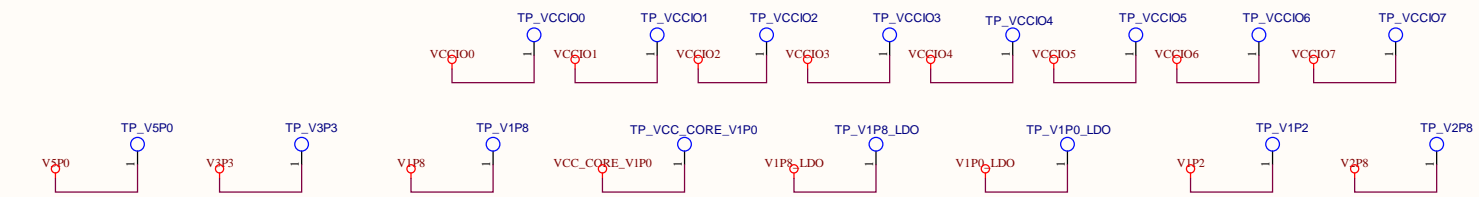
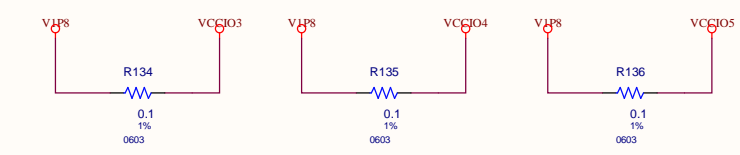
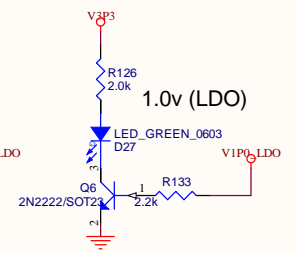
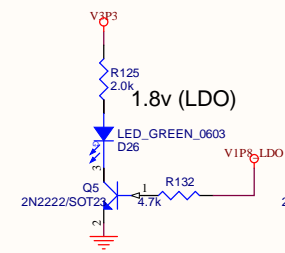
Group LEDs together



Flash Voltage Select
1-2 3.3V (Default)
2-3 1.8V (Note PMOD2 unavailable)



RPI / User I/O Voltage Select
1-2 3.3V (Default)
2-3 1.8V



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Title			
Power CSI and Banks			
Size B	Project	Schematic Rev 1.0	
		Board Rev B	
Date:		Sheet 2 of 12	
5		6	

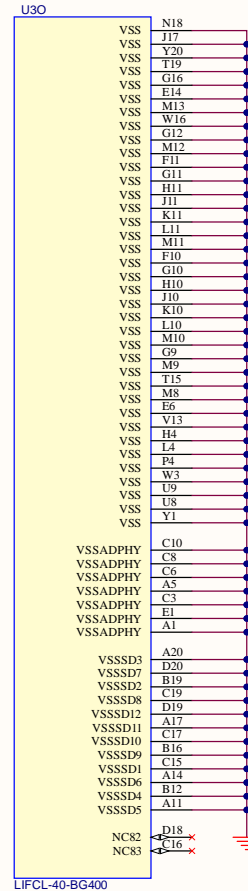
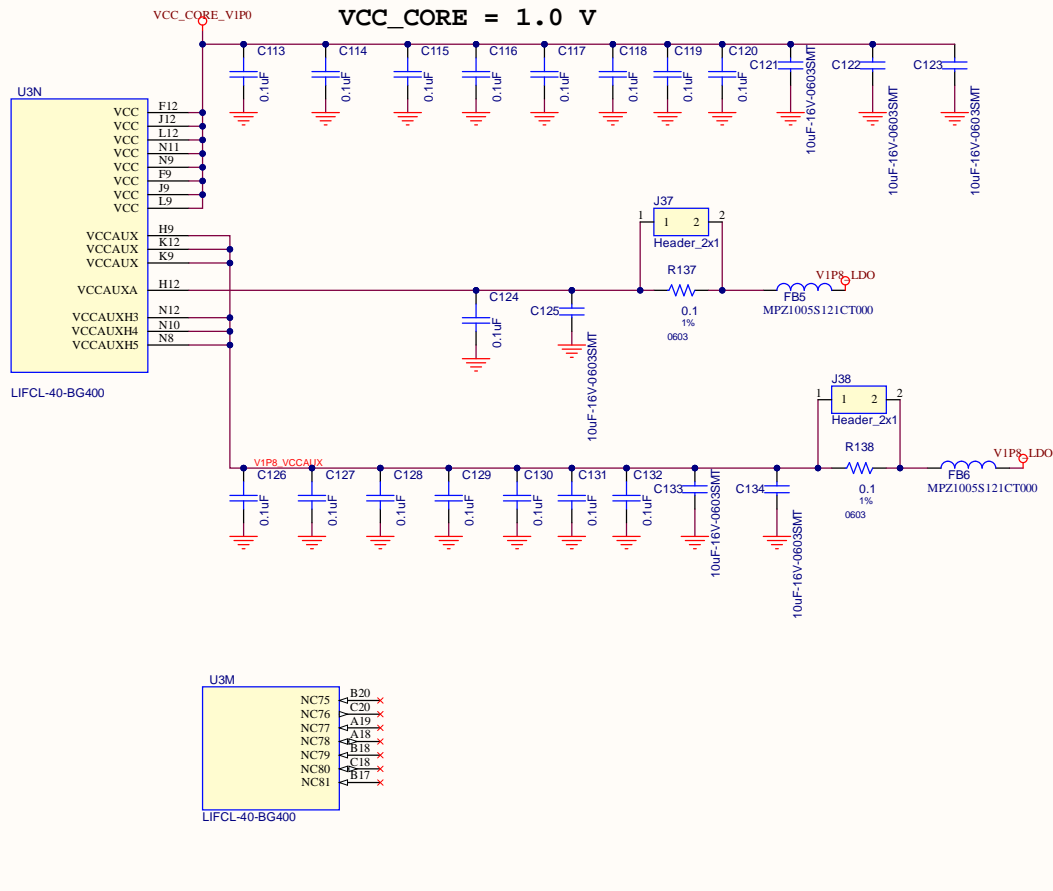
1 2 3 4 5 6

A

B

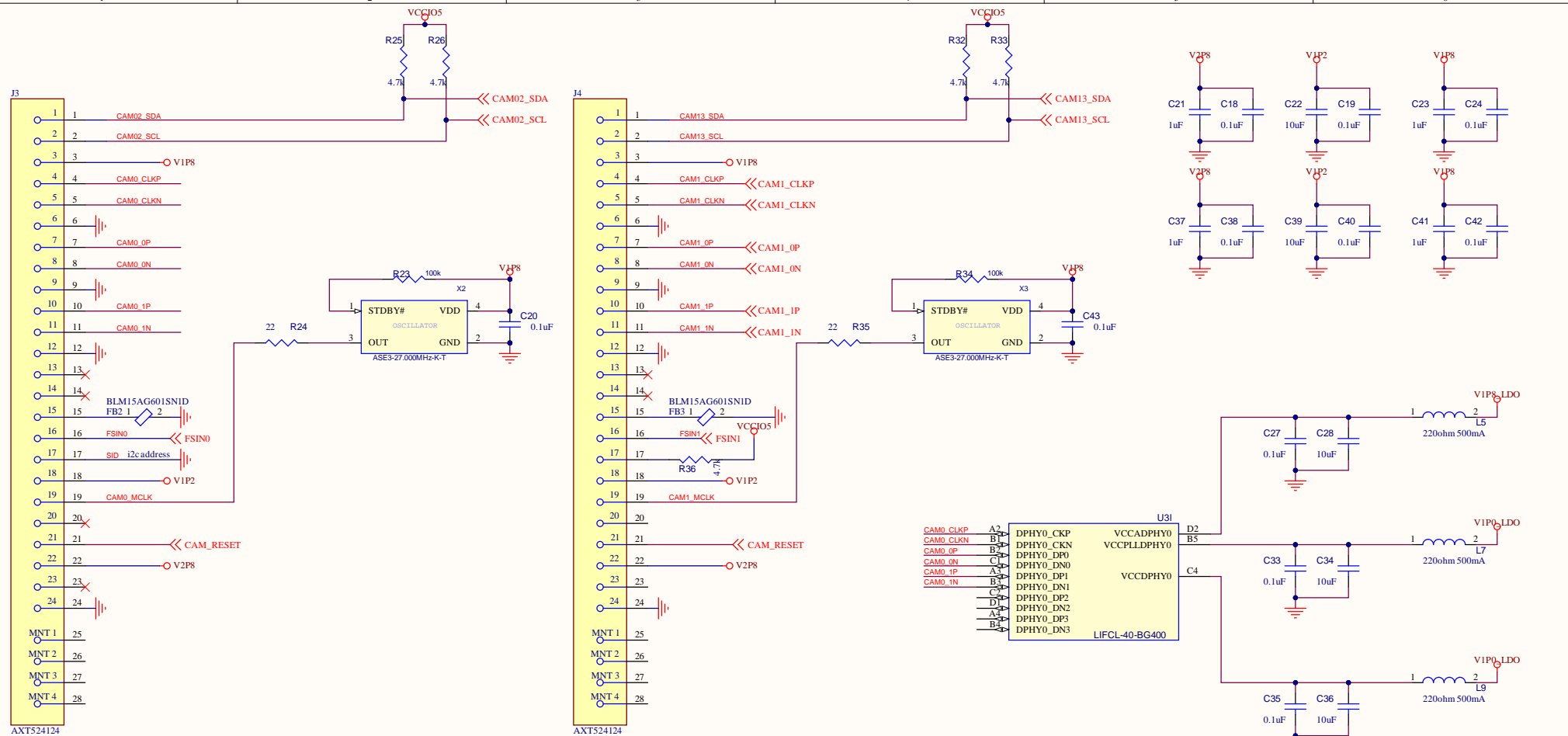
C

D

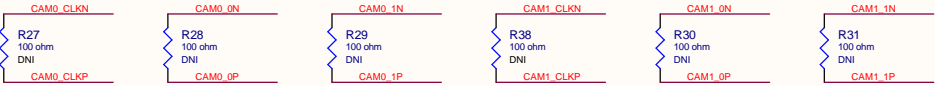


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Title Power Decoupling			
Size B	Project	Schematic Rev 1.0	Board Rev B
Date:		Sheet 3 of 12	



LVDS RX Termination Resistors

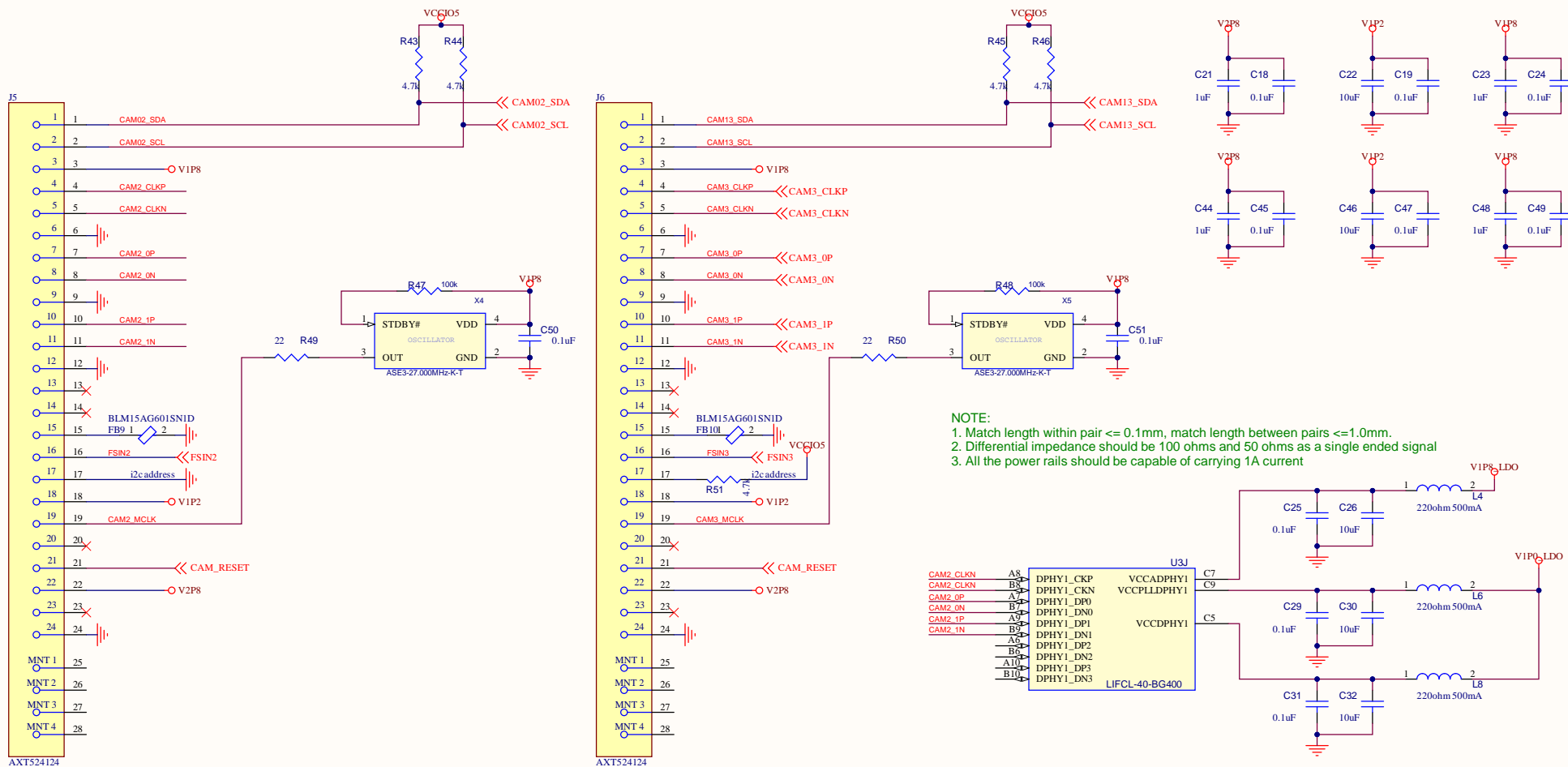


NOTE: Place close to FPGA

- NOTE:
1. Match length within pair <= 0.1mm, match length between pairs <=1.0mm.
 2. Differential impedance should be 100 ohms and 50 ohms as a single ended signal
 3. All the power rails should be capable of carrying 1A current

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Title Camera Interface (DPHYs)		
Size B	Project	Schematic Rev 1.0
Date:	Sheet 4 of 12	Board Rev B



LVDS RX Termination Resistors



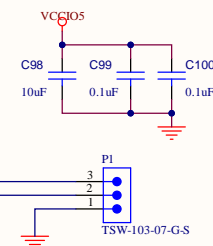
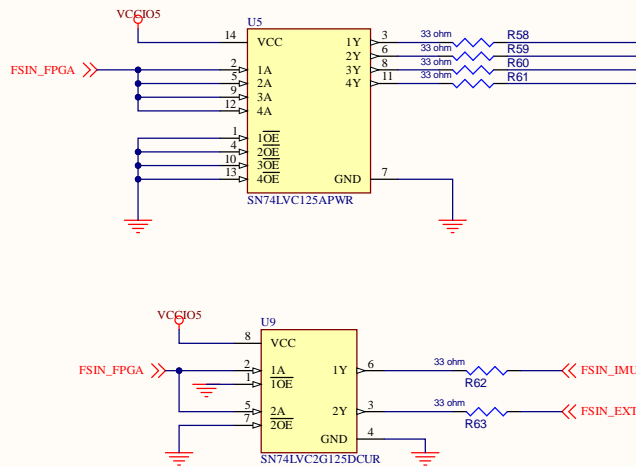
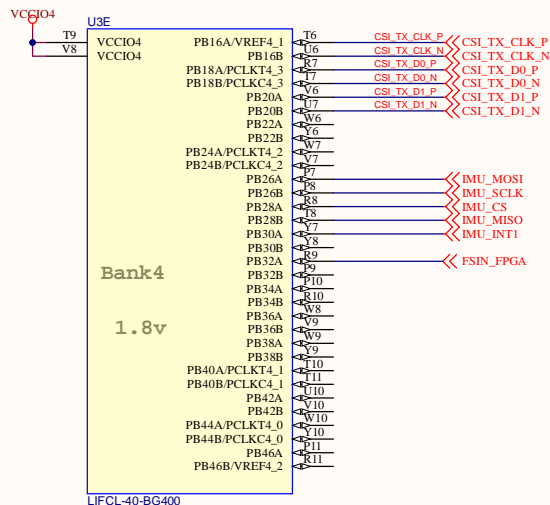
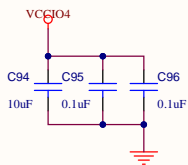
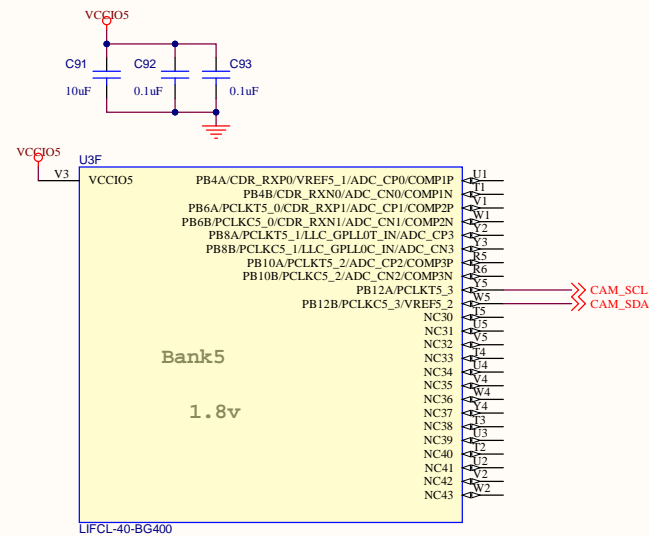
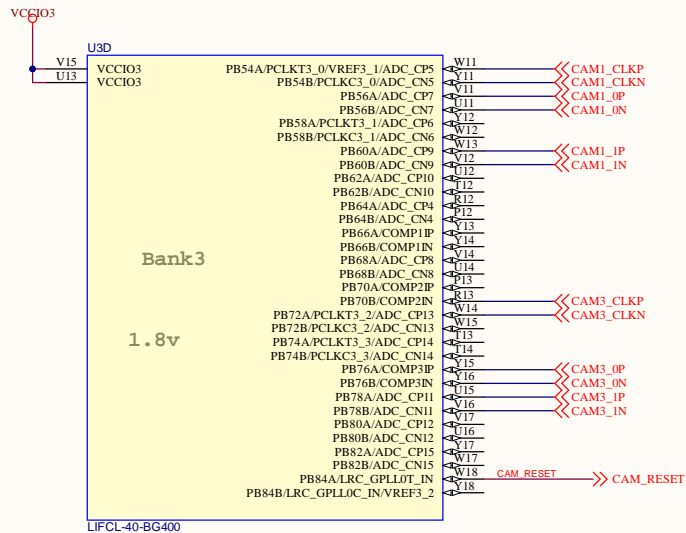
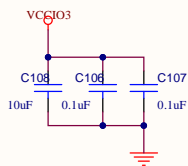
NOTE: Place close to FPGA

Keep LEDs away from Camera

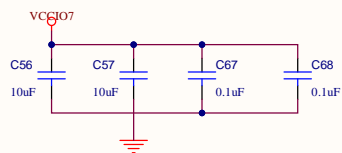
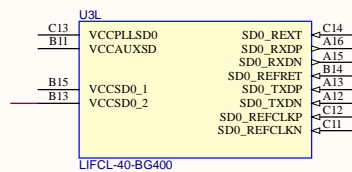
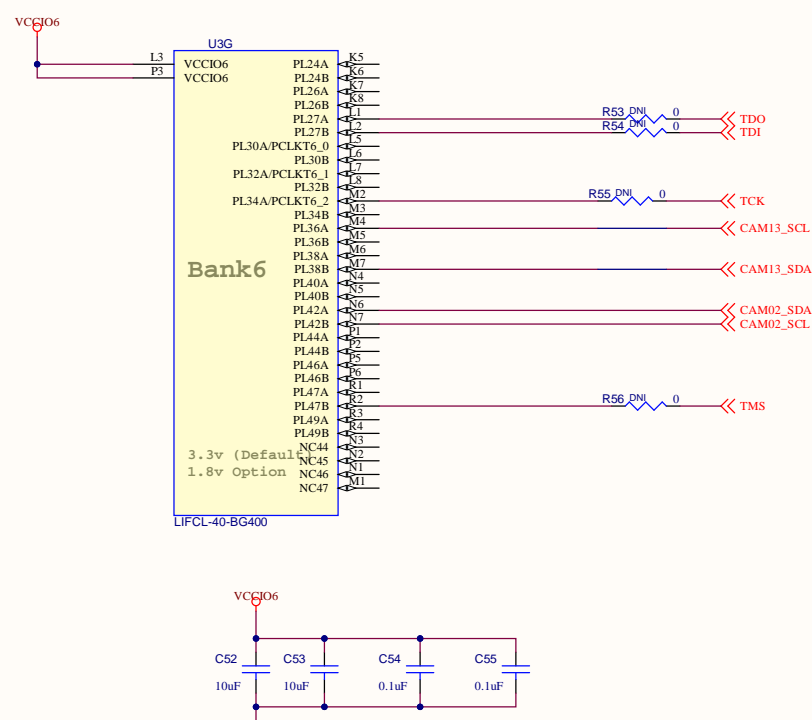
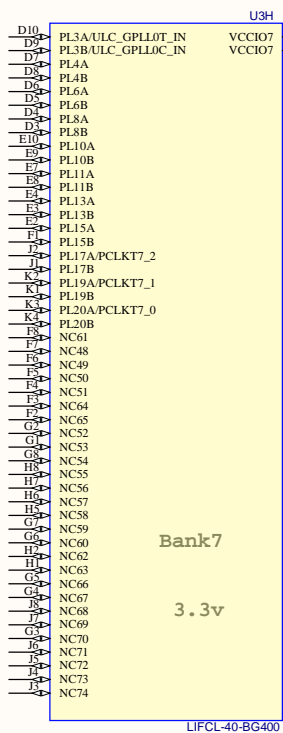
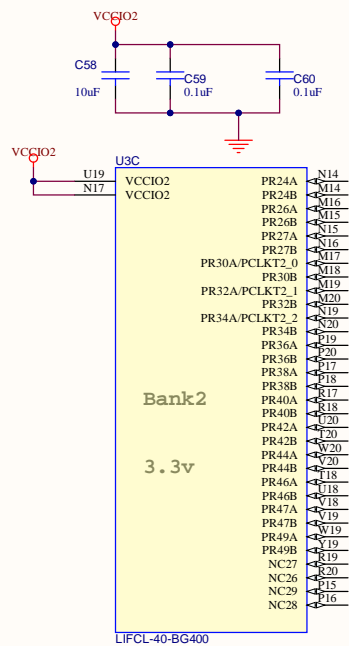


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Title		
Camera Interface (DPHYs)		
Size	Project	Schematic Rev
B		1.0
Date:	Sheet	Board Rev
	5 of 12	B



Lattice Semiconductor Applications http://www.latticesemi.com/Support			
Title Soft DPHY			
Size B	Project	Schematic Rev 1.0	Board Rev B
Date: 0	Sheet 6 of 12		

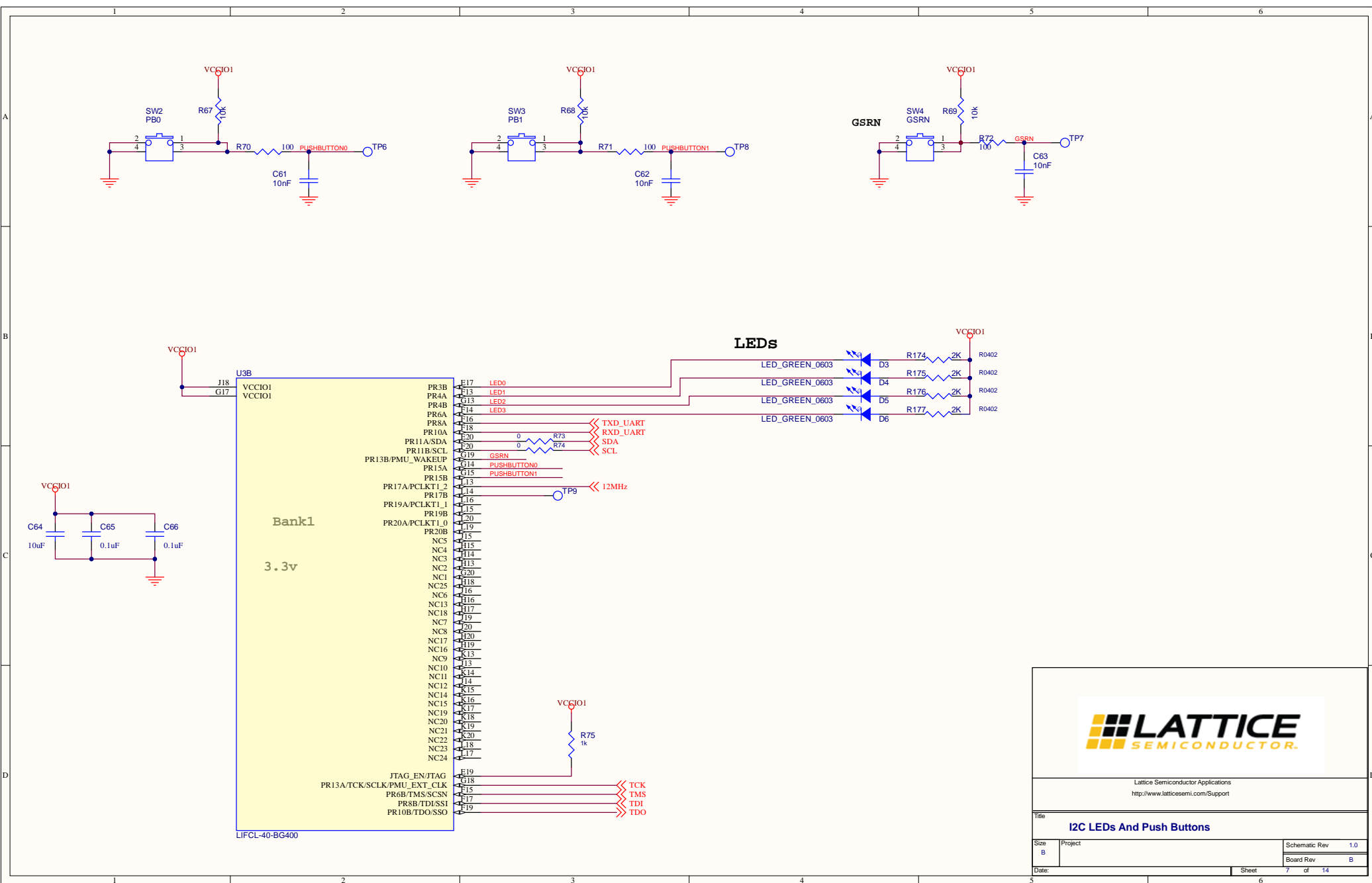


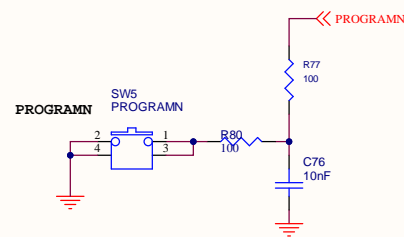
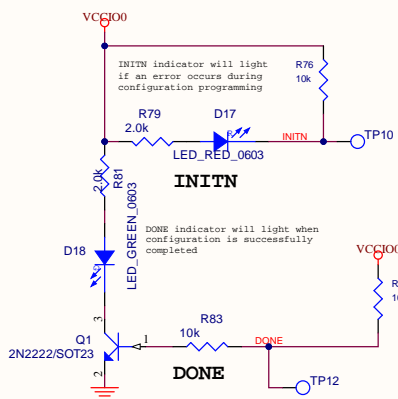
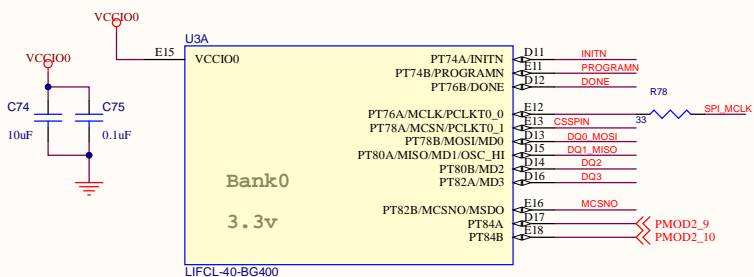
Route SMA pairs as 100 ohm differential



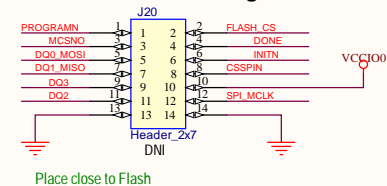
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Title			
Bank 2-6-7			
Size	Project	Schematic Rev	1.0
B		Board Rev	B
Date:	Sheet 6 of 14		

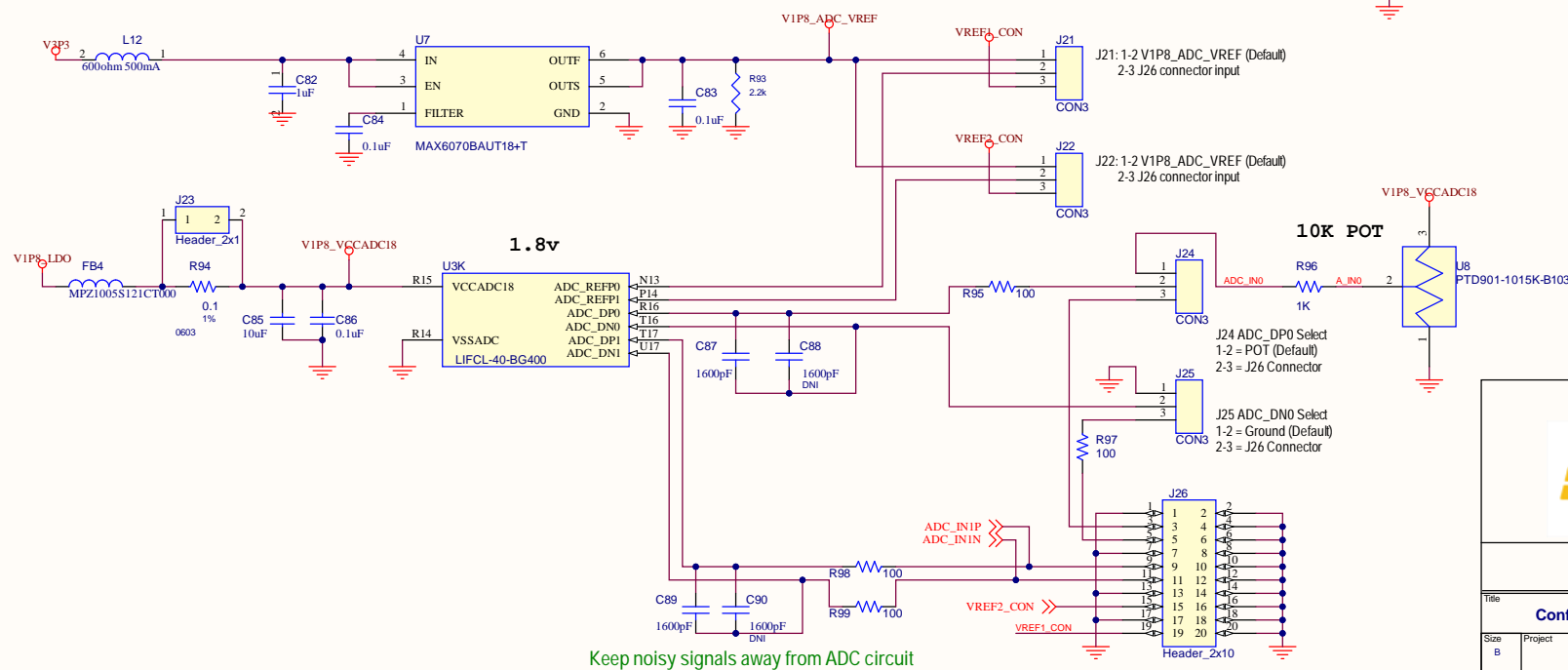
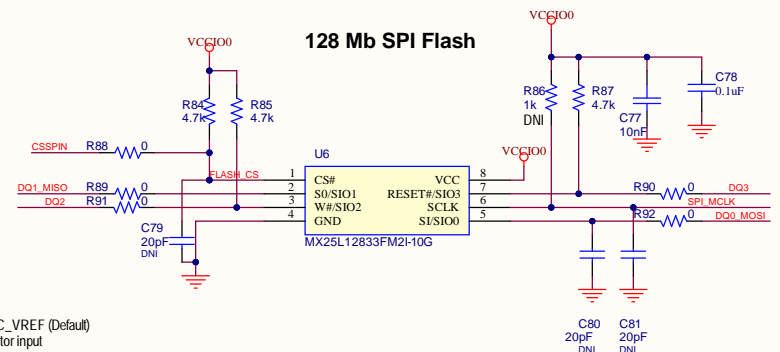




Parallel / SPI Config Header



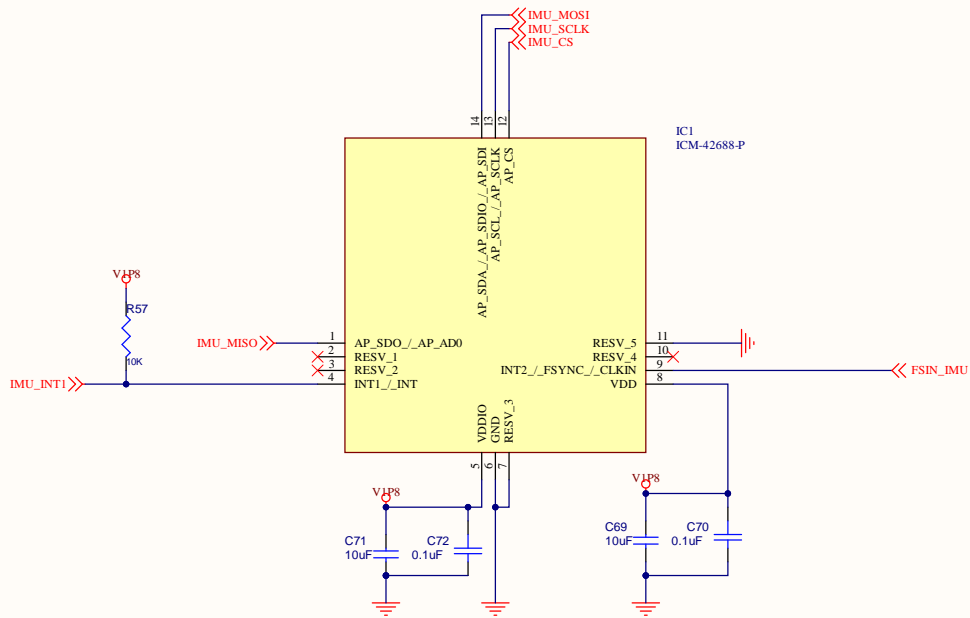
128 Mb SPI Flash



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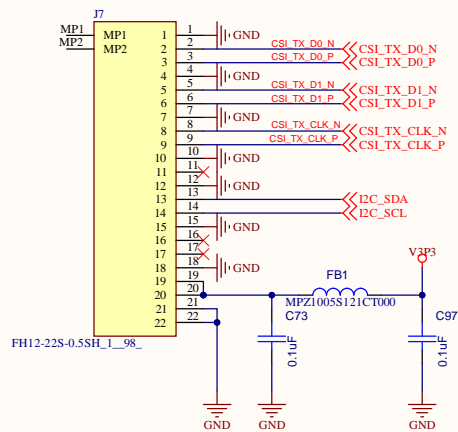
Configuration and ADC

Size	Project	Schematic Rev	1.0
B		Board Rev	B
Date:		Sheet	10 of 12



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Title			
IMU			
Size	Project		Schematic Rev
B			1.0
Date:			Board Rev
			B



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Title JETSON-CON		
Size	Project	Schematic Rev
Date:	Sheet	Board Rev