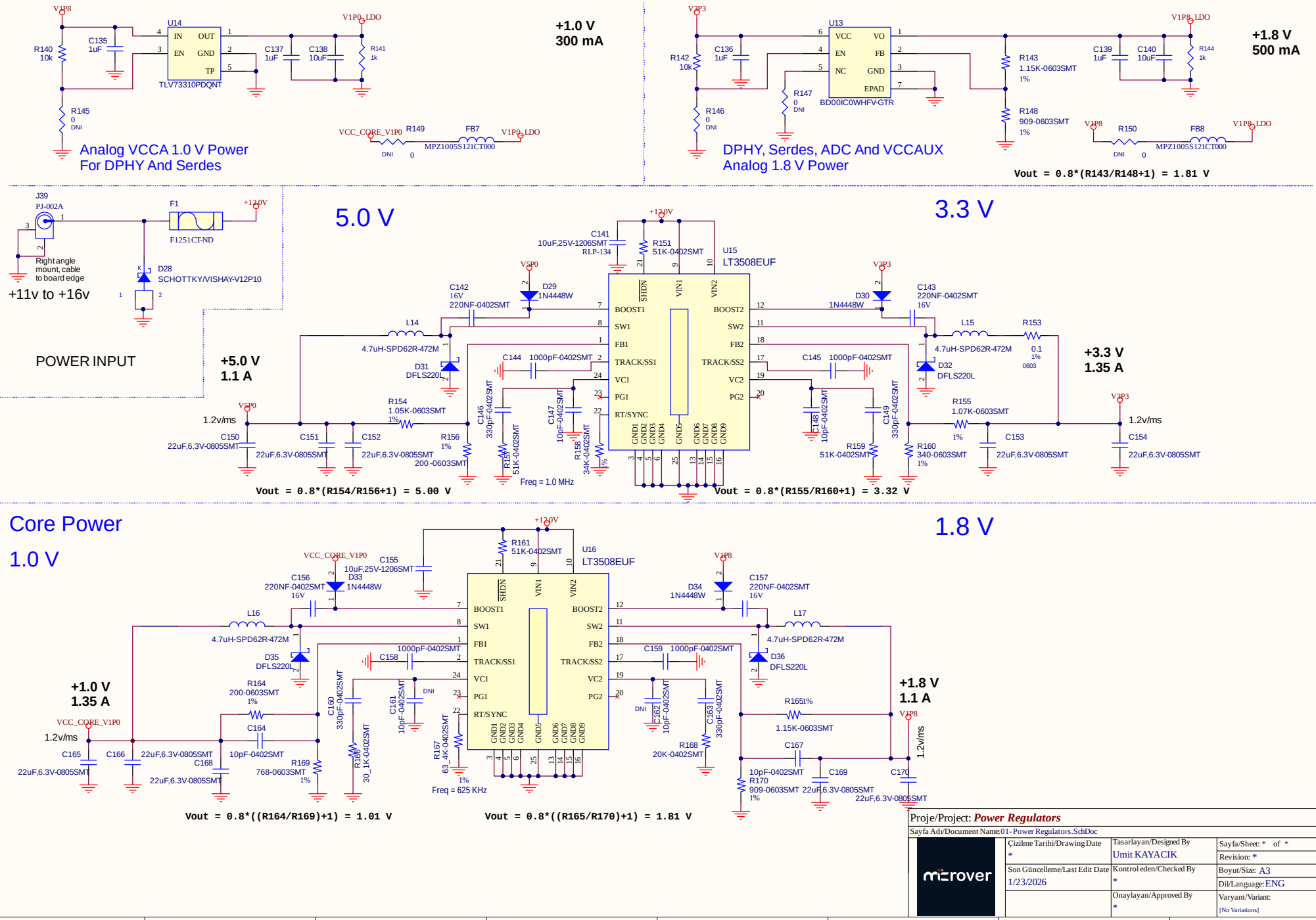
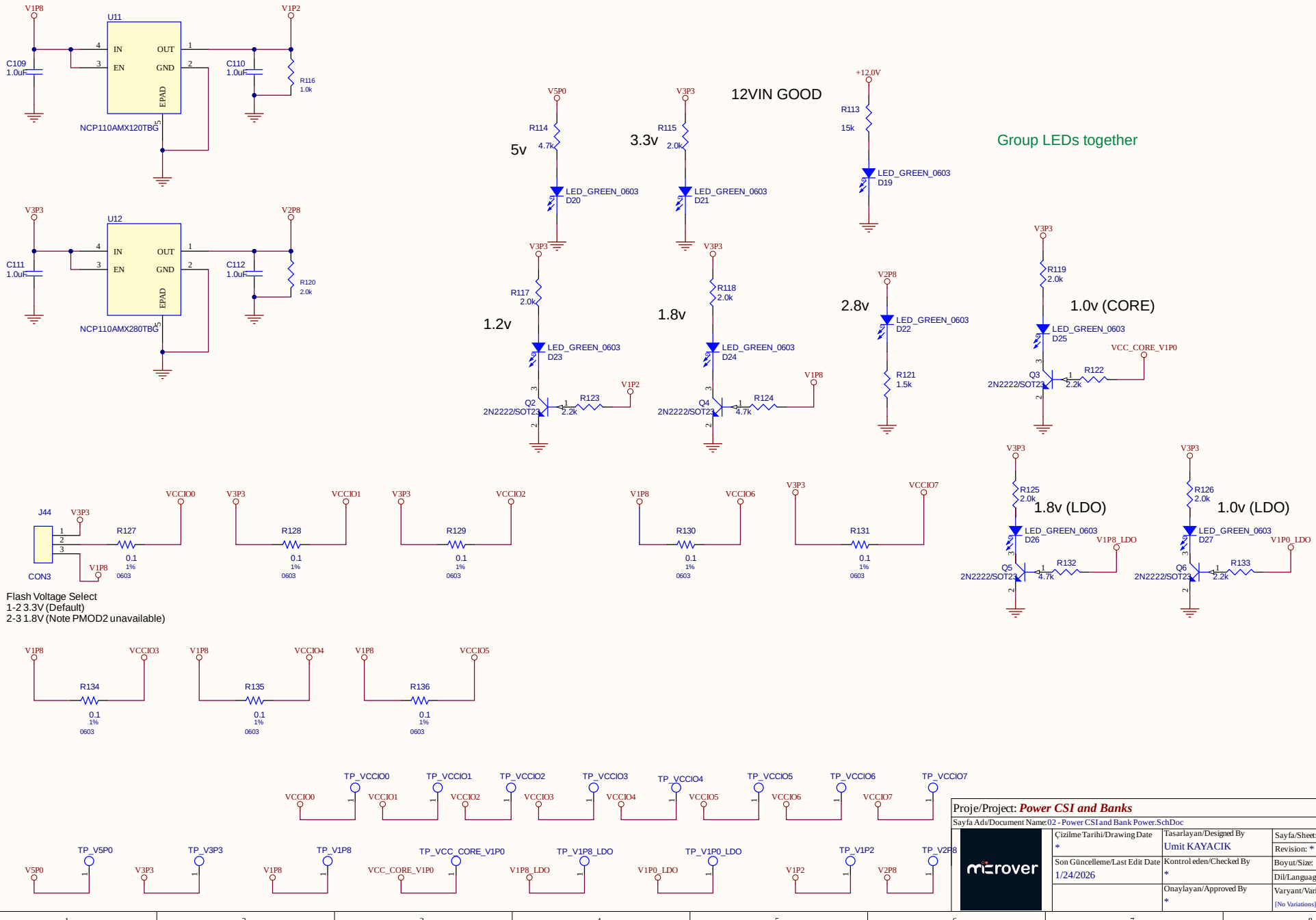
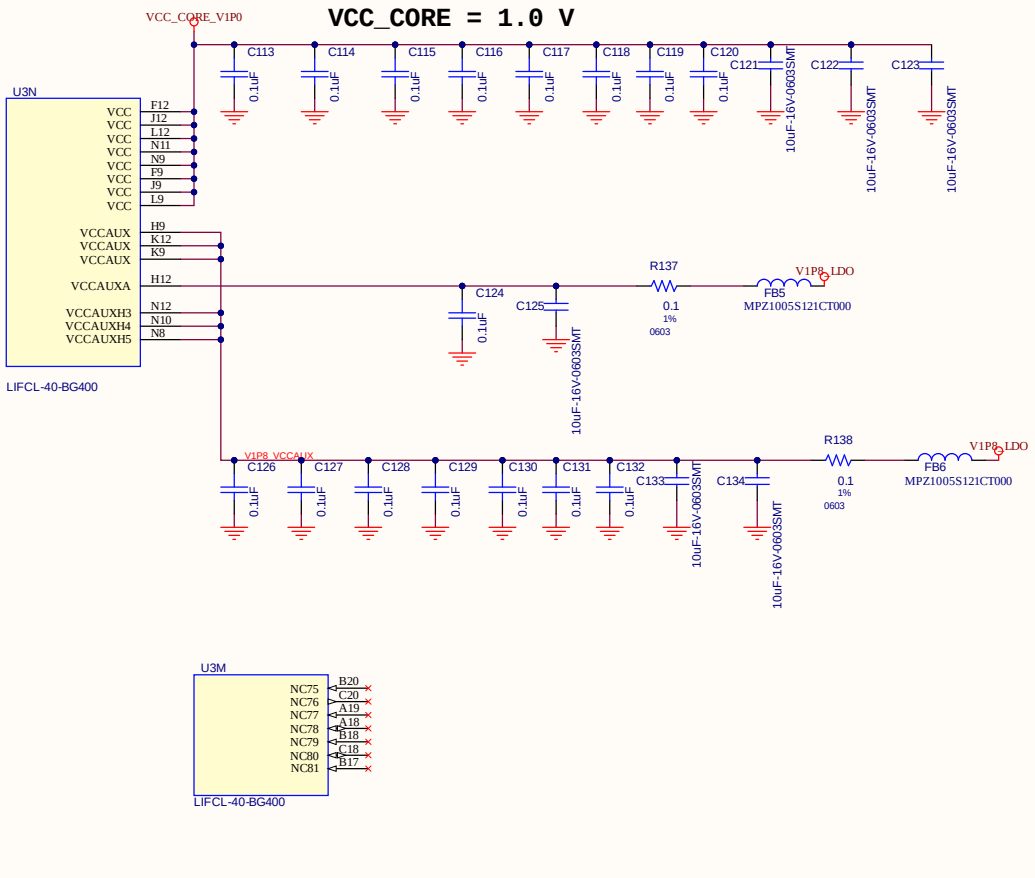

+1.0 V
300 mA
Analog VCCA 1.0 V Power
For DPHY And Serdes
+1.8 V
500 mA
DPHY, Serdes, ADC And VCCAUX
Analog 1.8 V Power
Vout = 0.8*(R143/R148+1) = 1.81 V
POWER INPUT
+11v to +16v
5.0 V
3.3 V
+5.0 V
1.1 A
+3.3 V
1.35 A
Vout = 0.8*(R154/R156+1) = 5.00 V
Vout = 0.8*(R155/R160+1) = 3.32 V
Core Power
1.0 V
1.8 V
+1.0 V
1.35 A
+1.8 V
1.1 A
Vout = 0.8*((R164/R169)+1) = 1.01 V
Vout = 0.8*((R165/R170)+1) = 1.81 V
Proje/Project: Power Regulators
Sayfa Adı/Document Name: 01- Power Regulators.SchDoc
Cizilme Tarihi/Drawing Date
Tasarlayan/Designed By
Umit KAYACIK
Sayfa/Sheet: * of *
Revision: *
Son Güncelleme/Last Edit Date
1/23/2026
Kontrol eden/Checked By
Boyut/Size: A3
Dil/Language: ENG
Onaylayan/Approved By
Varyant/Variant:
[No Variations]



Flash Voltage Select
1-2 3.3V (Default)
2-3 1.8V (Note PMOD2 unavailable)

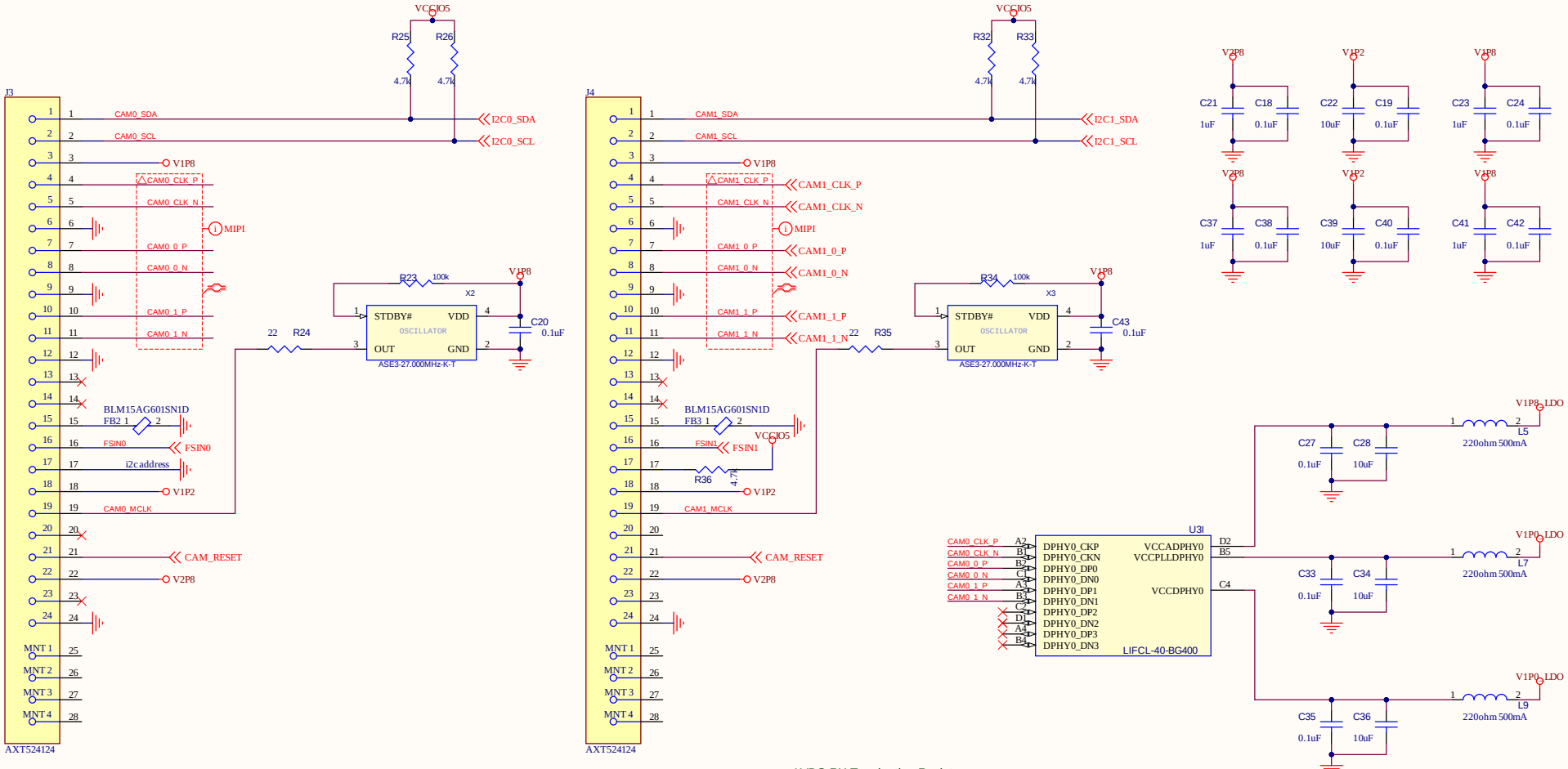
Proje/Project: ***Power CSI and Banks***			
Sayfa Adı/Document Name: 02 - Power CSI and Bank Power.SchDoc			
Çizilme Tarihi/Drawing Date: *	Tasarlayan/Designed By: Umit KAYACIK	Sayfa/Sheet: * of *	
Son Güncelleme/Last Edit Date: 1/24/2026	Kontrol eden/Checked By: *	Revision: *	
	Onaylayan/Approved By: *	Boyut/Size: A3	
		Dil/Language: ENG	
		Varyant/Variant: [No Variations]	



Proje/Project: ***Power Decoupling***

Sayfa Adı/Document Name: 03- Power Decoupling.SchDoc

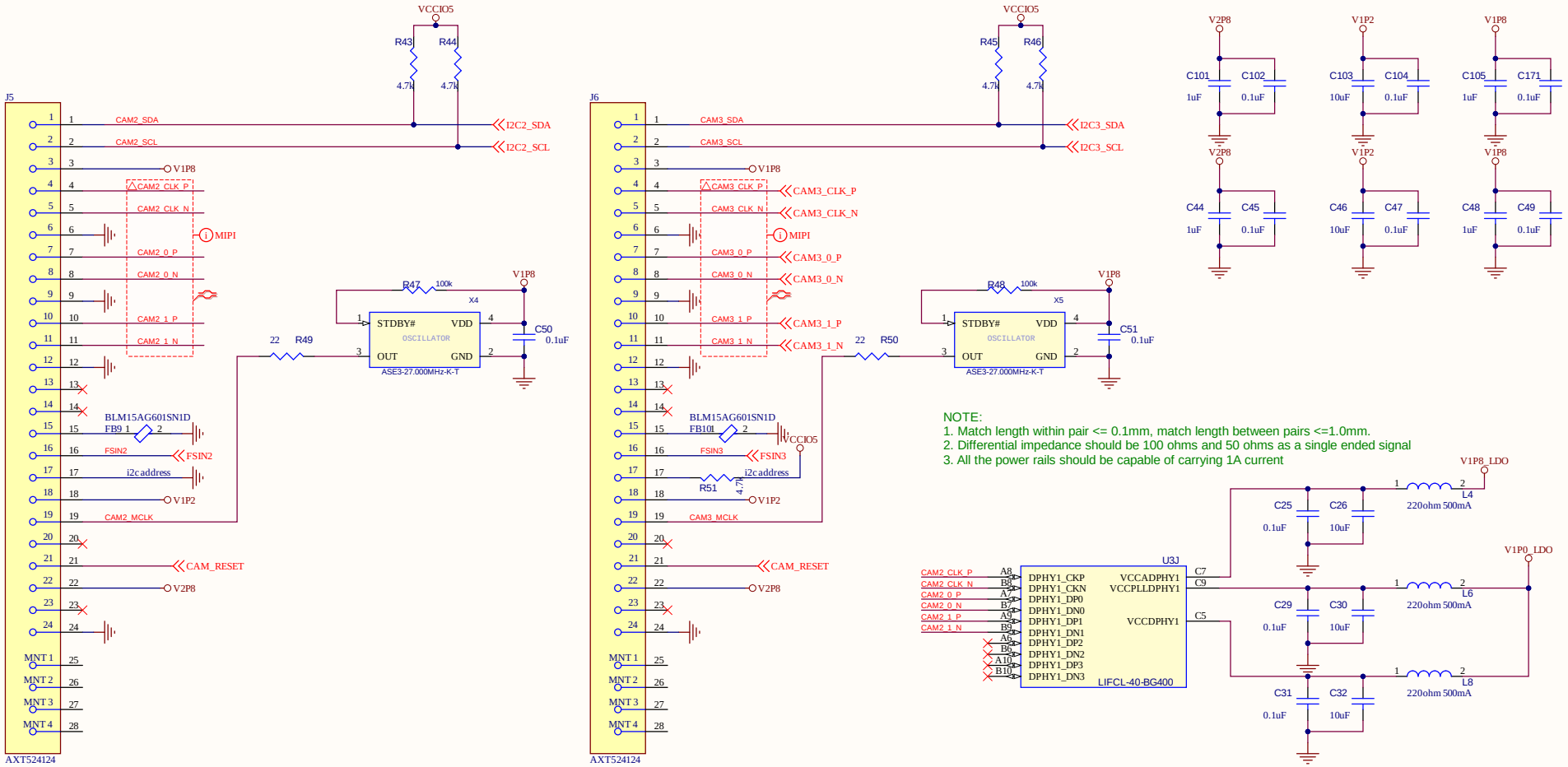
Çizilme Tarihi/Drawing Date: *	Tasarlayan/Designed By: Umit KAYACIK	Sayfa/Sheet: * of *
		Revision: *
Son Güncelleme/Last Edit Date: 1/23/2026	Kontrol eden/Checked By: *	Boyut/Size: A3
		Dil/Language: ENG
	Onaylayan/Approved By: *	Varyant/Variant: [No Variations]



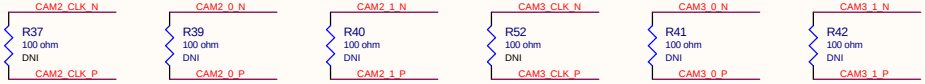
NOTE: Place close to FPGA

NOTE:
1. Match length within pair <= 0.1mm, match length between pairs <=1.0mm.
2. Differential impedance should be 100 ohms and 50 ohms as a single ended signal
3. All the power rails should be capable of carrying 1A current

Proje/Project: ***Camera Interface (DPHYs)***			
Sayfa Adı/Document Name: 04 - Camera Interface.SchDoc			
mrover	Çizilme Tarihi/Drawing Date: *	Tasarlayan/Designed By: Umit KAYACIK	Sayfa/Sheet: * of *
			Revision: *
	Son Güncelleme/Last Edit Date: 1/24/2026	Kontrol eden/Checked By: *	Boyut/Size: A3
			Dil/Language: ENG
		Onaylayan/Approved By: *	Varyant/Variant: [No Variations]



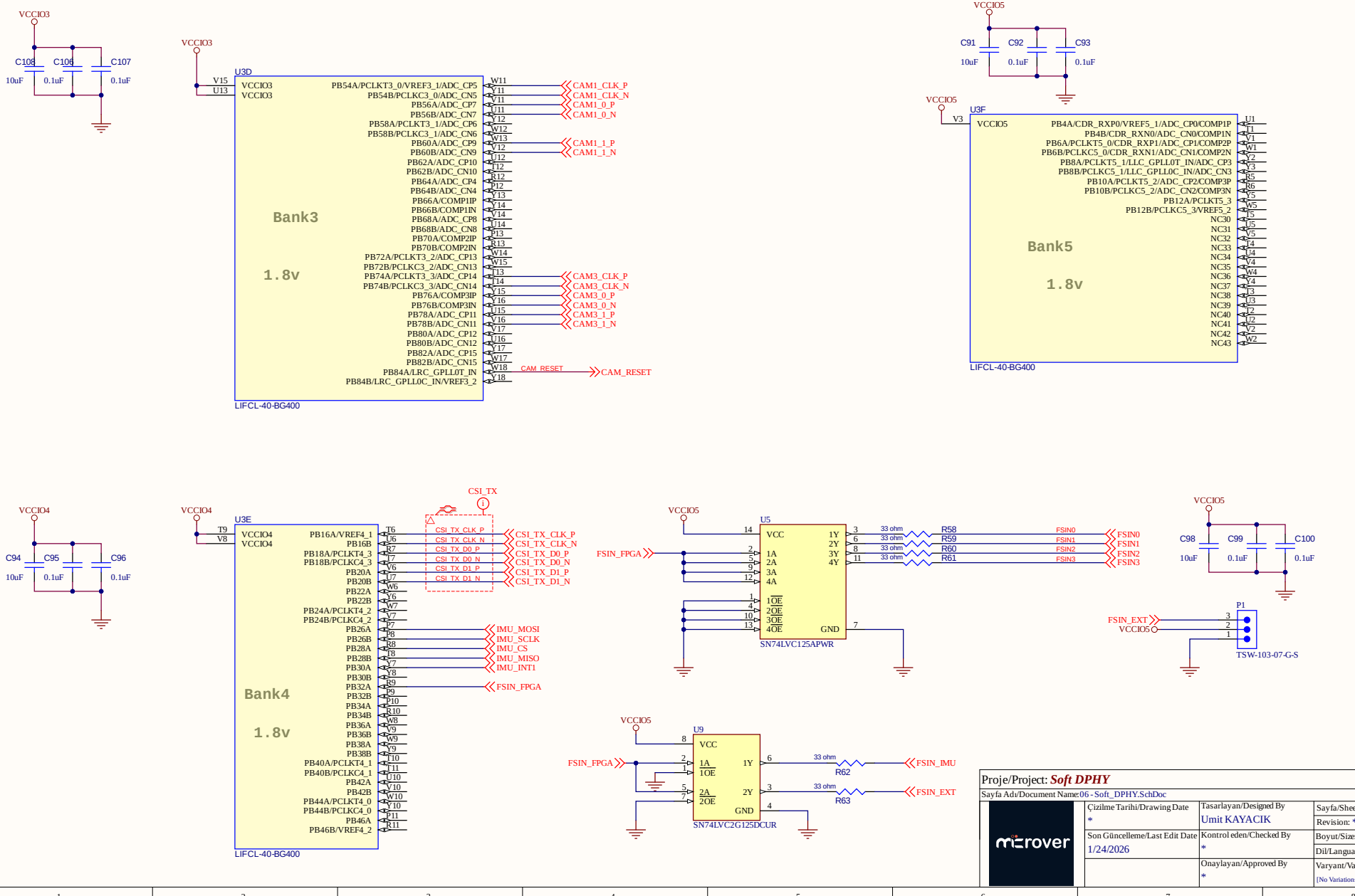
LVDS RX Termination Resistors



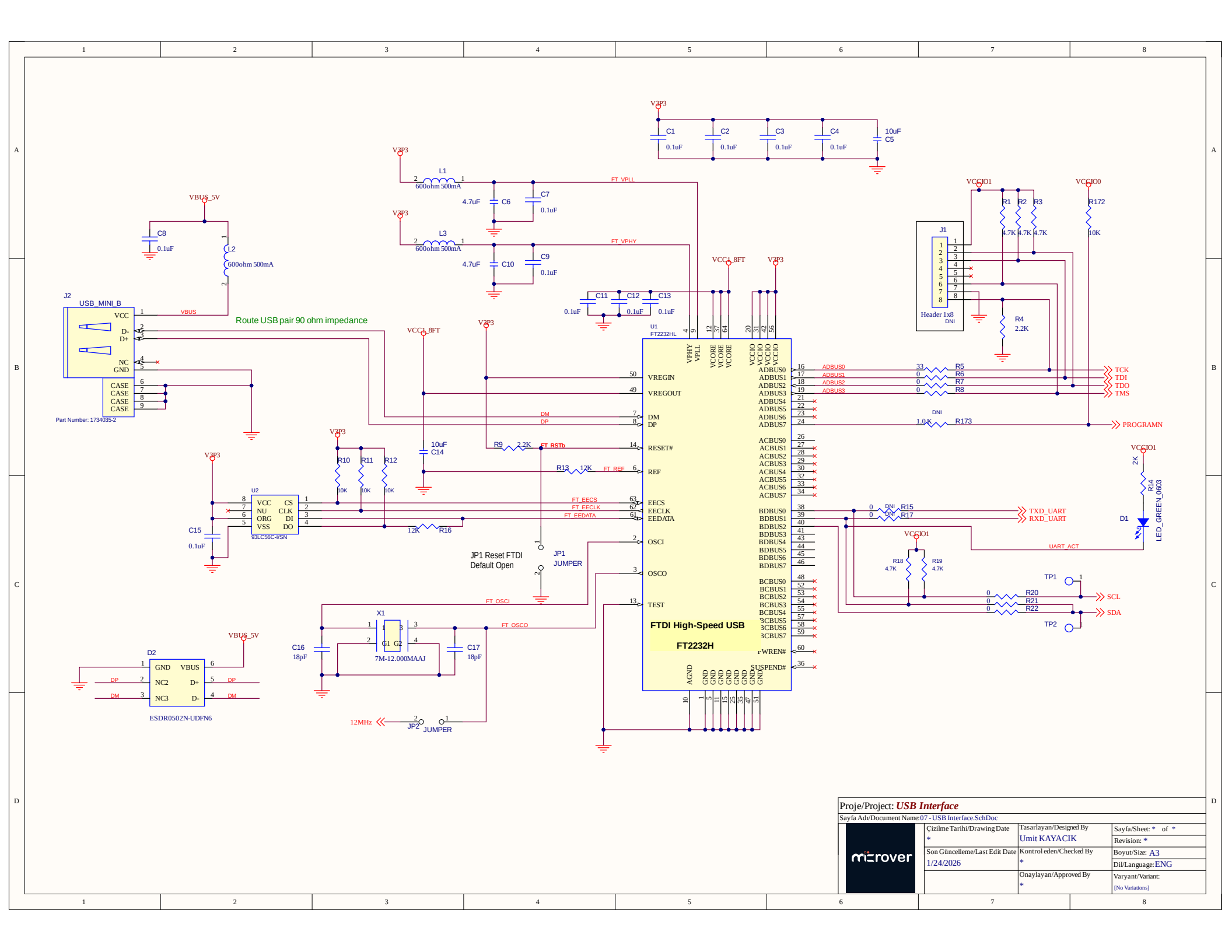
NOTE: Place close to FPGA

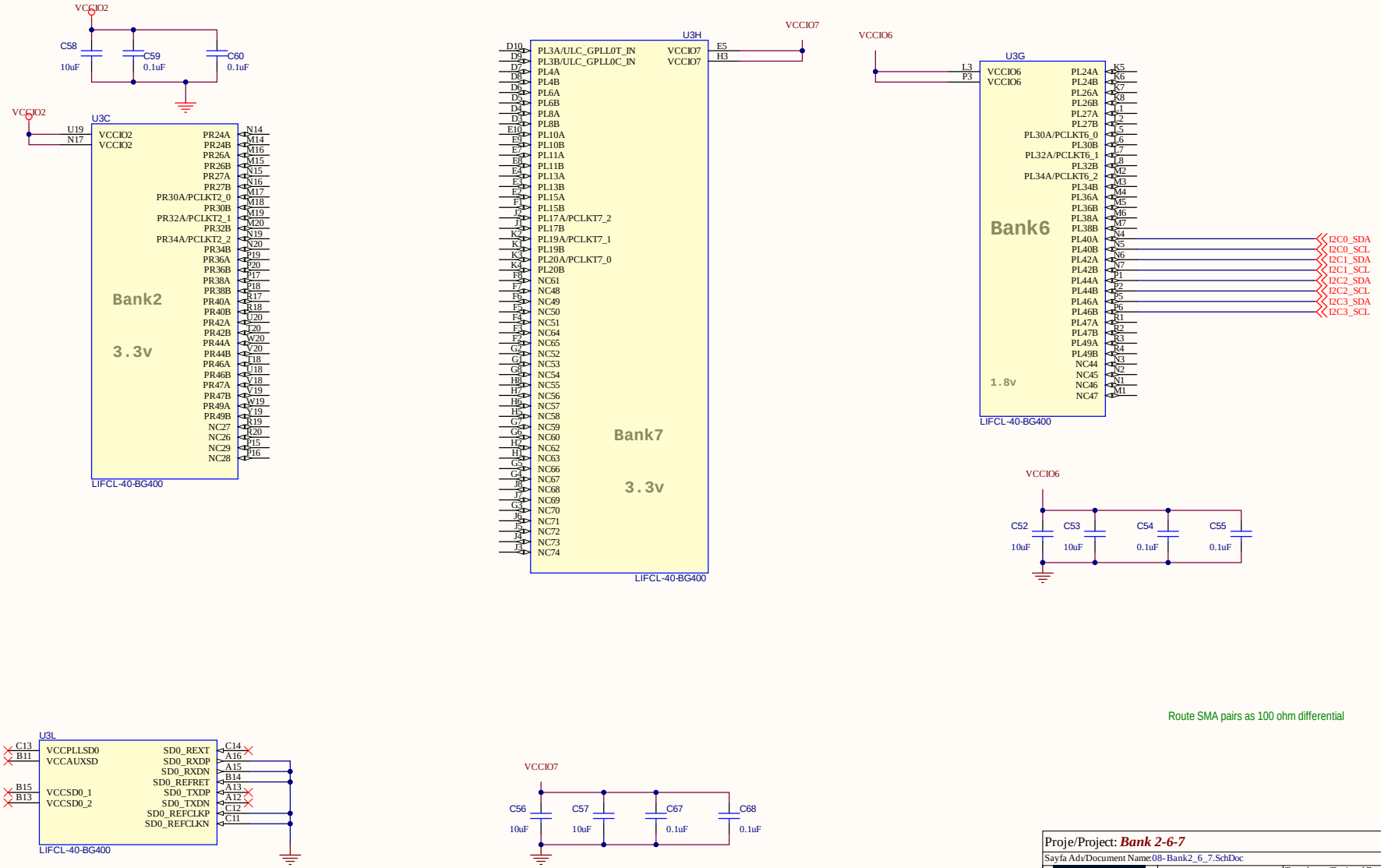
Keep LEDs away from Camera

Proje/Project: ***Camera Interface (DPHYs)***			
Sayfa Adı/Document Name: 05 - Camera Interface 2.SchDoc			
mcrover	Çizilme Tarihi/Drawing Date: *	Tasarlayan/Designed By: Umit KAYACIK	Sayfa/Sheet: * of *
			Revision: *
	Son Güncelleme/Last Edit Date: 1/24/2026	Kontrol eden/Checked By: *	Boyut/Size: A3
			Dil/Language: ENG
		Onaylayan/Approved By: *	Varyant/Variant: [No Variations]

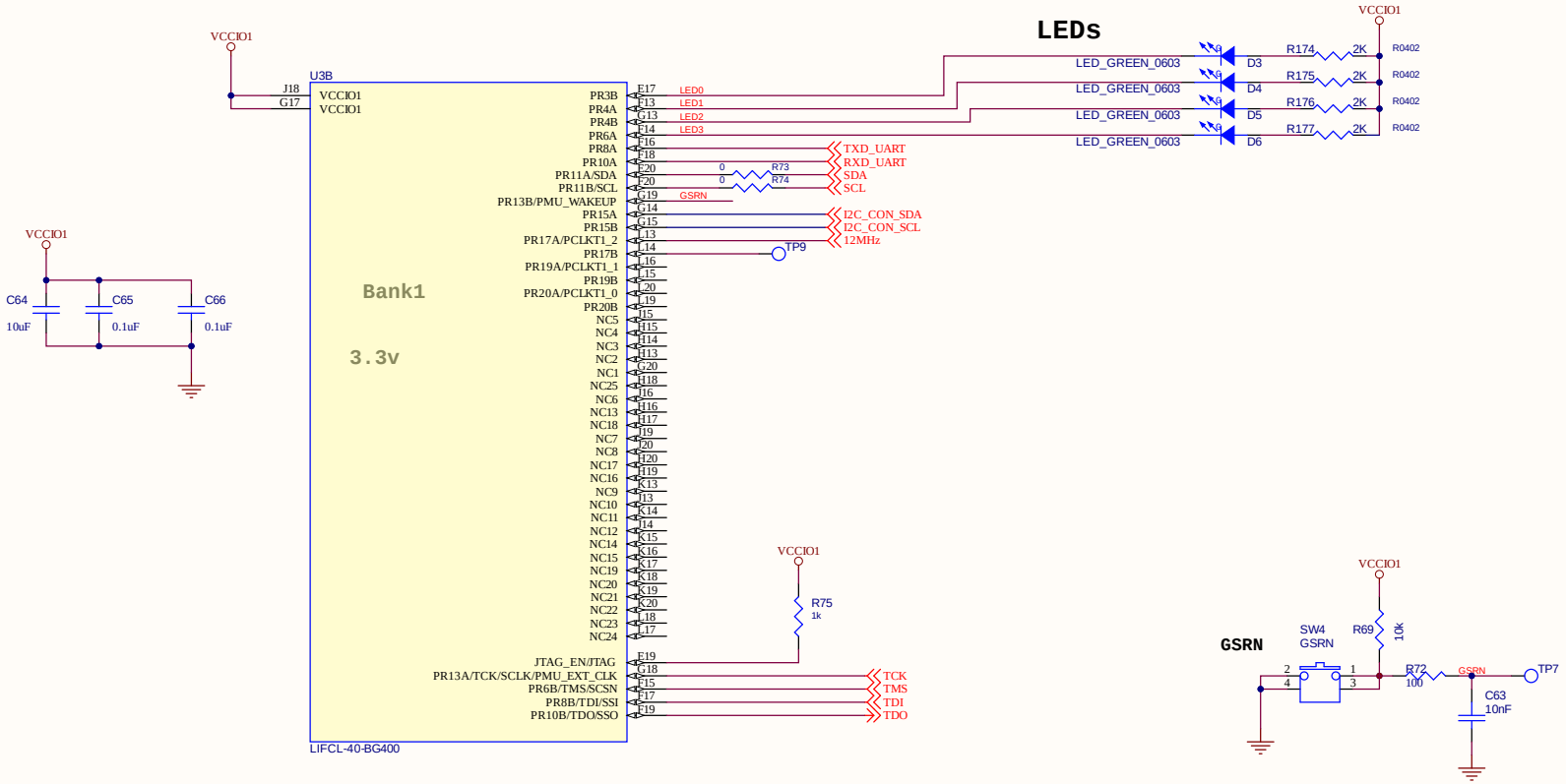


Proje/Project: ***Soft DPHY***			
Sayfa Adı/Document Name: 06 - Soft_DPHY.SchDoc			
mrover	Çizilme Tarihi/Drawing Date: *	Tasarlayan/Designed By: Umit KAYACIK	Sayfa/Sheet: * of *
			Revision: *
	Son Güncelleme/Last Edit Date: 1/24/2026	Kontrol eden/Checked By: *	Boyut/Size: A3
			Dil/Language: ENG
		Onaylayan/Approved By: *	Varyant/Variant: [No Variations]


Route USB pair 90 ohm impedance
FTDI High-Speed USB
FT2232H
JP1 Reset FTDI
Default Open
Proje/Project: USB Interface
Sayfa Adı/Document Name: 07 - USB Interface.SchDoc
Çizilme Tarihi/Drawing Date
Tasarlayan/Designed By
Umit KAYACIK
Son Güncelleme/Last Edit Date
1/24/2026
Kontrol eden/Checked By
Onaylayan/Approved By
Sayfa/Sheet:
Revision:
Boyut/Size: A3
Dil/Language: ENG
Varyant/Variant:
[No Variations]



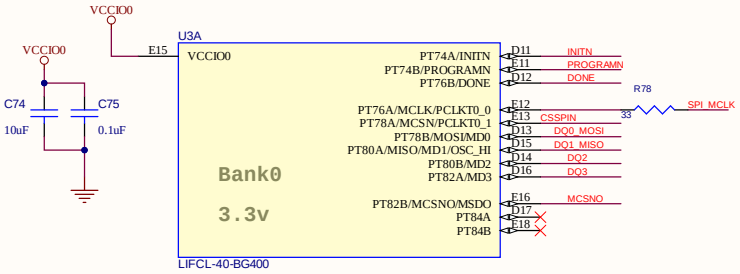
Proje/Project: ***Bank 2-6-7***			
Sayfa Adı/Document Name: 08- Bank2_6_7.SchDoc			
mrover	Çizilme Tarihi/Drawing Date: *	Tasarlayan/Designed By: Umit KAYACIK	Sayfa/Sheet: * of *
			Revision: *
	Son Güncelleme/Last Edit Date: 1/24/2026	Kontrol eden/Checked By: *	Boyut/Size: A3
			Dil/Language: ENG
		Onaylayan/Approved By: *	Varyant/Variant: [No Variations]

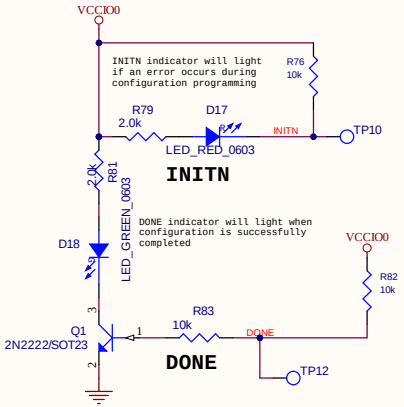


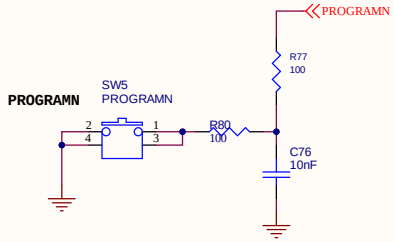
Proje/Project: ***I2C LEDs And Push Buttons***

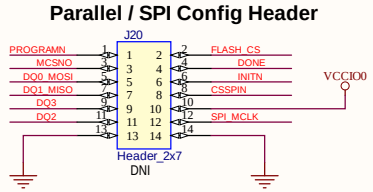
Sayfa Adı/Document Name: 09-I2C, LEDs And Push Button.SchDoc

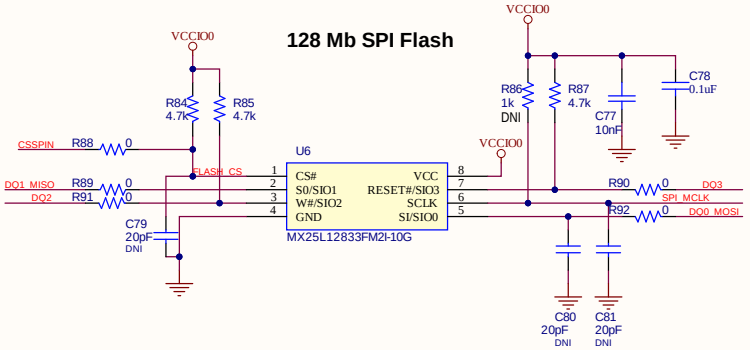
Çizilme Tarihi/Drawing Date: *	Tasarlayan/Designed By: Umit KAYACIK	Sayfa/Sheet: * of *
		Revision: *
Son Güncelleme/Last Edit Date: 1/24/2026	Kontrol eden/Checked By: *	Boyut/Size: A3
		Dil/Language: ENG
	Onaylayan/Approved By: *	Varyant/Variant: [No Variations]

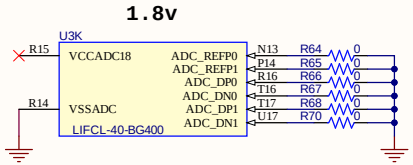






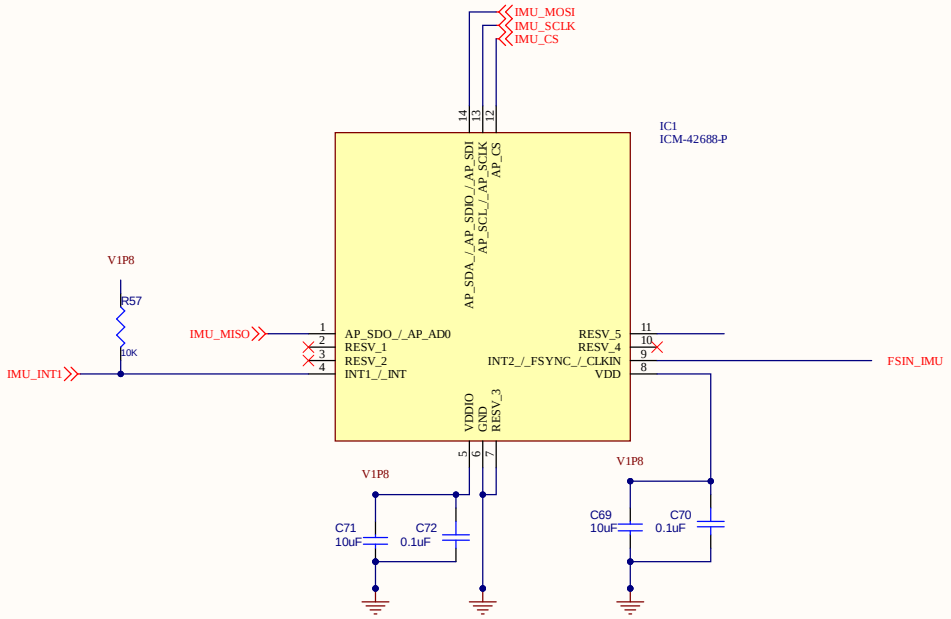






Keep noisy signals away from ADC circuit

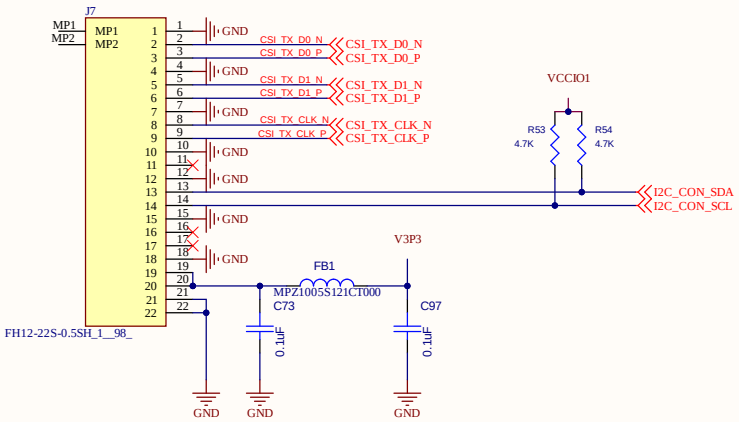
Proje/Project: ***Configuration and ADC***		
Sayfa Adı/Document Name: 10 - Configuration And ADC.SchDoc		
Çizilme Tarihi/Drawing Date: *	Tasarlayan/Designed By: Umit KAYACIK	Sayfa/Sheet: * of *
		Revision: *
Son Güncelleme/Last Edit Date: 1/24/2026	Kontrol eden/Checked By: *	Boyut/Size: A3
		Dil/Language: ENG
	Onaylayan/Approved By: *	Varyant/Variant: [No Variations]



Proje/Project: ***IMU***

Sayfa Adı/Document Name: 11-IMU.SchDoc

Çizilme Tarihi/Drawing Date: *	Tasarlayan/Designed By: Umit KAYACIK	Sayfa/Sheet: * of *
		Revision: *
Son Güncelleme/Last Edit Date: 1/23/2026	Kontrol eden/Checked By: *	Boyut/Size: A3
		Dil/Language: ENG
	Onaylayan/Approved By: *	Varyant/Variant: [No Variations]



Proje/Project: ***JETSON-CON***			
Sayfa Adı/Document Name: 12 - JETSON_CON.SchDoc			
	Çizilme Tarihi/Drawing Date *	Tasarlayan/Designed By Umit KAYACIK	Sayfa/Sheet: * of *
			Revision: *
	Son Güncelleme/Last Edit Date 1/24/2026	Kontrol eden/Checked By *	Boyut/Size: A3
			Dil/Language: ENG
		Onaylayan/Approved By *	Varyant/Variant: [No Variations]