TSF Library - ATMLDemo2DigitalPatterns

Schema Name:- ATMLDemo2DigitalPatterns
Version:- 0.1
Schema Location:- ATMLDemo2DigitalPatterns.xsd
namespace:- ATMLDemo2DigitalPatterns
prefix:- this
Description:-
Set of digital patterns for use with ATML demo

- InitTest1
- D00
- DFF
- D80

InitTest1

Definition

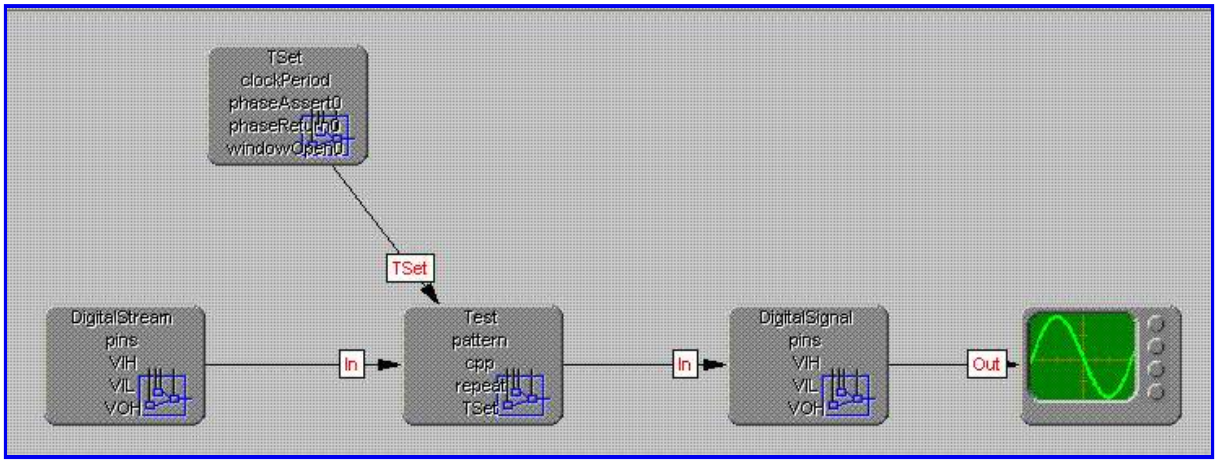

Figure 1-TSF InitTest1(InitTest1)

Interface Properties

Table 1-TSF InitTest1 Interface

Description	Name	Type	Default	Range

Notes

Model Description

Table 2-TSF InitTest1 Model

Name	Type	Terminal	Inputs	Output	Formula
DigitalSignal_4049	DigitalSignal	Signal [Out]			
		pins	data [d0,d1,d2,d3,d4,d5,d6,d7]		
		VIH			5 V
		VIL			0 V
		VOH			2.4 V
		VOL			0.5 V
		IOH			-0.4 mA
		IOL			8 mA
		VCom			1.5 V
		Signal [In]	Test_4057		

Test_4057	Test	Signal [Out]		DigitalSignal_4049	
		pattern	IH data[xA5]		
		cpp			1
		repeat			1
		delay			0 ns
		Signal [In]	DigitalStream_4040		
TSet_4059	TSet	Signal [Out]			
		clockPeriod			1000 ns
		phaseAssert0			0 ns
		phaseReturn0			25 ns
		windowOpen0			10 ns
		windowClose0			20 ns
DigitalStream_4040	DigitalStream	Signal [Out]		Test_4057	
		channels	[0,1,2,3,4,5,6,7]		
		pins	data [d0,d1,d2,d3,d4,d5,d6,d7]		
		VIH			5 V
		VIL			0 V
		VOH			2.4 V
		VOL			0.5 V
		IOH			-0.4 mA
		IOL			8 mA
		VCom			1.5 V
		impedance			50Ohm
		format	NRet		
		phase			0
		window			0
		capture	Window		

Rules

D00

Definition

Writes out 0x00 D7-0

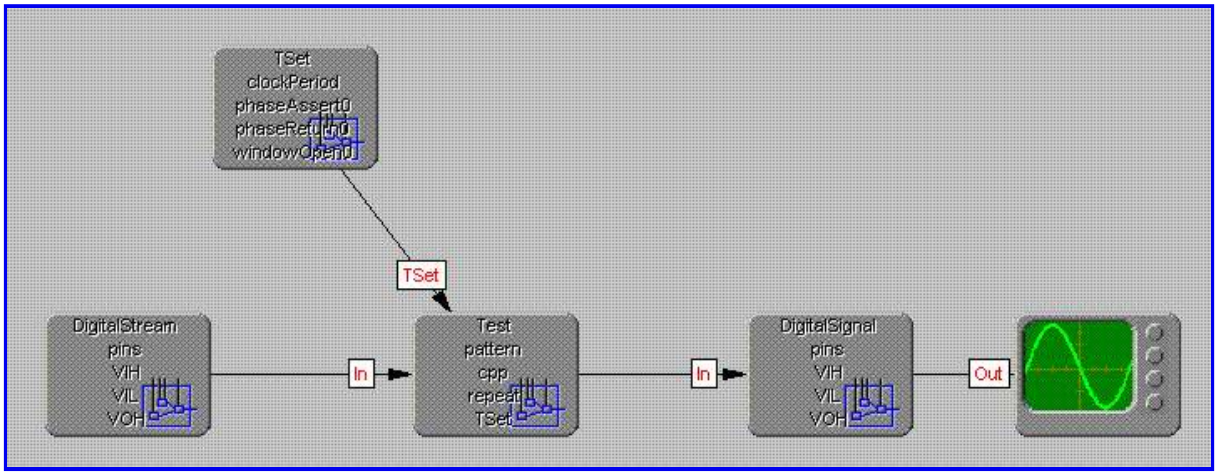

Figure 2-TSF D00(D00)

Interface Properties

Table 3-TSF D00 Interface

Description	Name	Type	Default	Range

Notes

Model Description

Table 4-TSF D00 Model

Name	Type	Terminal	Inputs	Output	Formula
DigitalSignal_4068	DigitalSignal	Signal [Out]			
		pins	data [d7, d6, d5, d4, d3, d2, d1, d0]		
		VIH			5 V
		VIL			0 V
		VOH			2.4 V
		VOL			0.5 V
		IOH			-0.4 mA
		IOL			8 mA
		VCom			1.5 V
		Signal [In]	Test_4076		
Test_4076	Test	Signal [Out]		DigitalSignal_4068	
		pattern	IH data[x00]		
		cpp			1
		repeat			1
		delay			0 ns
		Signal [In]	DigitalStream_4078		
TSet_4087	TSet	Signal [Out]			
		clockPeriod			1000 ns
		phaseAssert0			0 ns
		phaseReturn0			25 ns
		windowOpen0			10 ns
		windowClose0			20 ns
DigitalStream_4078	DigitalStream	Signal [Out]		Test_4076	
		channels	[7,6,5,4,3,2,1,0]		
		pins	data [d7, d6, d5, d4, d3, d2, d1, d0]		
		VIH			5 V
		VIL			0 V
		VOH			2.4 V
		VOL			0.5 V
		IOH			-0.4 mA
		IOL			8 mA
		VCom			1.5 V
		impedance			50Ohm
		format	NRet		
		phase			0
		window			0
		capture	Window		

Rules

DFF

Definition
Writes out 0xFF D7-0

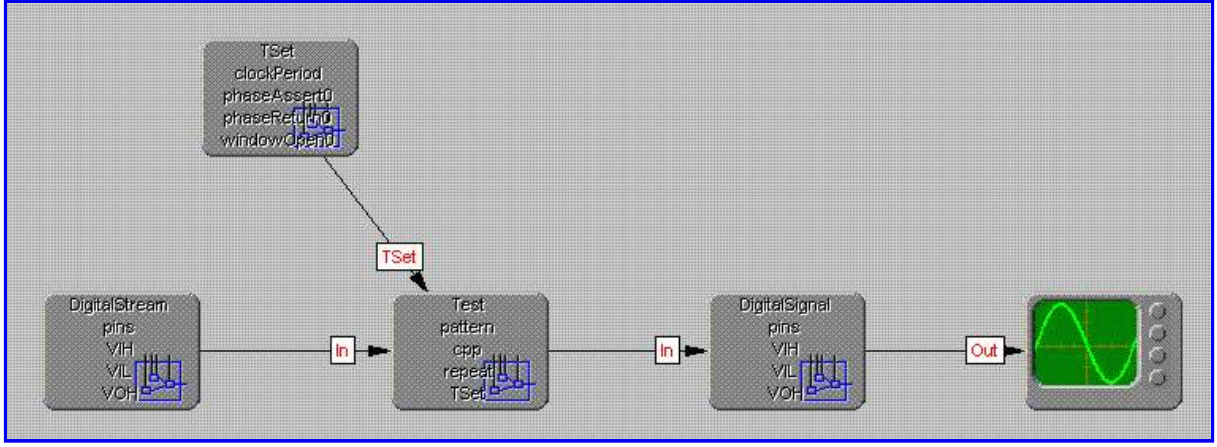

Figure 3-TSF DFF(DFF)

Interface Properties

Table 5-TSF DFF Interface

Description	Name	Type	Default	Range

Notes

Model Description

Table 6-TSF DFF Model

Name	Type	Terminal	Inputs	Output	Formula
DigitalSignal_4096	DigitalSignal	Signal [Out]			
		pins	data [d7, d6, d5, d4, d3, d2, d1, d0]		
		VIH			5 V
		VIL			0 V
		VOH			2.4 V
		VOL			0.5 V
		IOH			-0.4 mA
		IOL			8 mA
		VCom			1.5 V
		Signal [In]	Test_4119		
Test_4119	Test	Signal [Out]		DigitalSignal_4096	
		pattern	IH data[xFF]		
		cpp			1
		repeat			1
		delay			0 ns
		Signal [In]	DigitalStream_4110		
TSet_4104	TSet	Signal [Out]			
		clockPeriod			1000 ns
		phaseAssert0			0 ns
		phaseReturn0			25 ns
		windowOpen0			10 ns
		windowClose0			20 ns
DigitalStream_4110	DigitalStream	Signal [Out]		Test_4119	
		channels	[7,6,5,4,3,2,1,0]		
		pins	data [d7, d6, d5, d4, d3, d2, d1, d0]		
		VIH			5 V

		VIL			0 V
		VOH			2.4 V
		VOL			0.5 V
		IOH			-0.4 mA
		IOL			8 mA
		VCom			1.5 V
		impedance			50Ohm
		format	NRet		
		phase			0
		window			0
		capture	Window		

Rules

D80

Definition
Writes out 0x80 D7-0

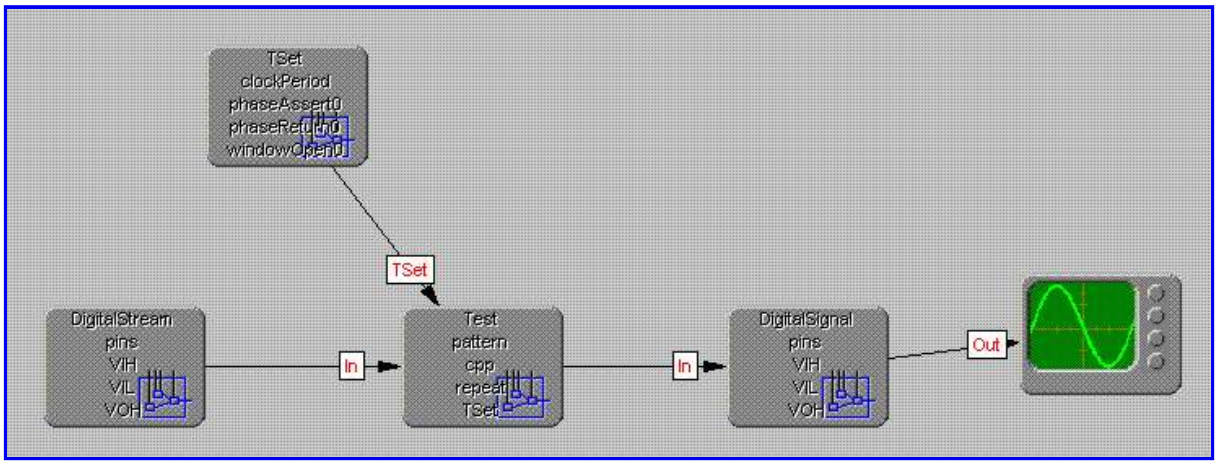

Figure 4-TSF D80(D80)

Interface Properties

Table 7-TSF D80 Interface

Description	Name	Type	Default	Range

Notes

Model Description

Table 8-TSF D80 Model

Name	Type	Terminal	Inputs	Output	Formula
DigitalSignal_4132	DigitalSignal	Signal [Out]			
		pins	data [d7, d6, d5, d4, d3, d2, d1, d0]		
		VIH			5 V
		VIL			0 V
		VOH			2.4 V
		VOL			0.5 V
		IOH			-0.4 mA

		IOL			8 mA
		VCom			1.5 V
		Signal [In]	Test_4130		
Test_4130	Test	Signal [Out]		DigitalSignal_4132	
		pattern	IH data[x80]		
		cpp			1
		repeat			1
		delay			0 ns
		Signal [In]	DigitalStream_4140		
TSet_4124	TSet	Signal [Out]			
		clockPeriod			1000 ns
		phaseAssert0			0 ns
		phaseReturn0			25 ns
		windowOpen0			10 ns
		windowClose0			20 ns
DigitalStream_4140	DigitalStream	Signal [Out]		Test_4130	
		channels	[7,6,5,4,3,2,1,0]		
		pins	data [d7, d6, d5, d4, d3, d2, d1, d0]		
		VIH			5 V
		VIL			0 V
		VOH			2.4 V
		VOL			0.5 V
		IOH			-0.4 mA
		IOL			8 mA
		VCom			1.5 V
		impedance			50Ohm
		format	NRet		
		phase			0
		window			0
		capture	Window		

Rules