Forth Capstone Project Design Magnitude Idaho

Design and implement a Forth Computer

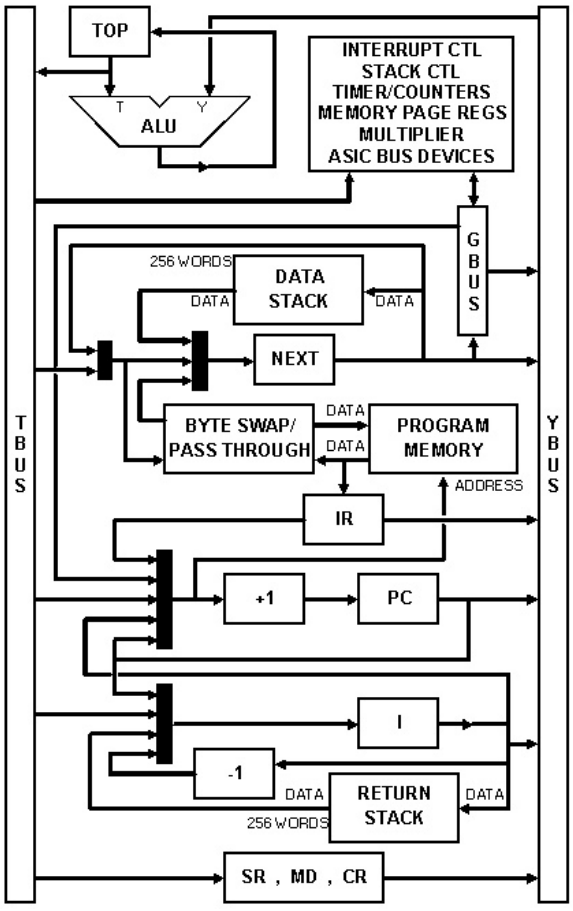
Develop an Arduino-like board/platform based upon an FPGA executing FORTH bytecode instructions. The board will support the ability to connect Arduino shields.

The user interface (software) will be a REPL (Read-Eval-Print Loop) to enable user interaction with the hardware.

Background

FORTH is a very small programming language that was originally developed for controlling scientific instrumentation.

The architecture is illustrated in the following diagram:



Design Requirements

- Hardware Tasks
  - FORTH CPU Design
    implemented in an FPGA using Verilog code
    - test bench for sub-blocks
    - test vectors
  - Memory
    - internal to FPGA?
    - external SRAM?
  - I/O
    - serial console
    - buttons (4?)
    - LEDs (8?)
    - other? (FLASH, I2C, SPI, Display Mouse, Keyboard, . . .)
  - Power Supply
  - PCB Design
- Software Tasks
  - FORTH Interpreter development (Raspberry Pi 4)
    to enable comparison/verifificaton of the Hardware CPU
  - FORTH OS/REPL (Read-Eval-Print Loop) that runs on the FORTH computer

Deliverables

- FORTH-board
- Verilog code for FORTH CPU implemented on an FPGA
- FORTH Interpreter (Raspberry Pi 4 and FORTH-board)
- FORTH OS/REPL