FORTH COMPUTING ON FPGA

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Objective

Develop an Arduino-like board/platform based upon an FPGA executing FORTH bytecode instructions.

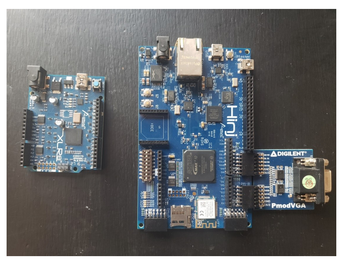
Background

FORTH is a very small programming language that was originally developed for controlling scientific instrumentation.

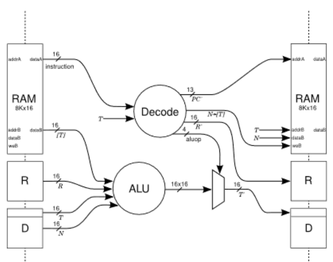
A custom designed soft-CPU that executes FORTH instructions on an FPGA is a very versatile, low power, and small form factor way to accomplish many computing tasks.

Our design, called the F18, is ideal for applications with many arithmetic calculations, high data throughput, or as a controller for designs with other subsystems.

Concept Development



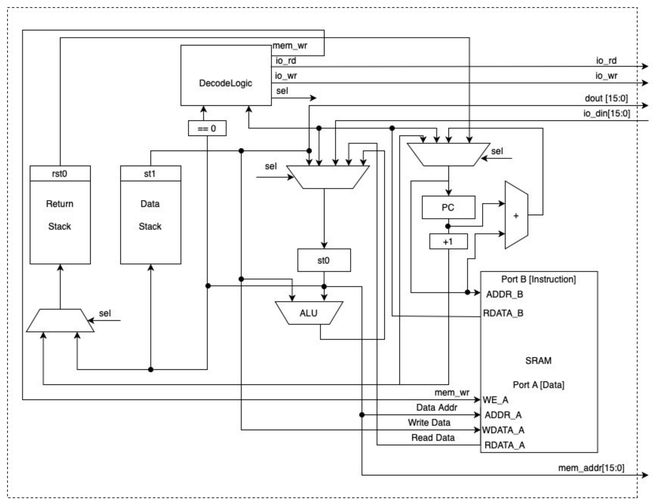
Several development boards were used for this project, with the Alorium Hinj being the final choice due to the convenient features and easy expansion.



The J1, an FPGA based Forth CPU created by James Bowman, served as inspiration for the project.

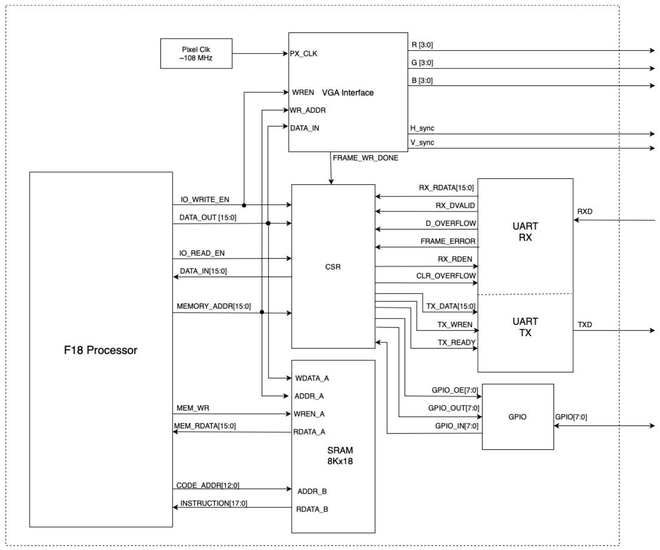
Final Design

F18 Processor

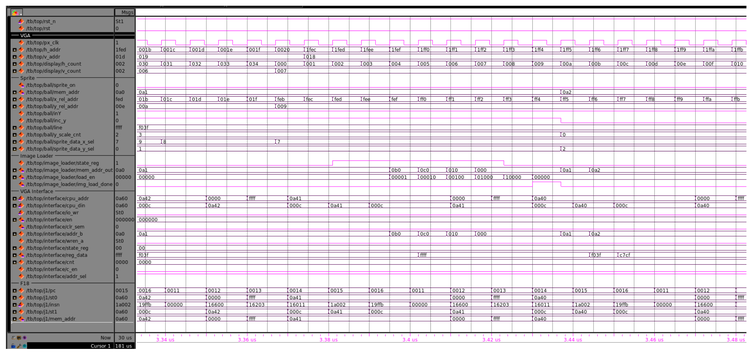


- Designed specifically for running FORTH
- Two RAM based LIFO stacks
  - Data Stack: Data manipulation and calculation
  - Return Stack: Stores return address for function calls
- 18-bit instruction width, 16-bit data paths
- Uses true dual port SRAM for data and program storage
- 16 MHz clock
- UART (Universal Asynchronous Trans./Rec.)
  - Allows for serial communication with external devices
- VGA (Video Graphics Array)
  - Allows for display on VGA monitor
  - Specifically designed for displaying Pong game
- GPIO (General Purpose I/O)
  - Allows for input and output to/from physical pins on board
- CSR (Control/Status Registers)
  - Coordinates data flow between I/O peripherals and F18 processor

System Input/Output



Testing and Validation



Logic analyzer waveforms were used very regularly to observe the functionality of different design elements. This shows sprite data being loaded from RAM to an internal register to be later drawn to the screen.

Going Forward

Throughout the year this project changed and grew. Our final design met the specifications of a CPU on an FPGA that executes FORTH instructions, and was geared toward running the pong program on the custom F18 processor. Moving forward these are some things we would like to implement and add:

- Full ANS FORTH on the board
- Arduino like tools/functions
- Hardware interrupts
- Prototype custom PCB

Acknowledgements

Thanks to Peter Baran for being a sponsor, mentor and teacher. Thanks to Mark Sapper for his help with hardware design and debugging. Thanks to James Bowman for allowing us to use his J1 core design. Thanks to Bruce Bolden for being the lead instructor throughout this project.

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