**Minutes (Sep 17 at 12:30) by Thys Ballard**

Kyle Hild was unable to attend today

Budget writing will happen once we talk with Peter.

Kyle Hartman will do minutes next week and Jess will do the agenda.

We are tentatively moving meetings to Thursdays at 3:30. We will meet at the Think Tank.

We need to brainstorm questions for Peter.

I will set up a Trello and Discord tonight and send out links.

Kyle sent out an email to Peter setting up a meeting for Sept 18 at 3:30 or Sept 19 at 3:30 in the Think Tank

**Meeting Minutes 9/26**

* Want to create a minutes/agenda template for future meetings
  + Thys
* Turn in the budget ASAP
* Get working on the product requirements
  + Create a google doc
  + Jess will create and start work on it
* Start installing software on rpi so we can clone and see what all we need
  + sudo apt install iverilog verilator gtkwave
* Someone should contact Peter replying to his email about video meetings and stuff
  + Kyle Hild
* Snapshot day 1 goals – by 10th
  + Custom hardware running on FPGA
  + Get J1 core running on FPGA
  + Custom FORTH applications/compiler/interpreter
  + Basically get good at FORTH
  + Have rpi workstations up and running
* Send Bruce an email about what is actually meant by “Due: client visit & interview w/lead instructor
* Learn how to use GIT at least the basics
* Git Kraken Glowboards for project planning/whatever – AGILE
  + Backlog, doing, to do, done
* Thys will send a thing about what we need to do to be AGILE
  + SCRUM and how we want to have our team organized.
  + Best Practices type stuff
  + SCRUM and xp from the trenches (book)
* Read more about the J1 core
* Modify team contract
* WRITE IN LOG BOOKS

**Notes From Meeting 2:**

* I am the primary contact for communication with Peter.

**To Do:**

* Learn a little more about AGILE
* Get a log book
* Continue Project Learning

**Minutes Taker: Thys Ballard**

**Date: October 3, 2019**

**Time: 3:30**

* Kyle Hartman did not attend today.
* Peter says we should figure out what we need to do next.
* James Bowman, who designed the J1 Forth chip, is on board for 8-10 hours of design review.
* Peter mentioned that modern FPGAs now have 18 bits instead of 16 bits.
* We need to get our toolchain working first.
* Jess will work on the block diagram for the serial port and getting it made.
* Kyle and Thys will work on getting a compiler started.
* We will all brush up on Forth
* By next Thursday we need to have a serial port design and blocks diagrams of the stack so that we can have time to work on the poster.
* We will probably also want on the poster what makes Forth different.
* Jess will have time at 11:30 on Friday.
* We are planning to meet on Saturday at around 11:00.
* We will push off the compiler design for the J1 until after the poster.
* The guy at FORTH, Inc. told Peter that the 3rd weekend of November will be FORTH week at Stanford University. One of us could probably go but it may not be worth

**Meeting Minutes 10/10/19**

* In Attendance: All Members
* Use J1 core
* Work on learning Arduino for shield
* Possible Product Requirements
  + Core Requirements
    - Arduino shield compatible
    - USB Port
    - Forth Compiler/Interpreter
    - Serial Port
    - Put it on PCB
    - REPL on rspi
    - Memory External/Internal
  + Stretch Goals
    - TCP/IP stack
    - Net Hack
    - Run Doom – Graphics stack
* Meet at 1pm on Sunday (Drone Lab), work on poster board and snapshot presentation
* Need to work on instructions set for J1
* Design peripherals, PCB
* Make project schedule on Sunday
* Make google drive for design portfolio – Jess
* Draft a project schedule – Kyle Hartman

**To Do:**

* Continue Project Learning
* Meeting Minutes Template (Realizing we are not hitting all the goals)
* Work on portfolio

**Meeting Minutes 10/13/19**

* All in attendance
* This was a meeting to prepare for the Snapshot Day 1 on the 15th.
* We had a video conference with Peter
* Spoke about the REPL loop diagram in chapter 8
  + Kyle Hild will start working on this in C (A Simulation)?
* Jess & Kyle Hartman was working on the J1
* Got the J1 to run an add instruction
* Worked on Snapshot Power-point slides
  + What Makes FORTH different?
  + Why FORTH
  + A little about how FORTH Works





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|  | **Name:** | Jess Totorica | | |  |  | **Date:** | 10/31/19 |
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| **Weekly Action Items** | | | | | | | | |
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| 1 | Continue working on J1a core, implement on Hin | | | | | | | |
| 2 | Start working on emulator | | | | | | | |
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| **Summary of Progress** | | | | | | | | |
| J1a core has been organized and instantied on top level file. We now have ability to load SRAM and feed instructions to the J1 core. | | | | | | | | |
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| **Meeting Attendance:** | | | |  | **Was Meeting Helpful?** | | Yes |  |
| **Name:** | | **P** | **NP** |  |  |  |  |  |
| Kyle Hartman: | | x |  |  | **If No Why?** | | | |
| Thys Ballard: | | x |  |  |  | | | |
| Jess Totorica: | | x |  |  |
| Kyle Hild | | x |  |  |
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| **Team Member Contributions:** | | | | | | | | |
| Kyle Hartman: | |  | | | | | | |
| Thys Ballard: | | Need to start working J1 core | | | | | | |
| Jess Totorica: | | UART Transmitter is up and working | | | | | | |
| Kyle Hild: | |  | | | | | | |
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|  | **Name:** | Kyle Hartman | | |  |  | **Date:** | 14-Nov |
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| **Weekly Action Items** | | | | | | | | |
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| 1 | Meeting on Sunday at 11am in the drone lab | | | | | | | |
| 2 | Get a design review time slot - Email Bruce | | | | | | | |
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| **Summary of Progress** | | | | | | | | |
| Implemented J1 on the Hinj board and got some tests running with the UART. | | | | | | | | |
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| **Meeting Attendance:** | | | |  | **Was Meeting Helpful?** | | Yes |  |
| **Name:** | | **P** | **NP** |  |  |  |  |  |
| Kyle Hartman: | | x |  |  | **If No Why?** | | | |
| Thys Ballard: | | x |  |  | Regrouping and planning the next steps. Concept Design Review | | | |
| Jess Totorica: | | x |  |  |
| Kyle Hild | | x |  |  |
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| **Team Member Contributions:** | | | | | | | | |
| Kyle Hartman: | | Stepper Motor PMOD | | | | | | |
| Thys Ballard: | |  | | | | | | |
| Jess Totorica: | |  | | | | | | |
| Kyle Hild: | |  | | | | | | |
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