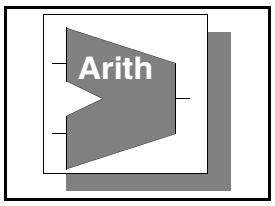
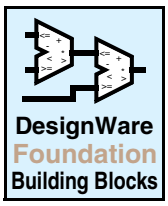




DW01_addsub

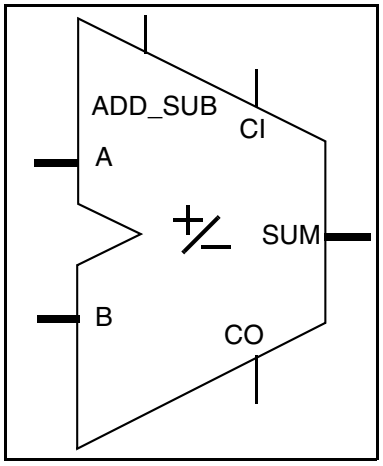
Adder-Subtractor

Version, STAR, and myDesignWare Subscriptions: IP Directory

Features and Benefits

- Parameterized word length
- Carry-in and carry-out signals

Revision History



Description

DW01_addsub is a two-input adder-subtractor. DW01_addsub adds or subtracts two operands A and B with a carry-in (CI) to produce the output SUM with a carry-out (CO).

The ADD_SUB signal determines whether the operation to perform is an addition (ADD_SUB = 0) or a subtraction (ADD_SUB = 1).

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
A	*width* bits	Input	Input data
B	*width* bits	Input	Input data
CI	1 bit	Input	Carry/borrow-in
ADD_SUB	1 bit	Input	Addition/subtraction control
SUM	*width* bits	Output	Sum (A + B + CI) or difference (A – B – CI)
CO	1 bit	Output	Carry/borrow-out

Table 1-2 Parameter Description

Parameter	Values	Description
width	≥ 1	Word length of A, B, and SUM

Table 1-3 Synthesis Implementations[a]

Implementation Name	Implementation	License Feature Required
rpl	Ripple-carry synthesis model	none

Table 1-3 Synthesis Implementations[a] (Continued)

Implementation Name	Implementation	License Feature Required
cla	Carry-look-ahead synthesis model	none
pparch	Delay-optimized flexible parallel-prefix	DesignWare
apparch	Area-optimized flexible architecture that can be optimized for area, for speed, or for area, speed	DesignWare

a. During synthesis, Design Compiler selects the appropriate architecture for your constraints. However, you may force Design Compiler to use one of the architectures described in this table.

Table 1-4 Simulation Models

Model	Function
DW01.DW01_ADDSUB_CFG_SIM	Design unit name for VHDL simulation
dw/dw01/src/DW01_addsub_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW01_addsub.v	Verilog simulation model source code

Table 1-5 Functional Description

ADD_SUB	A	B	CI	SUM	CO
0	A	B	0	A + B	Carry-out
0	A	B	1	A + B + 1	Carry-out
1	A	B	0	A - B	Carry-out
1	A	B	1	A - B - 1	Carry-out

Related Topics

- Math – Arithmetic Overview
- DesignWare Building Block IP User Guide

HDL Usage Through Operator Inferencing - VHDL

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;

entity  DW01_addsub_oper is
  generic(wordlength: integer := 8);
  port(in1, in2 : in STD_LOGIC_VECTOR(wordlength-1 downto 0);
       ctl      : in STD_LOGIC;
       sum      : out STD_LOGIC_VECTOR(wordlength-1 downto 0));
end DW01_addsub_oper;

architecture oper of DW01_addsub_oper is
  signal in1_signed, in2_signed, sum_signed: SIGNED(wordlength-1 downto 0);
begin
  in1_signed <= SIGNED(in1);
  in2_signed <= SIGNED(in2);
  process (in1_signed, in2_signed, ctl)
  begin
    if (ctl = '0') then
      sum_signed <= in1_signed + in2_signed;
    else
      sum_signed <= in1_signed - in2_signed;
    end if;
  end process;
  sum <= STD_LOGIC_VECTOR(sum_signed);
end oper;
```

HDL Usage Through Operator Inferencing - Verilog

```
module DW01_addsub_oper(in1,in2,ctl,sum);
  parameter wordlength = 8;

  input [wordlength-1:0] in1,in2;
  input ctl;
  output [wordlength-1:0] sum;
  reg [wordlength-1:0] sum;

  always @(in1 or in2 or ctl)
  begin
    if (ctl == 0)
      sum = in1 + in2;
    else
      sum = in1 - in2;
  end
endmodule
```

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW01_addsub_inst is
  generic ( inst_width : NATURAL := 8 );
  port ( inst_A       : in std_logic_vector(inst_width-1 downto 0);
         inst_B       : in std_logic_vector(inst_width-1 downto 0);
         inst_CI      : in std_logic;
         inst_ADD_SUB : in std_logic;
         SUM_inst     : out std_logic_vector(inst_width-1 downto 0);
         CO_inst      : out std_logic );
end DW01_addsub_inst;

architecture inst of DW01_addsub_inst is
begin

  -- Instance of DW01_addsub
  U1 : DW01_addsub
    generic map ( width => inst_width )
    port map ( A => inst_A, B => inst_B, CI => inst_CI,
               ADD_SUB => inst_ADD_SUB, SUM => SUM_inst, CO => CO_inst );
end inst;

-- pragma translate_off
configuration DW01_addsub_inst_cfg_inst of DW01_addsub_inst is
  for inst
  end for; -- inst
end DW01_addsub_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW01_addsub_inst( inst_A, inst_B, inst_CI, inst_ADD_SUB,
                         SUM_inst, CO_inst );

  parameter width = 8;

  input [width-1 : 0] inst_A;
  input [width-1 : 0] inst_B;
  input inst_CI;
  input inst_ADD_SUB;
  output [width-1 : 0] SUM_inst;
  output CO_inst;

  // Instance of DW01_addsub
  DW01_addsub #(width)
    U1 ( .A(inst_A), .B(inst_B), .CI(inst_CI), .ADD_SUB(inst_ADD_SUB),
         .SUM(SUM_inst), .CO(CO_inst) );

endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
March 2019	DWBB_201903.0	■ Removed Table 1-4, “Obsolete Synthesis Implementations”
January 2019	DWBB_201806.5	■ Updated example in “HDL Usage Through Component Instantiation - VHDL” on page 4 ■ Added this Revision History table and the document links on this page

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