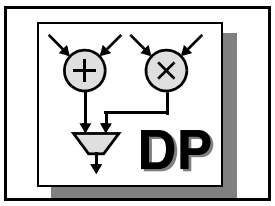

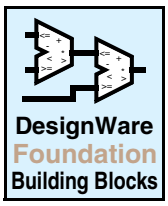

DWF_dp_count_ones functions

Count-Ones

Version, STAR, and myDesignWare Subscriptions: IP Directory

Description

The DWF_dp_count_ones functions count the number of bits with value 1 in argument vector `a`. Operation for unsigned and signed arguments is identical and the functions always return an unsigned value.

Table 1-1 Function Names

Function Name	Description
DWF_dp_count_ones	VHDL unsigned count-ones
DWF_dp_count_ones	VHDL signed (two's complement) count-ones
DWF_dp_count_ones	VHDL std_logic_vector count-ones
DWF_dp_count_ones	Verilog unsigned count-ones
DWF_dp_count_ones	Verilog signed (two's complement) count-ones

Table 1-2 Argument Description

Argument Name	Type	Width / Values	Description
a	Vector	width	Input data
DWF_dp_count_ones	Vector	ceil($\log_2$[width + 1])	Return value

Table 1-3 Parameter Description (Verilog)

Parameter	Values	Description
width	≥ 1	Word length of input `a`

Verilog Include File: `DW_dp_count_ones_function.inc`

Functional Description

```
z[bit_width(width+1)-1:0] = DWF_dp_count_ones (a[width-1:0])
```

```
z[bit_width(width+1)-1:0] =
          sum (i = 0, i < width, i++) ((a[i] == '1') ? 1 : 0)
```

For more information about the DesignWare datapath functions, refer to the topic titled DesignWare Datapath Functions Overview.

Related Topics

- DesignWare Datapath Functions Overview
- DesignWare Building Block IP User Guide

VHDL Example

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use DWARE.DW_dp_functions.all;
-- DWARE.DW_dp_functions_arith package if IEEE.std_logic_arith is used

entity DWF_dp_count_ones_test is
  port (a : in  unsigned(7 downto 0);
        b : in  unsigned(3 downto 0);
        z : out std_logic);
end DWF_dp_count_ones_test;

architecture rtl of DWF_dp_count_ones_test is
begin
  z <= '1' when (DWF_dp_count_ones (a) >= b) else '0';
end rtl;
```

Verilog Example

```
module DWF_dp_count_ones_test (a, b, z);

  input  [7:0] a;
  input  [3:0] b;
  output       z;

  // Passes the parameters to the function
  parameter width = 8;

  // add "$SYNOPSYS/dw/sim_ver" to the search path for simulation
  `include "DW_dp_count_ones_function.inc"

  assign z = (DWF_dp_count_ones (a) >= b) ? 1'b1 : 1'b0;

endmodule
```

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