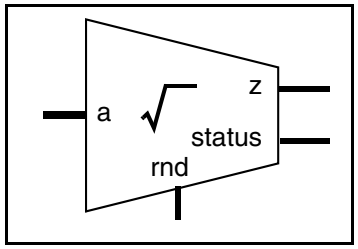
DW_fp_sqrt

Floating-Point Square Root

Version, STAR, and myDesignWare Subscriptions: IP Directory

Features and Benefits

Revision History



- The precision format is parameterizable for either IEEE single, double precision, or a user-defined custom format
- Hardware for denormal numbers of IEEE 754 standard is selectively provided.
- Configurable to be fully compliant with the IEEE Std 754-1985 standard
- Configurable for NaN representation compatible with the IEEE Std 754-2008 standard (controlled by the *ieee_compliance* parameter)
- DesignWare datapath generator is employed for better timing and area

Description

DW_fp_sqrt computes the floating-point square root of a floating-point operand, a.

Component pins are described in Table 1-1 and configuration parameters are described in Table 1-2.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
a	*exp_width* + *sig_width* + 1 bits	Input	Input data
rnd	3 bits	Input	Rounding mode; supports all rounding modes described in the *Datapath Floating-Point Overview*
z	*exp_width* + *sig_width* + 1 bits	Output	Square root of `a`
status	8 bits	Output	Status flags for the result `z` For details, see STATUS Flags in the *Datapath Floating-Point Overview.*

Table 1-2 Parameter Description

Parameter	Values	Description
sig_width	2 to 253 bits	Word length of fraction field of floating-point numbers `a` and `z`
exp_width	3 to 31 bits	Word length of biased exponent of floating-point numbers `a` and `z`

Table 1-2 Parameter Description (Continued)

Parameter	Values	Description
ieee_compliance	0, 1, or 3 Default: 0	Level of support for the IEEE Std 754 standards: ■ 0: No support for NaNs and denormals; NaNs are considered infinities and denormals are considered zeros ■ 1: Fully compliant with the IEEE Std 754-1985 standard, including support for NaNs and denormals ■ 2: Reserved ■ 3: Fully compliant with the IEEE Std 754-1985 standard plus NaN representation that matches the IEEE Std 754-2008 standard[a] For details, see Compatibility with IEEE Std 754 Standards in the *Datapath Floating-Point Overview*

a. Propagating payload information to the output during the NaN process, which is an optional feature specified in the IEEE Std 754-2008 standard, is supported.

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
rtl	Synthesis model	DesignWare

Table 1-4 Simulation Models

Model	Function
DW02.DW_FP_SQRT_CFG_SIM	Design unit name for VHDL simulation
dw/dw02/src/DW_fp_sqrt_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW_fp_sqrt.v	Verilog simulation model source code

Alternative Implementation of Floating-point Square Root Using DW_lp_fp_multifunc

The floating-point square root operation can also be implemented by DW_lp_fp_multifunc component, which evaluates the value of floating-point square root with 1 ulp error bound. There will be 1 ulp difference between the value from DW_lp_fp_multifunc and the value from DW_fp_sqrt. Performance and area of the synthesis results are different between the DW_fp_sqrt and reciprocal implementation of the DW_lp_fp_multifunc, depending on synthesis constraints, library cells and synthesis environments. By comparing performance and area between the square root implementation of DW_lp_fp_multifunc and DW_fp_sqrt component, the DW_lp_fp_multifunc provides more choices for the better synthesis results. Below is an example of the Verilog description for the floating-point square root of the DW_lp_fp_multifunc. For more detailed information, see the DW_lp_fp_multifunc datasheet.

```
DW_lp_fp_multifunc #(sig_width, exp_width, ieee_compliance, 2) U1 (
    .a(a),
    .func(16'h0002),
    .rnd(3'h0),
```

```
    .z(z),
    .status(status)
);
```

For more information about the floating-point, including `status` flag bits, and integer and floating-point formats, refer to the *Datapath Floating-Point Overview*.

Suppressing Warning Messages During Verilog Simulation

The Verilog simulation model includes macros that allow you to suppress warning messages during simulation.

To suppress all warning messages for all DWBB components, define the DW_SUPPRESS_WARN macro in either of the following ways:

- Specify the Verilog preprocessing macro in Verilog code:

  ```
  `define DW_SUPPRESS_WARN
  ```

- Or, include a command line option to the simulator, such as:

  `+define+DW_SUPPRESS_WARN` (which is used for the Synopsys VCS simulator)

The warning messages for this model include the following:

- If an invalid rounding mode has been detected on `rnd`, the following message is displayed:

  ```
  WARNING: <instance_path>:
      at time = <timestamp>: Illegal rounding mode.
  ```

  To suppress this message, use the DW_SUPPRESS_WARN macro explained earlier.

Related Topics

- Datapath Floating-Point Overview
- DesignWare Building Block IP User Guide

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.dw_foundation_comp.all;

entity DW_fp_sqrt_inst is
  generic (
    inst_sig_width : POSITIVE := 23;
    inst_exp_width : POSITIVE := 8;
    inst_ieee_compliance : INTEGER := 0
  );
  port (
    inst_a : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
    inst_rnd : in std_logic_vector(2 downto 0);
    z_inst : out std_logic_vector(inst_sig_width+inst_exp_width downto 0);
    status_inst : out std_logic_vector(7 downto 0)
  );
end DW_fp_sqrt_inst;

architecture inst of DW_fp_sqrt_inst is
begin

  -- Instance of DW_fp_sqrt
  U1 : DW_fp_sqrt
    generic map (
      sig_width => inst_sig_width,
      exp_width => inst_exp_width,
      ieee_compliance => inst_ieee_compliance
    )
    port map (
      a => inst_a,
      rnd => inst_rnd,
      z => z_inst,
      status => status_inst
    );

end inst;

-- pragma translate_off
configuration DW_fp_sqrt_inst_cfg_inst of DW_fp_sqrt_inst is
  for inst
  end for;
end DW_fp_sqrt_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_fp_sqrt_inst( inst_a, inst_rnd, z_inst, status_inst );

parameter inst_sig_width = 23;
parameter inst_exp_width = 8;
parameter inst_ieee_compliance = 0;


input [inst_sig_width+inst_exp_width : 0] inst_a;
input [2 : 0] inst_rnd;
output [inst_sig_width+inst_exp_width : 0] z_inst;
output [7 : 0] status_inst;

  // Instance of DW_fp_sqrt
  DW_fp_sqrt #(inst_sig_width, inst_exp_width, inst_ieee_compliance) U1 (
                      .a(inst_a),
                      .rnd(inst_rnd),
                      .z(z_inst),
                      .status(status_inst) );

endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
October 2020	DWBB_202009.1	■ For enhanced NaN compatibility with the IEEE Std 754 standards, added a new value for *ieee_compliance* in Table 1-2 on page 1
July 2020	DWBB_201912.5	■ Adjusted the description of the *ieee_compliance* parameter in Table 1-2 on page 1 ■ Added "Suppressing Warning Messages During Verilog Simulation" on page 3
January 2020	DWBB_201912.1	■ Corrected port names for DW_lp_fp_multifunc in "Alternative Implementation of Floating-point Square Root Using DW_lp_fp_multifunc" on page 2
July 2019	DWBB_201903.3	■ Removed reference to minPower library in "Alternative Implementation of Floating-point Square Root Using DW_lp_fp_multifunc" on page 2 ■ Added this Revision History table and the document links on this page

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