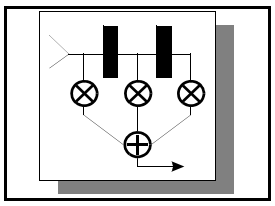
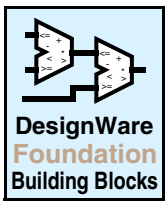




DW_thermdec

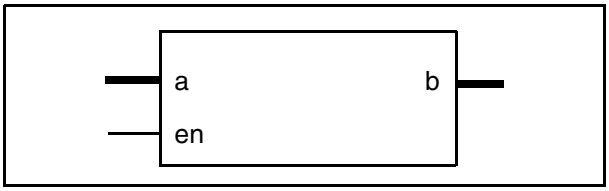
Binary Thermometer Decoder with Enable

Version, STAR, and myDesignWare Subscriptions: IP Directory

Features and Benefits

- Parameterized word length
- Integrates enable control

Revision History



Description

DW_thermdec decodes a binary value present at input port `a` and sets contiguous bits of the output port `b`, depending on the enable input (`en`). A thermometer decoder with input *width* = *n* bits has 2^n bits at the output, where each output with index $j \leq i$ becomes active when `en` = 1 (enable input) and input `a` = i. The output bits are active high. When `en` = 0 none of the output bits are active.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
en	1 bit	Input	Enable input (active high)
a	*width*	Input	Binary input data
b	2^{width}	Output	Decoded output data

Table 1-2 Parameter Description

Parameter	Values	Description
width[a]	1 to 16	Word length of input `a` is *width*. Word length of output `b` is 2^{width}

a. The `width` parameter value causes the size of output `b` to grow exponentially. Therefore, a `width` value near the upper bound results in a long compile time.

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
cgen	Datapath generator-based Implementation	DesignWare

Table 1-4 Simulation Models

Model	Function
DW01.DW_THERMDEC_CFG_SIM	Design unit name for VHDL simulation
dw/dw01/src/DW_thermdec_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW_thermdec.v	Verilog simulation model source code

Table 1-5 Truth Table (width = 3)

a(2:0)	en	b(7)	b(6)	b(5)	b(4)	b(3)	b(2)	b(1)	b(0)
000	1	0	0	0	0	0	0	0	1
001	1	0	0	0	0	0	0	1	1
010	1	0	0	0	0	0	1	1	1
011	1	0	0	0	0	1	1	1	1
100	1	0	0	0	1	1	1	1	1
101	1	0	0	1	1	1	1	1	1
110	1	0	1	1	1	1	1	1	1
111	1	1	1	1	1	1	1	1	1
xxx	0	0	0	0	0	0	0	0	0

Related Topics

- Logic – Combinational Overview
- DesignWare Building Block IP User Guide

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_Foundation_comp_arith.all;

entity DW_thermdec_inst is
      generic (
        inst_width : NATURAL := 8
        );
      port (
        inst_en : in std_logic;
        inst_a : in std_logic_vector(inst_width-1 downto 0);
        b_inst : out std_logic_vector(2**inst_width-1 downto 0)
        );
    end DW_thermdec_inst;


architecture inst of DW_thermdec_inst is

begin

    -- Instance of DW_thermdec
    U1 : DW_thermdec
    generic map (
          width => inst_width
          )
    port map (
          en => inst_en,
          a => inst_a,
          b => b_inst
          );


end inst;

-- pragma translate_off
configuration DW_thermdec_inst_cfg_inst of DW_thermdec_inst is
  for inst
  end for; -- inst
end DW_thermdec_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_thermdec_inst( inst_en, inst_a, b_inst );

parameter inst_width = 8;


input inst_en;
input [inst_width-1 : 0] inst_a;
output [(1<<inst_width)-1 : 0] b_inst;

    // Instance of DW_thermdec
    DW_thermdec #(inst_width) U1 (
                .en(inst_en),
                .a(inst_a),
                .b(b_inst) );

endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
October 2019	DWBB_201903.5	■ Adjusted the footnote in Table 1-2 on page 1 ■ Added this Revision History table and the document links on this page

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