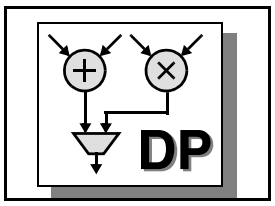

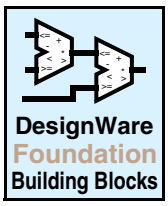

DWF_dp_sub_abs function

Subtract and Absolute Value

Version, STAR, and myDesignWare Subscriptions: IP Directory

Description

The DWF_dp_sub_abs function returns the absolute value (magnitude) of the result of the subtraction of two arguments `a` and `b`. Argument `a, b` and the returned value are either signed (two's complement), or unsigned, depending on the function used.

Either a signed or unsigned value can be returned depending on the functions name used:

Table 1-1 Function Names

Function Name	Description
DWF_dp_sub_abs	VHDL unsigned subtract and absolute value
DWF_dp_sub_abs	VHDL signed (two's complement) subtract and absolute value
DWF_dp_sub_abs_uns	Verilog unsigned subtract and absolute value
DWF_dp_sub_abs_tc	Verilog signed (two's complement) subtract and absolute value

Table 1-2 Argument Description

Argument Name	Type	Width	Description
a	Vector	width	Input minuend
b	Vector	width	Input subtrahend
DWF_dp_sub_abs	Vector	width	Returned value

Table 1-3 Parameter Description (Verilog)

Parameter	Values	Description
width	≥ 1	Word length of inputs `a`, `b` and the returned value `DWF_dp_sub_abs`

Verilog Include File: `DW_dp_sub_abs_function.inc`

Functional Description

```
z[width-1:0] = DWF_dp_abs(a[width-1:0],b[width-1:0])

z[width-1:0] =  a[width-1:0]-b[width-1:0]  if a[width-1:0] >= b[width-1:0]
             = -a[width-1:0]  else
```

For more information about the DesignWare datapath functions, refer to the topic titled Arithmetic – Datapath Functions Overview.

Related Topics

- Arithmetic – Datapath Functions Overview
- DesignWare Building Block IP User Guide

VHDL Example

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use DWARE.DW_dp_functions.all;
-- DWARE.DW_dp_functions_arith package if IEEE.std_logic_arith is used

entity DWF_dp_sub_abs_test is
  port (a, b, c, d : in  signed(7 downto 0);
        z          : out signed(15 downto 0));
end DWF_dp_sub_abs_test;

architecture rtl of DWF_dp_sub_abs_test is
begin
  z <= DWF_dp_sub_abs (a * b, c) + d;
end rtl;
```

Verilog Example

```
module DWF_dp_sub_abs_test (a, b, c, d, z);

  input  signed  [7:0] a, b, c, d;
  output signed [15:0] z;

  // Passes the parameter to the function
  parameter width = 16;

  // add "$SYNOPSYS/dw/sim_ver" to the search path for simulation
  `include "DW_dp_sub_abs_function.inc"

  assign z = DWF_dp_sub_abs_tc (a * b, c) + d;

endmodule
```

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