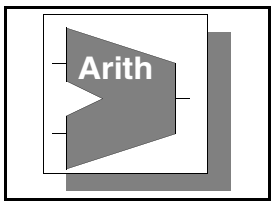
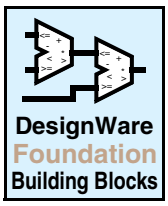




DW_div_sat

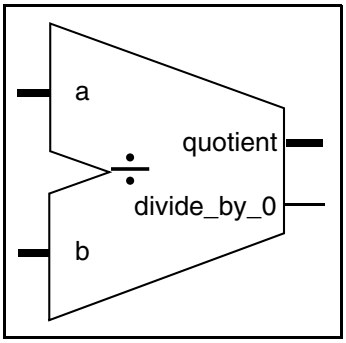
Combinational Divider with Saturation

Version, STAR and Download Information: IP Directory

Features and Benefits

Revision History

- Parameterized word lengths
- Parameterized quotient length with saturation
- Unsigned and signed (two's complement) data operation
- Multiple architectures for area/performance trade-off



Description

DW_div_sat is a combinational integer divider with parameterized quotient length. When the quotient length is smaller than the dividend length, the quotient is saturated in case of overflow.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
a	*a_width* bits	Input	Dividend
b	*b_width* bits	Input	Divisor
quotient	*q_width* bits	Output	Quotient
divide_by_0	1 bit	Output	Indicates if b equals 0

Table 1-2 Parameter Description

Parameter	Values	Description
a_width	≥ 2 Default: None	Word length of `a`
b_width	≥ 2 Default: None	Word length of `b`
q_width	2 to *a_width* Default: None	Word length of `quotient`
tc_mode	0 or 1 Default: 0	Two's- complement control ■ 0: Unsigned ■ 1: Signed

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
cla	Restoring carry-look-ahead divider synthesis model	DesignWare
cla2	Radix-4 restoring carry-look-ahead divider synthesis model	DesignWare
cla3	Radix-8 restoring carry-look-ahead divider synthesis model	DesignWare

Table 1-4 Simulation Models

Model	Function
DW02.DW_DIV_SAT_CFG_SIM	Design unit name for VHDL simulation
dw/dw02/src/DW_div_sat_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW_div_sat.v	Verilog simulation model source code

Table 1-5 Functional Description

tc_mode	a	b	quotient
0	a (unsigned)	b (unsigned)	sat(int(a/b)) (unsigned)
1	a (two's complement)	b (two's complement)	sat(int(a/b)) (two's complement)

The parameter *tc_mode* determines whether the data of the inputs `a` and `b` and the output `quotient` are interpreted as unsigned (*tc_mode* = 0) or two's-complement (*tc_mode* = 1) numbers.

Regular integer division yields a quotient that has the same number of bits as the dividend (see DW_div component). DW_div_sat allows to specify a shorter `quotient` length where the upper bits are truncated and only the lower *q_width* bits are kept. In case of overflow/underflow (for example, if the division result is too large to fit in the `quotient` output) the returned `quotient` value is saturated.

The `quotient` output is defined as follows:

```
q_int[a_width-1:0] = int (a/b)
```

Unsigned (*tc_mode* = 0):

```
quotient[q_width-1:0] = 2^q_width-1                if q_int[a_width-1:0] > 2^q_width-1
                      = q_int[q_width-1:0]      else
```

Signed (*tc_mode* = 1):

```
quotient[q_width-1:0] =  2^q_width-1-1             if      q_int[a_width-1:0] >  2^q_width-1-1
                      = -2^q_width-1               else if q_int[a_width-1:0] < -2^q_width-1
                      = q_int[q_width-1:0]      else
```

Divide-by-Zero Behavior

In the case of dividing by zero, the `divide_by_0` output is set to 1 and the `quotient` is saturated to the maximum positive value if `a` is positive and to the minimum negative value if `a` is negative.

Suppressing Warning Messages During Verilog Simulation

The Verilog simulation model includes macros that allow you to suppress warning messages during simulation.

To suppress all warning messages for all DWBB components, define the DW_SUPPRESS_WARN macro in either of the following ways:

- Specify the Verilog preprocessing macro in Verilog code:

  ```
  `define DW_SUPPRESS_WARN
  ```

- Or, include a command line option to the simulator, such as:

  `+define+DW_SUPPRESS_WARN` (which is used for the Synopsys VCS simulator)

The warning messages for this model include the following:

- If a divide-by-zero operation is attempted, the following message is displayed:

  ```
  WARNING: <instance_path>:
      at time = <timestamp>: Division by zero.
  ```

  To suppress this message, use the DW_SUPPRESS_WARN macro explained earlier.

Related Topics

- Math – Arithmetic Overview
- DesignWare Building Block IP User Guide

HDL Usage Through Component Instantiation - VHDL

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DW_Foundation_comp_arith.all;

entity DW_div_sat_inst is

  generic (width   : positive := 8;
           tc_mode : natural  := 0);
  port (a           : in  std_logic_vector(2*width-1 downto 0);
        b           : in  std_logic_vector(width-1 downto 0);
        quotient    : out std_logic_vector(width-1 downto 0);
        divide_by_0 : out std_logic);
end DW_div_sat_inst;

architecture inst of DW_div_sat_inst is
begin
  -- instance of DW_div_sat
  U1 : DW_div_sat
    generic map (a_width => 2*width, b_width => width,
                 q_width => width, tc_mode => tc_mode)
    port map (a => a, b => b,
              quotient => quotient, divide_by_0 => divide_by_0);
end inst;

-- pragma translate_off
configuration DW_div_sat_inst_cfg_inst of DW_div_sat_inst is
  for inst
  end for;
end DW_div_sat_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_div_sat_inst (a, b, quotient, divide_by_0);

  parameter width   = 8;
  parameter tc_mode = 0;

  input  [2*width-1 : 0] a;
  input    [width-1 : 0] b;
  output   [width-1 : 0] quotient;
  output                 divide_by_0;

  // Please add +incdir+$SYNOPSYS/dw/sim_ver+ to your verilog simulator
  // command line (for simulation).

  // instance of DW_div_sat
  DW_div_sat #(2*width, width, width, tc_mode)
    U1 (.a(a), .b(b),
        .quotient(quotient), .divide_by_0(divide_by_0));
endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
July 2020	DWBB_201912.5	■ Added "Suppressing Warning Messages During Verilog Simulation" on page 3
March 2019	DWBB_201903.0	■ Remove all information about functional inference for this component ■ Added this Revision History table and the document links on this page

Copyright Notice and Proprietary Information

Destination Control Statement

All technical data contained in this publication is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the reader's responsibility to determine the applicable regulations and to comply with them.

Disclaimer

SYNOPSYS, INC., AND ITS LICENSORS MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Trademarks

Synopsys and certain Synopsys product names are trademarks of Synopsys, as set forth at https://www.synopsys.com/company/legal/trademarks-brands.html.

All other product or company names may be trademarks of their respective owners.

Free and Open-Source Software Licensing Notices

If applicable, Free and Open-Source Software (FOSS) licensing notices are available in the product installation.

Third-Party Links

Any links to third-party websites included in this document are for your convenience only. Synopsys does not endorse and is not responsible for such websites and their practices, including privacy practices, availability, and content.

Synopsys, Inc.
www.synopsys.com