DW_ram_rw_s_lat

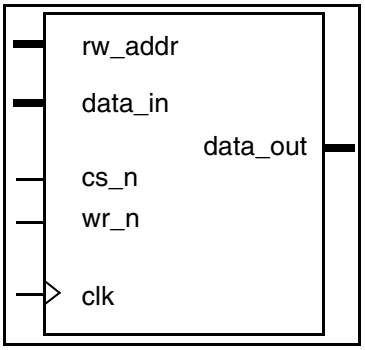
Synchronous Single-Port, Read/Write RAM (Latch-Based)

Version, STAR, and myDesignWare Subscriptions: IP Directory

Features and Benefits

Revision History

- Parameterized word depth
- Parameterized data width
- Synchronous static memory



Description

DW_ram_rw_s_lat implements a parameterized, synchronous, single-port static RAM.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
clk	1 bit	Input	Clock
cs_n	1 bit	Input	Chip select, active low
wr_n	1 bit	Input	Write enable, active low
rw_addr	ceil($\log_2$[*depth*]) bits	Input	Address bus
data_in	*data_width* bits	Input	Input data bus
data_out	*data_width* bits	Output	Output data bus

Table 1-2 Parameter Description

Parameter	Values	Description
data_width	1 to 256 Default: None	Width of `data_in` and `data_out` buses
depth	2 to 256 Default: None	Number of words in the memory array (address width)

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
str	Synthesis model	DesignWare

Table 1-4 Simulation Models

Model	Function
DW06.DW_RAM_RW_S_LAT_CFG_SIM	VHDL simulation configuration
dw/dw06/src/DW_ram_rw_s_lat_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW_ram_rw_s_lat.v	Verilog simulation model source code

The write data enters the RAM through the `data_in` input port and is read out through the `data_out` port. The read operation is asynchronous to the clock, allowing the data written into the RAM to be instantly read. The RAM is constantly reading regardless of the state of `cs_n`.

The `rw_addr` port is used to address the *depth* words in the memory. For addresses beyond the maximum depth (example: `rw_addr` = 7 and `depth` = 6), the `data_out` bus is driven low. No warnings are given during simulations when an address beyond the scope of *depth* is used.

Attention This component contains enable signals for internal latches that are derived from the wr_n port. To keep hold times to a minimum, you should consider instances of this component to be individual floorplanning elements.

Chip Selection, Reading and Writing

The `cs_n` input is the chip select, active low signal. When `cs_n` is low, data is constantly read from the RAM.

When `cs_n`, `wr_n` (write enable, active low), and `clk` are low, `data_in` is transparent to the memory cell being accessed (`data_in` equals `data_out`). Data is captured into the memory cell on the rising edge of `clk`.

When `cs_n` is high, the RAM is disabled, and the `data_out` bus is driven low.

Application Notes

DW_ram_rw_s_lat is intended to be used as small scratch-pad memory or register file. Because DW_ram_rw_s_lat is built from the cells within the ASIC cell library, it should be kept small to obtain an efficient implementation. If a larger memory is required, you should consider using a hard macro RAM from the ASIC library in use.

Suppressing Warning Messages During Verilog Simulation

The Verilog simulation model includes macros that allow you to suppress warning messages during simulation.

To suppress all warning messages for all DWBB components, define the DW_SUPPRESS_WARN macro in either of the following ways:

- Specify the Verilog preprocessing macro in Verilog code:

  ```
  `define DW_SUPPRESS_WARN
  ```

- Or, include a command line option to the simulator, such as:

  `+define+DW_SUPPRESS_WARN` (which is used for the Synopsys VCS simulator)

The warning messages for this model include the following:

- If values other than 1 or 0 are present on a clock port, the following message is displayed:

  ```
  WARNING: <instance_path>.<clock_name>_monitor:
      at time = <timestamp>, Detected unknown value, x, on <clock_name> input.
  ```

  To suppress only this warning message for all DWBB components, use the following macro:

  - Define the DW_DISABLE_CLK_MONITOR macro. You can define this macro in the following ways:
    - Specify the Verilog preprocessing macro in Verilog code:

      ```
      `define DW_DISABLE_CLK_MONITOR
      ```

    - Or, include a command line option to the simulator, such as:

      `+define+DW_DISABLE_CLK_MONITOR` (which is used for the Synopsys VCS simulator)

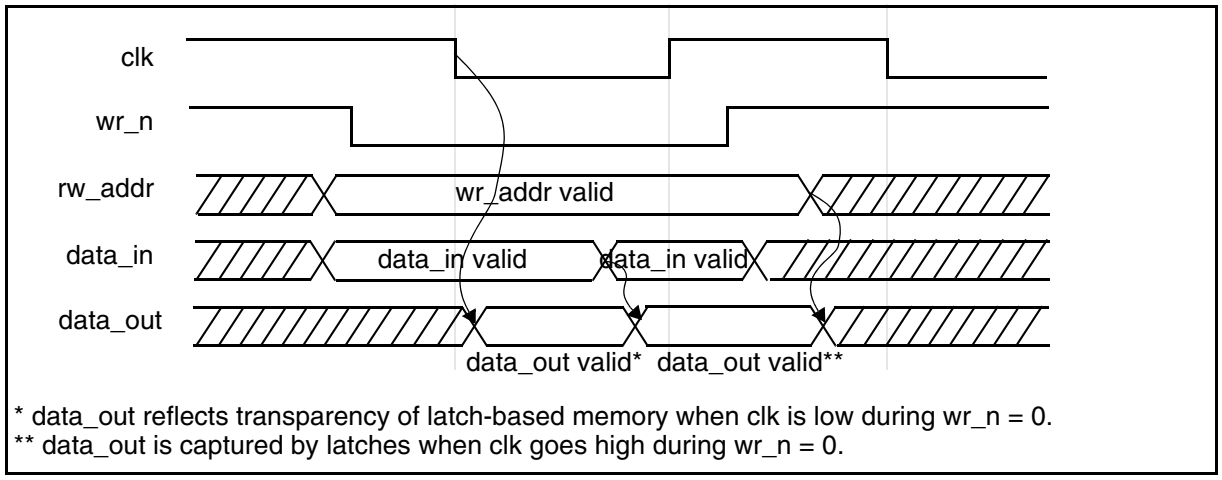
  This message is also suppressed using the DW_SUPPRESS_WARN macro explained earlier.

Timing Waveforms

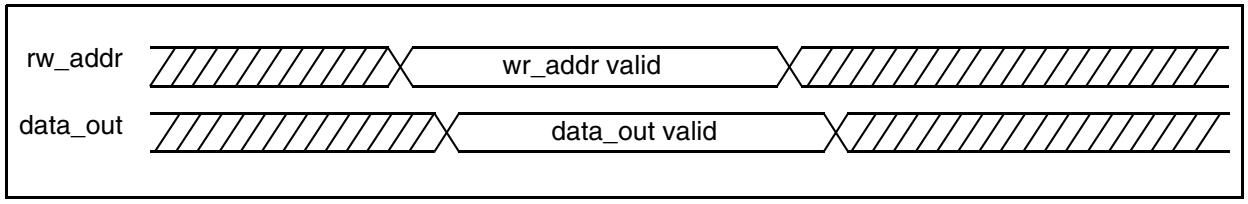
Figure 1-1 shows timing diagrams for various conditions of DW_ram_rw_s_lat.

Figure 1-1 Instantiated RAM Timing Waveforms

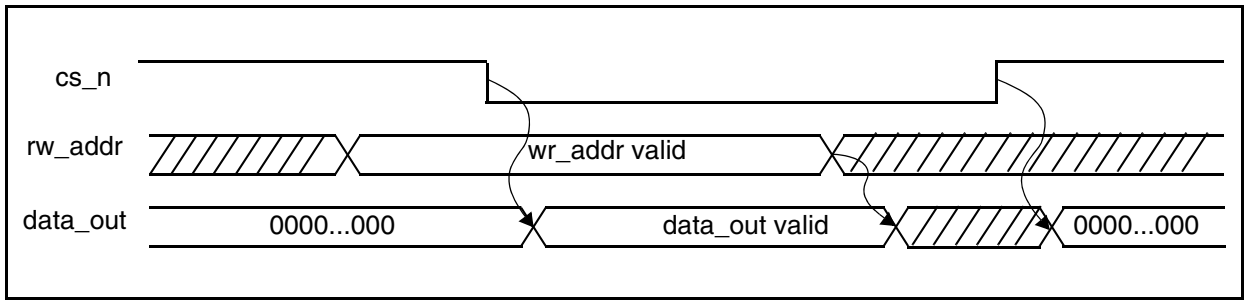
Write Timing, rst_n = 1, cs_n = 0



Read Timing, address controlled, cs_n = 0



Read Timing, cs_n controlled



Related Topics

- Memory – Synchronous RAMs Listing
- DesignWare Building Block IP User Guide

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW_ram_rw_s_lat_inst is
  generic (inst_data_width : INTEGER := 8;   inst_depth : INTEGER := 8 );
  port (inst_clk     : in std_logic;
        inst_cs_n    : in std_logic;
        inst_wr_n    : in std_logic;
        inst_rw_addr : in std_logic_vector(bit_width(inst_depth)-1 downto 0);
        inst_data_in : in std_logic_vector(inst_data_width-1 downto 0);
        data_out_inst: out std_logic_vector(inst_data_width-1 downto 0) );
end DW_ram_rw_s_lat_inst;

architecture inst of DW_ram_rw_s_lat_inst is
begin

  -- Instance of DW_ram_rw_s_lat
  U1 : DW_ram_rw_s_lat
    generic map (data_width => inst_data_width,   depth => inst_depth )
    port map (clk => inst_clk,   cs_n => inst_cs_n,   wr_n => inst_wr_n,
              rw_addr => inst_rw_addr,   data_in => inst_data_in,
              data_out => data_out_inst );
end inst;

-- pragma translate_off
configuration DW_ram_rw_s_lat_inst_cfg_inst of DW_ram_rw_s_lat_inst is
  for inst
  end for; -- inst
end DW_ram_rw_s_lat_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_ram_rw_s_lat_inst(inst_clk, inst_cs_n, inst_wr_n, inst_rw_addr,
                            inst_data_in, data_out_inst );

  parameter data_width = 8;
  parameter depth = 8;
  `define bit_width_depth 3 // ceil(log2(depth))

  input inst_clk;
  input inst_cs_n;
  input inst_wr_n;
  input [`bit_width_depth-1 : 0] inst_rw_addr;
  input [data_width-1 : 0] inst_data_in;
  output [data_width-1 : 0] data_out_inst;

  // Instance of DW_ram_rw_s_lat
  DW_ram_rw_s_lat #(data_width, depth)
  U1 (.clk(inst_clk),   .cs_n(inst_cs_n),   .wr_n(inst_wr_n),
      .rw_addr(inst_rw_addr),   .data_in(inst_data_in),
      .data_out(data_out_inst) );
endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
July 2020	DWBB_201912.5	■ Adjusted content and title of "Suppressing Warning Messages During Verilog Simulation" on page 3 and added the DW_SUPPRESS_WARN macro
October 2019	DWBB_201903.5	■ Added the "Disabling Clock Monitor Messages" section
January 2019	DWBB_201806.5	■ Updated example in "HDL Usage Through Component Instantiation - VHDL" on page 5 ■ Added this Revision History table and the document links on this page

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