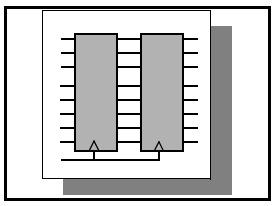
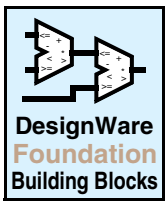




DW03_shftreg

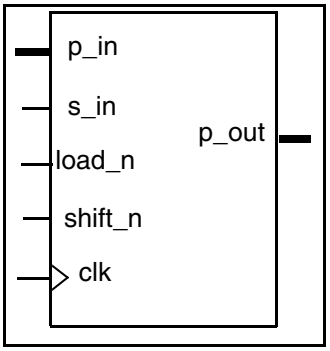
Shift Register

Version, STAR, and myDesignWare Subscriptions: IP Directory

Features and Benefits

- Parameterized word length
- Active low shift enable
- Active low load enable
- Provides minPower benefits with the DesignWare-LP license.

Revision History



Description

DW03_shftreg is a shift register of parameterized length. The active low load enable, `load_n`, provides parallel load access and the active low shift enable, `shift_n`, shifts the data. If `load_n` is set to a constant high value during synthesis, a serial shifter with no parallel access is built. The serial output of the shift register is computed as `p_out(`*length* `– 1)`.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
clk	1 bit	Input	Clock
s_in	1 bit	Input	Serial shift input
p_in	*length* bits	Input	Parallel input
shift_n	1 bit	Input	Shift enable, active low
load_n	1 bit	Input	Parallel load enable, active low
p_out	*length* bits	Output	Shift register parallel output

Table 1-2 Parameter Description

Parameter	Values	Description
length	≥ 1	Length of shifter

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
str	Synthesis model	DesignWare

Table 1-4 Simulation Models

Model	Function
DW03.DW03_SHFTREG_CFG_SIM	Design unit name for VHDL simulation
dw/dw03/src/DW03_shftreg_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW03_shftreg.v	Verilog simulation model source code

Table 1-5 Shift Register Operation Truth Table

load_n	shift_n	Operation
0	X	Parallel load
1	0	Serial shift
1	1	Standby

Suppressing Warning Messages During Verilog Simulation

The Verilog simulation model includes macros that allow you to suppress warning messages during simulation.

To suppress all warning messages for all DWBB components, define the DW_SUPPRESS_WARN macro in either of the following ways:

- Specify the Verilog preprocessing macro in Verilog code:

  ```
  `define DW_SUPPRESS_WARN
  ```

- Or, include a command line option to the simulator, such as:

  `+define+DW_SUPPRESS_WARN` (which is used for the Synopsys VCS simulator)

The warning messages for this model include the following:

- If values other than 1 or 0 are present on a clock port, the following message is displayed:

  ```
  WARNING: <instance_path>.<clock_name>_monitor:
      at time = <timestamp>, Detected unknown value, x, on <clock_name> input.
  ```

  To suppress only this warning message for all DWBB components, use the following macro:

  - Define the DW_DISABLE_CLK_MONITOR macro. You can define this macro in the following ways:
    - Specify the Verilog preprocessing macro in Verilog code:

      ```
      `define DW_DISABLE_CLK_MONITOR
      ```

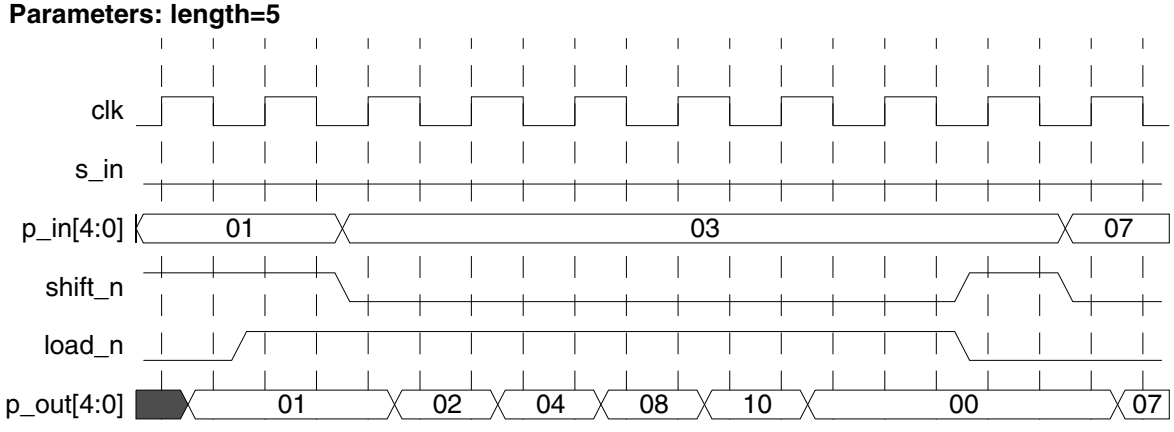
    - Or, include a command line option to the simulator, such as:

      `+define+DW_DISABLE_CLK_MONITOR` (which is used for the Synopsys VCS simulator)

  This message is also suppressed using the DW_SUPPRESS_WARN macro explained earlier.

Timing Diagram

Figure 1-1 Functional Operation



Related Topics

- Memory – Registers Overview
- DesignWare Building Block IP User Guide

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW03_shftreg_inst is
  generic ( inst_length : NATURAL := 4 );
  port ( inst_clk     : in std_logic;
         inst_s_in    : in std_logic;
         inst_p_in    : in std_logic_vector(inst_length-1 downto 0);
         inst_shift_n : in std_logic;
         inst_load_n  : in std_logic;
         p_out_inst   : out std_logic_vector(inst_length-1 downto 0) );
end DW03_shftreg_inst;

architecture inst of DW03_shftreg_inst is
begin

  -- Instance of DW03_shftreg
  U1 : DW03_shftreg
    generic map ( length => inst_length )
    port map ( clk => inst_clk,   s_in => inst_s_in,   p_in => inst_p_in,
               shift_n => inst_shift_n,    load_n => inst_load_n,
               p_out => p_out_inst );
end inst;

-- pragma translate_off
configuration DW03_shftreg_inst_cfg_inst of DW03_shftreg_inst is
  for inst
  end for; -- inst
end DW03_shftreg_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW03_shftreg_inst( inst_clk, inst_s_in, inst_p_in,
                          inst_shift_n, inst_load_n,  p_out_inst );

  parameter length = 4;

  input inst_clk;
  input inst_s_in;
  input [length-1 : 0] inst_p_in;
  input inst_shift_n;
  input inst_load_n;
  output [length-1 : 0] p_out_inst;

  // Instance of DW03_shftreg
  DW03_shftreg #(length)
    U1 (.clk(inst_clk),   .s_in(inst_s_in),   .p_in(inst_p_in),
        .shift_n(inst_shift_n),   .load_n(inst_load_n),  .p_out(p_out_inst));

endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
July 2020	DWBB_201912.5	■ Adjusted content and title of "Suppressing Warning Messages During Verilog Simulation" on page 3 and added the DW_SUPPRESS_WARN macro
October 2019	DWBB_201903.5	■ Added the "Disabling Clock Monitor Messages" section
January 2019	DWBB_201806.5	■ Updated example in "HDL Usage Through Component Instantiation - VHDL" on page 4 ■ Added this Revision History table and the document links on this page

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