



# DWF\_dp\_simd\_addc procedures

## SIMD add with carries

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### Description

The DWF\_dp\_simd\_addc procedures implement a configurable SIMD adder with input and output carries. They allow you to either add arguments *a* and *b* as full-width vectors (for example, one 32-bit addition) or to add smaller partitions of *a* and *b* using multiple parallel adders (for example, two 16-bit additions or four 8-bit additions), each with separate input carries *cin* and output carries *cout*. The argument *no\_confs* specifies the number of possible configurations, and argument *conf* dynamically selects one configuration. Configuration with number *conf* has  $2^{\text{conf}}$  partitions of size  $\text{width}/2^{\text{conf}}$ . Arguments *a* and *b* and the output *s* are either unsigned or signed (two's complement).

**Table 1-1 Procedure Names**

Function Name	Description
DWF_dp_simd_addc	VHDL unsigned SIMD add with carries
DWF_dp_simd_addc	VHDL signed (two's complement) SIMD add with carries
DWF_dp_simd_addc_uns	Verilog unsigned SIMD add with carries
DWF_dp_simd_addc_tc	Verilog signed (two's complement) SIMD add with carries

**Table 1-2 Argument Description**

Argument Name	Type	Direction	Width / Values	Description
<i>a</i>	Vector <sup>a</sup>	Input	width	Input addend
<i>b</i>	Vector <sup>a</sup>	Input	width	Input addend
<i>cin</i>	Vector <sup>b</sup>	Input	$2^{\text{no\_confs}-1}$	Input carries
<i>no_confs</i>	Integer	Input	$\geq 2$	Number of configurations (VHDL only, constant)
<i>conf</i>	Vector <sup>b</sup>	Input	$\text{ceil}(\log_2[\text{no\_confs}])$	Configuration selection: $2^{\text{conf}}$ partitions of size $\text{width}/2^{\text{conf}}$
<i>s</i>	Vector <sup>a</sup>	Output	width	Output sum
<i>cout</i>	Vector <sup>b</sup>	Output	$2^{\text{no\_confs}-1}$	Output carries

a. unsigned or signed in VHDL

b. std\_logic\_vector in VHDL

**Table 1-3 Parameter Description (Verilog)**

Parameter	Values	Description
width	$\geq 2$ , must be a multiple of $2^{\text{no\_confs}-1}$	Word length
no_confs	$\geq 2$	Number of configurations

Verilog Include File: DW\_dp\_simd\_addc\_function.inc

## Functional Description

```

DWF_dp_simd_addc (a[width-1:0], b[width-1:0], cin[2no_confs-1-1:0],
                  no_confs, conf[bit_width(no_confs)-1:0],
                  z[width-1:0], cout[2no_confs-1-1:0])

conf = 0:
  { cout[2no_confs-1-1],      z[width-1:0] }      =
    a[width-1:0]          + b[width-1:0]          + cin[0]
conf = 1:
  { cout[2no_confs-1-1],      z[width-1:width/2] }      =
    a[width-1:width/2]    + b[width-1:width/2]    + cin[2no_confs-1/2]
  { cout[2no_confs-1/2-1],    z[width/2-1:0] }      =
    a[width/2-1:0]        + b[width/2-1:0]        + cin[0]
conf = 2:
  { cout[2no_confs-1-1],      z[width-1:width*3/4] }      =
    a[width-1:width*3/4]  + b[width-1:width*3/4]  + cin[2no_confs-1*3/4]
  { cout[2no_confs-1*3/4-1],    z[width*3/4-1:width/2] }      =
    a[width*3/4-1:width/2] + b[width*3/4-1:width/2] + cin[2no_confs-1/2]
  { cout[2no_confs-1/2-1],    z[width/2-1:width/4] }      =
    a[width/2-1:width/4]  + b[width/2-1:width/4]  + cin[2no_confs-1/4]
  { cout[2no_confs-1/4-1],    z[width/4-1:0] }      =
    a[width/4-1:0]        + b[width/4-1:0]        + cin[0]
...

```

**Example:** width = 32, no\_confs = 3

```

conf = 0:
  { cout[3], z[31: 0] } = a[31: 0] + b[31: 0] + cin[0]
conf = 1:
  { cout[3], z[31:16] } = a[31:16] + b[31:16] + cin[2]
  { cout[1], z[15: 0] } = a[15: 0] + b[15: 0] + cin[0]
conf = 2:
  { cout[3], z[31:24] } = a[31:24] + b[31:24] + cin[3]
  { cout[2], z[23:16] } = a[23:16] + b[23:16] + cin[2]
  { cout[1], z[15: 8] } = a[15: 8] + b[15: 8] + cin[1]
  { cout[0], z[ 7: 0] } = a[ 7: 0] + b[ 7: 0] + cin[0]

```

For more information about the DesignWare datapath functions, refer to [DesignWare Datapath Functions Overview](#).

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## Related Topics

- [DesignWare Datapath Functions Overview](#)
- [DesignWare Building Block IP User Guide](#)

## VHDL Example

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use DWARE.DW_dp_functions.all;
-- DWARE.DW_dp_functions_arith package if IEEE.std_logic_arith is used

entity DWF_dp_simd_addc_test is
  port (op1, op2  : in  signed(31 downto 0);
        c_in      : in  std_logic_vector(3 downto 0);
        config_no : in  std_logic_vector(1 downto 0);
        sum       : out signed(31 downto 0);
        c_out     : out std_logic_vector(3 downto 0));
end DWF_dp_simd_addc_test;

architecture rtl of DWF_dp_simd_addc_test is
begin
  DWF_dp_simd_addc (a => op1, b => op2, cin => c_in,
                   no_confs => 3, conf => config_no,
                   s => sum, cout => c_out);
end rtl;
```

## Verilog Example

```
module DWF_dp_simd_addc_test (op1, op2, c_in, config_no, sum, c_out);

    input  signed [31:0] op1, op2;
    input          [3:0] c_in;
    input          [1:0] config_no;
    output signed [31:0] sum;
    output          [3:0] c_out;
    reg    signed [31:0] sum;
    reg          [3:0] c_out;

    // Passes the parameters to the function
    parameter width      = 32;
    parameter no_confs   = 3;

    // add "$SYNOPSYS/dw/sim_ver" to the search path for simulation
    `include "DW_dp_simd_addc_function.inc"

    always @* begin
        DWF_dp_simd_addc_tc (op1, op2, c_in, config_no, sum, c_out);
    end

endmodule
```

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