DW_bc_7

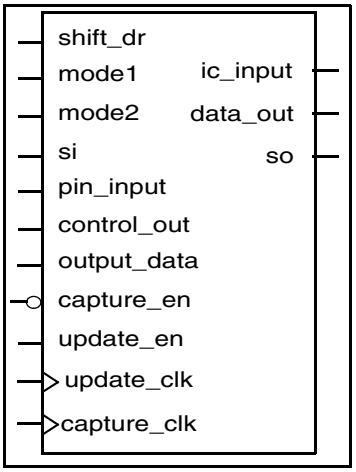
Boundary Scan Cell Type BC_7

Version, STAR and Download Information: IP Directory

Features and Benefits

Revision History

- IEEE Standard 1149.1 compliant
- Synchronous or asynchronous scan cells with respect to `tck`
- Supports the standard instructions: EXTEST, SAMPLE/PRELOAD, and BYPASS
- Supports the optional instructions INTEST, RUNBIST, CLAMP, and HIGHZ



Description

DW_bc_7 is a boundary scan cell used to control and observe both input and output data. DW_bc_7 is intended to be used with a type BC_2 boundary scan cell to form a bidirectional cell. The DW_bc_7 cell controls the input and output and the DW_bc_2 cell controls the enable of the bidirectional pad.

The Boundary Scan Description Language (BSDL) description of this cell is of type BC_7 described in the BSDL package STD_1149_1_1990.

The DW_bc_7 cell may be synchronous or asynchronous with respect to `tck` (Test Clock system pin) depending on the port connections.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
capture_clk	1 bit	Input	Clocks data into the capture stage
update_clk	1 bit	Input	Clocks data into the update stage
capture_en	1 bit	Input	Enable for data clocked into the capture stage, active low
update_en	1 bit	Input	Enable for data clocked into the update stage, active high
shift_dr	1 bit	Input	Enables the boundary scan chain to shift data one stage toward its serial output (tdo)
mode1	1 bit	Input	Determines whether data_out is controlled by the boundary scan cell or by the `output_data` signal
mode2	1 bit	Input	Determines whether ic_input is controlled by the boundary scan cell or by the `pin_input` signal
si	1 bit	Input	Serial path from the previous boundary scan cell

Table 1-1 Pin Description (Continued)

Pin Name	Width	Direction	Function
pin_input	1 bit	Input	IC system input pin
control_out	1 bit	Input	Control signal for the output enable
output_data	1 bit	Input	IC output logic signal
ic_input	1 bit	Output	IC input logic signal
data_out	1 bit	Output	Output data
so	1 bit	Output	Serial path to the next boundary scan cell

Table 1-2 Synthesis Implementations

Implementation Name	Function	License Feature Required
str	Synthesis model	DesignWare or Test-IEEE-STD-1149-1

Table 1-3 Simulation Models

Model	Function
DW04.DW_BC_7_CFG_SIM	Design unit name for VHDL simulation
dw/dw04/src/DW_bc_7_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW_bc_7.v	Verilog simulation model source code

The `mode` signal gives the Test Access Port (TAP) instructions control of the boundary scan cell. Table 1-4 lists the required values of the `mode` signal for each of the TAP instructions that DW_bc_7 supports.

Table 1-4 Mode Signal Generation for DW_bc_7

Instruction	mode1	mode2
EXTEST	1	0
SAMPLE/PRELOAD	0	0
INTEST	0	1
CLAMP	1	X
RUNBIST	X	X
BYPASS	0	0

Table 1-5 lists the connections for asynchronous boundary scan chains.

Table 1-5 Port Connections for Asynchronous Boundary Scan Chains

DW_bc_7 Port Name	Connection
capture_clk	clock_dr from TAP controller
update_clk	update_dr from TAP controller
capture_en	Logic zero
update_en	Logic one
shift_dr	shift_dr from TAP controller
mode1	mode1 generation logic
mode2	mode2 generation logic
si	so from previous boundary scan cell
pin_input	IC system input pin
control_out	Output enable signal
output_data	IC output logic
ic_input	IC input logic
data_out	System output pin
so	si of next boundary scan cell (si of DW_bc_2)

Table 1-6 lists the connections for synchronous boundary scan chains.

Table 1-6 Port Connections for Synchronous Boundary Scan Chains

DW_bc_7 Port Name	Connection
capture_clk	tck from system pin
update_clk	tck_n from system pin
capture_en	sync_capture_en from TAP controller
update_en	sync_update_dr from TAP controller
shift_dr	shift_dr from TAP controller
mode1	mode1 generation logic
mode2	mode2 generation logic
si	so from previous boundary scan cell
pin_input	IC system input pin
control_out	Output enable signal
output_data	IC output logic
ic_input	IC input logic
data_out	System output pin
so	si of next boundary scan cell

Related Topics

- Application Specific – JTAG Overview
- DesignWare Building Block IP User Guide

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW_bc_7_inst is
  port (inst_capture_clk : in std_logic;  inst_update_clk  : in std_logic;
        inst_capture_en  : in std_logic;  inst_update_en   : in std_logic;
        inst_shift_dr    : in std_logic;  inst_mode1       : in std_logic;
        inst_mode2       : in std_logic;  inst_si          : in std_logic;
        inst_pin_input   : in std_logic;  inst_control_out : in std_logic;
        inst_output_data : in std_logic;  ic_input_inst    : out std_logic;
        data_out_inst    : out std_logic; so_inst          : out std_logic );
end DW_bc_7_inst;

architecture inst of DW_bc_7_inst is
begin

  -- Instance of DW_bc_7
  U1 : DW_bc_7
    port map (capture_clk => inst_capture_clk,
              update_clk => inst_update_clk,   capture_en => inst_capture_en,
              update_en => inst_update_en,   shift_dr => inst_shift_dr,
              mode1 => inst_mode1,   mode2 => inst_mode2,   si => inst_si,
              pin_input => inst_pin_input,   control_out => inst_control_out,
              output_data => inst_output_data,   ic_input => ic_input_inst,
              data_out => data_out_inst,   so => so_inst );
end inst;

-- pragma translate_off
configuration DW_bc_7_inst_cfg_inst of DW_bc_7_inst is
  for inst
  end for; -- inst
end DW_bc_7_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_bc_7_inst(inst_capture_clk, inst_update_clk, inst_capture_en,
                    inst_update_en, inst_shift_dr, inst_mode1, inst_mode2,
                    inst_si, inst_pin_input, inst_control_out,
                    inst_output_data, ic_input_inst, data_out_inst, so_inst );
  input inst_capture_clk;
  input inst_update_clk;
  input inst_capture_en;
  input inst_update_en;
  input inst_shift_dr;
  input inst_mode1;
  input inst_mode2;
  input inst_si;
  input inst_pin_input;
  input inst_control_out;
  input inst_output_data;
  output ic_input_inst;
  output data_out_inst;
  output so_inst;

  // Instance of DW_bc_7
  DW_bc_7
    U1 (.capture_clk(inst_capture_clk),    .update_clk(inst_update_clk),
        .capture_en(inst_capture_en),    .update_en(inst_update_en),
        .shift_dr(inst_shift_dr),    .mode1(inst_mode1),    .mode2(inst_mode2),
        .si(inst_si),    .pin_input(inst_pin_input),
         .control_out(inst_control_out),    .output_data(inst_output_data),
         .ic_input(ic_input_inst),    .data_out(data_out_inst),
         .so(so_inst) );
endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
January 2019	DWBB_201806.5	■ Updated example in "HDL Usage Through Component Instantiation - VHDL" on page 5 ■ Added this Revision History table and the document links on this page

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