DW_fp_i2flt

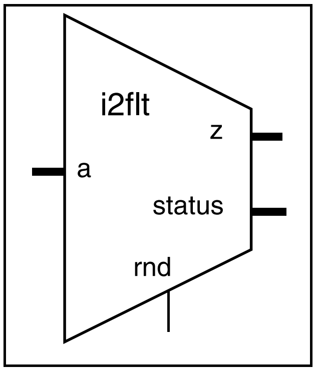
Integer to Floating-Point Converter

Version, STAR, and myDesignWare Subscriptions: IP Directory

Features and Benefits

Revision History

- The precision format is parameterizable for either IEEE single, double precision, or a user-defined custom format
- Accuracy conforms to IEEE 754 Floating-point standard
- DesignWare datapath generator is employed for better timing and area



Description

DW_fp_i2flt is an integer to floating-point converter that takes an integer number, a, to produce a floating-point number, z.

Component pins are described in Table 1-1 and configuration parameters are described in Table 1-2.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
a	*isize* bits	Input	Signed/unsigned integer number
rnd	3 bits	Input	Rounding mode; supports all rounding modes described in the *Datapath Floating-Point Overview*
z	(*sig_width* + *exp_width* + 1) bits	Output	Floating-point number
status	8 bits	Output	Status flags for the result z For details, see STATUS Flags in the *Datapath Floating-Point Overview.*

Table 1-2 Parameter Description

Parameter	Values	Description
sig_width	2 to 253 Default: 23	Word length of fraction field of floating-point number, z
exp_width	3 to 31 Default: 8	Word length of biased exponent of floating-point number, z
isize	(3 + *isign*) ≤ *isize* ≤ 512 Default: 32	Word length of integer number, a

Table 1-2 Parameter Description (Continued)

Parameter	Values	Description
isign	0 or 1 Default: 1	■ 0 = Unsigned integer number ■ 1 = Signed two's complement integer number

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
rtl	Area-optimized synthesis model	DesignWare
str	Delay-optimized synthesis model	DesignWare

Table 1-4 Simulation Models

Model	Function
DW02.DW_FP_I2FLT_CFG_SIM	Design unit name for VHDL simulation
dw/dw02/src/DW_fp_i2flt_sim.vhd	VHDL Simulation Model Source Code
dw/sim_ver/DW_fp_i2flt.v	Verilog Simulation Model Source Code

Table 1-5 Truth Table (*sig_width* = 10, *exp_width* = 5, *isize* = 16, *isign* = 1)

Description	a (Integer Format)	rnd	status	z (FP Format)
Zero	0000_0000_0000_0000	any	0000_0001	0000_0000_0000_0000
Normal Number	0001_1111_1111_1111	0	0010_0000	0111_0000_0000_0000
	0001_1111_1111_1111	1	0010_0000	0110_1111_1111_1111
	0001_1111_1111_1111	2	0010_0000	0111_0000_0000_0000
	0001_1111_1111_1111	3	0010_0000	0110_1111_1111_1111
	0001_1111_1111_1111	4	0010_0000	0111_0000_0000_0000
	0001_1111_1111_1111	5	0010_0000	0111_0000_0000_0000

DW_fp_i2flt block toggles 4 `status` bits among 8 bit: Zero flag, Infinity flag, Huge flag and Inexact flag.

Suppressing Warning Messages During Verilog Simulation

The Verilog simulation model includes macros that allow you to suppress warning messages during simulation.

To suppress all warning messages for all DWBB components, define the DW_SUPPRESS_WARN macro in either of the following ways:

- Specify the Verilog preprocessing macro in Verilog code:

  ```
  `define DW_SUPPRESS_WARN
  ```

- Or, include a command line option to the simulator, such as:

  `+define+DW_SUPPRESS_WARN` (which is used for the Synopsys VCS simulator)

The warning messages for this model include the following:

- If an invalid rounding mode has been detected on `rnd`, the following message is displayed:

  ```
  WARNING: <instance_path>:
      at time = <timestamp>: Illegal rounding mode.
  ```

  To suppress this message, use the DW_SUPPRESS_WARN macro explained earlier.

Related Topics

- Datapath Floating-Point Overview
- DesignWare Building Block IP User Guide

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DW_Foundation_comp.all;
-- If using numeric types from std_logic_arith package,
-- comment the preceding line and uncomment the following line:
-- use DWARE.DW_Foundation_comp_arith.all;

entity DW_fp_i2flt_inst is
  generic (
    inst_sig_width : POSITIVE := 23;
    inst_exp_width : POSITIVE := 8;
    inst_isize     : POSITIVE := 32;
    inst_isign     : INTEGER := 1
  );
  port (
    inst_a      : in std_logic_vector(inst_isize-1 downto 0);
    inst_rnd    : in std_logic_vector(2 downto 0);
    z_inst      : out std_logic_vector(inst_sig_width+inst_exp_width downto 0);
    status_inst : out std_logic_vector(7 downto 0)
  );
end DW_fp_i2flt_inst;


architecture inst of DW_fp_i2flt_inst is

begin

  -- Instance of DW_fp_i2flt
  U1 : DW_fp_i2flt
  generic map (
    sig_width => inst_sig_width,
    exp_width => inst_exp_width,
    isize => inst_isize,
    isign => inst_isign
  )
  port map (
    a => inst_a,
    rnd => inst_rnd,
    z => z_inst,
    status => status_inst
  );

end inst;

-- pragma translate_off
configuration DW_fp_i2flt_inst_cfg_inst of DW_fp_i2flt_inst is
   for inst
```

```
    end for;
end DW_fp_i2flt_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_fp_i2flt_inst( inst_a, inst_rnd, z_inst, status_inst );

parameter sig_width = 23;
parameter exp_width = 8;
parameter isize = 32;
parameter isign = 1;


input [isize-1 : 0] inst_a;
input [2 : 0] inst_rnd;
output [sig_width+exp_width : 0] z_inst;
output [7 : 0] status_inst;

    // Instance of DW_fp_i2flt
    DW_fp_i2flt #(sig_width, exp_width, isize, isign)
      U1 ( .a(inst_a), .rnd(inst_rnd), .z(z_inst), .status(status_inst) );

endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
July 2020	DWBB_201912.5	■ Added "Suppressing Warning Messages During Verilog Simulation" on page 3 ■ Added this Revision History table and the document links on this page

Copyright Notice and Proprietary Information

Destination Control Statement

All technical data contained in this publication is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the reader's responsibility to determine the applicable regulations and to comply with them.

Disclaimer

SYNOPSYS, INC., AND ITS LICENSORS MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Trademarks

Synopsys and certain Synopsys product names are trademarks of Synopsys, as set forth at https://www.synopsys.com/company/legal/trademarks-brands.html.

All other product or company names may be trademarks of their respective owners.

Free and Open-Source Software Licensing Notices

If applicable, Free and Open-Source Software (FOSS) licensing notices are available in the product installation.

Third-Party Links

Any links to third-party websites included in this document are for your convenience only. Synopsys does not endorse and is not responsible for such websites and their practices, including privacy practices, availability, and content.

Synopsys, Inc.
www.synopsys.com