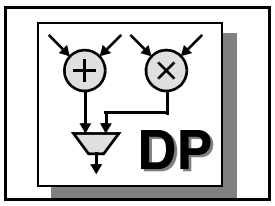

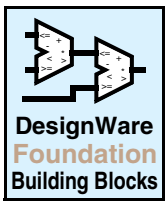

DWF_dp_sign_select functions

Sign Selection / Conditional Two's Complement

Version, STAR, and myDesignWare Subscriptions: IP Directory

Description

The DWF_dp_sign_select functions return the positive or negative (two's complement) value of argument `a` controlled by sign argument `s`. Argument `a` and the return value are both either signed (two's complement) or unsigned.

A signed return value has overflow for the value `DWF_dp_sign_select (-2`$^{\texttt{width-1}}$`, 1) = 2`$^{\texttt{width-1}}$, which cannot be represented as a signed number of `width` bits. The complement of an unsigned number always results in underflow (that is, a negative number cannot be represented as an unsigned), but the unsigned DWF_dp_sign_select can be meaningful for the conditional addition/subtraction in a larger unsigned expression.

Table 1-1 Function Names

Function Name	Description
DWF_dp_sign_select	VHDL unsigned sign select
DWF_dp_sign_select	VHDL signed (two's complement) sign select
DWF_dp_sign_select_uns	Verilog unsigned sign select
DWF_dp_sign_select_tc	Verilog signed (two's complement) sign select

Table 1-2 Argument Description

Argument Name	Type	Width	Description
a	Vector	width	Input data
s	Bit	1	Sign / complement control
DWF_dp_sign_select	Vector	width	Return value

Table 1-3 Parameter Description (Verilog)

Parameter	Values	Description
width	≥ 1	Word length of input `a` and return value

Verilog Include File: DW_dp_sign_select_function.inc

Functional Description

```
z[width-1:0] = DWF_dp_sign_select (a[width-1:0], s)

z[width-1:0] =  a[width-1:0]  if s == 0
             = -a[width-1:0]  else
```

For more information about the DesignWare datapath functions, refer to the topic titled Arithmetic – Datapath Functions Overview.

Related Topics

- Arithmetic – Datapath Functions Overview
- DesignWare Building Block IP User Guide

VHDL Example

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use DWARE.DW_dp_functions.all;
-- DWARE.DW_dp_functions_arith package if IEEE.std_logic_arith is used

entity DWF_dp_sign_select_test is
  port (a, b, c : in  signed(7 downto 0);
        s       : in  std_logic;
        z       : out signed(15 downto 0));
end DWF_dp_sign_select_test;

architecture rtl of DWF_dp_sign_select_test is
begin
  z <= DWF_dp_sign_select (a * b, s) + c;
end rtl;
```

Verilog Example

```
module DWF_dp_sign_select_test (a, b, c, s, z);

  input  signed  [7:0] a, b, c;
  input                s;
  output signed [15:0] z;

  // Passes the parameter to the function
  parameter width = 16;

  // add "$SYNOPSYS/dw/sim_ver" to the search path for simulation
  `include "DW_dp_sign_select_function.inc"

  assign z = DWF_dp_sign_select_tc (a * b, s) + c;

endmodule
```

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