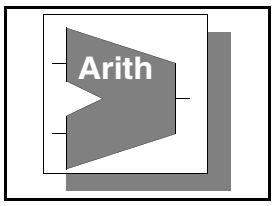
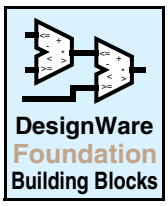




DW01_dec

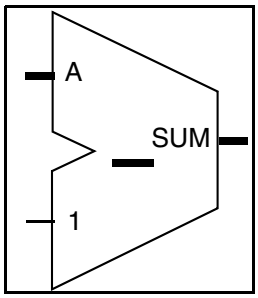
Decrementer

Version, STAR, and myDesignWare Subscriptions: IP Directory

Features and Benefits

- Parameterized word length

Revision History



Description

DW01_dec is a decrementer. DW01_dec subtracts 1 from an input number A to produce the output SUM.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
A	*width* bits	Input	Input data
SUM	*width* bits	Output	Decremented (A - 1)

Table 1-2 Parameter Description

Parameter	Values	Description
width	≥ 1	Word length of A and SUM

Table 1-3 Synthesis Implementations[a]

Implementation Name	Function	License Feature Required
rpl	Ripple-carry synthesis model	none
cla	Carry-look-ahead synthesis model	none
pparch	Delay-optimized flexible parallel-prefix	DesignWare
apparch	Area-optimized flexible architecture that can be optimized for area, for speed, or for area, speed	DesignWare

a. During synthesis, Design Compiler will select the appropriate architecture for your constraints. However, you may force Design Compiler to use one of the architectures described in this table. For more details, refer to the *DesignWare Building Block IP User Guide*.

Table 1-4 Simulation Models

Model	Function
DW01.DW01_DEC_CFG_SIM	Design unit name for VHDL simulation
dw/dw01/src/DW01_dec_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW01_dec.v	Verilog simulation model source code

Related Topics

- Math – Arithmetic Overview
- DesignWare Building Block IP User Guide

HDL Usage Through Operator Inferencing - VHDL

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;

entity  DW01_dec_oper is
  generic(wordlength: integer:=8);
  port(in1 : in STD_LOGIC_VECTOR(wordlength-1 downto 0);
       sum : out STD_LOGIC_VECTOR(wordlength-1 downto 0));
end DW01_dec_oper;

architecture oper of DW01_dec_oper is
  signal in_signed,sum_signed: SIGNED(wordlength-1 downto 0);
begin
  in_signed <= SIGNED(in1);
  -- infer the "-" subtraction operator
  sum_signed <= in_signed - 1;
  sum <= STD_LOGIC_VECTOR(sum_signed);
end oper;
```

HDL Usage Through Operator Inferencing - Verilog

```
module DW01_dec_oper(in,sum);
  parameter wordlength = 8;

  input [wordlength-1:0] in;
  output [wordlength-1:0] sum;

  assign  sum = in - 1;
endmodule
```

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW01_dec_inst is
  generic ( inst_width : NATURAL := 8 );
  port ( inst_A   : in std_logic_vector(inst_width-1 downto 0);
         SUM_inst : out std_logic_vector(inst_width-1 downto 0) );
end DW01_dec_inst;

architecture inst of DW01_dec_inst is
begin

  -- Instance of DW01_dec
  U1 : DW01_dec
    generic map ( width => inst_width )
    port map ( A => inst_A, SUM => SUM_inst );
end inst;

-- pragma translate_off
configuration DW01_dec_inst_cfg_inst of DW01_dec_inst is
  for inst
  end for; -- inst
end DW01_dec_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW01_dec_inst( inst_A, SUM_inst );

  parameter width = 8;

  input [width-1 : 0] inst_A;
  output [width-1 : 0] SUM_inst;

  // Instance of DW01_dec
  DW01_dec #(width)
    U1 ( .A(inst_A), .SUM(SUM_inst) );

endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
March 2019	DWBB_201903.0	■ Removed Table 1-4, “Obsolete Synthesis Implementations”
January 2019	DWBB_201806.5	■ Updated example in “HDL Usage Through Component Instantiation - VHDL” on page 5 ■ Added this Revision History table and the document links on this page

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