SYNOPSYS®

DesignWare® Building Block IP

Release Notes

DesignWare Building Blocks — Product Code: 2925-0

DWBB_202212.5 Release for Synthesis

Supported Synthesis Releases:
See Table 1-2 on page 7

Supported Synplify FPGA Releases:
See Table 1-3 on page 8

Version DWBB_202212.5
U-2022.12-SP5
July 2023

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Contents

Release Notes: Building Block IP

This document contains the latest information about the Synopsys® DesignWare® Building Block IP DWBB_202212.5 IP Release for Design Compiler®, Fusion Compiler™, Synplify Pro®, and VCS® MX. This library of IP was previously called the DesignWare Foundation (DWF) Library. The older DWF nomenclature appears in licensing and file naming. This release is based on the U-2022.12-SP5 Synthesis release.

This document also contains release information for DesignWare Building Block IP in FPGA synthesis (Synplify® tools).

The following lists the topics in this document:

1.1 Features and Changes in DWBB_202212.5 / U-2022.12-SP5

This release contains no technical bug fixes or enhancements.

This section lists additions and updates for the current release of DesignWare Building Block IP. This section also describes the release information and issues related to using DesignWare Building Block IP with Synopsys Synplify Premier and Synplify Premier with Design Planner tools.

This release contains the following updates. In the following table, links in the left column (if present) go to more information in the STARs on the Web (SotW) system.

Table 1-1 STARs Resolved in DWBB_202212.5 (U-2022.12-SP5)

Component	STAR ID	Type	Description
DW_ln	9001562707	Bug	DW_ln ulp errors are larger than the documented err_range ■ The documented values for err_range have been corrected
DW_lp_piped_div DW_lp_piped_ecc DW_lp_piped_fp_add DW_lp_piped_fp_sum3 DW_lp_piped_mult DW_lp_piped_prod_sum DW_lp_piped_sqrt	4819539	Bug	VHDL simulation model of DW_lp_fp_piped_add returns uninitialized output
DW_arb_rr	4833770	Enhancement	In the datasheet, clarify the how the `enable` signal works

1.2 Known Problems and Limitations

This section lists known problems and limitations. There are no known problems to report at this time.

1.3 Version Compatibility with Tools

This section presents compatible versions of related Synopsys tools.

For the latest compatibility information, view this document on the Synopsys website:
https://www.synopsys.com/dw/doc.php/doc/dwf/manuals/dwbb_relnotes/index.html

1.3.1 Version Compatibility with Synopsys Synthesis Tools

Table 1-2 shows which releases work with the supporting releases of Synopsys synthesis tools.

Table 1-2 Compatibility with Design Compiler and Fusion Compiler Synthesis Tools

DesignWare Building Block IP Release	Design Compiler/Fusion Compiler Release														
	2022.12 -SP5	2022.12 -SP4	2022.12 -SP2	2022.12 -SP1	2022.12	2022.03 -SP5	2022.03 -SP4	2022.03 -SP3	2022.03 -SP2	2022.03 -SP1	2022.03	2021.06 -SP5	2021.06 -SP4	2021.06 -SP3	2021.06 -SP2
DWBB_202212.5	Bundled														
DWBB_202212.4		Bundled													
DWBB_202212.2			Bundled												
DWBB_202212.1				Bundled											
DWBB_202212.0					Bundled										
DWBB_202203.5						Bundled									
DWBB_202203.4							Bundled								
DWBB_202203.3								Bundled							
DWBB_202203.2									Bundled						
DWBB_202203.1										Bundled					
DWBB_202203.0											Bundled				
DWBB_202106.5												Bundled			
DWBB_202106.4													Bundled		
DWBB_202106.3														Bundled	
DWBB_202106.2															Bundled

1.3.2 Synplify FPGA Synthesis Tool Compatibility

Table 1-3 shows which DesignWare Building Block IP releases work with the Synplify Premier releases:

Table 1-3 Version Compatibility with Synplify Premier Releases

Designware Building Block IP / Synthesis Tool Release	Synplify Premier Release											
	2023.03	2023.03	2022.09 -SP2	2022.09 -SP2	2022.09 -SP1	2022.09	2021.09 -SP2	2021.09 -SP2	2021.09 -SP1	2021.09 -SP1	2021.09 -SP1	2021.09
DWBB_202212.5/ U-2022.12-SP5	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_202212.4/ U-2022.12-SP4	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_202212.2/ U-2022.12-SP2	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_202212.1/ U-2022.12-SP1	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_202212.0/ U-2022.12	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_202203.5/ T-2022.03-SP5	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_202203.4/ T-2022.03-SP4	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_202203.3/ T-2022.03-SP3	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_202203.2/ T-2022.03-SP2	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_202203.1/ T-2022.03-SP1	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_202203.0/ T-2022.03	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_202106.5/ S-2021.06-SP5	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_202106.4/ S-2021.06-SP4	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_202106.3/ S-2021.06-SP3	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_202106.2/ S-2021.06-SP2	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔

1.3.3 VCS MX Compatibility

The DWBB_202212.5 release of DesignWare Building Block IP works with VCS MX.

1.4 Features and Changes in Previous Versions (History)

1.4.1 DWBB_202212.4 / U-2022.12-SP4

This release contains the following updates. In the following table, links in the left column (if present) go to more information in the STARs on the Web (SotW) system.

Table 1-4 STARs Resolved in DWBB_202212.4 (U-2022.12.SP4)

Component	STAR ID	Type	Description
DW_log2	9001562788	Bug	DW_log2 ulp errors are larger than err_range
DW_exp2	9001562658	Bug	DW_exp2 ulp errors are larger than err_range
DW_fp_div DW_fp_div_DG DW_fp_div_seq DW_lp_piped_fp_div	3638931	Bug	TINY flag is not behaving as the interpretation of the IEEE 754 standard states
DW_reset_sync	4351988	Enhancement	Update DW_reset_sync block diagram in datasheet
DW01_binenc DW01_prienc DW_lza DW_pricod DW_shifter	4760257	Enhancement	_function.inc generates errors in third-party simulation tool

1.4.2 DWBB_202212.3 / U-2022.12-SP3

The DesignWare Building Blocks IP library was not updated for this release.

1.4.3 DWBB_202212.2 / U-2022.12-SP2

This release contains the following updates. In the following table, links in the left column (if present) go to more information in the STARs on the Web (SotW) system.

Table 1-5 STARs Resolved in DWBB_202212.2 (U-2022.12-SP2)

Component	STAR ID	Type	Description
DW02_multp DW02_tree DW_squarep	4360627	Enhancement	Remove the carry-save randomness warnings from the warnings that are suppressed with DW_SUPPRESS_WARN

1.4.4 DWBB_202212.1 / U-2022.12-SP1

This release contains the following updates. In the following table, links in the left column (if present) go to more information in the STARs on the Web (SotW) system.

Table 1-6 STARs Resolved in DWBB_202212.1 (U-2022.12-SP1)

Component	STAR ID	Type	Description
DW_ecc	4479241	Enhancement	Add embedded script to disable ungrouping
DW_ecc DW_lp_piped_ecc	4548964	Bug	For some configurations, the simulation model is unable to detect and correct 1-bit errors in the most significant bit

1.4.5 DWBB_202212.0 / U-2022.12

This release contains the following updates. In the following table, links in the left column (if present) go to more information in the STARs on the Web (SotW) system.

Table 1-7 STARs Resolved in DWBB_202212.0 (U-2022.12)

Component	STAR ID	Type	Description
DW_div	4487770	Bug	The datasheet is missing the 'lut' synthesis implementation

1.4.6 DWBB_202203.5 / T-2022.03-SP5

This release contains the following updates. In the following table, links in the left column (if present) go to more information in the STARs on the Web (SotW) system.

Table 1-8 STARs Resolved in DWBB_202203.5 (T-2022.03-SP5)

Component	STAR ID	Type	Description
DW_fp_exp	3310285	Bug	The datasheet shows incorrect maximum ulp error
DW_fp_exp2	3310283	Bug	The datasheet shows incorrect maximum ulp error
DW_fp_log2	3315120	Bug	The datasheet shows incorrect maximum ulp error

1.4.7 DWBB_202203.4 / T-2022.03-SP4

This release contains the following updates. In the following table, links in the left column (if present) go to more information in the STARs on the Web (StoW) system.

Table 1-9 STARs Resolved in DWBB_202203.4 (T-2022.03-SP4)

Component	STAR ID	Type	Description
DW_crc_p	3922446	Bug	Synthesis fatal for certain configurations
DW_log2 DW_fp_log2	4320062	Bug	Numerical error is larger than 2 ulp when `op_width` >= 39
DW_log2 DW_fp_log2	4337513	Enhancement	Improve the Verilog simulation model when `op_width` >= 39
DW_iir_sc	9001520839	Bug	Fusion Compiler fails for DW_iir_sc when negative parameter values are used

1.4.8 DWBB_202203.3 / T-2022.03-SP3

This release contains the following updates. In the following table, links in the left column (if present) go to more information in the STARs on the Web (StoW) system.

Table 1-10 STARs Resolved in DWBB_202203.3 (T-2022.03-SP3)

Component	STAR ID	Type	Description
DW_asymfifoctl_2c_df	3463163	Bug	Synthesis error when parameter *verif_en* is set to 2 or 3
DW_fifo_2c_df DW_fifoctl_2c_df	3850715	Enhancement	Enhance source domain output flags during requested clearing sequences
Library	3973672	Enhancement	Improve efficiency of the dw_analyze_hybrid script
DW_squarep DW02_multp DW02_tree	4306649	Enhancement	In the datasheet, clarify that the *verif_en* parameter affects only the simulation model and not the synthesis model

1.4.9 DWBB_202203.2 / T-2022.03-SP2

This release contains the following updates. In the following table, links in the left column (if present) go to more information in the STARs on the Web (StoW) system.

Table 1-11 STARs Resolved in DWBB_202203.2 (T-2022.03-SP2)

Component	STAR ID	Type	Description
DW01_csa	3825567	Enhancement	Enhance datasheet for usage of HDL operator
DW_ecc	3851321	Enhancement	Clarify error detection/correction behavior in datasheet
DW_fp_mult DW_fp_mult_DG	4175244	Enhancement	Add a new parameter (*en_ubr_flag*) that enables a status flag (`status[6]`) for “underflow before rounding” conditions
DW02_multp	4219789	Bug	Correct error in Table 1-5 of the datasheet for the `out1` signal when *verif_en* = 3

1.4.10 DWBB_202203.1 / T-2022.03-SP1

This release contains the following updates. In the following table, links in the left column (if present) go to more information in the STARs on the Web (StoW) system.

Table 1-12 STARs Resolved in DWBB_202203.1 (T-2022.03-SP1)

Component	STAR ID	Type	Description
DW_fp_div DW_fp_div_DG	3947569	Bug	TINY status behaves incorrectly in 'str' implementation when ieee_compliance=0
DW_fp_div DW_fp_div_DG	3928902	Enhancement	Add a new parameter (*en_ubr_flag*) that enables a status flag (`status[6]`) for “underflow before rounding” conditions

1.4.11 DWBB_202203.0 / T-2022.03

This release contains no technical bug fixes or enhancements.

1.4.12 DWBB_202106.5 / S-2021.06-SP5

This release contains the following updates. In the following table, links in the left column (if present) go to more information in the STARs on the Web (StoW) system.

Table 1-13 STARs Resolved in DWBB_202106.5 (S-2021.06-SP5)

Component	STAR ID	Type	Description
DW_lp_fp_multifunc DW_lp_fp_multifunc_DG	9001472756	Bug	When ieee_compliance=1, tiny status bit error with exp2()
DW_lp_fp_multifunc DW_lp_fp_multifunc_DG	9001517959	Bug	The sign bit of zero output from sin/cos for special inputs does not match IEEE
DW_asymfifoctl_2c_df	3961887	Bug	Errors in datasheet waveforms with clr_* signal activity
DWBB Library	3975501	Enhancement	Enhance dw_analyze_idp script to improve execution time
DW_asymfifoctl_s1_df DW_asymfifoctl_s1_sf DW_asymfifoctl_s2_sf DW_asymfifo_s1_df DW_asymfifo_s1_sf DW_asymfifo_s2_sf	3984733	Bug	Replace GTECH FFs with RTL in DW_ASYMFIFOCTL_IN_WRAPPER (Fusion Compiler only)
DW02_multp DW02_tree DW_exp2 DW_lp_fp_multifunc DW_lp_fp_multifunc_DG DW_lp_multifunc DW_lp_multifunc_DG DW_squarep	3988003	Enhancement	Redundant pragmas in Verilog simulation model cause “Warning-[PHNE] Pragma has no Effect” warning

1.4.13 DWBB_202106.4 / S-2021.06-SP4

This release contains the following updates. In the following table, links in the left column (if present) go to more information in the STARs on the Web (StoW) system.

Table 1-14 STARs Resolved in DWBB_202106.4 (S-2021.06-SP4)

Component	STAR ID	Type	Description
DW_lp_piped_ecc	3754297	Bug	Simulation model causes VCS error in NLP flow for DW_lp_piped_ecc with large width
DW_fifo_2c_df DW_fifoctl_2c_df	3759415	Bug	DW_fifoctl_2c_df datasheet error in describing clr_sync_s/clr_sync_d used for resetting
DW_fifo_2c_df DW_fifoctl_2c_df	3837598	Bug	Datasheet error in describing clr_sync_s/clr_sync_d used for resetting
DW_ecc	3948056	Bug	Some errors that have more than two bits in error should be flagged as uncorrectable ('err_multiple'=1), but the simulation model does not flag as uncorrectable and, instead, mis-corrects the data

1.4.14 DWBB_202106.3 / S-2021.06-SP3

This release contains the following updates. In the following table, links in the left column (if present) go to more information in the STARs on the Web (StoW) system.

Table 1-15 STARs Resolved in DWBB_202106.3 (S-2021.06-SP3)

Component	STAR ID	Type	Description
DW_fp_cmp DW_fp_cmp_DG	3751139	Enhancement	Datasheet to explain DW_fp_cmp does not set the TINY or HUGE status
DW02_tree DW_squarep	3884129	Bug	Syntax error during simulation when DW_SUPPRESS_WARN is defined
Library Sample SotW: DW_div	3880900	Bug	Files in syn_ver/sim_ver of Fusion Compiler installation directory are missing

1.4.15 DWBB_202106.2 / S-2021.06-SP2

This release contains the following updates. In the following table, links in the left column (if present) go to more information in the STARs on the Web system.

Table 1-16 STARs Resolved in DWBB_202106.2 (S-2021.06-SP2)

Component	STAR ID	Type	Description
DW_asymfifoctl_2c_df DW_fifo_2c_df DW_fifoctl_2c_df	9001222511	Bug	Synthesis error when instantiating DW_*_2c_df and configured with clk_ratio=0
DW_reset_sync	3734661	Bug	Datasheet timing diagrams not updated
DW_lp_piped_fp_add DW_lp_piped_fp_sum3	3751139	Bug	The parameter order is not consistent between datasheet and RTL
DW_pulse_sync DW_pulseack_sync	3837593	Bug	Incorrect description of *pulse_mode* in datasheets

1.4.16 DWBB_202106.1 / S-2021.06-SP1

This release contains the following updates. In the following table, links in the left column go to more information in the STARs on the Web system.

Table 1-17 STARs Resolved in DWBB_202106.1 (S-2021.06-SP1)

Component	STAR ID	Type	Description
DW_ecc	3734661	Enhancement	LINT check reports warnings “[WMIA-L] Width mismatch in assignment”
DW_fp_cmp DW_fp_cmp_DG	3732029	Bug	Need datasheet update on z0/z1 output when ieee_compliance = 0
DW_lp_piped_fp_div	3714278	Bug	DW_lp_piped_fp_div VHDL simulation model compile error for "in_reg=stages=1, out_reg=0"
DW_lp_piped_fp_recip	9001427904	Bug	DW_lp_piped_fp_recip VHDL/Verilog sim models mismatch RTL *in_reg*=1, *no_pm*=1
DW_div_sat	9001238068	Bug	The functional inference of DW_div_sat aborts with ELAB-352 error
DW_ecc	9001219474	Bug	Simulation model causes VCS error in NLP flow for DW_ecc with large width
DW_dct_2d	9000554173	Bug	The *idct_mode* parameter does not work reliably when the input “enable” is not held HIGH.

1.4.17 DWBB_202106.0 / S-2021.06

This release contains the following updates.

- The Design Compiler and Fusion Compiler tools can now display information about updates to DWBB IP that have been released.

  The `report_synlib_history` command displays updates as early as P-2019.03 release. For releases prior to P, you can find similar details in the text file located at:

  $SYNOPSYS/dw/doc/manuals/dwbb_history.txt

  For information about the output, see the man page for the `report_synlib_history` command.

Table 1-18 STARs Resolved in DWBB_202106.0 (S-2021.06)

Component	STAR ID	Type	Description
DW_fp_addsub_DG DW_fp_addsub DW_fp_div DW_fp_dp2 DW_fp_dp3 DW_fp_dp4 DW_fp_flt2i DW_fp_i2flt DW_fp_invsqrt DW_fp_mult_DG DW_fp_mult DW_fp_recip DW_fp_sqrt DW_fp_square DW_fp_sum3 DW_fp_sum4 DW_ifp_fp_conv	3625874	Enhancement	Problem with simulation at $time=0 when rounding happens
DW_fp_dp2 DW_fp_mac DW_fp_mac_DG DW_fp_mult DW_fp_mult_DG DW_lp_piped_fp_mult	3638672	Enhancement	TINY flag is not behaving as the interpretation of the IEEE 754 standard states

1.4.18 DWBB_202009.5 / R-2020.09-SP5

This release contains the following updates. Links in the left column of the table (if present) go to more information in the STARs on the Web system.

Table 1-19 STARs Resolved in DWBB_202009.5 (R-2020.09-SP5)

Component	STAR ID	Type	Description
DW_fp_div_seq	3580221	Bug	Erroneous DW_fp_div_seq assertion fail
DW_lp_piped_fp_recip	3601858	Enhancement	DW_lp_piped_fp_recip datasheet fix

1.5 Obsoleted IP for New Designs

DesignWare Building Block IP components are occasionally removed from the library. The process of removing components occurs in three stages over a period of at least two years.

1.5.1 Stage 1: Notification of Obsoleted IP

The first stage in obsoleting IP is a notification that the IP will not be supported in the future. You can still simulate and synthesize the IP, but a warning is issued during simulation.

There is currently no DesignWare Building Block IP at this stage.

1.5.2 Stage 2: Notification of Obsoleted Simulation Models

The second stage of the IP obsolescence is to remove the simulation model from the library. This occurs approximately 1 year from the time of the announcement that a particular IP is being obsoleted for new designs. Simulation is not possible, but synthesis of old designs still is possible.

There is currently no DesignWare Building Block IP at this stage.

1.5.3 Stage 3: Notification of Obsoleted Synthesis Models

The third and final stage of the IP obsolescence process is to remove the remaining synthesis model from the library. This occurs approximately 2 years from the time of the announcement that a particular IP is being obsoleted for new designs. Simulation and synthesis is not possible.

The following DesignWare Building Block IP is at stage 3 of obsolescence: **none**.

1.5.4 Notification of Obsoleted Synthesis Implementations

There are no recent obsoleted synthesis implementations.

1.6 Installation

DesignWare Building Block IP is installed with your Design Compiler synthesis release. If you install a patch to Design Compiler, refer to "When to Run the Reanalysis Scripts" on page 19.

1.6.1 How Can I Tell Which DesignWare Building Block IP Version Is Installed?

One way to view which DesignWare Building Block IP library you currently have installed on your UNIX system is to issue the following command:

```
% cat $SYNOPSYS/dw/version
```

The string that is returned looks something like this:

```
U-2022.12-DWBB_202212.5
```

The "U-2022.12" portion indicates the Synthesis base release. The "DWBB_202212.5" portion indicates the DesignWare Building Block IP release, which uses the YYYYMM.S format (where 'S' is the service pack number).

1.6.2 Installation of DesignWare Building Block IP for FPGA Synthesis

The DesignWare Building Block IP installation for FPGA synthesis is the same process as for the Synopsys synthesis tools. For details, refer to "Installation" on page 19. You can use an existing Design Compiler or Fusion Compiler installation without modification for FPGA synthesis, as long as the version is compatible (see Table 1-2 on page 7 for version compatibility).

1.6.3 Version Label for Technical Support

For future reference, a file exists under $SYNOPSYS/dw called "version", which contains the release version label. You need to know this label when contacting Synopsys technical support.

1.6.4 When to Run the Reanalysis Scripts

There are two special script files included with each DesignWare Building Block IP release that reanalyze your DesignWare Building Block IP source files. When run, the dw_analyze_syn.csh or dw_analyze_sim.csh script reanalyzes all existing Design Compiler and VCS MX components in your $SYNOPSYS/dw/ or $VCS_HOME/dw/ tree to ensure compatibility with newer versions of Synopsys Synthesis releases.

You must run the appropriate script for either of the following situations:

- When you receive a patch to Design Compiler that does not include DesignWare Building Block IP, or if you add another tool after installing a Synopsys synthesis tool, you must do the following:

```
setenv SYNOPSYS path
set path = (${SYNOPSYS}/platform/syn/bin $path)
setenv LM_LICENSE_FILE ${SYNOPSYS}/admin/license/key:$LM_LICENSE_FILE
cd $SYNOPSYS/dw/scripts
./dw_analyze_syn.csh
egrep -i 'warning|error' $SYNOPSYS/dw_analyze_syn.*.log
```

- When you receive a patch to VCS MX that does not include DesignWare Building Block IP, or if you add another tool after VCS MX installation, you must do the following for every target platform:

```
set path = (${VCS_HOME}/platform/bin $path) # VCS MX
setenv LM_LICENSE_FILE ${VCS_HOME}/admin/license/key:$LM_LICENSE_FILE
cd $VCS_HOME/dw/scripts
./dw_analyze_sim.csh
egrep -i 'warning|error' $VCS_HOME/dw_analyze_sim.log
```

path is the directory location where DesignWare Building Block IP and Synopsys synthesis and simulation tools have been installed (for example, "/synopsys/U-2022.12" or "/synopsys/VCS_mxversion").

platform is one of the following: sparc64, sparcOS5, Linux, or any supported platform.

The reanalyze_sim.csh script is also available, along with dw_analyze_sim.csh. It is a simple reanalyze script that is independent of versions and the installation location of DesignWare Building Block IP.

1.7 Documentation

1.7.1 DesignWare Building Block IP Datasheets and Manuals

PDF files containing the complete set of current DesignWare Building Block IP datasheets and manuals exist in the directory:

```
$SYNOPSYS/dw/doc
```

The entry document is the *DesignWare Building Blocks IP User Guide*.

The latest documentation is also available on the Synopsys website at the following location:

https://www.synopsys.com/dw/buildingblock.php

To search for any IP product, you can use the following location:

https://www.synopsys.com/dw/ipsearch.php

In the results, use the "More Information" link to navigate to documents for the component.

1.7.2 FPGA Synthesis Documentation

For Synplify Premier tool and FPGA synthesis information, see the *Synopsys FPGA Synthesis User Guide*.

1.8 Synopsys Statement on Inclusivity and Diversity

Synopsys is committed to creating an inclusive environment where every employee, customer, and partner feels welcomed. We are reviewing and removing exclusionary language from our products and supporting customer-facing collateral. Our effort also includes internal initiatives to remove biased language from our engineering and working environment, including terms that are embedded in our software and IPs. At the same time, we are working to ensure that our web content and software applications are usable to people of varying abilities. You may still find examples of non-inclusive language in our software or documentation as our IPs implement industry-standard specifications that are currently under review to remove exclusionary language.

1.9 Getting Help

1.9.1 Web Resources

- Fast access to DWBB component instantiation code snippets, function inference snippets (where appropriate), and links to documentation:

  http://www.synopsys.com/dw/buildingblock.php

- To subscribe to receive proactive notifications on new product releases, information on Synopsys Technical Action Requests (STARs), product updates, and more (requires SolvNet login):

  https://www.synopsys.com/dw/mydesignware.php

- Up-to-date information about the latest DesignWare Library IP:

  https://www.synopsys.com/designware-ip.html

- General Synopsys Licensing (SCL) information:

  https://www.synopsys.com/keys

1.9.2 DesignWare IP Component Subscriptions

For components you are entitled to, you can subscribe to receive notifications on new product releases, Synopsys Technical Action Request (STAR) reports, product updates and more at the following page:

https://www.synopsys.com/dw/mydesignware.php

1.9.3 STARs on the Web (SotW)

You must review all STARs on the Web (SotWs) associated with your product. SotWs are considered a part of the Synopsys documentation suite, and show critical information related to your product. To review product SotWs, refer to the DesignWare IP product information:

To see STAR reports, go to the following link and navigate to the desired component, which lists the link for the Open and/or Closed STARs reports:

https://www.synopsys.com/dw/buildingblock.php

1.9.4 Customer Support

Synopsys provides various methods for contacting Customer Support, as follows:

1. Prepare the following debug information, if applicable:
   - When using the Synopsys coreConsultant or coreAssembler tool, for environment set-up problems or failures with configuration, simulation, or synthesis, select the following menu:

     File > Build Debug Tar-file

     Check all the boxes in the dialog box that apply to your issue. This option gathers all the Synopsys product data needed to begin debugging an issue and writes it to the <*core tool startup directory*>/debug.tar.gz file.

- For simulation issues outside of coreConsultant or coreAssembler:
  - Create a waveforms file (such as VPD or VCD).
  - Identify the hierarchy path to the DesignWare instance.
  - Identify the timestamp of any signals or locations in the waveforms that are not understood.

- *For the fastest response*, enter a case through SolvNetPlus:

a. https://solvnetplus.synopsys.com

Note SolvNetPlus does not support Internet Explorer. Use a supported browser such as Microsoft Edge, Google Chrome, Mozilla Firefox, or Apple Safari.

b. Click the **Cases** menu and then click **Create a New Case** (below the list of cases).

c. Complete the mandatory fields that are marked with an asterisk and click **Save**.

Make sure to include the following:

- **Product L1:** DesignWare Building Block IP
- **Product L2:** Select the category of the component (such as Math_Arithmetic)
- **Product L3**: Select the specific DesignWare Building Block IP component, if known

d. After creating the case, attach any debug files you created.

- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
  - Include the Product L1, Product L2, and Product L3 names, and Version number in your e-mail so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood
  - Attach any debug files you created.
- Or, telephone your local support center:
  - North America:
    Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
  - All other countries:
    https://www.synopsys.com/support/global-support-centers.html