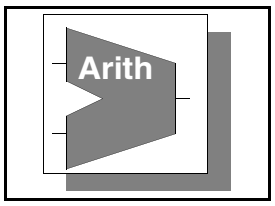
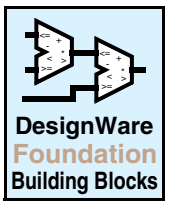




DW02_prod_sum1

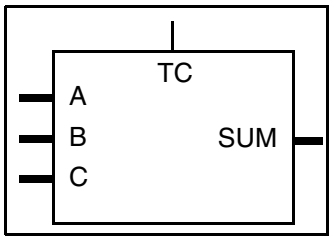
Multiplier-Adder

Version, STAR, and myDesignWare Subscriptions: IP Directory

Features and Benefits

- Parameterized word length

Revision History



Applications

- Multiply and accumulate
- Digital filtering

Description

DW02_prod_sum1 performs the mathematical operation SUM = A × B + C. This component is an extended version of DW02_mac, offering automatic sign extension on the output port SUM according to the parameter *SUM_width*. This component can also be considered a special case of DW02_prod_sum.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
A	*A_width* bits	Input	Input data
B	*B_width* bits	Input	Input data
C	*SUM_width* bits	Input	Input data
TC	1 bit	Input	Two's complement ■ 0 = Unsigned ■ 1 = Signed
SUM	*SUM_width* bits	Output	Sum of products

Table 1-2 Parameter Description

Parameter	Values	Description
A_width	≥ 1	Word length of A
B_width	≥ 1[a]	Word length of B
SUM_width	≥ 1	Word length of C and output SUM

a. For nbw implementation, *A_width* + *B_width* ≤ 36. Due to concern of implementation selection run time, a limitation is set for *A_width* and *B_width*.

Table 1-3 Synthesis Implementations[a]

Implementation Name	Function	License Feature Required
pparch	Delay-optimized flexible parallel-prefix	DesignWare
apparch	Area-optimized flexible architecture that can be optimized for area, for speed, or for area, speed	DesignWare

a. During synthesis, Design Compiler selects the appropriate architecture for your constraints. However, you may force Design Compiler to use one of the architectures described in this table.

Table 1-4 Simulation Models

Model	Function
DW02.DW02_PROD_SUM1_CFG_SIM	Design unit name for VHDL simulation
dw/dw02/src/DW02_prod_sum1_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW02_prod_sum1.v	Verilog simulation model source code

Related Topics

- Math – Arithmetic Overview
- DesignWare Building Block IP User Guide

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW02_prod_sum1_inst is
  generic ( inst_A_width : NATURAL := 5;
            inst_B_width : NATURAL := 5;
            inst_SUM_width : NATURAL := 11 );
  port ( inst_A   : in std_logic_vector(inst_A_width-1 downto 0);
         inst_B   : in std_logic_vector(inst_B_width-1 downto 0);
         inst_C   : in std_logic_vector(inst_SUM_width-1 downto 0);
         inst_TC  : in std_logic;
         SUM_inst : out std_logic_vector(inst_SUM_width-1 downto 0) );
end DW02_prod_sum1_inst;

architecture inst of DW02_prod_sum1_inst is
begin

  -- Instance of DW02_prod_sum1
  U1 : DW02_prod_sum1
    generic map ( A_width => inst_A_width,   B_width => inst_B_width,
                  SUM_width => inst_SUM_width )
    port map ( A => inst_A,   B => inst_B,   C => inst_C,
               TC => inst_TC,   SUM => SUM_inst );
end inst;

-- pragma translate_off
configuration DW02_prod_sum1_inst_cfg_inst of DW02_prod_sum1_inst is
  for inst
  end for; -- inst
end DW02_prod_sum1_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW02_prod_sum1_inst( inst_A, inst_B, inst_C, inst_TC, SUM_inst );

  parameter A_width = 5;
  parameter B_width = 5;
  parameter SUM_width = 11;

  input [A_width-1 : 0] inst_A;
  input [B_width-1 : 0] inst_B;
  input [SUM_width-1 : 0] inst_C;
  input inst_TC;
  output [SUM_width-1 : 0] SUM_inst;

  // Instance of DW02_prod_sum1
  DW02_prod_sum1 #(A_width, B_width, SUM_width)
    U1 ( .A(inst_A), .B(inst_B), .C(inst_C), .TC(inst_TC), .SUM(SUM_inst) );

endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
March 2019	DWBB_201903.0	■ Removed Table 1-4, “Obsolete Synthesis Implementations”
January 2019	DWBB_201806.5	■ Updated example in “HDL Usage Through Component Instantiation - VHDL” on page 3 ■ Added this Revision History table and the document links on this page

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