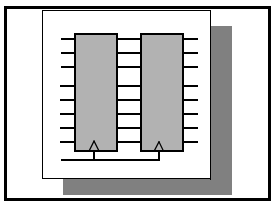
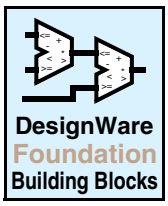




DW03_pipe_reg

Pipeline Register

Version, STAR, and myDesignWare Subscriptions: IP Directory

Features and Benefits

- Parameterized data width and depth

Revision History

Description

DW03_pipe_reg is a set of *width*-bit wide registers connected in series to form a pipeline shift register *depth* levels deep.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
A	*width* bits	Input	Input data bus
clk	1 bit	Input	Clock
B	*width* bits	Output	Output data bus

Table 1-2 Parameter Description

Parameter	Values	Description
depth	≥ 1	Depth of registers
width	≥ 1	Width of `A` and `B` buses

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
str	Synthesis model	DesignWare

Table 1-4 Simulation Models

Model	Function
DW03.DW03_PIPE_REG_CFG_SIM	Design unit name for VHDL simulation
dw/dw03/src/DW03_pipe_reg_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW03_pipe_reg.v	Verilog simulation model source code

This component is composed of a simple array of D flip-flops connected in series by their `D` and `Q` pins. Setup and hold constraints are relative to the rising edge of clock signal `clk` and are technology dependent.

Because this pipeline register has no reset pin, data output `B` is unknown for the first *depth* – 1 clock cycles after startup (the pipeline register's latency is *depth* – 1 clock cycles).

Suppressing Warning Messages During Verilog Simulation

The Verilog simulation model includes macros that allow you to suppress warning messages during simulation.

To suppress all warning messages for all DWBB components, define the DW_SUPPRESS_WARN macro in either of the following ways:

- Specify the Verilog preprocessing macro in Verilog code:

  ```
  `define DW_SUPPRESS_WARN
  ```

- Or, include a command line option to the simulator, such as:

  `+define+DW_SUPPRESS_WARN` (which is used for the Synopsys VCS simulator)

The warning messages for this model include the following:

- If values other than 1 or 0 are present on a clock port, the following message is displayed:

  ```
  WARNING: <instance_path>.<clock_name>_monitor:
      at time = <timestamp>, Detected unknown value, x, on <clock_name> input.
  ```

  To suppress only this warning message for all DWBB components, use the following macro:

  - Define the DW_DISABLE_CLK_MONITOR macro. You can define this macro in the following ways:
    - Specify the Verilog preprocessing macro in Verilog code:

      ```
      `define DW_DISABLE_CLK_MONITOR
      ```

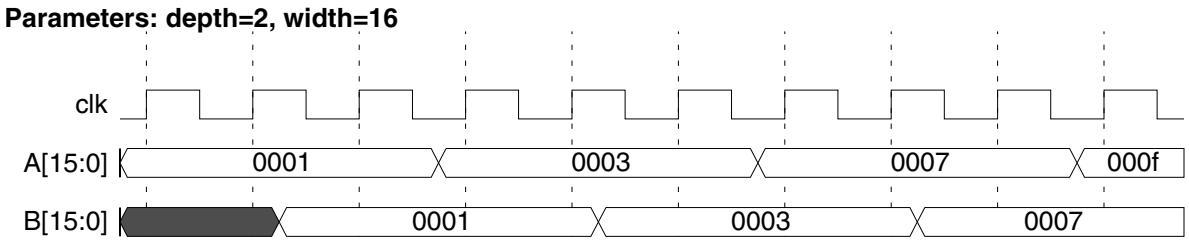
    - Or, include a command line option to the simulator, such as:

      `+define+DW_DISABLE_CLK_MONITOR` (which is used for the Synopsys VCS simulator)

  This message is also suppressed using the DW_SUPPRESS_WARN macro explained earlier.

Timing Diagram

Figure 1-1 Timing Waveforms for Pipeline Register



Related Topics

- Memory – Registers Overview
- DesignWare Building Block IP User Guide

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW03_pipe_reg_inst is
  generic ( inst_depth : INTEGER := 8;
            inst_width : INTEGER := 8 );
  port ( inst_A   : in std_logic_vector(inst_width-1 downto 0);
         inst_clk : in std_logic;
         B_inst   : out std_logic_vector(inst_width-1 downto 0) );
end DW03_pipe_reg_inst;

architecture inst of DW03_pipe_reg_inst is
begin

  -- Instance of DW03_pipe_reg
 U1 : DW03_pipe_reg
    generic map ( depth => inst_depth, width => inst_width )
    port map ( A => inst_A, clk => inst_clk, B => B_inst );
end inst;

-- pragma translate_off
configuration DW03_pipe_reg_inst_cfg_inst of DW03_pipe_reg_inst is
  for inst
  end for; -- inst
end DW03_pipe_reg_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW03_pipe_reg_inst( inst_A, inst_clk, B_inst );

  parameter depth = 8;
  parameter width = 8;

  input [width-1 : 0] inst_A;
  input inst_clk;
  output [width-1 : 0] B_inst;

  // Instance of DW03_pipe_reg
  DW03_pipe_reg #(depth, width)
    U1 ( .A(inst_A), .clk(inst_clk), .B(B_inst) );
endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
July 2020	DWBB_201912.5	■ Adjusted content and title of "Suppressing Warning Messages During Verilog Simulation" on page 2 and added the DW_SUPPRESS_WARN macro
October 2019	DWBB_201903.5	■ Added the "Disabling Clock Monitor Messages" section
January 2019	DWBB_201806.5	■ Updated example in "HDL Usage Through Component Instantiation - VHDL" on page 3 ■ Added this Revision History table and the document links on this page

Copyright Notice and Proprietary Information

Destination Control Statement

All technical data contained in this publication is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the reader's responsibility to determine the applicable regulations and to comply with them.

Disclaimer

SYNOPSYS, INC., AND ITS LICENSORS MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Trademarks

Synopsys and certain Synopsys product names are trademarks of Synopsys, as set forth at https://www.synopsys.com/company/legal/trademarks-brands.html.

All other product or company names may be trademarks of their respective owners.

Free and Open-Source Software Licensing Notices

If applicable, Free and Open-Source Software (FOSS) licensing notices are available in the product installation.

Third-Party Links

Any links to third-party websites included in this document are for your convenience only. Synopsys does not endorse and is not responsible for such websites and their practices, including privacy practices, availability, and content.

Synopsys, Inc.
www.synopsys.com