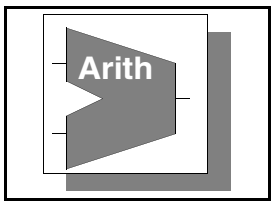
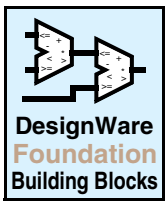




DW01_cmp6

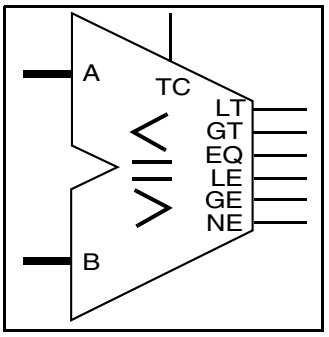
6-Function Comparator

Version, STAR, and myDesignWare Subscriptions: IP Directory

Features and Benefits

- Parameterized word length
- Unsigned and signed (two's-complement) data comparison

Revision History



Description

DW01_cmp6 is a two-input comparator. DW01_cmp6 compares two signed or unsigned numbers (A and B) and produces the following six output conditions:

1. Less-than (LT),
2. Greater-than (GT),
3. Equal (EQ),
4. Less-than-or-equal (LE),
5. Greater-than-or-equal (GE), and
6. Not equal (NE).

The input signal TC determines whether the two input numbers are compared as unsigned (TC = 0) or signed (TC = 1).

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
A	*width* bits	Input	Input data
B	*width* bits	Input	Input data
TC	1 bit	Input	Two's complement control ■ 0 = Unsigned ■ 1 = Signed
LT	1 bit	Output	Less-than output condition
GT	1 bit	Output	Greater-than output condition
EQ	1 bit	Output	Equal output condition
LE	1 bit	Output	Less-than-or-equal output condition
GE	1 bit	Output	Greater-than-or-equal output condition
NE	1 bit	Output	Not equal output condition

Table 1-2 Parameter Description

Parameter	Values	Description
width	≥ 1	Word length of `A` and `B`

Table 1-3 Synthesis Implementations[a]

Implementation Name	Function	License Feature Required
rpl	Ripple-carry synthesis model	None
pparch	Delay-optimized flexible parallel-prefix	DesignWare
apparch	Area-optimized flexible architecture that can be optimized for area, for speed, or for area, speed	DesignWare

a. During synthesis, Design Compiler selects the appropriate architecture for your constraints. However, you may force Design Compiler to use one of the architectures described in this table.

Table 1-4 Simulation Models

Model	Function
DW01.DW01_CMP6_CFG_SIM	Design unit name for VHDL simulation
dw/dw01/src/DW01_cmp6_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW01_cmp6.v	Verilog simulation model source code

Table 1-5 Functional Description

Condition	GT	LT	EQ	LE	GE	NE
A > B	1	0	0	0	1	1
A < B	0	1	0	1	0	1
A = B	0	0	1	1	1	0

Related Topics

- Math – Arithmetic Overview
- DesignWare Building Block IP User Guide

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW01_cmp6_inst is
  generic ( inst_width : NATURAL := 8 );
  port ( inst_A  : in std_logic_vector(inst_width-1 downto 0);
         inst_B  : in std_logic_vector(inst_width-1 downto 0);
         inst_TC : in std_logic;
         LT_inst : out std_logic;
         GT_inst : out std_logic;
         EQ_inst : out std_logic;
         LE_inst : out std_logic;
         GE_inst : out std_logic;
         NE_inst : out std_logic );
end DW01_cmp6_inst;

architecture inst of DW01_cmp6_inst is
begin

  -- Instance of DW01_cmp6
  U1 : DW01_cmp6
    generic map ( width => inst_width )
    port map ( A => inst_A, B => inst_B, TC => inst_TC, LT => LT_inst,
               GT => GT_inst, EQ => EQ_inst, LE => LE_inst,
               GE => GE_inst, NE => NE_inst );
end inst;

-- pragma translate_off
configuration DW01_cmp6_inst_cfg_inst of DW01_cmp6_inst is
  for inst
  end for; -- inst
end DW01_cmp6_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW01_cmp6_inst( inst_A, inst_B, inst_TC, LT_inst, GT_inst,
                       EQ_inst, LE_inst, GE_inst, NE_inst );

  parameter width = 8;

  input [width-1 : 0] inst_A;
  input [width-1 : 0] inst_B;
  input inst_TC;
  output LT_inst;
  output GT_inst;
  output EQ_inst;
  output LE_inst;
  output GE_inst;
  output NE_inst;

  // Instance of DW01_cmp6
  DW01_cmp6 #(width)
    U1 ( .A(inst_A), .B(inst_B), .TC(inst_TC), .LT(LT_inst), .GT(GT_inst),
         .EQ(EQ_inst), .LE(LE_inst), .GE(GE_inst), .NE(NE_inst) );

endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
March 2019	DWBB_201903.0	■ Removed Table 1-4, “Obsolete Synthesis Implementations”
January 2019	DWBB_201806.5	■ Updated example in “HDL Usage Through Component Instantiation - VHDL” on page 3 ■ Added this Revision History table and the document links on this page

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