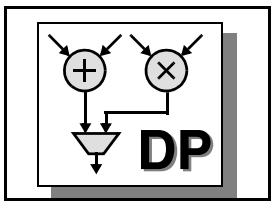

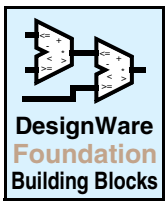

DWF_dp_mult_comb_ovfldet function

Combined Unsigned/Signed Multiply and Overflow Detection

Version, STAR, and myDesignWare Subscriptions: IP Directory

Description

The DWF_dp_mult_comb_ovfldet function performs combined (switchable) unsigned/signed multiplication of the two arguments `a` and `b`, truncates the upper bits of the result to the width specified by argument *p_width* and returns the truncated value and an overflow flag (`ovfl`) that indicates whether an overflow (or underflow) occurred. Argument `a` (`b`) is interpreted as signed if argument `a_tc` (`b_tc`) is 1, otherwise as unsigned. The result must be interpreted as signed if argument `a_tc` or `b_tc` (or both) is 1 (= signed multiplication), otherwise as unsigned (= unsigned multiplication). A dedicated overflow detection is used to improve QoR of the multiplier.

Table 1-1 Function Names

Function Name	Description
DWF_dp_mult_comb_ovfldet	VHDL combined multiply and overflow detection (std_logic_vector/unsigned/signed arguments)
DWF_dp_mult_comb_ovfldet	Verilog combined multiply and overflow detection
DWF_dp_mult_comb_ovfldet_tc	Verilog combined multiply and overflow detection (signed arguments)

Table 1-2 Argument Description

Name	Type	Direction	Width / Values	Description
a	Vector	Input	*a_width*	Input multiplier
a_tc	Bit	Input	1	Two's complement control for multiplier ■ 0 = Unsigned ■ 1 = Signed
b	Vector	Input	*b_width*	Input multiplicand
b_tc	Bit	Input	1	Two's complement control for multiplicand ■ 0 = Unsigned ■ 1 = Signed
p	Vector	Output	*p_width*	Output product
ovfl	Bit	Output	1	Output overflow flag

Table 1-3 Parameter Description (Verilog)

Parameter	Values	Description
a_width	≥ 2	Word length of input `a`

Table 1-3 Parameter Description (Verilog) (Continued)

Parameter	Values	Description
b_width	≥ 2	Word length of input `b`
p_width	≥ 2	Word length of output product

Verilog Include File: DW_dp_mult_ovfldet_function.inc

Functional Description

```
DWF_dp_mult_comb_ovfldet (a[a_width-1:0], a_tc, b[b_width-1:0], b_tc, z[p_width-1:0], ovfl)

p[a_width+b_width-1:0] (unsigned)  = a (unsigned) * b (unsigned)    if a_tc = 0 and b_tc = 0

p[a_width+b_width-1:0] (signed)    = a (signed)   * b (unsigned)    if a_tc = 1 and b_tc = 0
                                   = a (unsigned) * b (signed)      if a_tc = 0 and b_tc = 1
                                   = a (signed)   * b (signed)      if a_tc = 1 and b_tc = 1

z[p_width-1:0] = p[p_width-1:0]                                     if (a_tc = 0 and b_tc = 0)
               = { p[a_width+b_width-1], p[p_width-2:0] }  else

ovfl           = 1  if      (a_tc = 0 and b_tc = 0) and
                            (p[a_width+b_width-1:0] > 2p_width-1)
               = 1  else if (a_tc = 1 or b_tc = 1) and
                            (p[a_width+b_width-1:0] > 2p_width-1-1)
               = 1  else if (a_tc = 1 or b_tc = 1) and
                            (p[a_width+b_width-1:0] < -2p_width-1)
               = 0  else
```

NOTE: For signed multiply, the truncated output keeps the sign of the non-truncated result (corresponds to the 'resize' function in VHDL).

For more information about the DesignWare datapath functions, refer to the topic titled DesignWare Datapath Functions Overview.

Related Topics

- DesignWare Datapath Functions Overview
- DesignWare Building Block IP User Guide

VHDL Example

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use DWARE.DW_dp_functions.all;
-- DWARE.DW_dp_functions_arith package if IEEE.std_logic_arith is used

entity DWF_dp_mult_comb_ovfldet_test is
  port (a, b, c    : in  unsigned(7 downto 0);
        a_tc, b_tc : in  std_logic;
        z          : out unsigned(7 downto 0));
end DWF_dp_mult_comb_ovfldet_test;

architecture rtl of DWF_dp_mult_comb_ovfldet_test is
  signal p        : unsigned(7 downto 0);
  signal overflow : std_logic;
begin
  DWF_dp_mult_comb_ovfldet (a, a_tc, b, b_tc, p, overflow);
  z <= p + c when overflow = '0' else "11111111";
end rtl;
```

Verilog Example

```
module DWF_dp_mult_comb_ovfldet_test (a, a_tc, b, b_tc, c, z);

  input  [7:0] a, b, c;
  input        a_tc, b_tc;
  output [7:0] z;

  reg    [7:0] p;
  reg          overflow;

  // Passes the parameters to the function
  parameter a_width = 8;
  parameter b_width = 8;
  parameter p_width = 8;

  // add "$SYNOPSYS/dw/sim_ver" to the search path for simulation
  `include "DW_dp_mult_comb_ovfldet_function.inc"

  always @* begin
    DWF_dp_mult_comb_ovfldet (a, a_tc, b, b_tc, p, overflow);
  end
  assign z = (overflow == 1'b0) ? p + c : 8'b11111111;

endmodule
```

Copyright Notice and Proprietary Information

Destination Control Statement

All technical data contained in this publication is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the reader's responsibility to determine the applicable regulations and to comply with them.

Disclaimer

SYNOPSYS, INC., AND ITS LICENSORS MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Trademarks

Synopsys and certain Synopsys product names are trademarks of Synopsys, as set forth at https://www.synopsys.com/company/legal/trademarks-brands.html.

All other product or company names may be trademarks of their respective owners.

Free and Open-Source Software Licensing Notices

If applicable, Free and Open-Source Software (FOSS) licensing notices are available in the product installation.

Third-Party Links

Any links to third-party websites included in this document are for your convenience only. Synopsys does not endorse and is not responsible for such websites and their practices, including privacy practices, availability, and content.

Synopsys, Inc.
www.synopsys.com