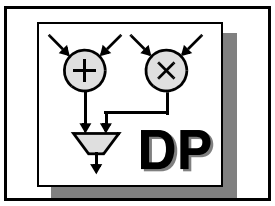

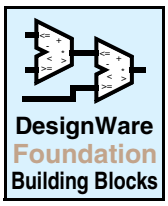

DWF_dp_rndsat functions

Arithmetic Rounding and Saturation

Version, STAR, and myDesignWare Subscriptions: IP Directory

Description

The DWF_dp_rndsat functions truncate the lower bits of argument `a` below the bit position specified by argument `lsb`, round according to the rounding mode specified by argument `mode`, truncate the upper bits above the bit position specified by argument `msb` and return a saturated value if an overflow (or underflow) occurs. Argument `a` and the return value are both either signed (two's complement) or unsigned.

Table 1-1 Function Names

Function Name	Description
DWF_dp_rndsat	VHDL unsigned rounding and saturation
DWF_dp_rndsat	VHDL signed (two's complement) rounding and saturation
DWF_dp_rndsat_uns	Verilog unsigned rounding and saturation
DWF_dp_rndsat_tc	Verilog signed (two's complement) rounding and saturation

Table 1-2 Argument Description

Argument Name	Type	Width / Values	Description
a	Vector	width	Input data
msb	Integer	> lsb, ≤ width−1	MSB index of return value (VHDL only, constant)
lsb	Integer	≥ 1, < msb	LSB index of return value (VHDL only, constant)
mode	Vector	4	Rounding mode Find more information on rounding and rounding modes in the DWF_dp_rnd Datasheet.
DWF_dp_rndsat	Vector	msb−lsb+1	Return value

Table 1-3 Parameter Description (Verilog)

Parameter	Values	Description
width	≥ 1	Word length of input `a`
msb	> lsb, ≤ width − 1	MSB index of return value
lsb	≥ 1, < msb	LSB index of return value

Verilog Include File: DW_dp_rndsat_function.inc

Functional Description

DWF_dp_rndsat is functionally equivalent to rounding followed by saturation (also requires special handling of rounding overflow).

```
z[msb-lsb:0] = DWF_dp_rndsat (a[width-1:0], msb, lsb, mode)
z[msb-lsb:0] = DWF_dp_sat (
                  DWF_dp_rnd (a[width-1:0], lsb, mode),
                    msb-lsb+1)
```

Unsigned / Signed Rounding

```
t[width-lsb-1:0] = a[width-1:lsb]+1  if a[lsb-1:0] > threshold(mode)
                 = a[width-1:lsb]    else
```

Find more information on rounding and rounding modes in the DWF_dp_rnd Datasheet.

Unsigned Saturation

$$z[msb-lsb:0] = \begin{cases} 2^{msb-lsb+1}-1 & \text{if } t[width-lsb-1:0] > 2^{msb-lsb+1}-1 \\ t[msb-lsb:0] & \text{else} \end{cases}$$

Signed Saturation

$$z[msb-lsb:0] = \begin{cases} 2^{msb-lsb}-1 & \text{if } t[width-lsb-1:0] > 2^{msb-lsb}-1 \\ -2^{msb-lsb} & \text{else if } t[width-lsb-1:0] < -2^{msb-lsb} \\ t[msb-lsb:0] & \text{else} \end{cases}$$

For more information about the DesignWare datapath functions, refer to the topic titled DesignWare Datapath Functions Overview.

Related Topics

- DesignWare Datapath Functions Overview
- DesignWare Building Block IP User Guide

VHDL Example

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use DWARE.DW_dp_functions.all;
-- DWARE.DW_dp_functions_arith package if IEEE.std_logic_arith is used

entity DWF_dp_rndsat_test is
  port (a, b, c : in  signed(7 downto 0);
        z       : out signed(7 downto 0));
end DWF_dp_rndsat_test;

architecture rtl of DWF_dp_rndsat_test is
begin
  z <= DWF_dp_rndsat (a * b, 11, 4, DW_dp_rnd_near_even) + c;
end rtl;
```

Verilog Example

```
module DWF_dp_rndsat_test (a, b, c, z);

  input  signed [7:0] a, b, c;
  output signed [7:0] z;

  // Passes the parameters to the function
  parameter width = 16;
  parameter msb   = 11;
  parameter lsb   = 4;

  // add "$SYNOPSYS/dw/sim_ver" to the search path for simulation
  `include "DW_dp_rndsat_function.inc"

  assign z = DWF_dp_rndsat_tc (a * b, DW_dp_rnd_near_even) + c;

endmodule
```

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