DW_cntr_gray

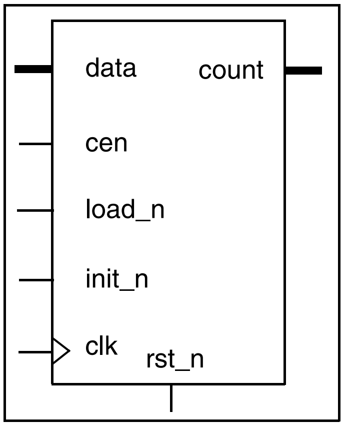
Gray Code Counter

Version, STAR, and myDesignWare Subscriptions: IP Directory

Features and Benefits

Revision History

- Gray encoded output
- Asynchronous and synchronous reset
- Count enable
- Includes a low-power implementation that has power benefits from minPower optimization (for details, see Table 1-3 on page 2)



Description

DW_cntr_gray is a Gray code counter. The counter is *width* bits wide and has 2^{width} states. The counter is clocked on the positive edge of the `clk` input. Because the count sequence is Gray code, only one counter bit changes value between successive states. DW_cntr_gray also has optional low power benefits.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
clk	1 bit	Input	Clock
rst_n	1 bit	Input	Reset, asynchronous, active low
init_n	1 bit	Input	Reset, synchronous, active low
load_n	1 bit	Input	Enable data load to counter, active low
data	*width* bits	Input	Counter load input
cen	1 bit	Input	Count enable, active high
count	*width* bits	Output	Gray coded counter output

Table 1-2 Parameter Description

Parameter	Values	Description
width	≥ 1	Word length of counter

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
str	Synthesis model	DesignWare
lpwr[a]	Low Power synthesis model	■ DesignWare (P-2019.03 and later) ■ DesignWare-LP (before P-2019.03)

a. Requires that you enable minPower; for details, see "Enabling minPower" on page 5.
When minPower is enabled, the lpwr implementation is always chosen during synthesis.

Table 1-4 Simulation Models

Model	Function
DW03.DW_chtr_gray_cfg_sim	Design unit name for VHDL simulation
dw/dw03/src/DW_cntr_gray_sim.vhd	VHDL simulation model source code
dw_sim_ver/DW_cntr_gray.v	Verilog simulation model source code

The active-low `rst_n` signal provides for an asynchronous reset of the counter to "000...0". The active-low `init_n` signal provides a synchronous reset of the counter to "000...0".

When the count enable pin `cen` is high, the counter is active. When `cen` is low, the counter is disabled and `count` remains unchanged.

The counter operates according to the following truth table:

rst_n	init_n	load_n	cen	Operation
0	X	X	X	Reset (asynchronous)
1	0	X	X	Reset (synchronous)
1	1	0	X	Load
1	1	1	0	Standby
1	1	1	1	Count

Suppressing Warning Messages During Verilog Simulation

The Verilog simulation model includes macros that allow you to suppress warning messages during simulation.

To suppress all warning messages for all DWBB components, define the DW_SUPPRESS_WARN macro in either of the following ways:

- Specify the Verilog preprocessing macro in Verilog code:

  ```
  `define DW_SUPPRESS_WARN
  ```

- Or, include a command line option to the simulator, such as:

  `+define+DW_SUPPRESS_WARN` (which is used for the Synopsys VCS simulator)

The warning messages for this model include the following:

- If values other than 1 or 0 are present on a clock port, the following message is displayed:

  ```
  WARNING: <instance_path>.<clock_name>_monitor:
      at time = <timestamp>, Detected unknown value, x, on <clock_name> input.
  ```

  To suppress only this warning message for all DWBB components, use the following macro:

  - Define the DW_DISABLE_CLK_MONITOR macro. You can define this macro in the following ways:
    - Specify the Verilog preprocessing macro in Verilog code:

      ```
      `define DW_DISABLE_CLK_MONITOR
      ```

    - Or, include a command line option to the simulator, such as:

      `+define+DW_DISABLE_CLK_MONITOR` (which is used for the Synopsys VCS simulator)

  This message is also suppressed using the DW_SUPPRESS_WARN macro explained earlier.

Timing Diagrams

Figure 1-1 Functional Operation with Asynchronous Reset

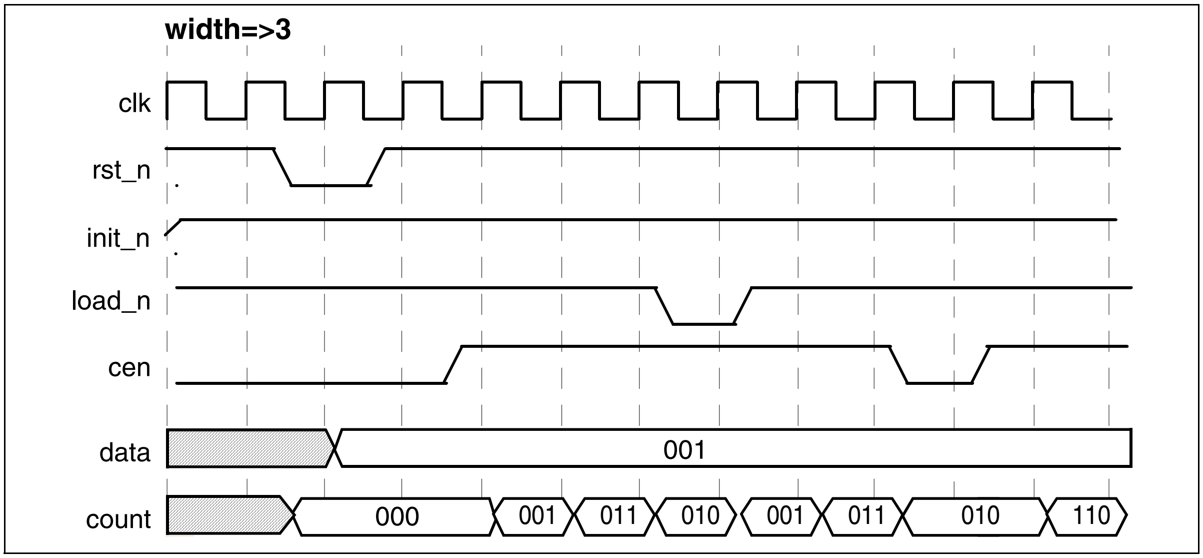
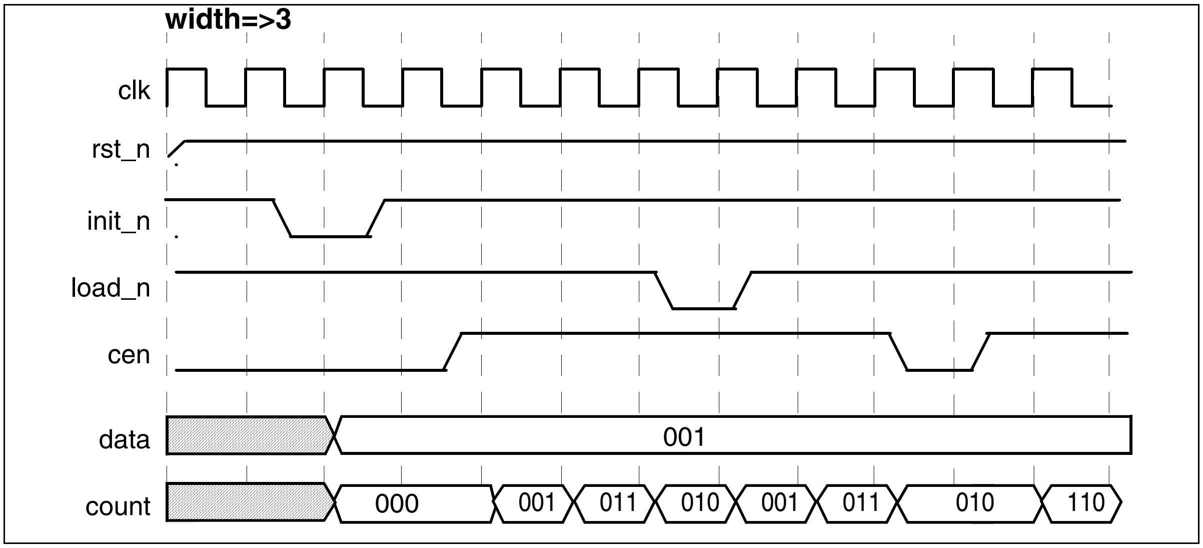


Figure 1-2 Functional Operation with Synchronous Reset



Enabling minPower

You can instantiate this component without enabling minPower, but to achieve power savings from the low-power implementation “lpwr” (see Table 1-3 on page 2), you must enable minPower optimization, as follows:

- Design Compiler
  - Version P-2019.03 and later:

    ```
    set power_enable_minpower true
    ```
  - Before version P-2019.03 (requires the DesignWare-LP license feature):

    ```
    set synthetic_library {dw_foundation.sldb dw_minpower.sldb}
    set link_library {* $target_library $synthetic_library}
    ```
- Fusion Compiler

  Optimization for minPower is enabled as part of the total_power metric setting. To enable the total_power metric, use the following:

  ```
  set_qor_strategy -stage synthesis -metric total_power
  ```

Related Topics

- Math – Arithmetic Overview
- DesignWare Building Blocks User Guide

HDL Usage Through Component Instantiation - VHDL

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DW_Foundation_comp_arith.all;

entity DW_cntr_gray_inst is
  generic (inst_width : positive := 8);
  port (inst_clk    : in  std_logic;
        inst_rst_n  : in  std_logic;
        inst_init_n : in  std_logic;
        inst_load_n : in  std_logic;
        inst_data   : in  std_logic_vector(inst_width-1 downto 0);
        inst_cen    : in  std_logic;
        count_inst  : out std_logic_vector(inst_width-1 downto 0));
end DW_cntr_gray_inst;

architecture inst of DW_cntr_gray_inst is
begin
  -- instance of DW_cntr_gray
  U1 : DW_cntr_gray
    generic map (width => inst_width)
    port map (clk    => inst_clk,
              rst_n  => inst_rst_n,
              init_n => inst_init_n,
              load_n => inst_load_n,
              data   => inst_data,
              cen    => inst_cen,
              count  => count_inst);
end inst;

-- pragma translate_off
configuration DW_cntr_gray_inst_cfg_inst of DW_cntr_gray_inst is
  for inst
  end for;
end DW_cntr_gray_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_cntr_gray_inst (inst_clk, inst_rst_n, inst_init_n, inst_load_n,
                          inst_data, inst_cen, count_inst);
  parameter inst_width = 8;

  input  inst_clk;
  input  inst_rst_n;
  input  inst_init_n;
  input  inst_load_n;
  input  [inst_width-1 : 0] inst_data;
  input  inst_cen;
  output [inst_width-1 : 0] count_inst;

  // Please add +incdir+$SYNOPSYS/dw/sim_ver+ to your verilog simulator
  // command line (for simulation).

  // instance of DW_cntr_gray
  DW_cntr_gray #(inst_width)
    U1 (.clk(inst_clk),
        .rst_n(inst_rst_n),
        .init_n(inst_init_n),
        .load_n(inst_load_n),
        .data(inst_data),
        .cen(inst_cen),
        .count(count_inst));
endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
July 2020	DWBB_201912.5	■ Adjusted content and title of "Suppressing Warning Messages During Verilog Simulation" on page 3 and added the DW_SUPPRESS_WARN macro
October 2019	DWBB_201903.5	■ Added the "Disabling Clock Monitor Messages" section
March 2019	DWBB_201903.0	■ Clarified implementations and license requirements in Table 1-3 on page 2 ■ Added "Enabling minPower" on page 5 ■ Added this Revision History table and the document links on this page

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