

## IC Compiler Laboratory Exercise

### **Design Preparation**

Copy lab file, please refer environment setup.

*Table I Lab*

DESIGN DATA	FILE OR DIRECTORY
Gate Level Netlist	~/icc_lab/design_data/CHIP_syn.v
IO Constraint File	~/icc_lab/design_data/io.tdf
Timing Constraint File	~/icc_lab/design_data/CHIP.sdc
Scandef File	~/icc_lab/design_data/CHIP.scandef
Technology File	~/icc_lab/tech/NangateOpenCellLibrary.tf
Layer Mapping File	~/icc_lab/tech/macro.map
Logical Library (Memory)	~/icc_lab/logical_lib/RF_2P_ADV64_16_tt_1.0_25.0_syn.db ~/icc_lab/logical_lib/RF_2P_ADV64_16_ff_1.1_-40.0_syn.db ~/icc_lab/logical_lib/RF_2P_ADV64_16_ss_0.9_125.0_syn.db
Logical Library (Core)	~/icc_lab/logical_lib/NangateOpenCellLibrary_typical.db ~/icc_lab/logical_lib/NangateOpenCellLibrary_fast.db ~/icc_lab/logical_lib/NangateOpenCellLibrary_slow.db
Logical Library (IO)	~/icc_lab/logical_lib/tpz_typ.db ~/icc_lab/logical_lib/tpz_fast.db ~/icc_lab/logical_lib/tpz_slow.db
Reference Library (Memory)	~/icc_lab/physical_lib/RF_2P_ADV64_16
Reference Library (Core)	~/icc_lab/physical_lib/NangateOpenCellLibrary
Reference Library (IO)	~/icc_lab/physical_lib/tpz
*TLU+ Data	~/icc_lab/tluplus/
Script Files	~/icc_lab/scripts/
Directory for Physical Verification	~/icc_lab/verify/

### **Environment Setup**

Setup software license, please refer environment setup.

## Lab1 Design Setup

1. Change directory to ~/icc\_lab/run and invoke IC Compiler

```
unix% cd ~/icc_lab/run
```

```
unix% icc_shell -gui
```

2. “File > Create Library”

New Library Name	CHIP
Technology File	.. /tech/NangateOpenCellLibrary.tf
Bus naming style	[ %d ]
Open library	enable

在Input reference libraries項目點選視窗 **Add**

在Select Directory視窗選擇 .. /physical\_lib/NangateOpenCellLibrary 按 **OK**  
.. /physical\_lib/RF\_2P\_ADV64\_16 按 **OK**  
.. /physical\_lib/tpz 按 **OK** 選擇完成。

按**OK**關閉視窗。

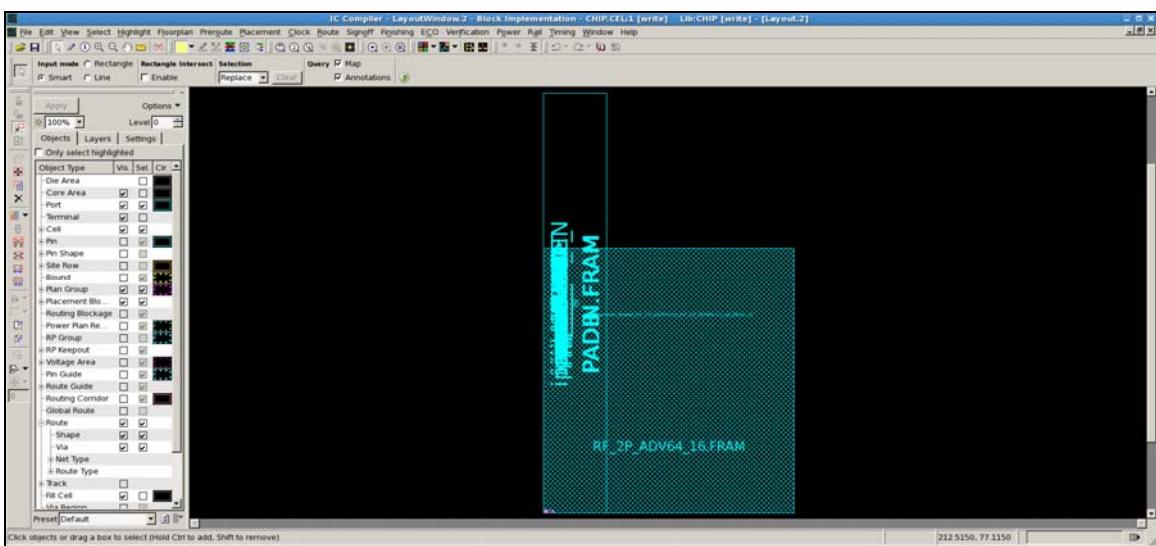
3. “File > Import Designs”

Import format	verilog
Import verilog files	.. /design_data/CHIP_syn.v
Top design name	CHIP

點選視窗 **Add**

在Select File視窗選擇 .. /design\_data/CHIP\_syn.v 按 **Open** 選擇。  
按**OK**。

可以看到ICC將整個design的CEL View建立出來。



4. “File > Set TLU+...”

Max TLU+ file	../tluplus/NangateOpenCellLibrary.tluplus
Layer name mapping file between technology library and ITF file	../tluplus/NangateOpenCellLibrary.map

5. “File > Import > Read SDC...”

Input file name	../design_data/CHIP.sdc
Version	Latest
Other	default value

6. “File > Save Design”

點選 **Save All**

“File > Save Design”

點選 **Show advanced options**

Save As	Enable
Save As Name	design_setup

按 **OK**。

7. “File > Close Design”

“File > Close Library”

※若 lab1 無法完成，可在 Message/Input Area 輸入 **source ..//scripts/01\_design\_setup.tcl** 以利後面的 lab 進行。

p.s. 執行前請先將 CHIP 資料夾刪除(在 Terminal 利用 **rm -rf \*** 指令)

## Lab2 Design Planning

1. Invoke IC Compiler (@path “~/icc\_lab/run ”)

```
unix% icc_shell -gui
```

2. “File > Open Library”

Library Name	CHIP
open library as read-only	disable
open reference library for writing	disable

按 **OK**。

“File > Open Design”

選擇 CHIP

按 **OK**。

3. 我們要加入 IO 及 Core 的 P/G pad, POC pad 及 Corner pad

在 Message/Input Area 輸入

```
source ../scripts/create_phy_cell.tcl
```

按 enter。



4. Read TDF file , 先切換至 LayoutWindows

“Floorplan > Read Pin/Pad Physical Constraints”

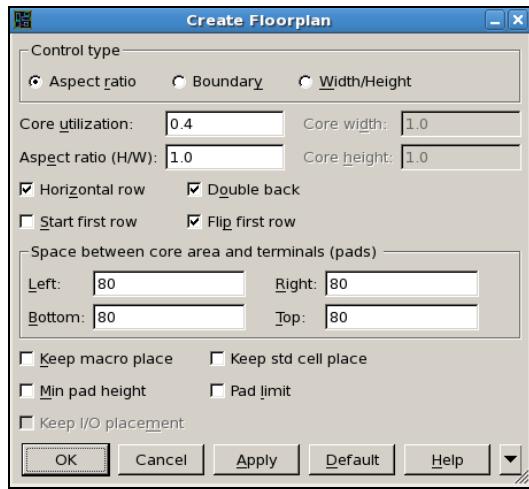
Input file name	../design_data/io.tdf
-----------------	-----------------------

按 **OK**。

“Floorplan > Create Floorplan... ”

Control type	Aspect ratio
Core utilization	0 . 4
Aspect ratio (H/W)	1
Horizontal row	Enable
Double back	Enable
Start first row	Disable
Flip first row	Enable
Core to left	80
Core to bottom	80
Core to right	80
Core to top	80

按 **OK**。

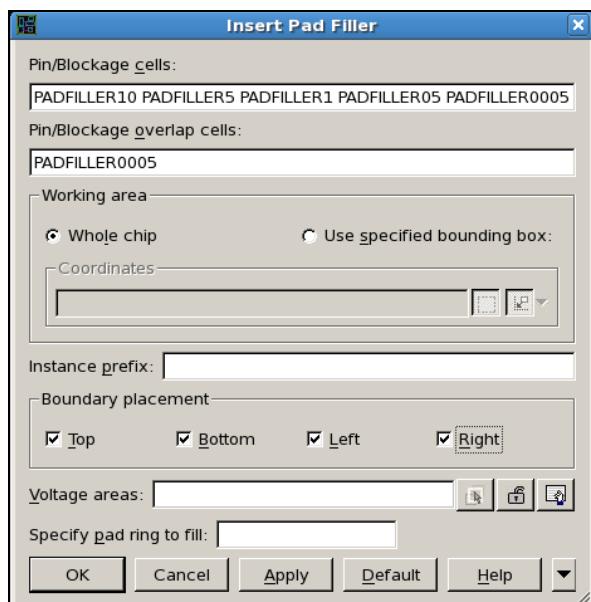


## 5. Insert pad filler

### “Finishing > Insert Pad Filler”

Pin/Blockage cells	PADFILLER20 PADFILLER10 \ PADFILLER5 PADFILLER1 \ PADFILLER05 PADFILLER0005 (由大至小排序)
Pin/Blockage overlap cells	PADFILLER0005
Boundary placement (Top)	Enable
Boundary placement (Bottom)	Enable
Boundary placement (Left)	Enable
Boundary placement (Right)	Enable
Other	Default value

按 **OK**。



## 6. “File > Save Design”

點上選 **Save All**

### “File > Save Design”

點選 Show advanced options

Save As	Enable
Save As Name	die_init

按 **OK**。

### 7. “Placement > Place Macro and Standard Cells” (如找不到選項請設定 File > Task > All Task)

Effort	Low
Congestion driven	disable
Timing driven	disable
Hierarchical gravity	enable

按 **OK**。

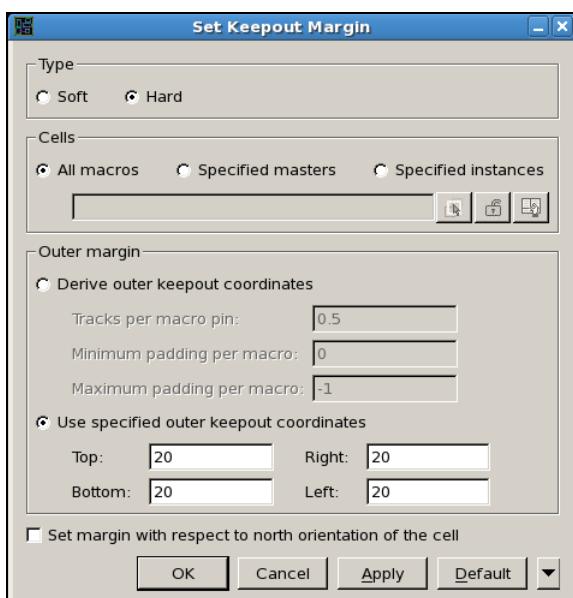


可以觀察到所有的 Macro 與 Standard Cell 皆放置完成

先設定所有的 macro 四周圍各 20um 的 keepout margin

### “Placement > Set Keepout Margin...”

Type	Hard
Cell	All macros
Use specified outer keepout coordinates	Top: 20 Right: 20 Bottom: 20 Left: 20

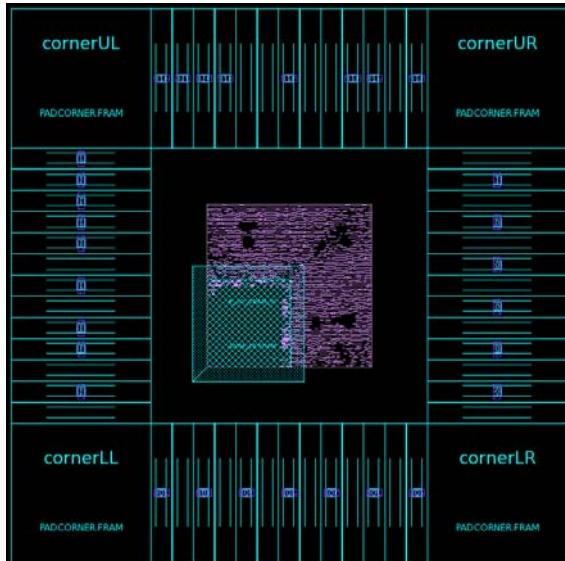


為了方便後續步驟，我們將 Macro 統一放置在固定位置  
在 Message/Input Area 輸入

```
move_objects -x 280 -y 280 [get_cells  
DCT_tposemem_Bisted_RF_2P_ADV64x16_RF_2P_ADV64x16_u0_SRAM_i0]
```

或者在 Message/Input Area 輸入

```
source ../scripts/mv_macro.tcl
```



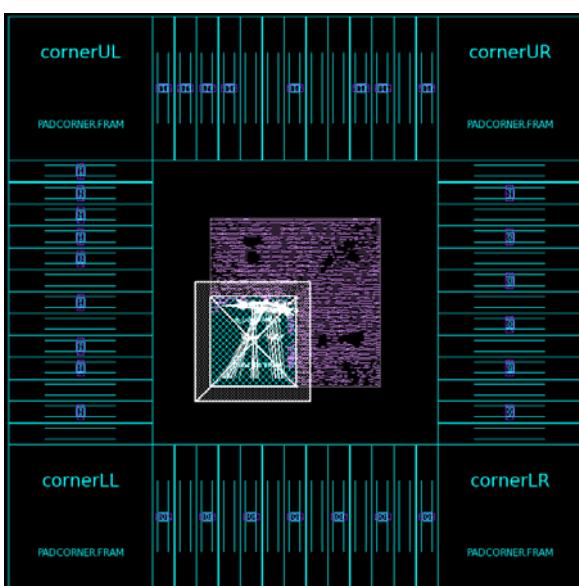
擺放完成後將所有 macro fix 住

在 Message/Input Area 輸入

```
set_dont_touch_placement [all_macro_cells]
```



接著點選 Macro，觀察 Macro 連線狀態，觀察完關閉。



8. 因為我們有變更 macro 的位置，所以執行 Incremental placement

“Placement > Place Macro and Standard Cells”

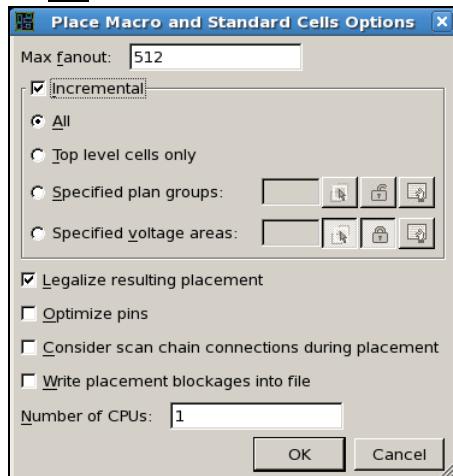
Effort	Low
Congestion driven	disable
Timing driven	disable
Hierarchical gravity	enable



選取 Advanced Options Tab

Incremental	enable
Other	Default Value

按 OK。



9. “File > Save Design”

點選 Save All

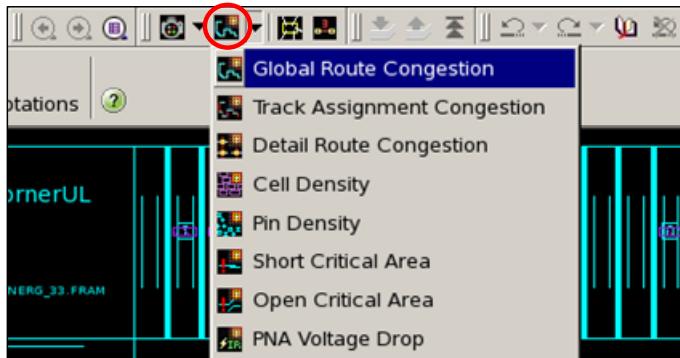
“File > Save Design”

點選 Show advanced options

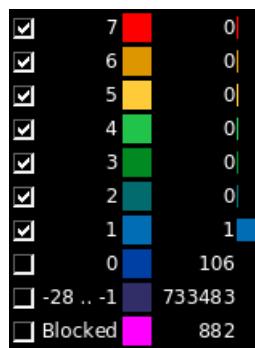
Save As	Enable
Save As Name	Before_PNS

按OK。

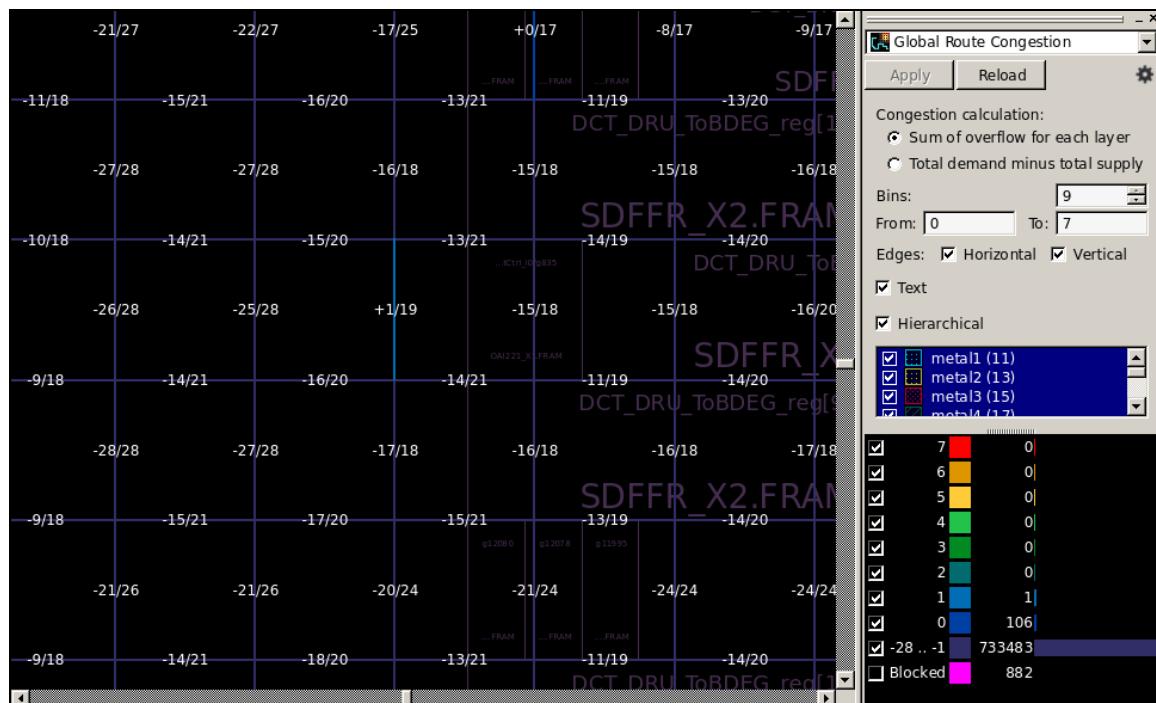
10. 分析 Congestion 狀態，點選 Global Route Congestion 視窗，再按下 reload，觀察完關閉



由於預設只有顯示發生 Congestion 的地方，如果觀察不到東西，可以檢查是否因為沒有 Congestion 發生。



如果要觀察沒有發生 Route Congestion 的地方，可將沒有發生 Congestion(意即 Congestion overflow  $\leq 0$ )的部分打勾，接著按 Apply，之後再 Zoom in 畫面即可觀察到，觀察完關閉。



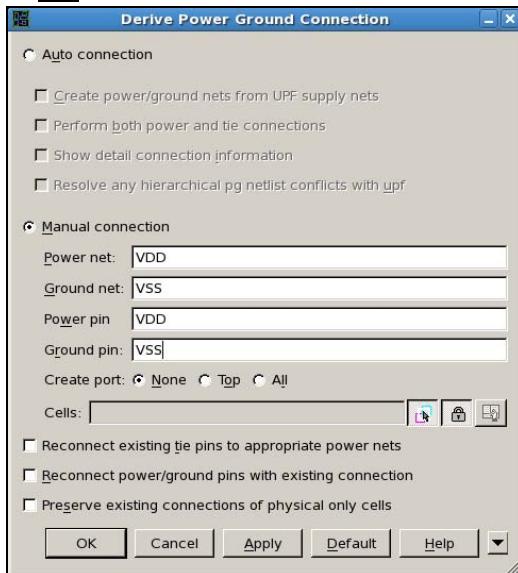
Note: 如果有 congestion 問題，如發生在 macro 附近，可以試著將 keepout margin 加大，或是將 macro 與 macro 之間的距離加大。如發生在 standard cell，可等至 placement 解決。

## 11. 連接 Cell 的 P/G nets

### “Preroute > Derive PG Connection”

Manual connection	selected
Power net	VDD
Ground net	VSS
Power pin	VDD
Ground pin	VSS
Other	Default value

按 **OK**。



可觀察 IC Compiler 的訊息視窗，顯示執行 Power / Ground Connection 後的訊息

```
icc_shell> derive_pg_connection -power_net {VDD} -ground_net {VSS} -power_pin {VDD} -ground_pin {VSS}
Information: connected 6611 power ports and 6611 ground ports
1
Log History Options
icc_shell>
```

## 12. 設定 PNS Constraints

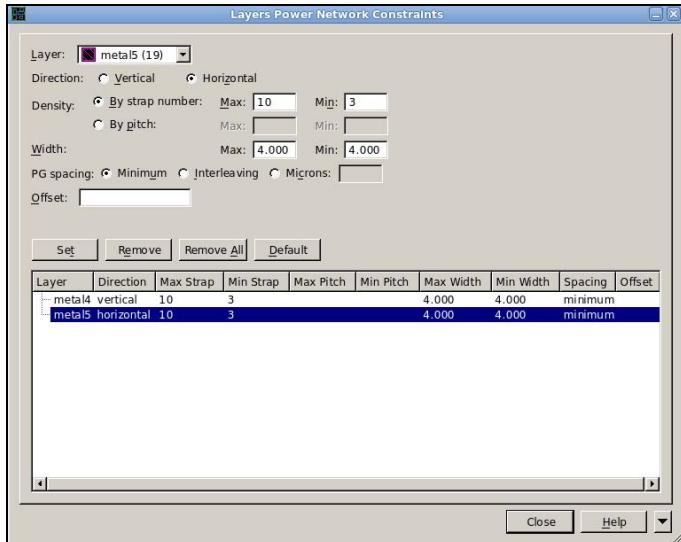
### “Preroute > Power Network Constraints > Strap Layers Constraints”

layer	metal14
Direction	Vertical
Density (By strap number)	Max:10 Min:3
Width	Max:4 Min:4

按 **Set** 再選

layer	metal15
Direction	Horizontal
Density (By strap number)	Max:10 Min:3
Width	Max:4 Min:4

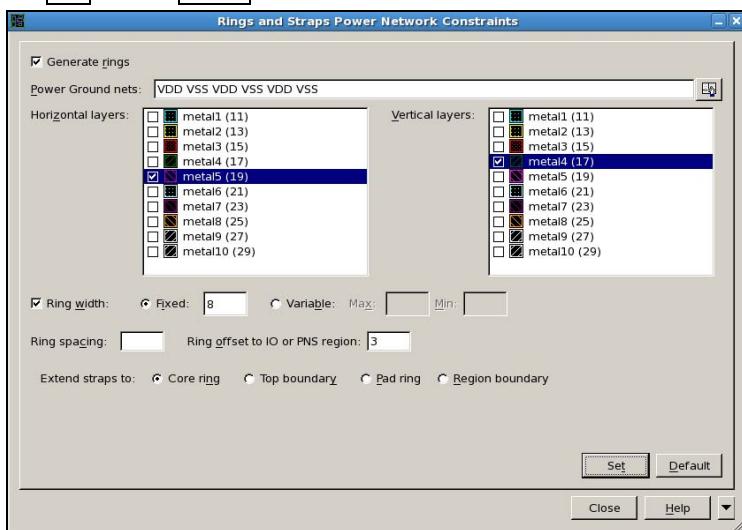
按 **Set** 後按 **Close** 離開。



#### “Preroute > Power Network Constraints > Ring Constraints”

Power Ground nets	VDD VSS VDD VSS VDD VSS (6 圈共 3 對)
Horizontal layers	metal5
Vertical layers	metal4
Ring width	enable
Variable	Fixed (8 um)
Ring offset to IO or PNS region	3
Variable	Core ring

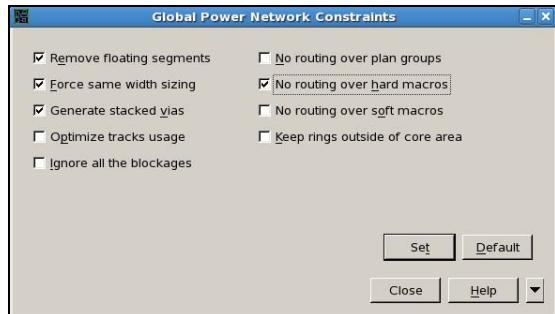
按 Set 後按 Close 離開。



#### “Preroute > Power Network Constraints > Global Constraints”

No routing over hard macros	enable
Other	Default value

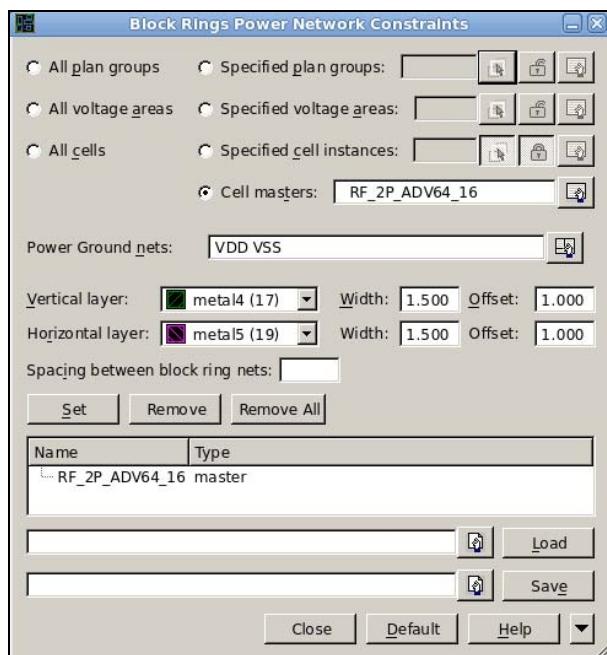
按 Set 後按 Close 離開。



#### “Preroute > Power Network Constraints > Block Ring Constraints”

Cell master	selected (RF_2P_ADV64_16)
Power Ground nets	VDD VSS
Vertical layer	metal4 (Width:1.5 Offset:1)
Horizontal layer	metal5 (Width:1.5 Offset:1)
Other	Default value

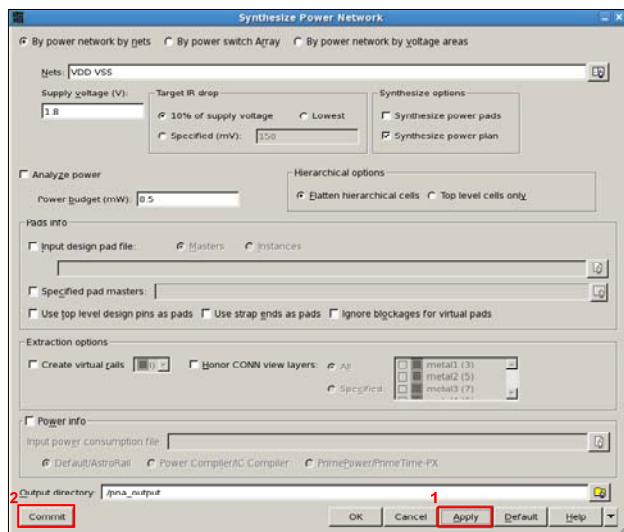
按 Set 後按 Close 離開。



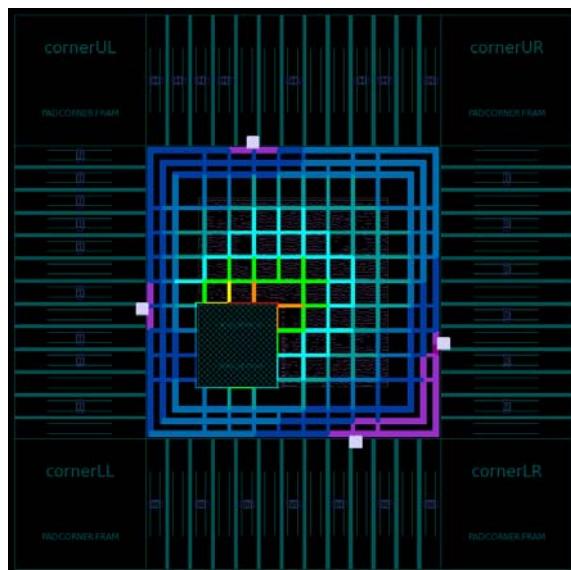
#### “Preroute > Synthesize Power Network”

By power network by nets	VDD VSS
Supply voltage	1.8
Target IR drop	10% of supply voltage
Power budget (mW)	8.5
Other	Default value

按 Apply 觀察 IR drop map 後，按 Commit 連接 P/G net，確認 Power Ring、Power Strap 和 Block Ring 建立起來後，按 Ok 離開(觀察 IR Drop 完畢，可以關閉 IR Drop Map)。

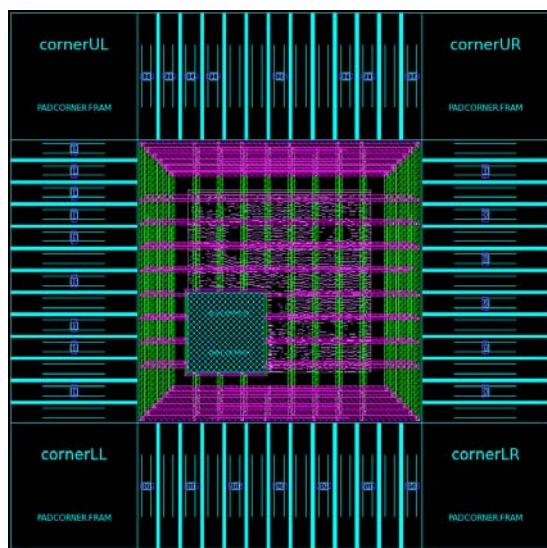


IR drop map:



Zoon In 畫面可觀察到 IR drop 的數值

Commit 後，可觀察到先前設定的 Power strap、Power ring 以及 Macro 的 Block ring 已經加上去。

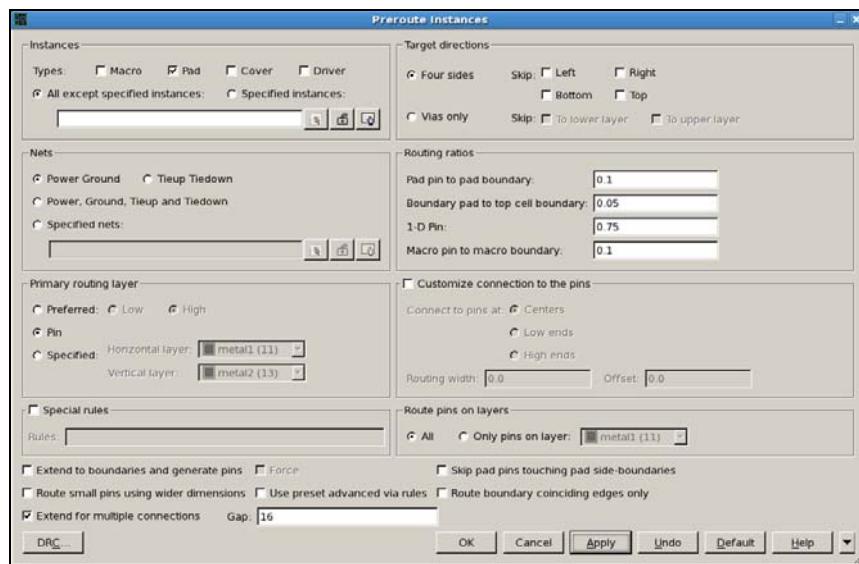


### 13. 建立 Power Pad 到 P/G Ring

#### “Preroute > Preroute Instances”

Instances	Pad(只勾選 Pad 其餘 disable)
Target directions	default value
Primary routing layer	Pin
Extend for multiple connections	Enable
Gap	16

按 **Apply** 之後再按 **Default**



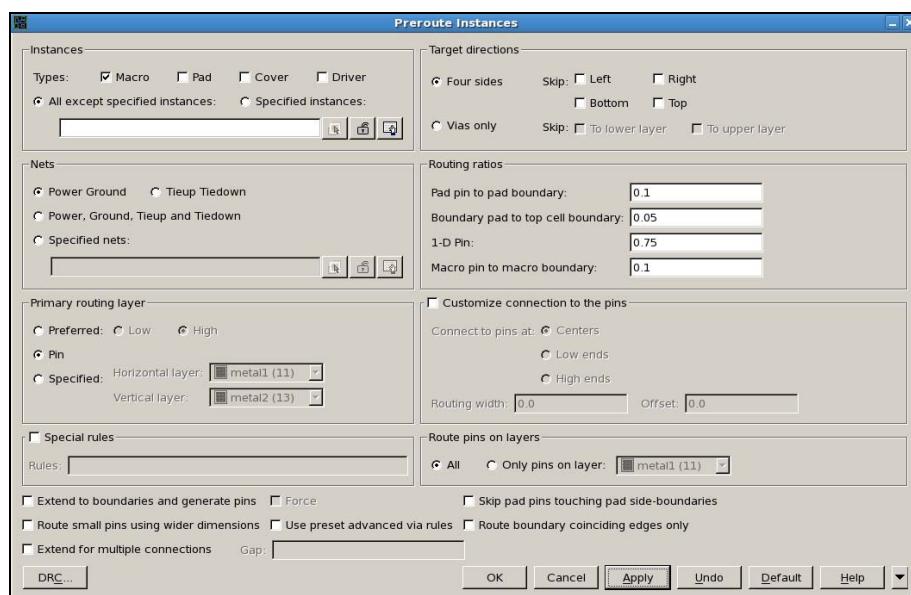
建立 Block Ring 到 P/G Ring 的連接

#### “Preroute > Preroute Instances”

Instances Types	Macro(只留 Macro 其餘 disable)
Primary routing layer	Pin

按 **Apply**

按 **OK**



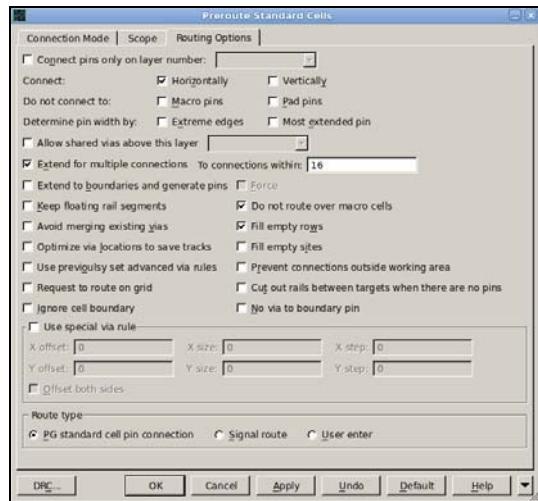
## 14. Preroute Standard Cell Rail

**“Preroute > Preroute Standard Cells...”**

選 Routing Option

Extend for multiple connections	Enable
To connections within	16
Keep floating rail segments	disable
Do not route over macro cells	enable
Fill empty rows	enable

按 **OK** 離開。



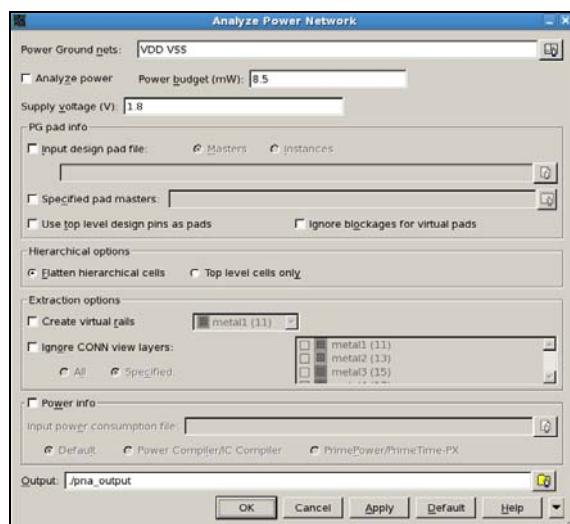
## 15. 分析做完整個 Power network synthesis 後的 IR drop 情形

**“Preroute > Analyze Power Network”**

Power Ground nets	VDD VSS
Supply voltage	1.8
Power budget (mW)	8.5
Other	Default value

按 **OK** 觀察 IR drop map，觀察 IR drop 最嚴重地點為何處？IR drop 最嚴重的量多少？

觀察後關閉 PNA Voltage Drop 選單



16. 設定 Strap 下不要擺放 Standard Cell

在 Message/Input Area 輸入

```
set_pnet_options -partial "metal4 metal5"  
create_fp_placement -incremental all
```

17. “File > Save Design”

點選 **Save All**

“File > Save Design”

點選 **Show advanced options**

Save As	Enable
Save As Name	design_planning

按 **OK**。

18. “File > Close Design”

“File > Close Library”

※若 lab2 無法完成，可在 Message/Input Area 輸入 **source .../scripts/02\_design\_planning.tcl** 以利後面的 lab 進行。

### Lab3 Placement

- Invoke IC Compiler (@path “~/icc\_lab/run ”)

```
unix% icc_shell -gui
```

- “File > Open Library”

Library Name	CHIP
open library as read-only	disable
open reference library for writing	disable

按 **OK**。

#### “File > Open Design”

選擇 CHIP

按 **OK**。

- “File > Import >Read SDC...”

Input file name	./design_data/CHIP.sdc
Version	Latest
Other	default value

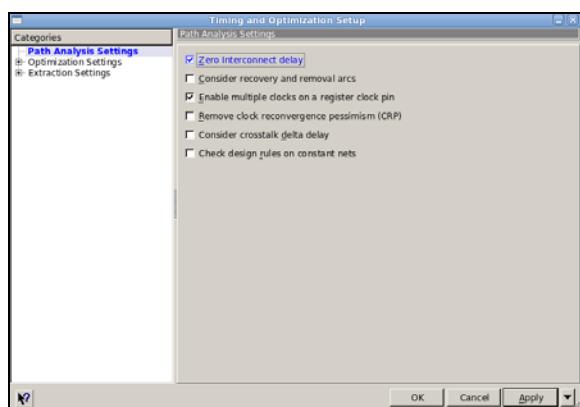
- 設定 zero interconnect delay 屬性為 true

#### “Timing > Timing and Optimization Setup... ”

Zero Interconnect delay	enable
Other	default value

按 **OK**。

如果出現需要 Update data model 請按 OK。



- Report timing

在 Message/Input Area 輸入  
report\_timing

- Check all constraint violations:

在 Message/Input Area 輸入  
report\_constraint -all

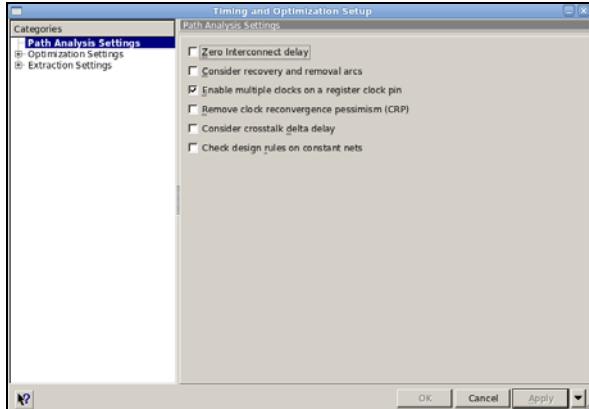
7. 設定 zero interconnect delay 屬性為 false

**“Timing > Timing and Optimization Setup...”**

Zero Interconnect delay	disable
Other	default value

按 **OK**。

如果出現需要 Update data model 請按 **OK**。

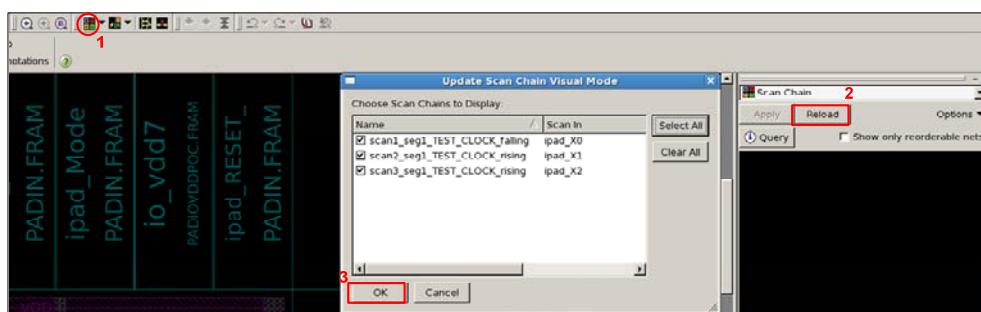


8. Load the SCANDEF file:

在 Message/Input Area 輸入

```
read_def ../design_data/CHIP.scandef
report_scan_chain
check_scan_chain
```

9. 點選 Scan Chain，在 Scan Chain 選單按 Reload 載入 Scan Chain 的資訊，接著在“Update Scan Chain Visual mode”視窗將 Choose Scan Chains to Display 將 Scan In 打勾，按 **OK**。在 LayoutWindows 觀察 scan chain，觀察完並關閉。

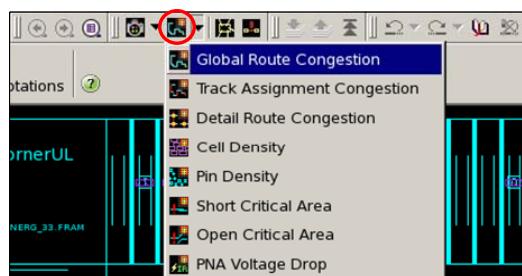


10. 產生 Power report:

在 Message/Input Area 輸入

```
report_power
```

11. 分析 Congestion 狀態，點選 Global Route Congestion 視窗，並按 reload，觀察完關閉



12. The following commands should be executed before performing place\_opt.

在 Message/Input Area 輸入

```
check_physical_design -stage pre_place_opt
```

13. Setup the tie cell option:

在 Message/Input Area 輸入

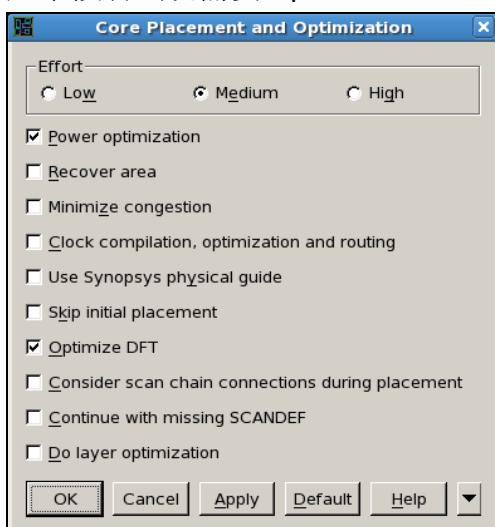
```
source ../scripts/add_tie.tcl
```

14. “Placement > Core Placement and Optimization...”

Effort	Medium
Power optimization	enable
Optimize DFT	enable

按 **OK**。

如果接著出現需要 Update data model 請按 **OK**。

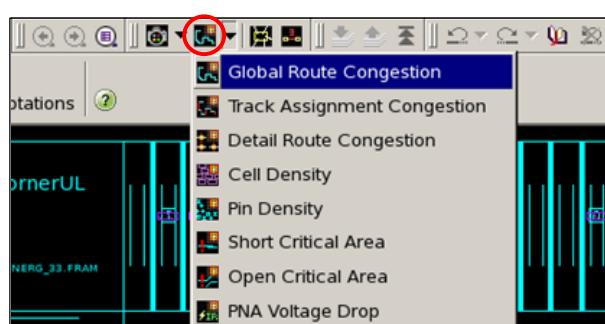


或者

在 Message/Input Area 輸入

```
place_opt -optimize_dft -power
```

15. 分析 Congestion 狀態，點選 Global Route Congestion 視窗，並按 reload，觀察完關閉



Note: 如果有 congestion 問題請下 refine\_placement

## 16. Report timing

在 Message/Input Area 輸入  
report\_timing

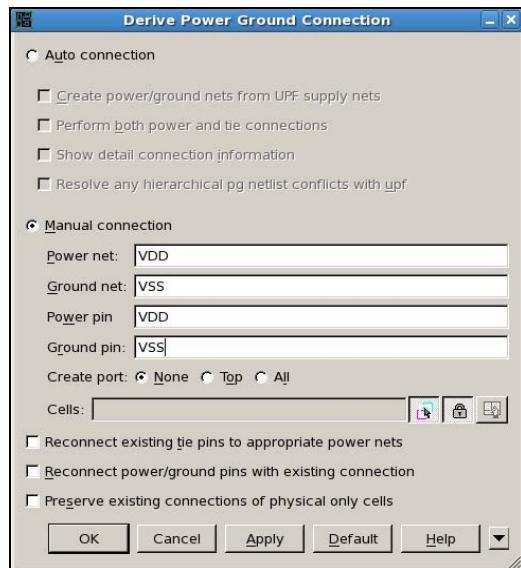
Note: 如果有 timing 問題請下 psynopt 或 place\_opt

## 17. 連接 Cell 的 P/G nets

### “Preroute > Derive PG Connection”

Manual connect	selected
Power net	VDD
Ground net	VSS
Power pin	VDD
Ground pin	VSS
Other	Default value

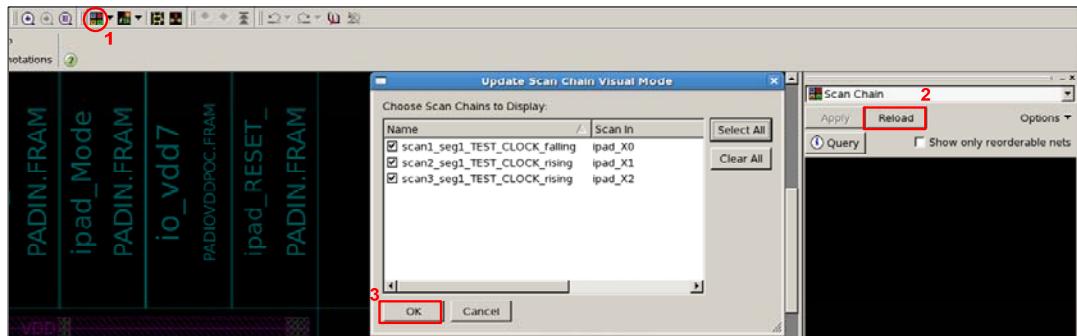
按 **OK**。



## 18. Report power:

在 Message/Input Area 輸入  
report\_power

## 19. 點選 Scan Chain，在 Scan Chain 選單按 Reload 載入 Scan Chain 的資訊，接著在“Update Scan Chain Visual mode 視窗將 Choose Scan Chains to Display 將 Scan In 打勾，按 **OK**。在 LayoutWindows 觀察 scan chain，觀察完並關閉。



20. “File > Save Design”

點選 **Save All**

“File > Save Design”

點選 **Show advanced options**

Save As	Enable
Save As Name	placement

按 **OK**。

21. “File > Close Design”

“File > Close Library”

※若 lab3 無法完成，可在 Message/Input Area 輸入 **source ..//scripts/03\_placement.tcl** 以利後面的 lab 進行。

## Lab4 CTS

- Invoke IC Compiler(@path “~/icc\_lab/run ”)

```
unix% icc_shell -gui
```

- “File > Open Library”

Library Name	CHIP
open library as read-only	disable
open reference library for writing	disable

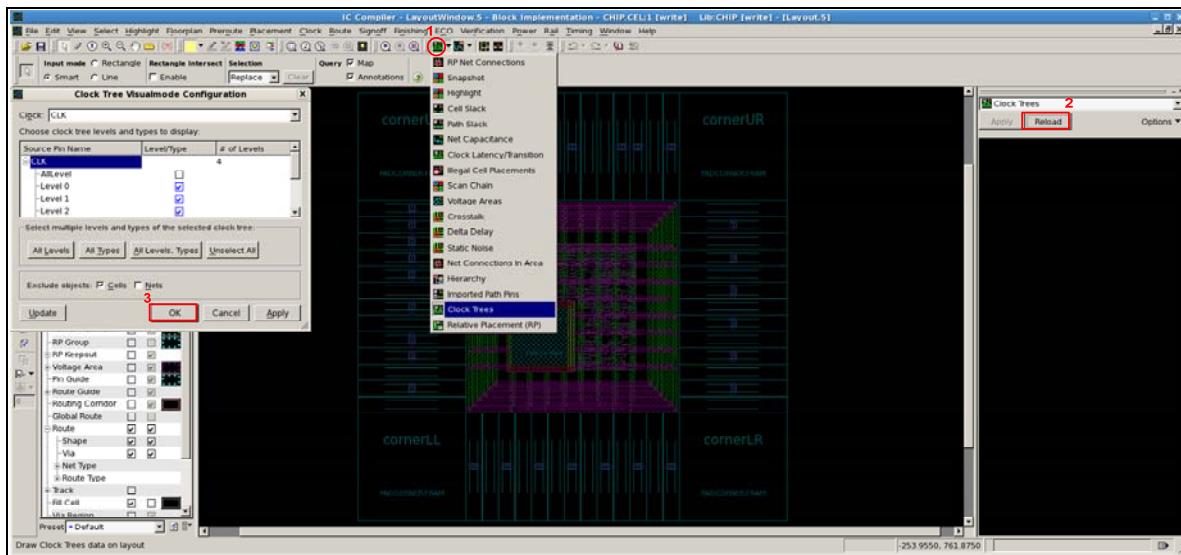
按 **OK**。

“File > Open Design”

選擇 CHIP

按 **OK**。

- 點選 Clock Trees，在 Clock Trees 選單按 **Reload** 載入 Clock Trees 的資訊，接著在“Clock Tree Visualmode Configuration”按 **OK**。在 LayoutWindows 觀察 Clock Tree，觀察完並關閉。



- The following commands should be executed before performing CTS.

在 Message/Input Area 輸入

```
check_physical_design -stage pre_clock_opt
```

檢查是否有 error?

```
report_constraint -all
```

觀察是否有 violation?

- Turn on hold time fixing.

在 Message/Input Area 輸入

```
set_fix_hold [all_clocks]
```

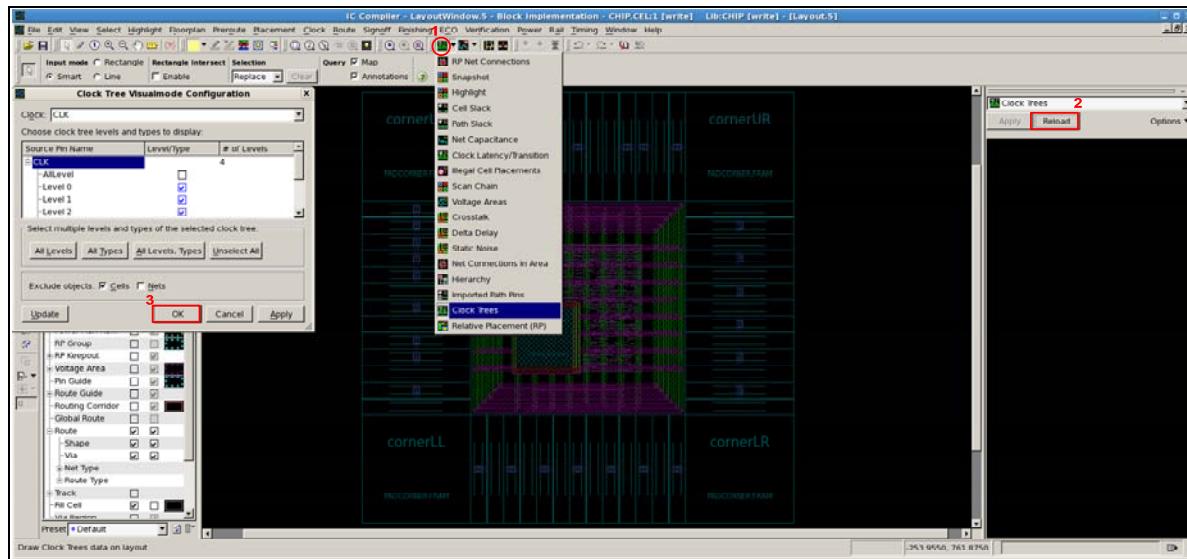
## 6. Report timing

在 Message/Input Area 輸入  
report\_timing

## 7. Perform CTS optimization:

在 Message/Input Area 輸入  
clock\_opt -fix\_hold\_all\_clocks -no\_clock\_route

## 8. 點選 Clock Trees，在 Clock Trees 選單按 Reload 載入 Clock Trees 的資訊，接著在"Clock Tree Visualmode Configuration"按 OK。在 LayoutWindows 觀察 Clock Tree，觀察完並關閉。



## 9. Report timing

在 Message/Input Area 輸入  
report\_timing

## 10. Review the global skew after CTS.

report\_clock\_tree -summary

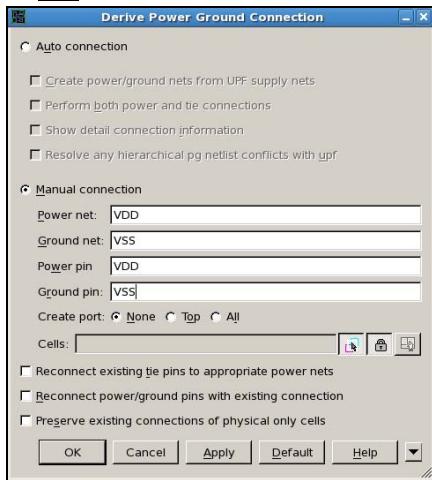
	Skew	Longestpath
CLK		

## 11. 連接 Cell 的 P/G nets

“Preroute > Derive PG Connection”

Manual connect	selected
Power net	VDD
Ground net	VSS
Power pin	VDD
Ground pin	VSS
Other	Default value

按 **OK**。



12. “File > Save Design”

點選 **Save All**

“File > Save Design”

點選 **Show advanced options**

Save As	Enable
Save As Name	cts

按 **OK**。

13. “File > Close Design”

“File > Close Library”

※若 lab4 無法完成，可在 Message/Input Area 輸入 **source ..//scripts/04\_cts.tcl** 以利後面的 lab 進行。

## Lab5 Route

1. Invoke IC Compiler(@path “~/icc\_lab/run ”)

```
unix% icc_shell -gui
```

2. “File > Open Library”

Library Name	CHIP
open library as read-only	disable
open reference library for writing	disable

按 **OK**。

“File > Open Design”

選擇 CHIP

按 **OK**。

3. Analyze the design for timing (setup and hold)

在 Message/Input Area 輸入

report\_timing

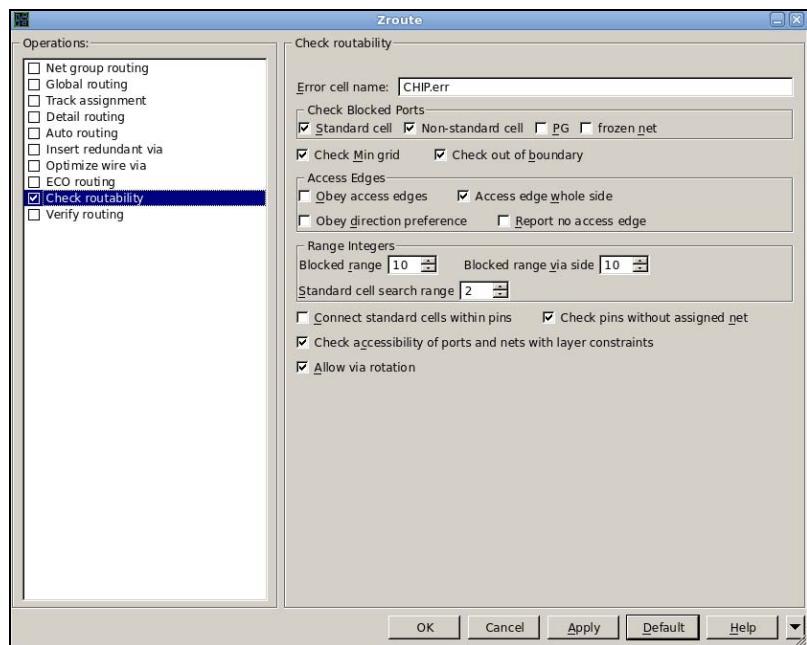
觀察 Timing 有無 violation?

4. Check the routeability of the design

“Route > Check Routability...”

按 **OK**。

觀察是否有 error?



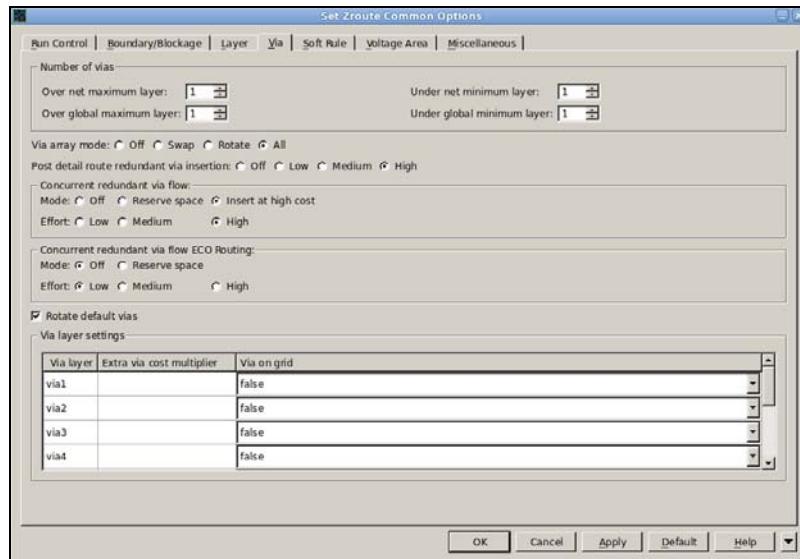
5. 設定在 routing 時的選項，並設定在 routing 時就加入 redundant via

**“Route > Routing Setup > Set common Route Option**

選 Via Tab

Post detail route redundant via insertion	High
Concurrent redundant via flow	Mode: Insert at High Cost
Concurrent redundant via flow	Effort: High

按 **OK**。

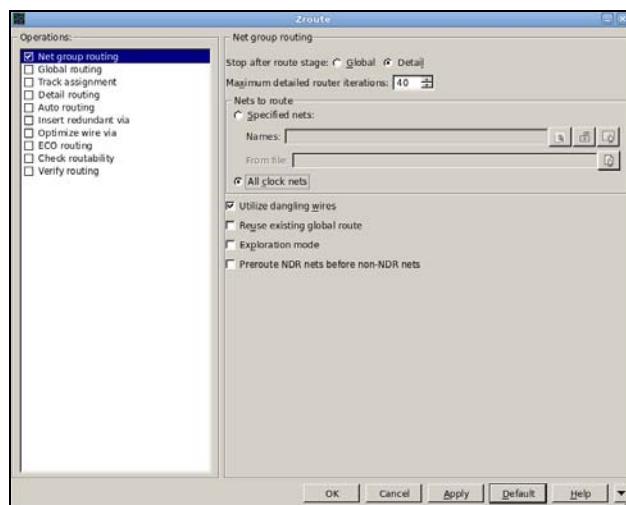


6. Perform clock net routing

**“Route > Net Group Route...”**

Net to route	All clock nets
other	default value

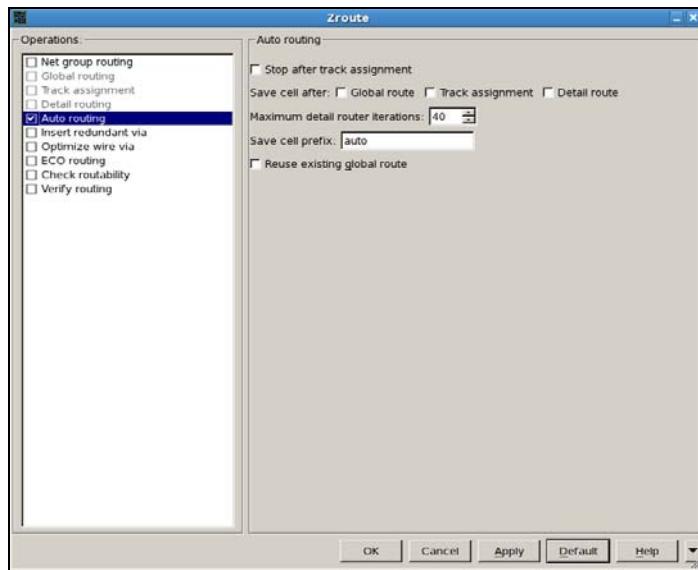
按 **OK**。



7. Perform auto routing

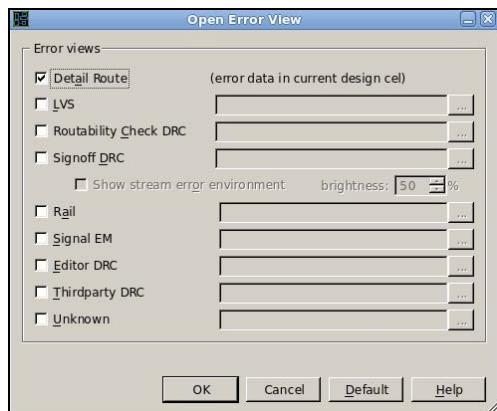
**“Route > Auto Route...”**

按 **OK**。



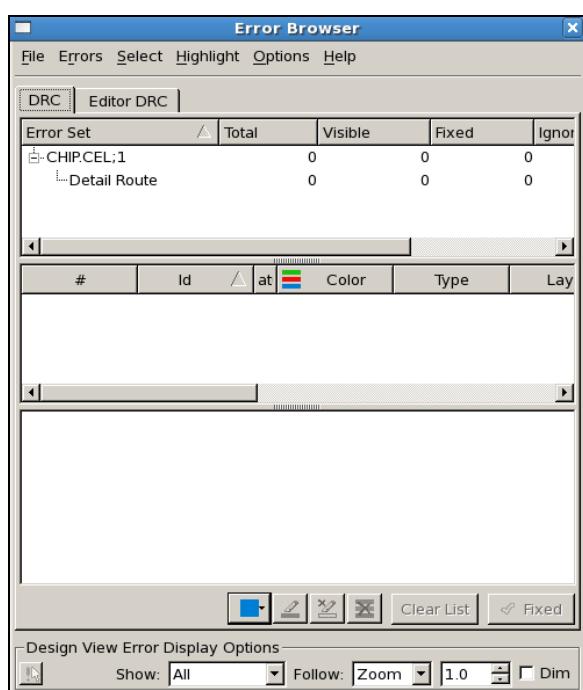
## 8. DRC violation error checking and fixing

**“Verification > Error Browser...”**



按 **OK**。

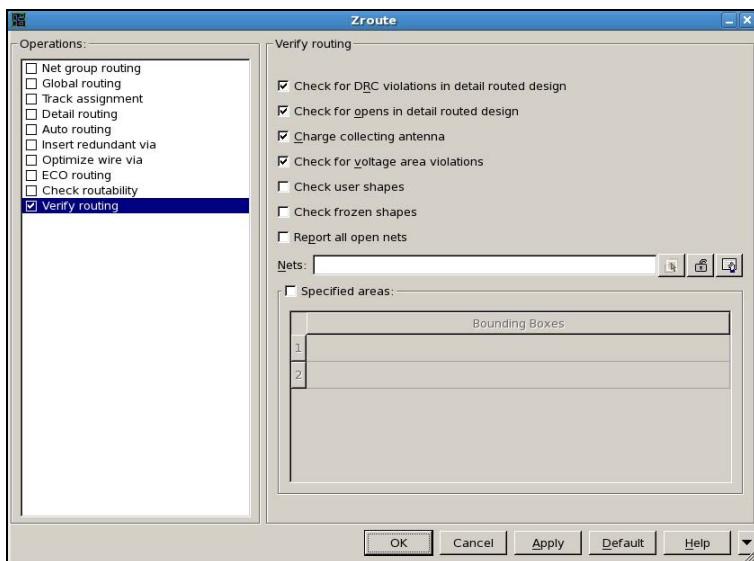
點取有 DRC error 的地方，會在 layout 中標示出來。



9. Recalculate the number of DRC violations as seen by the router

“Route > Verify Route...”

按 **OK**。



執行後如果還有 DRC Violation，訊息如下

Verify Summary:

Total number of nets = 10162, of which 0 are not extracted

**Total number of open nets = 0**, of which 0 are frozen

Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets

0 ports without pins of 0 cells connected to 0 nets

0 ports of 0 cover cells connected to 0 non-pg nets

**Total number of DRCs = 0**

Total number of antenna violations = no antenna rules defined

Total number of voltage-area violations = no voltage-areas defined

Total number of tie to rail violations = not checked

Total number of tie to rail directly violations = not checked

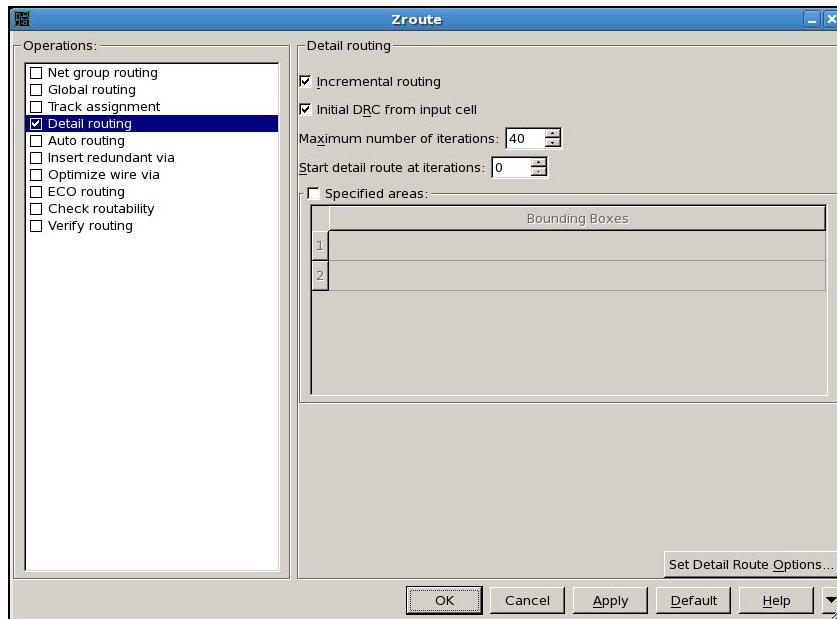
如有 **Open net** 或 **DRC violation** 則須執行 **Step 10**，如沒有 **DRC violation**，則可跳至 **Step 11**

10. Run a search & repair operation

“Route > Detail Route”

Incremental routing	enable
Initial DRC from input cell	enable

按 **OK**。

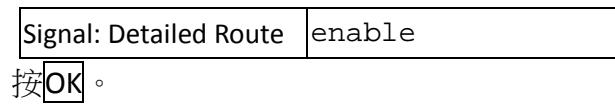


**注意!!** 執行 Detail Route 來修正 DRC violation 時，當 Initial DRC from input cell 選項為 enable 時，請務必確認有先做過 verify route

如有 DRC violation，可使用 Detail Route 並下 Incremental routing 與 Initial DRC from input cell 選項來修正

如果反覆執行 Step 9 與 Step 10，仍無法解決 Open net 或 DRC violation，可直接下 route\_opt 指令。如果還是無法解決的話，可以先使用下面步驟將繞線先刪除，繞線刪除完後再直接用 route\_opt 指令整個重新繞線

#### “Route > Delete Route...”



#### 11. Analyze the design for timing and fixing

在 Message/Input Area 輸入  
report\_timing

如有 Timing Violation 則請使用下列方式來修正

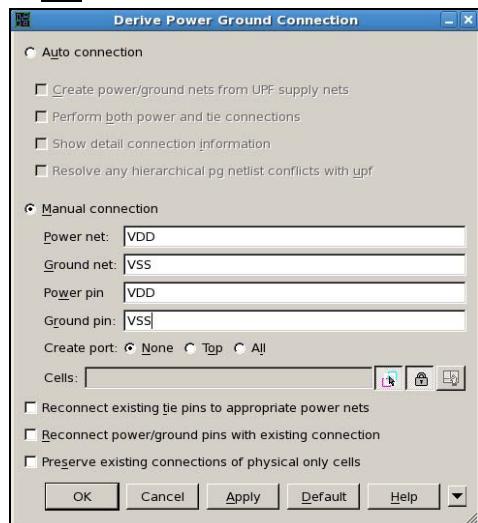
“Route > Core Routing and Optimization...” 按 **OK**。(即指 route\_opt 或 route\_opt -incremental)

## 12. 連接 Cell 的 P/G nets

“Preroute > Derive PG Connection”

Manual connect	selected
Power net	VDD
Ground net	VSS
Power pin	VDD
Ground pin	VSS
Other	Default value

按 **OK**。



## 13. “File > Save Design”

點選 **Save All**

“File > Save Design”

點選 **Show advanced options**

Save As	Enable
Save As Name	route

按 **OK**。

## 14. “File > Close Design”

“File > Close Library”

※若 lab5 無法完成，可在 Message/Input Area 輸入 **source ..//scripts/05\_route.tcl** 以利後面的 lab 進行。

## Lab6 DFM

- Invoke IC Compiler(@path “~/icc\_lab/run ”)

```
unix% icc_shell -gui
```

- “File > Open Library”

Library Name	CHIP
open library as read-only	disable
open reference library for writing	disable

按 **OK**。

“File > Open Design”

選擇 CHIP

按 **OK**。

- Insert standard cell filler

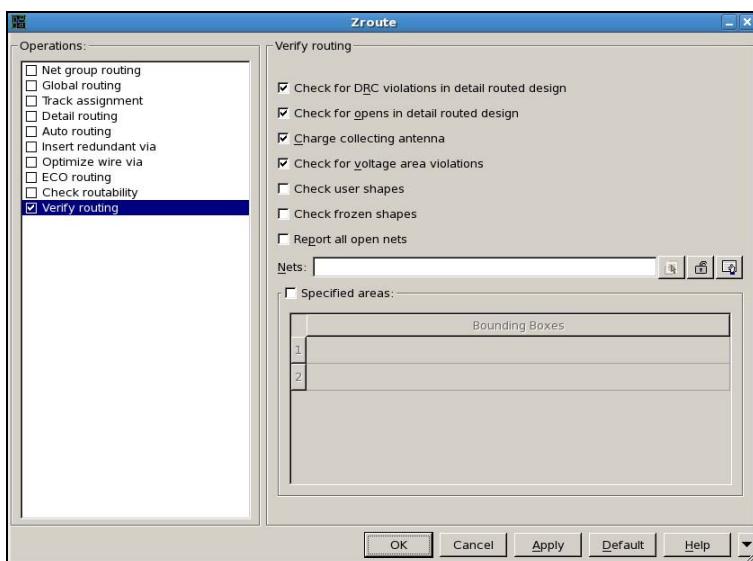
在 Message/Input Area 輸入

```
source ../scripts/addCoreFiller.cmd
```

- Verify insert standard cell filler 後的 DRC violation

“Route > Verify Route...”

按 **OK**。

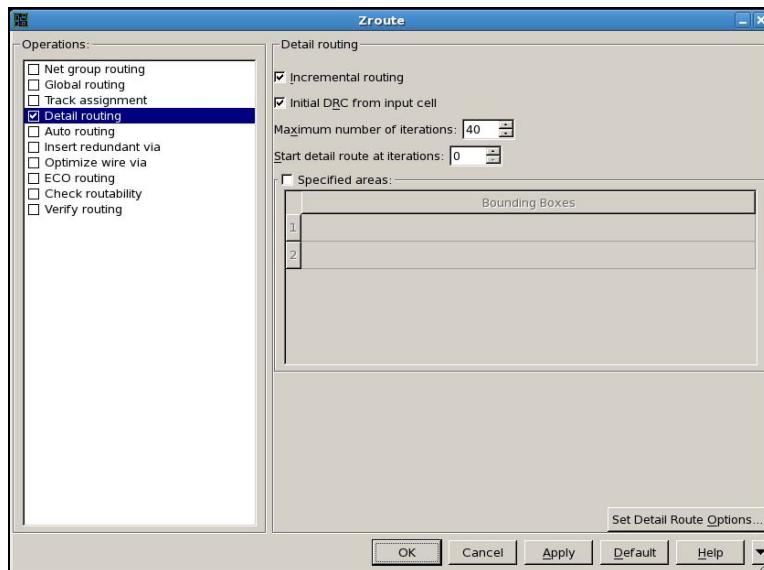


- 如果有 Open net 或 DRC violation 則執行 DRC Violation fixing

“Route > Detail Route”

Incremental routing	enable
Initial DRC from input cell	enable

按 **OK**。



**注意!!** 執行 Detail Route 來修正 DRC violation 時，當 Initial DRC from input cell 選項為 enable 時，請務必確認有先做過 verify route

#### 6. Analyze the design for timing and fixing

在 Message/Input Area 輸入  
report\_timing

但如果有 timing violation 時，則請使用下列方式來修正

**“Route > Core routing and Optimization...”** 按 **OK**。(即指 route\_opt or route\_opt -incremental)

#### 7. 如有 Antenna Violation 則需插入 antenna diode，沒有即可跳過此步驟 先設定插入 antenna diode 的設定

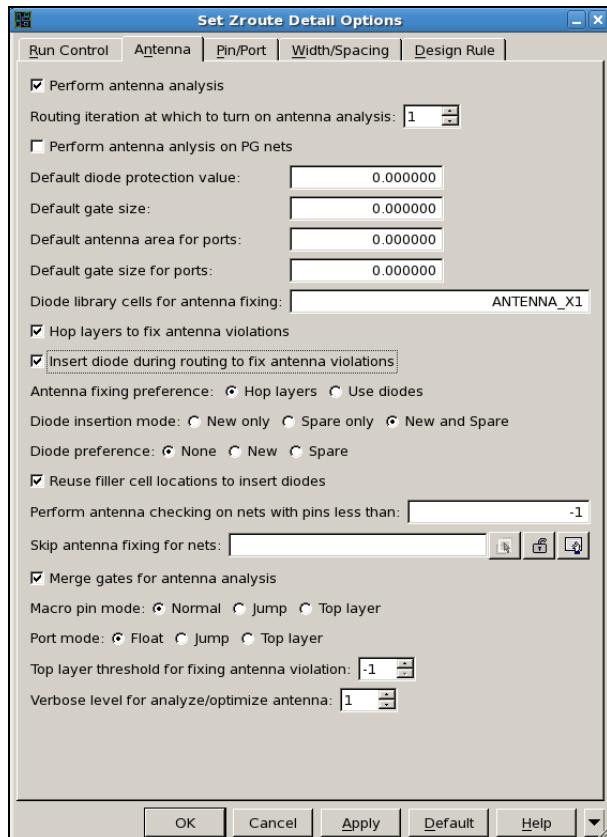
**“Route > Routing Setup > Set Detail Route Options...”**

選擇 Antenna Tab

Diode library cells for antenna fixing	ANTENNA_X1
Insert diode during routing to fix antenna violations	enable
Other	Default value

按 **OK** 離開。

由於虛擬製程並沒有提供 Antenna Rule，所以在執行 Verify route 時，不會檢查 Antenna violation，請跳過這個步驟，直接執行 Step 8。



再執行 Antenna Violation Fixing

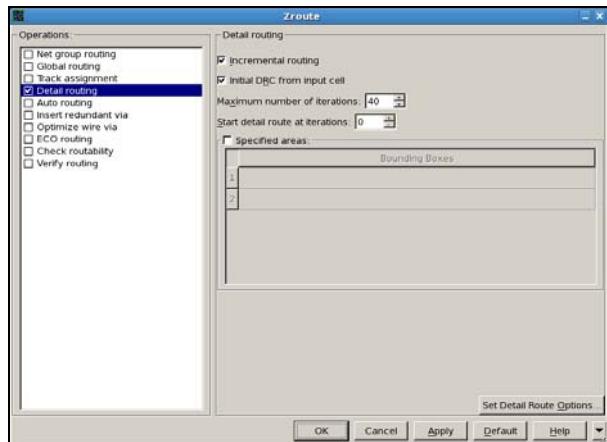
“Route > Verify Route...”

按 **OK**。

“Route > Detail Route”

Incremental routing	enable
Initial DRC from input cell	enable

按 **OK**。

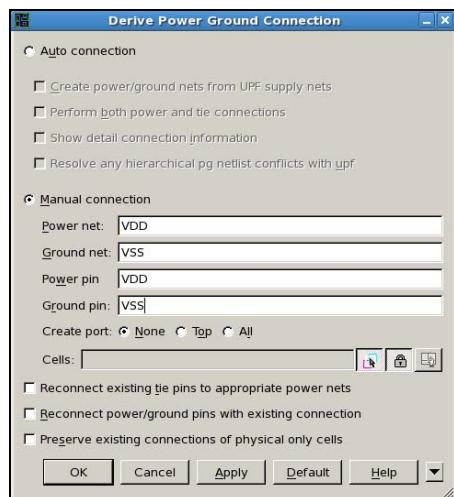


## 8. Reconnect PG net

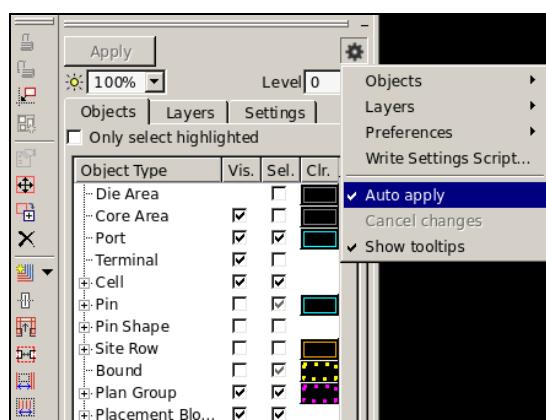
### “ Preroute > Derive PG Connection ”

Manual connect	selected
Power net	VDD
Ground net	VSS
Power pin	VDD
Ground pin	VSS
Other	Default value

按 **OK** 。



## 9. 將 View Settings Options 裡的 Auto apply 打勾

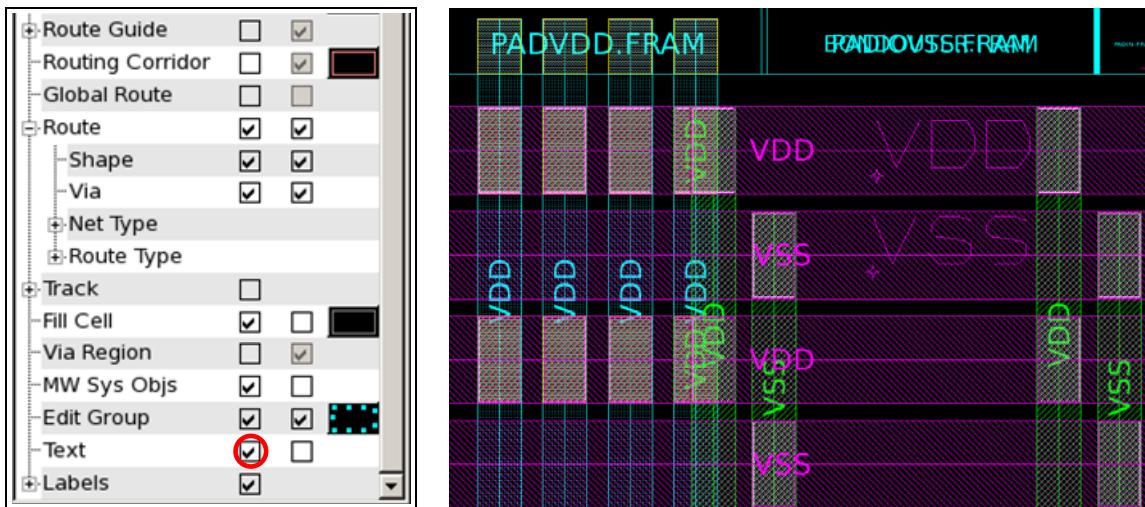


## 10. Add IO text

在 Message/Input Area 輸入

```
source ../scripts/add_io_text.tcl  
add_io_text metal7 5 portName
```

將 Core Power 打上 text，必須打在 design 的 Ring 上，VDD、VSS 各打 1 個就好。



**Edit >Create > Text...** or **Shift+t** Auto select 請先 disable

Text	VDD
Height	5
Layer	metal5

選定要打上的位置按一下滑鼠左鍵。



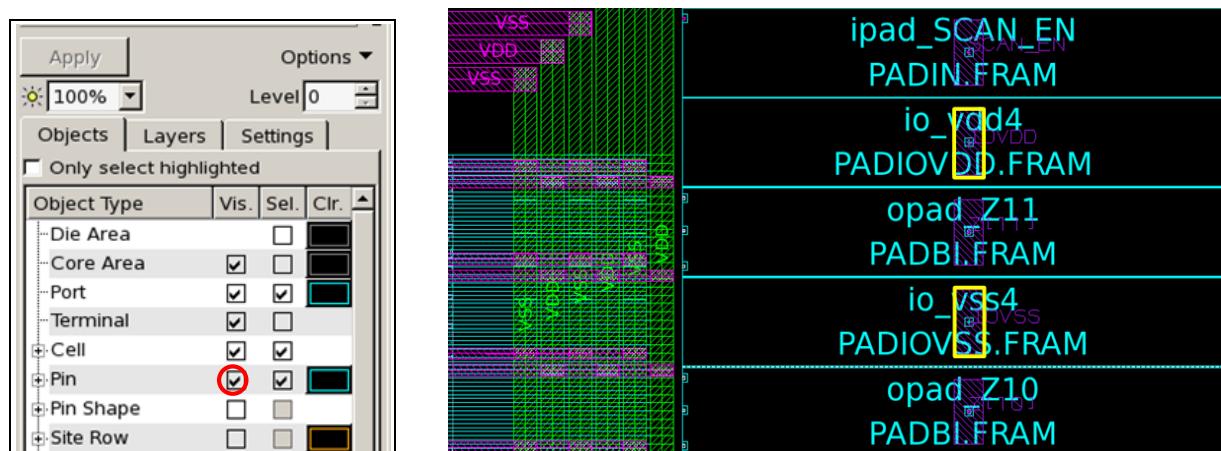
**Edit >Create > Text...** or **Shift+t** Auto select 請先 disable

Text	VSS
Height	5
Layer	metal5

選定要打上的位置按一下滑鼠左鍵。



將 IO Power 打上 text，必須打在 IO Power Pad 的 true pin 上，IOVDD、IOVSS 各打 1 個就好。



“Edit >Create > Text...” or **Shift+t** Auto select 請先 disable

Text	IOVDD
Height	5
Layer	metal7

選定要打上的位置按一下滑鼠左鍵。



“Edit >Create > Text...” or **Shift+t** Auto select 請先 disable

Text	IOVSS
Height	5
Layer	metal7

選定要打上的位置按一下滑鼠左鍵。



## 11. Add bonding pad

在 Message/Input Area 輸入

```
source ../scripts/createNplace_bondpads.tcl
createNplace_bondpads -inline_pad_ref_name BONDINNER \
                      -stagger true \
                      -stagger_pad_ref_name BONDOUTER
```

可以把 View Settings 裡，將 Level 由原本 0 改為 1，即可觀察到 Bonding pad 加上去。

## 12. “File > Save Design”

點選 **Save All**

### “File > Save Design”

點選 **Show advanced options**

Save As	Enable
Save As Name	dfm

按 **OK**。

## 13. Stream Out GDS II

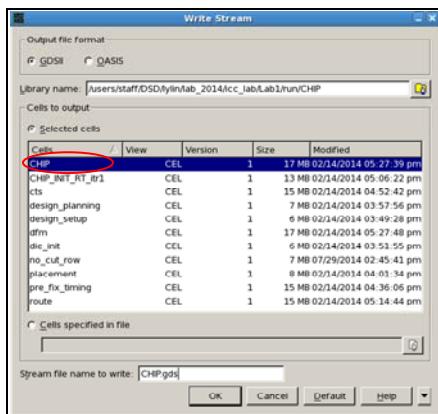
在 Message/Input Area 輸入

```
set_write_stream_options -map_layer ../tech/macro.map \
                         -child_depth 20 -flatten_via
```

### “File > Export > Write Stream...”

Output file format	GDSII
Cells to output	Selected cells "CHIP"
Stream file name to write	CHIP.gds

按 **OK**。



開啟另一個 Terminal 將 GDS 檔 copy 至 verify 資料夾內

```
[lylin@cic-dsd run]$ cp ./CHIP.gds ../verify/drc
[lylin@cic-dsd run]$ cp ./CHIP.gds ../verify/lvs
```

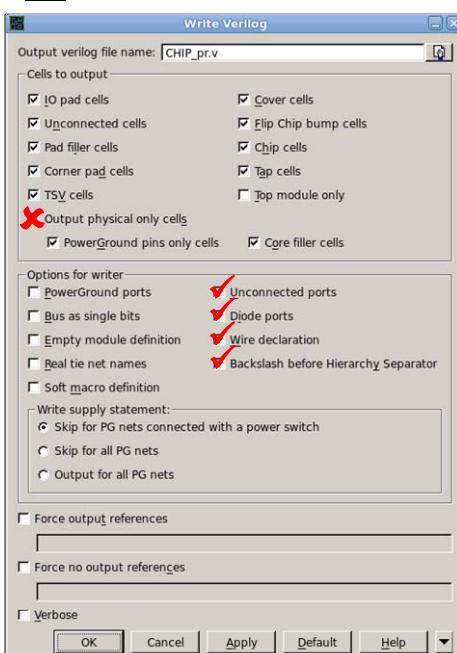
#### 14. Verilog Out for post-layout simulation & LVS

**“File > Export > Write Verilog...”**

先按 **Default**

Output verilog file name	CHIP_pr.v
Output physical only cells	disable
Unconnected ports	enable
Diode ports	enable
Wire declaration	enable
Backslash before Hierarchy Separator	enable

按 **OK**



使用 Terminal 將 verilog 檔 copy 至資料夾內

```
[lylin@cic-dsd run]$ cp ./CHIP_pr.v ../verify/lvs
```

15. 輸出 SDF 檔

在 Message/Input Area 輸入

```
write_sdf -version 2.0 -context verilog -load_delay net CHIP_pr.sdf
```

16. **File > Save Design**

點選 **Save All**

※ 建議待後面 Lab 7 執行完 Calibre DRC 及 LVS 驗證無誤後，再使用下列步驟關掉 IC Compiler

17. “**File > Close Design**”

“**File > Close Library**”

“**File > Exit**”

## Lab7 Calibre DRC & LVS

1. 使用 Terminal 將目錄切換至 ~/icc\_lab/verify/drc

```
unix% cd ~/icc_lab/verify/drc
```

2. 修改 calibreDRC.rul 檔(已編輯完畢)

```
LAYOUT PATH "./CHIP.gds"  
LAYOUT PRIMARY "CHIP"
```

3. 執行 Calibre DRC

```
unix% calibre -drc -hier calibreDRC.rul
```

Note: 注意開啟新的 Terminal，需重新 Setup software license，不然會出現 calibre: command not found.的錯誤訊息。

觀察 DRC.summary 檔看看是否有 drc error，應該會看到幾個 DRC error，所有的 density 相關 violation 都可以忽略，可以不予理會這個 DRC error

```
--- CALIBRE:::DRC-H EXECUTIVE MODULE COMPLETED. CPU TIME = 16 REAL TIME = 17  
--- TOTAL RULECHECKS EXECUTED = 167  
--- TOTAL RESULTS GENERATED = 0 (0)  
--- DRC RESULTS DATABASE FILE = DRC.results (ASCII)  
  
--- CALIBRE:::DRC-H COMPLETED - Fri Dec 25 13:46:36 2015  
--- TOTAL CPU TIME = 17 REAL TIME = 18  
--- PROCESSOR COUNT = 1  
--- SUMMARY REPORT FILE = DRC.summary
```

TOTAL RESULTS GENERATED 表示檢查到的 DRC violation 數量

若有 error，利用 Calibre RVE 可找到 drc 錯誤的數量、原因、坐標等資訊，再回到 IC Compiler 去做修正。

```
unix% calibre -rve DRC.results
```

4. 在 ICC 讀入 Calibre DRC 的結果

在 ICC Layout window 下

“Verification > Read Third-party DRC Error File...

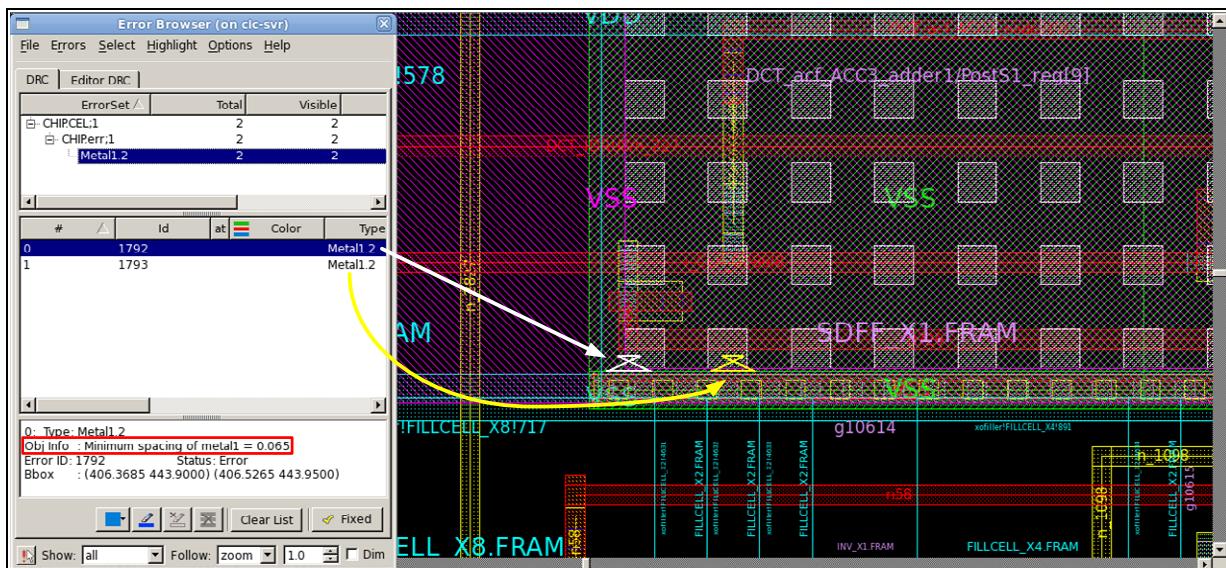
Error file	.../verify/drc/DRC.results
Other	default value

觀察有 Violation 的地方在哪，以及有哪些是 ICC 沒看到而 Calibre DRC 有看到的 violation

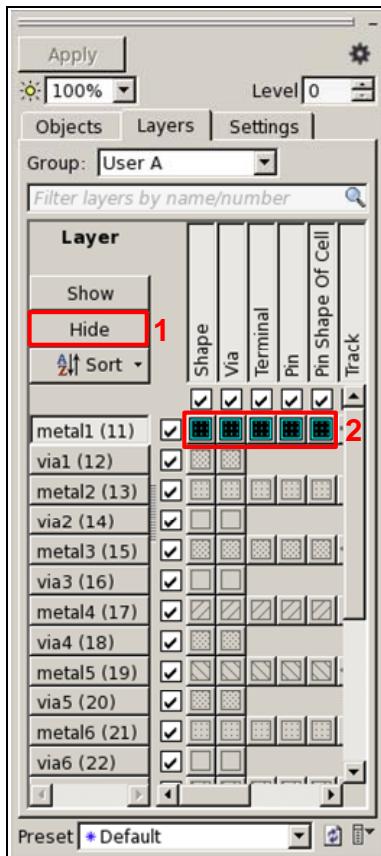


如果發生 Spacing 相關 DRC violation，但在 ICC 做 Verify route 時卻抓不到錯誤(**Total number of DRCs = 0**)，這個為虛擬製程本身的 Bug，正常 TSMC 與 UMC 製程不會出現 ICC Verify route 與 Calibre DRC 出現 Route violation 有 Mismatch 的問題。請參考下列流程解決：

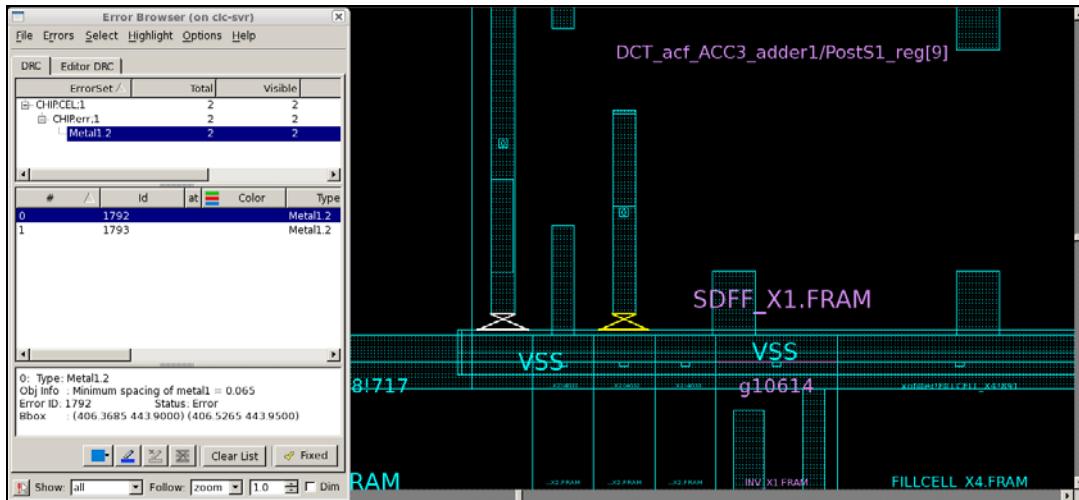
(1) 執行完上面 Step 4，可找出發生 DRC 錯誤的地方，訊息為違反 **Metal1 spacing** 的錯誤。



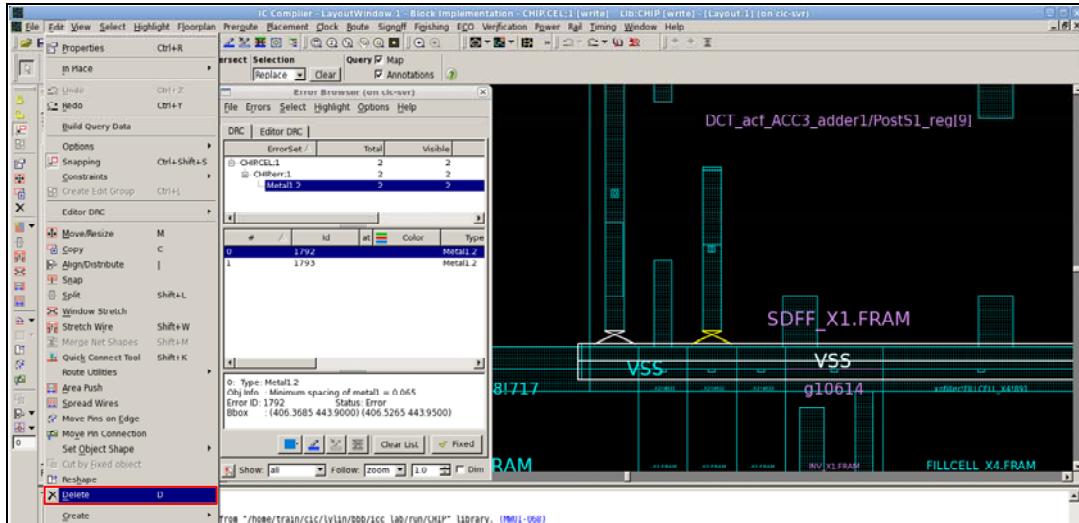
(2) 在左邊顯示的 Control Panel，Layers 設定的地方，先用左鍵點一下 Hide，將所有 Layers 顯示關閉，接著打開我們要觀察的 metal1 layer(將 metal1 的 Shape, Via, Terminal, Pin, Pin Shape of Cell 打開)。



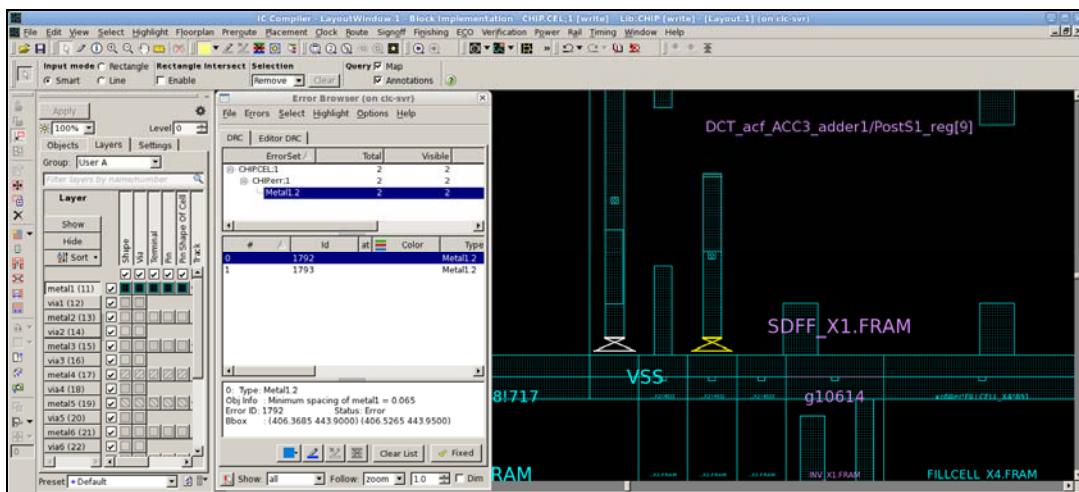
- (3) 可以觀察到 metal 1 spacing 的錯誤，是由於重疊的 Power Rail 造成，這個是虛擬製程本身的 Bug，請將多出來的 Power rail 刪除即可。



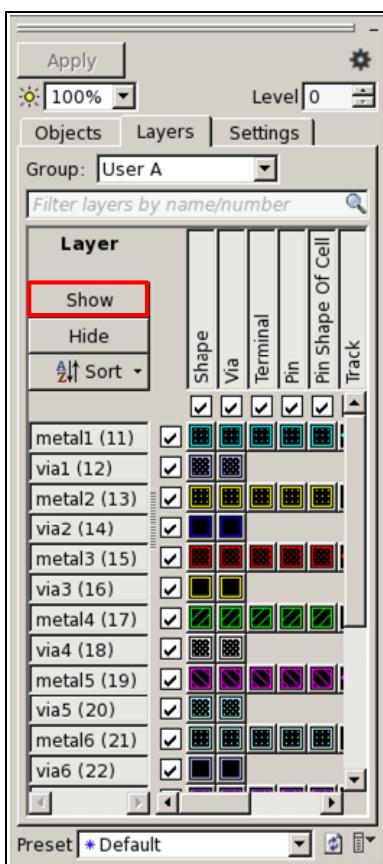
- (4) 刪除的方法：請用左鍵選取多出來的 Power rail，接著點選“Edit > Delete”，或直接按快捷鍵 D。注意多出來重疊的 Power rail 有 2 條，請 2 條都要刪除。



- (5) 刪除完成的畫面



- (6) 在左邊顯示的 Control Panel，Layers 設定的地方，用左鍵點一下 Show，恢復所有 Layers 顯示開啟。



- (7) 由於我們有修改 Layout，請重新執行 Lab 6 的 Step 13，重新產生 GDS，並且將新的 CHIP.gds 複製到“[..//verify/drc](#)”與“[..//verfy/lvs](#)”的資料夾，然後再跑一次 Calibre DRC。

5. 使用 Terminal 將目錄切換至 ~/icc\_lab/verify/lvs

```
unix% cd ~/icc_lab/verify/lvs
```

6. 產生 RAM Black Box 的 Verilog 和 Spice 檔

修改原來的 RF\_2P\_ADV64\_16\_lvs.v 檔，只留下 module、input、output 宣告和 endmodule，如還有其他 Memory 以此類推。

RF\_2P\_ADV64\_16\_lvs.v (已編輯完畢)

```
module RF_2P_ADV64_16(QA, CLKA, CENA, AA, CLKB, CENB, AB, DB, EMAA, EMAB);
    output [15:0]          QA;
    input           CLKA;
    input           CENA;
    input [5:0]         AA;
    input           CENB;
    input [5:0]         AB;
    input [15:0]        DB;
    input [2:0]          EMAA;
    input [2:0]          EMAB;
endmodule
```

利用 v2lvs 產生 RF\_2P\_ADV64\_16\_lvs.spi 檔(已產生)

```
unix% v2lvs -v RF_2P_ADV64_16_lvs.v -o RF_2P_ADV64_16_lvs.spi
```

RF\_2P\_ADV64\_16\_lvs.spi

```
$ Spice netlist generated by v2lvs
$ v2013.4_26.18
.SUBCKT RF_2P_ADV64_16 QA[15] QA[14] QA[13] QA[12] QA[11] QA[10] QA[9] QA[8]
VDD VSS
+ QA[7] QA[6] QA[5] QA[4] QA[3] QA[2] QA[1] QA[0] CLKA CENA AA[5] AA[4] AA[3]
+ AA[2] AA[1] AA[0] CLKB CENB AB[5] AB[4] AB[3] AB[2] AB[1] AB[0] DB[15] DB[14]
+ DB[13] DB[12] DB[11] DB[10] DB[9] DB[8] DB[7] DB[6] DB[5] DB[4] DB[3] DB[2]
+ DB[1] DB[0] EMAA[2] EMAA[1] EMAA[0] EMAB[2] EMAB[1] EMAB[0]
.ENDS
```

7. 修改 CHIP\_pr.v 將所有 Power pad 相關的關鍵字註解

```
//PADIOVSS io_vss7 (.VSSIO (SYNOPSYS_UNCONNECTED_189));
//PADIOVSS io_vss6 (.VSSIO (SYNOPSYS_UNCONNECTED_190));
//PADIOVSS io_vss5 (.VSSIO (SYNOPSYS_UNCONNECTED_191));
//PADIOVSS io_vss4 (.VSSIO (SYNOPSYS_UNCONNECTED_192));
//PADIOVSS io_vss3 (.VSSIO (SYNOPSYS_UNCONNECTED_193));
//PADIOVSS io_vss2 (.VSSIO (SYNOPSYS_UNCONNECTED_194));
```

```
//PADIOVSS io_vss1 (.VSSIO (SYNOPSYS_UNCONNECTED_195));  
//PADIOVDD io_vdd6 (.VDDIO (SYNOPSYS_UNCONNECTED_196));  
//PADIOVDD io_vdd5 (.VDDIO (SYNOPSYS_UNCONNECTED_197));  
//PADIOVDD io_vdd4 (.VDDIO (SYNOPSYS_UNCONNECTED_198));  
//PADIOVDD io_vdd3 (.VDDIO (SYNOPSYS_UNCONNECTED_199));  
//PADIOVDD io_vdd2 (.VDDIO (SYNOPSYS_UNCONNECTED_200));  
//PADIOVDD io_vdd1 (.VDDIO (SYNOPSYS_UNCONNECTED_201));  
//PADIOVDDPOC io_vdd7 (.VDDIO (SYNOPSYS_UNCONNECTED_202));
```

8. 將 CHIP\_pr.v 轉換成 spice 格式

```
v2lvs -v ./CHIP_pr.v -l NangateOpenCellLibrary_lvs.v -l RF_2P_ADV64_16_lvs.v -l tpz_lvs.v -s  
NangateOpenCellLibrary_lvs.spi -s RF_2P_ADV64_16_lvs.spi -s tpz_lvs.spi -o CHIP.spi -s1 VDD -s0  
VSS
```

或

```
unix% ./v2lvs_lab.sh
```

9. 修改 calibreLVS.rul(已編輯完畢)

```
LAYOUT PRIMARY "CHIP"  
LAYOUT PATH      "./CHIP.gds"  
  
SOURCE PRIMARY "CHIP"  
SOURCE PATH      "./CHIP.spi"
```

移除 IO Power & Ground 相關(已編輯完畢)

```
//LVS BOX  PADIOVDD  
//LVS BOX  PADIOVSS  
//LVS BOX  PADIOVDDPOC
```

移除 CORE Power & Ground 相關(已編輯完畢)

```
//LVS BOX  PADVDD  
//LVS BOX  PADVSS
```

移除 FILL 與 PADFILL 相關(已編輯完畢)

```
//LVS BOX FILLCELL_X1  
//LVS BOX FILLCELL_X2  
//LVS BOX FILLCELL_X4  
//LVS BOX FILLCELL_X8  
//LVS BOX FILLCELL_X16  
//LVS BOX FILLCELL_X32
```

```
//LVS BOX PADFILLER0005  
//LVS BOX PADFILLER05  
//LVS BOX PADFILLER1  
//LVS BOX PADFILLER5  
//LVS BOX PADFILLER10  
//LVS BOX PADFILLER20
```

並在最後新增一行(已編輯完畢)

```
LVS BOX RF_2P_ADV64_16
```

## 10. 執行 Calibre LVS

```
unix% calibre -lvs -spice layout.spi -hier -auto calibreLVS.rul
```

```
LVS completed. CORRECT. See report file: lvs.rep  
  
LVS completed. CPU TIME = 0 REAL TIME = 1 LVHEAP = 10/35/35 MALLOC = 78/78/78 ELAPSED TIME = 6  
--- LVS REPORT FILE = lvs.rep  
--- CALIBRE::LVS/XRC EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 1 LVHEAP = 1/35/35 MALLOC = 78/78/78 ELAPSED TIME = 6  
--- CALIBRE::LVS/XRC COMPLETED - Fri Dec 25 14:52:08 2015  
--- TOTAL CPU TIME = 0 REAL TIME = 1 LVHEAP = 1/35/35 MALLOC = 78/78/78 ELAPSED TIME = 6  
--- SPICE NETLIST FILE = layout.spi  
--- CIRCUIT EXTRACTION REPORT FILE = lvs.rep.ext  
--- GRAND TOTAL CPU TIME = 4 REAL TIME = 6 LVHEAP = 1/35/35 MALLOC = 78/78/78 ELAPSED TIME = 6
```

使用文字編輯器開啟 lvs.rep 檔案，找到 OVERALL COMPARISON RESULT 部份是否 match

OVERALL COMPARISON RESULTS

```
#      #####  
#      #  
#      #      CORRECT      #      *  *  
#  #      #      #      \_ /  
#      #####
```