Automated Chip Synthesis
Quick Reference

Version Y-2006.06, June 2006

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Man Page Viewing and Printing Instructions

The following sections describe how to set up your UNIX environment so you can view and print man pages.

Setting Up the UNIX Environment

Edit your .cshrc file to contain these lines:

```
setenv SYN_MAN_DIR synopsys_root/doc/syn/man
setenv MANPATH ${MANPATH}:${SYN_MAN_DIR}
```

SYN_MAN_DIR is a variable that contains the path to the man page directories, and *synopsys_root* represents the specific path to the Synopsys synthesis software directory at your site.

Viewing Man Pages From UNIX

Command

```
% man command_name
```

Variable

```
% man variable_name
```

Variable group

```
% man variable_group_name
```

All attributes

```
% man attributes
```

Attribute group

```
% man attribute_group_name
```

Error, warning, or information message

```
% man message_id
```

Viewing Man Pages From dc_shell

Command

```
dc_shell> man command_name
```

Variable

```
dc_shell> man variable_name
```

Variable group

```
dc_shell> man variable_group_name
```

All attributes

```
dc_shell> man attributes
```

Attribute group

```
dc_shell> man attribute_group_name
```

Error, warning, or information message

```
dc_shell> man message_id
```

Printing Man Pages From UNIX

User command

```
% man command_name | lpr [-P printer_name]
```

Synopsys command

```
% man command_name | lpr [-P printer_name]
```

Variable

```
% man variable_name | lpr [-P printer_name]
```

Variable group

```
% man variable_group_name \
    | lpr [-P printer_name]
```

All attributes

```
% man attributes | lpr [-P printer_name]
```

Attribute group

```
% man attribute_group_name \
    | lpr [-P printer_name]
```

You cannot print error, warning, or information message man pages from UNIX.

Printing Man Pages From dc_shell

You cannot print man pages from dc_shell.

Automated Chip Synthesis Commands

The following tools support the Automated Chip Synthesis feature: Design Compiler, Design Compiler FPGA, and Physical Compiler. Invoke these commands from within one of these tools. All Automated Chip Synthesis commands are available from a Tcl-based shell only.

acs_check_directories

Checks Automated Chip Synthesis (ACS) directory structure settings for correctness.

```
int acs_check_directories
```

acs_compile_design

Compiles the constrained RTL to a netlist using constraints propagated from the top-level design.

```
int acs_compile_design
[-destination pass_name]
[-prepare_only]
[-force]
[-update]
[-update_source source_pass]
design_name
```

acs_create_directories

Creates the project directory tree for Automated Chip Synthesis.

```
int acs_create_directories
```

acs_get_parent_partition

Creates a collection of designs that are compile partitions and that contain the specified subdesign.

```
string acs_get_parent_partition
design_name
[-hierarchy]
[-list]
```

acs_get_path

Gets the path location for the specified file. To specify a file, you specify its file type and for pass-dependent files, its pass directory.

```
string acs_get_path
-file_type filetype
[-mode read | write]
[-pass pass_name]
[-name filename [-append] ]
[-relative]
```

acs_merge_design

Preprocesses a design for incremental design update by merging the modified designs and their parent compile partitions with the mapped design being updated.

```
int acs_merge_design
[-auto_update | -update design_list]
[-unmapped source_dir]
[-mapped data_dir]
[-type pre | post]
[-destination dest_dir]
[-reference pre_compile_partition_dir]
design_name
```

acs_read_hdl

Reads in the HDL source code of a design and generates the GTECH representation.

```
int acs_read_hdl
[design_name]
[-hdl_source file_or_dir_list]
[-exclude_list file_or_dir_list]
[-format {verilog | vhdl}]
[-recurse]
[-no_dependency_check]
[-no_elaborate]
[-library design_lib_name]
[-verbose]
[-auto_update | -update file_list]
[-destination destination_dir]
```

acs_recompile_design

Compiles an unmapped constrained .db file using time budgets. The time budgets are created by using a previously mapped design.

```
int acs_recompile_design
-budget_source budget_pass
-destination destination_pass
[-source source_pass]
[-prepare_only]
[-force]
[-update]
[-update_source source_pass]
design_name
```

acs_refine_design

Refines an already mapped design.

```
int acs_refine_design
[-source pass_name]
[-destination pass_name]
[-prepare_only]
[-force]
[-update]
[-update_source source_pass]
design_name
```

acs_remove_dont_touch

Removes the dont_touch attributes on the specified designs.

```
int acs_remove_dont_touch
[-force | design_list]
```

acs_report_attribute

Reports the ACS attributes on the specified partitions.

```
int acs_report_attribute
[-partitions partition_list]
[attribute_name]
```

acs_report_directories

Reports the current directory structure settings.

```
int acs_report_directories
[-file_types type_list]
```

acs_report_user_messages

Reports the number of error, warning, and information messages.

```
int acs_report_user_messages
[-total]
[-errors]
[-warnings]
[-infos]
[-reset]
```

acs_reset_directory_structure

Resets the project directory tree for Automated Chip Synthesis to its default setting.

```
int acs_reset_directory_structure
```

acs_set_attribute

Sets Automated Chip Synthesis compile attributes on one or more partitions.

```
int acs_set_attribute
[-partitions partitions]
[attribute_value]
attribute_name
```

acs_submit

Specifies the compile configuration for normal compile partitions.

```
int acs_submit
[-command command]
[-host host]
[-exec exec]
[-show]
```

acs_submit_large

Specifies the compile configuration for large compile partitions.

```
int acs_submit_large
[-command command]
[-host host]
[-exec exec]
[-partitions part_list]
[-show]
```

acs_write_html

Creates an HTML page in the destination directory.

```
int acs_write_html
-destination pass_name
[-acs_work_dir acs_working_directory]
design_name
```

check_error

Prints extended information on errors from last command.

```
int check_error [-verbose] [-reset]
```

compile_partitions

Distributes compile jobs for a design.

```
compile_partitions -destination pass
```

create_pass_directories

Creates the directory structure required for storing Automated Chip Synthesis data.

```
int create_pass_directories pass_list
```

derive_constraints

Propagates design environment, constraints, and attribute settings from the top-level design to the specified subdesigns.

```
int derive_constraints
[-attributes_only]
[-verbose]
[-budget]
cell_list
```

read_partition

Reads the database for a design.

```
int read_partition
-source pass
-type pre | post
-format db | ddc
design_name
```

remove_pass_directories

Removes the data directories associated with the specified passes.

```
int remove_pass_directories pass_list
```

report_partitions

Lists the hierarchical designs and their associated attributes and relative size (estimated in RTL).

```
int report_partitions [-nosplit]
```

report_pass_data

Reports the data files that are available for a design created by Automated Chip Synthesis.

```
int report_pass_data
[-hierarchy]
[-pass_list pass_list]
[design]
```

set_compile_partitions

Specifies the compile partitions for the current design.

```
int set_compile_partitions
{-level level} | {-designs design_list} |
-all | -auto
[-force]
[-no_reset]
```

set_default_input_delay

Sets the value of the input delay as a percentage of the clock period to be assigned during environment propagation.

```
int set_default_input_delay
[-none]
[cell_or_pin_list]
percent_delay
```

set_default_output_delay

Sets the output delay as a percentage of the clock period to be assigned during environment propagation.

```
int set_default_output_delay
[-none]
[cell_or_pin_list]
percent_delay
```

set_svf

Generates a Formality setup information file for efficient compare point matching in Formality.

```
boolean set_svf
filename
[-append]
[-off]
```

sub_designs_of

Gets the subdesigns according to the options.

```
collection sub_designs_of
[-hierarchy]
[-in_partition | -partition_only]
[-dt_only | -ndt_only]
[-multiple_instances | -single_instances]
[-names_only]
design
```

sub_instances_of

Gets the subinstances according to the options.

```
collection sub_instances_of
[-hierarchy]
[-in_partition] [-partition_only]
[-dt_only] [-ndt_only]
[-of_references reference_list]
[-master_instance]
[-names_only]
design
```

write_compile_script

Writes a compile script for the specified design.

```
int write_compile_script
[-absolute_paths]
[-hierarchy]
[-no_reports]
[-refining]
-destination pass
[-update design_list]
[design]
```

write_environment

Writes the variable settings and constraints for the specified cells or designs.

```
write_environment
[-cells cell_list | -designs design_list]
[-output file_name]
[-suffix suffix]
[-environment_only]
[-constraints_only]
[-no_lib_info]
```

write_makefile

Writes a makefile that defines the dependencies and commands required to compile the specified design.

```
int write_makefile
[-absolute_paths]
[-dependencies depends]
-destination pass
[-target target_name]
[-lsf [-bsubargs bsub_args]]
[-update design_list]
[design]
```

write_partition

Writes the database for a design into the Automated Chip Synthesis data structure.

```
int write_partition
-type pre | post
[-destination pass]
[-hierarchy]
[design]
```

write_partition_constraints

Writes out the timing constraints for a design.

```
int write_partition_constraints
[-hierarchy]
-destination pass
[-update design_list]
[design]
```

Automated Chip Synthesis Variables

Automated Chip Synthesis defines a set of variables that are used to control its behavior. These variables have an effect in dctcl mode only.

acs_area_report_suffix

Specifies the suffix for area reports generated during the automated compile process.

Default value for this variable is area.

acs_autopart_max_area

Defines partition threshold; used with other acs variables to control chip-level partitioning.

Default value for this variable is 0.0 (no maximum area specified).

acs_autopart_max_percent

Controls chip-level partitioning; used with other acs variables.

Default value for this variable is 0.0% (no maximum percentage specified).

acs_budgeted_cstr_suffix

Specifies the suffix for constraint files generated by the derive_partition_budgets command.

Default value for this variable is con.

acs_compile_script_suffix

Specifies the default suffix for script files generated by the write_compile_script command, sourced in the makefile generated by the write_makefile command, and located by the report_pass_data command.

Default value for this variable is autoscr.

acs_constraint_file_suffix

Specifies the default suffix for constraint files generated by write_partition_constraints during the automated compile process.

Default value for this variable is con.

acs_cstr_report_suffix

Specifies the default suffix for constraint reports generated during the automated compile process.

Default value for this variable is cstr.

acs_db_suffix

Specifies the default suffix for .db files that are read or written during the automated compile process.

Default value for this variable is db.

acs_dc_exec

Specifies the location of the dc_shell executable. This variable is used by the acs_compile_design, acs_refine_design, and acs_recompile_design commands to generate the makefile.

Default value for this variable is $SYNOPSYS/$arch/syn/bin/dc_shell.

acs_default_pass_name

Specifies the prefix for the default data directory names. The pass number (either 0 or 1) is added to the prefix to generate the directory name.

Default value for this variable is pass.

acs_exclude_extensions

Specifies the file endings of files you do not want the acs_read_hdl command to analyze.

Default value for this variable is "".

acs_exclude_list

Specifies files and directories you do not want the acs_read_hdl command to analyze.

Default value for this variable is "[list $synopsys_root]".

acs_global_user_compile_strategy_script

Specifies the base file name for the user-defined default compile strategy.

Default value for this variable is default.

acs_hdl_source

Specifies the location of the source code files analyzed by the acs_read_hdl command.

Default value for this variable is "".

acs_hdl_verilog_define_list

Specifies a list of text macros which are to be defined by the acs_read_hdl command during verilog file analysis.

Default value for this variable is "".

acs_lic_wait

Specifies the maximum wait time for checking out all the licenses required by a compile job.

Default value for this variable is 0.

acs_log_file_suffix

Specifies the default suffix for log files generated during the automated compile process.

Default value for this variable is log.

acs_make_args

Specifies the command arguments for the make utility command (gmake, by default).

Default value for this variable is "-j".

acs_make_exec

Specifies the make utility command used to run the compile jobs.

Default value for this variable is gmake.

acs_makefile_name

Specifies the file name for the makefile generated by the write_makefile command and run by the compile_partitions command.

Default value for this variable is makefile.

acs_num_parallel_jobs

Specifies the number of compile jobs to run in parallel when using gmake as the make utility. .

Default value for this variable is 1.

acs_override_report_suffix

Specifies the suffix for user-defined partition report scripts.

Default value for this variable is report.

acs_override_script_suffix

Specifies the suffix for user-defined partition compile scripts.

Default value for this variable is scr.

acs_qor_report_suffix

Specifies the suffix for QOR reports generated during the automated compile process; the default is qor.

Default value for this variable is qor.

acs_svf_suffix

Specifies the suffix for SVF files generated during the automated compile process.

Default value for this variable is svf.

acs_timing_report_suffix

Specifies the suffix for timing reports generated during the automated compile process.

Default value for this variable is tim.

acs_use_autopartition

Sets autopartitioning as the default partitioning strategy for the chip-level compile commands.

Default value for this variable is false.

acs_use_default_delays

Sets top-down environment propagation as the constraint generation method for GTECH designs (the acs_compile_design command). When this variable is false (the default), the acs_compile_design command uses RTL budgeting to generate constraints for the compile partitions.

Default value for this variable is false.

acs_user_budgeting_script

Specifies the file name for the user-defined budgeting script.

Default value for this variable is budget.scr.

acs_user_compile_strategy_script_suffix

Specifies the suffix for user-defined partition compile strategies.

Default value for this variable is compile.

acs_verilog_extensions

Specifies the file endings of files analyzed as Verilog source code by the acs_read_hdl command.

Default value for this variable is ".v".

acs_vhdl_extensions

Specifies the file endings of files the acs_read_hdl command analyzes as VHDL source code.

Default value for this variable is vhd.

acs_work_dir

Specifies the root of the Automated Chip Synthesis project directory.

Default value for this variable is the current working directory.

check_error_list

Specifies the error codes that the check_error command checks for.

Default value for this variable is EQN-16 EQN-18 EQN-20.

default_input_delay

Specifies the global default input delay value to be used for environment propagation.

Default value for this variable is 30.0.

default_output_delay

Specifies the global default output delay value to be used for environment propagation.

Default value for this variable is 30.0.