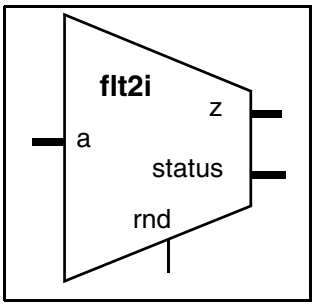
# DW_fp_flt2i

## Floating-Point to Integer Converter

Version, STAR, and myDesignWare Subscriptions: IP Directory

## Features and Benefits

- The precision format is parameterizable for either IEEE single, double precision, or a user-defined custom format
- Accuracy conforms to IEEE 754 standard
- DesignWare datapath generator is employed for better timing and area




## Revision History

## Description

DW_fp_flt2i is a floating-point to integer converter that takes a floating-point number, a, to produce an integer number, z. The output z is always a signed two's complement integer.

Component pins are described in Table 1-1 and configuration parameters are described in Table 1-2.

**Table 1-1 Pin Description**

| Pin Name | Width | Direction | Function |
|---|---|---|---|
| a | (*sig_width* + *exp_width* + 1) bits | Input | Floating-point number |
| rnd | 3 bits | Input | Rounding mode; supports all rounding modes described in the *Datapath Floating-Point Overview* |
| z | *isize* bits | Output | Two's complement integer number |
| status | 8 bits | Output | Status flags for the result z<br>For details, see STATUS Flags in the *Datapath Floating-Point Overview.* |

**Table 1-2 Parameter Description**

| Parameter | Values | Description |
|---|---|---|
| sig_width | 2 to 253<br>Default: 23 | Word length of fraction field of floating-point number a |
| exp_width | 3 to 31<br>Default: 8 | Word length of biased exponent of floating-point number a |
| isize | 3 to 512<br>Default: 32 | Word length of converted integer number z |

**Table 1-2 Parameter Description (Continued)**

| Parameter | Values | Description |
|---|---|---|
| ieee_compliance | 0 or 1<br>Default: 0 | Level of support for IEEE 754:<br>■ 0: No support for IEEE 754 NaNs and denormals; NaNs are considered infinities and denormals are considered zeros<br>■ 1: Fully compliant with the IEEE 754 standard, including support for NaNs and denormals<br>For more, see IEEE 754 Compatibility in the *Datapath Floating-Point Overview*. |

**Table 1-3 Synthesis Implementations**

| Implementation Name | Function | License Feature Required |
|---|---|---|
| rtl | Fast Synthesis model | DesignWare |

**Table 1-4 Simulation Models**

| Model | Function |
|---|---|
| DW02.DW_FP_FLT2I_CFG_SIM | Design unit name for VHDL simulation |
| dw/dw02/src/DW_fp_flt2i_sim.vhd | VHDL Simulation Model Source Code |
| dw/dw02/sim_ver/DW_fp_flt2i.v | Verilog Simulation Model Source Code |

**Table 1-5 Function Example 1 (*sig_width* = 10, *exp_width* = 5, *isize* = 16, *ieee_compliance* = 0)**

| Description | a (FP format) | rnd | status | z (Integer Number) |
|---|---|---|---|---|
| Zero | 0000_0000_0000_0000 | any | 0000_0001 | 0000_0000_0000_0000 |
| Denormal | 0000_0000_0000_0001 | any | 0000_0001 | 0000_0000_0000_0000 |
| Infinity | 0111_1100_0000_0000 | any | 0110_0000 | 0111_1111_1111_1111 |
| | 1111_1100_0000_0000 | any | 0110_0000 | 1000_0000_0000_0000 |
| NaN | 0111_1100_0000_0001 | any | 0110_0000 | 0111_1111_1111_1111 |
| | 1111_1100_0000_0001 | any | 0110_0000 | 1000_0000_0000_0000 |

**Table 1-5 Function Example 1 (*sig_width* = 10, *exp_width* = 5, *isize* = 16, *ieee_compliance* = 0) (Continued)**

| Description | a (FP format) | rnd | status | z (Integer Number) |
|---|---|---|---|---|
| Normal Number | 0110_0011_1111_1111 | 0 | 0010_0000 | 0000_0100_0000_0000 |
| | 0110_0011_1111_1111 | 1 | 0010_0000 | 0000_0011_1111_1111 |
| | 0110_0011_1111_1111 | 2 | 0010_0000 | 0000_0100_0000_0000 |
| | 0110_0011_1111_1111 | 3 | 0010_0000 | 0000_0011_1111_1111 |
| | 0110_0011_1111_1111 | 4 | 0010_0000 | 0000_0100_0000_0000 |
| | 0110_0011_1111_1111 | 5 | 0010_0000 | 0000_0100_0000_0000 |
| | 1110_0011_1111_1111 | 0 | 0010_0000 | 1111_1100_0000_0000 |

**Table 1-6 Function Example 2 (*sig_width* = 10, *exp_width* = 5, *isize* = 16, *ieee_compliance* = 1)[a]**

| Description | a (FP Format) | rnd | status | z (Integer Number) |
|---|---|---|---|---|
| Zero | 0000_0000_0000_0000 | any | 0000_0001 | 0000_0000_0000_0000 |
| Denormal | 0000_0000_0000_0001 | 0, 1, 3, 4 | 0010_1001 | 0000_0000_0000_0000 |
| | 0000_0000_0000_0001 | 2, 5 | 0010_0000 | 0000_0000_0000_0001 |
| | 1000_0000_0000_0001 | 0, 1, 2, 4 | 0010_1001 | 0000_0000_0000_0000 |
| | 1000_0000_0000_0001 | 3, 5 | 0010_0000 | 1111_1111_1111_1111 |
| Infinity | 0111_1100_0000_0000 | any | 0000_0100 | 0111_1111_1111_1111 |
| | 1111_1100_0000_0000 | any | 0000_0100 | 1000_0000_0000_0000 |
| NaN | 0111_1100_0000_0001 | any | 0000_0100 | 0111_1111_1111_1111 |
| | 1111_1100_0000_0001 | any | 0000_0100 | 1000_0000_0000_0000 |
| Normal Number | 0110_0011_1111_1111 | 0 | 0010_0000 | 0000_0100_0000_0000 |
| | 0110_0011_1111_1111 | 1 | 0010_0000 | 0000_0011_1111_1111 |
| | 0110_0011_1111_1111 | 2 | 0010_0000 | 0000_0100_0000_0000 |
| | 0110_0011_1111_1111 | 3 | 0010_0000 | 0110_0011_1111_1111 |
| | 0110_0011_1111_1111 | 4 | 0010_0000 | 0000_0100_0000_0000 |
| | 0110_0011_1111_1111 | 5 | 0010_0000 | 0110_0011_1111_1111 |
| | 1110_0011_1111_1111 | 0 | 0010_0000 | 1111_1100_0000_0000 |

a. Although the output is an integer number, the tiny bit is set when denormal input is rounded to 0.

## Suppressing Warning Messages During Verilog Simulation

The Verilog simulation model includes macros that allow you to suppress warning messages during simulation.

To suppress all warning messages for all DWBB components, define the DW_SUPPRESS_WARN macro in either of the following ways:

- Specify the Verilog preprocessing macro in Verilog code:

  ```
  `define DW_SUPPRESS_WARN
  ```

- Or, include a command line option to the simulator, such as:

  `+define+DW_SUPPRESS_WARN` (which is used for the Synopsys VCS simulator)

The warning messages for this model include the following:

- If an invalid rounding mode has been detected on `rnd`, the following message is displayed:

  ```
  WARNING: <instance_path>:
      at time = <timestamp>: Illegal rounding mode.
  ```

  To suppress this message, use the DW_SUPPRESS_WARN macro explained earlier.

## Related Topics

- Datapath Floating-Point Overview
- DesignWare Building Block IP User Guide

## HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DW_Foundation_comp.all;
-- If using numeric types from std_logic_arith package,
-- comment the preceding line and uncomment the following line:
-- use DWARE.DW_Foundation_comp_arith.all;

entity DW_fp_flt2i_inst is
  generic (
    inst_sig_width : POSITIVE := 23;
    inst_exp_width : POSITIVE := 8;
    inst_isize     : INTEGER := 32
  );
  port (
    inst_a      : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
    inst_rnd    : in std_logic_vector(2 downto 0);
    z_inst      : out std_logic_vector(inst_isize-1 downto 0);
    status_inst : out std_logic_vector(7 downto 0)
  );
end DW_fp_flt2i_inst;


architecture inst of DW_fp_flt2i_inst is

begin

  -- Instance of DW_fp_flt2i
  U1 : DW_fp_flt2i
  generic map (
    sig_width => inst_sig_width,
    exp_width => inst_exp_width,
    isize => inst_isize
  )
  port map (
    a => inst_a,
    rnd => inst_rnd,
    z => z_inst,
    status => status_inst
  );

end inst;


-- pragma translate_off
configuration DW_fp_flt2i_inst_cfg_inst of DW_fp_flt2i_inst is
   for inst
   end for;
```

```
end DW_fp_flt2i_inst_cfg_inst;
-- pragma translate_on
```

## HDL Usage Through Component Instantiation - Verilog

```
module DW_fp_flt2i_inst( inst_a, inst_rnd, z_inst, status_inst );

parameter inst_sig_width = 23;
parameter inst_exp_width = 8;
parameter inst_isize = 32;
parameter inst_ieee_compliance = 0;


input [inst_sig_width+inst_exp_width : 0] inst_a;
input [2 : 0] inst_rnd;
output [inst_isize-1 : 0] z_inst;
output [7 : 0] status_inst;

    // Instance of DW_fp_flt2i
    DW_fp_flt2i #(inst_sig_width, inst_exp_width, inst_isize, inst_ieee_compliance) U1
(
                .a(inst_a),
                .rnd(inst_rnd),
                .z(z_inst),
                .status(status_inst) );

endmodule
```

## Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

| Date | Release | Updates |
|---|---|---|
| July 2020 | DWBB_201912.5 | ■ Adjusted the description of the *ieee_compliance* parameter in Table 1-2 on page 1<br>■ Added "Suppressing Warning Messages During Verilog Simulation" on page 4 |
| December 2019 | DWBB_201912.0 | ■ For STAR 9001572518, corrected status bits for infinity and NAN entries in Table 1-6 on page 3<br>■ Added this Revision History table and the document links on this page |

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