DWF_dp_mult_ovfldet procedure

Multiply and Overflow Detection

Version, STAR, and myDesignWare Subscriptions: IP Directory

Description

The DWF_dp_mult_ovfldet procedure multiplies the two arguments a and b, truncates the upper bits of the result to the width specified by argument *p_width* and returns the truncated value and an overflow flag that indicates whether an overflow (or underflow) occurred. A dedicated overflow detection is used to improve the QoR of the multiplier.

Table 1-1 Function Names

Function Name	Description
DWF_dp_mult_ovfldet	VHDL unsigned multiply and overflow detection
DWF_dp_mult_ovfldet	VHDL signed (two’s complement) multiply and overflow detection
DWF_dp_mult_ovfldet_uns	Verilog unsigned multiply and overflow detection
DWF_dp_mult_ovfldet_tc	Verilog signed (two’s complement) multiply and overflow detection

Table 1-2 Argument Description

Name	Type	Direction	Width / Values	Description
a	Vector	Input	a_width	Input multiplier
b	Vector	Input	b_width	Input multiplicand
p	Vector	Output	p_width	Output product
ovfl	Bit	Output	1	Output overflow flag

Table 1-3 Parameter Description (Verilog)

Parameter	Values	Description
a_width	≥ 2	Word length of input a
b_width	≥ 2	Word length of input b
p_width	≥ 2	Word length of output product

Verilog Include File: DW_dp_mult_ovfldet_function.inc

Functional Description

```
DWF_dp_mult_ovfldet (a[a_width-1:0], b[b_width-1:0], z[p_width-1:0], ovfl)
```

Unsigned Multiply and Overflow Detection

```
p[a_width+b_width-1:0]   = a[a_width-1:0] * b[b_width-1:0]
z[p_width-1:0]           = p[p_width-1:0]
ovfl                     = 1   if p[a_width+b_width-1:0] > $2^{p\_width}-1$
                         = 0   else
```

Signed Multiply and Overflow Detection

```
p[a_width+b_width-1:0]   = a[a_width-1:0] * b[b_width-1:0]
z[p_width-1:0]           = { p[a_width+b_width-1], p[p_width-2:0] }
ovfl                     = 1   if p[a_width+b_width-1:0] > $2^{p\_width-1}-1$
                         = 1   else if p[a_width+b_width-1:0] < $-2^{p\_width-1}$
                         = 0   else
```

NOTE: For signed multiply, the truncated output keeps the sign of the non-truncated result (corresponds to the 'resize' function in VHDL).

For more information about the DesignWare datapath functions, refer to the topic titled DesignWare Datapath Functions Overview.

Related Topics

- DesignWare Datapath Functions Overview
- DesignWare Building Block IP User Guide

VHDL Example

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use DWARE.DW_dp_functions.all;
-- DWARE.DW_dp_functions_arith package if IEEE.std_logic_arith is used

entity DWF_dp_mult_ovfldet_test is
  port (a, b, c : in  unsigned(7 downto 0);
        z       : out unsigned(7 downto 0));
end DWF_dp_mult_ovfldet_test;

architecture rtl of DWF_dp_mult_ovfldet_test is
  signal p        : unsigned(7 downto 0);
  signal overflow : std_logic;
begin
  DWF_dp_mult_ovfldet (a, b, p, overflow);
  z <= p + c when overflow = '0' else "11111111";
end rtl;
```

Verilog Example

```
module DWF_dp_mult_ovfldet_test (a, b, c, z);

  input  [7:0] a, b, c;
  output [7:0] z;

  reg    [7:0] p;
  reg          overflow;

  // Passes the parameters to the function
  parameter a_width = 8;
  parameter b_width = 8;
  parameter p_width = 8;

  // add "$SYNOPSYS/dw/sim_ver" to the search path for simulation
  `include "DW_dp_mult_ovfldet_function.inc"

  always @* begin
    DWF_dp_mult_ovfldet_uns (a, b, p, overflow);
  end
  assign z = (overflow == 1'b0) ? p + c : 8'b11111111;

endmodule
```

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