DW04_par_gen

Parity Generator and Checker

Version, STAR, and myDesignWare Subscriptions: IP Directory

Features and Benefits

Revision History

- Generates parity for given input data
- Supports even and odd parity, selectable via a parameter
- Supports variable word widths
- Inferable using a function call

Applications

- Parity generation and checking on external DRAM
- Parity generation and checking on internal or external SRAM
- Parity generation and checking on words transmitted in telecommunications, via UART, disk drives, and so on

Description

The DW04_par_gen is a parity generator and checker circuit that is designed for systems such as computers, peripherals, and communications devices that require improved data integrity over unprotected systems.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
datain	*width* bits	Input	Input data word to check or generate parity
parity	1 bit	Output	Generated parity (see Table 1-5 on page 2)

Table 1-2 Parameter Description

Parameter	Values[a]	Description
width	1 to 256	Defines the width of the input bus
par_type	0 or 1	Defines the type of parity

a. The upper bound of the legal range is a guideline to ensure reasonable compile times.

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
str	Synthesis model	DesignWare

Table 1-4 Simulation Models

Model	Function
DW04.DW04_PAR_GEN__SIM	Design unit name for VHDL simulation
dw/dw04/src/DW04_par_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW04_par.v	Verilog simulation model source code

Table 1-5 Truth Table

datain	*par_type* parameter	parity
even number of 1s	0 (even)	1
odd number of 1s	0 (even)	0
even number of 1s	1 (odd)	0
odd number of 1s	1 (odd)	1

When input data is applied to `datain`, which is *width* bits in size, parity is generated at the output, `parity`, based on the value of the *par_type* parameter. This parameter selects whether odd or even parity is generated, as shown in Table 1-5.

Application Example

Extending the DW04_par_gen to a parity checker is accomplished by performing an exclusive-OR of the parity output of DW04_par_gen with the parity bit of the parity-checked input word received.

Related Topics

- Application Specific – Data Integrity Overview
- DesignWare Building Block IP User Guide

HDL Usage Through Function Inferencing - VHDL

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use DWARE.DW_foundation_arith.all;

entity DW04_par_gen_func is
  generic(func_width :integer:=8;   func_par_type: INTEGER := 1);
  port(func_data_in : in std_logic_vector(func_width-1 downto 0);
       parity_func  : out std_logic);
end DW04_par_gen_func;

architecture func of DW04_par_gen_func is
begin
  parity_func <= DWF_parity_gen(func_par_type, func_data_in);
end func;
```

HDL Usage Through Function Inferencing - Verilog

DW_parity_gen is an obsoleted function. Using this function multiple times may cause inconsistent logic when the initial parameter value is smaller than the actual parameter value. This is because HDL Compiler currently does not support defparam Verilog functions. For the detailed information, refer to STARs 59352 and 59348.

This function is released only for backward compatibility. New users should not use this function. Instead, new users should use this part through component instantiation.

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW04_par_gen_inst is
  generic (inst_width    : POSITIVE := 8;
           inst_par_type : INTEGER := 1  );
  port (inst_datain : in std_logic_vector(inst_width-1 downto 0);
        parity_inst : out std_logic  );
end DW04_par_gen_inst;

architecture inst of DW04_par_gen_inst is
begin

  -- Instance of DW04_par_gen
  U1 : DW04_par_gen
    generic map (width => inst_width,   par_type => inst_par_type )
    port map ( datain => inst_datain,   parity => parity_inst );
end inst;

-- pragma translate_off
configuration DW04_par_gen_inst_cfg_inst of DW04_par_gen_inst is
  for inst
  end for; -- inst
end DW04_par_gen_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW04_par_gen_inst( inst_datain, parity_inst );

  parameter width = 8;
  parameter par_type = 1;

  input [width-1 : 0] inst_datain;
  output parity_inst;

  // Instance of DW04_par_gen
  DW04_par_gen #(width, par_type)
    U1 ( .datain(inst_datain),   .parity(parity_inst) );
endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
January 2019	DWBB_201806.5	■ Updated example in "HDL Usage Through Component Instantiation - VHDL" on page 5 ■ Added this Revision History table and the document links on this page

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