



DWF_dp_simd_add functions

SIMD add

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Description

The DWF_dp_simd_add functions implement a configurable SIMD adder. They allow you to either add arguments *a* and *b* as full-width vectors (for example, one 32-bit addition) or to add smaller partitions of *a* and *b* using multiple parallel adders (for example, two 16-bit additions or four 8-bit additions). Argument *no_confs* specifies the number of possible configurations and argument *conf* dynamically selects one configuration. Configuration with number *conf* has 2^{conf} partitions of size $\text{width}/2^{\text{conf}}$. Arguments *a*, *b*, and the return value are all either unsigned or signed (two's complement).

Table 1-1 Function Names

Function Name	Description
DWF_dp_simd_add	VHDL unsigned SIMD add
DWF_dp_simd_add	VHDL signed (two's complement) SIMD add
DWF_dp_simd_add_uns	Verilog unsigned SIMD add
DWF_dp_simd_add_tc	Verilog signed (two's complement) SIMD add

Table 1-2 Argument Description

Argument Name	Type	Width / Values	Description
<i>a</i>	Vector ^a	width	Input addend
<i>b</i>	Vector ^a	width	Input addend
<i>no_confs</i>	Integer	≥ 2	Number of configurations (VHDL only, constant)
<i>conf</i>	Vector ^b	$\text{ceil}(\log_2[\text{no_confs}])$	Configuration selection: 2^{conf} partitions of size $\text{width}/2^{\text{conf}}$
DWF_dp_simd_add	Vector ^a	width	Returned value

a. unsigned or signed in VHDL

b. std_logic_vector in VHDL

Table 1-3 Parameter Description (Verilog)

Parameter	Values	Description
<i>width</i>	≥ 2 , must be a multiple of $2^{\text{no_confs}-1}$	Word length
<i>no_confs</i>	≥ 2	Number of configurations

Verilog Include File: DW_dp_simd_add_function.inc

Functional Description

```
z[width-1:0] = DWF_dp_simd_add (a[width-1:0], b[width-1:0],
                                no_confs, conf[bit_width(no_confs)-1:0])

conf = 0:
    z[width-1:0]          = a[width-1:0]          + b[width-1:0]
conf = 1:
    z[width-1:width/2]    = a[width-1:width/2]    + b[width-1:width/2]
    z[width/2-1:0]        = a[width/2-1:0]        + b[width/2-1:0]
conf = 2:
    z[width-1:width*3/4]  = a[width-1:width*3/4]  + b[width-1:width*3/4]
    z[width*3/4-1:width/2] = a[width*3/4-1:width/2] + b[width*3/4-1:width/2]
    z[width/2-1:width/4]  = a[width/2-1:width/4]  + b[width/2-1:width/4]
    z[width/4-1:0]        = a[width/4-1:0]        + b[width/4-1:0]
...

```

Example: width = 32, no_confs = 3

```
conf = 0:
    z[31: 0] = a[31: 0] + b[31: 0]
conf = 1:
    z[31:16] = a[31:16] + b[31:16]
    z[15: 0] = a[15: 0] + b[15: 0]
conf = 2:
    z[31:24] = a[31:24] + b[31:24]
    z[23:16] = a[23:16] + b[23:16]
    z[15: 8] = a[15: 8] + b[15: 8]
    z[ 7: 0] = a[ 7: 0] + b[ 7: 0]

```

For more information about the DesignWare datapath functions, refer to [DesignWare Datapath Functions Overview](#).

Related Topics

- [DesignWare Datapath Functions Overview](#)
- [DesignWare Building Block IP User Guide](#)

VHDL Example

```

library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use DWARE.DW_dp_functions.all;
-- DWARE.DW_dp_functions_arith package if IEEE.std_logic_arith is used

entity DWF_dp_simd_add_test is
  port (op1, op2  : in  signed(31 downto 0);
        config_no : in  std_logic_vector(1 downto 0);
        sum       : out signed(31 downto 0));
end DWF_dp_simd_add_test;

architecture rtl of DWF_dp_simd_add_test is
begin
  sum <= DWF_dp_simd_add (a => op1, b => op2,
                        no_confs => 3, conf => config_no);
end rtl;

```

Verilog Example

```

module DWF_dp_simd_add_test (op1, op2, config_no, sum);

  input  signed [31:0] op1, op2;
  input          [1:0] config_no;
  output signed [31:0] sum;

  // Passes the parameters to the function
  parameter width      = 32;
  parameter no_confs = 3;

  // add "$SYNOPSYS/dw/sim_ver" to the search path for simulation
  `include "DW_dp_simd_add_function.inc"

  assign sum = DWF_dp_simd_add_tc (op1, op2, config_no);

endmodule

```

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