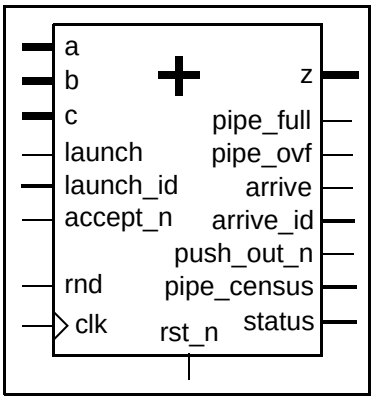
DW_lp_piped_fp_sum3

Low Power Pipelined 3-input Floating Point Adder

Version, STAR, and myDesignWare Subscriptions: IP Directory

Features and Benefits

Revision History



- The precision format is parameterizable for either IEEE single, double precision, or a user-defined custom format
- Hardware for denormal numbers of IEEE 754 standard is selectively provided.
- Fully compatible with the IEEE 754 standard with proper set of parameters
- DesignWare datapath generator is employed for better timing and area
- Saves power by only enabling stages as needed
- Saves power based on input data patterns
- Parameter controlled pipeline stages
- Flow control to interface directly to FIFO
- Flow control interfaces to another managed pipe
- Bubble removal extends depth of subsequent FIFO by pipe depth
- Parameter sized identifier tracks data operations

Description

DW_lp_piped_fp_sum3 is a floating point operator that adds three floating point operands: `a`, and `b`, and `c`, to produce a floating point sum, `z`. The input `rnd` is a 3-bit rounding mode (see Rounding Modes in the *Datapath Floating-Point Overview*) and the output `status` is an 8-bit `status` flag. The operation is conditionally managed by the DW_lp_pipe_mgr, a pipeline controller (if enabled when *no_pm* = 0). The component is configured with a user selectable number of *stages* of logic, allowing design compiler to optimize the logic between register stages to reduce power and area. DC is able to take advantage of the enable signals provided in the design to optimize the combinational logic throughout the addition operation. When *no_pm* = 0, the pipeline manager can manage the enabling of register stages of a pipeline based on `launch` requests that track the progress of a pipelined operation. Enabling stages of the pipeline only when they need to be clocked reduces dynamic power and is further enhanced through clock gate insertion (which requires Power Compiler). Launch requests can be accompanied by a `launch_id` which can be used as a tag to identify operation results as they pass out of the pipe. The `pipe_census` output monitors the number of operations in the pipe.

When *no_pm* = 1, DW_lp_piped_fp_sum3 satisfies the need to speed up designs via pipelining and still enable register re-timing capability as well as providing identification handle used tracking each initiated transaction. However, low power and flow control can only be obtained by setting *no_pm* = 0, thus using the

pipeline management mechanism (DW_lp_pipe_mgr). For implementation specific details on the actual 3-input add function, see the DW_fp_sum3 datasheet.

Component pins are described in Table 1-1 and configuration parameters are described in Table 1-2.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
a	(*sig_width* + *exp_width* + 1) bits	Input	Input data
b	(*sig_width* + *exp_width* + 1) bits	Input	Input data
c	(*sig_width* + *exp_width* + 1) bits	Input	Input data
rnd	3 bits	Input	Rounding mode; supports all rounding modes described in the *Datapath Floating-Point Overview*
z	(*sig_width* + *exp_width* + 1) bits	Output	(a + b) + c
status	8 bits	Output	Status flags for the result z For details, see STATUS Flags in the *Datapath Floating-Point Overview.*
launch	1 bit	Input	Active high control input to launch data into pipe
launch_id	*id_width* bits	Input	ID of launch
pipe_full	1 bit	Output	Status flag indication no available slot in pipe
pipe_ovf	1 bit	Output	Error flag indicating pipe overflow (data lost)
accept_n	1 bit	Input	Flow control input (active low)
arrive	1 bit	Output	z result is valid
arrive_id	*id_width* bits	Output	launch_id from the originating launch that produced the z result
push_out_n	1 bit	Output	Optional output used with FIFO (active low)
pipe_census	*ceiling(log_2(maximum(1,in_reg + (stages-1) + out_reg) + 1))* bits	Output	Output bus indicating the number of pipe stages currently occupied

Table 1-2 Parameter Description

Parameter	Values	Description
sig_width	2 to 253 bits	Word length of fraction field of floating point numbers a, b, c, and z
exp_width	3 to 31 bits	Word length of biased exponent of floating point numbers a, b, c, and z

Table 1-2 Parameter Description (Continued)

Parameter	Values	Description
ieee_compliance	0 or 1	Level of support for IEEE 754: ■ 0: No support for IEEE 754 NaNs and denormals; NaNs are considered infinities and denormals are considered zeros ■ 1: Fully compliant with the IEEE 754 standard, including support for NaNs and denormals For more, see IEEE 754 Compatibility in the *Datapath Floating-Point Overview*.
arch_type	0 or 1 Default: 0	Controls the use of an alternative architecture 0: Selects previous architecture 1: Selects alternative architecture; when value is 1, *ieee_compliance* must be 0
op_iso_mode	0 to 4 Default: 0	Operand isolation mode (controls datapath gating for minPower flow) Allows you to set the style of minPower datapath gating for this module ■ 0: Use the DW_lp_op_iso_mode[a] synthesis variable ■ 1: 'none' ■ 2: 'and' ■ 3: 'or' ■ 4: Preferred gating style: ‘and’ Datapath gating is inserted only when there are no input registers on the operands at the component boundary. When inserted, datapath gating circuits are placed immediately after the input ports of the component (see Figure 1-3 on page 7).
id_width	1 to 1024 Default: 1	Width of input `launch_id` and output `arrive_id`
in_reg	0 or 1 Default: 0	Input register control ■ 0: No input register ■ 1: Include input register
stages	1 to 1022 Default: 2	Number of logic stages
out_reg	0 or 1 Default: 0	Output register control ■ 0: No output register ■ 1: Include output register
no_pm	0 or 1 Default:1	No pipeline management used ■ 0: Use pipeline management ■ 1: Do not use pipeline management
rst_mode		Reset mode ■ 0: Asynchronous reset mode for `rst_n` ■ 1: Synchronous reset mode for `rst_n`

a. The DW_lp_op_iso_mode synthesis variable is available only in Design Compiler.
DW_lp_op_iso_mode sets a global style of datapath gating. To use the global style, set *op_iso_mode* to '0', Note that If the *op_iso_mode* parameter is set to '0' and DW_lp_op_iso_mode is either not set or set to 0', then no datapath gating is inserted for this component.

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
rtl	Synthesis model	■ DesignWare (P-2019.03 and later) ■ DesignWare-LP[a] (before P-2019.03)

a. For Design Compiler versions before P-2019.03, see "Enabling minPower" on page 9.

Table 1-4 Simulation Models

Model	Function
DW03.DW_LP_PIPED_fp_sum3_CFG_SIM	Design unit name for VHDL simulation
dw/dw03/src/DW_lp_piped_fp_sum3_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW_lp_piped_fp_sum3.v	Verilog simulation model source code

Functional Description

Block Diagram

Figure 1-1 shows the DW_lp_piped_fp_sum3 component with no pipeline management (*no_pm* = 1).

Figure 1-1 DW_lp_piped_fp_sum3 Block Diagram (*no_pm* = 1)

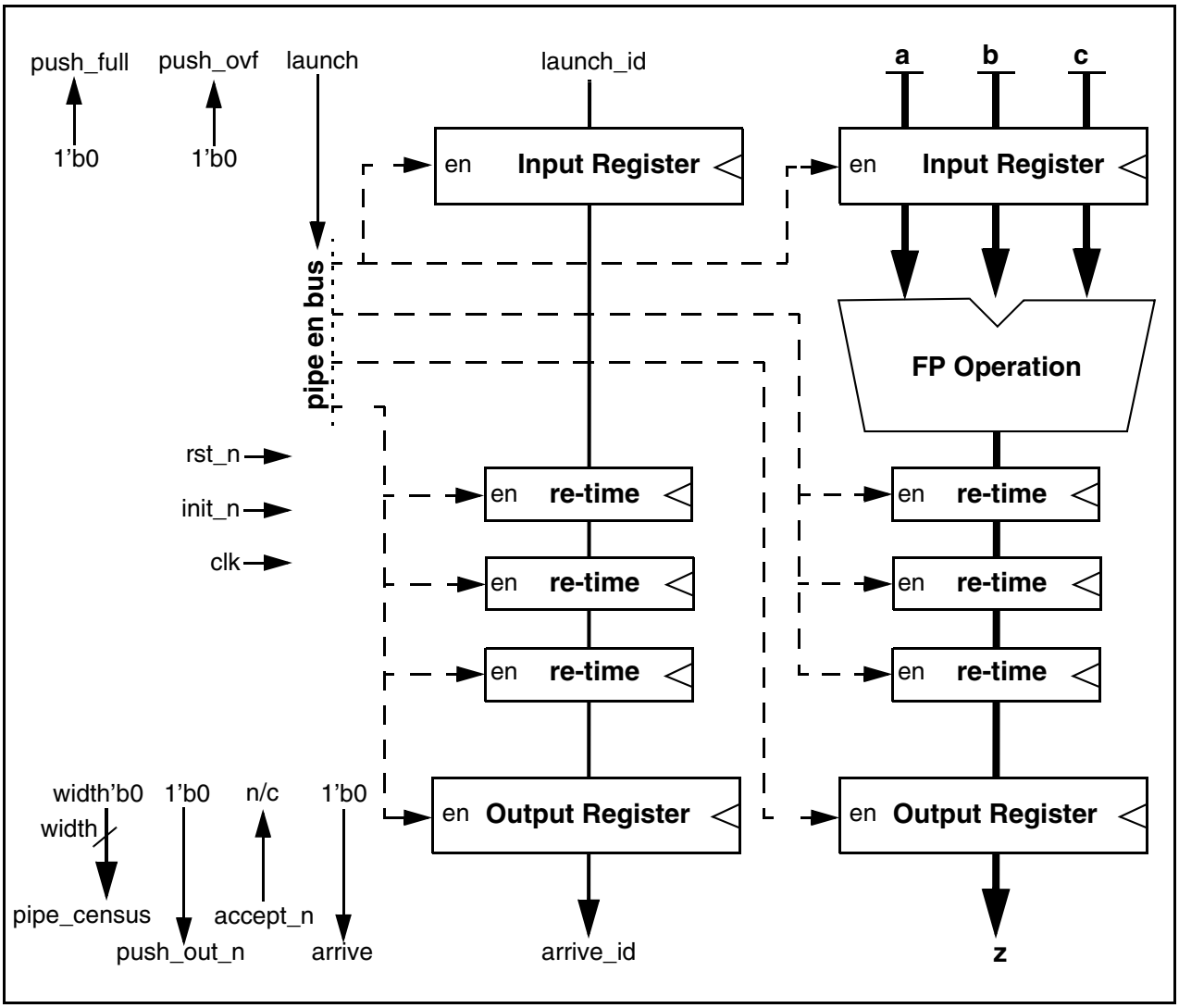
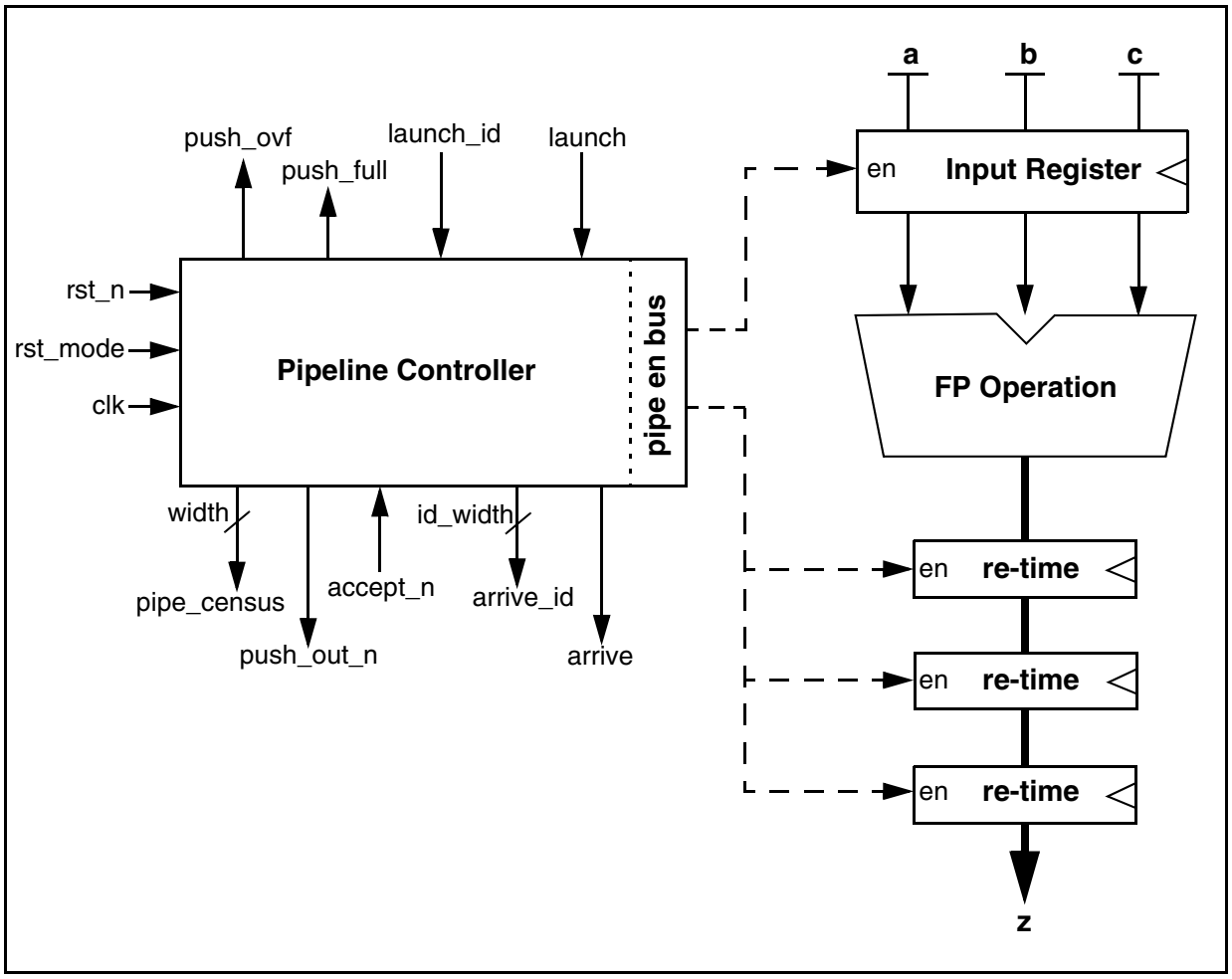


Figure 1-2 shows the DW_lp_piped_fp_sum3 component with pipeline management enabled (*no_pm* = 0):

Figure 1-2 DW_lp_piped_fp_sum3 Block Diagram (*no_pm* = 0)



When no pipeline manager is implemented (*no_pm* = 1), the outputs are purely pipelined results initiated by `a`, `b` and `c` when `launch` = 1. The pipeline is disabled (stalls) when `launch` = 0. Parameters *in_reg*, *stages*, and *out_reg* define the number of register levels as shown below in Table 1-5. To assist in tracking each set of `a`, `b` and `c` addition operations, transaction identifiers can be driven into `launch_id` and monitored on the pipelined output `arrive_id` to locate the associated results. That is, a unique `launch_id` value per `a`, `b`, `c` and `rnd` will make its way through the pipeline and show up at `arrive_d` along with its corresponding sum (`z`), and `status` results.

Table 1-5 Number of Pipeline Register Levels

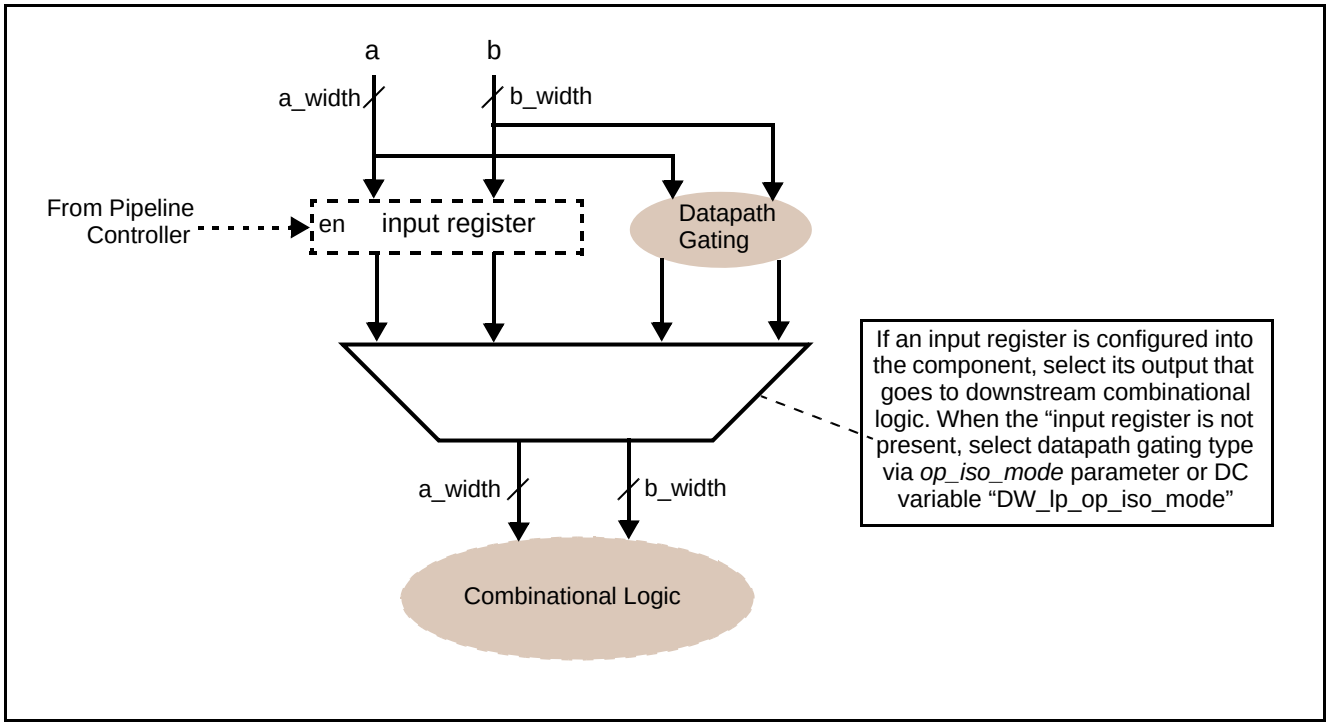
in_reg	*out_reg*	Number of Pipeline Register Levels
0	0	*stages* - 1
0	1	stages
1	0	stages

Table 1-5 Number of Pipeline Register Levels (Continued)

in_reg	*out_reg*	Number of Pipeline Register Levels
1	1	*stages* + 1

Figure 1-3 shows where datapath gating is inserted when the *op_iso_mode* parameter enables it.

Figure 1-3 Location of Datapath Gating (If Inserted)



Pipelining

The DW_lp_piped_fp_sum3 is configurable embed pipeline register levels. Setting the value for the parameters *in_reg*, *stages*, and *out_reg* (see Table 1-5 on page 6) determines the number of pipeline register level(s) that are inserted. Therefore, depending on the parameter *in_reg*, *stages*, and *out_reg* settings, the number of clock cycles for the sum (`z`) and `status` results to propagate out varies.

This DW_lp_piped_fp_sum3 is designed to make it easy to pipeline floating point addition logic using the register retiming features of Design Compiler (DC). It also contains parameter controlled input and output registers which will stay in place at their respective block boundary, that is, they are not allowed to be moved by DC register retiming features. The input and output registers are not available when using DC versions earlier than C-2009.06.

The parameter *stages* refers to the number of logic stages desired after register retiming is performed. The number of register levels is not necessarily the same as the number of logic stages. If no input or output registers are used (*in_reg* = 0 or *out_reg* = 0), then there is one fewer register level than logic stages. If either an input register or output register is specified, then the number of register levels is the same as the number of logic stages. If both input and output registers are specified, then the number of register levels is the

number of logic *stages* + 1. Refer to Table 1-5 on page 6 for a description. The number of pipeline register levels that can be retimed is always *stages* - 1.

Pipeline Control and Power Savings

When pipeline management is enabled (*no_pm* = 0), running in parallel to the pipeline register levels is pipeline control logic (as seen in Figure 1-2 on page 6) that monitors the activity. In cases where there is inactivity on a particular register level of the pipeline, the pipeline control disables those levels to promote power savings. Furthermore, if using the Synopsys Power Compiler tool, the presence of the pipeline control and its wiring to the pipeline register levels provides an opportunity for increased power reduction in the form of clock gating.

Along with the potential power savings that the pipeline control provides, it can be utilized to improve performance in cases where intermittent launch operations are present and there contains first-in first-out (FIFO) structures upstream and downstream of the DW_lp_piped_fp_sum3. The handshake is made between the DW_lp_piped_fp_sum3 and the external FIFOs via the `accept_n` and `pipe_full` ports. Effectively, the DW_lp_piped_fp_sum3 can be considered part of the external FIFO structures. The performance gain comes when inactive (bubbles) stages are detected. These pipeline 'bubbles' are removed to produce a contiguous set of active pipeline stages. The result is empty pipeline slots at the head of (or entering) the DW_lp_piped_fp_sum3 pipeline for new operations to be launched. Advancing the shifting of operations through the pipeline when a valid product result is available (`arrive` = 1) is controlled by the `accept_n` input. When the multiplier pipeline is full of active entries, the `pipe_full` output is 1. To disable this feature in cases where no external FIFOs are present, set the `accept_n` input to 0 which will effectively eliminate any flow control. At the same time, the `pipe_full` output would always be 0.

To assist in tracking of 'launched' operands, the pipeline control logic provides interface ports called `launch_id` and `arrive_id`. The `launch_id` input is assigned a value during an active launch operation. Given that `launch_id` values are unique in successive launch operations, the product results can be distinguished from one another with the assertion of arrive and the associated `arrive_id`. The `arrive_id` is the `launch_id` from the originating `launch` that produced the valid product result.

When *no_pm* = 1 the pipeline manager is not used, and the `launch` input is connected directly to the enable line of the pipeline registers. The pipeline stalls when `launch` = 0.

No Pipeline Register Levels Specified

In cases where no pipelining is required (*no_pm* = 1) through the DW_lp_piped_fp_sum3 (*in_reg* = 0, *stages* = 1, and *out_reg* = 0), the pipeline control flow control handshaking/status signals still remain active and meaningful with one exception. The `pipe_census`, which is intended to count the number of active pipeline register levels, becomes irrelevant and is fixed to 0.

Reset

System Resets (synchronous or asynchronous)

Two system reset modes are available from the `rst_n` input: asynchronous or synchronous. Asynchronous system reset is implemented when *rst_mode* is 0 and synchronous system reset is applied when *rst_mode* is 1.

During reset conditions, all the output ports are set to '0'.

Suppressing Warning Messages During Verilog Simulation

The Verilog simulation model includes macros that allow you to suppress warning messages during simulation.

To suppress all warning messages for all DWBB components, define the DW_SUPPRESS_WARN macro in either of the following ways:

- Specify the Verilog preprocessing macro in Verilog code:

  ```
  `define DW_SUPPRESS_WARN
  ```

- Or, include a command line option to the simulator, such as:

  `+define+DW_SUPPRESS_WARN` (which is used for the Synopsys VCS simulator)

The warning messages for this model include the following:

- If values other than 1 or 0 are present on a clock port, the following message is displayed:

  ```
  WARNING: <instance_path>.<clock_name>_monitor:
      at time = <timestamp>, Detected unknown value, x, on <clock_name> input.
  ```

  To suppress only this warning message for all DWBB components, use the following macro:

  - Define the DW_DISABLE_CLK_MONITOR macro. You can define this macro in the following ways:
    - Specify the Verilog preprocessing macro in Verilog code:

      ```
      `define DW_DISABLE_CLK_MONITOR
      ```

    - Or, include a command line option to the simulator, such as:

      `+define+DW_DISABLE_CLK_MONITOR` (which is used for the Synopsys VCS simulator)

  This message is also suppressed using the DW_SUPPRESS_WARN macro explained earlier.

- If an invalid rounding mode has been detected on `rnd`, the following message is displayed:

  ```
  WARNING: <instance_path>:
      at time = <timestamp>: Illegal rounding mode.
  ```

  To suppress this message, use the DW_SUPPRESS_WARN macro explained earlier.

Enabling minPower

In Design Compiler (version P-2019.03 and later) and Fusion Compiler, you can instantiate this component and use all its features without special settings.

For versions of Design Compiler before P-2019.03, enable minPower as follows:

```
set synthetic_library {dw_foundation.sldb dw_minpower.sldb}
set link_library {* $target_library $synthetic_library}
```

Related Topics

- Datapath Floating-Point Overview
- DesignWare Building Blocks User Guide

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_Foundation_comp.all;

entity DW_lp_piped_fp_sum3_inst is
      generic (
        inst_sig_width : POSITIVE := 23;
        inst_exp_width : POSITIVE := 8;
        inst_ieee_compliance : INTEGER := 0;
        inst_arch_type : INTEGER := 0;
        inst_op_iso_mode : NATURAL := 0;
        inst_id_width : POSITIVE := 8;
        inst_in_reg : NATURAL := 0;
        inst_stages : POSITIVE := 4;
        inst_out_reg : NATURAL := 0;
        inst_no_pm : NATURAL := 1;
        inst_rst_mode : NATURAL := 0
        );
      port (
        inst_clk : in std_logic;
        inst_rst_n : in std_logic;
        inst_a : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
        inst_b : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
        inst_c : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
        inst_rnd : in std_logic_vector(2 downto 0);
        z_inst : out std_logic_vector(inst_sig_width+inst_exp_width downto 0);
        status_inst : out std_logic_vector(7 downto 0);
        inst_launch : in std_logic;
        inst_launch_id : in std_logic_vector(inst_id_width-1 downto 0);
        pipe_full_inst : out std_logic;
        pipe_ovf_inst : out std_logic;
        inst_accept_n : in std_logic;
        arrive_inst : out std_logic;
        arrive_id_inst : out std_logic_vector(inst_id_width-1 downto 0);
        push_out_n_inst : out std_logic;
        pipe_census_inst : out
std_logic_vector(bit_width(maximum(1,inst_in_reg+(inst_stages-1)+inst_out_reg)+1)-1
downto 0)
        );
    end DW_lp_piped_fp_sum3_inst;


architecture inst of DW_lp_piped_fp_sum3_inst is

begin
```

```
    -- Instance of DW_lp_piped_fp_sum3
    U1 : DW_lp_piped_fp_sum3
    generic map ( sig_width => inst_sig_width, exp_width => inst_exp_width,
ieee_compliance => inst_ieee_compliance, arch_type => inst_arch_type, op_iso_mode =>
inst_op_iso_mode, id_width => inst_id_width, in_reg => inst_in_reg, stages =>
inst_stages, out_reg => inst_out_reg, no_pm => inst_no_pm, rst_mode => inst_rst_mode )
    port map ( clk => inst_clk, rst_n => inst_rst_n, a => inst_a, b => inst_b, c =>
inst_c, rnd => inst_rnd, z => z_inst, status => status_inst, launch => inst_launch,
launch_id => inst_launch_id, pipe_full => pipe_full_inst, pipe_ovf => pipe_ovf_inst,
accept_n => inst_accept_n, arrive => arrive_inst, arrive_id => arrive_id_inst,
push_out_n => push_out_n_inst, pipe_census => pipe_census_inst );


end inst;
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_lp_piped_fp_sum3_inst( inst_clk, inst_rst_n, inst_a, inst_b, inst_c,
          inst_rnd, z_inst, status_inst, inst_launch, inst_launch_id,
          pipe_full_inst, pipe_ovf_inst, inst_accept_n, arrive_inst, arrive_id_inst,
          push_out_n_inst, pipe_census_inst );

parameter sig_width = 23;
parameter exp_width = 8;
parameter ieee_compliance = 0;
parameter arch_type = 0;
parameter op_iso_mode = 0;
parameter id_width = 8;
parameter in_reg = 0;
parameter stages = 4;
parameter out_reg = 0;
parameter no_pm = 1;
parameter rst_mode = 0;


`define bit_width_MX_1__in_reg_P_stages_M_1_P_out_reg_P_1 2

input inst_clk;
input inst_rst_n;
input [sig_width+exp_width : 0] inst_a;
input [sig_width+exp_width : 0] inst_b;
input [sig_width+exp_width : 0] inst_c;
input [2 : 0] inst_rnd;
output [sig_width+exp_width : 0] z_inst;
output [7 : 0] status_inst;
input inst_launch;
input [id_width-1 : 0] inst_launch_id;
output pipe_full_inst;
output pipe_ovf_inst;
input inst_accept_n;
output arrive_inst;
output [id_width-1 : 0] arrive_id_inst;
output push_out_n_inst;
output [(`bit_width_MX_1__in_reg_P_stages_M_1_P_out_reg_P_1)-1 : 0] pipe_census_inst;

    // Instance of DW_lp_piped_fp_sum3
    DW_lp_piped_fp_sum3 #(sig_width, exp_width, ieee_compliance, arch_type,
op_iso_mode, id_width, in_reg, stages, out_reg, no_pm, rst_mode)
      U1 ( .clk(inst_clk), .rst_n(inst_rst_n), .a(inst_a), .b(inst_b), .c(inst_c),
.rnd(inst_rnd), .z(z_inst), .status(status_inst), .launch(inst_launch),
.launch_id(inst_launch_id), .pipe_full(pipe_full_inst), .pipe_ovf(pipe_ovf_inst),
.accept_n(inst_accept_n), .arrive(arrive_inst), .arrive_id(arrive_id_inst),
.push_out_n(push_out_n_inst), .pipe_census(pipe_census_inst) );
```

```
endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
July 2023	DWBB_202212.5	■ Updated version and date
September 2021	DWBB_202106.2	■ Adjusted the position of the *id_width* parameter in Table 1-2 on page 2 to match parameter order in RTL
July 2020	DWBB_201912.5	■ Adjusted the description of the *ieee_compliance* parameter in Table 1-2 on page 2 ■ Adjusted content and title of "Suppressing Warning Messages During Verilog Simulation" on page 9 and added the DW_SUPPRESS_WARN macro and the illegal round mode message
October 2019	DWBB_201903.5	■ Added "Disabling Clock Monitor Messages"
March 2019	DWBB_201903.0	■ Clarified the op_iso_mode parameter in Table 1-2 on page 2 ■ Clarified licensing requirements in Table 1-3 on page 4 ■ Clarified the figure titles for Figure 1-1 on page 5 and Figure 1-2 on page 6 ■ Added Figure 1-3 on page 7 to clarify datapath gating ■ Added "Enabling minPower" on page 9 ■ Added this Revision History table and the document links on this page

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