IC Compiler
Quick Reference

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Contents

Getting Help

IC Compiler provides various forms of online help.

- The help command provides you with quick help for one or more commands or procedures.
- The man command displays the man page.

You can use a wildcard pattern as the argument for the help command. The wildcard characters are

* Matches n characters.

? Matches exactly one character.

Accessing Brief Help

Use this command to list all commands by function group:

```
icc_shell> help
```

Use this command to display all commands that end with the word clock:

```
icc_shell> help *clock
```

Use this command to get syntax help for one or more commands:

```
icc_shell> help -verbose cmd_name_pattern
```

Use this command to get syntax help for a specific command:

```
icc_shell> command_name -help
```

Man Page Viewing Instructions

The following sections describe how to set up your environment and the syntax to use to view man pages.

Viewing Man Pages in SolvNet

You can view the man pages in HTML or PDF format in SolvNet. To view the man pages in SolvNet, go to

https://solvnet.synopsys.com/DocsOnWeb

and click Man Pages near the bottom of the page.

Setting Up the UNIX Environment

Edit your .cshrc file to contain these lines:

```
setenv ICC_MAN_DIR synopsys_root/doc/icc/man
setenv MANPATH ${MANPATH}:${ICC_MAN_DIR}
```

ICC_MAN_DIR is a variable that contains the path to the man page directories, and *synopsys_root* represents the specific path to the Synopsys software directory at your site.

Viewing Man Pages From UNIX

Command

```
% man command_name
```

Variable

```
% man variable_name
```

Error, warning, or information message

```
% man message_id
```

Viewing Man Pages From icc_shell

Command

```
icc_shell> man command_name
```

Variable

```
icc_shell> man variable_name
```

Error, warning, or information message

```
icc_shell> man message_id
```

User Commands

Invoke user commands from a UNIX shell.

icc_shell

Invokes the IC Compiler command shell.

```
icc_shell
[-gui [-display terminal_name]]
[-non_upf_mode]
[-xp_mode]
[-psyn_mode]
[-dp_mode]
[-f script_file]
[-x command_string]
[-no_init]
[-checkout feature_list]
[-64bit]
[-wait wait_time]
[-timeout timeout_value]
[-version]
[-no_log]
```

IC Compiler Commands

Invoke these commands from within the IC Compiler tool.

add_clock_drivers

Adds multiple levels of drivers into your design and connects them together. These drivers are suitable for driving a clock mesh.

```
status add_clock_drivers
-load net_or_pins -prefix prefix_string
 | -remove_display
[-configuration list_of_groups
 | -external_configuration config_file]
[-driver_type library_cell]
[-avoid cells]
[-max_displacement {x_distance y_distance}]
[-offset {x_distance y_distance}]
[-use_common_bbox]
[-check_only]
[-verbose]
```

add_distributed_hosts

Adds one or more distributed hosts for distributed jobs.

```
status add_distributed_hosts
[-target PrimeTime | StarRCXT | all]
[-32bit]
[-enable_ssh]
-farm lsf | grd | generic | now
[-setup_path setup_path]
[-num_of_hosts count]
[-options string]
[-submission_script submission_script]
[work_station_name]
```

add_drc_error_detail

Add shapes to an existing error object with additional details.

```
status add_drc_error_detail
-drc_error drc_error
-rectangles rectangles
[-net net]
[-layer layer]
[-error_view mw_error_view]
```

add_end_cap

Adds end cap cells at both ends of a cell row.

Equivalent Scheme command: `axAddEndCap`

```
status add_end_cap
[-mode both | bottom_left | upper_right]
[-mirror]
[-respect_padding]
[-respect_blockage]
-lib_cell lib_cell_name
[-vertical_cells lib_cell_names
[-fill_corner]]
[-respect_keepout]
```

add_open_drc_error_detail

Add shapes to an existing error object of a type in the Open type class with additional details.

```
status add_open_drc_error_detail
-drc_error drc_error
-node node_number
-rectangles rectangles
[-layer layer]
[-error_view mw_error_view]
```

add_pg_pin_to_db

Converts rail or non-pg_pin based logic library (db) into pg_pin based logic library.

```
status add_pg_pin_to_db
input_db_filename
[-mw_library_name mw_lib_name]
[-pg_map_file pg.map]
-output pg_db_filename
[-verbose]
[-pg_map_template
pg_pin_map_template_filename]
[-expanded]
```

add_pg_pin_to_lib

converts rail or non-pg_pin based logic library (.lib) into pg_pin based logic library (.lib).

```
status add_pg_pin_to_lib
input_lib_filename
[-mw_library_name mw_lib_name]
[-pg_map_file pg.map]
[-pg_map_template template_filename]
[-expanded]
-output pg_lib_filename
[-common_shell_path common_shell_path]
[-verbose]
```

add_port_state

Adds state information to a supply port.

```
string add_port_state
supply_port_name
-state {name nom | min nom max | off}
```

add_pst_state

Defines the states of each of the supply nets for one possible state of the design.

```
status add_pst_state
state_name
-pst table_name
-state supply_states
```

add_row

Creates a list of rows in the design.

Equivalent Scheme command: `axgAddRow`

```
status add_row
[-in base_array_name]
[-tile_pattern tile_pattern_name]
[-tile_name tile_name]
-area {{ll_x_ll_y}_{ur_x_ur_y}}
[-minimal_channel_height channel_height]
[-direction direction]
[-flip_first_row] | [-no_double_back]
[-no_start_from_first_row]
[-no_snap_to_wire_track]
[-dont_snap_to_existing_row]
[-no_double_back]
```

add_tap_cell_array

Adds tap cells to the design, forming a two-dimensional array structure.

Equivalent Scheme command:

```
axgArrayTapCell
```

```
integer add_tap_cell_array
[-master_cell_name ]
[-voltage_area {voltage_areas_collection}]
[-distance tap_cell_distance]
[-pattern normal | every_other_row |
stagger_every_other_row]
[-offset distance]
[-tap_cell_identifier tap_cell_prefix]
[-tap_cell_separator tap_cell_separator]
[-no_tap_cell_under_layers layer_list]
[-well_port_name port_name]
[-well_net_name net_name]
[-substrate_port_name port_name]
[-substrate_net_name substrate_tie_net_name]
[-connect_power_name power_net_name]
[-connect_ground_name ground_net_name]
[-fill_boundary_row true | false]
[-fill_macro_blockage_row true | false]
[-boundary_row_double_density true | false]
[-macro_blockage_row_double_density true |
false]
[-left_macro_blockage_extra_tap by_rule |
must_insert | no_insert]
[-right_macro_blockage_extra_tap by_rule |
must_insert | no_insert]
[-left_boundary_extra_tap by_rule |
must_insert | no_insert]
[-right_boundary_extra_tap by_rule |
must_insert | no_insert]
[-ignore_soft_blockage true | false]
[-at_distance_only true | false]
[-skip_fixed_cells true | false]
[-respect_keepout]
```

add_to_collection

Adds objects to a collection, resulting in a new collection. The base collection remains unchanged.

```
collection add_to_collection
base_collection
object_spec
[-unique]
```

add_to_rp_group

Adds a cell, hierarchical group, or keepout to an existing relative placement group.

Leaf Cells:

```
status add_to_rp_group
rp_groups
-leaf cell_name
[-column integer]
[-row integer]
[-pin_align_name pin_name]
[-orientation direction]
[-alignment bottom-left | bottom-right]
```

Hierarchical Groups:

```
status add_to_rp_group
rp_groups
-hierarchy group_name
[-instance instance_name]
[-column integer]
[-row integer]
[-alignment bottom-left | bottom-right]
```

Keepouts:

```
status add_to_rp_group
rp_groups
-keepout keepout_name
[-column integer]
[-row integer]
[-width integer]
[-height integer]
[-type hard | soft | space]
```

adjust_fp_floorplan

Adjusts an existing floorplan.

Equivalent Scheme command:

`axAdjustFloorPlan`

```
status adjust_fp_floorplan
[-core_aspect_ratio real]
[-core_utilization real]
[-core_width real]
[-core_height real]
[-number_rows int]
[-die_width real]
[-die_height real]
[-use_vertical_row sbool]
[-no_double_back sbool]
[-start_first_row sbool]
[-flip_first_row sbool]
[-row_core_ratio real]
[-left_io2core real]
[-right_io2core real]
[-bottom_io2core real]
[-top_io2core real]
[-min_pad_height sbool]
[-maintain_placement]
[-remove_filler_io]
[-die_origin point]
[-sm_utilization string_list]
[{-fc_periphery string | -fc_in_core
string}]
```

adjust_fp_io_placement

Adjusts I/O pad placement.

Equivalent Scheme command:

`fphAdjustIOPlacement`

```
int adjust_fp_io_placement
[-side l | r | t | b]
[-spacing float]
[-pitch float]
[-offset float]
[-undo]
[list of IO cells]
```

adjust_premesh_connection

Connects the load pins in the specified clock tree or subtree either as mesh loads or as part of the premesh tree. If you specify the -premesh option, it balances the first-level loads of the premesh tree.

```
status adjust_premesh_connection
-root root_name
[-premesh | -exclude_pins list_of_pins]
[-operating_condition min | max | min_max]
```

alias

Creates a pseudo-command which expands to one or more words, or lists current alias definitions.

```
string alias
[name] [def]
```

align_fp_pins

Physically aligns a set of soft macros (or black box) pins with a set of reference pin objects. These can be terminals or pins on hard macros, IO pad cells, standard cells, internal child hard macros, or another soft macro (or black box).

Equivalent Scheme commands:

```
fphAlignHMPin, fphAlignSMPin
```

```
status align_fp_pins
[-reference object]
[-direction {left | right | top | bottom}]
[-fixed]
[-change_layer_width]
[-order_type {low_to_high | high_to_low |
net_connection}]
[-align_with_child_hm_pins]
objects
```

align_objects

Aligns one or more objects.

```
status align_objects
[{-anchor object | -parent |
-to value_point_rect}]
[-side alignment_side]
[-offset float]
[-resize]
[-keep_area]
[-ignore_fixed]
objects
```

all_active_scenarios

Lists the active scenarios available in memory.

```
string all_active_scenarios
```

all_ao_cells

Returns a collection of always-on cells available in the design.

```
collection all_ao_cells
```

all_bounds_of_cell

Returns the collection of all bounds in the specified list of cells from the design.

```
collection all_bounds_of_cell
cell_list
```

all_cells_in_bound

Returns the collection of all cells in the specified list of group bounds and move bounds from the design.

```
collection all_cells_in_bound
{bound_list}
```

all_clocks

Returns a collection of all clocks in the current design.

```
collection all_clocks
```

all_connected

Returns the objects connected to a net, port, pin, net instance, or pin instance.

Equivalent Scheme command:
`dbGetConnectedObject`

```
collection all_connected
[-leaf] object
```

all_connectivity_fanin

Reports pins, ports, or cells in the fanin of specified sinks.

```
list all_connectivity_fanin
-to sink_list
[-startpoints_only]
[-only_cells]
[-flat]
[-levels count]
```

all_connectivity_fanout

Returns a set of pins, ports, or cells in the fanout of the specified sources.

```
list all_connectivity_fanout
-from source_list
[-endpoints_only]
[-only_cells]
[-flat]
[-levels count]
```

all_critical_cells

Returns a collection of critical leaf cells in the top hierarchy of the current design.

```
collection all_critical_cells
[-slack_range range_value]
```

all_critical_pins

Returns a collection of critical endpoints or startpoints in the current design.

```
collection all_critical_pins
[-type endpoint | startpoint]
[-slack_range range_value]
```

all_designs

Returns a collection containing all designs in the current design.

```
collection all_designs
```

all_dont_touch

Returns a collection of dont_touch cells or nets from the current design or from the specified input collection.

```
collection all_dont_touch
-cells | -nets
[input_coll]
```

all_drc_violated_nets

Returns a collection of DRC-violated nets from the current design or from the specified input collection.

```
collection all_drc_violated_nets
-max_capacitance | -max_transition |
-max_fanout
[input_coll]
[-bound upper]
[-threshold threshold]
```

all_fanin

Reports pins, ports, or cells in the fanin of specified sinks.

```
collection all_fanin
-to sink_list
[-startpoints_only]
[-exclude_bboxes]
[-break_on_bboxes]
[-only_cells]
[-flat]
[-levels count]
```

all_fanout

Returns a set of pins, ports, or cells in the fanout of the specified sources.

```
collection all_fanout
-clock_tree
-from source_list
[-endpoints_only]
[-exclude_bboxes]
[-break_on_bboxes]
[-only_cells]
[-flat]
[-levels count]
```

all_fixed_placement

Returns the collection of all fixed-placement cells or ports in the design or from a list of objects in the input collection.

```
collection all_fixed_placement
-cells | -ports
[input_coll]
```

all_high_fanout

Returns a collection of high-fanout nets from the current design or from the specified input collection.

```
collection all_high_fanout
-nets
[-threshold value]
[input_coll]
[-through_buf_inv]
```

all_ideal_nets

Returns a collection of ideal nets from the current design or from the specified input collection.

```
collection all_ideal_nets
[input_coll]
```

all_inputs

Returns a collection of input or inout ports in the current design.

```
collection all_inputs
[-clock clock_name]
[-edge_triggered | -level_sensitive]
```

all_isolation_cells

Returns a collection of isolation cells available in the design.

```
collection all_isolation_cells
```

all_level_shifters

Returns a collection of level-shifter cells available in the design.

```
collection all_level_shifters
[-type els | simple]
```

all_macro_cells

Returns a collection of all macro cells in the design or from a list of objects in the input collection.

```
collection all_macro_cells
[input_coll]
```

all_mtcmos_cells

Returns a collection of MTCMOS cells available in the design.

```
collection all_mtcmos_cells
[-type coarse | fine]
```

all_objects_in_bounding_box

Returns the collection of all cells and/or nets in the specified bounding box in the design or from a list of objects in the input collection.

```
collection all_objects_in_bounding_box
-cells | -nets
[-phys_cells]
-coordinates {llx lly urx ury}
[-flat]
[input_coll]
```

all_outputs

Returns a collection of output or inout ports in the current design.

```
collection all_outputs
[-clock clock_name]
[-edge_triggered | -level_sensitive]
```

all_physical_only_cells

Returns a collection of all physical-only (filler) cells in the design or from a list of objects in the input collection.

```
collection all_physical_only_cells
[-lib_cells lib_list | -cell_name list]
[-coordinates {llx lly urx ury}]
[input_coll_handle]
```

all_physical_only_nets

Returns a collection of all physical-only nets in the design or from a list of objects in the input collection.

```
collection all_physical_only_nets
[input_coll]
```

all_physical_only_ports

Returns a collection of all physical-only ports in the design or from a list of objects in the input collection.

```
collection all_physical_only_ports
[input_coll]
```

all_registers

Returns a collection of sequential cells or pins in the current design.

```
collection all_registers
[-no_hierarchy]
[-clock clock_name]
[-rise_clock rise_clock_name]
[-fall_clock fall_clock_name]
[-cells]
[-data_pins]
[-clock_pins]
[-slave_clock_pins]
[-output_pins]
[-inverted_output]
[-level_sensitive | -edge_triggered]
[-master_slave]
```

all_rp_groups

Returns a collection of specified relative placement groups and all groups in their hierarchy.

```
collection all_rp_groups
[rp_groups]
```

all_rp_hierarchicals

Returns a collection of hierarchical relative placement groups that contain specified groups in their hierarchy. The specified groups can be either included or instantiated in their parent group.

```
collection all_rp_hierarchicals
[rp_groups]
```

all_rp_inclusions

Returns a collection containing of hierarchical relative placement groups that include the specified groups.

```
collection all_rp_inclusions
[rp_groups]
```

all_rp_instantiations

Returns a collection of hierarchical relative placement groups that instantiate specified groups.

```
collection all_rp_instantiations
[rp_groups]
```

all_rp_references

Returns a collection of relative placement groups that directly contain the specified cells, which are either leaf cells or hierarchical cells that contain instantiated relative placement groups.

```
collection all_rp_references
[cell_list]
[-design design_name]
```

all_scenarios

Lists all defined scenarios available in memory.

```
string all_scenarios
```

all_size_only_cells

Returns the collection of cells that have been specified size_only attribute on them.

```
collection all_size_only_cells
cell_list
```

all_spare_cells

Returns a collection of all spare cells in the design or from a list of objects in the input collection.

```
collection all_spare_cells
[input_coll]
```

all_threestate

Returns a collection of threestate cells or nets.

```
collection all_threestate
-nets
[input_coll]
```

all_tieoff_cells

Returns a collection of all tie-off cells in the current design or in the input collection.

```
collection all_tieoff_cells
```

allocate_fp_budgets

Performs proportional timing budgeting.

Equivalent Scheme command:
`fphTimingBudgeting`

```
allocate_fp_budgets
[-black_box_cells bb_cells_list]
[-fixed_delay_objects objects]
[-file_format_spec file_format_string]
[-no_interblock_logic]
[-cells budget_cell_names]
[-incremental]
[-advanced]
[-no_split]
[-create_qtm_models [-qtm_model_path
output_directory]]
```

analyze_fp_rail

Analyzes a complete or partial power network for voltage (IR) drop and electromigration (EM) on the specified power and ground nets.

Equivalent Scheme command: `fphAnalyzeRail`

```
status analyze_fp_rail
-nets nets
[-power_budget power]
[-analyze_power]
[-voltage_supply voltage]
[-pad_masters pad_masters]
[-read_pad_instance_file file_name]
[-read_pad_master_file file_name]
[-use_pins_as_pads]
[-top_level_only]
[-create_virtual_rails layer]
[-ignore_blockages]
[-ignore_conn_view_layers layer]
[-read_power_compiler_file file_name]
[-read_prime_power_file file_name]
[-read_default_power_file file_name]
[-output_directory directory_name]
```

analyze_fp_routing

Analyzes the existing global routing to determine where nets cross plan groups or voltage areas boundaries. Creates feedthroughs on plan groups or on hierarchical modules that belong to voltage areas. In the case of plan groups, records the location, level, and direction of the pins (including feedthrough pins) that are implied by the routing.

Equivalent Scheme command:

```
fphAnalyzeRouting
```

```
int analyze_fp_routing
[-output_feedthrough_nets {plan_groups |
voltage_areas}
[-finalize_pins_feedthroughs {plan_groups |
voltage_areas}]
[-include_flip_chip_style_connections]
```

analyze_rail

Performs the targeted rail analyses on the specified nets. This command generates data needed to run PrimeRail and constructs a script that runs PrimeRail within the IC Compiler session. This command enables three target analyses: power and ground network integrity analysis, voltage drop analysis, and electromigration analysis. A previously generated PrimeRail command script can also be used to drive the rail analysis.

```
status analyze_rail
nets
[-integrity]
[-voltage_drop]
[-electromigration]
[-primerail_script_file pr_script]
[-script_only]
```

analyze_subcircuit

Invokes circuit simulation on a subcircuit of the current design. This command is suitable for analyzing clock meshes.

```
status analyze_subcircuit
[-name string]
[-to net_or_pins]
[-analysis_mode max | min | max_then_min]
[-effort low | medium | high]
[-simulator name_of_simulator]
[-spice_header_files list_of_files]
[-driver_subckt_files list_of_files]
[-starrcxt_map_file file_name]
[-configuration
list_of_scenario_configurations]
[-output_directory directory]
[-input_rise_transition transition_time]
[-input_fall_transition transition_time]
[-period pulse_duration]
[-clock clock_name]
[-no_extraction]
[-from pins]
[-tie_high pins_or_nets]
[-tie_low pins_or_nets]
[-zero_resistance nets]
[-reset_annotation]
[-purge_all_annotations]
[-projected_loads load_configuration]
[-projected_drivers driver_configuration]
[-projected_input_skew
input_skew_configuration]
[-probe_wires net]
[-verbose]
[-starrcxt_nxtgrd_file ]
```

append_to_collection

Adds objects to the collection in the specified variable. The variable is updated.

```
collection append_to_collection
var_name
object_spec
[-unique]
```

apropos

Searches the command database for a pattern.

```
string apropos
[-symbols_only]
pattern
```

archive_design

Archives the given design(s) to a new location.

```
status archive_design
-source library_path
-design design_names
-archive archive_directory
[-complete]
[-overwrite]
```

assign_flip_chip_nets

Creates or reconnects nets between flip chip drivers to bumps.

Equivalent Scheme command:

```
fcDriverBumpMatch
```

```
status assign_flip_chip_nets
[-personality_type personality_type_list]
[-prefix prefix]
[-uniquify num_to_uniquify]
[-eco]
```

balance_inter_clock_delay

Performs interclock delay balancing.

Equivalent Scheme command:

```
astCTOInterClocksBalance
```

```
status balance_inter_clock_delay
[-clock_trees list_of_clocks]
[-max_target_delay float_value]
[-operating_condition min | max | min_max]
```

break

Immediately exits a loop structure.

calculate_caa_based_yield2db

Calculate critical area analysis based yield and add it into db library.

```
status calculate_caa_based_yield2db
library_name/db_file_name
-particle_distr_func_file file_name]
[-data_kit_type tsmc | tsmc_encr]
[-layer_alias_dsd_format {x_y_z_r_t}]
[-output db_file_name]
```

cd

Changes the current directory.

```
int cd
[directory]
```

change_fp_soft_macro_to_black_box

Converts the specified soft macros to black boxes.

Equivalent Scheme command:

```
fphSoftMacroToBlackBox
```

```
status change_fp_soft_macro_to_black_box
black_boxes
```

change_link

Changes the design to which a cell is linked.

```
status change_link
object_list
design_name
[-all_instances]
```

change_macro_view

Changes the view of the macro that is used.

Equivalent Scheme command:

```
aprReplaceChildCell
```

```
status change_macro_view
-reference cell_reference_name
-view view_name
[-quiet]
```

change_names

Changes the names of ports, cells, and nets in a design.

```
integer change_names
[-rules name_rules]
[-hierarchy]
[-verbose]
[-names_file names_file]
[-log_changes log_file]
[-restore]
[-dont_touch object_list]
[-instance instance]
[-new_name new_name]
```

change_selection

Changes the selection in the GUI, taking a collection of objects and changing the selection according to the type of change specified.

Equivalent Scheme command: `geWindowSelect`

```
int change_selection
[-name slct_bus]
[-replace]
[-add]
[-remove]
[-toggle]
[-type object_type]
[-clock_trees clock_tree_list]
collection
```

change_selection_no_core

Indicates that objects had no core representation

```
change_selection_no_core -name Slct
[-add]
[-remove]
-type Type
-names NameList
```

change_selection_too_many_objects

Indicates that too many objects were involved in selection change

```
change_selection_too_many_objects -name Slct
[-add]
[-remove]
```

change_tie_connection

Changes tie connection of the specified signal pins and ports.

```
status change_tie_connection
[-net net]
-port port_list
-pin pin_list
```

characterize

Captures information about the environment of specific cell instances, and assigns the information as attributes on the design to which the cells are linked.

```
int characterize
cell_list
[-no_timing] [-constraints]
[-connections] [-power]
[-verbose]
```

check_clock_tree

Checks the clock trees of the current design for common problems that can adversely impact clock tree synthesis.

```
status check_clock_tree
[-clocks clock_list]
```

check_design

Checks the current design for consistency.

```
status check_design
[-summary]
[-no_warnings]
[-one_level]
[-multiple_designs]
[-no_connection_class]
[-post_layout | -only_post_layout]
```

check_error

Prints extended information on errors from last command.

```
int check_error
[-verbose] [-reset]
```

check_fp_budget_result

Performs post-budgeting timing analysis.

```
status check_fp_budget_result
[-blocks block]
[-pins pin]
-file_name output_design_report
```

check_fp_pin_alignment

Checks the soft macro pin alignment QoR.

Equivalent Scheme command:

```
fphCheckSMPinAlignment
```

```
status check_fp_pin_alignment
[-detour]
[-tolerance real]
[-report_nets]
[-nets collection]
```

check_fp_pin_assignment

Performs pin placement checks.

Equivalent Scheme command: `fphCheckSMPin`

```
status check_fp_pin_assignment
[-pin_spacing]
[-pin_preroute_spacing]
[-shorts]
[-no_stacking]
[-layers]
[-layers_pg]
[-wiretrack]
[-missing]
[-missing_pg]
[-single_pin]
[-off_edge]
[-outside_pin_guide]
[-block_level]
[-nets net_collection]
[objects]
```

check_fp_rail

Checks the integrity of the power network created by power network synthesis, early in the design planning stage.

```
status check_fp_rail
-nets nets
[-ring]
[-floating_segment]
[-power_switch_connection]
```

check_fp_timing_environment

Performs timing environment analysis.

Equivalent Scheme command:

```
fphCheckTimingEnvironment
```

```
integer check_fp_timing_environment
[-block_pin_stats]
[-unbudgetable_pins]
[-unconstrained_pins]
[-exception_pins]
[-static_logic_pins]
[-delay_violators percent]
[-num_pin_connections connections]
[-block_name string]
[-pin_name string]
[-zero_wire_delay slack_percent]
[-bottleneck slack_limit]
[-bottleneck_max_cell num_cells]
[-bottleneck_no_vipo]
[-vipo_timing slack_percent]
[-format_report]
```

check_isolation_cells

Reports the existing isolation cells in the current design. It also reports if any isolation cell is redundant or might be required.

```
status check_isolation_cells
[-input]
[-output]
[-inside]
[-outside]
[objects]
```

check_legality

Checks the legality of the current placement.

Equivalent Scheme commands:

`axgPlaceCheck, axgVAConsistencyCheck`

```
int check_legality
[-verbose]
```

check_level_shifters

Checks the design for all existing level shifters and nets against the specified level shifter strategy and threshold.

```
status check_level_shifters
[-verbose]
```

check_license

Checks the availability of a license for a feature.

```
status check_license
feature_list
```

check_mpc

Checks the result of the minimum physical constraints options on the design after running the design through the minimum physical constraints flow.

```
int check_mpc
[-macros]
[-ports]
[-conflicting]
[-verbose]
[object_list]
```

check_mv_design

Checks for violations in a multivoltage design.

```
status check_mv_design
[-verbose]
[-isolation]
[-target_library_subset]
[-opcond_mismatches]
[-connection_rules]
[-level_shifters]
[-power_nets]
[-max_messages message_count]
```

check_noise

Checks whether there are necessary data available to run noise analysis in the current design.

```
status check_noise
[-verbose]
[-nosplit]
[-include check_list]
```

check_physical_constraints

Checks the physical constraints and provides feedback about possible errors in input.

```
int check_physical_constraints
[-narrow_placement_area no_of_sites]
[-rc_check rc_variation_margin]
[-verbose]
[-analyze_legality [-nworst
no_of_worst_cells]
[-design]
[-lib_cell lib_cell_name]]
```

check_physical_design

Checks the readiness of the current design for IC Compiler.

```
status check_physical_design
-stage stage_value | -input_log log_file
[-output directory]
[-display]
```

check_route

Checks and reports the violations of a routed design.

```
status check_route
[-drc]
[-opens]
[-antenna]
[-top_layer_probe_constraints]
[-num_cpus num]
```

check_routeability

Verifies that the current design is routeable.

Equivalent Scheme commands:

`axgCheckDesignForRoute,`
`axgCheckWireTrack`

```
integer check_routeability
[-error_cell cell_name]
```

check_rp_groups

Checks the relative placement constraints and reports the failures.

```
collection check_rp_groups
{rp_groups | -all}
[-output filename]
[-verbose]
```

check_scan_chain

Allows scan chain structural consistency checking based on the scan chain information stored in the current design.

```
status check_scan_chain
[-chain_name name of the scan chain string]
```

check_target_library_subset

Checks and prints out the inconsistent settings among target library, target library subset, and operating conditions.

```
status check_target_library_subset
```

check_timing

Checks for possible timing problems in the current design.

Equivalent Scheme command:

```
astTimingDataCheck
```

```
status check_timing
[-overlap_tolerance minimum_distance]
[-override_defaults check_list]
[-multiple_clock]
[-retain]
[-include check_list]
[-exclude check_list]
```

check_tlu_plus_files

Checks the files used for TLUPlus extraction.

```
status check_tlu_plus_files
```

clock_opt

Performs clock tree synthesis, routing of clock nets, extraction, optimization, and hold-time violation fixing on the design. There is also an option to execute interclock delay balancing.

```
status clock_opt
[-only_psyn]
[-fix_hold_all_clocks]
[-inter_clock_balance]
[-update_clock_latency]
[-operating_condition min | max(default) |
min_max]
[-only_cts]
[-optimize_dft]
[-no_clock_route]
[-only_hold_time]
[-area_recovery]
[-size_only]
[-in_place_size_only]
[-power]
```

close_distributed_route

Closes all of the sockets and shuts down the daemons.

Equivalent Scheme command: `jpClose`

```
integer close_distributed_route
```

close_mw_cel

Closes the specified Milkyway designs.

Equivalent Scheme command: `geCloseCell`

```
status close_mw_cel
[-save]
[-all_views]
[-all_versions]
[mw_cel_list]
```

close_mw_lib

Closes the current Milkyway library.

Equivalent Scheme command: `geCloseLib`

```
status close_mw_lib
[-save]
```

commit_fp_group_block_ring

Commits the power ground group block ring and/or straps based on the results from the create_fp_group_block_ring command.

```
status commit_fp_group_block_ring
```

commit_fp_plan_groups

Transforms the specified plan groups into soft macros.

Equivalent Scheme command:
`fphCommitHierarchy`

```
status commit_fp_plan_groups
[-push_down_power_and_ground_straps]
[-new_top_cell new_cell_name]
[plan_groups]
```

commit_fp_rail

Commits the power network (power/ground wires and vias) based on power network synthesis (PNS) results.

Equivalent Scheme command: `fphCommitRail`

```
int commit_fp_rail
```

commit_skew_group

Checks the skew groups defined in the design for common problems that can adversely impact clock tree synthesis. If no problem is found, the command modifies clock tree structure to isolate skew groups.

```
status commit_skew_group
[-check_only]
```

compare_collections

Compares the contents of two collections. If the same objects are in both collections, the result is 0 (zero), like string compare. If they are different, the result is nonzero. The order of the objects can optionally be considered.

```
int compare_collections
[-order_dependent]
collection1
collection2
```

compare_delay_calculation

Compares the Arnoldi-based delays with the Elmore delays in the current design.

```
integer compare_delay_calculation
[-verbose]
[-ccs]
```

compare_interface_timing

Compares two write_interface_timing reports.

```
int compare_interface_timing
ref_timing_file
cmp_timing_file
[-output file_name]
[-absolute_tolerance atol_list]
[-nosplit]
[-significant_digit digits]
```

compare_lib

Performs a cross-reference check between a technology library and a symbol library or between a technology library and a physical library.

```
int compare_lib
library1
library2
```

compare_rc

Compares annotated capacitance with estimation capacitance.

```
int compare_rc
[-bound max_float_capacitance]
[-min]
[-net net_list]
[-threshold min_float_capacitance]
[-worst_nets integer_nets]
```

compile_clock_tree

Builds a clock tree based on the clock tree definition.

Equivalent Scheme command: `astCTS`

```
status compile_clock_tree
[-clock_trees name_or_source_pin_list]
[-config_file_read read_filename]
[-config_file_write write_filename]
[-operating_condition min | max | min_max]
[-high_fanout_net net_or_pin_list
[-sync_phase rise | fall | both]]
```

compile_fp_clock_plan

Compiles clock trees inside a plan group and builds clock trees at the top level according to the plan group's result.

Equivalent Scheme commands:
`fphAddAnchors, fphTcp`

```
status compile_fp_clock_plan
[-operation_cond min | max(default) |
min_max]
[-anchor_only]
[-parallel]
```

compile_premesh_tree

Invokes clock tree synthesis on a net that is driving a clock mesh.

```
status compile_premesh_tree
-clock_tree name_or_root_pin
```

compute_polygons

Returns a list of polygons that cover the areas according to the Boolean operation type.

```
list compute_polygons
-boolean type
polygon1
polygon2
```

connect_net

Connects the specified net to the specified pins or ports.

Equivalent Scheme command: `dbConnect`

```
status connect_net
net object_list
```

connect_pin

Connects pins or ports at any level of hierarchy.

```
int connect_pin
-from from_object
-to to_list
-port_name port_name
-verbose
```

connect_power_switch

Connects switch pins of the power switches in the design.

```
int connect_power_switch
-source object
-port_name port_name
-mode hfn | daisy
[-ack_out object]
[-ack_port_name port_name]
[-direction horizontal | vertical]
[-verbose]
[-voltage_area list]
[-object_list objects]
[-lib_pin library_pin_names]
```

connect_spare_diode

Uses the spare diode ports found in the design to fix antenna violations.

```
status connect_spare_diode
[-exclude_nets collection_of_nets]
[-antenna_check_engine internal | hercules]
[-internal_check_option all |
top_layer_only]
[-routing skip | route]
[-distance distance_number]
[-signal_route_options ignore_lower_layers |
include_lower_layers |
include_all_lower_layers | advanced]
[-max_ratio max_ratio_number]
```

connect_supply_net

Connects the supply net to the specified supply ports and pins. This command is supported only in UPF mode.

```
status connect_supply_net
supply_net_name
-ports list
```

connect_tie_cells

Instantiates tie-high and tie-low cells and connects them to the specified cell ports.

```
status connect_tie_cells
-objects {object_coll}
-obj_type port_inst | cell_inst | lib_cell
[-tie_high_lib_cell lib_cell]
[-tie_low_lib_cell lib_cell]
[-tie_highlow_lib_cell lib_cell]
[-tie_high_port_name port]
[-tie_low_port_name port]
[-max_fanout number]
[-max_wirelength number]
[-incremental true | false]
```

continue

Begins the next loop iteration.

convert_from_polygon

Fracture a polygon into a list of rectangles, which are mutually exclusive.

```
list convert_from_polygon
polygon
[-format format]
```

convert_mw_lib

Converts a Milkyway library's cell data.

```
status convert_mw_lib
mw_lib
[-cell_name cell_name]
[-all]
[-previous]
```

convert_to_polygon

Returns a polygon from any supported object.

```
list convert_to_polygon
[-quiet]
object_spec
```

convert_wire_ends

Converts the currently opened cell's signal wire ends.

```
status_value convert_wire_ends
```

convert_wire_to_pin

Converts wires to pins for either all nets or specified nets in the selected wire set.

```
status convert_wire_to_pin
[-net_names net_names]
objects
```

copy_collection

Duplicates the contents of a collection, resulting in a new collection. The base collection remains unchanged.

```
collection copy_collection
collection1
```

copy_floorplan

Copies floorplan data from a specified design to the current design in a Milkyway design library.

```
status copy_floorplan
[-library design_library_name]
-from design_name
[-macro]
[-filler]
[-pad]
[-power_plan]
[-verbose]
[-incremental]
```

copy_mim

Copies cell placement, blockages, or shape from one multiple instantiated module (MIM) plan group to others in same group.

```
status copy_mim
[-type placement | blockage | boundary]
[-restore_placement]
collection
```

copy_mw_cel

Copies Milkyway designs from a source design library to a target design library.

Equivalent Scheme command: `geCopyCell`

```
status copy_mw_cel
-from source_mw_cel_name
[-to target_mw_cel_name]
[-from_library source_library_name]
[-to_library target_library_name]
[-hierarchy]
[-check_only]
[-overwrite]
```

copy_mw_lib

Copies a Milkyway library to another location.

Equivalent Scheme command: `cmCopyLib`

```
status copy_mw_lib
[-from mw_lib | -from_lib_id lib_id]
-to lib_name
```

copy_objects

Copies one or more objects.

Equivalent Scheme command: `geCopy`

```
new_objects copy_objects
[-delta vector]
[-to point]
[-use_same_net]
objects
```

count_drc_violations

Returns the number of design rule constraint (DRC) violations.

```
int count_drc_violations
[-intersect bbox]
[-ignoring bbox]
[-include_types types]
[-ignore_types types]
[-include_layers layers]
[-ignore_layers layers]
[-use_new_drc]
[-drc_cell_name drc_cell_name]
[-return_error_type]
[-verbose]
```

cputime

Reports the CPU time in seconds.

```
int cputime
[-all]
[-verbose]
```

create_auto_shield

Performs automatic shield routing.

Equivalent Scheme command:

`axgAutoShieldRoute`

```
status create_auto_shield
[-with_ground net_name]
[-nets collection_of_nets]
[-ignore_shielding_net_pins]
[-ignore_shielding_net_rails]
[-coaxial_below]
[-coaxial_above]
```

create_base_array

Creates a base array record in the design.

Equivalent Scheme commands:

`axCreateBaseArrayRecord,`
`dbCreateBaseArrayRow`

```
status create_base_array
[-tile_name tile_name]
-coordinate rectangle
[-direction direction]
```

create_boundary

Creates a boundary for a design or library cell.

Equivalent Scheme command:

`dbCreateCellBoundary`

```
status create_boundary
[-coordinate rectangle
 | -poly {point point ...}
 | -by_terminal]
[-core]
[-left_offset l_offset]
[-right_offset r_offset]
[-top_offset t_offset]
[-bottom_offset b_offset]
[-lib_cell_type type
```

create_bounds

Creates a fixed move bound or floating group bound in the design.

Equivalent Scheme command:
`fphCreateMovebounds`

```
int create_bounds
[-name bound_name]
[-coordinate {llx1 lly1 urx1 ury1 ...}]
[-dimension {width height}]
[-effort low | medium | high | ultra]
[-type soft | hard]
[-exclusive]
[-color range_0_to_63]
[-cycle_color]
object_list
```

create_buffer_tree

Creates a buffer tree for the specified driver pins and nets.

Equivalent Scheme commands:
`astFanoutSetup, astHFCTS, pdsHFNOptimization`

```
status create_buffer_tree
[-from pin_net_list]
[-net_scope]
[-no_legalize]
```

create_cell

Creates cells in the current design or its subdesigns.

Equivalent Scheme command: `geAddCell`

```
int create_cell
cell_list
reference_name
```

create_clock

Creates a clock object and defines its waveform in the current design.

```
status create_clock
[-name clock_name]
[-add]
[source_objects]
[-period period_value]
[-waveform edge_list]
```

create_clock_mesh

Creates a grid of horizontal and vertical straps that are joined by vias for clock mesh implementation.

```
status create_clock_mesh
[-net net]
[-layers hor_ver_list]
[-num_straps hor_ver_list | pitches
hor_ver_list
  | -max_pitches hor_ver_list
  | -relative_pitches hor_ver_list]
[-widths hor_ver_list
  | -relative_widths hor_ver_list]
[-keepouts list_of_points]
[-ring]
[-bounding_box rectangle]
[-lower_left hor_ver_list]
[-upper_right hor_ver_list]
[-max_displacement hor_ver_list]
[-load net_or_pins]
[-avoid instances]
[-no_snap]
[-check_only]
[-remove_display]
[-verbose]
[-offset hor_ver_list]
[-full_pitch_perimeter]
[-pitches ]
```

create_command_group

Creates a new command group.

```
string create_command_group
group_name
```

create_connview

Automatically invoke Hercules connectivity engine to generate connectivity (CONN) view and current source files (CSF) for nonstandard cells. The generated CONN view and CSF files can be used during IR drop analysis.

```
status create_connview
-library library_name
-design design_name
[-power_nets net_names]
[-ground_nets net_names]
[-generate_csf]
[-skip_via mask_names]
[-connview_skip_cell cell_names]
[-csf_skip_cell cell_names]
[-layer_text mask_names_text]
```

create_differential_group

Defines a differential group for nets.

Equivalent Scheme commands:

```
axgDefineDifferential
```

```
status create_differential_group
-group group_name
-nets {collection_of_nets}
```

create_drc_error

Creates an error record.

```
collection create_drc_error
-type error_type
[-status error_status]
[-info description]
[-error_view mw_error_view]
[-details details]
```

create_drc_error_type

Creates an error type record. Each error object must be associated with one and only one error type record.

```
integer create_drc_error_type
-name type_name
[-class type_class]
[-info description]
[-status error_status]
[-level err_type_level]
[-error_view mw_error_view]
```

create_edit_group

Creates a new edit group from the specified objects.

```
collection create_edit_group
[-name group_name]
objects
```

create_fp_block_shielding

Creates signal shielding for plan groups and soft macros.

Equivalent Scheme command:

```
fphCreateHierSignalShielding
```

```
status create_fp_block_shielding
[-inside_boundary]
[-outside_boundary]
[-side_list {left | right | top | bottom}]
[-metal_layers layer_list]
[-shielding_width factor_or_distance]
[-width_in_microns]
[-tie_to_net net]
[-block_level]
[objects]
```

create_fp_blockages_for_child_hardmacro

Creates routing blockages for hard macros within soft macros.

Equivalent Scheme command:

`fphCreateBlkgFromSMHardmacro`

```
status
create_fp_blockages_for_child_hardmacro
list_of_softmacros
```

create_fp_group_block_ring

Creates a block ring for a group of hard macro blocks.

```
status create_fp_group_block_ring
-nets nets
[-horizontal_ring_layer layer]
[-horizontal_ring_offset offset]
[-horizontal_ring_spacing spacing]
[-horizontal_ring_width width]
[-vertical_ring_layer layer]
[-vertical_ring_offset offset]
[-vertical_ring_spacing spacing]
[-vertical_ring_width width]
[-horizontal_strap_width width]
[-horizontal_strap_layer layer]
[-vertical_strap_width width]
[-vertical_strap_layer layer]
[-output_directory directory]
[-skip_strap]
```

create_fp_pins

Creates pins for the specified list of child ports.

Equivalent Scheme commands:

`fphAddSMBusPin, fphAddSMPin, fphCreateCustomSMPins, fphCreateSMPins`

```
pins create_fp_pins
[-side side_num_or_name]
-layer layer
[-width width]
[-step step_num]
{-at location | -offset offset}
child_ports
```

create_fp_placement

Places hard macros and leaf cells.

Equivalent Scheme command: `fphPlaceDesign`

```
int create_fp_placement
[-effort low | high]
[-max_fanout positive_integer]
[-no_hierarchy_gravity]
[-no_legalize]
[-incremental placement_string]
[-congestion_driven]
[-timing_driven]
[-num_cpus number_of_cpus]
[-plan_groups collection_of_plan_groups]
[-voltage_areas collection_of_voltage_areas]
[-optimize_pins]
[-ignore_scan]
[-write_placement_blockages]
```

create_fp_plan_group_padding

Creates padding for the specified plan groups.

Equivalent Scheme command:
`fphPadPlangroups`

```
status create_fp_plan_group_padding
[-internal_widths {left right top bottom}]
[-external_widths {left right top bottom}]
[plan_groups]
```

create_fp_virtual_pad

Creates virtual power or ground pads for power network analysis and power network synthesis.

Equivalent Scheme command:
`fphAddVirtualPad`

```
status create_fp_virtual_pad
[-nets string]
[-layer string]
[-point {x y}]
[-load_file string]
[-save_file string]
```

create_generated_clock

Creates a generated clock object.

```
string create_generated_clock
[-name clock_name]
[-add]
source_objects
-source master_pin
[-master_clock clock]
[-divide_by divide_factor
 | -multiply_by multiply_factor]
[-duty_cycle percent]
[-invert]
[-preinvert]
[-edges edge_list]
[-edge_shift edge_shift_list]
[-combinational]
```

create_ilm

Creates an interface logic model (ILM) for the current design.

Equivalent Scheme command:

```
hdpCreateModels
```

```
status create_ilm
[-identify_only]
[-extract_only]
[-ignore_ports port_list]
[-no_auto_ignore]
[-latch_level levels]
[-keep_macros]
[-keep_boundary_cells]
[-keep_full_clock_tree]
[-include_side_load boundary | all | none]
[-traverse_disabled_arcs]
[-compact none | output | all]
[-case_controlled_ports port_list]
[-must_connect_ports port_list]
[-keep_parasitics]
[-include_xtalk]
[-include_all_logic]
[-scenarios scenario_list]
[-verbose]
```

create_ilm_models

Creates interface logic models (ILMs) for the specified macros of the design.

```
status create_ilm_models
[-no_auto_ignore]
[-latch_level levels]
[-keep_full_clock_tree]
[-keep_parasitics]
[-verbose]
[-include_xtalk]
[-include_all_logic]
[-compact none | output | all [-in_context]]
[-scenarios scenario_list]
macro_reference_list
```

create_lib_track

Creates wire tracks for a library.

```
status create_lib_track
[-lib lib_name]
[-tile tile_name]
[-dir dir_list]
[-offset offset_list]
```

create_macro_fram

Extracts blockage, pin and via information of an import macro cell.

Equivalent Scheme command: `geNewMakeMacro`

```
integer create_macro_fram
[-library_name library_name]
[-cell_name cell_name]
[-preserve_all_metal_blockage]
[-routing_blockage_output_layer metBlk |
rGuide | zeroG]
[-treat_all_blockage_as_thin_wire]
[-treat_metal_blockage_as_thin
{collection_of_layers}]
[-extract_blockage_by_block_core_with_margin
{collection_of_layer_value}]
[-extract_blockage_by_merge_with_threshold
{collection_of_layer_value}]
[-identify_macro_pin_by_pin_text]
[-extract_pin_connectivity_through
{collection_of_layers}]
[-poly_pin_text_layers {list_of_layers}]
[-m1_pin_text_layers {list_of_layers}]
[-m2_pin_text_layers {list_of_layers}]
[-m3_pin_text_layers {list_of_layers}]
[-m4_pin_text_layers {list_of_layers}]
[-m5_pin_text_layers {list_of_layers}]
[-m6_pin_text_layers {list_of_layers}]
[-m7_pin_text_layers {list_of_layers}]
[-m8_pin_text_layers {list_of_layers}]
[-m9_pin_text_layers {list_of_layers}]
[-m10_pin_text_layers {list_of_layers}]
[-m11_pin_text_layers {list_of_layers}]
[-m12_pin_text_layers {list_of_layers}]
[-m13_pin_text_layers {list_of_layers}]
[-m14_pin_text_layers {list_of_layers}]
[-m15_pin_text_layers {list_of_layers}]
[-pin_must_connect_area_layer_number
{collection_of_layer_value}]
[-auto_pin_must_connect_area_threshold
{collection_of_layer_value}]
[-extract_via_within_pin_area_only]
[-extract_via_on_layer
{collection_of_layers}]
```

create_mw_cel

Creates a Milkyway design.

Equivalent Scheme command: `geCreateCell`

```
status create_mw_cel
[-view CEL | FRAM | FILL | err | ILM]
[-verbose]
mw_cel_name
```

create_mw_lib

Creates a Milkyway library.

Equivalent Scheme command: `cmCreateLib`

```
status create_mw_lib
[-technology technology_file_name]
[-plib plib_file_name]
[-hier_separator sep]
[-bus_naming_style style]
[-mw_reference_library lib_list]
[-reference_control_file rc_file_name]
[-open]
libName
```

create_net

Creates nets in the current design or its subdesign.

Equivalent Scheme command: `dbCreateNet`

```
status create_net
[-power | -ground | -tie_high | -tie_low]
net_list
```

create_net_shape

Creates a new net shape.

Equivalent Scheme commands: `geAddPath, geAddWire`

```
collection create_net_shape
[-type wire | path | rect | poly]
-origin point
  | -points list_of_points
  | -bbox rect
  | -boundary boundary
[-length real]
[-width real]
[-path_type square | round |
extend_half_width | octagon]
-layer layer
-net net_name
[-vertical]
[-route_type route_type]
[-datatype int]
[-avoid_short_segment]
```

create_open_drc_error

Creates an error record of an error type in the "Open" type class.

```
collection create_open_drc_error
-type error_type
[-status error_status]
[-info description]
[-error_view mw_error_view]
[-net net]
[-details details]
```

create_open_locator_drc_error

Creates an error record of an error type in the "OpenLocator" type class.

```
collection create_open_locator_drc_error
-type error_type
-point1 point
-point2 point
[-status error_status]
[-info description]
[-net net]
[-referenced_drc_error drc_error]
[-error_view mw_error_view]
```

create_operating_conditions

Creates a new set of operating conditions in a library.

```
int create_operating_conditions
-name name -library library_name
-process process_value
-temperature temperature_value
-voltage voltage_value
[-tree_type tree_type]
[-calc_mode calc_mode]
[-rail_voltages rail_value_pairs]
```

create_pad_rings

Creates pad rings for pins in boundary pads.

Equivalent Scheme command:

```
axgCreatePadRings
```

```
integer create_pad_rings
[-create all | pg | specified_net]
[-nets {collection_of_nets}]
[-route_pins_on_layer number_or_name]
[-min_shrink_routing_boundaries_for_all_
boundary_pads distance]
[-max_shrink_routing_boundaries_for_all_
boundary_pads distance]
[-undo]
```

create_partition

Creates and manipulates partitions in a design through command-line specification, autopartitioning,or manual GUI-based changes.

```
status create_partition
[-input_files files]
[-reset overrides | partition | keepouts |
all]
[-auto_partition instance_count | area]
[-physical]
[-logical]
[-area sub_block_area]
[-internal_keepout keepout]
[-external_keepout keepout]
[-utilization block_utilization]
[-aspect_ratio float]
[-force]
[-output_dir dir_name]
[-create verilog_files | design |
top_level_floorplan]
[-verbose]
[module_name_list]
```

create_pg_network

Creates or changea a power and ground network connecting multiple hierarchical cells.

```
status create_pg_network
[-net net
 | -create_net net_name [-power
 | -ground]]
[cell_list]
```

create_physical_bus

Creates a physical bus with a list of nets.

```
collection create_physical_bus
name
-nets net_list
[-sort {ascending | descending | none}]
[-delimiter delimiter]
[-right_precedence]
[-quiet]
```

create_physical_buses_from_patterns

Automatically groups nets into buses based on their net name and group size criteria.

```
status create_physical_buses_from_patterns
[-net_name_prefix string]
[-net_order ascending | descending]
[-minimum_nets integer]
[-maximum_nets integer]
[-divider integer]
[-no_braces]
[-no_brackets]
[-no_angle_brackets]
[-no_underlines]
[-no_colons]
[-no_parentheses]
```

create_pin_guide

Creates a pin guide for a plan group, or soft macro, or the current cell to constrain terminals generated by pin assignment to a specified bounding box.

Equivalent Scheme command:

```
fphCreatePinGuide
```

```
pin_guide create_pin_guide
{-bbox bounding_box_rect
 | -boundary rectilinear_boundary}
[-parents soft_macro_or_plan_group]
[-name pin_guide_name]
objects
```

create_placement

Performs coarse placement on the current design.

Equivalent Scheme command: `astPlaceDesign`

```
int create_placement
[-effort low | medium | high]
[-quick]
[-timing_driven]
[-congestion [-congestion_effort low |
medium | high]]
[-check_only]
[-num_cpus number_of_cpus]
[-mpc]
[-ignore_scan]
```

create_placement_blockage

Creates a new placement blockage.

Equivalent Scheme commands:
`axgAddBlockage, axgAddSoftBlockage`

```
status create_placement_blockage
-bbox rectangle
[-type {hard | soft | pin | hard_macro |
partial}]
[-blocked_percentage percentage]
[-no_register]
[-blocked_layers layers]
[-name blockage_name]
```

create_plan_groups

Creates instance plan groups in the design.

Equivalent Scheme command: `axgHierPlan`

```
int create_plan_groups
[-coordinate {coordinates_list}]
[-rectangle rectangle_area]
[-polygon {polygon_area}]
[-dimension {width height}]
[-target_aspect_ratio aspect_ratio]
[-target_utilization utilization]
[-is_fixed]
[-color range_0_to_63]
[-cycle_color]
logic_cell_list
```

create_port

Creates ports in the current design or its subdesign.

Equivalent Scheme command: `dbCreatePort`

```
status create_port
port_list
[-direction dir]
```

create_power_domain

Creates a power domain, which provides a power supply distribution network.

UPF Mode

```
string create_power_domain
domain_name
[-elements list]
[-include_scope]
[-scope instance_name]
```

Non-UPF Mode

```
status create_power_domain
domain_name
[-power_down]
[-power_down_ctrl object_list]
[-power_down_ack object_list]
[-object_list object_list]
```

create_power_straps

Creates power straps in a design.

Equivalent Scheme command:

axgCreateStraps

```
status create_power_straps
-nets collection_of_nets | -undo
[-direction horizontal | vertical]
[-start_at distance]
[-layer number_or_name]
[-width distance]
[-configure groups_and_step |
groups_and_stop | step_and_stop | rows |
macros | groups_and_stop | step_and_stop |
rows | macros]
[-num_groups int]
[-step distance]
[-stop distance]
[-pitch_within_group distance]
[-start_low_ends boundary | first_targets |
coordinate | last_targets | first_targets |
coordinate | last_targets]
[-start_low_ends_coordinate distance]
[-start_high_ends boundary | first_targets |
coordinate | last_targets | first_targets |
coordinate | last_targets]
[-start_high_ends_coordinate distance]
[-extend_low_ends to_first_target |
to_boundary_and_generate_pins |
force_to_boundary_and_generate_pins | off |
to_boundary_and_generate_pins |
force_to_boundary_and_generate_pins | off]
[-extend_high_ends to_first_target |
to_boundary_and_generate_pins |
force_to_boundary_and_generate_pins | off |
to_boundary_and_generate_pins |
force_to_boundary_and_generate_pins | off]
[-num_placement_strap int]
[-increment_x_or_y distance]
[-special_via_rule
[-special_via_x_offset distance]
[-special_via_y_offset distance]
[-offset_both_sides_for_special_via]
[-special_via_x_size distance]
[-special_via_y_size distance]
[-special_via_x_step distance]
[-special_via_y_step distance]]
[-advanced_via_rules]
[-special_rules string]
[-look_inside_std_cells
```

```
[-std_cells collection_of_cells]]
[-keep_floating_wire_pieces]
[-ignore_cell_boundary]
[-clip_at_top_cell_boundaries]
[-do_not_merge_targets]
[-optimize_wire_locations]
[-ignore_parallel_targets
[-define_parallel_targets_by_wire_directions
]]
[-do_not_route_over_macros]
[-extend_for_multiple_connections
[-extension_gap distance]]
[-mark_as_std_cell_pin_connections |
-mark_as_ring]
[-num_cpu int]
```

create_power_switch

Creates a power switch at the specified power domain. This command is supported only in UPF mode.

```
string create_power_switch
switch_name
-domain domain_name
-output_supply_port {port_name
supply_net_name}
-input_supply_port {port_name
supply_net_name}
-control_port {port_name net_name}
[-ack_port {port_name net_name
[{boolean_function}]}]
[-ack_delay {port_name delay}]
-on_state {state_name input_supply_port
{boolean_function}}
[-off_state {state_name {boolean_function}}]
```

create_power_switch_array

Adds header/footer cells into the design in an array pattern.

```
status create_power_switch_array
-lib_cell lib_cell_or_power_switch
[-voltage_area voltage_area]
[-bounding_box rectangle]
[-relative_to_voltage_area]
[-design hierarchy_name]
-x_increment dx
-y_increment dy
[-start_row index]
[-start_column index]
[-snap_to_row_and_tile]
[-orientation {N | W | S | E | FN | FE | FS |
FW}]
[-respect list]
[-pattern normal | staggered]
[-prefix prefix_name]
```

create_power_switch_ring

Creates multithreshold-CMOS cells around a voltage area or a macro, in a ring pattern, either full ring or part of ring. If the pattern is part of ring, specify the start point and end point on the boundary. The switch cells will be placed anti-clockwise.

```
status create_power_switch_ring
-switch_lib_cell lib_cells_or_power_switches
[-outer_corner_lib_cell
outer_corner_lib_cell_name]
[-inner_corner_lib_cell
inner_corner_lib_cell_name]
[-area_obj voltage_area_or_macro]
[-design hierarchy_name]
[-prefix string]
[-switch_orientation N | W | S | E | FN | FE
| FS | FW]
[-outer_corner_orientation N | W | S | E |
FN | FE | FS | FW]
[-inner_corner_orientation N | W | S | E |
FN | FE | FS | FW]
[-density float]
[-offset {f1 f2...}]
[-start_point {x_y}]
[-end_point {x_y}]
[-check_overlap]
[-filler_lib_cell {pattern}]
```

create_preroute_vias

Creates vias between specified layers.

Equivalent Scheme command:

axgCreatePrerouteContacts

```
status create_preroute_vias
[-nets {collection_of_nets}]
[-buses list_of_bus_names]
[-from_layer number_or_name]
[-to_layer number_or_name]
[-from_object_strap]
[-from_object_user]
[-from_object_std_pin]
[-from_object_std_pin_connection]
[-from_object_macro_io_pin]
[-from_object_macro_io_pin_connection]
[-from_object_ring]
[-from_object_bus]
[-to_object_strap]
[-to_object_user]
[-to_object_std_pin]
[-to_object_std_pin_connection]
[-to_object_macro_io_pin]
[-to_object_macro_io_pin_connection]
[-to_object_ring]
[-to_object_bus]
[-connect_to_targets_on_all_layers_in_betwee
n]
[-ignore_parallel_targets]
[-do_not_merge_targets]
[-special_via_rule
[-special_via_x_offset distance]
[-special_via_y_offset distance]
[-offset_both_sides_for_special_via]
[-special_via_x_size distance]
[-special_via_y_size distance]
[-special_via_x_step distance]
[-special_via_y_step distance]]
[-within {{llx lly} {urx ury}}]
[-advanced_via_rules]
[-optimize_via_locations]
[-undo]
[-mark_as strap | user_defined |
standard_cell_pin_connection |
macro_io_pin_connection | ring | bus]
```

create_pst

Creates a power state table (PST), using a specific order of supply nets.

```
string create_pst
table_name
-supplies list
```

create_qor_snapshot

Creates a QoR snapshot of timing, physical, constraints, clock, and power data on active scenarios and stores it in the location specified by the icc_snapshot_storage_location variable.

NOTE: This is the new version of the create_qor_snapshot command that supports both multicorner-multimode designs as well as non-multicorner-multimode designs.

```
create_qor_snapshot
[-name name]
[-power]
[-clock_tree]
[-show_all]
[-save_mw]
[-significant_digits digits]
```

create_qtm_clock

Creates a quick timing model (QTM) clock port.

```
string create_qtm_clock
-type clock_type
clock_list
```

create_qtm_constraint_arc

Creates a constraint arc for a quick timing model (QTM).

```
string create_qtm_constraint_arc
[-name arc_name]
[-setup] [-hold]
-from port_name [-to port_spec]
-edge triggering_edge
[-path_type name]
[-path_factor multiplication_factor]
[-value constraint_value]
[-input_transition_fall ftrans]
[-input_transition_rise rtrans]
```

create_qtm_delay_arc

Creates a delay arc for a quick timing model (QTM).

```
string create_qtm_delay_arc
[-name arc_name]
-from port_spec
-to port_spec
[-edge triggering_edge]
[-path_type path_type]
[-path_factor multiplication_factor]
[-value delay_value]
[-total_value total_value]
[-input_transition_fall ftrans]
[-input_transition_rise rtrans]
```

create_qtm_drive_type

Creates a drive type in a quick timing model (QTM).

```
string create_qtm_drive_type
-lib_cell lib_cell_name
[-input_pin pin_name]
[-output_pin pin_name]
[-input_transition_rise rtrans]
[-input_transition_fall ftrans]
drive_type_name
[-lib_cell_input_transition
lib_cell_input_transition]
```

create_qtm_generated_clock

Creates a generated clock for a quick timing model (QTM).

```
string create_qtm_generated_clock
-source master_clock_name
[-divide_by divide_factor
 | -multiply_by multiply_factor]
[-invert]
generated_clock_name
```

create_qtm_insertion_delay

Specifies the insertion delay on the clock port of a quick timing model (QTM).

```
string create_qtm_insertion_delay
[-max]
[-min]
[-value insertion_delay]
port_list
```

create_qtm_load_type

Creates a load type for a quick timing model (QTM) description.

```
string create_qtm_load_type
-lib_cell name
[-input_pin pin_name]
load_type name
```

create_qtm_model

Begins the definition of a quick timing model (QTM) description.

```
string create_qtm_model
model_name
```

create_qtm_path_type

Creates a path type in a quick timing model (QTM) description.

```
string create_qtm_path_type
-lib_cell name
[-input_pin pin_name]
[-output_pin pin_name]
[-fanout count]
path_type name
```

create_qtm_port

Creates a quick timing model (QTM) port.

```
string create_qtm_port
-type port_type
port_list
```

create_rail_setup

Creates a setup file and writes out necessary files for performing rail analysis in PrimeRail.

```
status create_rail_setup
[-sdc sdc_file]
[-spef spef_file]
[-verilog verilog_file]
[-no_rc_extract]
[-hierarchy]
[-directory dir_name]
[-parasitic_corner min | max]
[-no_save]
[-upf string]
```

create_rectangular_rings

Creates rectangular rings in the design.

Equivalent Scheme command:

`axgCreateRectangularRings`

```
integer create_rectangular_rings
[-around core | specified |
specified_as_group |
all_macros_except_specified | rectangle]
[-cells {collection_of_cells}]
[-within {{llx lly} {urx ury}}]
-nets {collection_of_nets}
[-skip_left_side]
[-skip_right_side]
[-skip_bottom_side]
[-skip_top_side]
[-left_segment_layer number_or_name]
[-right_segment_layer number_or_name]
[-bottom_segment_layer number_or_name]
[-top_segment_layer number_or_name]
[-left_segment_width distance]
[-right_segment_width distance]
[-bottom_segment_width distance]
[-top_segment_width distance]
[-offsets adjusted | absolute]
[-left_offset distance]
[-right_offset distance]
[-bottom_offset distance]
[-top_offset distance]
[-extend_ll]
[-extend_lh]
[-extend_rl]
[-extend_rh]
[-extend_bl]
[-extend_bh]
[-extend_tl]
[-extend_th]
[-create_innermost_core_ring_conservatively]
[-ignore_parallel_targets]
[-advanced_via_rules]
[-extend_for_multiple_connections]
[-extension_gap distance]
-undo
```

create_rectilinear_rings

Creates rectilinear rings in the design.

```
status create_rectilinear_rings
[-nets {collection_of_nets}]
[-around core | macros |
all_macros_except_specified]
[-macro_cells {collection_of_macro_cells}]
[-offset {x_offset y_offset}]
[-layers {h_segment_layer_name
v_segment_layer_name}]
[-width {width_of_h_segments
width_of_v_segments}]
[-space {space_between_h_segments
space_between_v_segments}]
[-exclude_instances
{collection_of_macro_cells}]
[-extension_of_excluded_instances
{x_extension y_extension}]
[-max_deviation distance]
[-create_bridges {offset space}]
[-ignore_parallel_targets]
[-undo]
```

create_route_guide

Creates a new route guide.

Equivalent Scheme commands:

```
axCreateRouteGuide, axgAddRouteGuide
```

```
object create_route_guide
-coordinate rect
[-no_signal_layers string]
[-no_preroute_layers string]
[-preferred_direction_only_layers string]
[-zero_min_spacing]
[-repair_as_single_sbox]
[-horizontal_track_utilization int_range]
[-vertical_track_utilization int_range]
[-switch_preferred_direction]
[-name string]
```

create_routing_blockage

Creates a new routing blockage on metal or via routing blockage layers.

```
collection create_routing_blockage
-layers layer_list
-bbox | -boundary {polygon_boundary_points}
```

create_rp_group

Creates relative placement groups.

```
collection create_rp_group
group_list
[-design design_name]
[-columns num_cols]
[-rows num_rows]
[-alignment bottom-left | bottom-pin |
bottom-right]
[-pin_align_name pin_name]
[-utilization percentage]
[-ignore]
[-x_offset float]
[-y_offset float]
[-compress]
[-cts_option fixed_placement | size_only]
[-route_opt_option fixed_placement |
in_place_size_only]
[-psynopt_option fixed_placement |
size_only]
[-move_effort low | medium | high]
[-allow_keepout_over_tapcell false | true]
```

create_scenario

Creates a scenario in memory.

```
status create_scenario
scenario_name
```

create_short_drc_error

Creates an error record of an error type in the "Short" type class.

```
collection create_short_drc_error
-type error_type
-bbox {llx lly urx ury}
[-status error_status]
[-info description]
[-net1 net]
[-net2 net]
[-layer layer]
[-error_view mw_error_view]
```

create_site_row

Creates a row of sites.

Equivalent Scheme command:

dbCreateCellRow

```
collection create_site_row
-coordinate {X Y}
[-name row_name]
-kind site_type
-space space
-count site_count
[-orient orientation]
[-dir direction]
```

create_spacing_drc_error

Creates an error record of an error type in the "Spacing" type class.

```
collection create_spacing_drc_error
-type error_type
-bbox {llx lly urx ury}
[-status error_status]
[-info description]
[-direction direction]
[-net1 net]
[-net2 net]
[-layer layer]
[-error_view mw_error_view]
```

create_stack_via_on_pad_pin

create stack vias from pad layer to top layer for flip-chip drivers.

Equivalent Scheme command:

trCreateStackViaOnPadPin

```
status create_stack_via_on_pad_pin
-from_metal mX | MX | tech_layer_number
-to_metal mX | MX | tech_layer_number
[-remove_existing_stack_via bool]
[-route_type user_enter | signal_route]
```

create_supply_net

Creates a supply net for the specified power domain. The supply net is created in the logic hierarchy at the same scope as the specified power domain. This command is supported only in UPF mode.

```
string create_supply_net
supply_net_name
-domain domain_name
[-reuse]
[-resolve unresolved | parallel]
```

create_supply_port

Creates a supply port in the specified power domain or in the current scope if no power domain is specified. This command is supported only in UPF mode.

```
string create_supply_port
supply_port_name
[-domain domain_name]
[-direction in | out]
```

create_terminal

Creates a new terminal for a logical port.

Equivalent Scheme command: `geAddRectPin`

```
terminal create_terminal
{-bbox rect | -boundary boundary}
-layer layer
-port string
[-direction {left | right | up | down}]
[-name string]
```

create_text

Creates a new text.

Equivalent Scheme command: `dbCreateText`

```
object create_text
-origin {x_y}
[-height height]
[-layer layer_name]
[-orient orient_type]
[-anchor text_anchor]
text
```

create_track

Creates the tracks for a routing layer or a poly layer.

Equivalent Scheme commands:
`auCreateWireTracks, axAddWireTracks, axCreateTrackRecord`

```
int create_track
-layer layer
[-space track_pitch]
[-count number_of_tracks]
[-coord start_x_or_y]
[-dir X | Y]
[-bounding_box track_boundary_box]
```

create_user_shape

Creates a new user shape. A user shape is a metal shape that is not associated with a net.

Equivalent Scheme command: `geAddRectangle`

```
collection create_user_shape
[-type wire | path | trap | rect | poly]
-origin point
  | -points list_of_points
  | -bbox rect
  | -boundary boundary
[-length real]
[-width real]
[-path_type square | round |
extend_half_width | octagon]
-layer layer
[-vertical]
[-route_type route_type]
[-datatype int]
[-avoid_short_segment]
```

create_via

Creates a new via.

Equivalent Scheme commands: `geAddContact, geAddContactArray`

```
object create_via
-at point
[-name string]
-master string | -auto
[-net string | -no_net]
[-route_type route_type | signal_route |
signal_route_global | signal_route_detail |
pg_ring | pg_strap | pg_macro_io_pin_conn |
pg_std_cell_pin_conn | clk_ring | clk_strap
| clk_zero_skew_route | bus | shield |
shield_dynamic | clk_fill_track]
[-orient orient | FN | FS | FE | FW | NW | NE
| EN | ES | SE | SW | WN | WS | 0 | 90 | 180
| 270 | 0-mirror | 90-mirror | 180-mirror |
270-mirror]
[-type via | via_array | via_cell]
[-row int]
[-col int]
[-x_pitch real]
[-y_pitch real]
[-allow_multiple]
```

create_voltage_area

Creates a voltage area at the specified region for providing placement constraints of cells associated with the region.

Equivalent Scheme commands:
`aprCreateVoltageArea, axgSetCellInstVoltage, axgSetVoltageOperatingCond`

```
int create_voltage_area
modules -name voltage_area_name
 | -power_domain power_domain_name
-coordinate llx1_lly1_urx1_ury1_...
[-guard_band_x guard_band_width]
[-guard_band_y guard_band_width]
[-is_fixed]
[-target_utilization utilization]
[-color string]
[-cycle_color]
```

create_zrt_shield

Performs automatic shield routing.

```
status create_zrt_shield
[-mode new | unshield | reshield]
[-nets collection_of_nets]
[-with_ground net_name]
[-ignore_shielding_net_pins true | false]
[-ignore_shielding_net_rails true | false]
[-coaxial_below true | false]
[-coaxial_above true | false]
[-coaxial_below_skip_tracks
number_of_tracks]
[-coaxial_above_skip_tracks
number_of_tracks]
[-pg_via_tie_effort_level low | medium |
high]
```

current_design

Sets the working design.

```
string current_design
[design]
```

current_design_name

Returns the current design name.

```
string current_design_name
```

current_instance

Sets the working instance object and enables other commands to be used on a specific cell in the design hierarchy.

```
string current_instance
[instance]
```

current_mw_cel

Gets (or sets) the working Milkyway design in the tool.

Equivalent Scheme command: `geGetEditCell`

```
collection current_mw_cel
[mw_cel]
```

current_mw_lib

Gets the current Milkyway library.

Equivalent Scheme command:

```
dbGetCurrentLibId
```

```
collection current_mw_lib
```

current_scenario

Sets the current scenario.

```
string current_scenario
[scenario_name]
```

cut_objects

Cuts from or adds to the boundary of one or more geometric objects.

```
new_objects cut_objects
{-bbox rect | -boundary boundary
 | -by collection}
[-channel extra_channel_spacing]
[-invert]
[-keep_placement]
[-keep_pad_to_core_distance]
objects
```

cut_row

Cuts rows from the current design.

Equivalent Scheme command:

```
axgCutRowByArea
```

```
status cut_row
[-all]
[-area {{ll_x ll_y} {ur_x ur_y}}]
```

date

Returns a string containing the current date and time.

```
string date
```

define_antenna_accumulation_mode

Defines an antenna accumulation mode route rule.

Equivalent Scheme command:

`dbDefineAntennaAccumMode`

```
status define_antenna_accumulation_mode
[mw_lib]
[-cut_to_metal]
[-metal_to_cut]
```

define_antenna_layer_ratio_scale

Creates an antenna layer ratio route rule.

Equivalent Scheme command:

`dbDefineAntennaLayerRatioScale`

```
status define_antenna_layer_ratio_scale
[mw_lib]
-layer layer_name
-layer_scale layer_scale
-accumulate_scale accumulate_scale
```

define_antenna_layer_rule

Defines an advanced antenna rule for the specified layer and stores it in the library.

Equivalent Scheme command:

`dbAddAntennaLayerRule`

```
status define_antenna_layer_rule
[mw_lib]
-mode mode
-layer layer_name
-ratio ratio
[-pratio pratio]
[-nratio nratio]
-diode_ratio diode_ratio
[-scale_factor scale_factor]
```

define_antenna_rule

Defines an advanced antenna rule for the specified mode and stores it in the library.

Equivalent Scheme command:

dbDefineAntennaRule

```
status define_antenna_rule
[mw_lib]
-mode mode
-diode_mode diode_mode
-metal_ratio metal_ratio
-cut_ratio cut_ratio
[-protected_metal_scale metal_scale]
[-protected_cut_scale cut_scale]
```

define_name_rules

Defines a set of name rules for designs.

```
status define_name_rules
name_rules
[-max_length length]
[-target_bus_naming_style bus_naming_style]
[-allowed allowed_chars]
[-restricted restricted_chars]
[-first_restricted first_chars]
[-last_restricted last_chars]
[-reserved_words reserves]
[-replacement_char char]
[-remove_chars]
[-equal_ports_nets]
[-inout_ports_equal_nets]
[-collapse_name_space]
[-case_insensitive]
[-special output_format]
[-prefix prefix_name]
[-map map_string]
[-type object_type] [-reset]
[-remove_internal_net_bus]
[-remove_port_bus]
[-check_bus_indexing]
[-check_bus_indexing_use_type_info]
[-rename_three_state_port_net]
[-check_internal_net_name]
[-remove_irregular_port_bus]
[-remove_irregular_net_bus]
[-flatten_multi_dimension_busses]
[-dont_change_bus_members]
[-dont_change_ports]
[-add_dummy_nets]
[-dummy_net_prefix dummy_nets_format]
[-dir_inout_as_in]
```

define_proc_attributes

Defines attributes of a Tcl procedure, including an information string for help, a command group, a set of argument descriptions for help, and so on. The command returns the empty string.

```
string define_proc_attributes
proc_name
[-info info_text]
[-define_args arg_defs]
[-command_group group_name]
[-hide_body]
[-hidden]
[-dont_abbrev]
[-permanent]
```

define_routing_rule

Defines design-specific, nondefault routing rules that are stored in the design database.

Equivalent Scheme commands:

```
axgDefineVarRule, dbDefineVarRouteRule
```

```
status define_routing_rule
rule_name
-reference_rule_name ref_rule_name
 | -default_reference_rule
[-widths layer_name_and_width_pairs]
[-snap_to_track]
[-spacings layer_name_and_spacing_pairs]
[-shield_widths
layer_name_and_shield_width_pairs]
[-shield_spacings
layer_name_and_shield_spacing_pairs]
[-via_cuts via_name_and_cut_number_pairs]
[-taper_level tapering_level]
[-multiplier_width layer_width]
[-multiplier_spacing layer_spacing]
```

define_scaling_lib_group

Defines a scaling library group to support voltage and temperature scaling.

```
status define_scaling_lib_group
[-name name]
[lib_file_names]
```

define_user_attribute

Defines a new user-defined attribute.

```
int define_user_attribute
-type data_type
-class class_list
[-range_min min]
[-range_max max]
[-one_of values]
[-quiet]
attr_name
```

define_via

Creates a special via that is not defined in the physical library.

```
int define_via
via_name
-rect {layer_name X1 Y1 X2 Y2}
```

define_zrt_redundant_vias

Sets options for redundant via insertion.

```
status define_zrt_redundant_vias
[-from_via {list_of_from_vias}]
[-to_via {list_of_to_vias}]
[-to_via_x_size {list_of_contact_numbers}]
[-to_via_y_size {list_of_contact_numbers}]
[-to_via_weights {list_of_weights}]
```

delete_operating_conditions

Deletes a specific set of operating conditions from a library.

```
status delete_operating_conditions
-library library_name
-name op_cond_name
```

derive_constraints

Propagates design environment, constraints, and attribute settings from the top-level design to the specified subdesigns.

```
int derive_constraints
[-attributes_only]
[-verbose]
[-budget]
cell_list
```

derive_mpc_macro_options

Derives placement constraints for a specific macro or derives macro array constraints for a group of macros.

```
int derive_mpc_macro_options
[-output filename]
[-append]
[-array]
[-footprint]
[-array_name array_name]
[-location {exact | anchor_bound |
anchor_offset | anchor_orient | none}]
[-apply]
[-verbose]
list_of_macros
```

derive_mpc_options

Derives design level floorplan information and generic information for the ports and macros.

```
int derive_mpc_options
[-output filename]
[-append]
[-origin ll | center]
[-core exact | relative | height_only |
width_only]
[-pnets exact | model | none]
[-ports exact | relative | side | none]
[-macros exact | anchor_bound |
anchor_orient | anchor_offset | none]
[-footprint]
[-corner_keepout exact | relative | none]
[-apply]
[-verbose]
```

derive_mpc_port_options

Derives the physical constraints for a specific port or a group of ports.

```
int derive_mpc_port_options
[-output filename]
[-append]
[-group]
[-group_name group_name]
[-order]
[-location {exact | relative | side | none}]
[-apply]
[-verbose]
port_list
```

derive_pg_connection

Connects power and ground pins and tie-off pins to the power and ground nets. It supports both manual mode, where you specify the power and ground nets, and automatic mode, where the tool derives the power and ground nets from the power domain connections. Automatic mode is supported only for multivoltage designs with UPF descriptions and requires logic libraries with power and ground pins.

detect_flcc_hotspot

Performs lithography hot spot detection. FLCC stands for Fast Lithography Compliance Check.

```
detect_flcc_hotspot
[-cell_name
```

detect_lcc_hotspot

Performs full-chip lithography compliance check (LCC) hotspot detection.

```
status detect_lcc_hotspot
-lcc_file_path lcc_path_name
-layers list_of_layers
[-dp_hosts list_of_dp_hosts]
```

disconnect_net

Disconnects a net from pins or ports.

Equivalent Scheme command: `dbDisconnect`

```
status disconnect_net
net
object_list | -all
```

display_flip_chip_route_flylines

Displays flylines of flip-chip nets in the layout view of the IC Compiler GUI.

```
status display_flip_chip_route_flylines
[-nets | -nets_in_file nets_file]
[-open_nets [-output_open_nets
open_net_file]]
```

distribute_objects

Distributes one or more objects.

```
status distribute_objects
[-anchor object]
[-parent]
[-from value_point_rect]
[-to value_point_rect]
[-side {left | right | top | bottom |
hcenter | vcenter}]
[-spread]
[-vertical]
[-offset real]
[-wiretrack_offset int]
[-resize]
[-keep_area]
[-ignore_fixed]
objects
```

drive_of

Returns the drive resistance value of the specified library cell pin.

```
float drive_of
library_cell_pin
[-rise | -fall]
[-piece best | worst | average
average_value]
 | [-min]
```

echo

Echos arguments to standard output.

```
string echo
[-n] [argument...]
```

eco_netlist

Performs engineering change order (ECO) operations on current Milkyway cell.

```
status eco_netlist
[-by_verilog_file verilog_filename]
[-physical]
[-compare_pg]
[-freeze_silicon]
[-write_changes write_changes_file_name]
```

end_fp_trace_mode

Removes the trace mode design from memory.

```
status end_fp_trace_mode
```

error_info

Prints extended information on errors from last command.

```
string error_info
```

estimate_fp_area

Performs automated die size exploration for finding the smallest die size possible to decrease the cost per die. Can also be applied to blocks.

```
status estimate_fp_area
[-min_height min_height]
[-max_height max_height]
[-min_width min_width]
[-max_width max_width]
[-acceptable_overflow percentage]
[-sizing_type fixed_width | fixed_height |
fixed_aspect_ratio]
[-core_sizing_only]
[-keep_blockages]
[-increase_area area]
[-replace_io]
[-maintain_iopad_alignment]
[-power_net_names list_of_names]
[-ir_drop_value target_value]
[-run_preroute_script preroute_script_name]
[-run_pns_script script_name]
[-save_as name]
[-maintain_power_structure]
[-estimate_optimization]
```

estimate_fp_black_boxes

Sets the size of a black box based on an estimation of the objects that it will contain when replaced with real logic.

Equivalent Scheme command: `fphEstBlackBox`

```
status estimate_fp_black_boxes
[[{-sm_size size
  | -polygon {polygon_area}]
  | -sm_gate_equiv gate_count}]
[-sm_util util]
[-hard_macros names]
[-fixed_shape]
[-reset_shape]
black_boxes
```

estimate_rc

Estimates RC coefficients based on annotated data.

```
status estimate_rc
[-bound max_float_capacitance]
[-min]
[-net net_list]
[-nworst_nets percentage]
[-threshold min_float_capacitance]
```

exit

Terminates the application.

```
string exit
[exit_code]
```

expand_flip_chip_cell_locations

Pushes flip-chip bump or driver cells away proportionally or pulls them closer according to a specified ratio.

Equivalent Scheme command:

```
aprCmdEnlargeFC
```

```
status expand_flip_chip_cell_locations
-flip_chip_cells cell_list
-expand_ratio ratio
```

expand_objects

Expands one or more objects by moving each side out until it hits another object or the core boundary (number of sides retained) or make object fill available space around it (number of sides is not retained)

```
status expand_objects
[-side {left | right | top | bottom | all}]
[-fill]
[-offset real]
[-hit_types string_list]
[-ignore_fixed]
objects
```

explore_power_switch

Explores and estimates the placement of MTCMOS header or footer cells based on IR drop.

```
status explore_power_switch
-lib_cells lib_cells_or_power_switches
-real_pg_net real_pg_net_name
-virtual_pg_net virtual_pg_net_name
[-header]
[-bounding_box bounding_box]
[-x_increment {x_inc_list}]
[-y_increment {y_inc_list}]
[-orientation {N | W | S | E | FN | FE | FS |
FW}]
[-voltage_area voltage_area]
[-no_placement]
[-legalize_placement]
[-no_pns]
[-run_pns_script file_name]
[-design hierarchy_name]
[-save_placement prefix]
[-preroute_mode_real_pg_port {rail | tie |
net}]
[-no_preroute_real_pg_port]
[-preroute_mode_virtual_pg_port {rail | tie
| net}]
[-no_preroute_virtual_pg_port]
```

extract_blockage_pin_via

Extracts blockage, pin, and via information of child library cells.

Equivalent Scheme command:

auExtractBlockagePinVia

```
status extract_blockage_pin_via
-library_name library_name
-cell_name cell_name
[-generate_boundary collection_of_sides]
[-cell_types collection_of_cell_types]
[-preserve_all_metal_blockage]
[-routing_blockage_output_layer metBlk |
rGuide | zeroG]
[-treat_all_blockage_as_thin_wire]
[-treat_metal_blockage_as_thin
collection_of_layers]
[-extract_pin_connectivity_through
collection_of_layers]
[-poly_pin_text_layers list_of_layers]
[-m1_pin_text_layers list_of_layers]
[-m2_pin_text_layers list_of_layers]
[-m3_pin_text_layers list_of_layers]
[-m4_pin_text_layers list_of_layers]
[-m5_pin_text_layers list_of_layers]
[-m6_pin_text_layers list_of_layers]
[-m7_pin_text_layers list_of_layers]
[-m8_pin_text_layers list_of_layers]
[-m9_pin_text_layers list_of_layers]
[-m10_pin_text_layers list_of_layers]
[-m11_pin_text_layers list_of_layers]
[-m12_pin_text_layers list_of_layers]
[-m13_pin_text_layers list_of_layers]
[-m14_pin_text_layers list_of_layers]
[-m15_pin_text_layers list_of_layers]
[-pin_must_connect_area_layer_number {layer
number_name ...}]
[-auto_pin_must_connect_area_threshold
collection_of_layer_values]
[-skip_rotated_via_region]
[-contact_selections
collection_of_contactCode_numbers]
```

extract_flcc_hotspot

Performs lithography hot spot extraction (model-based). FLCC stands for Fast Lithography Compliance Check.

```
extract_flcc_hotspot
[-cell_name
```

extract_fp_rail_to_constraints

Extracts existing power network structure to a file with a set of power network synthesis constraints. The file can be used to recreate a power network rgat is the same as the existing one.

```
status extract_fp_rail_to_constraints
[-power_net power_net_name]
[-output_file output_file_name]
[-ground_net ground_net_name]
[-rail_type type]
[-ignore_layers layer_names]
[-preroute_script script_file_name]
```

extract_fp_relative_location

Extracts relative location constraints from the current placement.

```
status extract_fp_relative_location
[-target_cells cells]
[-target_corner bl | br | tl | tr]
[-anchor_object object_name]
[-anchor_corner bl | br | tl | tr]
[-output_file file_name]
```

extract_hier_antenna_property

Extracts the hierarchical antenna properties of all the top-level ports in the given cell.

Equivalent Scheme command:

```
axComputeHierAntennaProp
```

```
integer extract_hier_antenna_property
[-cell_name cell_name]
```

extract_rc

Executes 2.5D extraction for routes in a design.

```
status extract_rc
[-coupling_cap]
[-estimate]
[-routed_nets_only]
```

extract_rp_group

Extracts a relative placement group from your design based on your specifying either a collection of cells or a bounding box.

```
status extract_rp_group
-group_name group_name
[-rows number_of_rows]
[-columns number_of_columns]
[-output file_name]
[-append]
[-physical]
[-nosplit]
[-objects object_list]
[-coordinates coordinate_list]
[-apply]
[-descending]
```

extract_zrt_hier_antenna_property

Extracts the hierarchical antenna properties of all the top-level ports in the specified cell. You should use this command for designs routed with Zroute.

```
status extract_zrt_hier_antenna_property
-cell_name cell_name
```

filter_collection

Filters a collection, resulting in a new collection. The base collection remains unchanged.

```
collection filter_collection
base_collection
expression
[-regexp [-nocase]]
```

fix_flcc_hotspot

Performs lithography hot spot fixing. FLCC stands for Fast Lithography Compliance Check.

```
fix_flcc_hotspot
```

fix_isolated_via

Fixes isolated via violations by inserting hang-on vias in specified range.

```
integer fix_isolated_via
[-isolated_via_spacing distance]
[-isolated_via_quadrant_spacing distance]
```

fix_lcc_hotspot

Performs lithography compliance check (LCC) hotspot fixing.

```
status fix_lcc_hotspot
-lcc_file_path lcc_path_name
[-types list_of_types]
[-level level]
[-num_loops number_of_loops]
[-num_cpus number_of_cpus]
```

flatten_clock_gating

Restructures integrated clock gating (ICG) cells to flatten the hierarchy of the clock tree for clock mesh creation.

```
status flatten_clock_gating
-icgs cells
  | -mesh_nets nets
  | -clocks clocks
[-max_depth positive_integer]
[-optimize]
```

flatten_fp_black_boxes

Flattens objects to remove them from the physical cell and restore them to hierarchy preservation (logical view).

Equivalent Scheme command:

```
fphFlattenBlackBoxes
```

```
status flatten_fp_black_boxes
black_boxes
```

flatten_fp_hierarchy

Removes a level of hierarchy.

Equivalent Scheme command: `axgHierPlan`

```
int flatten_fp_hierarchy
cell_list
[-input_sdc_file input_file_name]
[-output_sdc_file output_file_name]
[-load_back_sdc]
[-prefix prefix_name]
[-simple_name]
[-no_backslash_for_hierarchy_delimiter]
```

flip_mim

Flips the cell placement in a multiple instantiated module (MIM) plan group.

```
status flip_mim
[-direction X | Y]
collection
```

flip_objects

Flips one or more movable objects.

```
status flip_objects
[-anchor anchor_point]
[-direction x | y | -x float | -y float]
[-flip_transform]
[-ignore_fixed]
objects
```

focal_opt

Performs postroute optimization to fix setup, hold, or logical design rule constraint (DRC) violations on the design. The selected optimization is referred to as the *focal metric*.

```
status focal_opt
-setup_endpoints all | file_name
 | -hold_endpoints all | file_name
 | -drc_nets all | file_name
[-effort medium | high]
[-size_only_mode density | in_place |
footprint]
[-prioritize]
```

foreach

Specifies the control structure for list traversal loop execution.

foreach_in_collection

Iterates over the elements of a collection.

Equivalent Scheme command: `db_foreach`

```
string foreach_in_collection
itr_var
collections
body
```

generate_qtm_model

Generate Quick Timing Model (QTM) from design CEL view.

```
string generate_qtm_model
[-block name_list]
-clock_definitions
filename_or_cellname_filename_pairs
[-directory directory_name]
```

get_adjusted_endpoints

Creates a collection of endpoints that have been adjusted in feasibility mode.

```
status get_adjusted_endpoints
[-zero_path]
[-zero_wire_load]
[-io]
[-slack_threshold]
[-all]
[-scenarios scenarios]
```

get_alternative_lib_cells

Creates a collection of equivalent library cells from loaded libraries, for a given cell or library cell. This collection can be used to replace or resize a specified cell in the current design. You can assign these library cells to a variable or pass them into another command.

```
string get_alternative_lib_cells
[-quiet]
[-regexp [-nocase]]
[-exact]
[-filter expression]
[-library libraries]
pattern_or_objects
```

get_always_on_logic

Returns a collection of cells and nets on always-on paths in the design.

```
collection get_always_on_logic
[-cells]
[-nets]
[-all]
```

get_app_var

Gets the value of an application variable.

```
string get_app_var
[-default | -details | -list]
[-only_changed_vars]
var
```

get_attribute

Returns the value of an attribute on an object.

Equivalent Scheme command:

```
dbFetchObjectField
```

```
string get_attribute
[-class class_name]
[-quiet]
object_spec
attribute_name
```

get_bounds

Creates a collection of bounds from the current design.

```
collection get_bounds
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-filter expression]
patterns | -of_objects objects
```

get_buffers

Creates a collection of buffer cells from the libraries loaded in memory.

```
collection get_buffers
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-inverter]
[-inverting_buffers]
[-library lib_spec]
patterns
```

get_cell_sites

Creates a collection of cell sites from the current design.

```
collection get_cell_sites
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-filter expression]
patterns
```

get_cells

Creates a collection of cells that match certain criteria.

Equivalent Scheme command:

```
dbGetCellInstByName
```

```
collection get_cells
[-hierarchical]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-filter expression]
[patterns
 | -of_objects objects
 | -object_id object_id
 | -within region
 | -intersect region
 | -touching region
 | -at point]
[-all]
[-design_id design_id]
[-hsc separator]
```

get_clocks

Creates a collection of clocks from the current design.

```
collection get_clocks
[-quiet]
[-regexp]
[-nocase]
[-filter expression]
patterns
```

get_command_option_values

Queries current/default option values.

```
get_command_option_values
[-default | -current]
-command command_name
```

get_core_area

Creates a collection containing the core area of the current design.

```
collection get_core_area
```

get_coupling_capacitors

Reports coupling capacitors for the given net.

```
int get_coupling_capacitors
[-min]
net
```

get_cts_scenario

Returns the name of the clock tree synthesis scenario or the empty string if a clock tree synthesis scenario is not defined.

```
string get_cts_scenario
```

get_design_lib_path

Returns the directory to which the specified library is mapped.

```
status get_design_lib_path
library_name
```

get_designs

Creates a collection of one or more designs loaded into the tool.

```
collection get_designs
[-hierarchical]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-filter expression]
patterns
```

get_die_area

Creates a collection containing the die area of the current design.

```
collection get_die_area
```

get_dominant_scenarios

Returns a list of dominant scenarios.

```
list get_dominant_scenarios
[-scenarios scenario_list]
[-distributed]
[-setup_distributed]
[-run_distributed]
[-process_distributed]
```

get_drc_errors

Return a collection of errors matching given criteria.

```
status get_drc_errors
[-error_view mw_error_view]
[-error_id error_id]
[-type error_type]
[-bbox area]
[-quiet]
[-nocase]
[-exact]
[-regexp]
[-filter expression]
```

get_edit_groups

Gets a collection of edit groups.

```
collection get_edit_groups
[-filter expression]
[-of_objects collection]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-object_id string]
[-design_id string]
[patterns]
```

get_error_view_property

Return error view property value.

```
string get_error_view_property
-writer
  | -version
  | -ignore_type_name_property
  | -run_set
  | -areas
  | -excluded_areas
  | -command
[-error_view mw_error_view]
```

get_flat_cells

Creates a collection of leaf cells that match certain criteria in the current design.

```
collection get_flat_cells
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-filter expression]
patterns
  | -of_objects objects
  | -object_id object_id
[-all]
```

get_flat_nets

Creates a collection of top nets of hierarchical net groups and meet the specifed criteria in the current design.

```
collection get_flat_nets
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
patterns
  | -of_objects objects
  | -object_id object_id
[-all]
```

get_flat_pins

Creates a collection of pins of leaf cells that match the specified criteria in the current design.

```
collection get_flat_pins
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
patterns
  | -of_objects objects
  | -object_id object_id
[-all]
```

get_floorplan_data

Returns the value of the specified floorplan data attribute on the specified module.

```
string get_floorplan_data
-module module_object
[-view one_level | logical | physical]
[-quiet]
attribute_name
```

get_fp_trace_mode

Determines whether a design is in trace mode.

```
int get_fp_trace_mode
```

get_fp_wirelength

Calculates the virtual route wirelength as a minimum length needed to connect all pins.

Equivalent Scheme command:

```
fphEstimateWirelength
```

```
status get_fp_wirelength
[-specified_nets object_list
  | -internal_nets
  | -interface_nets]
```

get_generated_clocks

Creates a collection of generated clocks.

```
collection get_generated_clocks
[-quiet]
[-regexp]
[-nocase]
[-filter expression]
[-exact]
patterns
```

get_ilm_objects

Returns a collection of nets, cells, or pins that are part of the interface logic models for the current design.

```
collection get_ilm_objects
[-type net | pin | cell]
```

get_ilms

Creates a collection of interface logic models (ILMs) defined in the current design.

```
collection get_ilms
[-quiet]
[-reference]
[-filter expression]
patterns
```

get_layer_attribute

Queries layer attribute.

Equivalent Scheme command:

```
dbFetchLayerInfo
```

```
string get_layer_attribute
[-quiet]
[-layer layer]
[attribute]
```

get_layers

Creates a collection of one or more layers.

Equivalent Scheme command:
`dbFetchLayerIdList`

```
collection get_layers
[-filter expression]
[-quiet]
[-regexp [-nocase]] | [-exact]
[-include_system]
[patterns]
[-exact]
```

get_lib_attribute

Returns the value of an attribute on a list of library objects.

```
list get_lib_attribute
object_list
attribute_name
```

get_lib_cells

Creates a collection of library cells from the libraries loaded into memory.

Equivalent Scheme command: `db_foreach`

```
collection get_lib_cells
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-scenario scenario_name]
[patterns]
[-of_objects objects]
```

get_lib_pins

Creates a collection of library cell pins from libraries loaded into memory.

Equivalent Scheme command: db_foreach

```
collection get_lib_pins
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
patterns | -of_objects objects
```

get_libs

Creates a collection of libraries loaded into memory.

Equivalent Scheme command: db_foreach

```
collection get_libs
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-scenario scenario_name]
[-of_objects objects]
[patterns]
```

get_license

Obtains a license for a feature.

```
status get_license
feature_list
```

get_location

Gets the location of the specified objects.

```
list get_location
object_list
[-rp_group rp_group]
```

get_magnet_cells

Returns a collection of cells that can be pulled closer to magnet cells. Magnet cells can be specified as an argument to this command.

```
collection get_magnet_cells
[-stop_by_sequential_cells]
[-exclude_buffers]
[-logical_level level]
[-stop_points object_list]
magnet_objects
```

get_message_info

Returns information about diagnostic messages.

```
Integer get_message_info
[-error_count | -warning_count | -info_count
|
-limit l_id
 | -occurrences o_id
 | -suppressed s_id]
```

get_mw_cels

Creates a collection of one or more Milkyway designs.

Equivalent Scheme command: `geShowCellList`

```
collection get_mw_cels
[-hierarchical]
[-quiet]
[-regexp [-nocase]] | [-exact]
[-filter expression]
patterns
[-exact]
```

get_net_shapes

Creates a collection by selecting net shapes from the current design.

Equivalent Scheme command: `geWindowSelect`

```
collection get_net_shapes
[-within region
 | -intersect region
 | -touching region
 | -at point]
[-filter expression]
[-quiet]
[-type {vw | hw | path}]
[patterns | -of_objects net_list]
```

get_nets

Creates a collection of nets that meet the specified criteria.

Equivalent Scheme command: `dbGetNetByName`

```
collection get_nets
[-hierarchical]
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-top_net_of_hierarchical_group]
[-segments]
[-boundary_type boundary_type]
patterns
 | -of_objects objects
 | -object_id object_id
[-all]
[-design_id design_id]
```

get_new_bounds

Creates a collection of bounds from the current design.

```
collection get_new_bounds
[-quiet]
[-within rectangle]
[-filter expression]
[patterns]
```

get_object_fixed_edit

Gets the fixed state for the specified objects.

```
fixed get_object_fixed_edit
objects
```

get_object_name

Returns the name of the object in a single-object collection.

```
string get_object_name
collection
```

get_object_snap_type

Returns the snap type for the specified object class.

```
string get_object_snap_type
-class object_class | -enabled
```

get_path_groups

Creates a collection of path groups from the current design.

```
collection get_path_groups
[-quiet]
[-regexp]
[-nocase]
[-filter expression]
patterns
```

get_physical_buses

Returns a collection of physical buses from the current design. You can assign these physical buses to a variable or pass them into another command.

```
collection get_physical_buses
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-filter expression]
patterns
  | -of_objects objects
  | -object_id id
```

get_physical_lib_cells

Creates a collection of library cells from libraries loaded into the tool.

```
collection get_physical_lib_cells
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
patterns | -of_objects objects
[-hsc separator]
```

get_physical_lib_pins

Creates a collection of library cell pins from libraries.

```
collection get_physical_lib_pins
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
patterns | -of_objects objects
[-hsc separator]
```

get_physical_libs

Creates a collection of libraries.

```
collection get_physical_libs
[-filter expression]
[-quiet]
[-regexp [-nocase]]
[-exact]
patterns | -of_objects objects
```

get_pin_guides

Retrieves a collection of pin guides existing in the current design.

```
collection get_pin_guides
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-object_id object_id]
[patterns]
```

get_pin_shapes

Creates a collection of pin shapes that matches the criteria.

```
collection get_pin_shapes
[-within region
 | -intersect region
 | -touching region
 | -at point]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-filter expression]
[patterns | -of_objects objects]
```

get_pins

Creates a collection of pins that match the specified criteria.

Equivalent Scheme command: `db_foreach`

```
collection get_pins
[-hierarchical]
[-filter expression]
[-quiet]
[-regexp [-nocase] | -exact]
[patterns
 | -of_objects objects [-leaf]
 | -object_id object_id]
[-all]
[-hsc separator]
```

get_placement_area

Returns a list of coordinates for the current core placement area.

```
string get_placement_area
```

get_placement_blockages

Creates a collection of placement blockages from the current design.

Equivalent Scheme commands:

```
fphDumpHierFP, geWindowSelect
```

```
collection get_placement_blockages
[-within rectangle | -touching rectangle]
[-filter expression]
[-quiet]
[-type hard | soft | pin | hard_macro |
partial]
[patterns]
```

get_plan_groups

Returns a collection of plan groups from the current design.

Equivalent Scheme commands:

```
dbGetPlanGroupByName,
dbGetPlangroupByName
```

```
collection get_plan_groups
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-filter expression]
patterns | -of_objects objects
```

get_polygon_area

Calculate the area of the input polygon.

```
double get_polygon_area
polygon
```

get_ports

Creates a collection of ports from the current design.

Equivalent Scheme command:

```
dbGetPortByName
```

```
collection get_ports
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-filter expression]
patterns
  | -of_objects objects
  | -object_id object_id
[-all]
```

get_power_domains

Creates a collection of power domains that meet the specified criteria.

UPF Mode

```
collection get_power_domains
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[[patterns] [-hierarchical] |
-of_objects objects]
```

Non-UPF Mode

```
collection get_power_domains
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[patterns | -of_objects objects]
```

get_power_switches

Creates a collection of power switches that meet the specified criteria. This command is supported only in UPF mode.

```
collection get_power_switches
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[patterns] [-hierarchical]
 | -of_objects objects]
```

get_route_guides

Creates a collection of route guides from the current design.

Equivalent Scheme command: `geWindowSelect`

```
collection get_route_guides
[-within rectangle | -touching rectangle]
[-filter expression]
[-quiet]
[patterns]
```

get_route_mode_options

Gets the mode value for running zroute.

```
status get_route_mode_options
[-zroute]
```

get_route_zrt_common_options

Gets the values of the specified common route options.

```
status get_route_zrt_common_options
[-name pattern]
```

get_route_zrt_detail_options

Gets the values of the specified droute options.

```
status get_route_zrt_detail_options
[-name pattern]
```

get_route_zrt_global_options

Gets the values of the specified groute options.

```
status get_route_zrt_global_options
[-name pattern]
```

get_route_zrt_track_options

Gets the values of the specified track assignment options.

```
status get_route_zrt_track_options
[-name pattern]
```

get_routing_blockages

Creates a collection of routing blockages from the current design.

```
collection get_routing_blockages
[-within rectangle
 | -intersect rectangle
 | -touching rectangle
 | -at point]
[-filter expression]
[-quiet]
[-type via | metal]
[patterns]
```

get_rp_group_keepouts

Creates a collection of the specified relative placement group keepouts.

```
collection get_rp_group_keepouts
[-quiet]
[patterns]
[-exact]
[-regexp]
[-filter expression]
[-of_objects objects]
```

get_rp_groups

Creates a collection of relative placement groups.

```
collection get_rp_groups
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-ignored]
[-top]
[-filter expression]
[patterns | -of_objects objects]
```

get_scan_cells_of_chain

Returns a collection containing all scan cells of the specified scan chain.

```
collection get_scan_cells_of_chain
-chain chain_name
```

get_scan_chains

Returns the number of scan chains in the current design.

Equivalent Scheme command:

```
dbDumpScanChain
```

```
status get_scan_chains
```

get_selection

Returns a collection containing the current selection in the GUI.

Equivalent Scheme command: `geWindowSelect`

```
collection get_selection
[-slct_targets target_selection_bus
[-slct_targets_operation operation]]
-create_slct_buses
[-name selection_bus]
[-type object_type]
[-design design]
[-more_than more]
[-fewer_than fewer]
[-count]
[-num num]
```

get_si_xtalk_bumps

Reports individual aggressor bumps for a given net.

```
status get_si_xtalk_bumps
net
```

get_site_rows

Returns a collection of site rows from the current design. You can assign these site rows to a variable or pass them into another command.

```
collection get_site_rows
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-filter expression]
patterns
 | -of_objects objects
 | -object_id id
```

get_supply_nets

Creates a collection of supply nets that meet the specified criteria. This command is supported only in UPF mode.

```
collection get_supply_nets
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[[patterns] [-hierarchical]
 | -of_objects objects]]
```

get_supply_ports

Creates a collection of supply ports that meet the specified criteria. This command is supported only in UPF mode.

```
collection get_supply_ports
[-filter expression]
[-quiet]
[-regexp [-nocase]]
[-exact]
[[patterns]
[-hierarchical] | -of_objects objects]
```

get_terminals

Creates a collection by selecting terminals from the current design.

Equivalent Scheme command: `dbGetPinByName`

```
collection get_terminals
[patterns
 | -of_objects port_list
 | -object_id object_id]
[-within region
 | -intersect region
 | -touching region
 | -at point]
[-filter expression]
[-regexp [-nocase] | -exact]
[-quiet]
```

get_text

Creates a collection of text from the current design.

Equivalent Scheme command: `dbFetchObject`

```
collection get_text
[-within rectangle
 | -intersect rectangle
 | -touching rectangle
 | -at point]
[-filter expression]
[-quiet]
[patterns]
```

get_timing_paths

Creates a collection of timing paths for custom reporting and other processing.

```
collection get_timing_paths
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]
[-rise_through rise_through_list]
[-fall_through fall_through_list]
[-delay_type delay_type]
[-nworst paths_per_endpoint]
[-max_paths max_path_count]
[-enable_preset_clear_arcs]
[-group group_name]
[-true [-true_threshold path_delay]]
[-slack_greater_than greater_slack_limit]
[-slack_lesser_than lesser_slack_limit]
[-greater greater_limit]
[-lesser lesser_limit]
[-include_hierarchical_pins]
[-path_type full_clock_expanded | full]
```

get_tracks

Creates a collection of tracks from the current design. You can assign the return value to a variable or pass it to another command (i.e get_attribute or report_attributes).

```
collection_handle get_tracks
[-within rectangle | -intersect rectangle
 | -at at_point | -touching rectangle]
[-filter expression]
[patterns | -of_objects layers]
[-quiet]
```

get_unix_variable

This is a synonym for the getenv command.

get_user_grid

Gets the user grid for this session.

```
status get_user_grid
[design]
```

get_user_shapes

Creates a collection of one or more user shapes.

Equivalent Scheme command: `db_foreach`

```
collection get_user_shapes
[-filter expression]
[-quiet]
[-regexp [-nocase] | -exact]
[-within region
 | -intersect region
 | -touching region]
[patterns]
```

get_via_masters

Returns a name list of contact codes (via masters) defined in the current library.

Equivalent Scheme command: `dbFetchObject`

```
status get_via_masters
[-of_objects via_list]
-cut_layer cut_layer
-up_layer upper_layer
-low_layer lower_layer
patterns
```

get_vias

Creates a collection by selecting vias from the current design.

Equivalent Scheme command:
`dbFetchContactNames`

```
collection get_vias
[-within region
 | -intersect region
 | -touching region
 | -at point]
[-filter expression]
[-of_objects net_list]
[-quiet]
[patterns]
```

get_voltage_areas

Creates a collection of voltage areas from the current design.

Equivalent Scheme command: `geWindowSelect`

```
collection get_voltage_areas
[-quiet]
[-regexp [-nocase] | -exact]]
[-filter expression]
patterns | -of_objects cell_list
```

get_zero_interconnect_delay_mode

Reports whether or not the timer is currently using zero interconnect delay mode.

```
status get_zero_interconnect_delay_mode
```

get_zrt_net_properties

Gets the value of specified property for a net.

```
status get_zrt_net_properties
-net net_name
-property property_name
```

getenv

Returns the value of a system environment variable.

```
string getenv
variable_name
```

group

Creates a new level of hierarchy.

```
status group
[cell_list | -logic | -pla | -fsm]
[-soft
 | -hdl_block block_name
 | -hdl_all_blocks
 | -hdl_bussed]
[-design_name design_name]
[-cell_name cell_name]
[-except exclude_list]
```

group_path

Groups a set of paths for cost function calculations.

```
int group_path
[-weight weight_value]
[-critical_range range_value]
-default | -name group_name
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]
[-rise_through rise_through_list]
[-fall_through fall_through_list]
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
```

gui_bin

Bin a collection

```
string gui_bin -clct Clct
[-attr Attr]
[-cmd Cmd]
[-lower_bound LBound]
[-lower_bound_strict]
[-upper_bound UBound]
[-upper_bound_strict]
[-boundary Boundary]
[-num_bins numBins]
[-bin_range inRange]
[-underflow]
[-overflow]
[-nice_level niceLevel]
[-small_is_good]
[-exact_binning]
[-ignore_values ignoreList]
[-bar_brush brushPattern]
[-create_slct_buses]
[-filter_cmd filterCmd]
[-numBin numBins]
[-return_values]
[-slct_targets slctTargets]
[-slct_targets_operation slctTargetOp]
[-value_list valList]
```

gui_change_highlight

Manipulate the set of globally highlighted objects.

```
string gui_change_highlight
[-add | -remove | -toggle]
[-color color_id | -all_colors]
[-collection clct]
```

gui_create_attrdef

Creates the user-defined attribute for the design objects.

```
status_value gui_create_attrdef
 -class design_object
 -name attribute_name
 -get_value_cmd get_value_tcl_command
 -clct_and_values
collection_and_values_list_pair
 [-set_value_cmd set_value_tcl_command]
 [-enum_list enum_list]
 [-model_kind model_name]
 [-type "int | double | boolean | string"]
 [-format format_string]
 [-display_name display_name]
 [-subtype "name | full_name"]
 [-width display_width]
 [-show | -hide]
 [-show_infotip | -hide_infotip]
 [-custom_edit_name custom_edit_name]
 [-custom_edit_args custom_edit_args]
 [-is_editable_cmd is_editable_tcl_command]
```

gui_create_attrgroup

Creates the group of attributes for the design object.

```
status_value gui_create_attrgroup
 -class design_object (name of design
object)
 -name name (attribute group name)
 [-model_kind model_name] (model kind, if
omitted - default model kind)
 [-attr_list {{attr_1}...{attr_n}}]
 (list of attributes)
```

gui_create_pref_category

Create a preference category.

```
string gui_create_pref_category -category
Category
```

gui_create_pref_key

Create a preference key.

```
string gui_create_pref_key -key Key
-value_type ValueType
-value Value
[-category Category]
```

gui_create_vm

Create new Visual Mode

```
string gui_create_vm -name identifier
[-update_cmd pdate_command]
[-tag tag]
[-title label]
[-infotip infotip]
```

gui_create_vm_objects

Create objects to hold annotations in visual modes

```
string gui_create_vm_objects <clct>
```

gui_create_vmbucket

Create new Visual Mode Bucket

```
string gui_create_vmbucket -vmname
mode_identifier
-name bucket_identifier
[-infotip infotip]
[-color color]
[-pattern pattern]
[-visible visibility]
[-title label]
[-collection handle]
[-above bucket_identifier | -below
bucket_identifier -at top|bottom]
```

gui_delete_attrdef

Deletes the user-defined attribute for the design objects.

```
status_value gui_delete_attrdef
 [-class design_object]
 [-model_kind model_name]
 [-name attribute_name]
 [-all]
```

gui_delete_attrgroup

Deletes the group of attributes for the design object.

```
status_value gui_delete_attrgroup
 -class design_object (name of design
object)
 -name name (attribute group name)
 [-model_kind model_name] (model kind, if
omitted - default model kind)
 [-all] (delete all groups)
```

gui_edit_vmbucket_contents

Edit the collection contents of a Visual Mode Bucket

```
string gui_edit_vmbucket_contents -vmname
mode_identifier
-name bucket_identifier
[-add | -remove | -replace]
[-collection handle]
```

gui_exist_pref_category

Check the existence of a preference category.

```
bool gui_exist_pref_category -category
Category
```

gui_exist_pref_key

Check the existence of a preference key.

```
bool gui_exist_pref_key -key Key
[-category Category]
```

gui_get_current_task

Get the name of the current task.

```
string gui_get_current_taskP
```

gui_get_highlight

Get a collection of highlighted objects.

```
string gui_get_highlight
[-color color_id | -all_colors]
```

gui_get_highlight_options

Query the options that control highlighting.

```
string gui_get_highlight_options
[-current_color | -all_colors |
-auto_cycle_color]
```

gui_get_pref_keys

Return a list of preference keys under the specified category.

```
string gui_get_pref_keys -category Category
```

gui_get_pref_value

Get the value of a preference key.

```
string gui_get_pref_value -key Key
[-category Category]
```

gui_get_setting

Gets a setting on the specified window.

```
string gui_get_setting
-window WindowID
-setting Setting
```

gui_get_current_task_list

List all available task names.

```
string gui_get_task_listP
```

gui_get_vm

Get attributes for Visual Mode

```
string gui_get_vm -name identifier
[-buckets]
[-tag]
[-title]
[-infotip]
[-discrete]
```

gui_get_vmbucket

Get attributes for Visual Mode Bucket

```
string gui_get_vmbucket -vmname
mode_identifier
-name bucket_identifier
[-infotip]
[-netfilter]
[-color]
[-pattern]
[-visible]
[-title]
[-collection]
```

gui_get_window_ids

Get a list of window ids

```
ids gui_get_window_ids
[ -parent window_id ]
[ -type window_type ]
```

gui_get_window_pref_categories

Get list of preference categories for object specified by window

```
categories gui_get_window_pref_categories
{ -window window_id | -window_type
window_type }
```

gui_get_window_pref_keys

Get list of preference categories for object specified by window

```
categories gui_get_window_pref_keys
{ -window window_id | -window_type
window_type }
[ -category category ]
```

gui_get_window_pref_value

Get preference value for object specified by window or window type

```
value gui_get_window_pref_value
{ -window window_id | -window_type
window_type }
[ -category category ]
-key key
```

gui_get_window_types

Get a list of window types

```
types gui_get_window_types
[ -type token ]
```

gui_list_attrdefs

Lists user-defined attributes.

```
status_value gui_list_attrdefs
 [-class design_object]
 [-model_kind model_name]
 [-name attrdef_name]
 [-all]
 [-tcl]
 [-full]
```

gui_list_attrgroup

Lists the group of attributes for the design object.

```
status_value gui_list_attrgroup
 -class design_object (name of design
object)
 -name name (attribute group name)
 [-model_kind model_name] (model kind, if
omitted - default model kind)
 [-all] (all object classes)
 [-tcl] (tcl output format)
 [-full] (full tcl output format)
 [-attr_list] (list attributes only)
```

gui_list_vm

List Current Visual Modes

```
string gui_list_vm
```

gui_load_cell_density_mm

Loads the data for cell density map mode.

```
status gui_load_cell_density_mm
[-area area]
```

gui_load_pin_density_mm

Loads the data for pin density map mode.

```
status gui_load_pin_density_mm
[-area area]
```

gui_remove_pref_key

Remove a preference key.

```
string gui_remove_pref_key -key Key
[-category Category]
```

gui_remove_vm

Remove Visual Mode

```
string gui_remove_vm -name identifier
```

gui_remove_vmbucket

Remove Visual Mode Bucket

```
string gui_remove_vmbucket -vmname
mode_identifier
[-name bucket_identifier]
[-all]
```

gui_set_current_task

Set current task to the given task.

```
string gui_set_current_task -name task_name
-name task_name
```

gui_set_highlight_options

Change the options that control highlighting.

```
string gui_set_highlight_options
[-current_color color_id | -next_color |
-auto_cycle_colors enable]
```

gui_set_pref_value

Set the value of a preference key.

```
string gui_set_pref_value -key Key -value
Value
[-category Category]
```

gui_set_setting

Sets a setting on the specified window.

```
gui_set_setting
-window WindowID
-setting Setting
-value Value
```

gui_set_vm

Set Visual Mode attributes

```
string gui_set_vm -name identifier
[-update_cmd pdate_command]
[-tag tag]
[-title label]
[-infotip infotip]
[-buckets uckets]
```

gui_set_vmbucket

Set attributes for Visual Mode Bucket

```
string gui_set_vmbucket -vmname
mode_identifier
-name bucket_identifier
[-infotip infotip]
[-color color]
[-pattern pattern]
[-visible visibility]
[-title label]
[-collection handle]
[-above bucket_identifier | -below
bucket_identifier | -at top|bottom]
```

gui_set_window_pref_key

Create a preference key owned by a particular window or window type

```
new_value gui_set_window_pref_key
{ -window window_id | -window_type
window_type }
[ -category category ]
-key key
-value_type value_type
-value value
```

gui_show_man_page

Show a man page in the man browser

```
string gui_show_man_page topic [-apropos]
```

gui_start

Starts the application GUI.

```
string gui_start
[-file name_of_script_file]
[-no_windows]
[-- x_args ...]
```

gui_stop

Stops the application GUI.

```
string gui_stop
```

gui_update_attrdef

Updates the user-defined attribute for the design objects.

```
status_value gui_update_attrdef
 -class design_object
 -name attribute_name
 [-get_value_cmd get_value_tcl_command]
 [-set_value_cmd set_value_tcl_command]
 [-enum_list enum_list]
 [-model_kind model_name]
 [-type "int | double | boolean | string"]
 [-format format_string]
 [-display_name display_name]
 [-subtype "name | full_name"]
 [-width display_width]
 [-show | -hide]
 [-show_infotip | -hide_infotip]
 [-custom_edit_name custom_edit_name]
 [-custom_edit_args custom_edit_args]
```

gui_update_attrgroup

Updates the group of attributes for the design object.

```
status_value gui_update_attrgroup
 -class design_object (name of design
object)
 -name name (attribute group name)
 [-model_kind model_name] (model kind, if
omitted - default model kind)
 [-attr_list {{attr_1}...{attr_n}}]
 (list of attributes)
 [-add] (add new attribute to the group)
 [-delete] (delete attribute from the group)
 [-move destination] (move attribute in the
list:
 Values: up, down, top, bottom, after,
 before)
 [-attr attribute] (single attribute)
 [-anchor attribute] (anchor attribute)
```

gui_update_pref_file

Save current application preferences to the user preference file.

```
string gui_update_pref_file [-file
FilePathName]
```

gui_update_vm

Update Visual Mode

```
string gui_update_vm -name identifier
```

gui_update_vm_annotations

Update visual mode annotaions

```
string gui_update_vm_annotations
-clear
-center
-add <points>
-draw_net <style>
[-type <shape>]
[-text <msg>]
[-color <color>]
[-pattern <pattern>]
[-line_style <line style>]
[-width <width>]
<obj>
```

help

Displays quick help for one or more commands.

```
string help
[-verbose] [-groups] [pattern]
```

history

Displays or modifies the commands recorded in the history list.

```
string history
[-h] [-r] [args...]
```

hookup_retention_register

Hooks up the save and restore pins of the retention registers to the save signal and the restore signal. This command is supported only in UPF mode.

```
status hookup_retention_register
```

identify_clock_gating

Identifies Power Compiler inserted clock-gating circuitry in a structural netlist.

```
integer identify_clock_gating
[-reset]
[-reset_only cell_or_pin_list]
[-gating_element gating_cell]
[-gated_element gated_cell_or_pin_list]
[-ungated_element ungated_cell_list]
```

if

Conditional execution control structure.

ignore_site_row

Indicates to ignore specified site rows or all site rows defined in the current design.

```
string ignore_site_row
[-row row_name]
[-site site_name]
```

import_designs

Imports one or more design files in Verilog or .ddc format.

Equivalent Scheme command:

```
auVerilogToCell
```

```
status import_designs
-format verilog | ddc
[-top design_name]
[-cell cell_filename]
[-rp_constraint tcl_script_file]
file_list
```

import_fp_black_boxes

Imports one or more black boxes from the hierarchy preservation information (logical view) into the physical cell.

Equivalent Scheme command:

```
fphImportBlackBoxes
```

```
status import_fp_black_boxes
[-max_count num_black_box]
[-side_length length
 | -gate_count gate_count | [-utilization
utilization]]
black_boxes
```

index_collection

Given a collection and an index, if the index is in range, extracts the object at that index and creates a new collection containing only that object. The base collection remains unchanged.

```
collection index_collection
collection1
index
```

initialize_floorplan

Produces a floorplan with chip boundary, core, rows, and wire tracks.

Equivalent Scheme command: `axgPlanner`

```
status initialize_floorplan
[-control_type aspect_ratio |
width_and_height | row_number | boundary]
[-core_aspect_ratio float]
[-core_utilization float]
[-row_core_ratio float]
[-core_width float]
[-core_height float]
[-number_rows int]
[-use_vertical_row]
[-no_double_back]
[-start_first_row]
[-flip_first_row]
[-left_io2core float]
[-right_io2core float]
[-bottom_io2core float]
[-top_io2core float]
[-keep_macro_place]
[-keep_std_cell_place]
[-min_pad_height]
[-pad_limit]
[-pin_snap]
[-keep_io_place]
```

initialize_rectilinear_block

Creates L-, T-, U-, and cross-shaped floorplans for rectilinear blocks.

Equivalent Scheme command:

```
axgRectiPlanner
```

```
status initialize_rectilinear_block
[-shape L | T | U | X]
[-control_type ratio | length]
[-core_side_dim {side_a_dim side_b_dim
side_c_dim side_d_dim [side_e_dim
side_f_dim]}]
[-use_current_boundary]
[-row_core_ratio ratio_type]
[-core_utilization ratio_type]
[-orientation N | W | S | E]
[-use_vertical_row]
[-no_double_back]
[-start_first_row]
[-flip_first_row]
[-left_io2core distance]
[-right_io2core distance]
[-top_io2core distance]
[-bottom_io2core distance]
[-keep_macro_place]
[-keep_std_cell_place]
[-keep_io_place]
```

insert_buffer

Inserts buffer cells on nets connected to specified pins.

```
collection insert_buffer
[-new_net_names new_net_names]
[-new_cell_names new_cell_names]
[-no_of_cells number]
[-inverter_pair]
[-repeater_distance distance_between
[-tolerance length]]
[-divide_load_by denominator
[-ignore_pin_cap]]
[-port_half_distance]
[-location coordinate_list]
[-on_route]
[-orientation orientation_list]
object_list
buffer_lib_cell
```

insert_diode

Inserts diodes into the design to fix antenna violations.

Equivalent Scheme command: `axgInsertDiode`

```
status insert_diode
[-nets collection_of_nets]
[-antenna_check_engine internal | hercules]
[-internal_check_option all |
top_layer_only]
[-no_auto_cell_selection]
[-diode_cells collection_of_diode_cells]
[-prefix prefix_name]
[-use_hierarchical_diode_instance_name]
[-same_row]
[[-dont_freeze_existing_placement]
 | [-routing skip |
when_all_violations_are_gone | always]]
[-signal_route_options ignore_lower_layers |
include_lower_layers |
include_all_lower_layers | advanced]
[-max_ratio max_ratio_number]
```

insert_isolation_cell

Inserts isolation cells on the specified nets, pins or ports. Isolation cell is a general term that applies to isolation (ISO) cells and enabled level-shifter (ELS) cells.

```
status insert_isolation_cell
[-force]
[-verbose]
-enable enable_signal
-object_list objects
-reference lib_cell_name
```

insert_level_shifters

Inserts appropriate level shifters in the current design.

Equivalent Scheme command:

`astInsertLevelShifter`

```
status insert_level_shifters
[-preserve]
[-all_clock_nets]
[-clock_net clock_name]
[-verbose]
```

insert_metal_filler

Fills an empty track with the metal wires to meet the metal density rules.

Equivalent Scheme command:

`axgFillWireTrack`

```
int insert_metal_filler
[-out self | cellview_name]
[-purge]
[-bounding_box {{llx lly} {urx ury}}]
[-dont_overwrite]
[-timing_driven]
[-insert_as_instance instance_name]
[-tie_to_net none | ground | net_name]
[-create_floating_vias]
[-floating_via_ftr_spacing]
[-routing_space route_space]
[-from_metal from_metal_number]
[-to_metal to_metal_number]
[-width {layer width}]
[-space {layer space_between_fills}]
[-min_length {layer min_length}]
[-max_length {layer max_length}]
[-space_to_route {layer
keep_from_metal_space}]
[-space_to_pg {layer
keep_from_pg_nets_space}]
[-stagger {layer}]
[-x_offset {layer x_distance}]
[-y_offset {layer y_distance}]
[-dont_snap_fill_to_track]
[-fill_poly]
[-distance_to_boundary
poly_to_cell_distance]
```

insert_ng_filler

Generates notch and gap filling information for filling notches and gaps that are smaller than the minimum distance required between objects of the same net on the same layer.

Equivalent Scheme command: `geNewFillNG`

```
int insert_ng_filler
[-include_existing_notch_gap_fill_cell]
[-skip_filling_child_cell]
[-dont_apply_fat_wire_rule]
[-dont_fill_corner_to_corner]
[-out outname]
[-notch_layer_data_type notch_datatype]
[-gap_layer_data_type gap_datatype]
[-layers layer_list]
```

insert_pad_filler

Fills gaps in the pad ring with instances of pad filler cells.

Equivalent Scheme commands:
`axgAddPadFiller, axgAddPadFillerByArea`

```
int insert_pad_filler
-cell lib_cells
[-overlap_cell overlap_lib_cells]
[-voltage_area voltage_area_list]
[-bounding_box rectangle]
[-prefix prefix]
[-no_left]
[-no_right]
[-no_bottom]
[-no_top]
```

insert_port_protection_diodes

Inserts diodes around the specified ports to protect them. One diode is added to each specified port.

```
status insert_port_protection_diodes
[-prefix name]
[-ignore_dont_touch ]
{-diode_cell lib_cell}
-port list
```

insert_redundant_vias

Replaces the specified single-cut vias with a multiple-cut via array. It can also replace a single via with another single via that has a different contact code.

Equivalent Scheme command:

```
axDrouteOptimizeContact
```

```
status insert_redundant_vias
-from_via list_of_from_vias
-to_via list_of_to_vias
[-to_via_x_size list_of_x-sizes]
[-to_via_y_size list_of_y-sizes]
[-via_array_no_swap]
[-optimize_level level_of_optimization]
[-num_cpus number_of_cpus]
[-auto_mode preview | insert]
```

insert_spare_cells

Inserts spare cells in the legalized design.

```
status insert_spare_cells
[-lib_cell lib_cell_name]
-cell_name prefix_name
[-num_instances number]
[-hier_cell hierarchy_name]
[-num_cells {lib_cell_name number}]
[-tie]
[-skip_legal]
```

insert_stdcell_filler

Fills empty spaces in standard cell rows with instances of master filler cells only.

Equivalent Scheme command:

`axgAddFillerCell`

```
status insert_stdcell_filler
[-cell_without_metal lib_cell_without_list]
[-cell_with_metal lib_cell_with_list]
[-bounding_box rectangle]
[-dont_respect_hard_placement_blockage]
[-dont_respect_soft_placement_blockage]
[-between_std_cells_only]
[-randomize]
[-respect_overlap]
[-cell_without_metal_prefix
cell_without_prefix]
[-cell_with_metal_prefix cell_with_prefix]
[-avoid_layers layers_list]
[-connect_to_power Power_net_name]
[-connect_to_ground Ground_net_name]
[-voltage_area voltage_area_list]
[-vt_filler lib_cell_list]
[-check_only]
[-restore_filler_snapshot]
[-vt_filler_prefix vt_filler_prefix]
[-respect_keepout]
```

insert_tap_cells_by_rules

Adds tap cells while meeting the maximum spacing design rule from the diffusion to the substrate or well contact.

```
status insert_tap_cells_by_rules
[-drc_spacing_check | -tap_cell_insertion]
[-tap_distance_based | -drc_spacing_based]
[-move | -freeze]
[-tap_master physical_lib_cell]
[-tap_layer layer_name]
[-tap_distance_limit distance]
[-n_well_layer layer_name]
[-p_well_layer layer_name]
[-contact_layer layer_name]
[-p_diffusion_layer layer_name]
[-n_diffusion_layer layer_name]
[-p_implant_layer layer_name]
[-n_implant_layer layer_name]
[-tap_spacing_design_rule distance]
[-tap_filler_name_identifier prefix]
[-ignore_hard_blockage]
[-ignore_soft_blockage]
[-ignore_double_back_sharing]
[-connect_to_power_net power_net]
[-connect_to_ground_net ground_net]
[-no_tap_cells_under_metal_layer
metal_layers_list]
[-voltage_area voltage_area_list]
[-respect_keepout]
```

insert_well_filler

Fills gaps between cells in the same row containing wells on the specified layer.

Equivalent Scheme command:

```
axgAddWellFiller
```

```
status insert_well_filler
-layer layer_name_or_number
[-ignore_PRboundary]
[-fill_gaps_smaller_than gap_size]
[-higher_edge min | max]
[-lower_edge min | max]
-gap_type {tt | bb | tb | bt}
[-respect_blockages]
[-row_overlap {row_overlap_value}]
[-min_gap {min_gap_distance}]
[-max_gap {max_gap_distance}]
[-enclosure_only width]
```

insert_zrt_redundant_vias

Replaces single-cut vias with multiple-cut via arrays. It can also replace a single-cut via with another single-cut via that has a different contact code.

```
status insert_zrt_redundant_vias
[-effort low | medium | high]
[-list_only]
[-timing_preserve_nets {collection_of_nets}]
[-timing_preserve_setup_slack_threshold
slack_value
[-timing_preserve_hold_slack_threshold
slack_value
```

is_false

Tests the value of a specified variable, and returns a 1 if the value is 0 or the case-insensitive string *false*; returns a 0 if the value is 1 or the case-insensitive string *true*.

```
int is_false
value
```

is_true

Tests the value of a specified variable, and returns a 1 if the value is 1 or the case-insensitive string *true*; returns a 0 if the value is 0 or the case-insensitive string *false*.

```
int is_true
value
```

is_zrt_routed_design

Checks if the current design is routed by Zroute.

```
int is_zrt_routed_design
```

legalize_fp_placement

Resolves standard cell placement conflicts after performing an initial placement.

Equivalent Scheme command:

```
fphLegalizePlacement
```

```
status legalize_fp_placement
```

legalize_placement

Executes detailed placement on a design.

```
status legalize_placement
[-effort low | medium | high]
[-check_only]
[-eco]
[-incremental]
[-cells cell_objects]
[-priority low | medium | high]
[-timing]
[-coordinates {llx1 lly1 urx1 ury1 ...}]
```

lib2saif

Creates a forward-annotation SAIF file for a specified technology library.

```
int lib2saif
[-output file_name]
library
[-lib_pathname lib_path_name]
```

license_users

Lists the current users of the Synopsys licensed features.

```
status license_users
[feature_list]
```

link

Resolves design references.

```
int link
[-force]
```

link_physical_library

Links the physical library with the logical library for physical synthesis.

```
int link_physical_library
```

list

Creates a list.

```
int list arg1 arg2 arg arg ...
```

list_attributes

Lists the currently defined attributes.

Equivalent Scheme command: `dbFetchObject`

```
string list_attributes
[-application]
[-class class_name]
[-nosplit]
```

list_designs

List the designs available in memory.

```
int list_designs
[design_list]
[-show_file]
```

list_drc_error_types

Lists error type names

```
list list_drc_error_types
[-error_view mw_error_view]
[-class type_class]
[-name type_name]
[-id]
```

list_files

Lists the files that are loaded into memory.

```
integer list_files
```

list_floorplan_data

Lists the currently defined floorplan data attribute names.

```
string list_floorplan_data
[-module top | child_cell | plan_group]
[-view one_level | logical | physical]
```

list_instances

Lists the instances in the current design or current instance.

```
int list_instances
[instance_list]
[-hierarchy]
[-max_levels num_levels]
[-full]
```

list_libs

Lists the libraries available in memory.

```
status list_libs
[lib_list]
```

list_licenses

Displays a list of licenses currently checked out by the user.

```
status list_licenses
```

list_mw_cels

Prints the list of Milkyway designs in the current Milkyway library.

Equivalent Scheme command: `geShowCellList`

```
status list_mw_cels
[-all_views]
[-all_versions]
[-sort]
```

list_partition_data

Queries a partition browser and returns data from it.

```
status list_partition_data
[-top_blocks]
[-IOs]
[-hard_macros]
[-missing_modules]
[-top_hard_macros]
[-sub_blocks]
[-area cells_only | boundary |
include_external_keepout]
[-power_ports]
[-ground_ports]
[-instance_count all | std_cells |
hard_macros | IOs | modules | missing |
black_box]
[-keepouts]
[-utilization]
[-tcl_output]
[-verbose]
[module_name_list]
```

lminus

Removes one or more named elements from a list and returns a new list.

```
list lminus
[-exact] the_list elements
```

load_fp_rail_map

Loads a voltage (IR) drop, electromigration (EM), resistance map or instance based voltage (IR) drop, power or power density map for display.

Equivalent Scheme command:

```
fphDisplayVoltageDropMap
```

```
status load_fp_rail_map
[-nets net_name]
[-instance]
[-type map_type]
[-min min_value]
[-max max_value]
[-directory directory_name]
[-clear]
```

load_of

Returns the capacitance of the specified library cell pin.

```
float load_of
library_cell_pin
```

load_upf

Reads a script in the Unified Power Format (UPF). This command is supported only in UPF mode.

```
status load_upf
upf_file_name
[-scope instance_name]
[-noecho]
```

ls

Lists the contents of a directory.

```
string ls [filename ...]
```

magnet_placement

Performs magnet placement. Pulls standard cells closer to macros and assigns legal locations.

Equivalent Scheme command: `astMagnetPlace`

```
int magnet_placement
[-move_fixed]
[-mark_fixed]
[-move_soft_fixed]
[-mark_soft_fixed]
[-avoid_soft_blockages]
[-stop_by_sequential_cells]
[-exclude_buffers]
[-logical_level level]
[-stop_points object_list]
[-align]
magnet_objects
```

man

Displays reference manual pages.

```
string man
topic
```

map_isolation_cell

Specifies how to map or remap the isolations and enable level-shifter cells belonging to the specified isolation strategy. This command is supported only in UPF mode.

```
status map_isolation_cell
isolation_strategy
-domain power_domain
-lib_cells lib_cells
```

map_level_shifter_cell

Specifies that the level-shifter cells belonging to the specified strategy can only be mapped to a subset of the library cells. This command is supported only in UPF mode.

```
status map_level_shifter_cell
level_shifter_strategy
-domain power_domain
-lib_cells lib_cells
```

map_power_switch

Defines which power switch library cells to use for the mapping of the given UPF power switch.

```
status map_power_switch
switch_name
-domain domain_name
-lib_cells list
```

map_retention_cell

Defines how to map the unmapped sequential cells to retention cells for the specified UPF retention strategy of the power domain. This command is supported only in UPF mode.

```
status map_retention_cell
retention_strategy
-domain power_domain
[-lib_cells lib_cells]
[-lib_cell_type lib_cell_type]
[-elements objects]
```

mark_clock_tree

Marks clock attributes on clock objects.

Equivalent Scheme command:

```
astMarkClockTree
```

```
status mark_clock_tree
[-clock_trees name_or_source_pin_list]
[-clock_synthesized]
[-fix_sinks]
[-clock_net]
[-ideal_net]
[-routing_rule
name_of_the_non_default_routing_rule]
[-use_default_routing_for_sinks n]
[-layer_list list_of_layer_names]
[-remove]
```

mem

Reports memory usage information.

```
int mem
[-all]
[-verbose]
```

merge_clock_gates

Merges multiple compatible clock gates into one.

```
status merge_clock_gates
[-verbose]
[-preview]
```

merge_flip_chip_nets

Merges the flip-chip nets into one net.

```
status merge_flip_chip_nets
-from from_nets
-to to_net
[-update_routing]
```

merge_fp_hierarchy

Creates a new level of hierarchy.

Equivalent Scheme command: `axgHierPlan`

```
int merge_fp_hierarchy
[-design_name design_name]
[-new_cell_name cell_name]
[-cells cell_list]
[-wrapper]
[-input_sdc_file input_file_name]
[-output_sdc_file output_file_name]
[-load_back_sdc]
[-no_port_merging]
```

merge_net_shapes

Merges a collection of net shapes and returns the collection of net shapes after merge.

```
collection merge_net_shapes
shape_collection
```

merge_saif

Reads a list of SAIF files with their corresponding weights, computes the merged toggle rate and static probability, and annotates the switching activity for nets, pins,and ports in the current design. The command then generates a merged output SAIF file.

```
integer merge_saif
-input_list saif_file_and_weight_list
-instance_name inst_name
[-output merged_saif_name]
[-simple_merge]
[-ignore ignore_name]
[-ignore_absolute ig_absolute_name]
[-exclude exclude_file_name]
[-exclude_absolute ex_absolute_file_name]
[-unit_base unit_value]
[-scale scale_value]
[-khrate khrate_value]
[-map_names]
[-rtl_direct]
[-strip_module annotated_instance_name]
```

move_mw_cel_origin

Moves the origin of a Milkyway design.

```
status move_mw_cel_origin
-to point
[mw_cel_list]
```

move_objects

Moves one or more objects to the specified location.

Equivalent Scheme command: `geMove, geMoveCell`

```
status move_objects
[-delta vector]
[-from point]
[-to point]
[-x real]
[-y real]
[-keep_placement]
[-keep_pad_to_core_distance]
[-ignore_fixed]
objects
```

move_pins_on_edge

Moves a set of pins along the side of a cell or macro.

Equivalent Scheme commands: `fphSnapSMPin, fphSnapSMPinToSMEdge`

```
status move_pins_on_edge
-distance real
[-overlap_policy overlap_policy_type]
[-layer_policy layer_policy_type]
pins
```

name_format

Specifies the name format for the isolation cells and level shifters.

```
status name_format
[-isolation_prefix name]
[-isolation_suffix name]
[-level_shift_prefix name]
[-level_shift_suffix name]
```

open_mw_cel

Opens a Milkyway design.

Equivalent Scheme command: `geOpenCell`

```
collection open_mw_cel
[-readonly]
[-library library]
[-version version]
[-not_as_current]
mw_cel_name
```

open_mw_lib

Opens a Milkyway library.

Equivalent Scheme command: `geOpenLib`

```
collection open_mw_lib
[-readonly | -write_ref]
mw_lib
```

optimize_clock_tree

Performs clock tree optimization.

Equivalent Scheme command: `astCTO`

```
status optimize_clock_tree
[-clock_trees clock_trees]
[-buffer_relocation]
[-buffer_sizing]
[-gate_relocation]
[-gate_sizing]
[-delay_insertion]
[-operating_condition min | max | min_max]
[-premesh]
[-postmesh]
[-mesh_net mesh_net_name]
[-routed_clock_stage none | global | track |
detail | detail_with_signal_routes]
[-search_repair_loop loop_number]
[-no_clock_eco_route]
```

optimize_dft

Performs placement-aware or clock-aware scan reordering.

```
status optimize_dft
[-clock_buffer]
[-plan_group]
```

optimize_flip_chip_route

Beautifies the flip-chip routing patterns.

```
status optimize_flip_chip_route
[-nets collection_of_nets
 | -nets_in_file nets_file]
[-layer tech_layer_number | layer_name]
[-change_route_type user_enter |
signal_route]
```

optimize_fp_timing

Performs timing optimization on the design.

Equivalent Scheme command: `fphOptimize`

```
status optimize_fp_timing
[-effort medium | high]
[-fix_design_rule]
[-area_recovery]
[-report_qor]
[-feedthrough_buffering_only]
```

optimize_netlist_hierarchy

Modifies the net-list tree structure contained in the input net-list in order to create physically partition-able hierarchy nodes in the top level such that the size of the nodes are relatively well-balanced while minimizing the number of top level nets that need to connect to hierarchy block interface.

```
status optimize_netlist_hierarchy
-netlist_files filelist
-top topName
[-opaque_modules modulelist]
[-max_partition_to_chip_ratio sizeRatio]
[-keep_top_hier modulelist]
[-hier_marker symbol]
[-max_hier_mod_depth Level]
[-max_num_nodes Count]
[-size_metric {simple | instcnt | area}]
[-filename string]
```

optimize_power_switch

Optimizes IR drop by sizing header and footer cells up or down.

```
status optimize_power_switch
-real_pg_net real_pg_net_name
-virtual_pg_net virtual_pg_net_name
[-lib_cell lib_cells_or_power_switches]
[-cells instances]
[-legalize_placement]
[-remove_preroute]
[-preroute_mode_real_pg_port rail | tie |
net]
[-no_preroute_real_pg_port]
```

optimize_pre_cts_power

Performs power optimization before the clock tree synthesis stage.

```
status optimize_pre_cts_power
[-operating_condition min | max(default) |
min_max]
[-update_clock_latency]
```

optimize_wire_via

Optimizes the routing to minimize wire length.

Equivalent Scheme command: `axgRoutOpt`

```
status optimize_wire_via
[-nets collection_of_nets]
[-exclude_nets collection_of_nets]
[-search_repair_loop num]
[-run_time_limit num]
[-num_cpus num]
```

order_rp_groups

Orders the relative placement groups created by the extract_rp_group command in a sequential manner.

```
int order_rp_groups
-group_name group_name
[-output file_name]
[-append]
[-nosplit]
[-apply]
rp_groups
```

pack_fp_macro_in_area

Automatically packs macros in the specified area.

Equivalent Scheme command:
`fphPackMacroInArea`

```
status pack_fp_macro_in_area
[-preferred_edges edge_string]
[-objects collection]
[-area list_of_points]
```

parse_proc_arguments

Parses the arguments passed into a Tcl procedure.

```
string parse_proc_arguments -args arg_list
result_array
```

place_flip_chip_array

Creates flip-chip bumps and places them in a two-dimensional matrix configuration.

Equivalent Scheme command: `fcArrayPlace`

```
status place_flip_chip_array
-physical_lib_cell {phy_lib_cels}
-prefix prefix
-start_point start_point
-number num_bump
-delta {x y}
-repeat {i j}
[-orientation N | W | S | E | FN | FE | FS |
FW]
[-cell_origin lower_left | center]
```

place_flip_chip_ring

Creates flip-chip bump cells and places them in a ring configuration.

Equivalent Scheme command: `fcRingPlace`

```
status place_flip_chip_ring
-physical_lib_cell {cell_name}
-prefix prefix
-number num_bump
-bump_spacing spacing
-ring_number ring_number
-ring_spacing ring_spacing
-boundary boundary_box
[-left_orientation N | W | S | E | FN | FS |
FW | FE]
[-stagger_offset offset]
[-extra_spacing extra_spacing]
[-num_extra_spacing num_extra]
```

place_fp_pins

Performs pin assignment for soft macros or at the block level.

Equivalent Scheme command: `fphAssignPins`

```
status place_fp_pins
[-block_level]
[-effort low | high]
[-verbose]
[soft_macros]
```

place_freeze_silicon

Automatically places new cell instances by swapping out spare cells. This command is typically used in a freeze silicon ECO flow.

Equivalent Scheme command:
`axgECOAutoPlaceFS`

```
status place_freeze_silicon
```

place_io_pads

Adjusts the placement of unconstrained pins and pads.

Equivalent Scheme command: `ioReplacePads`

```
status place_io_pads
[-io_style io_style | flipchip | center |
core | distribute | abut | old]
[-adjust_core no_change | macro_and_region |
offset_from_pads]
[-left_to_core double]
[-right_to_core double]
[-top_to_core double]
[-bottom_to_core double]
[-min_pad_height]
```

place_opt

Performs simultaneous placement, routing, and optimization on the design.

Equivalent Scheme commands: `astAutoPlace, astPostPS, astPrePS`

```
status place_opt
[-effort low | medium | high]
[-area_recovery]
[-optimize_dft]
[-congestion]
[-power]
[-cts]
[-num_cpus number_of_cpus]
```

preroute_instances

Connects pins in instances to power and ground targets.

Equivalent Scheme command:

```
axgPreRouteInstances
```

```
status preroute_instances
[-ignore_macros]
[-ignore_pads]
[-ignore_cover_cells]
[-consider_driver_cells]
[-connect_instances all_but_specified |
specified | specified]
[-cells {collection_of_cells}]
[-target_directions four_sides | vias_only |
vias_only]
[-skip_left_side]
[-skip_right_side]
[-skip_bottom_side]
[-skip_top_side]
[-skip_vias_to_lower_layer]
[-skip_vias_to_higher_layer]
[-select_net_by_type pg | tieup_and_tiedown
| pg_and_tieup_tiedown | specified |
tieup_and_tiedown | pg_and_tieup_tiedown |
specified]
[-nets {collection_of_nets}]
[-route_pins_on_layer layer_from_tech_file]
[-primary_routing_layer preferred | pin |
specified | pin | specified]
[-preferred_routing_layer high | low]
[-specified_horizontal_layer h_layer]
[-specified_vertical_layer v_layer]
[-pad_pin_to_pad_boundary distance
[-one_d_pin one_d_pin_dist]
[-boundary_pad_to_top_cell_boundary distance
[-macro_pin_to_macro_boundary distance
[-customize]
[-routing_width connection_width]
[-connect_to_pins_at center | low_end |
high_end | low_end | high_end]
[-offset pin_connection_offset]
[-extend_to_boundaries_and_generate_pins]
[-force_extend_to_boundaries_and_generate_
pins]
[-route_small_pins_using_wider_dimension]
[-route_boundary_coinciding_edges_only]
[-skip_pad_pins_touching_pad_side_
boundaries]
[-advanced_via_rules]
```

```
[-special_rules special_rules_name]
[-extend_for_multiple_connections]
[-extension_gap space_threshold]
[-undo]
```

preroute_standard_cells

Connects power and ground pins in the standard cells to the power and ground rings or straps, and connects power and ground rails in the standard cells.

Equivalent Scheme command:

```
axgPrerouteStandardCells
```

```
status preroute_standard_cells
[-mode rail | tie | net]
[-connect horizontal | vertical | both]
[-nets {collection_of_nets}]
[-route_pins_on_layer layer]
[-within {{llx lly} {urx ury}}]
[-no_routing_outside_working_area]
[-special_via_rule]
[-offset_both_sides_for_special_via]
[-special_via_x_offset distance]
[-special_via_y_offset distance]
[-special_via_x_size distance]
[-special_via_y_size distance]
[-special_via_x_step distance]
[-special_via_y_step distance]
[-advanced_via_rules]
[-skip_macro_pins]
[-skip_pad_pins]
[-remove_floating_pieces]
[-pin_width_by_extreme_edges]
[-pin_width_by_most_extended_pin]
[-tie_mode_max_route_width distance]
[-extend_to_boundaries_and_generate_pins]
[-force_extend_to_boundaries_and_generate_
pins]
[-avoid_merging_vias]
[-optimize_via_locations]
[-snap_shapes_to_tracks]
[-do_not_route_over_macros]
[-fill_empty_rows]
[-cut_out_empty_spans]
[-extend_for_multiple_connections]
[-extension_gap distance]
[-num_cpu int_number]
[-max_fanout int_number]
[-h_layer name_of_metal_layer]
```

```
[-v_layer name_of_metal_layer]
[-h_width distance]
[-v_width distance]
[-port_filter pattern]
[-cell_master_filter pattern]
[-cell_instance_filter pattern]
[-voltage_area_filter pattern]
[-port_filter_mode off | select | skip]
[-cell_master_filter_mode off | select |
skip]
[-cell_instance_filter_mode off | select |
skip]
[-voltage_area_filter_mode off | select |
skip]
[-undo]
```

print_message_info

Prints information about diagnostic messages which have occurred or have been limited.

```
string print_message_info
[-ids id_list] [-summary]
```

print_proc_new_vars

Check for new variables created within a Tcl procedure.

```
string print_proc_new_vars
```

print_suppressed_messages

Displays an alphabetical list of message ids that are currently suppressed.

```
string print_suppressed_messages
```

printenv

Prints the value of environment variables.

```
string printenv
[variable_name]
```

printvar

Prints the values of one or more variables.

```
string printvar
[pattern] [-user_defined] [-application]
```

proc_args

Displays the formal parameters of a procedure.

```
string proc_args
proc_name
```

proc_body

Displays the body of a procedure.

```
string proc_body
proc_name
```

process_particle_probability_file

Encrypts or decrypts the particle probability function file.

```
process_particle_probability_file
-key
-input_file
[-output_file ]
```

propagate_constraints

Propagates timing constraints from lower levels of the design hierarchy to the current design.

```
status propagate_constraints
[-design design_list]
[-all]
[-clocks]
[-disable_timing]
[-dont_apply]
[-false_path]
[-gate_clock]
[-ideal_network]
[-ignore_from_or_to_port_exceptions]
[-ignore_through_port_exceptions]
[-max_delay]
[-min_delay]
[-multicycle_path]
[-operating_conditions]
[-power_supply_data]
[-output file_name]
[-port_isolation]
[-verbose]
[-case_analysis]
[-target_library_subset]
```

propagate_ilm

Propagates specified information of the interface logic model (ILM) blocks to the top-level design.

```
status propagate_ilm
[-clock_mesh_annotation]
[-verbose]
[cell_list]
```

propagate_switching_activity

Forces a propagation of the power switching activity information.

```
int propagate_switching_activity
[-effort low | medium | high]
[-verbose]
[-infer_related_clocks]
```

psynopt

Performs incremental synthesis on the design.

Equivalent Scheme commands: `astAutoPlace, astPostPS, astPostPS1`

```
int psynopt
[-area_recovery]
[-only_area_recovery]
[-congestion]
[-no_design_rule | -only_design_rule]
[-only_hold_time]
[-in_place_size_only]
[-size_only]
[-on_route]
[-preserve_footprint]
[-use_annotation]
[-power]
[-only_power]
```

push_down_fp_objects

Transfers physical objects from the top level to the soft macro level.

Equivalent Scheme command: `fphCutPreRoute`

```
status push_down_fp_objects
[-object_type {routing | route_guides |
blockages | cells | rows | shapes}]
[-cut_type push_down | cut_down | copy_down]
[-no_overlap_checking]
[-connect_copy_down_wires]
[-wire_net_type {pg | clock | signal}]
[-freeze_push_down_nets]
[-allow_feedthroughs]
[-nets net_object_list]
[-partial_overlap]
[-row_offset_x int]
[-row_offset_y int]
[-include all | shapes_with_net_id |
shapes_without_net_id]
[soft_macros]
```

push_flip_chip_route

Pushes routed flip-chip wires either in a specified direction or away from the specified nets.

```
status push_flip_chip_route
-nets collection_of_nets
 | -nets_in_file nets_file
[-layer mX | MX | tech_layer_number]
[-direction up | down | left | right]
[-mode 1 | 2 | 3]
[-sweep_range sweep_range]
[-all]
```

push_up_fp_objects

Transfers physical objects from the soft macro level to the top level.

Equivalent Scheme command:
`fphRecoverPreroute, fphPushUp, fphDeleteSMCellRow`

```
status push_up_fp_objects
[-object_type {routing | pins | route_guides
| blockages | cells | rows}]
[-layers ayer_object_list]
[-to_object_type routing | terminals]
[-top_level_interface_nets net_object_list]
[-preserve_child_preroutes]
[-include pushed_down_objects_only | all]
[-child_object_names object_list]
[soft_macros]
[-ignore_not_push_down_nets]
```

pwd

Displays the pathname of the present working directory (pwd), also called the current directory.

```
string pwd
```

query_objects

Searches for and displays objects in the database.

Equivalent Scheme command: `geQueryObject`

```
string query_objects
[-verbose]
[-class class_name]
[-truncate elem_count]
object_spec
```

quit

Exits the shell.

```
string quit
```

quit!

Quits the application without posting an application exit dialog.

```
quit!
```

read_antenna_violation

The command is used to read antenna violation file to ICC.

```
int read_antenna_violation
[-format hercules]
[-file file_name]
```

read_ddc

Reads in one or more design files in .ddc (Synopsys logical database) format.

```
status read_ddc
file_names
[-scenarios scenario_list]
[-active_scenarios active_scenario_list]
```

read_def

Annotates the design with the data from a file in Design Exchange Format (DEF).

```
status read_def
[-check_only]
[-enforce_scaling]
[-no_incremental]
[-verbose]
[-turn_via_to_inst]
[-inexactly_matched_via_to_inst]
[-lef lef_file_names]
[-snet_no_shape_as_user_enter]
[-snet_no_shape_as_detail_route]
[-preserve_wire_ends]
def_file_names
```

read_drc_error_file

Creates an error cell from the given drc error file.

```
status read_drc_error_file
[-drc_type type]
[-error_cell cell_name]
drc_file
```

read_file

Reads designs or libraries into memory, or reads libraries into the shell.

```
list read_file
file_list
[-format format_name]
[-ilm]
[-single_file single_file_name]
[-scenarios scenario_list]
[-active_scenarios active_scenario_list]
```

read_flip_chip_bumps

Reads bump locations and connected nets from a file with the advanced input format (AIF).

Equivalent Scheme command: `fcRingPlace`

```
status read_flip_chip_bumps
-physical_lib_cell {phy_lib_cels}
[-orientation N | W | S | E | FN | FE | FS |
FW]
file_name
```

read_floorplan

Reads in a script that describes a floorplan into current Milkyway cel.

Equivalent Scheme command: `load`

```
int read_floorplan
file_name [-echo]
```

read_io_constraints

Reads I/O constraints into the specified design.

Equivalent Scheme commands: `axgLoadTDF`, `axgLoadTDFforChildCell`

```
status read_io_constraints
[-append]
[-cell name]
io_constraints_file
```

read_lib

Reads a technology library, physical library, or symbol library into the shell. Creates a physical library for GDSII.

```
int read_lib
[-format format_name]
[-symbol intermediate_symbol_library_file]
[-plibrary physical_library_output_file]
[-pplibrary pseudo_physical_file_name]
file_name
[-no_warnings]
[-names_file file_list]
[-test_model CTL_file_list]
[-html]
[-lib_message_var_name lib_msg_var_name]
```

read_mw_eco_list

Reads an ECO change file and performs ECO operations on Milkyway designs.

Equivalent Scheme command:

```
auHierECOByChangeFile
```

```
status read_mw_eco_list
[designcell_name]
[-library lib_name]
[-change_file change_filename]
[-explicit_uniq]
[-loose_name_match]
[-softmacro]
```

read_parasitics

Reads parasitics information from a disk file for the delay calculation tools.

```
int read_parasitics
[-format SPEF | SBPF]
[-syntax_only]
[-max_file max_file_name
[-min_file min_file_name]]
[-keep_capacitive_coupling]
[-triplet_type min | typ | max]
 | | [-eco]
[-ilm_context]
[file_list]
```

read_rail_maps

Reads rail map data from a map file.

```
status read_rail_maps
[-file file_name]
```

read_saif

Reads a SAIF file and annotates switching activity information on nets, pins, ports, and cells in the current design.

```
status read_saif
-input file_name
-instance_name name
[-target_instance instance]
[-ignore ignore_name]
[-ignore_absolute ig_absolute_name]
[-exclude exclude_file_name]
[-exclude_absolute ex_absolute_file_name]
[-names_file name_changes_log_file]
[-scale scale_value]
[-unit_base unit_value]
[-khrate khrate_value]
[-map_names]
[-auto_map_names]
[-rtl_direct]
[-verbose]
```

read_sdc

Reads in a script in Synopsys Design Constraints (SDC) format.

Equivalent Scheme commands: `ataLoadSDC`

```
status read_sdc
file_name
[-echo]
[-syntax_only]
[-version sdc_version]
```

read_sdf

Reads leaf cell and net timing information from a file in Standard Delay Format (SDF) and uses that information to annotate the current design.

```
string read_sdf
[-load_delay net | cell]
[-path path_name]
[-min_type sdf_min | sdf_typ | sdf_max]
[-max_type sdf_min | sdf_typ | sdf_max]
[-worst]
[-min_file min_sdf_file_name]
[-max_file max_sdf_file_name]
sdf_file_name
```

read_tdf_ports

Reads in a Top Design Format (TDF) file and translates the "pin" and "pad" to mpc constraints for ports in the floorplan in the mpc flows.

Equivalent Scheme command: `ioLoadTdf`

```
int read_tdf_ports
[TDF file]
-output string
-apply
-verbose
```

read_verilog

Reads in one or more design or library files in Verilog format.

```
status read_verilog
[-dirty_netlist]
[-allow_black_box]
[-verbose]
[-bus_direction_for_undefined_cell
connection | msb | lsb]
[-keep_module keep_module_list]
[-top top_module_name]
[-cell cell_name]
 | verilog_files
```

rebuild_mw_lib

Rebuilds the Milkyway library.

Equivalent Scheme commands: `dbRebuildLib`

```
status_value rebuild_mw_lib
libName
```

recover_tie_connection

Recover tie connection from direct PG implementation.

```
status recover_tie_connection
[-net pg_net_list]
[-cell cell_list]
[-hierarchy_based]
```

redirect

Redirects the output of a command to a file.

```
string redirect
[-append] [-tee] [-file
 | -variable
 | -channel] [-compress]
target
{command_string}
```

redo

Redoes last undo operation

```
status redo
[-all]
[-mark string]
```

reduce_fp_rail_stacked_via

Given a complete or partial power network, you can select a set of stacked vias in the power network for removal to reduce congestion. This command honors the specified voltage (IR) drop constraint and maintains power network connectivity. The layer-based global route congestion maps are required for this command. route_zrt_global, route_global or route_fp_proto can be used to create the congestion maps. The reduce_fp_rail_stacked_via command does not physically remove the selected stacked vias. Signal vias are not removed. Power network stacked vias in hard-macros or soft-macros are not removed. Power network stacked via reduction does not support running more than two nets at a time.

```
status reduce_fp_rail_stacked_via
-nets nets
[-power_budget power]
[-analyze_power]
[-lowest_voltage_drop]
[-target_voltage_drop target_voltage]
[-voltage_supply voltage]
[-effort low | medium | high]
[-pad_lib_cells pad_lib_cells]
[-read_pad_instance_file file_name]
[-read_pad_lib_cell_file file_name]
[-extract_stacked_via_only]
[-use_pins_as_pads]
[-top_level_only]
[-ignore_blockages]
[-ignore_conn_view_layers layer]
[-read_power_compiler_file file_name]
[-read_prime_power_file file_name]
[-read_default_power_file file_name]
[-output_directory directory_name]
```

refine_fp_macro_channels

Refines channels between macros to avoid congestion.

```
status refine_fp_macro_channels
```

refine_placement

Performs incremental placement with congestion optimization.

```
int refine_placement
[-congestion_effort low | medium | high]
[-perturbation_level min | medium | high |
max]
[-ignore_scan]
[-num_cpus number_of_cpus]
[-coordinate {X1 Y1 X2 Y2}]
```

remove_all_spacing_rules

Removes all inter-cell spacing rules from the current library.

```
status remove_all_spacing_rules
```

remove_annotated_check

Removes annotated timing check information.

```
int remove_annotated_check
-all | -from from_list | -to to_list
[-rise | -fall]
[-clock rise | fall]
[-setup] [-hold]
[-recovery] [-removal]
[-nochange_low] [-nochange_high]
```

remove_annotated_delay

Removes the annotated delay between two pins.

```
int remove_annotated_delay
-all
  | -cell_all
  | -net_all
  | -non_clock_cell_all
  | -non_clock_net_all
  | -from from_list
  | -to to_list
```

remove_annotated_transition

Removes the annotated transition at a pin.

```
int remove_annotated_transition
-all
```

remove_annotations

Removes all annotated information on the design.

```
status remove_annotations
```

remove_antenna_rules

Deletes all of the antenna rules stored in the library.

Equivalent Scheme command:
`dbClearLibAntennaRules`

```
status_value remove_antenna_rules
[mw_lib]
```

remove_attribute

Removes an attribute from the specified objects.

Equivalent Scheme command: `astSetDontUse`

```
collection remove_attribute
[-class class_name]
[-quiet]
object_list
attribute_name
```

remove_base_arrays

Removes base arrays from the current design.

Equivalent Scheme commands:
`axPurgeSingleRecordType, dbDeleteObject`

```
status_value remove_base_arrays
[-all | pattern]
```

remove_bounds

Removes bounds from the current design.

```
int remove_bounds
[-verbose]
[-all]
[-name bound_name_list]
objects
```

remove_buffer

Removes the buffer cells at a specified driver pin or net on a mapped design.

```
status remove_buffer
-from start_point
-net net_list
[-to end_point_list]
[-level integer]
cell_list
```

remove_buffer_tree

Removes the buffer tree at a given driver pin.

Equivalent Scheme commands:

```
pdsHFNCollapse, pdsHFNCollapseNet
```

```
int remove_buffer_tree
[-from pin_or_net_list]
[-verbose]
[-all]
```

remove_bus

Removes a port bus or net bus.

```
status remove_bus
object_list
```

remove_case_analysis

Removes the case analysis value from the specified input ports or pins.

```
string remove_case_analysis
port_or_pin_list | -all
```

remove_cell

Removes cells from the current design.

Equivalent Scheme command:

```
dbPurgeCellInstMaster,
```

```
status remove_cell
cell_list | -all
```

remove_cell_degradation

Removes the cell_degradation attribute on specified ports or designs.

```
int remove_cell_degradation
object_list
```

remove_cell_sites

Deletes the specified cell sites.

```
status remove_cell_sites
-all | cell_sites
```

remove_cell_vt_type

removes voltage threshold type of a library cell or all cells of a library. Voltage threshold type is used for mixed voltage threshold filler cell insertion

```
integer remove_cell_vt_type
-library library_name | -lib_cell cell_name
```

remove_checkpoint_designs

Remove checkpoint designs created preroute optimization commands

```
int remove_checkpoint_designs
[-command command]
```

remove_clock

Removes clocks from the current design.

```
int remove_clock
clock_list | -all
```

remove_clock_gates

Identifies and removes clock-gating cells according to the specified option.

```
status remove_clock_gates
[-gated_registers gated_register_list]
[-min_bitwidth minsize_value]
[-gating_cells clock_gating_cells_list]
```

remove_clock_gating_check

Removes setup and hold checks from the specified clock gating cells.

```
int remove_clock_gating_check
[-setup]
[-hold]
[-rise]
[-fall]
object_list
```

remove_clock_groups

Removes specific exclusive or asynchronous clock groups from the current design.

```
status remove_clock_groups
-logically_exclusive
  | -asynchronous
  | -physically_exclusive
name_list | -all
```

remove_clock_latency

Removes clock latency information from the specified objects.

```
string remove_clock_latency
[-fall]
[-min]
[-max]
[-source]
[-early]
[-late]
object_list
[-rise]
```

remove_clock_mesh

Removes the premesh tree, clock mesh or the postmesh tree routes and/or logical connections based on the options specified.

```
status remove_clock_mesh
[-premesh]
[-clockmesh]
[-postmesh]
[-route_only]
[-clock_tree ]
```

remove_clock_sense

Removes clock sense information from the specified pins.

```
integer remove_clock_sense
[-all]
[-clocks clock_list]
pins
```

remove_clock_transition

Removes clock transition attributes on the specified clock objects.

```
int remove_clock_transition
clock_list
```

remove_clock_tree

Removes buffers and inverters from the clock tree.

Equivalent Scheme command:

```
astDeleteClockTree
```

```
status remove_clock_tree
[-clock_trees name_or_source_pin_list]
[-honor_dont_touch]
[-synopsys_only]
[-high_fanout_net net_or_pin_list]
```

remove_clock_tree_exceptions

Removes the specified clock tree exceptions, which were previously set with the set_clock_tree_exceptions command.

```
status remove_clock_tree_exceptions
[-all]
[-float_pins float_pin_collection]
[-stop_pins stop_pin_collection]
[-non_stop_pins non_stop_pin_collection]
[-exclude_pins exclude_pin_collection]
[-dont_touch_subtrees dts_pin_collection]
[-dont_buffer_nets
collection_or_list_of_nets]
[-dont_size_cells
collection_or_list_of_cells]
[-size_only_cells
collection_or_list_of_cells]
[-float_pin_logic_level]
[-preserve_hierarchy
collection_of_pin_or_cells]
[-clocks object_list]
```

remove_clock_tree_options

Removes clock tree objects from database.

```
void remove_clock_tree_options
[-clock_trees name_or_source_pin_list]
```

remove_clock_uncertainty

Removes clock uncertainty information previously set by the set_clock_uncertainty command.

```
string remove_clock_uncertainty
[object_list
 | -from from_clock
 | -rise_from rise_from_clock
 | -fall_from fall_from_clock
-to to_clock
 | -rise_to rise_to_clock
 | -fall_to fall_to_clock]
[-rise]
[-fall]
[-setup]
[-hold]
```

remove_congestion_options

Removes congestion options from the current design.

```
int remove_congestion_options
[-all] id_list
```

remove_cts_scenario

Removes the current CTS scenario setting. This command doesn't remove the scenario itself, it only removes the CTS scenario setting.

```
Boolean remove_cts_scenario
```

remove_dangling_wires

Removes dangling wires and vias on specified nets, except for power and ground nets and those with short or open violations.

```
integer remove_dangling_wires
[-nets {collection_of_nets}]
[-route_types {list_of_route_types}]
[-layers {collection_of_layers}]
[-no_rerun_drc]
```

remove_data_check

Removes specified data-to-data checks previously set by set_data_check.

```
string remove_data_check
-from from_object
 | -rise_from from_object
 | -fall_from from_object
-to to_object
 | -rise_to to_object
 | -fall_to to_object
[-setup | -hold]
[-clock clock]
```

remove_design

Removes a list of designs or libraries from memory.

```
status remove_design
[design_list | -designs | -all]
[-hierarchy] [-quiet]
```

remove_diode

deletes the diode cells

Equivalent Scheme command: `axgDeleteDiode`

```
integer remove_diode
[-cells diode_cell_name]
-nets collection_of_nets
[-all_clock_net]
[-dangling_wires]
```

remove_disable_clock_gating_check

For specified cells and pins, restores clock gating checks previously disabled by the set_disable_clock_gating_check command.

```
string remove_disable_clock_gating_check
object_list
```

remove_disable_timing

Enable previously user-disabled timing arcs in the current design. It is an equivalent to set_disable_timing -restore.

```
int remove_disable_timing
object_list
[-from from_pin_name -to to_pin_name]
[-all_loop_breaking]
```

remove_distributed_hosts

Remove all the hosts added to the distributed hosts list.

```
int remove_distributed_hosts
```

remove_distributed_route

Terminates a job.

Equivalent Scheme command: `jpKillJob`

```
integer remove_distributed_route
-job jobId
```

remove_dont_touch_placement

Removes the restriction of fixed placement from a leaf cell and/or cluster.

```
status remove_dont_touch_placement
object_list
```

remove_dp_int_round

Remove the rounding attribute from datapath output nets.

```
int remove_dp_int_round
nets
```

remove_drc_error

Remove one or more errors from the error view.

```
status remove_drc_error
-drc_error drc_error
[-error_view mw_error_view]
drc_error
```

remove_driving_cell

Removes driving cell attributes from the specified input or inout ports of the current design.

```
int remove_driving_cell
[port_list]
```

remove_edit_groups

Removes a list of edit groups.

```
collection remove_edit_groups
[-all]
[-quiet]
[objects]
```

remove_filler_with_violation

Deletes filler cells that have routing violations

Equivalent Scheme command:

```
axDeleteFillerWithViolation
```

```
integer remove_filler_with_violation
-name cell_name
```

remove_flip_chip_route

Removes the specified flip-chip wires and contacts.

```
status remove_flip_chip_route
[-nets collection_of_nets
 | -nets_in_file nets_file]
[-width width]
[-contact]
```

remove_fp_block_shielding

Removes signal shielding (route blockages) created by create_fp_block_shielding.

Equivalent Scheme command:

```
fphDeleteHierSignalShielding
```

```
status remove_fp_block_shielding
[-inside_boundary]
[-outside_boundary]
[-side_list {left | right | top | bottom}]
[-metal_layers layer_list]
[objects]
```

remove_fp_feedthroughs

Removes feedthrough ports and nets that exist within the design.

Equivalent Scheme command:

```
fphRemoveFeedthroughs
```

```
status remove_fp_feedthroughs
[-include {buffered original}]
[-nets object_list]
[-blocks object_list]
[-voltage_areas object_list]
```

remove_fp_pin_constraints

Resets the pin assignment constraints for the specified soft macros or plan groups to the default values.

```
status remove_fp_pin_constraints
[-block_level]
[blocks]
```

remove_fp_pin_overlaps

Removes overlaps between all pins on the specified soft macros and the specified top-level or soft macro pins.

Equivalent Scheme command:

```
fphRemoveSMPinOverlap
```

```
status remove_fp_pin_overlaps
[-cells collection]
[-pins collection]
```

remove_fp_plan_group_padding

Deletes the padding from plan groups.

Equivalent Scheme command:

```
fphDeletePlangroupPadding
```

```
status_value remove_fp_plan_group_padding
plan_groups
```

remove_fp_rail_stacked_via

Removes the selected power network stacked vias from the design based on the stacked via reduction results from the reduce_fp_rail_stacked_via command. These stacked vias are removed to reduce congestion.

```
int remove_fp_rail_stacked_via
```

remove_fp_rail_voltage_area_constraints

Removes the multi-voltage power network synthesis (PNS) constraints in the specified voltage area(s).

```
status
remove_fp_rail_voltage_area_constraints
[-voltage_area voltage_area]
[-all]
-layer string
```

remove_fp_relative_location

Removes previously set relative location constraint(s).

```
status remove_fp_relative_location
[-name constraint_name]
[-target_cells cells]
```

remove_fp_virtual_pad

Remove virtual power or ground pads for PNA and PNS.

Equivalent Scheme command:

```
fphAddVirtualPad
```

```
status remove_fp_virtual_pad
[-nets nets]
[-layer layer]
[-point {x y}]
[-all]
```

remove_fp_voltage_area_constraints

Resets the feedthrough constraints for the specified voltage areas to the default values.

```
status remove_fp_voltage_area_constraints
```

remove_from_collection

Removes objects from a collection, resulting in a new collection. The base collection remains unchanged.

```
collection remove_from_collection
base_collection
object_spec
```

remove_from_rp_group

Removes an item (cell, relative placement group, or keepout) from the specified relative placement groups.

```
status remove_from_rp_group
rp_groups
-leaf cell_name
-hierarchy group_name
[-instance instance_name]
-keepout keepout_name
```

remove_generated_clock

Removes a generated_clock object.

```
string remove_generated_clock
-all |
clock_list
```

remove_host_options

Remove host or pool definitions created by set_host_options.

```
status remove_host_options
[-all]
[-name options_name]
[name]
```

remove_ideal_latency

Removes ideal latency information from the specified objects.

```
string remove_ideal_latency
[-rise | -fall] [-min | -max] object_list |
-all
```

remove_ideal_net

Restores the ideal nets set by the set_ideal_net or set_ideal_network -no_propagate command to their initial nonideal state from the specified nets in the current design.

```
status remove_ideal_net
net_list
```

remove_ideal_network

Removes a set of ports or pins in an ideal network in the current design. Cells and nets in the transitive fanout of the specified objects are no longer treated as ideal.

```
int remove_ideal_network
object_list | -all
```

remove_ideal_transition

Removes ideal transition information from the specified objects.

```
string remove_ideal_transition
[-rise | -fall] [-min | -max] object_list |
-all
```

remove_ignore_cell_timing

Undoes the effects of set_ignore_cell_timing

```
int remove_ignore_cell_timing
cell_list
```

remove_ignored_layers

Removes ignored routing layers in congestion analysis and RC estimation. This command can also remove the design minimum and maximum routing layers if those layers have been already set.

```
int remove_ignored_layers
list_of_layers
[-all]
[-min_routing_layer]
[-max_routing_layer]
```

remove_input_delay

Removes input delay on pins or input ports.

```
int remove_input_delay
[-clock clock] [-clock_fall]
[-level_sensitive]
[-rise]
[-fall]
[-max]
[-min]
port_pin_list
```

remove_io_constraints

Removes previously set physical constraints

```
status remove_io_constraints
[-cell name]
[-pin_only]
[-pad_only]
[-chiplevel_pad_only]
[objects]
```

remove_io_pin_overlap

Spreads pins so that they do not overlap one another and have spacing violations.

Equivalent Scheme command:

```
axRemoveIOPinOverlap
```

```
int remove_io_pin_overlap
```

remove_isolate_ports

Removes the specified ports from the list of ports that are isolated in the current design.

```
int remove_isolate_ports
port_list
```

remove_isolation_cell

Removes specified isolation cell or cells from design.

```
int remove_isolation_cell
[-force]
-object_list cells
```

remove_keepout_margin

Removes keepout margin of specified type for the specified cells/lib cells in the design.

Equivalent Scheme command:

```
fphDeleteMacroPadding
```

```
int remove_keepout_margin
[-type hard | soft]
[-derived]
object_list
```

remove_left_right_filler_rule

removes left-right filler cell insertion rules.

```
integer remove_left_right_filler_rule
-lib_cell
```

remove_level_shifters

Removes all of the level shifters from the design.

```
integer remove_level_shifters
[-force]
```

remove_license

Removes a licensed feature.

```
status remove_license
feature_list
```

remove_map_power_switch

Removes library cells from the mapping definition for the specified power switch, which was previously defined by using the map_power_switch command. This command is supported only in UPF mode.

```
status remove_map_power_switch
power_switch_name
-all | -lib_cells cells
```

remove_mim_property

Removes multiply-instantiated-module data for selected instances. These instances will no longer be treated as multiply-instantiated-modules; that is, each will now refer to a unique master.

```
status remove_mim_property
{collection_of_cells}
```

remove_mw_cel

Removes Milkyway designs from the design library.

Equivalent Scheme command: `geDeleteCell`

```
status remove_mw_cel
[-hierarchy [-check_only]]
[-version_kept count]
[-verbose]
[-all_versions]
[-all_view]
mw_cel_list
```

remove_net

Removes nets from the *current design*.

Equivalent Scheme command: `dbDeleteObject`

```
int remove_net
net_list | -all
```

remove_net_routing

Removes all routing (vias and segments) for specific nets.

```
int remove_net_routing
list_of_nets
```

remove_net_routing_layer_constraints

Removes routing layer constraints for specific nets.

```
int remove_net_routing_layer_constraints
list_of_nets
```

remove_net_shape

Removes objects of net shapes. The objects could be specified by a collection or by name.

Equivalent Scheme command: `dbDeleteObject`

```
status_value remove_net_shape
[-verbose]
net_shapes
```

remove_net_timing_spacing

Remove timing spacing flags.

Equivalent Scheme command:
`dbResetAllNetTimingSpacing`

```
status remove_net_timing_spacing
```

remove_objects

Removes a list of objects

Equivalent Scheme command: `geDelete`

```
status remove_objects
objects
```

remove_output_delay

Removes output delay on pins or output ports.

```
int remove_output_delay
[-clock clock [-clock_fall]
[-level_sensitive]]
[-rise]
[-fall]
[-max]
[-min]
port_pin_list
```

remove_pg_network

Removes or changes the hierarchical power and ground network.

```
status remove_pg_network
-net list_of_pg_net
hier_cell_list | -top
```

remove_physical_bus

Removes physical buses.

```
status remove_physical_bus
physical_bus_list | -all
```

remove_pin_guides

Deletes the specified pin guides from the design.

```
status remove_pin_guides
-all | patterns
[-verbose]
```

remove_pin_name_synonym

Removes pin name synonym definitions.

```
status remove_pin_name_synonym
[-all]
[synonym_list]
```

remove_placement

Unplace cells in the core area.

```
status remove_placement
[-object_type {standard_cell | macro_cell |
all}]
[-new_location {top_right | origin |
center}]
```

remove_placement_blockage

Remove placement blockages.

Equivalent Scheme commands:

`axPurgePlaceBlockage, axPurgeSoftPlaceBlockage, dbDeleteObject`

```
int remove_placement_blockage
[-verbose]
[-name name]
patterns | -all
```

remove_plan_groups

Removes plan groups from the current design.

Equivalent Scheme command: `dbPurgeAllPlangroup`

```
int remove_plan_groups
[-verbose]
-all | objects
```

remove_pnet_options

Removes options set by the set_pnet_optionscommand.

```
int remove_pnet_options
```

remove_port

Removes ports from the current design or its subdesign.

Equivalent Scheme command: `dbDeleteObject`

```
int remove_port
port_list
```

remove_power_domain

Removes the specified power domains.

UPF Mode

```
status remove_power_domain
[-verbose]
[-scope instance_name]
[power_domains]
```

Non-UPF Mode

```
status remove_power_domain
domain_name | -all
```

remove_power_switch

Removes a power switch from the specified power domain. This command is supported only in UPF mode.

```
status remove_power_switch
[-verbose]
[power_switches]
[-domain domain_name]
```

remove_preferred_routing_direction

Removes the preferred routing direction for the given routing layer(s).

```
string remove_preferred_routing_direction
-layers list_of_layers
```

remove_propagated_clock

Removes a propagated clock specification.

```
string remove_propagated_clock
object_list
```

remove_qor_snapshot

Removes an existing QoR snapshot of timing, drc, area, power, etc. The remove utility deletes snapshots from the location specified by the icc_snapshot_storage_location variable.

NOTE: This is the new version of the remove_qor_snapshot command that supports both multicorner-multimode designs as well as non-multicorner-multimode designs.

```
void remove_qor_snapshot
[-name name]
[-all ]
```

remove_rail_maps

Removes all rail map data from the current session.

```
status remove_rail_maps
```

remove_route_by_type

Remove route by type.

```
status remove_route_by_type
[-nets nets]
[-signal_detail_route]
[-signal_user]
[-clock_ring]
[-clock_strap]
[-clock_tie_off]
[-clock_user]
[-pg_ring]
[-pg_strap]
[-pg_tie_off]
[-pg_user]
[-pg_std_cell_pin_conn]
[-pg_macro_io_pin_conn]
[-keep_pg_vias]
[-keep_pg_pins_at_boundary]
[-bus]
[-shield]
[-keep_frozen_net]
```

remove_route_guide

Removes route guides.

Equivalent Scheme commands:

```
axDeleteAllRouteGuide, dbDeleteObject
```

```
int remove_route_guide
[-verbose]
[-name name]
patterns | -all
```

remove_routing_blockage

Removes the specified routing blockages.

```
status remove_routing_blockage
[-verbose]
patterns
```

remove_routing_rules

Removes nondefault routing rules in a design defined by the define_routing_rule command.

```
int remove_routing_rules
[-all]
rule_name_list
```

remove_row_type

Remove row type attribute on the specified rows.

```
status remove_row_type
[-site site_name row_name_list]
```

remove_rp_group_options

Removes relative placement (RP) group attributes from the specified relative placement groups.

```
collection remove_rp_group_options
rp_groups
[-ignore]
[-x_offset]
[-y_offset]
[-compress]
```

remove_rp_groups

Removes a list of relative placement (RP) groups.

```
status remove_rp_groups
rp_groups | -all
[-hierarchy]
[-quiet]
```

remove_scaling_lib_group

Removes any previously specified scaling_lib_group from the current design, or from a subdesign.

```
status remove_scaling_lib_group
[-object_list objects]
```

remove_scan_def

Removes any scan chain data stored in Milkyway.

```
status remove_scan_def
```

remove_scan_pin_type

Removes the scan-in or scan-out type if set on the specified pin.

```
status remove_scan_pin_type
[-pin pin | -ref_pin physical_lib_pin]
```

remove_scenario

Removes a scenario from memory.

```
status remove_scenario
[scenario_name | -all]
```

remove_sdc

Removes all Synopsys Design Constraints (SDC).

Equivalent Scheme command: `ataRemoveTC`

```
int remove_sdc
[-keep_parasitics]
```

remove_site_row

Removes specified site rows or all site rows defined in the current design.

```
string remove_site_row
[row_name_list]
```

remove_skew_group

Removes the user-defined skew group.

```
remove_skew_group
[-name skew_group_name]
```

remove_stdcell_filler

Deletes standard, pad, and tap filler cells.

Equivalent Scheme commands:

```
axgPurgeFillerCell,
axgPurgeFillerCellByArea
```

```
status remove_stdcell_filler
-stdcell | -pad | -tap
[-bounding_box {{llx lly} {urx ury}}]
```

remove_supply_net

Removes supply nets from the specified power domain. This command is supported only in UPF mode.

```
status remove_supply_net
[-verbose]
[supply_nets]
[-domain domain_name]
```

remove_supply_port

Removes a supply port from the scope of the specified power domain or the current scope. This command is supported only in UPF mode.

```
status remove_supply_port
[-verbose]
[supply_ports]
[-domain domain_name]
```

remove_target_library_subset

Removes target library subset constraints (including both the target library subset specified by library_list option and -milkyway_reflibs option) from root design or from specified instances.

```
int remove_target_library_subset
[-object_list cells]
[-top]
```

remove_terminal

Removes terminals.

Equivalent Scheme command: `dbDeletePin`

```
status_value remove_terminal
terminals
[-verbose]
```

remove_text

Removes text.

Equivalent Scheme commands:
`dbDeleteObject, geDelete`

```
int remove_text
text_list | -all
```

remove_tie_cells

Removes tie cells and changes their connected pins and ports in the Milkyway database.

```
status remove_tie_cells
[-use_default_tie_net]
tie_cell_list
```

remove_track

Removes tracks.

Equivalent Scheme commands:
`axClearWireTracks, axPurgeSingleRecordType`

```
status remove_track
-all | patterns | -layer layer [-dir X | Y]
[-verbose]
```

remove_unconnected_ports

Removes unconnected ports or pins from cells, references, and subdesigns.

```
int remove_unconnected_ports
cell_list
[-blast_buses]
```

remove_user_shape

Remove objects of user shapes. The objects can be specified by a collection or by name.

Equivalent Scheme command: `dbDeleteObject`

```
status_value remove_user_shape
[-verbose]
user_shapes
```

remove_via

Removes vias.

Equivalent Scheme command: `dbDeleteObject`

```
status_value remove_via
[-verbose]
vias
```

remove_voltage_area

Removes voltage areas from the current design.

Equivalent Scheme command: `dbDeleteObject`

```
int remove_voltage_area
[-verbose]
-all | patterns
```

remove_vt_filler_rule

removes multiple threshold voltage filler cell insertion rules.

```
integer remove_vt_filler_rule
-threshold_voltage
```

remove_well_filler

Deletes all well fillers in a specified layer.

Equivalent Scheme command:
`axgPurgeWellFiller`

```
int remove_well_filler
-layer
[-core_only]
```

remove_xtalk_prop

remove aggressor/victim list properties

Equivalent Scheme command:
`dbClearAllNetXtalkProp`

```
status remove_xtalk_prop
```

remove_zrt_filler_with_violation

Deletes filler cells that have Zroute routing violations.

```
status remove_zrt_filler_with_violation
[-name cell_name]
```

rename

Rename or delete a command.

```
string rename
oldName newName
string oldName
```

rename_mw_cel

Renames a Milkyway design.

Equivalent Scheme command: `cmRenameCel`

```
int rename_mw_cel
old_name
new_name
[-all_version]
```

rename_mw_lib

Renames a Milkyway library.

Equivalent Scheme command: `cmRenameLib`

```
status_value rename_mw_lib
-from lib_name
-to lib_name
```

replace_power_switch

Replaces the reference cells of the specified header or footer cell instances with the specified reference cell and performs IR drop analysis.

```
status_value replace_power_switch
-cells {instances}
-lib_cell {lib_cell_or_power_switch}
[-virtual_pg_net virtual_net]
[-real_pg_net real_net]
[-no_analyze_power]
```

report_adjusted_endpoints

Gives a report of the adjusted endpoints in feasibility mode.

```
int report_adjusted_endpoints
[-zero_path]
[-zero_wire_load]
[-io]
[-slack_threshold]
[-all]
[-verbose]
[-scenarios {scenario_name1, scenario_name2,
...}]
```

report_ahfs_options

Writes a report about the automatic high-fanout synthesis (AHFS) options.

```
integer report_ahfs_options
```

report_annotated_check

Displays all annotated timing checks on the current design.

```
int report_annotated_check
[-nosplit]
```

report_annotated_delay

Displays all annotated delays on cells and nets of the current design.

```
int report_annotated_delay
[-cell] [-net] [-nosplit] [-summary]
```

report_annotated_transition

Displays annotated transitions on all pins of the current design.

```
int report_annotated_transition
-nosplit
```

report_antenna_ratio

Runs the antenna checker in the router and dumps a detailed report of antenna violations into the log file.

Equivalent Scheme command:

```
axReportAntennaRatio
```

```
integer report_antenna_ratio
```

report_antenna_rules

Reports all of the antenna rules stored in the library.

Equivalent Scheme command:

```
dbDumpLibAntennaRules
```

```
status_value report_antenna_rules
[mw_lib]
[-output file_name]
```

report_app_var

Shows the application variables.

```
string report_app_var
[-verbose]
[-only_changed_vars]
[pattern]
```

report_area

Displays area information for the current design or instance.

Equivalent Scheme command: `axgListPRSummary`

```
integer report_area
[-nosplit]
[-physical]
[-hierarchy]
```

report_attribute

Reports the attributes on one or more objects.

Equivalent Scheme command: `dbFetchObject`

```
string report_attribute
[-application]
[-class class_name]
[-quiet]
[object_list]
```

report_bounds

Reports bounds in the design.

```
int report_bounds
-all | bound | -name name_list
```

report_buffer_tree

Reports the buffer tree and its level information at the given driver pin.

```
status report_buffer_tree
[-from start_point_list | -net net_list]
[-break_points]
[-depth max_depth]
[-connections]
[-hierarchy]
[-physical]
[-nosplit]
```

report_buffer_tree_qor

Displays quality related properties of the buffer trees at the given driver pins.

```
int report_buffer_tree_qor
[-from list_of_driving_pins_or_nets]
```

report_bus

Lists the bused ports and nets in the current instance or in the current design.

```
integer report_bus
[-nosplit]
```

report_case_analysis

Reports case analysis on ports or pins.

```
string report_case_analysis
[-all] [-nosplit]
```

report_cbt_options

Reports options used by the create_buffer_tree command.

```
int report_cbt_options
```

report_cell

Displays information about cells in the current instance or in the current design.

Equivalent Scheme command:

```
axgListPRSummary
```

```
status report_cell
[-nosplit]
[-connections]
[-verbose]
[-physical]
[-only_physical]
[-significant_digits digits]
[cell_list]
```

report_cell_physical

Displays information about cells in the current instance or in the current design.

```
status report_cell_physical
[-connections]
[-verbose]
[cell_list]
```

report_cell_vt_type

prints out voltage threshold type of a cell master or all cell masters of a library. Voltage threshold type is used for mixed voltage threshold filler cell insertion

```
integer report_cell_vt_type
-library library_name | -lib_cell cell_name
```

report_change_list

Reports the ECO changes after running incremental optimization.

```
status report_change_list
```

report_check_library_options

Reports the values or the status of the options set by the set_check_library_options command. The report_check_library_options command provides information about options used for checking between logical libraries, options used for checking between physical libraries, and options used for checking between logical libraries and physical libraries.

```
status report_check_library_options
[-physical]
[-logic_vs_physical]
[-logic]
[-default]
```

report_clock

Displays clock-related information on the current design.

```
status report_clock
[-attributes] [-skew] [-nosplit] [-groups]
[-scenario
```

report_clock_gating

Reports information about clock gating performed by Power Compiler.

```
status report_clock_gating
[-no_hier]
[-verbose]
[-gated]
[-ungated]
[-gating_elements]
[-only cell_list]
[-nosplit]
[-physical]
[-multi_stage]
[-style]
[-structure]
[-scenario scenario_list]
```

report_clock_gating_check

Prints a report of the clock gating checks.

```
string report_clock_gating_check
[-nosplit]
[-significant_digits digits]
[instance_list]
```

report_clock_timing

Reports the timing attributes of clock networks.

Equivalent Scheme command: `astClockTiming`

```
string report_clock_timing
-type report_type
[-clock clock_list]
[-from_clock from_clock_list]
[-to_clock to_clock_list]
[-to to_list]
[-from from_list]
[-setup] | [-hold]
[-launch] | [-capture]
[-rise] | [-fall]
[-min] | [-max]
[-nworst worst_entries]
[-greater_than lower_limit]
[-lesser_than upper_limit]
[-slack_lesser_than slack_upper_limit]
[-include_uncertainty_in_skew]
[-verbose]
[-show_clocks]
[-nosplit]
[-significant_digits digits]
[-nets]
[-capacitance]
[-attributes]
[-physical]
[-max]
[-fall]
[-capture]
[-hold]
```

report_clock_tree

Reports structural and timing characteristics of a compiled clock tree.

Equivalent Scheme command:

```
astSkewAnalysis
```

```
status report_clock_tree
[-clock_trees clock_tree_list]
[-summary]
[-structure]
[-drc_violators]
[-settings]
[-exceptions [-show_all_sinks]]
[-from from_list | -to to_list]
[-operating_condition condition]
[-level_info]
[-high_fanout_net net_or_pin_list
 | -premesh
 | -postmesh]
[-nosplit]
[-all_drc_violators]
[-partial_structure_within_exceptions]
[-skew_group skew_groups_string]
```

report_clock_tree_optimization_options

Reports options used by clock tree optimization.

```
status
report_clock_tree_optimization_options
[-clock_trees clock_name_or_collection]
```

report_clock_tree_power

Calculates and reports dynamic and static power for a clock network.

Equivalent Scheme command:

```
astReportClockTreePower
```

```
int report_clock_tree_power
[-net]
[-cell]
[-verbose]
[-include_input_nets]
[-include_register]
[-sort_mode mode]
[-nosplit]
[clock_list]
```

report_congestion

Reports the congestion statistics.

```
status report_congestion
[-search_repair | -no_reroute]
[-grc_based
{-grc_number grc_number}]
[-overflow_threshold threshold]
[-by_layer]
[-coords {rectangle}
 | -polygon {polygon_area}]
```

report_congestion_options

Reports congestion options in the design.

```
integer report_congestion_options
[-all]
id_list
```

report_constraint

Displays constraint-related information about a design.

```
status report_constraint
[-all_violators]
[-verbose]
[-significant_digits digits]
[-max_area]
[-max_delay]
[-critical_range]
[-min_delay]
[-max_capacitance]
[-min_capacitance]
[-max_transition]
[-max_fanout]
[-cell_degradation]
[-min_porosity]
[-max_dynamic_power]
[-max_leakage_power]
[-max_net_length]
[-connection_class]
[-multiport_net]
[-nosplit]
[-max_toggle_rate]
[-max_total_power]
[-scenario scenario_list]
```

report_critical_area

Calculates the critical area of the design.

```
status report_critical_area
[-particle_distr_func_file filename]
[-input_layers layerlist]
[-fault_type short | open]
[-tsmc_encr_particle_distr_file]
[-layer_alias_DSD_format layeraliaslist]
[-suppress_zeros_in_report]
[-multiparticle_report_format]
```

report_crpr

Reports the clock reconvergence pessimism calculated between specified register clock pins or ports.

```
status report_crpr
-from from_latch_clock_pin
-to to_latch_clock_pin
[-from_clock from_clock]
[-to_clock to_clock]
[-setup | -hold]
[-significant_digits digits]
```

report_cts_batch_mode

Reports the clock tree synthesis batch mode status.

```
status report_cts_batch_mode
```

report_delay_calculation

Displays the actual calculation of a timing arc delay value for a cell or net.

```
status report_delay_calculation
-min
-max
-from from_pin
-to to_pin
[-nosplit]
[-crosstalk]
[-from_rise_transition from_rise_value]
[-from_fall_transition from_fall_value]
```

report_delay_estimation_options

Reports the parameters that influence delay estimation.

```
status report_delay_estimation_options
```

report_design

Displays attributes of the current design.

```
int report_design
[-nosplit]
[-physical]
```

report_design_lib

Lists the design units contained in the specified libraries.

```
int report_design_lib
[-libraries] [-designs] [-architectures]
[-packages] [library_list]
```

report_design_physical

Displays design-related information for the current design.

```
status report_design_physical
[-design_setup]
[-netlist]
[-floorplan]
[-route]
[-utilization]
[-all]
[-verbose]
```

report_direct_power_rail_tie

Reports all the library pins on which the direct_power_rail_tie attribute is set to true.

```
int report_direct_power_rail_tie
```

report_disable_timing

Reports disabled timing arcs in the current design.

```
string report_disable_timing
[-nosplit]
```

report_distributed_hosts

Creates a detailed report on user defined distributed hosts in the farm's pool

```
Boolean report_distributed_hosts
```

report_distributed_route

Return status of a specified job and total number of available CPUs.

Equivalent Scheme commands:

```
jpCheckJobStatus, jpQueryAvailableCPUs
```

```
integer report_distributed_route
-job jobId
```

report_drc_error_type

Output a formatted report on the given error types.

```
status report_drc_error_type
[-type error_type | -class type_class]
[-error_view mw_error_view]
```

report_droute_options

Reports the persistent detail route options, their current value, default value, range, type, and a brief description.

```
status report_droute_options
[-name ]
```

report_error_coordinates

Displays the coordinates of all error objects in the error cell.

```
status report_error_coordinates
error_cell_name
```

report_extraction_options

Reports the options that influence postroute extraction.

```
status report_extraction_options
[-scenario scenario_list]
```

report_fast_mode

Reports the fast mode settings.

```
report_fast_mode
```

report_feasibility_options

Reports options set for feasibility using set_feasibility_options command.

```
int report_feasibility_options
[-scenarios {scenario_name1, scenario_name2,
...}]
```

report_filler_placement

Reports on the standard cell fillers contained in a design.

```
int report_filler_placement
[-abut]
-lib_cell libcells
```

report_flip_chip_driver_bump

Issues a report of flip chip drivers and bumps matching results set with assign_flip_chip_nets command.

Equivalent Scheme command:

```
fcDumpDriverBumpMatch
```

```
status_value report_flip_chip_driver_bump
```

report_flip_chip_type

Report the personality type of specified nets, flip chip bumps or drivers

Equivalent Scheme command:

```
fcDumpDriverBumpMatch
```

```
status_value report_flip_chip_type
net_or_cell_list
```

report_floorplan_data

Reports the floorplan data on one or more modules.

```
status report_floorplan_data
-module module_objects
[-view view_name]
[-quiet]
```

report_fp_clock_plan_options

Reports options for the clock planning clock tree synthesis engine.

```
status report_fp_clock_plan_options
```

report_fp_macro_array

Report user defined macro array constraints.

```
status report_fp_macro_array
[-output_file file_name]
[array_name]
```

report_fp_macro_options

Issues a report about the floorplan macro options.

```
status report_fp_macro_options
[-output_file file_name]
[macro_cells]
```

report_fp_pin_constraints

Displays the pin assignment options that have been set for the specified soft macros, plan groups or ports.

Equivalent Scheme command:

```
fphGetSMPinAssignOptions
```

```
int report_fp_pin_constraints
[blocks]
[-block_level]
```

report_fp_placement

Generates a quality of results (QoR) report for virtual flat placement.

Equivalent Scheme commands:
`axgListPRSummary, fphPlacementReport`

```
int report_fp_placement
[-check_abutment]
[-verbose integer]
```

report_fp_placement_strategy

Prints the current values and default values for the parameters controlled by set_fp_placement_strategy.

Equivalent Scheme command: `fphPrintParams`

```
status report_fp_placement_strategy
```

report_fp_rail_constraints

Reports power network synthesis (PNS) constraints defined by the user or by default.

Equivalent Scheme command:
`fphSetPNSConstraints`

```
status report_fp_rail_constraints
[-all]
[-layer layer]
[-ring]
[-global]
[-block_ring block]
```

report_fp_rail_strategy

Reports the user-defined strategy in power network synthesis (PNS) and power network analysis (PNA) strategies.

```
status report_fp_rail_strategy
[-all]
[-use_lm_view]
[-use_tluplus]
[-pna_ultra_solver]
[-virtual_pad_wire_width]
[-define_pad_connection]
[-pad_resistance_file]
[-pns_skip_ir]
[-honor_macro_strap_config]
[-pns_hor_relative_offset]
[-pns_ver_relative_offset]
[-pns_ignore_via_cut_to_edge]
[-pns_ignore_soft_macro_blockage]
[-pns_clip_top_boundaries]
[-cut_plangroup_edge_layers]
[-pna_via_cut_row_column]
[-honor_macro_route_constraints]
[-align_strap_with_top_pin ]
[-align_strap_with_mtcmos_cells]
[-align_strap_with_bump_cells]
[-align_strap_with_m1_rail]
[-put_strap_in_std_cell_row]
```

report_fp_rail_voltage_area_constraints

Reports multi-voltage power network synthesis (MVDD PNS) constraints defined by the user or by default.

```
status
report_fp_rail_voltage_area_constraints
-all
-voltage_area voltage_area
[-synthesis]
[-layer layer]
[-ring]
[-global]
```

report_fp_relative_location

Report macro relative location constraints.

```
status report_fp_relative_location
[-output_file file_name]
[cells]
```

report_fp_voltage_area_constraints

Displays the feedthrough options that have been set for the specified voltage areas.

```
int report_fp_voltage_area_constraints
```

report_groute_options

Reports global router cell-persistent options, their current value, default value, range, type and a brief description.

```
status report_groute_options
[-name ]
```

report_hierarchy

Displays the reference hierarchy of the current instance or the current design.

```
integer report_hierarchy
[-nosplit]
[-full]
[-noleaf]
```

report_host_options

Prints a report of hosts, pools, and their options as defined by the *set_host_options* command.

```
int report_host_options
```

report_ideal_network

Displays information about ports, pins, nets, and cells on ideal networks in the current design.

```
int report_ideal_network
[-net]
[-cell]
[-load_pin]
[-timing]
[object_list]
```

report_ignored_layers

Reports the routing layers that are ignored during congestion analysis and RC estimation. If you have set the minimum and maximum routing layers for the design, they are also reported.

```
status report_ignored_layers
```

report_ilm

Reports information about the specified ILM instance.

```
status report_ilm
[ilm_list]
```

report_internal_loads

Displays internal loads on the nets in the current design.

```
int report_internal_loads
[-nosplit]
```

report_io_constraints

Displays a report of the pin and pad physical constraints.

```
status report_io_constraints
[-cell name]
[-pin_only]
[-pad_only]
[-chiplevel_pad_only]
[objects]
```

report_isolate_ports

Displays the status of port isolation on ports on which isolation was requested.

```
int report_isolate_ports
[-nosplit]
```

report_isolated_via

Reports isolated via violations.

```
integer report_isolated_via
[-isolated_via_spacing distance]
[-isolated_via_quadrant_spacing distance]
```

report_isolation_cell

Displays information about isolation cells in the current scope. This command is supported only in UPF mode.

```
status report_isolation_cell
[isolation_cells]
[-domain power_domains]
[-verbose]
[-port
a_list_of_ports,_port_instances_or_hierarchy
_ports]
[-strategy a_list_of_isolation_strategies]
```

report_keepout_margin

Reports keepout margins of a specified type for the specified cells in the design.

Equivalent Scheme command:

```
fphDumpMacroPadding
```

```
int report_keepout_margin
[-type hard | soft]
[-original]
[-parameters]
[-all_derivable]
[object_list]
```

report_latency_adjustment_options

Reports the options for I/O latency adjustment, defined by using the set_latency_adjustment_options command.

```
status report_latency_adjustment_options
```

report_lcc_hotspot

Reports lithography compliance check (LCC) hotspots.

```
status report_lcc_hotspot
[-sort_by_attribute layer | level | type]
```

report_left_right_filler_rule

Prints out the left and right filler cell insertion rules.

```
status report_left_right_filler_rule
```

report_level_shifter

Displays information about level shifter cells in the current scope. This command is supported only in UPF mode.

```
status report_level_shifter
[level_shifter_cells]
[-domain power_domains]
[-verbose]
[-nosplit]
```

report_lib

Displays information about technology, symbol libraries, or physical libraries.

```
int report_lib
[-all]
[-ccs_recv]
[-em]
[-fpga]
[-full_table]
[-k_factors]
[-power]
[-power_label]
[-routing_rule]
[-rwm]
[-table]
[-timing]
[-timing_arcs]
[-timing_label]
[-user_defined_data]
[-vhdl_name]
[-yield]
[-switch]
[-pg_pin]
[-char]
[-operating_condition]
[-op_cond_name op_cond_name]
[cell_list]
library_name
```

report_milkyway_version

Reports information for the specified cell, including the Milkyway data model version and revision information.

```
status report_milkyway_version
[-cell cell_name | -all]
```

report_mim

Generates a report on the multiple instantiated modules (MIMs) in the design.

```
status report_mim
```

report_mode

Prints a report of the instance modes.

```
string report_mode
[-nosplit]
[instance_list]
```

report_mpc_macro_array

Issues a report on the floorplan macro array set by using the set_mpc_macro_array command.

```
status report_mpc_macro_array
[macro_array]
```

report_mpc_macro_options

Issues a report about the floorplan macro options.

```
int report_mpc_macro_options
macro_list
```

report_mpc_options

Issues a report about the floorplan options.

```
int report_mpc_options
```

report_mpc_pnet_options

Issues a report about the floorplan pnet options.

```
int report_mpc_pnet_options
-name
```

report_mpc_port_options

Issues a report about the floorplan port options.

```
int report_mpc_port_options
port_list
```

report_mpc_rectilinear_outline

Issues a report about the floorplan rectilinear outline.

```
int report_mpc_rectilinear_outline
```

report_mpc_ring_options

Issues a report about the mpc ring options.

```
int report_mpc_ring_options
```

report_mtcmos_pna_strategy

Prints the current values and default values for the parameters controlled by set_mtcmos_pna_strategy.

```
status_value report_mtcmos_pna_strategy
```

report_mw_design_ecos

Report ECO history information and output specific ECO changelist

```
int report_mw_design_ecos
[design_name]
[-output outfile_name]
[-history]
[-id id_number]
```

report_mw_lib

Displays information about a Milkyway library.

```
status_value report_mw_lib
[-unit_range]
[-mw_reference_library]
mw_lib
```

report_name_rules

Reports the values of name rules.

```
int report_name_rules
[name_rules]
```

report_names

Reports potential name changes of ports, cells, and nets in a design.

```
int report_names
[-rules name_rules]
[-hierarchy]
[-dont_touch designs_list]
[-nosplit]
[-original]
```

report_net

Reports net information for the design of the current instance or for the current design.

```
status report_net
[-nosplit]
[-noflat]
[-transition_times]
[-only_physical]
[-verbose]
[-cell_degradation]
[-min]
[-connections]
[-physical]
[net_list]
[-significant_digits digits]
[-max_toggle_rate]
[-scenario scenario_list]
```

report_net_changes

Reports net changes that occurred during some IC Compiler optimizations, such as place_opt, create_buffer_tree, and route_opt.

```
int report_net_changes
[-verbose]
```

report_net_fanout

Displays net fanout or buffer tree information for the current design.

```
status report_net_fanout
[-nosplit]
[-high_fanout]
[-threshold lower]
[-bound upper]
[-verbose]
[-connections]
[-physical]
[-min]
[-tree [-depth level]]
[net_list]
```

report_net_routing_layer_constraints

Reports routing layer constraints for specific nets.

```
int report_net_routing_layer_constraints
list_of_nets
```

report_net_routing_rules

Displays a report of user-specified routing rules for the specified nets.

```
int report_net_routing_rules
list_of_nets
```

report_noise

Reports static noise for the worst pins or the specified pins, or all violators.

```
status report_noise
[-nworst_pins worst_pin_count]
[names]
[-slack_lesser_than slack_limit]
[-all_violators]
[-verbose]
[-significant_digits digits]
[-slack_type area | height]
```

report_noise_calculation

Displays the actual calculation of noise information for the specified net arc.

```
status report_noise_calculation
[-significant_digits digits]
-from from_pin
-to to_pin
```

report_operating_conditions

Display a specific or all the operating conditions in a library.

```
int report_operating_conditions
-library library_name
[-name op_cond_name]
```

report_optimize_dft_options

Reports options for physical design-for-test (DFT) optimization.

```
status report_optimize_dft_options
```

report_optimize_pre_cts_power_options

Reports the option settings for optimize_pre_cts_power command.

```
status_value
report_optimize_pre_cts_power_options
```

report_parameter

Reports the details of a parameter, such as name, type, current value, default value, valid range, and a brief description.

```
int report_parameter
[-name name]
[-module route | groute | droute |
trackAssign | ek | preroute | sr | all]
[-type integer | real | string]
```

report_path_group

Reports information about path groups in the current design.

```
status report_path_group
[-nosplit]
[-expanded]
[-scenario scenario_list]
```

report_pg_net

Reports power and ground net information for the opened Milkyway design.

```
status report_pg_net
[-net net_list]
[-connections]
```

report_physical_bus

Displays information about physical bus.

```
status report_physical_bus
[physical_bus_list]
```

report_physical_signoff_options

Reports option values set by set_physical_signoff_options that are shared (in common) by signoff_drc command and signoff_metal_fill command, etc.

```
status report_physical_signoff_options
[-default]
```

report_pin_guides

Displays information about the pin guides.

```
status report_pin_guides
[{-pins pins_collection
 | -nets nets_collection}]
[pin_guides]
```

report_pin_name_synonym

Reports pin name synonym definitions.

```
status report_pin_name_synonym
[-nosplit]
```

report_pin_shape

Displays information about a list of pin shapes.

```
status report_pin_shape
pin_shape_list
```

report_placement_utilization

Reports the placement utilization for the entire design or a certain region.

```
status report_placement_utilization
[-non_fixed_only ]
[-grid_size Float]
[-verbose ]
[-coordinates {X1 Y1 X2 Y2}]
```

report_pnet_options

Issues a report of the options set with the set_pnet_options command.

```
int report_pnet_options
```

report_port

Displays information about ports of the current instance or the current design.

```
integer report_port
[-drive]
[-verbose]
[-physical]
[-only_physical]
[-nosplit]
[-significant_digits digits]
[port_list]
```

report_port_protection_diodes

Reports the port protection diodes in the current design.

```
status report_port_protection_diodes
```

report_power

Calculates and reports dynamic and static power for a design or instance.

```
int report_power
[-net]
[-cell]
[-only cell_or_net_list]
[-hier]
[-hier_level level_value]
[-verbose]
[-cumulative]
[-flat]
[-exclude_boundary_nets]
[-include_input_nets]
[-analysis_effort low | medium | high]
[-nworst number]
[-sort_mode mode]
[-histogram [-exclude_leq le_val
 | -exclude_geq ge_val]]
[-nosplit]
[-scenario scenario_list]
```

report_power_calculation

Displays the calculation of the internal power for a pin, the leakage power for a cell, or the switching power for a net.

```
int report_power_calculation
pin_cell_or_net_list
[-state_condition boolean_eq_of_pins |
default | all]
[-path_source pin_name | default | all]
[-rise]
[-fall]
[-verbose]
[-nosplit]
```

report_power_domain

Reports information about the specified power domain.

UPF Mode

```
status report_power_domain
[power_domains]
[-scope instance_name]
```

Non-UPF Mode

```
status report_power_domain
[power_domains]
```

report_power_gating

Reports the power gating style of retention registers in the design.

```
int report_power_gating
[cell_or_design_list]
[-missing]
[-unconnected]
```

report_power_guide

Reports existing power guides with different information.

```
report_power_guide
[power_guide_list]
```

report_power_options

Reports different power optimization options.

```
status report_power_options
```

report_power_pin_info

Reports the power pin information for technology library cells or leaf cells. In UPF mode, the command reports power pin information only for instantiated cells and not the library cells.

```
status report_power_pin_info
object_list
```

report_power_switch

Reports all of the specified power switches. This command is supported only in UPF mode.

```
status report_power_switch
[-verbose]
```

report_preferred_routing_direction

Reports the preferred routing direction for all routing layers.

```
string report_preferred_routing_direction
```

report_preroute_drc_strategy

Reports preroute drc options set in set_preroute_drc_strategy to change the internal rules in the following PG commands: create_rectangular_rings, create_pad_rings, create_power_straps, create_preroute_vias, preroute_instances, preroute_standard_cells These settings are not persistent in the Milkyway design.

```
status report_preroute_drc_strategy
```

report_primetime_options

Reports the PrimeTime options for the signoff_opt command.

```
status report_primetime_options
```

report_pst

Report power states in current design (UPF mode only).

```
int report_pst
[-verbose]
[-supplies supply_list]
[-scope instance_name]
[-power_nets supply_net_list]
[-compress]
[-trace_name]
[-significant_digits digit]
[-width line_width]
[-column_space column_space]
[-derived]
```

report_qor

Displays QoR information and statistics for the current design.

```
status report_qor
[-significant_digits digits]
[-physical]
[-scenario scenario_list]
```

report_qor_snapshot

Reports existing QoR snapshot of timing, DRC, area, clock, power, etc. The report utility gets snapshot information from the location specified by the icc_snapshot_storage_location variable.

NOTE: This is the new version of the report_qor_snapshot command that supports both multicorner-multimode designs as well as non-multicorner-multimode designs.

```
void report_qor_snapshot
[-name name]
[-display]
[-save_as report_name]
```

report_qtm_model

Reports Quick Timing Model (QTM) data.

```
string report_qtm_model
[-global_parameters]
[-ports]
[-arcs]
```

report_rail_options

Reports the current option settings of the analyze_rail command.

```
report_rail_options
```

report_reference

Displays information about references in the current instance or in the current design.

```
integer report_reference
[-nosplit]
[-hierarchy]
```

report_retention_cell

Displays information about retention cells in the current scope. This command is supported only in UPF mode.

```
status report_retention_cell
[retention_cells]
[-domain power_domains]
[-verbose]
[-strategy a_list_of_strategies]
```

report_route_opt_strategy

Reports the parameters that influence route_opt flow.

```
int report_route_opt_strategy
```

report_route_options

Report settings of route options that are shared (in common) among multiple router commands.

Equivalent Scheme command:

```
axgSetRouteOptions
```

```
status report_route_options
[-default]
```

report_route_zrt_common_options

Reports the settings of route options that are common among the Zroute router commands.

```
status report_route_zrt_common_options
```

report_route_zrt_detail_options

Reports the settings of the detail router options.

```
status report_route_zrt_detail_options
```

report_route_zrt_global_options

Reports the settings of the global router options.

```
status report_route_zrt_global_options
```

report_route_zrt_track_options

Reports the settings of track assignment options.

```
status report_route_zrt_track_options
```

report_routing_rules

Reports design-specific nondefault routing rules defined by the define_routing_rule command and their current values.

Equivalent Scheme command:

```
dbDumpAllVarRouteRules
```

```
integer report_routing_rules
rule_name
```

report_rp_group_options

Reports relative placement group attributes on the specified relative placement groups.

```
status report_rp_group_options
rp_groups
```

report_saif

Reports statistics on the switching activity annotation on the current design or instance.

```
int report_saif
[-hier]
[-flat]
[-type rtl | gate]
[-rtl_saif]
[-missing]
[-only cell_or_net_list]
[-annotated_flag]
```

report_scan_chain

Reports the scan chains defined on the current design.

```
status report_scan_chain
```

report_scenario_options

Reports the scenario options set by the set_scenario_options command.

```
status report_scenario_options
[-scenarios scenario_list]
```

report_scenarios

Reports scenarios setup information for multi-scenario design.

```
int report_scenarios
```

report_si_options

Reports signal integrity options used for analysis or optimization.

```
int report_si_options
```

report_signal_em

Reports signal electromigration results for the violating or specified nets. Also generates a repair file consisting of variable routing rules that can be loaded into the database for rerouting.

```
status report_signal_em
[-healing_factor healing_factor_value]
[-violation_rule_type mean | abs_avg | rms |
peak | auto]
[-repair_file repair_file_name]
[-min]
[-max]
[-violated]
[-verbose]
[list_of_nets]
```

report_skew_group

Reports the user-defined skew groups in the design.

```
status report_skew_group
[-clock clock_name]
[-name skew_group_name]
```

report_spacing_rules

Reports inter-cell spacing rules from the library.

```
status report_spacing_rules
-all
 | -of_library_cells
{library_cell_collection}
```

report_split_clock_gates_options

Reports the option settings of the split_clock_gates command.

```
status report_split_clock_gates_options
```

report_starrcxt_options

Reports Star-RCXT options for the signoff_opt command.

```
status report_starrcxt_options
```

report_supply_net

Reports all the supply nets in the current scope. This command is supported only in UPF mode.

```
status report_supply_net
[-include_exception]
```

report_supply_port

Reports information about the supply ports in the current scope. This command is supported only in UPF mode.

```
status report_supply_port
```

report_target_library_subset

Reports target library subsets on the design.

```
int report_target_library_subset
[-object_list cells]
[-top]
```

report_threshold_voltage_group

Reports the percentage of cells for each threshold voltage group in the design.

```
int report_threshold_voltage_group
[cell_or_design_list]
[-verbose]
```

report_tie_nets

Report tie high and tie low nets in the current design.

```
status report_tie_nets
```

report_timing

Displays timing information about a design.

Equivalent Scheme command:

astReportTiming

```
status report_timing
[-to to_list]
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]
[-rise_through rise_through_list]
[-fall_through fall_through_list]
[-path short | full | full_clock |
full_clock_expanded | only | end]
[-delay min | min_rise | min_fall | max |
max_rise | max_fall]
[-nworst paths_per_endpoint]
[-max_paths max_path_count]
[-input_pins]
[-nets]
[-transition_time]
[-crosstalk_delta]
[-capacitance]
[-attributes]
[-physical]
[-slack_greater_than greater_slack_limit]
[-slack_lesser_than lesser_slack_limit]
[-lesser_path max_path_delay]
[-greater_path min_path_delay]
[-loops]
[-true [-true_threshold path_delay]]
[-justify]
[-enable_preset_clear_arcs]
[-significant_digits digits]
[-nosplit]
[-sort_by group | slack]
[-group group_name]
[-trace_latch_borrow]
[-derate]
[-scenario scenario_list]
[-temperature]
[-voltage]
```

report_timing_derate

Reports timing derate factors for the design or specified objects.

```
string report_timing_derate
[-include_inherited]
object_list
[-nosplit]
[-scenario scenario_list]
```

report_timing_requirements

Reports timing path requirements (user attributes) and related information.

```
int report_timing_requirements
[-attributes]
[-ignored]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]
[-rise_through rise_through_list]
[-fall_through fall_through_list]
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
[-expanded]
[-nosplit]
```

report_tlu_plus_files

Reports the files used for TLUPlus extraction.

Equivalent Scheme command: `cmDumpTLUPlus`

```
integer report_tlu_plus_files
[-scenario scenario_list]
```

report_track

Reports the routing tracks for a specified layer or for all layers.

```
int report_track
[-layer layer]
[-dir X | Y]
```

report_transitive_fanin

Reports logic in the transitive fanin of specified sinks.

```
int report_transitive_fanin
-to sink_list
[-nosplit]
```

report_transitive_fanout

Reports logic in the transitive fanout of specified sources.

```
int report_transitive_fanout
-clock_tree | -from source_list
[-nosplit]
```

report_units

Reports the units used for resistance, capacitance, timing, leakage power, current, and voltage in the flow. The units must be consistant with the main library units.

```
string report_units
```

report_voltage_area

Reports the voltage areas in the design.

Equivalent Scheme commands:

```
axgDumpFloorPlan, axgPlaceCheck
```

```
int report_voltage_area
-all | patterns
```

report_vt_filler_rule

Writes out multiple threshold voltage filler cell insertion rules.

```
status report_vt_filler_rule
-threshold_voltage vt_type_1_vt_type_2
```

report_write_stream_options

Reports stream out options for the write_stream command.

```
status report_write_stream_options
[-default]
```

report_xtalk_route_options

Reports the settings of the global route and track assignment crosstalk options.

```
status report_xtalk_route_options
[-default]
```

report_zrt_net_properties

Reports the property settings for a net.

```
status report_zrt_net_properties
-net net_name
```

reset_clock_tree_optimization_options

Resets options used by clock tree optimization.

```
status reset_clock_tree_optimization_options
[-clock_trees clock_name_or_collection]
[-enable_multicorner_optimization]
[-gate_sizing]
[-gate_relocation]
[-preserve_levels]
[-area_recovery]
[-all]
[-balance_rc]
[-relax_insertion_delay]
[-corner_target_skew]
```

reset_clock_tree_options

Removes clock tree options which are set by user using set_clock_tree_options command.

```
void reset_clock_tree_options
[-root pin_col_spec]
[-buffer_relocation]
[-buffer_sizing]
[-delay_insertion]
[-gate_relocation]
[-gate_sizing]
[-layer_list]
[-max_buffer_levels]
[-max_capacitance]
[-max_fanout]
[-max_transition]
[-max_rc_delay_constraint]
[-max_rc_scale_factor]
[-routing_rule]
[-target_early_delay]
[-target_skew]
[-use_default_routing_for_sinks]
[-top_mode]
[-logic_level_balance]
[-config_file_read]
[-config_file_write]
[-all]
[-global]
[-ocv_clustering]
```

reset_clock_tree_references

Removes previously defined references from a clock tree.

```
status reset_clock_tree_references
[-references pin_collection]
```

reset_cts_batch_mode

Disables clock tree synthesis batch mode.

```
status reset_cts_batch_mode
```

reset_design

Removes from the current design all user-specified objects and attributes, except those defined using set_attribute.

```
status reset_design
```

reset_fp_clock_plan_options

Removes clock planning options which are set by user using set_fp_clock_plan_options command.

```
status reset_fp_clock_plan_options
[-output_directory]
[-no_feeds_plan_group]
[-clock_nets]
[-anchor_cell]
[-route_mode]
[-keep_block_tree]
[-all]
```

reset_latency_adjustment_options

Resets the options for I/O latency adjustment, defined by using the set_latency_adjustment_options command.

```
status reset_latency_adjustment_options
[-latency]
[-exclude_clock]
[-from_clock]
```

reset_mode

Resets the modes of the specified instances.

```
int reset_mode
[instance_list]
```

reset_path

Resets specified paths to single cycle timing.

```
int reset_path
[-setup | -hold]
[-rise | -fall]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]
[-rise_through rise_through_list]
[-fall_through fall_through_list]
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
```

reset_split_clock_gates_options

Specifies to reset the options of split_clock_gates to the default settings. The set option command is set_split_clock_gates_options.

```
status reset_split_clock_gates_options
```

reset_switching_activity

Removes the toggle rate and static probability attributes, or the maximum toggle rate attribute, from nets, pins, cells, and ports of the current design.

```
integer reset_switching_activity
-switching_activity | -max_toggle_rate |
-all
[-verbose]
[object_list]
```

reset_timing_derate

Removes all derate factors set on the current design or libraries.

```
string reset_timing_derate
```

reset_upf

Removes all UPF constraints and UPF data-dependent constraints from the current design. This command is supported only in UPF mode.

```
status reset_upf
```

resize_objects

Resizes one or more objects.

Equivalent Scheme command: `geStretch`

```
status resize_objects
{-bbox bounding_box
 | -delta offset
 | -scale scale_factor
 | -width object_width
 | -height object_height
 | -utilization util_factor
 | -aspect aspect
 | -area area_name}
[-keep_placement]
[-keep_pad_to_core_distance]
[-ignore_fixed]
objects
```

resize_polygon

Returns a list of polygons whose edges have been pushed outwards or inwards (away from the area covered by the target polygon) by a specified distance.

```
list resize_polygon
polygon
-size size
```

rotate_objects

Rotates one or more objects either geometrically or by setting the current orientation.

Equivalent Scheme command: `geTransform`

```
new_objects rotate_objects
{-to orient
 | -by rotate
 | -mirror mirror}
[{-pivot point | -anchor anchor_point}]
[-ignore_fixed]
objects
```

route_area

Performs detail routing in specified area of the design.

Equivalent Scheme command: `axgAreaRoute`

```
status route_area
-within {{llx1 lly1} {urx1 ury1} ....}
[-mode (initial_route | search_and_repair |
optimize)]
[-loop num]
[-run_time_limit time]
```

route_auto

Performs global routing, track assignment, detail routing, and search and repair in one step.

Equivalent Scheme command: `axgAutoRoute`

```
status route_auto
[-no_global]
[-no_track]
[-no_detail]
[-search_repair_loop num]
[-effort (minimum | low | medium | high)]
[-save_after_global_route]
[-save_after_track]
[-save_after_detail_route]
[-num_cpus num]
```

route_detail

Performs detail routing on the design.

Equivalent Scheme command: `axgDetailRoute`

```
status route_detail
[-track_assign (auto | skip)]
[-search_repair_loop num]
[-run_time_limit num]
[-num_cpus num]
```

route_differential

Routes the nets in the specified differential groups.

Equivalent Scheme command: `axgRouteDifferential`

```
status route_differential
-groups group_names
[-ignore_global]
[-ignore_track_assign]
[-ignore_detail]
[-search_repair_loop int]
```

route_eco

Performs ECO routing on the design.

Equivalent Scheme commands: `axgECORoute, axgECORouteDesign`

```
status route_eco
[-no_global]
[-no_track]
[-no_detail]
[-auto]
[-region_based file]
[-distributed]
[-num_cpus num]
[-search_repair_loop num]
[-utilize_dangling_wires]
[-scope (global | local)]
[-reroute (modified_nets_only |
modified_nets_first_then_others | any_nets)]
[-freeze_routing_on_layer name]
[-freeze_vias_on_frozen_metal]
```

route_flip_chip

Routes flip-chip nets on a single metal layer.

```
status route_flip_chip
[-nets | -nets_in_file nets_file]
[-route_by_input_net_order ]
[-45_degree ]
-routing_layer layer
```

route_fp_proto

Performs quick global routing on the design.

Equivalent Scheme command: `axgProtoRoute`

```
status route_fp_proto
[-effort (low | medium)]
[-congestion_map_only]
[-track_assignment]
```

route_global

Performs global routing on the design.

Equivalent Scheme command: `axgGlobalRoute`

```
status route_global
[-effort (minimum | low | medium | high)]
[-congestion_map_only]
```

route_group

Performs routing on a group of nets in the design.

Equivalent Scheme command: `axgRouteGroup`

```
status route_group
[-nets nets | -all_clock_nets]
[-no_global]
[-no_track]
[-no_detail]
[-search_repair_loop num]
[-utilize_dangling_wires]
[-trim_antenna_of_user_wires]
[-dont_optimize_route_pattern]
[-num_cpus num]
```

route_htree

Creates routes of H, I, or T (rotated H, rotated I, or rotated T) shape on the specified nets.

```
status route_htree
-nets list_of_nets
-layers {horizontal_layer vertical_layer}
[-orientation
list_of_three_orientation_values]
[-allow_off_grid]
[-allow_violation]
[-root root_buffer_of_the_H/I_tree]
[-mesh_net mesh_net]
```

route_mesh_net

Routes the connections from the clock mesh wire grid to the associated drivers and loads.

```
status route_mesh_net
-net
[-mode comb | fishbone]
[-max_backbone_fanout
-max_backbone_fanout_value]
[-max_span max_span_value]
[-backbone_dir horizontal | vertical | both]
[-max_rc_delay float]
```

route_opt

Performs simultaneous routing and post-route optimization on the design.

Equivalent Scheme commands: `astPostRT, astPostRouteOpt, axgAdvRouteOpt, axgRoutOpt`

```
status route_opt
[-effort low | medium | high]
[-xtalk_reduction]
[-only_xtalk_reduction]
[-skip_initial_route]
[-stage global | track | detail]
[-power]
[-incremental]
[-size_only]
[-optimize_wire_via]
[-area_recovery]
[-wire_size]
[-only_wire_size]
[-only_hold_time]
[-only_design_rule]
[-only_power_recovery]
[-only_area_recovery]
[-num_cpus number]
[-initial_route_only]
```

route_rc_reduction

Optimizes the timing and crosstalk on a fully-routed design, based on the detail routing results. This command works only on completely detail-routed designs that include all the necessary timing information.

Equivalent Scheme command: `axgAdvRouteOpt`

```
status route_rc_reduction
[-slack_target slack_target_number]
[-setup_slack_effort optimize | preserve]
[-max_transition]
[-max_capacitance]
[-crosstalk_noise]
[-run_time_limit number]
[-opt_delay_loop number]
[-opt_delay_search_repair_loop number]
```

route_search_repair

Performs a search and repair routing operation on the design.

Equivalent Scheme command:
`axgSearchRepair`

```
status route_search_repair
[-loop num]
[-run_time_limit num]
[-reset_width]
[-rerun_drc]
[-reset_min_max_layer]
[-trim_antenna_of_user_wires]
[-dont_connect_tie_off]
[-ignore_open_nets]
[-num_cpus num]
```

route_spreadwires

Spreads wires in the opened cell for DFM.

```
route_spreadwires
[-timing_driven]
[-search_repair_loop number_of_loops]
[-setup_slack_threshold setup_time]
[-min_jog_length min_ratio]
[-num_cpus number_of_cpus]
```

route_track

Assigns wires to tracks in the design.

Equivalent Scheme command:

```
axgAssignToTracks
```

```
status route_track
```

route_widen_wire

Performs wire widening for wires of signal nets.

```
status route_widen_wire
[-search_repair_loop number_of_loops]
[-nonuniform_widening]
[-timing_driven]
[-setup_slack_threshold
value_of_setup_slack_threshold]
[-hold_slack_threshold
value_of_hold_slack_threshold]
```

route_zrt_auto

Performs global routing, track assignment, and detail routing in one step.

```
status route_zrt_auto
[-max_detail_route_iterations num]
[-reuse_existing_global_route true | false]
[-stop_after_track_assignment true | false]
[-save_after_global_route true | false]
[-save_after_track_assignment true | false]
[-save_after_detail_route true | false]
[-save_cell_prefix name]
```

route_zrt_clock_tree

Performs routing on the clock nets in the design using Zroute.

```
status route_zrt_clock_tree
[-utilize_dangling_wires false|true]
[-reuse_existing_global_route false|true]
[-max_detail_route_iterations int]
```

route_zrt_detail

Performs detail routing on the design.

```
status route_zrt_detail
[-max_number_iterations count]
[-coordinates {{llx1_lly1}_{urx1_ury1}_...}]
[-incremental true | false]
[-initial_drc_from_input true | false]
[-start_iteration int]
```

route_zrt_eco

Performs ECO routing on the design.

```
status route_zrt_eco
[-max_detail_route_iterations count]
[-nets list]
[-open_net_driven true | false]
[-reroute modified_nets_only |
modified_nets_first_then_others | any_nets]
[-reuse_existing_global_route true | false]
[-utilize_dangling_wires true | false]
```

route_zrt_global

Performs global routing on the design.

```
status route_zrt_global
[-effort minimum | low | medium | high]
[-congestion_map_only true | false]
[-reuse_existing_global_route true | false]
```

route_zrt_group

Performs routing on a group of nets in the design.

```
status route_zrt_group
[-max_detail_route_iterations num]
[-nets nets | -all_clock_nets]
[-stop_after_global_route true | false]
[-reuse_existing_global_route true | false]
[-utilize_dangling_wires true | false]
-from_file file_name
```

route_zrt_track

Performs track assignment on the design.

```
status route_zrt_track
```

rp_group_inclusions

Returns a collection of relative placement groups that are directly included in the specified relative placement groups.

```
collection rp_group_inclusions
[rp_groups]
```

rp_group_instantiations

Returns a collection of relative placement groups that are instantiated in any of the specified relative placement groups.

```
collection rp_group_instantiations
[rp_groups]
```

rp_group_references

Returns a collection of cells that are directly included by the specified relative placement groups.

```
collection rp_group_references
[rp_groups]
[-leaf | -instance]
```

run_parallel_jobs

Runs parallel jobs controlled by the tool. It is typically used to invoke the tool on a group of subblocks in a hierarchical design.

run_signoff

Performs signoff analysis by invoking PrimeTime and Star-RCXT.

```
status run_signoff
[-check_only]
[-incremental]
[-signoff_analysis true | false | sleep |
wakeup]
[-aocvm]
[-path_based_analysis]
[-variation]
[-keep_license]
[-snapshot base_name]
[-correlation {setup spef_out}]
```

save_mw_cel

Saves the specified design in Milkyway format.

Equivalent Scheme command: `dbSaveCell`

```
status save_mw_cel
[-as name]
[-increase_version]
[-scenarios scenario_list]
[-hierarchy]
[-previous]
[-check_only]
design_name
[-overwrite]
```

save_qtm_model

Saves the current Quick Timing Model (QTM) description.

```
string save_qtm_model
```

save_upf

Writes out the UPF commands in the specified file. This command is supported only in UPF mode.

```
collection save_upf
upf_file_name
```

select_mim_master_instance

```
status select_mim_master_instance
plan_group
```

send_flow_status

Sends flow status from a running job to its parent. It is used exclusively with the run_parallel_jobs command.

```
status send_flow_status
[-job_name job_name]
[-host host_name]
[-port port_number]
-stage_name stage_name
-status current_status
[-eof]
[-verbose]
```

set_active_scenarios

Specifies which scenarios are to be active.

```
int set_active_scenarios
scenario_list | -all
```

set_ahfs_options

Specifies the options to be used when running automatic high-fanout synthesis (AHFS).

```
status set_ahfs_options
[-optimize_buffer_trees true | false]
[-skip_for_hfs pins_or_ports]
[-enable_port_punching true | false]
[-no_port_punching cells]
[-default_reference references]
[-port_map_file file_name]
[-preserve_boundary_phase true | false]
[-constant_nets true | false]
[-hf_threshold integer]
[-mf_threshold integer]
[-remove_effort none | medium | high]
[-default]
```

set_always_on_strategy

Sets the always-on strategy for shutdown power domains.

```
status set_always_on_strategy
-object_list list_of_domains
-cell_type single_power | dual_power
```

set_annotated_check

Sets the setup, hold, recovery, or removal timing check value between two pins.

```
int set_annotated_check
check_value
-from from_pins
-to to_pins
-setup
 | -hold
 | -recovery
 | -removal
 | -nochange_high
 | -nochange_low
[-rise | -fall]
[-clock clock_check]
[-worst]
```

set_annotated_delay

Sets the net or cell delay value between two pins.

```
int set_annotated_delay
-net | -cell
[-load_delay load_delay_type]
[-rise | -fall] [-min] [-max] delay_value
-from from_pins -to to_pins [-worst]
```

set_annotated_transition

Sets the transition time at a given pin.

```
int set_annotated_transition
[-rise | -fall] [-min] [-max] transition
port_pin_list
```

set_app_var

Sets the value of an application variable.

```
string set_app_var
-default
var
value
```

set_attribute

Sets an attribute to a specified value on the specified list of objects.

Equivalent Scheme commands:

```
astSetDontUse, cmMarkCellType,
dbSetCellPortTypes, geModify
```

```
collection set_attribute
[-class class_name]
object_list
attribute_name
attribute_value
[-quiet]
```

set_auto_disable_drc_nets

Sets the auto_disable_drc_net attribute on the current design, causing the specified networks to be have DRC disabled. This command was previously called set_auto_ideal_nets.

```
int set_auto_disable_drc_nets
[-default]
[-none]
[-all]
[-clock true | false]
[-constant true | false]
[-scan true | false]
```

set_buffer_opt_strategy

Invokes new buffering strategy.

```
int set_buffer_opt_strategy
[-effort string]
```

set_case_analysis

Specifies that a port or pin is at a constant logic value 1 or 0, or is considered with a rising or falling transition..

```
string set_case_analysis
value
port_or_pin_list
```

set_cbt_options

Sets options used by the create_buffer_tree command.

```
int set_cbt_options
[-threshold threshold_value]
[-references list_of_references]
[-default]
[-cluster_mode_cluster_size int_0]
```

set_cell_degradation

Sets the cell_degradation attribute to a specified value on specified ports or designs.

```
int set_cell_degradation
cell_degradation_value
object_list
```

set_cell_internal_power

Sets or removes the power_value attribute on the specified pins. The value represents the power consumption for a single toggle of each pin.

```
int set_cell_internal_power
[-delete_all]
pin_list
[power_value [unit]]
```

set_cell_location

Specifies the physical location for leaf cells.

```
int set_cell_location
object_list
-coordinates {X Y}
[-ignore_fixed]
```

set_cell_row_type

Binds the logical hierarchical module to the specified row type attribute.

```
int set_cell_row_type
-type row_type
cell_list
```

set_cell_type

Changes the cell_type attribute on any library reference cell so you can set or unset any cell as a macro cell.

```
status set_cell_type
-type BLOCK | COVER | RING | PAD | CORE
list_of_library_reference_cells
```

set_cell_vt_type

Sets the threshold voltage type of a library cell or of all cells of a library. The threshold voltage type is used for mixed threshold voltage filler cell insertion.

```
status set_cell_vt_type
-library library_name | -lib_cell cell_name
-vt_type
```

set_check_library_options

Sets specific options for the check_library command for logic library versus logic library checking, logic library versus physical library checking, and for checks between physical libraries.

```
status set_check_library_options
[-cell_area]
[-cell_footprint]
[-bus_delimiter]
[-tech_consistency]
[-view_comparison]
[-same_name_cell]
[-signal_em]
[-antenna]
[-rectilinear_cell]
[-physical_only_cell]
[-phys_property {property_list}]
[-routeability]
[-tech]
[-drc]
[-scaling {scaling_types}]
[-mcmm]
[-upf]
[-compare {construct | attribute | value}]
[-tolerance {type relative_tolerance
absolute_tolerance}]
[-validate {validation_types}]
[-va_analysis {std_error=val_err
slope=val_sl trend=['/' | '' | '^' | 'V']}]
[-nosplit]
[-physical]
[-logic_vs_physical]
[-logic]
[-reset]
[-all]
```

set_checkpoint_strategy

Set the checkpoint strategy for preroute optimization commands

```
int set_checkpoint_strategy
[-enable | -disable]
[-overwrite]
[-prefix prefix]
```

set_chiplevel_pad_physical_constraints

Set chiplevel physical constraints on PAD cells.

```
status
set_chiplevel_pad_physical_constraints
[-dist_left_edge_to_pad float]
[-dist_top_edge_to_pad float]
[-dist_right_edge_to_pad float]
[-dist_bottom_edge_to_pad float]
```

set_clock_gating_check

Puts setup and hold checks on clock gating cells.

Equivalent Scheme command:

```
ataEnableGatingClock
```

```
int set_clock_gating_check
[-setup setup_margin]
[-hold hold_margin]
[-rise]
[-fall]
[-high | -low]
[object_list]
```

set_clock_gating_registers

Forces the enabling or disabling of clock gating for specified registers in the current design, overriding all conditions necessary for automatic RTL clock gating by the compile_ultra -gate_clock command.

```
status set_clock_gating_registers
[-include_instances register_list]
[-exclude_instances register_list]
[-undo register_list]
```

set_clock_groups

Specifies clock groups that are mutually exclusive or asynchronous with each other in a design so that the paths between these clocks are not considered during the timing analysis.

```
Boolean set_clock_groups
-physically_exclusive
 | -logically_exclusive
 | -asynchronous
[-allow_paths]
[-name name]
-group clock_list
```

set_clock_latency

Specifies clock network latency.

```
string set_clock_latency
[-rise]
[-fall]
[-min]
[-max]
[-source]
[-early]
[-late]
[-clock clock_list]
delay
object_list
```

set_clock_sense

Specifies the clock sense (with respect to the clock source) propagating forward from the specified pins.

```
string set_clock_sense
[-stop_propagation]
[-positive]
[-negative]
[-pulse {rise_triggered_high_pulse |
rise_triggered_low_pulse |
fall_triggered_high_pulse |
fall_triggered_low_pulse}]
[-clocks clocks]
pins
```

set_clock_transition

Sets clock transition attributes on clock objects.

```
int set_clock_transition
transition
[-rise | -fall]
[-min]
[-max]
clock_list
```

set_clock_tree_exceptions

Creates definitions for the following exceptions: float pins, stop pins, nonstop pins, exclude pins, dont_touch_subtree pins, dont_buffer nets, dont_size cells, and size_only cells.

```
status set_clock_tree_exceptions
[-float_pin_max_delay_rise
max_delay_rise_value]
[-float_pin_min_delay_rise
min_delay_rise_value]
[-float_pin_max_delay_fall
max_delay_fall_value]
[-float_pin_min_delay_fall
min_delay_fall_value]
[-float_pins float_pin_collection]
[-stop_pins stop_pin_collection]
[-non_stop_pins non_stop_pin_collection]
[-exclude_pins exclude_pin_collection]
[-dont_touch_subtrees
dont_touch_pin_collection]
[-dont_buffer_nets
collection_or_list_of_nets]
[-dont_size_cells
collection_or_list_of_cells]
[-size_only_cells
collection_or_list_of_cells]
[-float_pin_logic_level logic_level_number]
[-max_float_pin_scale_factor
max_scale_factor]
[-min_float_pin_scale_factor
min_scale_factor]
[-preserve_hierarchy
hierarchy_preservation_pin_or_cell]
[-clocks object_list]
```

set_clock_tree_optimization_options

Sets options used by clock tree optimization.

```
status set_clock_tree_optimization_options
[-clock_trees clock_name_or_collection]
[-enable_multicorner_optimization {none |
all | corner_spec}]
[-corner_target_skew corner_values]
[-gate_sizing true | false]
[-gate_relocation true | false]
[-area_recovery true | false]
[-preserve_levels true | false]
[-relax_insertion_delay true | false]
[-balance_rc true | false]
```

set_clock_tree_options

Traces the net and creates or modifies the clock tree structure that is input to the clock tree synthesis engine.

Equivalent Scheme command:

```
astClockOptions
```

```
status_value set_clock_tree_options
[-clock_trees clock_name_or_collection]
[-layer_list list_of_layer_names]
[-target_early_delay
minimum_insertion_delay]
[-target_skew desired_skew]
[-max_capacitance max_capacitance_value]
[-max_transition max_transition_value]
[-max_fanout max_fanout_value]
[-max_buffer_levels number_of_levels_value]
[-max_rc_delay_constraint
max_rc_delay_value]
[-max_rc_scale_factor
scale_factor_of_internal_derived_rc_delay]
[-routing_rule
name_of_the_non_default_routing_rule]
[-use_default_routing_for_sinks n]
[-buffer_relocation true | false]
[-buffer_sizing true | false]
[-gate_relocation true | false]
[-gate_sizing true | false]
[-delay_insertion true | false]
[-logic_level_balance true | false]
[-ocv_clustering true | false]
[-config_file_read filename]
[-config_file_write filename]
[-insert_boundary_cell true | false]
[-operating_condition string]
```

set_clock_tree_references

Specifies the buffers and inverters that can be used in clock tree synthesis.

Equivalent Scheme command:

```
astSetClockCell
```

```
status set_clock_tree_references
-references references
[-sizing_only]
[-delay_insertion_only]
[-boundary_cell_only]
```

set_clock_uncertainty

Specifies the uncertainty (skew) of specified clock networks.

```
string set_clock_uncertainty
[object_list
 | -from from_clock
 | -rise_from rise_from_clock
 | -fall_from fall_from_clock
-to to_clock
 | -rise_to rise_to_clock
 | -fall_to fall_to_clock]
[-rise]
[-fall]
[-setup]
[-hold]
uncertainty
```

set_combinational_type

Sets attributes on cell instances to specify which combinational cells from the target library are to be used by compile.

```
int set_combinational_type
-replacement_gate replacement_gate
[cell_list]
```

set_congestion_options

Sets options for congestion optimization.

```
int set_congestion_options
[-max_util value]
[-layer name]
[-availability value]
[-coordinate {X1 Y1 X2 Y2}]
```

set_connection_class

Sets the connection class value on ports.

```
status set_connection_class
connection_class_value
object_list
```

set_context_margin

Specifies the margin by which to tighten or relax constraints.

```
string set_context_margin
[-percent]
[-relax]
[-min]
[-max]
value
[object_list]
```

set_cost_priority

Sets the cost_priority attribute to a specified value on the current design.

```
int set_cost_priority
[-default]
[-delay]
cost_list
[-design_rules]
[-min_delay]
```

set_critical_range

Sets the critical_range attribute to a specified value on a list of designs.

```
int set_critical_range
range_value designs
```

set_cts_batch_mode

Enables clock tree synthesis batch mode.

```
status set_cts_batch_mode
```

set_cts_scenario

Sets the specified scenario as the clock tree synthesis scenario.

```
string set_cts_scenario
[scenario_name]
```

set_current_command_mode

```
string set_current_command_mode
-mode command_mode | -command command
```

set_data_check

Sets data-to-data checks using the specified values of setup and hold time.

```
string set_data_check
-from from_object
  | -rise_from from_object
  | -fall_from from_object
-to to_object
  | -rise_to to_object
  | -fall_to to_object
[-setup | -hold]
[-clock clock_object]
[check_value]
```

set_default_drive

Sets the default driving strength for specified objects, to be used by Top-Down Environmental Propagation (TDEP).

```
status set_default_drive
[-min]
[-max]
[-rise]
[-fall]
[-none]
[resistance]
[cell_or_pin_list]
```

set_default_driving_cell

Sets the default driving cell for specified objects, to be used by Top-Down Environmental Propagation (TDEP).

```
int set_default_driving_cell
[-lib_cell lib_cell_name]
[-library lib]
[-rise] [-fall]
[-pin pin_name]
[-from_pin from_pin_name]
[-dont_scale] [-no_design_rule]
[-multiply_by factor] [-none]
cell_or_pin_list
```

set_default_fanout_load

Sets the default fanout load to be used by Top-Down Environmental Propagation (TDEP).

```
status set_default_fanout_load
[-none]
[fanout_load_value]
[cell_or_pin_list]
```

set_default_input_delay

Sets the value of the input delay as a percentage of the clock period to be assigned during environment propagation.

```
int set_default_input_delay
[-none]
percent_delay
[cell_or_pin_list]
```

set_default_load

Sets the default load to be used by Top-Down Environmental Propagation (TDEP).

```
status set_default_load
[-min]
[-max]
[-pin_load]
[-wire_load]
[-none]
[value]
[cell_or_pin_list]
```

set_default_output_delay

Sets the output delay as a percentage of the clock period to be assigned during environment propagation.

```
int set_default_output_delay
[-none]
percent_delay
[cell_or_pin_list]
```

set_delay_calculation

Defines the delay model used to compute a timing arc delay value for a cell or net.

Equivalent Scheme command:

`ataSetWireDelayModel`

```
int set_delay_calculation
[-arnoldi]
[-elmore]
[-clock_arnoldi]
```

set_delay_estimation_options

Sets the parameters that influence preroute delay estimation.

```
int set_delay_estimation_options
[-min_unit_horizontal_capacitance float]
[-min_unit_vertical_capacitance float]
[-min_unit_horizontal_resistance float]
[-min_unit_vertical_resistance float]
[-max_unit_horizontal_capacitance float]
[-max_unit_vertical_capacitance float]
[-max_unit_horizontal_resistance float]
[-max_unit_vertical_resistance float]
[-min_unit_horizontal_capacitance_scaling_fa
ctor float]
[-min_unit_vertical_capacitance_scaling_fact
or float]
[-min_unit_horizontal_resistance_scaling_fac
tor float]
[-min_unit_vertical_resistance_scaling_facto
r float]
[-max_unit_horizontal_capacitance_scaling_fa
ctor float]
[-max_unit_vertical_capacitance_scaling_fact
or float]
[-max_unit_horizontal_resistance_scaling_fac
tor float]
[-max_unit_vertical_resistance_scaling_facto
r float]
[-min_via_resistance float_resistance]
[-max_via_resistance float_resistance]
[-min_via_resistance_scaling_factor float]
[-max_via_resistance_scaling_factor float]
[-default]
```

set_design_license

Adds license information to the current design and can be used to require a license before a design can be read in.

```
status set_design_license
[-dont_show references]
[-quiet]
[-limited limited_keys]
regular_keys
```

set_design_top

Specifies the top-level design instance.

```
status set_design_top
instance_name
```

set_die_area

Sets the dimensions of the die area.

```
int set_die_area
-coordinate {X1 Y1 X2 Y2}
```

set_direct_power_rail_tie

Sets the direct_power_rail_tie attribute on library pins.

```
int set_direct_power_rail_tie
lib_pin_list [true | false]
```

set_disable_clock_gating_check

Disables the clock gating check for specified objects in the current design.

Equivalent Scheme command:

```
ataDisableGatingClock
```

```
string set_disable_clock_gating_check
object_list
```

set_disable_timing

Disables timing arcs in the current design.

```
int set_disable_timing
object_list
[-from from_pin_name -to to_pin_name]
[-restore]
```

set_distributed_route

Initializes the network for distributing routing jobs.

Equivalent Scheme command: `jpParallelJob`

```
status set_distributed_route
[-lsf]
[-lsf_advanced bsub_options]
[-jp_disconnect]
[-jp_machines {mname1 mname2 mname3...}]
[-jp_limit {mname0 limit mname1 limit mname2
limit...}]
[-jp_bin {mname1 bin_path mname2
bin_path...}]
[-jp_lib {mname1 lib_path mname2
lib_path...}]
```

set_domain_supply_net

Set the primary power net and primary ground net of an already existing power_domain. This command is supported only in UPF mode.

```
int set_domain_supply_net
domain_name
-primary_power_net supply_net_name
-primary_ground_net supply_net_name
```

set_dont_touch

Sets the dont_touch attribute on cells, nets, references, and designs in the current design, and on library cells, to prevent modification or replacement of these objects during optimization.

```
status set_dont_touch
object_list
[true | false]
```

set_dont_touch_network

Sets the dont_touch_network attribute on clocks, pins, or ports in the current design to prevent cells and nets in the transitive fanout of the set_dont_touch_network objects from being modified or replaced during optimization.

```
status set_dont_touch_network
object_list
[-no_propagate]
```

set_dont_touch_placement

Fixes the location of a cell or cluster.

```
status set_dont_touch_placement
object_list
```

set_dont_use

Sets the dont_use attribute on library cells to exclude them from the target library during optimization.

Equivalent Scheme command: `astSetDontUse`

```
int set_dont_use
[-power] object_list
```

set_dp_int_round

Set the rounding positions on datapath output nets.

```
status set_dp_int_round
nets
external_rounding_position
[internal_rounding_position]
```

set_drive

Sets the rise_drive or fall_drive attributes to specified resistance values on specified input and inout ports.

```
int set_drive
resistance
[-rise] [-fall] [-min] [-max]
port_list
```

set_driving_cell

Sets attributes on input or inout ports of the current design, specifying that a library cell or pin drives ports.

```
int set_driving_cell
[-lib_cell lib_cell_name]
[-library lib]
[-rise]
[-fall]
[-min]
[-max]
[-pin pin_name]
[-from_pin from_pin_name]
[-dont_scale]
[-no_design_rule]
[-none]
[-input_transition_rise rtran]
[-input_transition_fall ftran]
[-multiply_by factor]
port_list
[-cell
obsolete_-_please_use_-lib_cell_instead]
```

set_droute_options

Sets detailed router cell-persistent options.

```
status set_droute_options
[-name ]
[-value ]
[-default]
```

set_equal

Defines two input ports as logically equivalent.

```
int set_equal
port1
port2
```

set_error_view_property

Write error view properties. Fails with a warning if a property already exists.

```
status set_error_view_property
[-error_view mw_error_view]
[-writer product_name]
[-version version_string]
[-ignore_type_name_property true | false]
[-run_set run_set_name]
[-areas areas]
[-excluded_areas areas]
[-command command_string]
```

set_extraction_options

Sets the parameters that influence extraction.

```
status set_extraction_options
[-max_cap_scale max_cap_scaling]
[-min_cap_scale min_cap_scaling]
[-max_res_scale max_res_scaling]
[-min_res_scale min_res_scaling]
[-max_ccap_scale max_ccap_scaling]
[-min_ccap_scale min_ccap_scaling]
[-max_net_ccap_thres max_net_ccap_threshold]
[-min_net_ccap_thres min_net_ccap_threshold]
[-max_net_ccap_ratio max_net_ccap_ratio]
[-min_net_ccap_ratio min_net_ccap_ratio]
[-max_net_ccap_avg_ratio
max_net_ccap_avg_ratio]
[-min_net_ccap_avg_ratio
min_net_ccap_avg_ratio]
[-max_process_scale max_process_scaling]
[-min_process_scale min_process_scaling]
[-no_obstruction]
[-no_break_segments]
[-max_segment_length max_segment_length]
[-real_metalfill_extraction none | floating
| grounded | auto]
[-virtual_shield_extraction true | false]
[-fan_out_thres high_fan_out_threshold]
[-default]
```

set_false_path

Removes timing constraints from particular paths.

```
int set_false_path
[-rise | -fall] [-setup | -hold]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]
[-rise_through rise_through_list]
[-fall_through fall_through_list]
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
[-reset_path]
```

set_fanout_load

Sets the fanout_load attribute to a specified value on specified output ports of the current design.

```
int set_fanout_load
value
port_list
```

set_fast_mode

Turns on or turns off fast mode.

```
status set_fast_mode
[-no_congestion]
[set_fast_mode]
```

set_feasibility_options

Sets feasibility options for place_opt and reporting commands.

```
status set_feasibility_options
[-enable true | false]
[-zero_path_violations true | false]
[-zero_wire_load_violations true | false]
[-zero_path_margin zero_path_margin_num]
[-zero_wire_load_margin
zero_wire_load_margin_num]
[-io_margin io_margin_num]
[-group_io true | false]
[-design_slack_threshold
slack_threshold_num]
[-slack_threshold_path_groups
path_groups_list]
[-path_group_slack_threshold
path_group_slack_threshold_num]
[-verbose_level verbose_level_num]
[-feasibility_reporting boolean-string]
```

set_fix_hold

Sets a fix_hold attribute on clocks in the current design.

```
int set_fix_hold
clock_list
```

set_fix_hold_options

Specifies options for hold fixing during optimization.

```
int set_fix_hold_options
-default
-prioritize_tns
-prioritize_min
[-preferred_buffer]
```

set_fix_multiple_port_nets

Sets the fix_multiple_port_nets attribute to a specified value on the current design or a list of designs.

```
int set_fix_multiple_port_nets
-default | -all
[-feedthroughs]
[-outputs]
[-constants]
[-buffer_constants]
[design_list]
```

set_flip_chip_cell_site

Modifies flip_chip_cell_site properties to set different flip chip driver legal location constraints.

Equivalent Scheme command:

```
fcDumpDriverBumpMatch
```

```
status_value set_flip_chip_cell_site
-flip_chip_site {site_list}
[-personality {personality_list}]
[-personality_type_constraints
{{personality_type max_num}
{personality_type max_num}...}]
[-reserved_for_cell {{cell_ref {row_index
col_index}...} {cell_ref {row_index
col_index}...} ...}]
```

set_flip_chip_driver_array

Defines the legal locations for flip chip driver cells in a matrix configuration.

Equivalent Scheme command:

```
fcArrayLegalDriverLoc
```

```
status_value set_flip_chip_driver_array
-personality_type {personality_type_list}
-max_driver_size {width height}
-start_point start_point
-dimension {col row}
-delta {pitch_x pitch_y}
[-orientation N | W | S | E | FN | FS | FW |
FE]
```

set_flip_chip_driver_island

Defines the legal locations to place flip chip drivers in an island style.

Equivalent Scheme command:

`fcIslandLegalDriverLoc`

```
status_value set_flip_chip_driver_island
-start_point start_point
-repeat {num_columns num_rows}
-spacing {x_spacing y_spacing}
-island_size {width height}
-num_driver {num_x num_y}
[-filler cell_ref]
[-personality_type_constraints
{{personality_type max_num}
{personality_type max_num}...}]
[-default_orientation N | W | S | E | FN | FE
| FS | FW]
[-orient_by_row]
[-compaction vertical | horizontal | none]
[-center_packing]
[-forced_orientation {{orientation
col_index} {orientation col_index} ...}]
[-reserved_for_cell {{cell_ref {col_index
row_index}...} {cell_ref {col_index
row_index}...} ...}]
```

set_flip_chip_driver_ring

Defines the legal locations for flip chip driver cells in a ring configuration.

Equivalent Scheme command:

`fcRingLegalDriverLoc`

```
status_value set_flip_chip_driver_ring
-personality_type {personality_type_list}
-max_driver_size {width height}
-max_driver_num_per_ring driver_num
-min_driver_spacing driver_spacing
-ring_number ring_number
-ring_spacing ring_spacing
-outer_ring boundary_box
[-orientation N | W | S | E | FN | FS | FW |
FE]
[-num_extra_spacing num_extra]
[-extra_spacing extra_spacing]
[-stagger_drivers]
```

set_flip_chip_grid

Creates equally spaced grid points for flip chip driver placement.

Equivalent Scheme command:
`fcCreateUniformGrid`

```
status_value set_flip_chip_grid
-grid_origin {llx lly}
-x_step x
-y_step y
```

set_flip_chip_options

Sets general flip-chip driver placement options during virtual flat placement.

Equivalent Scheme command:
`astPlaceFcOptions`

```
status_value set_flip_chip_options
[-disable_driver_placement]
[-package_driven]
[-one_softmacro_per_island]
[-flip_chip_net_weight weight]
[-softmacro_net_weight sm_weight]
[-guardband_width {x y}]
[-multiple width | height | both]
```

set_flip_chip_type

Assigns personality types to specified nets, flip chip bumps or drivers.

Equivalent Scheme command: `fcFcType`

```
status_value set_flip_chip_type
-personality_type type
net_or_cell_list
```

set_fp_base_gate

Sets either a library leaf cell area or a user-specified cell area as the base unit area to use for gate equivalence calculations related to estimating the size of black boxes.

Equivalent Scheme command:

```
fphSetGateEquivalence
```

```
status set_fp_base_gate
{-cell master_name | -area cell_area}
```

set_fp_black_boxes_estimated

Sets the specified objects as estimated so that they are flagged as not needing to be sized before floorplanning.

Equivalent Scheme command:

```
fphSetBlackBoxesEstimated
```

```
status set_fp_black_boxes_estimated
black_boxes
```

set_fp_black_boxes_unestimated

Sets the specified objects as unestimated so that they are flagged as needing to be sized correctly before floorplanning.

Equivalent Scheme command:

```
fphSetBlackBoxesUnestimated
```

```
status set_fp_black_boxes_unestimated
black_boxes
```

set_fp_block_ring_constraints

Defines the power and ground rings that are automatically created around plan groups and macros when power network straps are synthesized by power network synthesis (PNS).

Equivalent Scheme command:

```
fphSetPNSBlockRings
```

```
status set_fp_block_ring_constraints
-add
  | -remove
  | -remove_all
  | -save_file file_name
  | -load_file file_name
[-block_type master | instance | plan_group
| voltage_area]
-block blocks
[-all_blocks]
-nets nets
[-horizontal_layer layer]
[-vertical_layer layer]
[-horizontal_width distance]
[-vertical_width distance]
[-horizontal_offset distance]
[-vertical_offset distance]
[-spacing distance]
```

set_fp_clock_plan_options

Sets options for the clock planning clock tree synthesis engine.

Equivalent Scheme command:

```
fphClockOptions
```

```
status set_fp_clock_plan_options
[-output_directory directory]
[-no_feeds_plan_group plan_groups
[-clock_nets clock_nets]
-anchor_cell cell
[-route_mode detailed | global | none]
[-keep_block_tree true | false]
```

set_fp_flow_strategy

Sets the strategy for the hierachical flow. These settings are not persistent in the Milkyway database.

```
status set_fp_flow_strategy
[-plan_group_aware_routing true | false]
[-top_level_routing_only true | false]
```

set_fp_macro_array

Specifies an array of macro cells.

```
status set_fp_macro_array
-name string
[-elements collection_of_macro_cell_objects]
[-align_edge t | b | l | r | c | top | bottom
| left | right | center]
[-align_pins {list of two pin objects}]
[-x_offset float]
[-y_offset float]
[-use_keepout_margin]
[-vertical]
[-rectilinear]
[-align_2d lb | lc | lt | rb | rc | rt | cb |
cc | cr | left-bottom | left-center |
left-top | right-bottom | right-center |
right-top | center-bottom | center-center |
center-top]
[-reset]
```

set_fp_macro_options

Specifies constraints on the specific floorplan macro cells and macro arrays in design planning.

Equivalent Scheme command:

```
fphSetPlaceConstraints
```

```
status set_fp_macro_options
collection_of_macro_objects
[-legal_orientations list]
[-anchor_bound {tl | t | tr | r | br | b | bl
| l | tm | bm | lm | rm | c}]
[-x_offset float]
[-y_offset float]
[-align_pins list]
[-side_channel {left_right_top_bottom}]
[-reset]
```

set_fp_pin_constraints

Sets pin assignment constraints that are honored during pin cutting and pin assignment.

Equivalent Scheme command:

`fphSetPAConstraints`

```
status set_fp_pin_constraints
[-allowed_layers layers]
[-pin_spacing pin_spacing_number]
[-hard_constraints {off | spacing | location
| layer}]
[-pin_preroute_spacing
preoute_spacing_number]
[-no_stacking stacking_allowed |
pg_pins_only | signal_pins_only | all]
[-corner_keepout_num_wiretracks
wiretracks_number
 | -corner_keepout_percent_side
keepout_percentage]
[-exclude_sides side_numbers]
[-allow_feedthroughs off | on]
[-exclude_network]
[-exclude_clock_feedthroughs off | on]
[-exclude_scan_chain_net_feedthroughs off |
on]
[-exclude_hfn_feedthroughs hfn_number]
[-exclude_feedthroughs nets]
[-incremental off | on]
[-nets nets | -exclude_nets nets]
[-keep_buses_together off | on
[-bus_ordering lsb_to_msb | msb_to_lsb |
scrambled | consistent_wirelengths]]
[-scramble_skip skip_number]
[-use_physical_constraints off | on]
[-block_level]
[blocks]
```

set_fp_placement_strategy

Sets parameters for controlling the command create_fp_placement.

Equivalent Scheme command: `fphPrintParams`

```
status set_fp_placement_strategy
[-default]
[-macro_orientation automatic | all | N]
[-auto_grouping none | user_only | low |
high]
[-macro_setup_only on | off]
[-macros_on_edge on | off | auto]
[-snap_macros_to_user_grid on | off]
[-sliver_size distance]
[-fix_macros none | soft_macros_only | all]
[-congestion_effort low | high]
[-IO_net_weight float]
[-plan_group_interface_net_weight float]
[-voltage_area_interface_net_weight float]
[-voltage_area_net_weight_LS_only on | off]
[-legalizer_effort low | high]
[-spread_spare_cells on | off]
[-virtual_IPO on | off]
[-pin_routing_aware on | off]
```

set_fp_power_pad_constraints

Defines the power pad synthesis constraints.

Equivalent Scheme command:
`fphSetPPSConstraints`

```
status set_fp_power_pad_constraints
[-honor_existing_pads | -honor_even_space]
[-target_pad_current current]
[-maximum_number_of_pads number]
[-save_file file_name]
```

set_fp_rail_constraints

Defines power network synthesis (PNS) constraints, including layer constraints, power ring and strap constraints, and global constraints.

Equivalent Scheme command:

```
fphSetPNSConstraints
```

```
status set_fp_rail_constraints
[-add_layer
 | -remove_layer
 | -remove_all_layers
 | -set_ring
 | -skip_ring
 | -set_global]
[-layer layer]
[-direction vertical | horizontal]
[-max_strap number]
[-min_strap number]
[-max_pitch distance]
[-min_pitch distance]
[-max_width distance]
[-min_width distance]
[-spacing distance | minimum | interleaving]
[-offset distance]
[-nets nets]
[-horizontal_ring_layer layer]
[-vertical_ring_layer layer]
[-ring_width distance]
[-ring_max_width distance]
[-ring_min_width distance]
[-ring_spacing distance]
[-ring_offset distance]
[-extend_strap core_ring | boundary |
pad_ring]
[-keep_floating_segments]
[-no_stack_via]
[-no_same_width_sizing]
[-optimize_tracks]
[-keep_ring_outside_core]
[-no_routing_over_hard_macros]
[-no_routing_over_plan_groups]
[-no_routing_over_soft_macros]
[-ignore_blockages]
```

set_fp_rail_region_constraints

Defines the region where power plan synthesis creates a rectilinear power mesh.

Equivalent Scheme command:

`fphSetSynthesizeRailRegion`

```
status_value set_fp_rail_region_constraints
[-voltage_area voltage_area
 | -polygon
-load_file file_name
 | -remove]
[-save_file file_name]
```

set_fp_rail_strategy

Sets the strategy for power network synthesis (PNS) and power network analysis (PNA). These settings are not persistent in the Milkyway database.

```
status set_fp_rail_strategy
[-reset]
[-use_lm_view true | false]
[-use_tluplus true | false]
[-pna_ultra_solver true | false]
[-virtual_pad_wire_width virt_wire_width]
[-define_pad_connection
connection_config_file_name]
[-pad_resistance_file
pad_resistance_file_name]
[-pns_skip_ir true | false]
[-honor_macro_strap_config
configuration_file]
[-pns_hor_relative_offset {h_layer
h_rel_offset}]
[-pns_ver_relative_offset {v_layer
v_rel_offset}]
[-pns_ignore_via_cut_to_edge true | false]
[-pns_ignore_soft_macro_blockage true |
false]
[-pns_clip_top_boundaries true | false]
[-cut_plangroup_edge_layers layers]
[-pna_via_cut_row_column number]
[-honor_macro_route_constraints
routing_constraints_file_name]
[-align_strap_with_top_pin true | false]
[-align_strap_with_mtcmos_cells
alignment_constraints_file_name]
[-align_strap_with_bump_cells
alignment_constraints_file_name]
[-align_strap_with_m1_rail true | false]
[-put_strap_in_std_cell_row true | false]
[-commit_fast true | false]
[-set_operating_temperature temperature]
[-create_hierarchical_pns_script true |
false]
```

set_fp_rail_voltage_area_constraints

Defines power network synthesis (PNS) constraints for the specified voltage area. This command specifies four groups of PNS constraints: synthesis constraints, layer constraints, ring constraints, and global constraints. Note that these constraints cannot be specified together in command; they must be specified in separate commands.

```
status set_fp_rail_voltage_area_constraints
-voltage_area voltage_area
[[-nets pg_nets]
-voltage_supply supply_voltage
[-power_budget power]
[-target_voltage_drop voltage]
[-power_switch power_switch_or_lib_cell]] |
[-layer pg_layer
-direction vertical | horizontal
[[-max_strap max_strap_number]
[-min_strap min_strap_number]] |
[[-max_pitch max_pitch_distance]
[-min_pitch min_pitch_distance]]
[-max_width max_width_distance]
[-min_width min_width_distance]
[-spacing minimum | interleaving | distance]
[-offset offset_distance]
[-mtcmos_net_type permanent | virtual]] |
[[-ring_nets ring_nets | -skip_ring]
[-horizontal_ring_layer h_ring_layer]
[-vertical_ring_layer v_ring_layer]
[-ring_width pg_ring_width]
[-ring_max_width max_ring_width]
[-ring_min_width min_ring_width]
[-ring_spacing distance_between_rings]
[-ring_offset distance_to_boundary]
[-extend_strap voltage_area_ring | core_ring
| boundary]
[-num_extend_straps number_extended]
[-extend_strap_direction
directions_to_extend]] |
[-global
[-keep_floating_segments]
[-no_stack_via]
[-no_same_width_sizing]
[-optimize_tracks]
[-no_routing_over_hard_macros]
[-no_routing_over_plan_groups]
[-no_routing_over_soft_macros]
```

```
[-ignore_blockages]
[-allow_routing_over_voltage_area]]
```

set_fp_relative_location

Specifies a constraint to place a macro relative to an anchor object.

```
status set_fp_relative_location
-name constraint_name
-target_cell cell_name
[-target_orientation N | S | E | W | FN | FS
| FE | FW]
[-target_corner bl | br | tl | tr]
[-anchor_object object_name]
[-anchor_corner bl | br | tl | tr]
[-x_offset distance]
[-y_offset distance]
```

set_fp_trace_mode

Marks a design and then loads the design in trace mode.

```
status set_fp_trace_mode
[-verbose]
[-verbose]
```

set_fp_voltage_area_constraints

Sets voltage area feedthrough constraints that are used by the global routing and the analyze_fp_routing command to create logical pins on voltage areas.

```
status set_fp_voltage_area_constraints
[-allow_feedthroughs true | false]
[-create_feedthrough_module true | false]
[-exclude_feedthroughs nets]
[voltage_areas]
```

set_groute_options

Sets global router cell-persistent options.

```
status set_groute_options
[-name ]
[-value ]
[-default]
```

set_hierarchy_color

Sets colors on all leaf cells descended from top hierarchical cells in the current design or hierarchical cells in the specified collection.

```
int set_hierarchy_color
-color color_Id | -cycle_color
[collection]
```

set_host_options

Controls the number of threads used by commands in the parent (master) process. Also controls the options used by commands that can run distributed jobs.

set_ideal_latency

Specifies ideal network latency.

```
string set_ideal_latency
[-rise | -fall]
[-min | -max]
delay
object_list
```

set_ideal_net

This command is replaced by set_ideal_network -no_propagate under the hood. It is recommended to use set_ideal_network instead of set_ideal_net.

```
status set_ideal_net
net_list
```

set_ideal_network

Marks a set of ports or pins in the current design as sources of an ideal network. This disables timing update and optimization of cells and nets in the transitive fanout of the specified objects.

```
integer set_ideal_network
object_list
[-dont_care_placement]
[-no_propagate]
```

set_ideal_transition

Specifies ideal transition for the ideal network & ideal nets.

```
string set_ideal_transition
[-rise | -fall]
[-min | -max]
transition_time
object_list
```

set_ignore_cell_timing

Skips the analysis of part of the design.

```
int set_ignore_cell_timing
cell_list
```

set_ignored_layers

Sets ignored routing layers for congestion analysis and RC estimation. This command can also set design minimum and maximum layers.

Equivalent Scheme command:

```
axgSetMinMaxLayer
```

```
int set_ignored_layers
[-rc_congestion_ignored_layers names]
[-min_routing_layer name]
[-max_routing_layer name]
```

set_input_delay

Sets input delay on pins or input ports relative to a clock signal.

```
status set_input_delay
delay_value
[-clock clock_name]
[-clock_fall]
[-level_sensitive]
[-network_latency_included]
[-source_latency_included]
[-rise]
[-fall]
[-max]
[-min]
[-add_delay]
port_pin_list
```

set_input_transition

Sets the max_transition_rise, max_transition_fall, min_transition_rise, or min_transition_fall attributes to the specified transition values on the specified input and inout ports.

```
int set_input_transition
transition
[-rise] [-fall] [-min] [-max]
port_list
```

set_inter_clock_delay_options

Sets options for interclock delay balancing.

```
status set_inter_clock_delay_options
[-balance_group source_objects]
[-balance_group_name string]
[-delay_offset float]
[-offset_to source_objects]
[-offset_from offset_from_obj]
[-offset_from_group string]
[-target_delay_clock target_clock_obj]
[-target_delay_value float]
[-honor_sdc true | false]
```

set_isolate_ports

Specifies the ports that are to be isolated from internal fanouts of their driver nets.

```
int set_isolate_ports
[-type inverter | buffer]
[-driver cell_name]
[-force]
port_list
```

set_isolation

Defines the UPF isolation strategy for the power domains in the design. This command is supported only in UPF mode.

```
status set_isolation
isolation_strategy
-domain power_domain
-isolation_power_net isolation_power_net
-isolation_ground_net isolation_ground_net
[-clamp_value 0 | 1 | z | latch]
[-applies_to inputs | outputs | both]
[-elements objects]
[-no_isolation]
```

set_isolation_control

Provides additional options needed for creating isolation cells. This command is needed with most set_isolation commands. This command is supported only in UPF mode.

```
status set_isolation_control
isolation_strategy
-domain power_domain
-isolation_signal isolation_signal
[-isolation_sense low | high]
[-location self | parent]
```

set_keepout_margin

Creates a keepout margin of the specified type for the specified cell or library cell.

Equivalent Scheme command: `fphPadMacros`

```
status set_keepout_margin
[-type hard | soft]
[-outer {lx by rx ty}]
[-tracks_per_macro_pin value]
[-min_padding_per_macro value]
[-max_padding_per_macro value]
[-all_macros]
[-macro_masters]
[-macro_instances]
[-north]
[object_list]
```

set_latency_adjustment_options

Performs setting options for io latency adjustment.

```
int set_latency_adjustment_options
[-from_clock clock_name]
[-to_clock collection_or_string_list]
[-exclude_clock collection_or_string_list]
[-latency float]
```

set_left_right_filler_rule

Sets left-right filler cell insertion rules.

```
status set_left_right_filler_rule
-left
-right
-lib_cell
[-follow_stdcell_orientation
```

set_level_shifter

Sets a strategy for level shifting during implementation. This command is supported only in UPF mode.

```
status set_level_shifter
level_shifter_name
-domain domain_name
[-elements list]
[-applies_to inputs | outputs | both]
[-threshold value]
[-rule low_to_high | high_to_low | both]
[-location self | parent | fanout |
automatic]
[-no_shift]
```

set_level_shifter_strategy

Sets the type of strategy to use for adjusting the voltage levels in the design.

```
int set_level_shifter_strategy
-rule all | low_to_high | high_to_low
[-location inside | outside | source | sink]
```

set_level_shifter_threshold

Sets the minimum threshold beyond which the voltage adjustment is required.

```
int set_level_shifter_threshold
-voltage volt
-percent diff
```

set_lib_attribute

Sets the value of an attribute on a library object.

```
list set_lib_attribute
object_list
attribute_name
attribute_value
```

set_lib_cell_spacing_label

Sets an intercell-spacing constraint label on a reference cell.

```
status set_lib_cell_spacing_label
-names {list_of_label_names}
[-left_lib_cells {lib_cell_collection}]
[-right_lib_cells {lib_cell_collection}]
```

set_load

Sets the load attribute to a specified value on specified ports and nets.

```
status set_load
value
objects
[-subtract_pin_load]
[-min]
[-max]
[[-pin_load] [-wire_load]]
```

set_local_link_library

Sets the local_link_library attribute to specified files and libraries on the current design.

```
int set_local_link_library
local_link_library
```

set_logic_dc

Specifies one or more input ports in the current design that are to be driven by don't care. The set_logic_one and set_logic_zero commands are used the same way as this command.

```
int set_logic_dc
port_list
```

set_logic_one

Specifies one or more input ports in the current design that are to be driven by logic one. The set_logic_zero and set_logic_dc commands are used the same way as this command.

```
int set_logic_one
port_list
```

set_logic_zero

Specifies one or more input ports in the current design that are to be driven by logic zero. The set_logic_one and set_logic_dc commands are used the same way as this command.

```
int set_logic_zero
port_list
```

set_macro_cell_bound_spot

Updates the macro cell move bound or group bound by specifying the exact location (spot) for the bound inside the macro cell.

```
status set_macro_cell_bound_spot
macro_cell_object
-coordinates {spot_x spot_y}
```

set_max_area

Sets the max_area attribute to a specified value on the current design.

```
int set_max_area
[-ignore_tns]
area_value
```

set_max_capacitance

Sets the max_capacitance attribute to a specified value on the specified input ports and designs.

```
int set_max_capacitance
capacitance_value
object_list
```

set_max_delay

Specifies a maximum delay target for paths in the current design.

```
int set_max_delay
delay_value
[-rise | -fall]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]
[-rise_through rise_through_list]
[-fall_through fall_through_list]
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
[-group_path group_name]
[-reset_path]
```

set_max_dynamic_power

Sets the target dynamic power for the current design by setting the max_dynamic_power attribute to a specified value.

```
int set_max_dynamic_power
dynamic_power
[GW | MW | KW | W | mW | uW | nW | pW | fW |
aW]
```

set_max_fanout

Sets the max_fanout attribute to a specified value on specified input ports and/or designs.

```
int set_max_fanout
fanout_value
object_list
```

set_max_leakage_power

Sets the target leakage power for the current design by setting the max_leakage_power attribute to a specified value.

```
int set_max_leakage_power
leakage_power
[GW | MW | KW | W | mW | uW | nW | pW | fW |
aW]
```

set_max_lvth_percentage

Sets the the maximum percentage of the total cell area that can be of a low threshold voltage group.

```
status set_max_lvth_percentage
[max_lvth]
[-lvth_groups groups]
[-reset]
```

set_max_net_length

Sets the max_net_length attribute to a specified value on specified input ports and/or designs.

```
int set_max_net_length
net_length_value
object_list
```

set_max_time_borrow

Sets the max_time_borrow attribute to a specified value on clocks, latch cells, data pins, or clock (enable) pins, to constrain the amount of time borrowing possible for level-sensitive latches.

```
int set_max_time_borrow
delay_value
object_list
```

set_max_total_power

Sets the target total power for the current design by setting the max_total_power attribute to a specified value.

The set_max_total_power constraint will be obsolete in a future release. Use set_max_leakage_power and set_max_dynamic_power constraints as a replacement.

```
int set_max_total_power
total_power
[GW | MW | KW | W | mW | uW | nW | pW | fW |
aW]
```

set_max_transition

Sets the max_transition attribute to a specified value on specified clocks group, ports or designs.

```
int set_max_transition
transition_value
object_list
```

set_mcmm_job_options

Sets various job control options for Distributed MCMM.

```
status set_mcmm_job_options
[-work_dir working_directory_path]
[-exec ICC_executable_path]
[-setup_script setup_script_name]
[-analysis_script analysis_script_name]
```

set_message_info

Set some information about diagnostic messages.

```
string set_message_info
-id message_id [-limit max_limit
 | -stop_on]
```

set_min_capacitance

Sets the min_capacitance attribute to a specified value on specified input ports in the current design.

```
int set_min_capacitance
capacitance_value
object_list
```

set_min_delay

Specifies a minimum delay target for paths in the current design.

```
int set_min_delay
delay_value
[-rise | -fall]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]
[-rise_through rise_through_list]
[-fall_through fall_through_list]
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
[-reset_path]
```

set_min_library

Sets an alternate library to use for minimum delay analysis.

```
int set_min_library
max_library
-min_version min_library | -none
```

set_mode

Selects the mode of a component.

```
int set_mode
[mode_list]
[instance_list]
```

set_mpc_macro_array

Specifies an array of macro cells.

```
int set_mpc_macro_array
-name string
-elements list
[-align_edge t | b | l | r | c | top | bottom
| left | right | center]
[-align_pins {ref_pin const_pin}]
[-x_offset float]
[-y_offset float]
[-use_keepout_margin]
[-vertical]
[-rectilinear]
[-align_2d lb | lc | lt | rb | rc | rt | cb |
cc | cr | left-bottom | left-center |
left-top | right-bottom | right-center |
right-top | center-bottom | center-center |
center-top]
[-verbose]
[-reset]
```

set_mpc_macro_options

Specifies constraints on the specific floorplan macro cells and macro arrays in MPC flows.

```
int set_mpc_macro_options
[list_of_macro_objects]
-legal_orientations list
-anchor_bound {tl | t | tr | r | br | b | bl
| l | tm | bm | lm | rm | c}
-x_offset float
-y_offset float
-align_pins list
-snap_to_edge side_and_float_list
-edge_channel float
-side_channel {left_right_top_bottom}
-group_name string
-group_spacing float
-reset
```

set_mpc_options

Specifies the constraints used to generate the floorplan in the create_placement -mpc flow, the compile_physical -mpc flow, or the physopt -mpc flow.

```
int set_mpc_options
-utilization util
-aspect_ratio y_x_ratio
-row_direction {h | v}
-origin {X Y}
-top_port_limit limit_value
-bottom_port_limit limit_value
-left_port_limit limit_value
-right_port_limit limit_value
-horz_port_layer_name layer
-vert_port_layer_name layer
-min_port_pitch integer
-routing_track_offset_x {h | f}
-routing_track_offset_y {h | f}
-io_margin_left margin_value
-io_margin_right margin_value
-io_margin_top margin_value
-io_margin_bottom margin_value
-corner_keepout distance
-core_width width
-core_height height
-first_row_orientation orient
-dont_snap_port
-dont_promote_layer
-shift_to_center
-rectilinear_outline
-reset
```

set_mpc_pnet_options

Specifies the constraints for pnet generation in the floorplan in the create_placement -mpc or physopt -mpc flows.

```
int set_mpc_pnet_options
-name pnet_name
-reset
-layer layer_name
-type pwr | gnd
-width float
-pitch float
-offset float
-direction {h | v}
-model_vias
-mult_via_x float
-mult_via_y float
```

set_mpc_port_options

Specifies the constraints for ports in the floorplan in the create_placement -mpc, the physopt -mpc, or the compile_physical -mpc flows.

```
int set_mpc_port_options
-side {l | r | t | b}
-x_bounds {min max}
-y_bounds {min max}
-layer layer_name
-group
-group_name group_name
-order {cw | ccw}
-pitch int
-start_location {x y}
-pin_order int
-offset float
-width float
-height float
-dont_snap
-reset
[port_list]
```

set_mpc_rectilinear_outline

Specifies the rectilinear outline constraint for the core generation in create_placement -mpc, physopt -mpc or compile_physical -mpc flows.

```
int set_mpc_rectilinear_outline
-coordinates list_of_floats
-reset
-verbose
```

set_mpc_ring_options

Specifies the constraints for ring generation around cores, macros, macro arrays, and designs in the floorplan in the flows of the create_placement, physopt, and compile_physical commands with the -mpc option.

```
int set_mpc_ring_options
[-name name]
[-reset] | [-layer layer_name -type -width
width]
[-offset offset]
[-sides {top | left | right | bottom}]
[-layer ]
```

set_mtcmos_pna_strategy

Sets options for power network synthesis (PNS) and power network analysis (PNA), when exploring, replacing, and optimizing MTCMOS cell size. These settings are not persistent in the Milkyway database.

```
status set_mtcmos_pna_strategy
[-reset]
[-power_budget budget]
[-voltage_supply voltage_supply]
[-lowest_voltage_drop]
[-target_voltage_drop target_voltage]
[-pad_lib_cell pad_names]
[-read_pad_cell_file cell_file]
[-read_pad_lib_cell_file lib_cell_file]
[-use_pins_as_pads]
[-use_strap_ends_as_pads]
[-create_virtual_rails layer_names]
[-synthesize_voltage_areas ]
[-disable_snap_to_row_and_tile]
[-relative_to_voltage_area]
[-pattern {normal | stagger}]
[-voltage_areas list]
```

set_multicycle_path

Modifies the single-cycle timing relationship of a constrained path.

```
integer set_multicycle_path
path_multiplier
[-rise | -fall]
[-setup | -hold]
[-start | -end]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]
[-rise_through rise_through_list]
[-fall_through fall_through_list]
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
[-reset_path]
```

set_mw_lib_reference

Sets the reference library for the Milkyway library.

Equivalent Scheme commands: `cmRefLib, cmReplaceRefLib, dbPurgeRefLib, dbSetRefLibControl`

```
status_value set_mw_lib_reference
[-mw_reference_library lib_list]
[-reference_control_file file_name]
libName
```

set_mw_technology_file

Sets the technology file of the Milkyway library.

Equivalent Scheme commands:
`cmReplaceTech, dbReplaceTechFile`

```
status_value set_mw_technology_file
[-technology tech_file]
[-plib plib_file]
libName
```

set_name

Changes the name of the specified netlist object.

```
status set_name
-type net | port | cell
object
-name local_name
```

set_net_aggressors

Sets the aggressor nets for a victim net.

Equivalent Scheme command:
`dbSetNetXtalkAggressorList`

```
status set_net_aggressors
-victim_net net
-aggressor_nets collection_of_nets
```

set_net_routing_layer_constraints

Assigns routing layer constraints to specific nets.

Equivalent Scheme command:

`axgSetMinMaxLayer`

```
int set_net_routing_layer_constraints
list_of_nets
-min_layer_name minimum_routing_layer_name
-max_layer_name maximum_routing_layer_name
```

set_net_routing_rule

Assigns a nondefault or default routing rule to specific nets.

Equivalent Scheme commands:

`axgSetNetConstraint,`
`dbAssignVarRouteRule`

```
integer set_net_routing_rule
-rule rule_name
list_of_nets
[-timing_driven_spacing]
[-reroute normal | minorchange | freeze]
[-top_layer_probe AnyPort | OutPort |
AllPort]
```

set_object_boundary

Sets the boundary of a set of objects to a bounding box or a list of points.

```
status set_object_boundary
{-bbox rect | -boundary boundary}
[-keep_placement]
[-keep_pad_to_core_distance]
[-ignore_fixed]
objects
```

set_object_fixed_edit

Sets the fixed state for one or more objects.

```
status set_object_fixed_edit
objects
fixed
```

set_object_shape

Sets the shape of a set of objects to one of the standard rectilinear shapes.

Only objects which can be resized can be set to a "rect" shape.

Only objects which can be rectilinear can be set to a "l", "t", "u" or "cross" shape.

See get_edit_property(2) man page for details on which objects can be resized and which objects can be rectilinear.

```
status set_object_shape
-shape {rect | l | t | u | cross}
-lengths real_list
[{-utilization real
 | -area real
 | -keep_area}]
[-rotate {0 | 90 | 180 | 270}]
[-keep_placement]
[-keep_pad_to_core_distance]
[-ignore_fixed]
objects
```

set_object_snap_type

Sets the snapping type for an object class.

```
old_value set_object_snap_type
{-class {soft_macro | plan_group |
hard_macro | standard_cell | routing | shape
| pin}
 | -enabled sbool}
[-snap {litho | row | row_tile | mid_row |
mid_row_tile | flip_chip | unit_tile |
wiretrack | halfwiretrack | user | none}]
```

set_operand_isolation_scope

Specifies whether a design or instance should be included or excluded for operand isolation processing.

```
status set_operand_isolation_scope
object_list
[true | false]
```

set_operating_conditions

Defines the operating conditions for the current design.

```
int set_operating_conditions
[-analysis_type bc_wc | on_chip_variation]
[-min min_condition]
[-max max_condition]
[-min_library min_lib]
[-max_library max_lib]
[-min_phys min_proc]
[-max_phys max_proc]
[-library lib]
[-object_list objects]
[condition]
```

set_opposite

Defines two input ports as logically opposite.

```
int set_opposite
port1
port2
```

set_optimize_dft_options

Defines options for physical design-for-test (DFT) optimization.

```
status set_optimize_dft_options
[-repartitioning_method none |
single_directional | multi_directional |
adaptive]
[-single_dir_option horizontal | vertical]
```

set_optimize_pre_cts_power_options

Specifies options for the optimize_pre_cts_power command.

```
status set_optimize_pre_cts_power_options
[-default]
[-honor_dont_touch]
[-honor_size_only]
[-psyn_constraint_file file_name]
[-cts_constraint_file file_name]
[-split_clock_gates true | false]
```

set_output_delay

Sets output delay on pins or output ports relative to a clock signal.

```
int set_output_delay
delay_value
[-clock clock_name [-clock_fall]
[-level_sensitive]]
[-network_latency_included]
[-source_latency_included]
[-rise]
[-fall]
[-max]
[-min]
[-add_delay]
[-group_path group_name]
port_pin_list
```

set_pad_physical_constraints

Sets physical constraints per pad instance.

```
status set_pad_physical_constraints
-pad_name stringpad_name objects
 | [-side side_number]
[-order order_number]
[-offset offset_distance]
[-orientation reflect | optimizeReflect]
[-min_left_iospace min_space_left]
[-min_right_iospace min_space_right]
```

set_parameter

Sets parameters for placement and routing operations.

Equivalent Scheme commands:

```
axSetIntParam, axSetRealParam
```

```
int set_parameter
-name name
-value value
[-module {route | groute | droute |
trackAssign | ek | preroute | sr}]
[-type {{int | integer} | {real | float} |
string}]
```

set_physical_signoff_options

Sets the environment setting for IC Validator (ICV) or Hercules before executing the signoff_drc or signoff_metal_fill command, and so on.

```
status set_physical_signoff_options
[-default]
[-exec_cmd icv | hercules]
[-drc_runset filename]
[-fill_runset filename]
[-mapfile filename]
[-dp_hosts {list_of_dp_hosts}]
[-num_cpus integer]
```

set_physopt_cpulimit_options

Specifies the options for performing a CPU-limited optimization.

```
status set_physopt_cpulimit_options
[-name limit_name]
[-mode max_delay | design_rule | max_area |
tns | max_static_power]
[-absolute_time absolute_time_value]
[-absolute_cost absolute_cost_value]
[-delta_time delta_time_value]
[-delta_cost delta_cost_value]
[-path_group path_group_name]
[-remove]
```

set_pin_name_synonym

Defines synonyms for pin names.

```
Boolean set_pin_name_synonym
[-full_name]
[-force]
pin_name_synonym
pin_name
```

set_pin_physical_constraints

Sets physical constraints per pin instance.

```
status set_pin_physical_constraints
[-pin_name pin_name]
[-cell cell_name]
[-layers layers]
[-width pin_width]
[-depth pin_depth]
[-side side_number]
[-offset offset_distance]
[-order order_number]
[-off_edge {center | location | auto}]
[-location point]
[objects
```

set_place_opt_cts_strategy

Specifies clock-tree-related options for the place_opt -cts command.

```
status set_place_opt_cts_strategy
[-operating_condition min | max(default) |
min_max]
[-no_clock_route]
[-inter_clock_balance]
[-fix_hold]
[-update_clock_latency]
```

set_pnet_options

Sets up placement tools to avoid power strap violations.

```
int set_pnet_options
[-partial | -complete | -none]
[-min_height height_threshold]
[-min_width width_threshold]
[-no_via_additive]
[-density value]
[-see_object object_type_names]
layer_names
```

set_port_fanout_number

Sets the number of external fanout points driven by specified ports in the current design.

```
status set_port_fanout_number
fanout_number
port_list
```

set_port_location

Annotates the specified top-level port with x- and y-coordinates and layer geometry, which the tool uses when running the reoptimize_design command.

```
status set_port_location
[-coordinate {x y}]
[-layer_name layer_name]
[-layer_area {lx ly ux uy}]
[-append]
port_name
```

set_power_guide

Sets an existing exclusive movebound as power guide or power well. This power guide will be used as always-on power_guide.

```
status set_power_guide
-name exclusive_movebound_name
[-guard_band_x horizontal_guard_band_width]
[-guard_band_y vertical_guard_band_width]
```

set_power_net_to_voltage_area

Links, unlinks, or reports power nets for the specified voltage area.

```
status set_power_net_to_voltage_area
[-action link | unlink | report]
[-voltage_area
voltage_area_name_voltage_area_name]
[-power_net net_name]
```

set_power_options

Specifies options for power optimization.

```
status set_power_options
[-default]
[-leakage true | false]
[-dynamic true | false]
[-low_power_placement true | false]
[-clock_gating true | false]
[-leakage_effort low | high]
[-dynamic_effort low | high]
```

set_prefer

Sets the preferred attribute on specified library cells.

```
integer set_prefer
[-min]
cell_list
```

set_preferred_routing_direction

Sets the preferred routing direction for the specified routing layers.

Equivalent Scheme command:

```
axgDefineWireTracks
```

```
string set_preferred_routing_direction
-layers list_of_layers
-direction horizontal | vertical
```

set_preroute_advanced_via_rule

Sets preroute advanced via rule options.

```
integer set_preroute_advanced_via_rule
[-move_via_to_center]
[-offset_both_sides]
[-x_offset_recommended]
[-y_offset_recommended]
[-x_offset distance]
[-y_offset distance]
[-x_step distance]
[-y_step distance]
[-cut_layer layer]
[-contact_code contact]
[-size_by_via_area {distance distance}]
[-size_by_array_dimensions {int int}]
[-rotation_mode on | required | off]
```

set_preroute_drc_strategy

Sets preroute drc options to change the internal rules for design rule checking in the following power and ground commands: create_rectangular_rings, create_pad_rings, create_power_straps, create_preroute_vias, preroute_instances, and preroute_standard_cells.

```
status set_preroute_drc_strategy
[-spacing_rules radial | manhattan]
[-protect_pin_access_edge]
[-protect_pin_access_edge_within_pin_layer_p
itch]
[-protect_pin_access_edge_within_range
protect_range]
[-treat_fat_blockage_as_fat_wire]
[-use_fat_via]
[-ignore_std_cells]
[-ignore_top_level_pins]
[-ignore_same_net_check]
[-quick_check]
[-merge_thin_wires]
[-no_design_rule]
[-report_fail]
[-jog_range jog_range_distance]
[-min_layer min_layer]
[-max_layer max_layer]
[-honor_shapes_of_nets collection_of_nets |
ALL]
```

set_preroute_special_rules

Defines a set of special rules to be honored by the create_power_straps and preroute_instances preroute commands.

```
status set_preroute_special_rules
-name name
[-do_not_connect_pins]
[-extension_layers ext_layers_list]
[-extension_width segments_width]
[-extension_space space_between_segments]
[-extension_count {min_count max_count}]
[-extension_via_array {columns_count
rows_count}]
[-extension_try_jog conn_length_threshold]
[-leave_space_for_io_connections]
[-resolve_conflicts_by_jogs]
[-connection_point_default {offset pitch}]
[-connection_point_layers
conn_pt_layers_list]
[-connection_point_offsets offsets_list]
[-connection_point_pitches pitches_list]
[-first_strap_offset first_strap_offset]
[-strap_endcap strap_endcap_distance]
[-create_local_straps min_dist_threshold]
[-keep_straps_in_standard_cell_area]
[-macro_cells {macro_cells_collection}]
[-pin_layer pin_layer_name]
[-strap_to_pin_offset strap_to_pin_offset]
[-end_point_offset
end_point_offset_distance]
[-target_area {{dx-left dy-bottom} {dx-right
dy-top}}]
[-target_layer target_layer_name]
[-jog_horizontal_layers h_layers_list]
[-jog_vertical_layers v_layers_list]
[-jog_width {h_segments_width
v_segments_width}]
```

set_primetime_options

Sets up PrimeTime options for the signoff_opt command.

```
status set_primetime_options
[-default]
[-exec_dir string]
[-sdc_file string]
[-max_image string]
[-min_image string]
[-setup_slack_limit float]
[-hold_slack_limit float]
[-common_file string]
[-specific_file string]
[-license_limit integer]
```

set_propagated_clock

Specifies propagated clock latency.

```
string set_propagated_clock
object_list
```

set_pulse_clock_cell

Specifies the pulse type for a pulse clock cell with a single input and a single output.

```
string set_pulse_clock_cell
-type pulse_type
object_list
```

set_qtm_global_parameter

Sets a global parameter for quick timing models (QTMs).

```
string set_qtm_global_parameter
[-param parameter]
[-lib_cell lib_cell]
[-pin pin_name]
[-clock pin_name]
[-value parameter_value]
```

set_qtm_port_drive

Sets the drive on quick timing model (QTM) ports.

```
string set_qtm_port_drive
[-type drive_type]
[-value drive_value]
[-input_transition_rise rtrans]
[-input_transition_fall ftrans]
port_list
```

set_qtm_port_load

Sets the load on quick timing model (QTM) ports.

```
string set_qtm_port_load
[-type load_type]
[-factor multiplication_factor]
[-value load_value]
port_list
```

set_qtm_technology

Sets quick timing model technology variables.

```
string set_qtm_technology
[-library name]
[-max_transition max_trans_value]
[-min_transition min_trans_value]
[-max_capacitance max_cap_value]
[-min_capacitance min_cap_value]
[-wire_load_model wlm_name]
[-process process_value]
[-voltage voltage_value]
[-temperature temperature_value]
```

set_rail_options

Specifies setup options for the analyze_rail command.

```
status set_rail_options
[-default]
[-output_dir dir_name]
[-use_pins_as_pads true | false]
[-pad_master_file file_name]
[-pad_instance_file file_name]
[-user_defined_tap_file file_name]
[-packaging_file file_name]
[-vd_threshold value]
[-switching_activity {type file_name
strip_path}]
[-host machine_name]
[-pr_exec_dir dir_name]
[-pt_exec_dir dir_name]
[-sdc file_name]
[-spef file_name]
[-verilog file_name]
[-upf file_name]
```

set_register_merging

Sets the register_merging attribute on the specified cells or designs, allowing register merging optimization on the objects.

```
status set_register_merging
obj_list
[true | false]
```

set_register_type

Sets the latch_type or flip_flop_type attributes on designs or cell instances, to specify which sequential cells from the target library are to be used by the compile command.

```
int set_register_type
-latch example_latch -exact |
-flip_flop example_flip_flop [-exact]
[cell_or_design_list]
```

set_related_supply_net

Associates an external supply net to the port of the design.

```
status set_related_supply_net
[supply_net_name]
[-object_list objects]
[-reset]
[-ground ground_net_name]
[-power power_net_name]
```

set_resistance

Sets the resistance value on nets.

```
int set_resistance
value
[-min] [-max] net_list
```

set_retention

Defines the UPF retention strategy for the power domains in the design. This command is supported only in UPF mode.

```
status set_retention
retention_strategy
-domain power_domain
-retention_power_net retention_power_net
-retention_ground_net retention_ground_net
[-elements objects]
```

set_retention_control

Defines the UPF retention control signals for the defined UPF retention strategy. This command is supported only in UPF mode.

```
status set_retention_control
retention_strategy
-domain power_domain
-save_signal {save_signal high | low}
-restore_signal {restore_signal high | low}
```

set_route_flip_chip_options

Sets flip-chip router options.

```
status set_route_flip_chip_options
[-number_of_loops 1 | 2 | 3]
[-route_with_soft_macros true | false]
[-search_effort easy | normal | hard]
[-layer_spacing {layer_spacing_pairs}]
[-layer_width {layer_width_pairs}]
[-rule_name name]
[-nets | -nets_in_file nets_file]
[-output_unrouted_nets open_net_file]
[-design_style area_IO |
peripheral_without_corner_driver |
peripheral_with_corner_driver]
[-min_access_edge_length length]
```

set_route_mode_options

To set the mode for running zroute.

```
status set_route_mode_options
[-zroute true | false]
```

set_route_opt_strategy

Sets the nonpersistent options that influence route_opt.

```
status set_route_opt_strategy
[-default]
[-fix_hold_mode all | route_base]
[-xtalk_reduction_loops loop_count]
[-route_run_time_limit run_time]
[-search_repair_loops detail_loop_count]
[-optimize_wire_via_search_repair_loops
optimize_loop_count]
[-route_drc_threshold threshold]
[-eco_route_search_repair_loops
eco_routing_loop_count]
```

set_route_options

Set specific options into the internal router control database.

Equivalent Scheme command:

`axgSetRouteOptions`

```
status set_route_options
[-default]
[-groute_timing_driven true | false]
[-groute_timing_driven_weight number]
[-groute_skew_control true | false]
[-groute_skew_weight number]
[-groute_congestion_weight number]
[-groute_clock_routing normal | comb |
balanced]
[-groute_incremental true | false]
[-track_assign_timing_driven true | false]
[-track_assign_timing_driven_weight number]
[-droute_connect_tie_off true | false]
[-droute_connect_open_nets true | false]
[-droute_reroute_user_wires true | false]
[-droute_CTS_nets normal |
minor_change_only]
[-droute_single_row_column_via_array center
| optimize]
[-droute_stack_via_less_than_min_area forbid
| add_metal_stub]
[-droute_stack_via_less_than_min_area_cost
number]
[-poly_pin_access auto | off]
[-drc_distance diagonal | manhattan]
[-same_net_notch ignore | check_and_fix]
[-fat_wire_check quick | merge_then_check]
[-merge_fat_wire_on preroute_only |
preroute_signal | preroute_signal_blockage]
[-fat_blockage_as thin_wire | fat_wire]
[-wire_contact_eol_rule ignore |
check_and_fix]
```

set_route_type

Sets the route type of a group of objects.

Equivalent Scheme commands:

```
axgMarkRouteType, dbSetNetType
```

```
status set_route_type
[-signal detail_route | user]
[-clock ring | strap | tie_off | user]
[-pg ring | strap | tie_off | user |
std_cell_pin_conn | macro/IO_pin_conn]
objects
objects
```

set_route_zrt_common_options

Sets the options common to all phases of routing.

```
status set_route_zrt_common_options
[-child_process_net_threshold int]
[-concurrent_redundant_via_mode off |
reserve_space | insert_at_high_cost
[-concurrent_redundant_via_effort_level low
| medium | high]]
[-eco_route_concurrent_redundant_via_mode
off | reserve_space
[-eco_route_concurrent_redundant_via_effort_
level low | medium | high]]
[-connect_within_pins list of {layer
off/via_standard_cell_pins/via_wire_standard
_cell_pins/via_all_pins/via_wire_all_pins}
pairs(off | via_wire_standard_cell_pins |
via_standard_cell_pins | via_wire_all_pins |
via_all_pins)]
[-enforce_voltage_areas off | strict |
relaxed]
[-extra_nonpreferred_direction_wire_cost_
multiplier {{layer multiplier}...}]
[-extra_preferred_direction_wire_cost_
multiplier {{layer multiplier}...}]
[-extra_via_cost_multiplier {{layer
multiplier}...}]
[-freeze_layer {{layer true | false}...}]
[-freeze_via_to_frozen_layer true | false]
[-mark_clock_nets_minor_change true | false]
[-max_layer_mode soft | allow_pin_connection
| hard]
[-max_number_of_threads int]
[-min_layer_mode soft | allow_pin_connection
| hard]
```

```
[-number_of_vias_over_max_layer int]
[-number_of_vias_under_min_layer int]
[-off_grid_routing_mode allow_off_grid |
allow_end_points_off_grid | no_off_grid]
[-plan_group_aware off | all_routing |
top_level_routing_only]
[-post_detail_route_redundant_via_insertion
off | low | medium | high]
[-read_user_metal_blockage_layer true |
false]
[-reroute_clock_shapes true | false]
[-reroute_user_shapes true | false]
[-rotate_default_vias true | false]
[-route_soft_rule_effort_level off | min |
low | medium | high]
[-route_top_boundary_mode
stay_half_min_space_inside | stay_inside |
ignore]
[-single_connection_to_pins off |
standard_cell_pins | all_pins]
[-standard_cell_blockage_as_thin true |
false]
[-threshold_noise_ratio ratio]
[-track_auto_fill true | false]
[-verbose_level int]
[-via_array_mode off | swap | rotate | all]
[-wide_macro_pin_as_fat_wire true | false]
[-default true | false]
```

set_route_zrt_detail_options

Sets the options for detail routing.

```
set_route_zrt_detail_options
[-antenna true | false]
[-antenna_on_iteration num]
[-antenna_verbose_level num]
[-check_antenna_on_pg true | false]
[-check_pin_min_area_min_length true |
false]
[-check_port_min_area_min_length true |
false]
[-elapsed_time_limit limit]
[-default true | false]
[-default_diode_protection real]
[-default_gate_size real]
[-default_port_external_antenna_area real]
[-default_port_external_gate_size real]
[-diagonal_min_width true | false]
[-diode_libcell_names lib_cells]
[-eco_route_use_soft_spacing_for_timing_
optimization true | false]
```

```
[-force_max_number_iterations true | false]
[-generate_extra_off_grid_pin_tracks true |
false]
[-generate_off_grid_feed_through_tracks off
| low | medium | high]
[-ignore_drc {{same_net_metal_space |
same_net_enclosed_cut_space |
all_same_net_drc_for_frozen_net
[-ignore_var_spacing_to_blockage true |
false]
[-ignore_var_spacing_to_pg true | false]
[-insert_diodes_during_routing true | false]
[-max_antenna_pin_count int]
[-merge_gates_for_antenna true | false]
[-optimize_tie_off_effort_level off | low |
high]
[-optimize_wire_via_effort_level off | low |
medium | high]
[-pin_taper_mode default_width | pin_width |
off]
[-port_antenna_mode float | jump |
top_layer]
[-save_after_iterations iter_list]
[-save_cell_prefix prefix]
[-reshield_rerouted_nets off | unshield |
reshield]
[-reuse_filler_locations_for_diodes true |
false]
[-timing_driven true | false]
[-top_layer_antenna_fix_threshold int]
[-use_default_width_for_min_area_min_len_stu
b true | false]
[-use_wide_wire_to_input_pin true | false]
[-use_wide_wire_to_macro_pin true | false]
[-use_wide_wire_to_output_pin true | false]
[-use_wide_wire_to_pad_pin same_as_macro_pin
| true | false]
[-use_wide_wire_to_port same_as_macro_pin |
true | false]
[-user_defined_partition {llx lly urx ury}]
[-var_spacing_to_same_net true | false]
```

set_route_zrt_global_options

Sets the options for global routing.

```
status set_route_zrt_global_options
[-clock_topology comb | normal]
[-comb_distance int]
[-comb_max_connections int]
[-congestion_map_only true | false]
[-crosstalk_driven true | false]
[-default true | false]
[-effort minimum | low | medium | high]
[-macro_boundary_track_utilization int]
[-macro_boundary_width int]
[-macro_corner_track_utilization int]
[-timing_driven true | false]
```

set_route_zrt_track_options

Sets the options for track assignment.

```
status set_route_zrt_track_options
[-crosstalk_driven true | false]
[-default true | false]
[-timing_driven true | false]
```

set_row_type

Sets a specified row type attribute on the specified rows.

```
status set_row_type
[-site site_name row_name_list]
-type row_type
```

set_rp_group_options

Sets relative placement group attributes on the specified relative placement groups.

```
collection set_rp_group_options
rp_groups
[-alignment bottom-left | bottom-pin |
bottom-right]
[-pin_align_name pin_name]
[-utilization percentage]
[-ignore]
[-x_offset float]
[-y_offset float]
[-compress]
[-cts_option fixed_placement | size_only]
[-route_opt_option fixed_placement |
in_place_size_only]
[-psynopt_option fixed_placement |
size_only]
[-move_effort low | medium | high]
[-allow_keepout_over_tapcell false | true]
```

set_scaling_lib_group

Specifies the scaling_lib_group to use for the current design, or a subdesign.

```
status set_scaling_lib_group
[-min min_group]
[-max max_group]
[-object_list objects]
[group]
```

set_scan_pin_type

Sets the scan-in or scan-out type for the specified pin.

```
status set_scan_pin_type
-type in | out
-pin pin | -ref_pin physical_lib_pin
```

set_scenario_options

Sets the scenario options for one or more scenarios.

```
status set_scenario_options
[-scenarios scenario_list]
[-leakage_only true | false]
[-hold_only true | false]
[-setup true | false]
[-hold true | false]
[-leakage_power true | false]
[-dynamic_power true | false]
[-reset_all true | false]
```

set_scope

Specifies the current UPF scope. This command is supported only in UPF mode.

```
string set_scope
[instance]
```

set_separate_process_options

Sets options controlling whether IC Compiler uses separate OS processes for extraction, placement and routing.

```
status set_separate_process_options
[-extraction true | false]
[-placement true | false]
[-routing true | false]
```

set_si_options

Defines signal integrity options used for analysis or optimization.

Equivalent Scheme commands:

```
ataIgnoreXtalk, ataIncludeXtalk
```

```
status set_si_options
[-delta_delay true | false]
[-static_noise true | false]
[-timing_window true | false]
[-min_delta_delay true | false]
[-static_noise_threshold_above_low
threshold_value]
[-static_noise_threshold_below_high
threshold_value]
[-route_xtalk_prevention true | false]
[-route_xtalk_prevention_threshold
threshold_value]
[-analysis_effort low | medium]
[-max_transition_mode normal_slew |
total_slew]
[-reselect true | false]
```

set_size_only

Sets a list of attributes on specified leaf cells so that they can be sized only in optimization during compile.

```
int set_size_only
[-all_instances]
object_list
flag
```

set_skew_group

Creates a new user-defined skew group.

```
set_skew_group
[-name ]
[-target_skew desired_skew]
[-target_early_delay
minimum_insertion_delay]
list_of_sink_pin or net_name
```

set_spacing_label_rule

Sets intercell spacing constraint between reference cells that have been assigned labels with set_lib_cell_spacing_label command.

```
status set_spacing_label_rule
-labels {list_of_label_names}
{min max}
```

set_split_clock_gates_options

Set options for the split_clock_gates command.

```
status set_split_clock_gates_options
[-slack_margin margin_value]
[-honor_dont_touch]
[-honor_size_only]
```

set_starrcxt_options

Sets up StarRCXT options for the signoff_opt command.

```
status set_starrcxt_options
[-default]
[-exec_dir string]
[-max_nxtgrd_file string]
[-min_nxtgrd_file string]
[-map_file string]
[-num_parts integer]
[-mode 100 | 150 | 200 | 400]
[-option_file string]
[-min_image string]
[-max_image string]
```

set_switching_activity

Sets switching activity annotation on nets, pins, ports and cells of the current design.

```
int set_switching_activity
[-static_probability sp_value]
[-toggle_rate tr_value]
[-state_dep state_condition]
[-path_dep path_sources]
[-rise_ratio ratio_value]
[-period period_value | -clock clock_name]
[-select select_types]
[-hier]
[-instances instances]
[object_list]
[-verbose]
```

set_synlib_dont_get_license

Specifies a list of synthetic library part licenses that are not automatically checked out.

```
int set_synlib_dont_get_license
license_list
```

set_target_library_subset

Restricts optimization of a block to use a given subset of the target_library, for cases where operating condtion alone is not sufficient to define the subset.

```
int set_target_library_subset
[-object_list cells]
[-top]
library_list
[-milkyway_reflibs milkyway_reflib_paths]
```

set_timing_derate

Sets derate factors on the current design or specified objects. Derate factors specify upper and lower limits on delays for a particular operating condition.

```
int set_timing_derate
[-min]
[-max]
[-early]
[-late]
[-clock]
[-data]
[-net_delay]
[-cell_delay]
[-cell_check]
value
object_list
```

set_timing_ranges

Sets timing ranges for the current design.

```
int set_timing_ranges
[timing_ranges]
[-library library_name]
```

set_tlu_plus_files

Sets the files used for TLUPlus extraction.

```
int set_tlu_plus_files
[-max_tluplus max_tluplus_string]
[-min_tluplus min_tluplus_string]
[-max_emulation_tluplus max_emul_string]
[-min_emulation_tluplus min_emul_string]
[-tech2itf_map mapping_file]
```

set_true_delay_case_analysis

Sets the true_delay_case_analysis attribute, which specifies the input vector value to use for specified pins or ports of the current design with the -true and -justify options of report_timing.

```
status set_true_delay_case_analysis
0 | 1 | r | f | none
port_pin_list
```

set_unconnected

Lists output ports to be unconnected.

```
int set_unconnected
port_list
```

set_undoable_attribute

Sets an attribute to a specified value on the specified list of objects with support for undo.

```
collection set_undoable_attribute
[-class class_name]
object_list
attribute_name
[-quiet]
```

set_ungroup

Sets the ungroup attribute on specified designs, cells, or references, indicating that they are to be ungrouped during compile.

```
int set_ungroup
object_list true | false
```

set_unix_variable

This is a synonym for the setenv command.

set_user_grid

Sets the user grid for this session.

```
status set_user_grid
[-x_offset float]
[-y_offset float]
[-x_step float]
[-y_step float]
[-user_grid {{x_offset y_offset} {x_step
y_step}}]
[-x_get_from_layer layer]
[-y_get_from_layer layer]
[-reset]
[design]
```

set_via_array_size

Modifies the array size of an existing via or via array.

```
collection set_via_array_size
-array_size {row col}
via_collection
```

set_voltage

Applies an operating voltage on a list of supply nets objects.

```
int set_voltage
max_case_voltage
[-min min_case_value]
-object_list list_of_supply_nets
```

set_vt_filler_rule

Sets multiple threshold voltage filler cell insertion rules.

```
integer set_vt_filler_rule
-threshold_voltage
-lib_cell
```

set_write_stream_options

Sets options for the write_stream command.

```
status set_write_stream_options
[-reset]
[-map_layer layer_mapping_file_name]
[-rename_cell cell_renaming_file_name]
[-child_depth child_cell_depth]
[-skip_ref_lib_cells]
[-resize_text {width
text_conversion_factor}]
[-flatten_via]
[-contact_prefix $$]
[-output_filling {list_of_types}]
[-output_outdated_fill]
[-output_instance_name_as_property
inst_prop_value]
[-output_geometry_property]
[-remove_backslash_from_instance_net_names]
[-max_name_length max_name_length]
[-keep_data_type]
[-output_by_layer {layer_number_strings}]
[-oasis_compression_level
compress_level_value]
[-compressed]
[-output_pin {output_pin_types}]
[-pin_name_mag pin_name_mag]
[-net_name_mag net_name_mag]
[-output_net {output_net_types}]
[-output_net_name_as_property
net_prop_value]
[-output_polygon_pin]
[-output_design_intent]
[-design_intent_cell_name di_struct_name]
[-critical_object_names
critical_inst_net_name_list]
[-map_design_intent_layers
di_layer_mapping_file_name]
[-design_intent_only]
[-rotate_pin_text_by_access_dir]
[-set_hier_instance_name_long]
[-set_hier_net_name_long]
[-ignore_layer_mapping_for_imported_cells]
```

set_xtalk_route_options

Sets global route and track assignment crosstalk options.

```
status set_xtalk_route_options
[-default]
[-groute_minimize_xtalk true | false]
[-groute_xtalk_weight number]
[-track_assign_minimize_xtalk true | false]
[-track_assign_noise_threshold value]
```

set_zero_interconnect_delay_mode

Forces the timer to ignore the contribution on a timing path from any wire capacitance in the design.

Equivalent Scheme commands:

```
ataIgnoreInterconnect,
ataIgnoreWireDelay
```

```
status set_zero_interconnect_delay_mode
[true | false]
```

set_zrt_net_properties

Sets net properties for Zroute.

```
status set_zrt_net_properties
[-ignore_voltage_areas true | false]
-nets collection_of_nets
-from_file file_name
```

setenv

Sets the value of a system environment variable.

```
string setenv
variable_name new_value
```

sh

Executes a command in a child process.

```
string sh [args]
```

shape_fp_blocks

Automatically places and shapes plan group boundaries, black boxes, and other soft macros in a design core.

Equivalent Scheme commands:

`fphBlockPlacement, fphShapeDesign`

```
status shape_fp_blocks
[-rectilinear]
[-incremental target_utilization_driven |
congestion_driven]
[-channels]
[-refine_placement]
[-constraint_file file_name]
[-top_down]
[-sliver_threshold threshold]
[-place_submacros]
```

shell_is_in_upf_mode

Determines if the shell is in UPF mode.

```
status shell_is_in_upf_mode
```

signoff_drc

Detects 65nm and below process design rule checking (DRC) violations with foundry runset.

```
status signoff_drc
[-error_view errview_name]
[-check_all_layers]
[-read_cel_view]
[-ignore_child_cell_errors]
[-select_layers {collection_of_layers}]
[-select_rule {list_of_rule_names}]
[-unselect_rule {list_of_rule_names}]
[-bounding_boxes {{llx1 lly1} {urx1 ury1}
...}]
[-excluded_bounding_boxes {{llx1 lly1} {urx1
ury1} ...}]
[-run_dir string]
[-num_cpus integer]
```

signoff_metal_fill

Invokes Hercules or IC Validator to perform metal fill on current cells to meet the metal density requirements.

```
status signoff_metal_fill
[-output_view fillview_name]
[-purge]
[-eco]
[-append]
[-mode flat]
[-select_layers {layer_name}]
[-bounding_boxes {rectangle_list}]
[-excluded_bounding_boxes {rectangle_list}]
[-run_dir dir_path]
```

signoff_opt

Performs signoff ECO optimization.

```
status signoff_opt
[-effort low | medium | high]
[-only_psyn]
[-no_design_rule | -only_design_rule |
-only_hold_time]
[-xtalk_reduction | -only_xtalk_reduction]
[-full_extract | -full_analysis]
[-skip_initial_analysis]
[-num_iteration integer]
[-aocvm]
[-path_based_analysis]
[-update_rail_voltage]
[-variation]
[-ignore_design_readiness]
[-keep_license]
[-snapshot base_name]
```

size_cell

Relinks leaf cells to a new library cell that has the required drive strength (or other properties).

```
collection size_cell
cell_object
lib_cell_object
```

sizeof_collection

Returns the number of objects in a collection.

```
int sizeof_collection
collection1
```

skew_opt

Optimizes clock skews to increase timing slack and writes the solution to an output file. By default, the output file is named "skew_opt.tcl" and is automatically sourced.

```
status skew_opt
[-output file_name]
[-clock_balancing_only]
[-no_optimization]
[-no_auto_source]
[-fix_boundary_pins]
[-ignore_boundary_paths]
[-pins pin_list]
[-clocks clock_list]
[-path_groups path_group_list]
[-enable_pins]
[-macro_pins]
[-halfcycle_path_pins]
[-setup]
[-hold]
[-setup_margin setup_margin_value]
[-hold_margin hold_margin_value]
[-guard_band guard_band_value]
[-adjustment_limit adjustment_limit_value]
[-decrease_factor decrease_factor_value]
[-improvement_threshold
improvement_threshold_value]
[-resolution resolution_value]
```

slot_wire

Slots wide wires and contact arrays on selected nets by replacing them with thinner wires and smaller arrays.

Equivalent Scheme command: `axgSlotWire`

```
integer slot_wire
-nets {collection_of_nets}
[-signal_net]
[-cutwidth {layer distance list}]
[-cutlength {layer distance list}]
[-width {layer distance list}]
[-length {layer distance list}]
[-sidespace {layer distance list}]
[-endspace {layer distance list}]
[-sideclearance {layer distance list}]
[-endclearance {layer distance list}]
[-no_stagger {layer list}]
[-dmode {layer list}]
[-treat_width_as_max]
[-treat_length_as_min]
[-treat_space_clearance_min]
[-min_via_removal]
[-recreate_vias]
[-report]
[-report_wire_relationship file_name]
[-undo]
```

snap_objects

Snaps objects to the default snap type. An object is snapped onto the nearest position that satisfies the snapping constraint.

```
status snap_objects
[-snap_pin_to_edge]
objects
```

sort_collection

Sorts a collection based on one or more attributes, resulting in a new, sorted collection. The sort is ascending by default.

```
collection sort_collection
[-descending] collection1 criteria
```

sort_fp_pins

Sorts the specified collection of pins into alphabetic order by name or in reverse alphabetic order if -reverse is specified.

Equivalent Scheme command: `fphSortSMPins`

```
status sort_fp_pins
[-reverse]
pins
```

source

Read a file and evaluate it as a Tcl script.

```
string source
[-echo] [-verbose] [-continue_on_error] file
```

split_clock_gates

Replicates (splits) integrated clock-gating cells that have timing violations on the enable pin.

```
status split_clock_gates
```

split_clock_net

Duplicates the gates on the clock nets.

```
status split_clock_net
[-objects net_or_gate_list]
[-gate_sizing]
[-gate_relocation]
[-split_any_cell_type]
[-split_intermediate_level_clock_gates]
[-operating_condition min | max | min_max]
[-isolate_float_pins]
[-drive_ungated_registers]
[-estimated_early_delay float]
```

split_mw_lib

Splits the top-level Milkyway design into different libraries. Splitting the library hierarchically facilitates concurrent design.

Equivalent Scheme command: `dbHierSplit`

```
status split_mw_lib
[-check_only]
[-to_dir path]
[-lib_prefix prefix]
-from_library mw_lib
mw_top_design
```

split_net

Splits routing objects on one net into many other nets.

```
status split_net
-start | list_of_nets | -batch
[-cells cell_list]
```

split_objects

Splits one or more objects at the specified x or y coordinate or by a specified line.

Equivalent Scheme command: `geSplit`

```
new_objects split_objects
{-x float | -y float | -line line}
[-gap float]
objects
```

spread_spare_cells

Places the specified cells evenly throughout a rectilinear region.

Equivalent Scheme command:
`axgSpreadGroupCells`

```
status spread_spare_cells
cells
[-bbox spare_cells_region
 | -poly {{x1 y1} {x2 y2} ...}]
```

spread_zrt_wires

Spreads the wires in the opened cell for DFM.

```
spread_zrt_wires
[-min_jog_length min_ratio]
[-pitch number_of_pitches]
[-timing_preserve_nets {collection_of_nets}]
[-timing_preserve_setup_slack_threshold
slack_value
[-timing_preserve_hold_slack_threshold
slack_value
```

start_gui

Starts the application GUI.

```
string start_gui
[-file name_of_script_file]
[-no_windows]
[-- x_args ...]
```

stop_gui

Stops the application GUI.

```
string stop_gui
```

stretch_wire

Stretches given wires or contacts horizontally or vertically without loosing connections.

```
status stretch_wire
objects
{-x distance | -y distance}
[-snap_to_track yes | no | halftrack]
[-jog_layer same | up | down]
[-auto_repair_net]
[-end_point_range distance]
[-undo]
```

sub_designs_of

Gets the subdesigns according to the options.

```
collection sub_designs_of
[-hierarchy]
[-in_partition | -partition_only]
[-dt_only | -ndt_only]
[-multiple_instances | -single_instances]
[-names_only]
design
```

sub_instances_of

Gets the subinstances according to the options.

```
collection sub_instances_of
[-hierarchy]
[-in_partition] [-partition_only]
[-dt_only] [-ndt_only]
[-of_references reference_list]
[-master_instance]
[-names_only]
design
```

suppress_message

Disables printing of one or more informational or warning messages.

```
string suppress_message
[message_list]
```

swap_cell_locations

Swaps the locations of two cells.

```
int swap_cell_locations
cell1
[-cell1_orient N | W | S | E | FN | FE | FS |
FW]
[-cell2_orient N | W | S | E | FN | FE | FS |
FW]
```

syntax_check

Enables or disables the Syntax Checker's syntax_check mode which checks commands for syntax errors.

```
integer syntax_check
true | false
```

synthesize_fp_rail

Synthesizes power networks or power switch arrays based on user-specified constraints. In a single run, you can synthesize either a power network for a single voltage design, power networks for a multivoltage design, or a power switch array.

trace_scan_chain

Traces scan chain in the current design.

Equivalent Scheme command: `axgScanTrace`

```
status trace_scan_chain
[-from scan_input] [-to scan_output]
```

translate_zrt_parameters

Translates the routing parameters to Zroute.

```
status translate_zrt_parameters
[-output filename]
```

trim_fill_eco

Trims the metal fill. Use this command after you finish inserting metal fill and running ECO routing.

Equivalent Scheme command: `axgECOTrimFill`

```
status trim_fill_eco
[-input fill_view_name]
[-output fill_view_name]
[-spacing_to_routing number]
[-remove_vio_fill]
[-from_metal metal_layer_name]
[-to_metal metal_layer_name]
```

unalias

Removes one or more aliases.

```
string unalias
pattern
```

uncommit_fp_soft_macros

Transforms soft macros into plan groups.

Equivalent Scheme command:
`fphSoftMacroToPlanGroup`

```
status uncommit_fp_soft_macros
[-push_up_preroutes pg | none]
[-remove_feedthroughs]
[objects]
```

undo

Undoes the last operation.

```
status undo
[-all]
[-mark string]
```

undo_config

Configures the undo stack.

```
status undo_config
{-max_depth int | -max_memory int
 | -depth int
 | -memory int
 | -enable
 | -disable}
-enabled sbool
```

undo_mark

Marks a position in the undo stack to undo back to.

```
status undo_mark
mark
```

ungroup

Removes a level of hierarchy.

```
status ungroup
cell_list | -all
[-prefix prefix_name]
[-flatten]
[-simple_names]
[-soft]
[-small n]
[-force]
[-start_level n]
[-all_instances]
```

uniquify

Removes multiply-instantiated hierarchy in the current design by creating a unique design for each cell instance.

```
int uniquify
[-force]
[-base_name base_name]
[-cell cell_list]
[-reference design_name]
[-new_name new_design_name]
[-dont_skip_empty_designs]
```

uniquify_fp_mw_cel

Removes multiple-instantiated hierarchy lib cell in the current design or a specified design by creating a unique hierarchy lib cell for each hierarchy cell instance.

Equivalent Scheme command: `axgHierPlan`

```
status uniquify_fp_mw_cel
[-verbose]
[-store_mim_property cell_instances]
[design_name]
```

unset_hierarchy_color

Removes colors set on leaf cells.

```
status unset_hierarchy_color
[collection1]
```

unset_power_guide

Unsets an existing power guide to be just like an exclusive movebound.

```
unset_power_guide
[power_guide_list]
```

unsuppress_message

Enables printing of one or more suppressed informational or suppressed warning messages.

```
string unsuppress_message
[messages]
```

update_bounds

Updates an existing bound by adding or removing objects. The bound should be of type move bound.

```
int update_bounds
[-name bound_name]
[-bound bound_object]
[-add]
[-remove]
cell_list
```

update_clock_latency

Updates the latencies of real and virtual clock objects after clock tree synthesis.

```
status update_clock_latency
```

update_flip_chip_pin_locations

Updates the flip chip bump I/O pin locations for timing purposes.

Equivalent Scheme command:

```
fcCreateBumpTimingInfo
```

```
status_value update_flip_chip_pin_locations
```

update_lib

Reads in a specified library file and uses it to update an existing technology, synthetic, or symbol library.

```
int update_lib
[-overwrite] [-permanent] library_name
file_name [-no_warnings]
```

update_physical_bus

Updates an existing physical bus by adding or removing objects.

```
status update_physical_bus
physical_bus
-add net_list | -remove net_list
[-position position]
[-sort {ascending | descending | none}]
[-delimiter delimiter]
[-right_precedence]
[-quiet]
```

update_timing

Updates timing information on the current design.

```
int update_timing
```

update_voltage_area

Updates an existing voltage area by adding or removing logical hierarchies.

Equivalent Scheme command:

```
dbCreateVoltageArea
```

```
int update_voltage_area
-voltage_area list
[-add]
[-remove]
[-guard_band_x int]
[-guard_band_y int]
[modules]
```

verify_drc

Detects DRC violations.

Equivalent Scheme command: `geAdvDRC`

```
integer verify_drc
[-error_cell cell_name]
[-dir runset_directory]
[-ignore_width]
[-ignore_spacing]
[-ignore_area]
[-ignore_enclosed_area]
[-ignore_density]
[-ignore_min_edge_length]
[-check_via_size]
[-ignore_via_spacing]
[-ignore_adjacent_via]
[-ignore_min_via_number]
[-ignore_stack_level]
[-ignore_stackable]
[-check_enclosure]
[-check_end_of_line]
[-check_via_farm]
[-check_fat_poly_contact]
[-check_blockage]
[-ignore_child_cell]
[-read_cell_view]
[-check_cross_hier_short_only]
[-write_hercules_runset_only]
[-selected_area {{llx1 lly1} {urx1 ury1}
...}]
[-excluded_area {{llx1 lly1} {urx1 ury1}
...}]
[-exclude_by_cell_name
{collection_of_master_cells}]
[-offset_distance value]
```

verify_lvs

Checks for inconsistencies between the schematic and physical layout of the current design. Violations discovered by the check are written to a design error view (error cell). You can browse the error view with the IC Compiler Error Browser.

Equivalent Scheme command: `geNewLVS`

```
status verify_lvs
[-error_cell cell_name]
[-ignore_floating_port]
[-ignore_floating_net]
[-ignore_short]
[-ignore_open]
[-ignore_eeq_pin]
[-ignore_min_area]
[-use_notch_gap_fill_cell]
[-ignore_blockage_overlap]
[-check_single_pin_net_for_floating_port]
[-check_floating_port_on_null_net]
[-ignore_floating_metal_fill_net]
[-max_error ]
[-check_single_pin_net_for_floating_net]
[-check_short_locator]
[-check_open_locator]
```

verify_pg_nets

Checks whether or not all power and ground pins of standard cells, macro cells and pad cells are connected to the corresponding power and ground nets.

Equivalent Scheme command: `axgVeriPGConn`

```
integer verify_pg_nets
[-error_cell cell_name]
[-std_cell_pin_connection ( check | ignore)]
[-macro_pin_connection ( at_least_one | all
| ignore)]
[-pad_pin_connection ( at_least_one | all |
ignore)]
```

verify_route

Verifies and reports DRC violations and opens

Equivalent Scheme command:

```
axgRouterVerify
```

```
status verify_route
[-nets {collection_of_nets}]
[-no_drc]
[-no_opens]
[-antenna]
[-top_layer_probe_constraints]
[-num_cpu int]
[-bounding_box {{llx lly} {urx ury}}]
[-output file_name]
```

verify_zrt_route

Verifies and reports design rule constraint (DRC) violations, net opens, antenna rule violations, and voltage area rule violations.

```
status verify_zrt_route
[-nets {collection_of_nets}]
[-open_net true | false]
[-report_all_open_nets true | false]
[-drc true | false]
[-antenna true | false]
[-voltage_area true | false]
[-check_from_user_shapes true | false]
```

which

Locates a file and displays its pathname.

```
string which
filename_list
```

while

Loop execution control structure.

widen_zrt_wires

Performs wire widening.

```
status widen_zrt_wires
[-timing_preserve_nets {collection_of_nets}]
[-timing_preserve_setup_slack_threshold
slack_value
[-timing_preserve_hold_slack_threshold
slack_value
```

win_select_objects

Creates a collection of objects equivalent to a graphical selection operation.

Equivalent Scheme commands: `geLineSelect, geWindowSelect`

```
string win_select_objects
[-slct_targets slct_bus]
[-slct_targets_operation operation]
[-create_slct_buses]
[-root instance]
[ -within rectangle | -line line |-at point
|
 -radius r | -again_at ]
[-intersect]
[-index i]
```

win_set_filter

Sets a filter to apply to objects selected by the win_select_objects command.

```
int win_set_filter
-class class_name
[ -level level ]
[ -filter expression ]
[ -layer list ]
[-highlighted_only true|false ]
```

win_set_select_class

Sets the design objects to be collected by the win_select_objects command.

```
string win_set_select_class
{-all | class_names}
```

window_stretch

Stretches one or more objects by moving the objects points or edges that are containing within a bounding box

```
status window_stretch
-delta vector
-rectangle rect
[-keep_placement]
[-keep_pad_to_core_distance]
[-ignore_fixed]
objects
```

write

Writes a design netlist or schematic from memory to a file.

```
status write
[-format output_format]
[-hierarchy]
[-no_implicit]
[-modified]
[-output output_file_name]
[-names_file name_mapping_files]
[-donot_expand_dw]
[-scenarios scenario_list]
[design_list]
[-library library_name]
```

write_app_var

Writes a script to set the current variable values.

```
string write_app_var
-output file
[-all | -only_changed_vars]
[pattern]
```

write_def

Writes the design data of the specified design to a file in DEF format, including the physical layout, netlist, and design constraints.

Equivalent Scheme command: `write_def`

```
status write_def
-output output_file_name
[-version 5.3 | 5.4 | 5.5 | 5.6 | 5.7]
[-unit conversion_factor]
[-compressed]
[-rows_tracks_gcells]
[-vias]
[-all_vias]
[-nondefault_rule]
[-lef lef_file_name]
[-regions_groups]
[-components]
[-macro]
[-fixed]
[-placed]
[-pins]
[-blockages]
[-specialnets]
[-notch_gap]
[-pg_metal_fill]
[-nets]
[-routed_nets]
[-diode_pins]
[-floating_metal_fill]
[-scanchain]
[-no_legalize]
[-verbose]
```

write_design_lib_paths

Writes into a file the paths to which design libraries are mapped.

```
status write_design_lib_paths
[-filename file_name]
[-dc_setup]
```

write_environment

Writes the variable settings and constraints for the specified cells or designs.

```
return_val write_environment
[-cells cell_list | -designs design_list]
[-format dcsh | dctcl]
[-output file_name]
[-suffix suffix]
[-environment_only]
[-constraints_only]
[-no_lib_info]
[-consistency]
```

write_flip_chip_bumps

Write bump locations and connected nets to a specified AIF format file.

```
status write_flip_chip_bumps
file_name
```

write_flip_chip_nets

Writes the flip-chip nets into a text file.

```
status write_flip_chip_nets
-file_name nets_file
```

write_floorplan

Writes a Tcl script that can be used to recreate elements of the floorplan of the specified design.

Equivalent Scheme command:

```
axgDumpFloorPlan
```

```
status write_floorplan
[-placement {io std_cell hard_macro
soft_macro}
[-create_terminal]]
[-row]
[-track]
[-no_bound]
[-create_bound]
[-no_placement_blockage]
[-no_route_guide]
[-preroute]
[-no_plan_group]
[-no_voltage_area]
[-no_create_boundary]
[-pin_guide]
[-objects heterogeneous_collection]
[-all]
[-cell design_name]
[-sm_placement {io std_cell hard_macro
soft_macro}]
[-sm_placement_blockage]
[-sm_route_guide]
[-sm_plan_group]
[-sm_voltage_area]
[-sm_bound]
[-sm_cell_row]
[-sm_track]
[-sm_preroute]
[-sm_all]
file_name
```

write_interface_timing

Generates an interface timing ASCII report for a gate-level netlist or an interface logic model (ILM).

```
int write_interface_timing
file_name
[-ignore_ports port_list]
[-significant_digit digits]
[-nosplit]
```

write_io_constraints

Writes an I/O constraints file.

Equivalent Scheme command:
`ioDumpIOLocation`

```
status write_io_constraints
[-library lib_name]
[-cell cell_name]
[-constraint_type side_only | side_order |
side_location]
[-pin_only | -pad_only]
file_name
```

write_lib

Writes a compiled library to disk in Synopsys database, EDIF, or VHDL format.

```
int write_lib
library_name
[-format db | edif | vhdl]
[-compress compression_format]
[-output file_name]
[-names_file file_list]
[-macro_only]
```

write_link_library

Writes shell commands to save the current link library settings for design instances.

```
int write_link_library
[-full_path_lib_names] [-nosplit]
[-full_path_lib_names] [-nosplit]
[-output file_name]
[-target target]
```

write_mw_lib_files

Writes the technology, or plib, or reference control file of the Milkyway library.

Equivalent Scheme command: `cmDumpTech`

```
status_value write_mw_lib_files
[-technology]
[-plib]
[-reference_control_file]
-output file_name
libName
```

write_parasitics

Writes parasitics to a disk file for delay calculation tools.

```
status write_parasitics
[-output file_name]
[-format SPEF | SBPF]
[-compress]
[-routed_nets_only]
[-no_name_mapping]
```

write_physical_constraints

Writes floorplan information in Tcl format for use in Design Compiler topographical mode.

```
status write_physical_constraints
-output tcl_file
[-port_side]
```

write_physical_script

Writes a Tcl script to save the current physical settings.

```
status write_physical_script
-mpc
-nosplit
-output file_name
```

write_plib

Writes the library data of the specified library to a file in Synopsys physical library (.plib) format.

```
int write_plib
[-lib_name lib_name]
[-cell_name cell_name]
[-ignore_tech_info]
[-signal_em_only]
[-antenna_rule_only]
[-cell_info]
[-ignore_cell_geom]
[-antenna_prop_only]
[-metal_density_only]
[-basic_cell_pin_info_only]
plib_file_name
```

write_qtm_model

Writes the Quick Timing Model (QTM) file.

```
string write_qtm_model
-out_dir output_qtm_directory
[-text]
```

write_route

Writes the routing information to the specified file.

Equivalent Scheme command: `axgDumpRouting`

```
status write_route
-output file_name
[-nets collection_of_nets]
[-skip_route_guide]
[-output_metal_fill]
[-objects collection_of_objects]
```

write_rp_groups

Writes out the relative placement constraints for the specified relative placement groups.

```
collection write_rp_groups
rp_groups | -all
[-hierarchy]
[-quiet]
[-nosplit]
[-output filename]
[-create]
[-leaf]
[-keepout]
[-instance]
[-include]
```

write_script

Writes shell commands to save the current settings.

```
int write_script
[-no_annotated_check] [-no_annotated_delay]
[-no_cg]
[-full_path_lib_names] [-nosplit]
[-format dctcl | dcsh]
[-include loop_breaking]
[-output file_name]
```

write_sdc

Writes out a script in Synopsys Design Constraints (SDC) format.

Equivalent Scheme commands: `ataDumpSDC, ataWriteTC`

```
int write_sdc
file_name
[-nosplit]
[-version sdc_version]
```

write_sdf

Writes a Standard Delay Format (SDF) back-annotation file.

Equivalent Scheme command: `ataDumpSDF`

```
string write_sdf
[-version sdf_version] [-significant_digits
digits]
[-instance inst_name]
file_name
```

write_stream

Writes a design (library) into a GDSII or Oasis file.

```
status write_stream
[-lib_name lib_name]
[-format gds | oasis]
[-cells list_of_cells]
[-cell_file cell_name_file]
stream_file_name
```

write_verilog

Outputs a hierarchical Verilog file for the current design.

Equivalent Scheme command:

`astDumpHierVerilog`

```
status write_verilog
[-pg]
[-split_bus]
[-empty_module]
[-no_physical_only_cells]
[-no_pg_pin_only_cells]
[-no_corner_pad_cells]
[-no_pad_filler_cells]
[-no_core_filler_cells]
[-no_flip_chip_bump_cells]
[-no_cover_cells]
[-no_chip_cells]
[-no_io_pad_cells]
[-no_tap_cells]
[-no_unconnected_cells]
[-unconnected_ports]
[-keep_backslash_before_hiersep]
[-diode_ports]
[-wire_declaration]
[-output_net_name_for_tie]
[-macro_definition]
[-force_output_references reference_names]
[-force_no_output_references
reference_names]
verilog_file_name
```

Scheme to IC Compiler Command Mapping

Scheme Command	IC Compiler Command
aprCmdEnlargeFC	expand_flip_chip_cell_locations
aprCreateVoltageArea	create_voltage_area
aprCrossVANet	check_mv_design -level_shifters
aprPGConnect	derive_pg_connection
aprReplaceChildCell	change_macro_view
astAreaRecovery	psynopt -only_area_recovery route_opt -area_recovery
astAutoPlace	place_opt psynopt
astCTO	optimize_clock_tree

astCTOInterClocksBalance	balance_inter_clock_delay
astCTS	compile_clock_tree
astCTSBasic	compile_clock_tree -config_file_read
astCheckDesignForCTS	report_clock_tree
astClockOptions	set_clock_tree_options
astClockTiming	report_clock_timing
astDeleteClockTree	remove_clock_tree
astDumpHierVerilog	write_verilog write -format verilog
astFanoutSetup	create_buffer_tree
astHFCTS	create_buffer_tree
astHoldFix	set_fix_hold
astInsertLevelShifter	insert_level_shifters
astLenBI	set_max_net_length
astMagnetPlace	magnet_placement
astMarkClockTree	mark_clock_tree
astPlaceDesign	create_placement
astPlaceFcOptions	set_flip_chip_options
astPostGR	route_opt -stage global
astPostPS	place_opt psynopt
astPostPS1	psynopt
astPostRT	route_opt
astPostRouteOpt	route_opt
astPowerRecovery	place_opt -power_mode route_opt -power_mode
astPrePS	place_opt
astReportClockTreePower	report_clock_tree_power
astReportTiming	report_timing
astSetClockCell	set_clock_tree_references
astSetDontUse	set_attribute remove_attribute set_dont_use
astSkewAnalysis	report_clock_tree
astSplitClockNet	split_clock_net
astTimingDataCheck	check_timing

astTopoHold	set_fix_hold
ataDefineIgnorePin	set_clock_tree_exceptions -exclude_pins
ataDefineSyncPins	set_clock_tree_exceptions -float_pins
ataDisableGatingClock	set_disable_clock_gating_check
ataDumpIgnorePin	report_clock_tree -exceptions
ataDumpPropagatedMaxCap	report_constraint -max_capacitance -verbose
ataDumpPropagatedMaxTrans	report_constraint -max_transition -verbose
ataDumpSDC	write_sdc
ataDumpSDF	write_sdf
ataDumpSyncPin	report_clock_tree -exceptions
ataEnableGatingClock	set_clock_gating_check
ataEnablePresetClearArcs	report_timing -enable_preset_clear_arcs
ataIgnoreInterconnect	set_zero_interconnect_delay_ mode
ataIgnoreWireDelay	set_zero_interconnect_delay_ mode
ataIgnoreXtalk	set_si_options
ataIncludeXtalk	set_si_options
ataLoadSDC	read_sdc
ataPurgeIgnorePin	remove_clock_tree_exceptions -exclude_pins
ataPurgeSyncPin	remove_clock_tree_exceptions -float_pins
ataRemoveMaxCapBoundPort	remove_attribute
ataRemoveMaxCapClock	remove_attribute
ataRemoveMaxCapClockData	remove_attribute
ataRemoveMaxTransBoundPort	remove_attribute
ataRemoveMaxTransClock	remove_attribute
ataRemoveMaxTransClockData	remove_attribute

ataRemoveTC	remove_sdc
ataSetAndPropagateMaxCapBoundPort	set_max_capacitance
ataSetAndPropagateMaxCapClock	set_max_capacitance
ataSetAndPropagateMaxCapClockData	set_max_capacitance
ataSetAndPropagateMaxTransBoundPort	set_max_transition
ataSetAndPropagateMaxTransClock	set_max_transition
ataSetAndPropagateMaxTransClockData	set_max_transition
ataSetWireDelayModel	set_delay_calculation
ataWriteTC	write_sdc
auCreateWireTracks	create_track
auExtractBlockagePinVia	extract_blockage_pin_via
auHierECOByChangeFile	read_mw_eco_list
auVerilogToCell	import_designs
axAddEndCap	add_end_cap
axAddWireTracks	create_track
axAdjustFloorPlan	adjust_fp_floorplan
axClearWireTracks	remove_track
axComputeHierAntennaProp	extract_hier_antenna_property
axCreateBaseArrayRecord	create_base_array
axCreateRouteGuide	create_route_guide
axCreateTrackRecord	create_track
axDeleteAllRouteGuide	remove_route_guide
axDeleteFillerWithViolation	remove_filler_with_violation
axDrouteOptimizeContact	insert_redundant_vias
axPrintParams	report_parameter -module
axPurgePlaceBlockage	remove_placement_blockage
axPurgeSingleRecordType	remove_track remove_base_arrays

axPurgeSoftPlaceBlockage	remove_placement_blockage
axRemoveIOPinOverlap	remove_io_pin_overlap
axReportAntennaRatio	report_antenna_ratio
axSearchParams	report_parameter -name
axSetIntParam	set_parameter
axSetRealParam	set_parameter
axShowParams	report_parameter -module
axgAddBlockage	create_placement_blockage
axgAddFillerCell	insert_stdcell_filler
axgAddFillerCellByArea	insert_stdcell_filler -bounding_box
axgAddPadFiller	insert_pad_filler
axgAddPadFillerByArea	insert_pad_filler
axgAddRouteGuide	create_route_guide
axgAddRow	add_row
axgAddSoftBlockage	create_placement_blockage
axgAddWellFillRowGap	insert_well_filler -gap_type
axgAddWellFiller	insert_well_filler
axgAdvRouteOpt	route_opt route_rc_reduction
axgAreaRoute	route_area
axgArrayTapCell	add_tap_cell_array
axgAssignToTracks	route_track
axgAutoRoute	route_auto
axgAutoShieldRoute	create_auto_shield
axgCheckDesignForRoute	check_routeability
axgCheckWireTrack	check_routeability
axgCreatePadRings	create_pad_rings
axgCreatePrerouteContacts	create_preroute_vias
axgCreateRectangularRings	create_rectangular_rings
axgCreateStraps	create_power_straps
axgCutRowByArea	cut_row
axgDefineDifferential	create_differential_group
axgDefineVarRule	define_routing_rule
axgDefineWireTracks	set_preferred_routing_direction

axgDeleteDiode	remove_diode
axgDetailRoute	route_detail
axgDumpFloorPlan	report_voltage_area write_floorplan
axgDumpRouting	write_route
axgECOAutoPlaceFS	place_freeze_silicon
axgECORoute	route_eco
axgECORouteDesign	route_eco
axgECOTrimFill	trim_fill_eco
axgFillWireTrack	insert_metal_filler
axgGlobalRoute	route_global
axgHierPlan	create_plan_groups
axgHierPlan	uniquify_fp_mw_cel flatten_fp_hierarchy merge_fp_hierarchy
axgInsertDiode	insert_diode
axgListPRSummary	report_design -physical report_cell report_area report_fp_placement
axgLoadTDF	read_io_constraints
axgLoadTDFforChildCell	read_io_constraints
axgMarkRouteType	set_route_type
axgPlaceCheck	check_legality report_voltage_area
axgPlanner	initialize_floorplan
axgPreRouteInstances	preroute_instances
axgPrerouteStandardCells	preroute_standard_cells
axgProtoRoute	route_fp_proto
axgPurgeFillerCell	remove_stdcell_filler
axgPurgeFillerCellByArea	remove_stdcell_filler remove_stdcell_filler -boundingbox
axgPurgeWellFiller	remove_well_filler
axgRectiPlanner	initialize_rectilinear_block
axgRoutOpt	route_opt optimize_wire_via
axgRouteDifferential	route_differential

axgRouteGroup	route_group
axgRouterVerify	verify_route
axgScanChainOptim	place_opt -reorder_scan place_opt -optimize_dft
axgScanTrace	trace_scan_chain
axgSearchRepair	route_search_repair
axgSetCellInstVoltage	create_voltage_area
axgSetMinMaxLayer	set_net_routing_layer_ constraints set_ignored_layers
axgSetNetConstraint	set_net_routing_rule
axgSetRouteOptions	report_route_options set_route_options
axgSetVoltageOperatingCond	create_voltage_area
axgSlotWire	slot_wire
axgSpreadGroupCells	spread_spare_cells
axgVAConsistencyCheck	check_mv_design -verbose check_mv_design -level_shifters check_legality
axgVeriPGConn	verify_pg_nets
axgVerifyNetGroup	verify_route -nets
cmCopyLib	copy_mw_lib
cmCreateLib	create_mw_lib
cmDumpTLUPlus	report_tlu_plus_files
cmDumpTech	write_mw_lib_files
cmMarkCellType	set_attribute
cmRefLib	set_mw_lib_reference
cmRenameCel	rename_mw_cel
cmRenameLib	rename_mw_lib
cmReplaceRefLib	set_mw_lib_reference
cmReplaceTech	set_mw_technology_file
create_boundary	create_boundary
dbAddAntennaLayerRule	define_antenna_layer_rule
dbAssignVarRouteRule	set_net_routing_rule
dbClearAllNetXtalkProp	remove_xtalk_prop
dbClearLibAntennaRules	remove_antenna_rules
dbConnect	connect_net

dbCreateBaseArrayRow	create_base_array
dbCreateCellBoundary	create_boundary
dbCreateCellRow	create_site_row
dbCreateNet	create_net
dbCreatePort	create_port
dbCreateText	create_text
dbCreateVoltageArea	update_voltage_area
dbDefineAntennaAccumMode	define_antenna_accumulation_mode
dbDefineAntennaLayerRatioScale	define_antenna_layer_ratio_scale
dbDefineAntennaRule	define_antenna_rule
dbDefineVarRouteRule	define_routing_rule
dbDeleteAllVarRouteRules	remove_routing_rules -all
dbDeleteObject	remove_base_arrays remove_net remove_net_shape remove_placement_blockage remove_port remove_route_guide remove_text remove_user_shape remove_via remove_voltage_area
dbDeletePin	remove_terminal
dbDisconnect	disconnect_net
dbDumpAllVarRouteRules	report_routing_rules
dbDumpLibAntennaRules	report_antenna_rules
dbDumpScanChain	get_scan_chains
dbFetchContactNames	get_vias
dbFetchLayerIdList	get_layers
dbFetchLayerInfo	get_layer_attribute
dbFetchObject	report_attribute list_attributes get_via_masters get_text
dbFetchObjectField	get_attribute
dbGetCellInstByName	get_cells

dbGetConnectedObject	all_connected
dbGetCurrentLibId	current_mw_lib
dbGetNetByName	get_nets
dbGetPinByName	get_terminals
dbGetPlanGroupByName	get_plan_groups
dbGetPlangroupByName	get_plan_groups
dbGetPortByName	get_ports
dbHierSplit	split_mw_lib
dbPurgeAllPlanGroup	remove_plan_groups
dbPurgeAllPlangroup	remove_plan_groups
dbPurgeCellInstMaster,remove_cell	
dbPurgeRefLib	set_mw_lib_reference
dbRebuildLib	rebuild_mw_lib
dbReplaceTechFile	set_mw_technology_file
dbResetAllNetTimingSpacing	remove_net_timing_spacing
dbSaveCell,save_mw_cel	
dbSetCellPortTypes	set_attribute
dbSetNetType	set_route_type
dbSetNetXtalkAggressorList	set_net_aggressors
dbSetRefLibControl	set_mw_lib_reference
db_foreach	foreach_in_collection get_lib_cells get_lib_pins get_libs get_pins get_user_shapes
fcArrayLegalDriverLoc	set_flip_chip_driver_array
fcArrayPlace	place_flip_chip_array
fcCreateBumpTimingInfo	update_flip_chip_pin_locations
fcCreateUniformGrid	set_flip_chip_grid
fcDriverBumpMatch	assign_flip_chip_nets
fcDumpDriverBumpMatch	report_flip_chip_driver_bump report_flip_chip_type set_flip_chip_cell_site
fcFcType	set_flip_chip_type
fcIslandLegalDriverLoc	set_flip_chip_driver_island

fcRingLegalDriverLoc	set_flip_chip_driver_ring
fcRingPlace	place_flip_chip_ring read_flip_chip_bumps
fphAddAnchors & fphTcp	compile_fp_clock_plan
fphAddSMBusPin	create_fp_pins
fphAddSMPin	create_fp_pins
fphAddVirtualPad	create_fp_virtual_pad remove_fp_virtual_pad
fphAdjustIOPlacement	adjust_fp_io_placement
fphAdsSMPinBlockage	create_placement_blockage -type pin
fphAlignHMPin	align_fp_pins
fphAlignSMPin	align_fp_pins
fphAnalyzeRail	analyze_fp_rail
fphAnalyzeRouting	analyze_fp_routing
fphBlockPlacement	shape_fp_blocks
fphCheckSMPin	check_fp_pin_assignment
fphCheckSMPinAlignment	check_fp_pin_alignment
fphCheckTimingEnvironment	check_fp_timing_environment
fphClockOptions	set_fp_clock_plan_options
fphCommitHierarchy	commit_fp_plan_groups
fphCommitRail	commit_fp_rail
fphCopyCellRow2SM	push_down_fp_objects -object_type rows
fphCreateCustomSMPins	create_fp_pins
fphCreateHierSignalShielding	create_fp_block_shielding
fphCreateMovebounds	create_bounds
fphCreatePinGuide	create_pin_guide
fphCutPreRoute	push_down_fp_objects
fphDeleteAllSMPins	remove_objects [get_selection]
fphDeleteHierSignalShielding	remove_fp_block_shielding
fphDeleteMacroPadding	remove_keepout_margin
fphDeletePlangroupPadding	remove_fp_plan_group_padding

fphDeleteSMPin, fphDeleteAllSMPins, fphDeleteAllMovableSMPins	remove_objects [get_selection]
fphDeleteSMPinBlockage	remove_objects [get_selection]
fphDisplayVoltageDropMap	load_fp_rail_map
fphDumpHierFP	get_placement_blockages
fphDumpMacroPadding	report_keepout_margin
fphEditToolbar	align_objects distribute_objects flip_objects move_objects rotate_objects set_object_fixed_edit
fphEstBlackBox	estimate_fp_black_boxes
fphEstimateWirelength	get_fp_wirelength
fphFixOrUnfixSMPins	set_object_fixed_edit [get_selection] 1
fphFlattenBlackBoxes	flatten_fp_black_boxes
fphImportBlackBoxes	import_fp_black_boxes
fphLegalizePlacement	legalize_fp_placement
fphOptimize	optimize_fp_timing
fphPackMacroInArea	pack_fp_macro_in_area
fphPadMacros	set_keepout_margin
fphPadPlangroups	create_fp_plan_group_padding
fphPinDetourReport	check_fp_pin_alignment -detour
fphPlaceDesign	create_fp_placement
fphPlacementReport	report_fp_placement
fphPrintParams	report_fp_placement_strategy set_fp_placement_strategy
fphRemoveFeedthroughs	remove_fp_feedthroughs
fphRemoveSMPinOverlap	remove_fp_pin_overlaps
fphSetBlackBoxesEstimated	set_fp_black_boxes_estimated
fphSetBlackBoxesUnestimated	set_fp_black_boxes_unestimated
fphSetGateEquivalence	set_fp_base_gate
fphSetPAConstraints	set_fp_pin_constraints
fphSetPNSBlockRings	set_fp_block_ring_constraints

fphSetPNSConstraints	set_fp_rail_constraints report_fp_rail_constraints
fphSetPPSConstraints	set_fp_power_pad_constraints
fphSetPlaceConstraints	set_fp_macro_options
fphSetSynthesizeRailRegion	set_fp_rail_region_constraints
fphShapeDesign	shape_fp_blocks
fphSnapSMPin	move_pins_on_edge
fphSnapSMPinToSMEdge	move_pins_on_edge
fphSoftMacroToBlackBox	change_fp_soft_macro_to_black_box
fphSoftMacroToPlanGroup	uncommit_fp_soft_macros
fphSynthesizeail	synthesize_fp_rail
fphTimingBudgeting	allocate_fp_budgets
geAddCell	create_cell
geAddContact	create_via
geAddContactArray	create_via
geAddPath	create_net_shape
geAddRectPin	create_terminal
geAddRectangle	create_user_shape
geAddWire	create_net_shape
geAdvDRC	verify_drc
geCloseCell	close_mw_cel
geCloseLib	close_mw_lib
geCopy	copy_objects
geCopyCell,copy_mw_cel	
geCreateCell	create_mw_cel
geDelete	remove_objects remove_text
geDeleteCell,remove_mw_cel	
geGetEditCell	current_mw_cel
geLineSelect	win_select_objects
geModify	set_attribute
geMove	move_objects
geMove, geMoveCell	move_objects
geNewFillNG	insert_ng_filler

geNewLVS	verify_lvs
geNewMakeMacro	create_macro_fram
geOpenCell	open_mw_cel
geOpenLib	open_mw_lib
geQueryObject	query_objects
geShowCellList	list_mw_cels get_mw_cels
geSplit	split_objects
geStretch	resize_objects
geTransform	rotate_objects flip_objects
geWindowSelect	change_selection get_net_shapes get_placement_blockages get_route_guides get_voltage_areas win_select_objects get_selection
hdpCreateModels	create_ilm
ioDumpIOLocation	write_io_constraints
ioLoadTdf	read_tdf_ports
ioReplacePads	place_io_pads
jpCheckJobStatus	report_distributed_route
jpClose	close_distributed_route
jpKillJob	remove_distributed_route
jpParallelJob	set_distributed_route
jpQueryAvailableCPUs	report_distributed_route
load	read_floorplan
pdsHFNCollapse	remove_buffer_tree
pdsHFNCollapseNet	remove_buffer_tree
pdsHFNOptimization	create_buffer_tree
read_def	read_def
trCreateStackViaOnPadPin	create_stack_via_on_pad_pin
write_def	write_def
fphAssignPins	place_fp_pins
fphCreateBlkgFromSMHardmacro	create_fp_blockages_for_child_hardmacro
fphCreateSMPins	create_fp_pins

fphGetSMPinAssignOptions	report_fp_pin_constraints
fphRecoverPreroute, fphPushUp, fphDeleteSMCellRow	push_up_fp_objects
fphSortSMPins	sort_fp_pins

IC Compiler Variables

IC Compiler defines a set of variables that are used to control its behavior.

For a list of all variables and their current values, enter the following command from within icc_shell:

```
icc_shell> printvar
```

The syntax for setting a variable is

```
icc_shell> set variable_name value
```

access_internal_pins

Controls the creation, deletion, and user access of internal pins.

Default value for this variable is true.

alib_library_analysis_path

Specifies a single path, similar to a search path, for reading and writing the alib files that correspond to the target libraries.

Default value for this variable is "./".

auto_insert_level_shifters

Setting this variable to false would prevent automatic level shifter insertion in commands like compile, insert_dft etc

Default value for this variable is true.

auto_insert_level_shifters_on_clocks

This variable is used to direct automatic level shifter insertion to insert level shifter on specified clocks

Default value for this variable is "".

auto_link_disable

Specifies whether the code to perform an auto_link during any Design Compiler command should be disabled.

Default value for this variable is false.

auto_link_options

Specifies the link command options to be used when link is invoked automatically by various Design Compiler and DFT Compiler commands (for example, create_schematic and compile).

Default value for this variable is -all.

auto_ungroup_preserve_constraints

Preserves (when *true*) the timing constraints on the hierarchy when the hierarchy is ungrouped during the process of optimization.

Default value for this variable is true.

auto_wire_load_selection

Controls automatic selection of wire load model.

Default value for this variable is area_locked.

bind_unused_hierarchical_pins

Specifies if unused input and output hierarchical pins should be connected to constant tie-off cells during compile.

Default value for this variable is true.

blockPlace_addChannelBlockages

Enables adding placement blockages in congested channels during *shape_fp_blocks -incremental congestion_driven* .

Default value for this variable is 2.

blockPlace_adjustMacroLocations

Adjusts macro locations during *shape_fp_blocks -incremental congestion_driven* .

Default value for this variable is 0.

blockPlace_avoidPowerGrid

Controls whether the power grid is on during channel resizing.

Default value for this variable is 0.

blockPlace_distanceToPowerGrid

Specifies the minimum allowed distance between a plan group boundary and the power grid.

Default value for this variable is -1.

blockPlace_keepTopLevelTogether

Controls whether the top level is kept together (contiguous) during shaping.

Default value for this variable is 0.

blockPlace_minChannelSize

Specifies the minimum channel size between two plan groups.

Default value for this variable is 0.

blockPlace_preserveAbutment

Enables preserving abutment during *shape_fp_blocks -incremental target_utilization_driven* .

Default value for this variable is 0.

blockPlace_utilSlack

Controls how much channel resizing can exceed the target utilization.

Default value for this variable is 0.1.

budget_generate_critical_range

Enables automatic generation of set_critical_range commands by dc_allocate_budgets for multiply-instantiated subdesigns.

Default value for this variable is false.

budget_map_clock_gating_cells

Maps integrated clock gating cells into target library during RTL budgeting.

Default value for this variable is false.

bus_inference_descending_sort

Specifies that the members of that port bus are to be sorted in descending order rather than in ascending order.

Default value for this variable is true.

bus_inference_style

Specifies the pattern used to infer individual bits into a port bus.

Default value for this variable is "".

bus_minus_style

Controls the naming of individual members of bit-blasted port, instance, or net buses with negative indices.

Default value for this variable is -%d.

bus_multiple_separator_style

Determines the name of a multibit cell that implements bits that do not form a range.

Default value for this variable is ,.

bus_naming_style

Specifies the style to use in naming an individual port member, net member, or cell instance member of an EDIF array or of a Verilog or VHDL vector.

Default value for this variable is %s[%d].

bus_range_separator_style

Specifies the style to use in naming a net connected to the "wire" end of a ripper in the EDIF file.

Default value for this variable is :.

cache_dir_chmod_octal

Specifies the value of the mode bits for created cache directories.

Default value for this variable is 777.

cache_file_chmod_octal

Specifies the value of the mode bits for created cache files.

Default value for this variable is 666.

case_analysis_log_file

Specifies the name of a log file generated during propagation of constant values, from case analysis or from nets tied to logic zero or logic one. Each scenario has its proprietary log file if multiple scenarios exist.

Default value for this variable is "".

case_analysis_propagate_through_icg

Determines whether case analysis is propagated through integrated clock gating cells.

Default value for this variable is false.

case_analysis_with_logic_constants

When true, enables constant propagation, even if a design contains only logic constants.

Default value for this variable is false.

change_names_bit_blast_negative_index

Bit blast the bus if any bit of it is negative.

Default value for this variable is false.

change_names_dont_change_bus_members

Controls how the change_names command modifies the names of bus members.

Default value for this variable is false.

check_design_allow_non_tri_drivers_on_tri_bus

Specifies the severity level to be applied during compile or check_design command execution, when three-state buses with non three-state driver(s) are found in the design.

Default value for this variable is true.

check_design_allow_unknown_wired_logic_type

Specifies the severity level to be applied during compile or check_design command execution, when nets with multiple drivers(unknown wired-logic type) are found in the design.

Default value for this variable is true.

check_error_list

Specifies the error codes that the check_error command checks for.

Default value for this variable is CMD-004 CMD-006 CMD-007 CMD-008 CMD-009 CMD-010 CMD-011 CMD-012 CMD-014 CMD-015 CMD-016 CMD-019 CMD-026 CMD-031 CMD-037 DB-1 DCSH-11 DES-001 ACS-193 FILE-1 FILE-2 FILE-3 FILE-4 LINK-7 LINT-7 LINT-20 LNK-023 OPT-100 OPT-101 OPT-102 OPT-114 OPT-124 OPT-127 OPT-128 OPT-155 OPT-157 OPT-181 OPT-462 UI-11 UI-14 UI-15 UI-16 UI-17 UI-19 UI-20 UI-21 UI-22 UI-23 UI-40 UI-41 UID-4 UID-6 UID-7 UID-8 UID-9 UID-13 UID-14 UID-15 UID-19 UID-20 UID-25 UID-27 UID-28 UID-29 UID-30 UID-32 UID-58 UID-87 UID-103 UID-109 UID-270 UID-272 UID-403 UID-440 UID-444 UIO-2 UIO-3 UIO-4 UIO-25 UIO-65 UIO-66 UIO-75 UIO-94 UIO-95 EQN-6 EQN-11 EQN-15 EQN-16 EQN-18 EQN-20.

collection_result_display_limit

Sets the maximum number of objects that can be displayed by any command that displays a collection.

Default value for this variable is 100.

command_log_file

Specifies the name of the file to which a log of the initial values of variables and commands executed is written. If the value is an empty string, a command log file is not created.

Default value for this variable is "./command.log".

company

Specifies the name of the company where Synopsys software is installed. The company name is displayed on the schematics.

Default value for this variable is "".

compatibility_version

Sets the default behavior of the system to be the same as the Synopsys software version specified in the variable.

Default value for this variable is C-2009.06-ICC.

compile_clock_gating_through_hierarchy

Controls whether the compile or compile_ultra command with the -gate_clock option will perform clock gating through hierarchy boundaries.

Default value for this variable is false.

compile_dont_use_dedicated_scanout

Controls whether optimizations use a scan cell's dedicated scan-out pin for functional connections.

Default value for this variable is 1.

compile_instance_name_prefix

Specifies the prefix used in generating cell instance names when compile is executed.

Default value for this variable is U.

compile_instance_name_suffix

Specifies the suffix used for generating cell instance names when compile is executed.

Default value for this variable is "".

compile_keep_original_for_external_references

Controls compile command to keep the original design when there is an external reference to the design.

Default value for this variable is false.

compile_log_format

Controls the format of the columns to be displayed during the mapping phases of compile and reoptimize_design.

Default value for this variable is %elap_time %area %wns %tns %drc %endpoint.

compile_power_domain_boundary_optimization

Sets the variable to false to disable boundary optimization across power domain boundaries.

Default value for this variable is true.

compile_retime_exception_registers

Controls whether registers with common path exceptions, including max_path, min_path, multicycle_path, false_path, and group_path, can be moved by adaptive retiming.

Default value for this variable is false.

compile_seqmap_identify_shift_registers

Controls the identification of shift registers in compile -scan. This feature is only supported in test-ready compile with Design Compiler Ultra with a multiplexed scan-style.

Default value for this variable is true.

compile_ultra_ungroup_small_hierarchies

Determines whether to automatically ungroup small hierarchies in the compile_ultra flow.

Default value for this variable is true.

compile_use_fast_delay_mode

Selects the algorithm used for delay calculations when using the CMOS2 or nonlinear delay models.

Default value for this variable is true.

complete_mixed_mode_extraction

Enables extraction of both routed and unrouted nets with a single command. This is known as mixed-mode extraction.

Default value for this variable is true.

context_check_status

Reports whether the context_check mode is enabled (read-only).

Default value for this variable is false.

cp_full_abut_cts_region_aware

Set clock planning and clock tree synthesis to be region (plan group) aware. It is necessary to be true to handle design with full-abut floorplan.

Default value for this variable is false.

cp_in_full_abut_mode

Set clock planning to handle design with full-abut floorplan

Default value for this variable is false.

create_clock_no_input_delay

Affects delay propagation characteristics of clock sources created by using the create_clock command.

Note: This variable will become obsolete. Please adjust your scripts accordingly.

Default value for this variable is false.

cts_blockage_aware

Setting this variable to false will turn off the blockage aware clock tree synthesis algorithm in compile_clock_tree.

Default value for this variable is true.

cts_clock_opt_batch_mode

Runs the compile_clock_tree, optimize_clock_tree, and balance_inter_clock_delay commands in clock tree synthesis (CTS) batch mode when this variable is set to true.

Default value for this variable is false.

cts_clock_source_is_exclude_pin

This variable controls the cascaded create-clock behavior. If this variable is set to true, clock tree synthesis (CTS) marks the clock source of a downstream create_clock command as an implicit exclude pin.

Default value for this variable is true.

cts_do_characterization

Specifies for clock tree synthesis to print additional information to the log file when both the cts_do_characterization and cts_use_debug_mode variable are set to true. It prints detailed characterization data for the buffers and inverters that clock tree synthesis uses.

Default value for this variable is false.

cts_enable_clock_at_hierarchical_pin

Specifies that clock tree construction be performed bottom-up for clocks at hierarchical pins. It is for designs with clock sources or clock exceptions defined at hierarchical pins.

Default value for this variable is true.

cts_enable_rc_constraints

When this variable is set to true, CTS will apply internally derived RC constraints during clustering to reduce skew caused by wire delay. This feature is to be used with config file only.

Default value for this variable is false.

cts_fix_clock_tree_sinks

Specifies for clock tree synthesis (CTS) to put the cts_fixed attribute on all sinks for optimization and legalization to honor, when set to true.

Default value for this variable is false.

cts_fix_drc_beyond_exceptions

Specifies for clock tree synthesis (CTS) to fix all design rule checking (DRC) violations before skew minimization, when set to true. From the A2007.12 release forward, this tool fixes all DRC violations, including those beyond clock exceptions by default. This variable provides you with a switch to prevent DRC fixing beyond clock exceptions.

Default value for this variable is true.

cts_force_user_constraints

Specifies for clock tree synthesis (CTS) to ignore library constraints for capacitance and transition, when set to true. This variable is useful for comparing CTS results between IC Compiler and other tools.

Default value for this variable is false.

cts_instance_name_prefix

Specifies string to prepend to names of cells created during compile_clock_tree and optimize_clock_tree.

Default value for this variable is "".

cts_move_clock_gate

This variable controls the initial relocation of existent clock gates in compile_clock_tree.

Default value for this variable is true.

cts_net_name_prefix

Specifies string to prepend to names of nets created during compile_clock_tree and optimize_clock_tree.

Default value for this variable is "".

cts_prects_upsize_gates

Specifies for the compile_clock_tree command to up-size the original clock gates to the LEQ cell with the highest driving strength, when set to true.

Default value for this variable is true.

cts_push_down_buffer

Enables the split_clock_net command to push down clock sinks by creating new cell instances to drive them, when set to true.

Default value for this variable is false.

cts_rc_relax_factor

This variable controls the internally derived RC constraints for clustering.

Default value for this variable is 1.

cts_region_aware

Setting this variable to true will turn on the region aware clock tree synthesis algorithm in compile_clock_tree.

Default value for this variable is false.

cts_target_cap

Sets target capacitance value for clock tree synthesis (CTS) clustering instead of using the tool-calculated target based on maximum capacitance.

Default value for this variable is 0.

cts_target_transition

Sets target transition value for clock tree synthesis (CTS) clustering instead of using the tool-calculated target based on maximum transition.

Default value for this variable is 0.

cts_traverse_dont_touch_subtrees

Specifies for compile_clock_tree command to set clock net type and routing properties for nets beyond dont_touch_subtree exceptions, when set to true.

Default value for this variable is true.

cts_use_debug_mode

Specifies for clock tree synthesis (CTS) to print additional debugging information in the log file, when set to true.

Default value for this variable is false.

cts_use_lib_max_fanout

When set to true, clock tree synthesis will honor max fanout constraint set on library cell pins.

Default value for this variable is false.

cts_use_sdc_max_fanout

When set to true, clock tree synthesis will honor SDC max fanout constraint set on current design.

Default value for this variable is false.

current_design

Specifies the design being worked on. This variable is used by most of the Synopsys commands.

Default value for this variable is "".

db_load_ccs_data

The variable is obsolete and is not needed any more. The tool takes care of loading the CCS timing information automatically.

Default value for this variable is false.

dct_placement_ignore_scan

Sets the flag for the placer to ignore scan connections in Design Compiler topograpical.

Default value for this variable is false.

ddc_allow_unknown_packed_commands

Causes the read_file command to attempt to read DDC files which contain packed commands which are unknown to the current version of dc_shell.

Default value for this variable is true.

default_input_delay

Specifies the global default input delay value to be used for environment propagation.

Default value for this variable is 30.

default_name_rules

Contains the name of a name rule to be used as a default by the change_names command, if the command's -rules option does not specify a *name_rules* value.

Default value for this variable is "".

default_output_delay

Specifies the global default output delay value to be used for environment propagation.

Default value for this variable is 30.

default_port_connection_class

Contains the value of the connection class to be assigned to ports that do not have a connection class assigned to them.

Default value for this variable is universal.

default_schematic_options

Specifies options to use when schematics are generated.

Default value for this variable is -size infinite.

disable_auto_time_borrow

Determines whether the report_timing command and other commands will use automatic time borrowing.

Default value for this variable is false.

disable_case_analysis

When true, disables constant propagation from both logic constants and set_case_analysis command constants.

Default value for this variable is false.

disable_library_transition_degradation

Controls whether the transition degradation table is used to determine the net transition time.

Default value for this variable is false.

do_operand_isolation

Enables or disables operand isolation as a dynamic power optimization technique for a design.

Default value for this variable is false.

dont_touch_nets_with_size_only_cells

Specifies whether a net is marked dont touch if it is driven by at least one cell marked size_only and drives at least one cell marked by size_only.

Default value for this variable is false.

droute_advancedRouteLoops

The droute_advancedRouteLoops variable specifies the number of loops for the IC Compiler command route_advanced.If the value is set to N, it means that the route_advanced command stops after N loops.

droute_areaSrLoop

The droute_areaSrLoop variable specifies the number of search and repair loops during area optimization and routing in the route_area command.The search and repair loop terminates if DRC count reaches 0 even if the specified number of iterations are not reached.If the DRC number is still converging (reducing) after reaching the specified number of iterations, specifying more iterations could help reducing DRC count further, at the cost of more runtime.

droute_autoSaveInterval

The droute_autoSaveInterval variable specifies how frequent checkpoints (intermediate results) are saved during detail routing. If the value is set to 0, no checkpoint is saved during detail routing. Otherwise, the variable sets the time interval in minutes for each checkpoint to be saved.

droute_autoSrLoop

The droute_autoSrLoop variable sets the number of search and repair loops to be carried out after initial routing.The search and repair loop terminates if a DRC violation count reaches 0 even if the specified number of iterations is not reached. If the DRC violation number is still converging (reducing) after reaching the specified number of iterations, specifying more iterations could further help in reducing the DRC violation count at the cost of more runtime.

droute_connBrokenNet

The droute_connBrokenNet variable specifies whether broken nets are to be left broken or are to be reconnected. A broken net is a net that is not totally connected by glinks, preroutes, wires, or vias. If the value is set to 0, broken nets are ignored during detail routing. If the value is set to 1, broken nets are to be reconnected by detail routing.This variable does not affect tie-off connections, which are controlled by the connTieOff variable.

droute_connTieRail

The droute_connTieRail variable specifies where to connect tie-off pins. If the value is set to 0, the router connects tie-off pins anywhere on power and ground nets. If the value is set to 1, the router connects tie-off pins to power and ground rails and power and ground pins only.

droute_doMaxCapConx

The droute_doMaxCapConx variable specifies whether maximum capacitance constraints should be met or ignored during in-route optimization. If the value is set to 0, the maximum capacitance constraints are ignored during in-route optimization. If the value is set to 1, in-route optimization tries to meet maximum capacitance constraints.

droute_doMaxTransConx

The droute_doMaxTransConx variable specifies whether maximum transition constraints should be met or ignored during in-route optimization. If the value is set to 0, the maximum transition constraints are ignored during in-route optimization. If the value is set to 1, in-route optimization tries to meet maximum transition constraints.

droute_doProbeConx

The droute_doProbeConx variable specifies whether nets with top-layer probe constraints are to be routed to top layer for probing.

droute_doSelectedNetAntennaConx

The droute_doSelectedNetAntennaConx variable controls whether all antenna violations should be fixed or whether only antenna violations for specified nets should be fixed.

droute_doXtalkConx

The droute_doXtalkConx variable specifies whether crosstalk constraints (such as static noise voltage constraints and capacitance constraints) are to be honored during in-route optimization.

droute_ecoListToFile

The droute_ecoListToFile variable specifies whether to save the routing ECO list to the ecoRoute.list file.

droute_ecoMode

The droute_ecoMode variable specifies what nets are to be routed in ECO mode, and how they are rerouted. If the value is set to 0, only modified nets can be rerouted. If the value is set to 1, modified nets are rerouted first, and other nets can be rerouted later. If the value is set to 2, any nets can be rerouted in any order. Mode 0 produces minimum routing change, but offers you the least freedom to resolve DRC violations. Mode 2 offers the most freedom to resolve DRC violations, but can introduce significant changes in the routing solution.

droute_ecoScope

The droute_ecoScope variable specifies whether to use global or local scope during ECO routing. If the value set to 0, the router uses global scope mode. If the value is set to 1, the router uses local scope. Set this value to 0 if design has many violations. Set it to 1 to get better runtime if the design has very few violations.

droute_ecoSrLoop

The droute_ecoSrLoop variable sets the number of search and repair loops to be carried out after ECO routing.The search and repair loop terminates if DRC violation count reaches 0 even if the specified number of iterations are not reached. If the DRC violation number is still converging (reducing) after reaching specified number of iterations, specifying more iterations could help further reduce DRC violation count at the cost of more runtime.

droute_enable_one_pass_partitioning

Specifies which partitioning algorithm to use for distributed routing.

droute_expandFillTracks

The droute_expandFillTracks variable specifies whether the track region for metal fill should be expanded or not.

droute_fillDataType

The droute_fillDataType variable specifies a data type of filled metals. The value N is the data type of filled metals.

droute_fillEndByMinSpcPercent

The droute_fillEndByMinSpcPercent variable specifies the spacing requirement between the routing wires and the ends of fill metal. If the value is set to -1, the normal required spacing is used between the routing wires and the ends of fill metal. Otherwise, the value sets the percentage of normal required spacing to be used between the routing wires and the ends of fill metal. Normally, this value is to be left at its default value of -1. It should only be changed if the user understands the impact of it on the yield, and the final verification should be set accordingly.

droute_fillMetalCloseToMinDensityValue

The droute_fillMetalCloseToMinDensityValue variable specifies the target metal density for metal fill insertion. If the value is set to 0, the router tries to maximize dummy metals as long as maximum density is not violated. If the value is set to 1, the router tries to minimize dummy metals as long as minimum density is met.

droute_fillMetalUniformly

The droute_fillMetalUniformly variable specifies whether to fill dummy metal uniformly. If the value is set to 0, the router fills dummy metal in contiguous tracks. If the value is set to 1, the router tries to fills dummy metal uniformly in each window to meet the density rule.

droute_fillViaDataType

The droute_fillViaDataType variable specifies a data type of filled vias. If the value set to N, N is the data type of filled via.

droute_fixMinEdgeLengthByFilling

The droute_fixMinEdgeLengthByFilling variable specifies whether to allow filling metals to fix minEdgeLength violations during search and repair.

droute_followPolyTrkForPolyFill

The droute_followPolyTrkForPolyFill variable specifies to whether tracks on poly layer are used for poly fills. If the value is set to 0, the router follows M2 tracks to fill poly layer. If the value is set to 1, the router follows poly tracks to fill poly layer.

droute_groupSrLoop

The droute_groupSrLoop variable specifies the number of search and repair loops in the route_group command.The search and repair loop terminates if DRC violation count reaches 0 even if the specified number of iterations are not reached. If the DRC violation number is still converging (reducing) after reaching specifies number of iterations, specifying more iterations could help reducing DRC violation count further at the cost of more runtime.

droute_lowSkewClkRoute

The droute_lowSkewClkRoute variable specifies how many changes are allowed on nets from clock tree synthesis during detail routing.If the value is set to 0, nets from clock tree synthesis are treated the same as other nets. If the value is set to 1, minimal changes are to be made to nets from clock tree synthesis, if necessary.

droute_maxOffGridTrack

The droute_maxOffGridTrack variable specifies how off-grid tracks are to be added for off-grid pins and off-grid feedthroughs. If the value is set to 0, off-grid tracks are added selectively in via regions, which are determined by the router. If the value is set to 1, as many off-grid tracks as possible are added for off-grid pins. If the value is set to 2, 3, or 4, more off-grid tracks are aggressively added in increasing order for off-grid feedthroughs and pins.By creating as many off-grid tracks as possible for off-grid pins, the router has the maximum flexibility in accessing these pins, at the cost of more routing time.It is recommended to leave droute_maxOffGridTrack variable at the default value of 0 to start with if the you do not know how bad the off-grid situation is, and gradually increase the value if the results suffer from

off-grid pin access or off-grid feedthrough usage. If you know beforehand that there will be off-grid difficulty from previous experience, droute_maxOffGridTrack can be set to higher value to start with.You can also set the value to -1. This lets the router start from 0 and then automatically and gradually increase to 1, 2, 3, 4 during search and repair. The side effect of setting droute_maxOffGridTrack to a higher value is increased runtime.

droute_maxTieOffDistance

The droute_maxTieOffDistance variable specifies the search distance to connect tieoffs. If the value is set to -1, there is no search distance limit to connect tieoffs. Otherwise, the variable specifies the search distance for the search engine to use in number of gcells to connect tieoffs.

droute_metalFillDensityIncrement

The droute_metalFillDensityIncrement variable specifies increment value for metal fill. If the value is set to N, the router targets metal density N percent higher than minimum density during dummy metal insertion. The value N specifies the increment from minDensity value for metal fill. It is used when fillMetalCloseToMinDensityValue is enabled. For example, if minDensity (in the technology file) is 20 percent and droute_metalFillDensityIncrement is set as 10 percent, target density of metal fill will be 30 percent.

droute_minLengthCheckCutMode

The droute_minLengthCheckCutMode variable specifies how to compute minimum length when a polygon completely encloses a via. If the value is set to 0, the router does not check whether a wire completely encloses via. If the value is set to 1, the router checks whether a wire completely encloses via. When a via connects more than one wire segment on the same metal layer, minimum length is checked against the longest wire that completely encloses the via. When a via connects only to single wire segment on one metal layer, the wire needs to be checked for minimum length rule.

droute_minShieldLength

The droute_minShieldLength variable specifies minimum length for a wire to be shielded in the unit of pitches. For example, if the variable is left at its default value of 4, only the wires longer than 4 pitches are shielded.

droute_numCPUs

The droute_numCPUs variable specifies the number of CPUs to be used for distributed routing.

droute_offGridCost

The droute_offGridCost variable specifies extra off-grid routing cost. The default on-grid unit wire cost is 1. Therefore, if the value is set to 0, off-grid routes have the same cost as on-grid cost, and wires are routed as in a gridless router. If the value is set to N, off grid unit wire cost becomes 1 + N.This variable can be used to encourage or discourage off-grid routing against on-grid routing.

droute_offsetFillTrack

The droute_offsetFillTrack variable specifies how to offset the metal fill track.

droute_optDelaySlackTarget

The droute_optDelaySlackTarget variable specifies slack target for delay optimization during in-route optimization.

droute_optDelaySrLoop

The droute_optDelaySrLoop variable specifies the number of search and repair loops after delay optimization in the route_opt command.The search and repair loop terminates if DRC violation count reaches 0 even if the specified number of iterations is not reached. If the DRC violation number is still converging (reducing) after reaching the specified number of iterations, specifying more iterations could help reduce DRC violation count further at the cost of more runtime.

droute_optSetup

The droute_optSetup variable specifies whether setup slack is to be maintained or improved during in-route optimization. If the value is set to 0, the router tries to maintain setup slack, and does not try to improve the slack. If the value is set to 1, the router tries to improve setup slack.

droute_optSrLoop

The droute_optSrLoop variable specifies the number of search and repair loops after route optimization in route_opt command.The search and repair loop terminates if DRC violation count reaches 0 even if the specified number of iterations is not reached. If the DRC violation number is still converging (reducing) after reaching specified number of iterations, specifying more iterations could help reduce DRC violation count further at the cost of more runtime.

droute_optViaHoldTimeThreshold

The droute_optViaHoldTimeThreshold variable specifies the hold time threshold for contact optimization. If the value is set to N, the router tries to preserve hold time by not inserting redundant vias for the nets whose hold time is worse than N.

droute_optViaSetupSlackThreshold

The droute_optViaSetupSlackThreshold variable specifies the setup slack threshold for contact optimization. If the value is set to N, the router tries to preserve setup time by not inserting redundant vias for the nets whose setup slack is worse than N.

droute_optViaSrLoop

The droute_optViaSrLoop variable specifies search and repair loops after contact optimization. If the value set to N, the router runs N loops of search and repair after contact optimization.

droute_optViaTimingDriven

The droute_optViaTimingDriven variable specifies whether to preserve timing for critical nets with timing violations. If the value is set to 0, the router does contact optimization for all nets. If the value is set to 1, the router tries to preserve timing for critical nets by not doing contact optimization on those nets.

droute_optimizeRouteGroup

The droute_optimizeRouteGroup variable specifies whether optimization is to be run in the route_group command.Skipping optimization at the end of the route net group could save some runtime.

droute_parallelLengthMode

The droute_parallelLengthMode variable specifies how to compute parallel length for the fat metal spacing rule. If the value is set to 0, the router merges fat neighboring shapes only and determines parallel length based on the merged fat wire. If the value is set to 1, the router merges all neighboring (fat and thin) shapes and the total length of the merged wire will be used to compute the parallel length.

droute_pinTaperLengthLimit

The droute_pinTaperLengthLimit variable specifies the limit for pin tapering length. If the value is set to -1, there is no limit for tapering length, and tapering should go all the way to the Steiner point. Otherwise, this variable specifies the tapering length limit in the units of routing pitches.

droute_pinTaperMode

The droute_pinTaperMode variable specifies pin tapering width. If the value is set to 0, the tapering width is the default width. If the value is set to 1, the tapering width is the pin width.

droute_reportLimit

The droute_reportLimit variable specifies the maximum number of DRC violations that the router reports.If the value is set to -1, no limit is set, and the router reports all DRC violations. Otherwise, the value specifies the maximum number of DRC violations to be reported.

droute_rerouteUserWire

The droute_rerouteUserWire variable specifies whether user-created wires and vias are to be treated as fixed or reroutable.

droute_rerunDRC

The droute_rerunDRC variable specifies whether DRC violations are regenerated before search and repair.

droute_resetMinMaxLayer

The droute_resetMinMaxLayer variable resets minimum-maximum rule constraints defined by set_ignored_layers, set_net_routing_layer_constraints, and set_net_routing_rule commands before search and repair.

droute_shieldLimitSboxExt

The droute_shieldLimitSboxExt variable specifies the processing of routing area Sboxes during shielding, and is used to speed shielding up by limiting routing area Sbox extension size to technology file minSpacing layer parameters in such routing areas. The default is to maximize Sbox extension size by technology file fat layer parameters, which in some cases produces more accurate results, but contributes to increased shielding run time.

droute_shieldRerouteSignalNets

The droute_shieldRerouteSignalNets variable specifies whether to reroute signal nets during shielding. If the value is set to 0, the router does not reroute signal nets to improve shielding coverage. If the value is set to 1, the router reroutes signal nets and possibly creates minimized DRC violations as a tradeoff of improved shielding coverage. You need to run search and repair after shielding if DRC violations are created on signal nets.

droute_shieldSkipNotShieldedSboxes

The droute_shieldSkipNotShieldedSboxes variable specifies the processing of routing area Sboxes that have no shielding, and is used to speed shielding up by skipping checking for DRC violations in such routing areas.

droute_shieldViaMinSpacing

The droute_shieldViaMinSpacing variable specifies the spacing requirement on shielded vias. If the value is set to 0, the specified spacing from the GUI form for shielding wires is used to shield vias. If the value is set to 1, minimum spacing is used to shield vias to minimize routing resource usage.

droute_smallJogMinLength

The droute_smallJogMinLength variable specifies the minimum length of a small jog. If the value is set to 0, the router does consider the small jog recommended rule. If the value is set to N, the router reports and fixes the small jog violation if the jog length is less than (N) times a quarter pitch.

droute_srLoop

The droute_srLoop variable sets the number of search and repair loops in the search and repair phase in the route_search_repair command.The search and repair loop terminates if DRC violation count reaches 0 even if the specified number of iterations is not reached. If the DRC violation number is still converging (reducing) after reaching specified number of iterations, specifying more iterations could help further reduce DRC violation count at the cost of more runtime.

droute_stopIfNoLicense

The droute_stopIfNoLicense variable flags whether to stop the router or continue if the tool cannot obtain the option license. If the value is set to 0, the router continues by ignoring certain constraints if the router fails to get the corresponding option license. If the value is set to 1, the router will exit if it fails to get the needed option license.

droute_timeLimit

The droute_timeLimit variable specifies the corresponding detail routing step runtime limit.If the value is set to -1, no runtime limit is set. Otherwise, the variable sets the runtime limits in minutes.This is a very useful variable if you have a time limit and do not care about the final number of DRC violations as much. For example, you might want to get the feeling of how "routable" a design is in a given amount of time.Not all detail routing steps support time limits, such as route_auto and route_global. You can check the GUI form to see which routing steps support time limits.

droute_timingDriven

The droute_timingDriven variable specifies whether timing-critical nets with setup violations are to be optimized during initial detail routing. If the value is set to 0, timing-critical nets with setup violations are not optimized. If the value is set to 1, timing-critical nets with setup violations are optimized.By setting the value to 1, initial detail routing tries to generate routes with less resistance and capacitance (shorter wires and fewer vias) for timing-critical nets.

droute_timingSpace

The droute_timingSpace variable specifies whether the detailed router should try to allocate extra same-layer spacing to timing-critical net wires.

droute_treatTiedFillAsFillToFillSpacing

The droute_treatTiedFillAsFillToFillSpacing variable specifies whether fill-to-fill spacing is applied to tied fills. If the value is set to 0, the router follows fill-to-route spacing for tied fills during metal fill. If the value is set to 1, the router follows fill-to-fill spacing for tied fills.

droute_trimUserAntenna

The droute_trimUserAntenna variable determines how user-created dangling wires are handled.This is useful for creating a long bus, and the router can trim the unused part after connecting pins to the bus.Note that antenna here means dangling wires.

droute_ultraWideWireMode

The droute_ultraWideWireMode variable specifies the routing grids used for ultra wide wire routing. If the value is set to 0, regular routing grids are used. If the value is set to 1, wide routing grids are used. If the value is set to a larger value, even wider grids are used.Setting a large value for ultra wide wires can lead to fast routing time due to coarser grids for them. This is useful for the flip-chip designs.

droute_wireWidenForceWrongWay

The droute_wireWidenForceWrongWay variable specifies whether to force widened wrong-way wires. If the value is set to 0, the router does not force widened wrong-way wires. If the values is set to 1, the router forces widened wrong-way wires to improve coverage of widened wires.

droute_wireWidenIgnoreMinEdgeLengthVio

The droute_wireWidenIgnoreMinEdgeLengthVio variable specifies whether to ignore the minimum edge length rule during wire widening. If the value is set to 0, the router checks all DRC violations during wire widening. If the value is set to 1, the router does not check the minimum edge length violation during wire widening.

droute_wireWidenPieceWise

The droute_wireWidenPieceWise variable specifies whether to widen a wire segment uniformly or to widen it piece by piece. If the value is set to 0, the router will widen a wire segment uniformly. If the value is set to 1, the router first breaks a wire into several pieces according to its neighboring routing objects, then tries to widen each piece with different width. This nonuniform widening can improve coverage of widened wires.

droute_wireWidenSrLoop

The droute_wireWidenSrLoop variable specifies the number of search and repair loops after wire widening. If the value is set to N, the router runs N loops of search and repair after wire widening to fix DRC violations created during wire widening.

droute_wireWidenTimingDriven

The droute_wireWidenTimingDriven variable specifies whether to widen wires on timing-critical nets. If the value is set to 0, the router does wire widening on all signal wires. If the value is set to 1, the router does not widen wires on timing-critical nets.

droute_wireWidenWidthScheme

The droute_wireWidenWidthScheme variable specifies how many different widths are used for wire widening. If the value is set to N, the router tries N different widths during wire widening.

droute_wrongWayExtraCost

The droute_wrongWayExtraCost variable specifies extra wrong-way wire cost. The default wrong-way unit distance cost is 2 (versus default right-way unit distance cost of 1).If the value is set to 0, no extra wrong-way cost is added. Otherwise, if the value is set to N, the wrong-way unit distance cost is 2 + N. Therefore, if the value is set to 2, the wrong-way cost is four times the right-way unit distance cost.This variable can be used to further discourage wrong-way direction routing. It can be especially useful if you observe excessive wrong-way direction routing during the route net group command, where most nets are not routed yet.

duplicate_ports

Specifies whether ports are to be drawn on every sheet for which an input or output signal appears.

Default value for this variable is false.

echo_include_commands

Controls whether the contents of a script file is printed as it executes.

Default value for this variable is true.

enable_cell_based_verilog_reader

This variable turns on the verilog2cel verilog reader.

Default value for this variable is false.

enable_instances_in_report_net

Enables report_net to report on instances in the current design.

Default value for this variable is true.

enable_page_mode

Controls whether long reports are displayed one page at a time (similar to the UNIX more command).

Default value for this variable is false.

enable_recovery_removal_arcs

Controls whether Design Compiler accepts recovery and removal arcs that are specified in the technology library.

Default value for this variable is false.

enable_slew_degradation

Determines whether the transition degradation is taken into account for nets with physical information.

Default value for this variable is true.

enable_special_level_shifter_naming

Setting this variable to true would enable special naming for automatically inserted level shifters

Default value for this variable is false.

estimate_io_latency

Uses estimated I/O latency in timing calculations for ports when true.

Default value for this variable is false.

exit_delete_command_log_file

Controls whether the file specified by the variable command_log_file is deleted after design_analyzer or dc_shell exits normally.

Default value for this variable is false.

exit_delete_filename_log_file

Controls whether the file specified by the variable filename_log_file is deleted after design_analyzer or dc_shell exits normally.

Default value for this variable is true.

filename_log_file

Specifies the name of the filename log file to be used in case a fatal error occurs during execution of design_analyzer or dc_shell.

Default value for this variable is filenames.log.

find_allow_only_non_hier_ports

Controls find command to search for ports in sub-designs (described as hier_ports here).

Default value for this variable is false.

find_converts_name_lists

Controls whether the find command converts the *name_list* string to a list of strings before searching for design objects.

Default value for this variable is false.

find_ignore_case

Controls whether the find command is case-sensitive when matching object names.

Default value for this variable is false.

focalopt_endpoint_margin

Read and set the endpoint slack value during focal_opt setup or hold optimization.

Default value for this variable is true.

fsm_auto_inferring

Determines whether or not to automatically extract finite state machine during the compile.

Default value for this variable is false.

fsm_enable_state_minimization

Determines whether or not the state minimization is performed for all finite state machines (FSMs) in the design.

Default value for this variable is false.

fsm_export_formality_state_info

Determines whether or not state machine encoding information is exported into the files that will be used by Formality.

Default value for this variable is false.

gen_bussing_exact_implicit

Controls whether schematics generated using the create_schematic -implicit command should contain implicit bus names instead of bus rippers.

Default value for this variable is false.

gen_cell_pin_name_separator

Specifies the character used to separate cell names and pin names in the bus names generated by the create_schematic command.

Default value for this variable is /.

gen_create_netlist_busses

Controls whether create_schematic creates netlist buses whenever it creates buses on the schematic.

Default value for this variable is true.

gen_dont_show_single_bit_busses

Controls whether single-bit buses are generated in the schematic.

Default value for this variable is false.

gen_match_ripper_wire_widths

Controls whether the create_schematic command generates rippers whose width always equals the width of the ripped net.

Default value for this variable is false.

gen_max_compound_name_length

Controls the maximum length of compound names of bus bundles (for the create_schematic -sge command).

Default value for this variable is 256.

gen_max_ports_on_symbol_side

Specifies the maximum allowed size of a symbol created by create_schematic.

Default value for this variable is 0.

gen_open_name_postfix

Specifies the postfix to be used by create_schematic -sge when creating placeholder net names for unconnected pins.

Default value for this variable is "".

gen_open_name_prefix

Specifies the prefix to be used by create_schematic -sge when creating placeholder net names for unconnected pins.

Default value for this variable is Open.

gen_show_created_busses

Controls whether a message is printed out every time a schematic bus is created from cell pins for which no equivalent net bus exists in the netlist.

Default value for this variable is false.

gen_show_created_symbols

Controls whether create_schematic prints a warning message every time it generates a new symbol for a cell because an appropriate symbol could not be found in the symbol libraries.

Default value for this variable is false.

gen_single_osc_per_name

Controls whether more than one off-sheet connector with any particular name is drawn on any schematic sheet.

Default value for this variable is false.

generic_symbol_library

Specifies the generic symbol library used for schematics.

Default value for this variable is generic.sdb.

groute_VABoundaryToLSWeight

The groute_VABoundaryToLSWeight variable is used in multivoltage mode. It specifies the value to adjust the cost for a level-shifter connection when switching voltage area from one to another.

groute_avoidCouplingUser

The groute_avoidCouplingUser variable enables the global router to space nets during routing. The nets to be considered need to be set with the Set Net Constraints command. If this variable is set to 1, timing spacing will be honored.

groute_avoidXtalk

The groute_avoidXtalk variable turns on/disables crosstalk prevention during global routing. If this variable is set to 1, the global router tries to avoid assigning nets with coupling to the same gcell.

groute_blncdToSkewCntrlRatio

The groute_blncdToSkewCntrlRatio variable sets a threshold for turning on the balanced skew control mode. For nets with an aspect ratio smaller than the variable value, balanced skew control mode is enabled. The aspect ratio is calculated based on the bounding box formed by enclosing the pins.

groute_blockEdgeAccess

The groute_blockEdgeAccess variable allows the global router to access pins on edges of hard macros. By default, the global router reaches pins on edges of hard macros. When the variable is set to 1, it allows the global router is allowed to access or drop vias on whole macro pins without edges limitation.

groute_brokenNetsThresholdPercent

The groute_brokenNetsThresholdPercent variable specifies a threshold for incremental global routing to be performed. This is effective when incremental is set to 1.

groute_clockBalanced

The groute_clockBalanced variable turns balanced routing on clock nets on and off.

groute_clockComb

The groute_clockComb variable enables the global router to connect ports directly to the prerouted clock trunks to minimize clock skew. Be aware that this requires greater routing resources, if the clock pins are not close to the clock trunks. The Comb mode works on designs with pre-existing clock nets.

groute_combDistance

The groute_combDistance variable sets a distance threshold, in gcell units, for clock routing to connect clock pins directly to clock nets.

groute_combMaxConnections

The groute_combMaxConnections variable limits the number of direct connections allowed to the clock pins from the same clock trunk. The default value of -1 allows a clock net to be connected to any number of clock pins.

groute_compactMode

The groute_compactMode variable determines the size of gcell used for global routing. If it is set to 0, gcells of 1 cellrow height will be created. If it is set to 1, the global router automatically adjusts the global route cell size.Increasing the size of gcell will complete the global routing faster at the cost of quality as routing becomes coarser.

groute_congestionWeight

The groute_congestionWeight variable specifies the relative importance of routing congestion versus wire length. As the variable value increases, the router tries harder to avoid routing congestion at the cost of increased wire length.

groute_densityDriven

The groute_densityDriven variable turns density-driven global routing on or off. In the default mode, the router decides the weight given to density relative to wire length during global routing. If timing driven or crosstalk is turned on, global route turns on the groute_densityDriven automatically.

groute_detourLimitMinNetLen

The groute_detourLimitMinNetLen variable controls the way the global router implements maxDetourPercent on nets. If the value is set to 0, the router forces maxDetourPercent on all nets. If the value is set to n, maxDetourPercent is applied only to nets of length greater than n gcells.

groute_extraCostsApplyPercent

The groute_extraCostsApplyPercent variable applies the wireCost and viaCost settings to the top n percent of nets in the design. The wireCost and viaCost variables are route variables. The route extra cost applies to global routing, track assignment and detail routing. This variable applies the extra cost percentage only for global route.

groute_extraWireLengthOpt

The groute_extraWireLengthOpt variable instructs the global router to run an additional rerouting phase to reduce wire length on nets that have no congestion. It does not perform any optimization.

groute_forceUpperLayersForCritNets

The groute_forceUpperLayersForCritNets variable specifies the mode for upper layers usage. To improve timing, IC Compiler will route timing-critical nets on upper layers that have lower RC.

groute_horReserveTracks

The groute_horReserveTracks variable determines the number of horizontal free tracks reserved in each gcell.

groute_ignoreViaBlockage

The groute_ignoreViaBlockage variable specifies the mode to honor a via blockage. By default, global route ignores via blockage.

groute_incremental

The groute_incremental variable controls whether global router runs groute_incrementally.

groute_macroBndryDir

The groute_macroBndryDir variable controls the use of macroBndryTrkUtil for layers in different directions. If the value is set to 1, macroBndryTrkUtil will be applied to layers in both directions.

groute_macroBndryTrkUtil

The groute_macroBndryTrkUtil variable limits the utilization of tracks available in the gcells near a macro boundary to a specified percentage. This variable is used to control the accessibility of pins and congestion at the macro boundaries. By default, the router uses 100 percent of available tracks in the macro boundary width.

groute_macroBndryWidth

The groute_macroBndryWidth variable specifies a distance from the corners of macros. Within this distance, the global router obeys the limits on track utilization specified by macroCornerTrkUtil and macroBndryTrkUtil. By default, one row or column of gcells is considered from the corners of the macro.

groute_macroCornerTrkUtil

The groute_macroCornerTrkUtil variable limits the utilization of tracks available in the gcells near a macro corner to a specified percentage. This variable is used to control the accessibility of pins and congestion at the macro corners. By default, the router uses 100 percent of available tracks in the macro boundary width.

groute_mapOnly

The groute_mapOnly variable specifies whether the router generates the congestion map based on global routing without creating the global wires.

groute_maxDetourPercent

The groute_maxDetourPercent variable directs the global router to have no more than the specified percentage of detours on any net. If the value is set to -1, the router is free to make any number of detours (or none).

groute_netCriticality

The groute_netCriticality variable determines the order in which the global router routes the nets during initial route. Net criticality can be set on nets in the design by using the Scheme function dbSetNetCriticality. If this variable is set to 1, the global router first routes the nets with higher criticality value. If the value is set to 0, net criticality has no effect on routing order. However, net criticality always has an effect on the congestion cost.

groute_noTopLevelBusFeedThroughs

The groute_noTopLevelBusFeedThroughs variable determines whether feedthroughs are allowed on bus signals.

groute_paEqPinNetMaxPort

Setting the groute_paEqPinNetMaxPort variable to 1 creates equivalent pins for nets with no more than n ports.

groute_powerDriven

The groute_powerDriven variable turns power-driven global routing on or off.

groute_rcOptByLength

The groute_rcOptByLength variable controls the choice of layers for global router to reduce RC. The global router chooses layers with lower RC values based on the value of this variable. This variable is only active when the timing driven global route option is enabled.

groute_reportDemandOnly

The groute_reportDemandOnly variable specifies the mode to report demand only. In this mode, IC Compiler performs virtual route only, with no reroute phases. In the log file, it reports average gcell capacity per layer.

groute_reportEffectiveOverflow

The groute_reportEffectiveOverflow variable specifies the mode for generating an effective overflow report.

groute_reportGCellDensity

The groute_reportGCellDensity variable controls reporting of gcell density for each layer. In density-driven mode, the router generates a report of gcell density. However, this variable is independent of the density-driven switch.

groute_reportNetOrdering

The groute_reportNetOrdering variable specifies the number of nets to be reported according to the routing order. By default, the global router does not report on net ordering. If this variable is set to n, global route will report the first n nets in the order of routing.

groute_reserveTracksForPowerFile

The file indicated by the groute_reserveTracksForPowerFile variable is used to define the percentage of routing tracks on each layer that are reserved for power routing. For example, Suppose the reservedTracks.rc file defines METAL1 layer as 20. Then, the router reserves 20 percent of available routing tracks in METAL1 for power routing later. Therefore, global route uses only 80 percent of the routing tracks.

groute_skewControl

The groute_skewControl variable turns skew control on or off during global routing. If the value is set to 1, the global router tries to minimize the gross delay in net skew. Skew control applies to all signal nets (except for small nets) but skew control for clock nets occurs only when clockBalanced is set to 1.

groute_skewControlWeight

The groute_skewControlWeight variable determines the importance given to skew control on the net during global routing. You can set the skew control weight from 1 to 10 based on net criticality.

groute_speed

The groute_speed variable specifies the effort at which the global router should run. The global router runs a different number of phases, depending on the specified value. It is recommended you run the router in default mode.

groute_timingDriven

The groute_timingDriven variable turns timing-driven global routing on or off. The timingWeight variable controls the trade-off between timing and wire length during global routing. By default, timing-driven mode is turned off.

groute_timingWeight

The groute_timingWeight variable sets the weight given to the timing relative to wire length during global routing. This variable is effective only in timing-driven mode.

groute_turboMode

The groute_turboMode variable is used to improve runtime.

groute_verReserveTracks

The groute_verReserveTracks variable determines the number of vertical free tracks reserved in each gcell.

groute_xtalkWeight

The groute_xtalkWeight variable defines the weight given to crosstalk prevention during global routing.

gui_custom_setup_files

Specifies the GUI customization files to be loaded when the GUI starts up.

This variable can be set in the application setup file to specify a set of files that should be sourced to customize the GUI when the GUI starts up. This variable is intended for use by companies or teams that want to share some customization of the GUI. Typically the file will contain commands to specify hotkeys, menus, or toolbars which implement customer-specific functions to support their environment or flow. .p The GUI will initialize itself and then search the list of files in order. Each file in the list which exists it will be sourced. Finally, the user's .synopsys_<app>_gui.tcl file will be loaded to complete the customizations. .p To disable the loading of the customizations the gui_disable_custom_setup(3) variable can be used.

Default value for this variable is $synopsys/admin/setup/.synopsys_<app

gui_default_window_type

Read-only variable specifying the default window type for gui customization commands.

This read-only variable has the name of the window type that is used as the default when a menu, hotkey, or toolbar customization is specified without specifying a window type explicitly.

Default value for this variable is false.

gui_disable_custom_setup

Variable for disabling gui customizations.

This variable can be set to true to specify that gui customizations should not be loaded when the gui starts up. This includes customizations specified in the gui_custom_setup_files(3) variable as well as the user's .synopsys_<app>_gui.tcl file.

Default value for this variable is false.

gui_online_browser

Specifies the name of the browser used to invoke the online help system from the help menu of the product

Default value for this variable is netscape.

hercules_home_dir

Specifies the path to the Hercules installation to be used for VUE to ICC integration.

Default value for this variable is "".

hier_dont_trace_ungroup

Disables ungroup tracing set on the design with the ungroup command.

Default value for this variable is 0.

high_fanout_net_pin_capacitance

Specifies the pin capacitance used to compute the loading of high-fanout nets.

Default value for this variable is 1.000000.

high_fanout_net_threshold

Specifies the minimum number of loads for a net to be classified as a high-fanout net.

Default value for this variable is 1000.

icc_magnetpl_stop_after_seq_cell

Controls if sequential cells need to be pulled towards a specified magnet during magnet_placement the with -stop_by_sequential_cells option.

Default value for this variable is false.

icc_snapshot_storage_location

Specifies the location for the create_qor_snapshot, remove_qor_snapshot, and report_qor_snapshot utilities.

Default value for this variable is snapshot.

ignore_guardband

Specifies that power switches inserted will not honor other voltage areas' guardband while executing command create_power_switch_array. The default is *false*.

Default value for this variable is false.

ilm_enable_power_calculation

Perform power calculation on design which is to be used as ILM block.

Default value for this variable is true.

ilm_ignore_percentage

Specifies a threshold for the percentage of total registers in the transitive fanout of an input port, beyond which the port is to be ignored when identifying interface logic.

Default value for this variable is 25.

ilm_preserve_core_constraints

Enables the ILM mode (ilm_mode), which preserves constraints set on an interface logic model (ILM) core, if set to true.

Default value for this variable is false.

in_gui_session

This read-only variable has the value "true" when the GUI is active and the value "false" when the GUI is not active.

This variable can be used in writing Tcl code that depends on the presence the graphical user interface (GUI). The read-only variable has the value "true" if gui_start has been invoked and the GUI is active. Otherwise, the variable has the value "false" (default).

Default value for this variable is false.

initial_target_library

Specifies the list of technology libraries of components to be used for the first part of leakage power optimization in place_opt.

Default value for this variable is "".

lbo_cells_in_regions

Puts new cells at specific locations within a cluster.

Default value for this variable is false.

level_shifter_naming_prefix

Using this variable, users can specify a prefix for the level shifters names

Default value for this variable is "".

lib_thresholds_per_lib

Causes trip-point values in the Synopsys library to override user-specified values.

Default value for this variable is true.

lib_use_thresholds_per_pin

Causes pin specific trip-point values in the Synopsys library to override Library default trip-point values.

Default value for this variable is true.

libgen_max_differences

Specifies to the read_lib command the maximum number of differences to list between the v3.1 format description of a library cell and its statetable description.

Default value for this variable is -1.

link_force_case

Controls the case-sensitive or case-insensitive behavior of the link command.

Default value for this variable is check_reference.

link_library

Specifies the list of design files and libraries used during linking.

Default value for this variable is * your_library.db .

ltl_obstruction_type

Controls the routing blockage type for the named obstructions, without route type being specified.

Default value for this variable is placement_only.

mcmm_enable_high_capacity_flow

Enables Multi-corner/Multi_mode (MCMM) high capacity flow in IC Compiler

Default value for this variable is false.

mcmm_high_capacity_effort_level

Controls the behavior of Multi-corner/Multi_mode (MCMM) scenario reduction.

Default value for this variable is 0.

monitor_cpu_memory

Displays the CPU time, elapsed time, and peak memory usage before and after each core command.

Default value for this variable is false.

mpc_disable_macro_fitting

Controls whether to disable the function that calculates core area to include all the macro blocks automatically.

Default value for this variable is false.

mpc_disable_pad_legalization

Controls whether to disable the function that legalizes I/O pad cells.

Default value for this variable is false.

mpc_dont_cut_pnet_over_macros

Controls whether power nets created in minimal physical constraints flow are to be cut over macros.

Default value for this variable is false.

mux_auto_inferring_effort

Specifies the MUX inferring effort level.

Default value for this variable is 2.

mv_allow_ls_on_leaf_pin_boundary

Sets the variable to true to allow level-shifter insertion on leaf pin (such as macro cell pin) boundaries.

Default value for this variable is false.

mw_allow_rect_and_polygon_in_def

Controls whether the read_def command imports rectangles and polygons in the special net section.

Default value for this variable is false.

mw_attr_value_extra_braces

Controls whether extra braces are added to the value returned by the get_attribute command.

Default value for this variable is false.

mw_attr_value_no_space

Controls whether the route_type and net_type attribute values returned by the get_attribute and report_attribute commands contain spaces or underscores.

Default value for this variable is false.

mw_cell_name

Contains the Milkyway design cell name.

Default value for this variable is "".

mw_design_library

Contains the Milkyway design library.

Default value for this variable is "".

mw_disable_escape_char

Specifies to disable the escape characters for hierarchy delimiter.

Default value for this variable is true.

mw_hdl_bus_dir_for_undef_cell

Specify how to determine the bus direction for undefined cell.

Default value for this variable is 0.

mw_hdl_expand_cell_with_no_instance

This variable determines whether to expand netlist cells without instances or not.

Default value for this variable is false.

mw_logic0_net

Contains the equivalent logic0 net for the design.

Default value for this variable is VSS.

mw_logic1_net

Contains the equivalent logic1 net for the design.

Default value for this variable is VDD.

mw_reference_library

Contains the Milkyway reference libraries.

Default value for this variable is "".

mw_site_name_mapping

Specifies pairs of site names that is used to synchronize floorplan's site name with physcal libary's site name.

Default value for this variable is "".

mwdc_allow_higher_mem_usage

Specifies the frequency that the tool flushes in-memory data to disk during optimization(including the mega commands place_opt/clock_opt/route_opt, and the command create_placement/legalize_placement, compile_clock_tree...). It should be set as one of the values 0, 1, and 2. The default value is 0. It can be used to tune runtime and memory.

Default value for this variable is 0.

optimize_reg_always_insert_sequential

Controls whether the optimize_registers command will remove and reinsert the sequential elements in the circuits even if no register was moved.

Default value for this variable is false.

optimize_reg_max_time_borrow

Specifies the maximum amount of time borrowing at all latches when retiming latches using the optimize_registers command. A negative value means there is no limit on borrowing other than the one resulting from the clock period.

Default value for this variable is -1048576.0.

optimize_reg_retime_clock_gating_latches

Specifies whether to move clock gating latches during retiming of latches.

Default value for this variable is false.

physopt_area_critical_range

Specifies a margin of slack for cells during area optimization. If a cell has a slack less than the area critical range, area optimization is not done for the cell.

Default value for this variable is -1.04858e+06.

physopt_change_list

Controls tracking of eco changes when physopt -incremental is running. By default the tracking is always on. Use this variable to turn off the tracking.

Default value for this variable is true.

physopt_check_site_array_overlap

Checks for multi-type site array overlapping in floorplan, within a certain threshold.

Default value for this variable is true.

physopt_checkpoint_stage

Writes an intermediate database at intervals during the physical optimization run.

Default value for this variable is 0.

physopt_cpu_limit

This variable is obsolete and cannot be enabled. Please use set_physopt_cpulimit_options command instead.

Default value for this variable is 0.

physopt_create_missing_physical_libcells

Directs IC Compiler to create dummy physical descriptions of missing physical library cells.

Default value for this variable is false.

physopt_delete_unloaded_cells

Controls whether the physopt command deletes unloaded cells, including both sequential and combinational cells.

Default value for this variable is true.

physopt_enable_extractor_rc

Enables and disables the support of extractor-based RC computation.

Default value for this variable is true.

physopt_enable_power_optimization

Enables power optimization in IC Compiler.

Default value for this variable is true.

physopt_enable_router_process

Enables and disables the use of a separate process to perform routing.

Default value for this variable is true.

physopt_enable_rp_in_xg_mode

Determines whether the tool is to honor relative placement in xg mode.

Default value for this variable is false.

physopt_enable_tlu_plus

Enables and disables the support of TLU+ based RC computation.

Default value for this variable is true.

physopt_enable_tlu_plus_process

Enables and disables using a separate process to perform TLU+ based RC extraction.

Default value for this variable is true.

physopt_enable_via_res_support

Enables and disables the support of via resistance for virtual route RC estimation.

Default value for this variable is false.

physopt_hard_keepout_distance

Specifies the keepout distance used by the physopt, create_placement, and legalize_placement commands.

Default value for this variable is 0.

physopt_heterogeneous_site_array

Enables the detailed placer to handle floorplan with multi-height site arrays in multi-voltage mode.

Default value for this variable is false.

physopt_ignore_lpin_fanout

The tool ignore max fanout constraints which are specfied in the library.

Default value for this variable is false.

physopt_ignore_structure

Determines whether the tool ignores the relative placement groups.

Default value for this variable is false.

physopt_macro_cell_height_threshold

Specifies the threshold value for the tool's detail placer to decide whether an extremely tall standard cell is to be treated as a "hard macro." The tool's detail placer is designed to place standard cells. If the design has some extremely tall standard cells, then the detail placer might not work as well as it does when placing "normal" standard cells. Thus, by default, if an extremely tall standard cell has a height that is greater than this threshold value, the detail placer treats the standard cell as a "hard macro."

Default value for this variable is 6.

physopt_mw_checkpoint_filename

Specifies the name of the file to which the MW database containing all hierarchy of the checkpointed design is to be written.

Default value for this variable is "".

physopt_new_fix_constants

Determines whether the tool is to observe the maximum capacitance constraint during tie-off optimization.

Default value for this variable is true.

physopt_pin_based_pad

Specifies whether is_pad attribute is set to pin.

Default value for this variable is false.

physopt_power_critical_range

Specifies a margin of slack for cells during leakage power optimization. If a cell has a slack less than the power critical range, power optimization will not be done for the cell.

Default value for this variable is -1.04858e+06.

physopt_ref_pdef_loaded

Stores the name of the reference loaded during report_cell_displacement -load_pdef. Otherwise, stores the null string.

Default value for this variable is "".

physopt_row_overlap_threshold

Specifies a threshold for checking multi-type site array overlapping floorplan.

Default value for this variable is 0.1.

physopt_rp_enable_orient_opt

Determines whether the tool is to allow orientation optimization of cells in relative placement groups.

Default value for this variable is true.

physopt_tie_const_cells

Connects all unconnected pins in the same hierarchy to one logic cell.

Default value for this variable is false.

physopt_tie_spare_cells

Instructs the physical optimization to connect the inputs of a spare cells to tie-off cells.

Default value for this variable is true.

physopt_ultra_high_area_effort

Enables very high effort area optimization for potentially better area recovery but with more runtime.

Default value for this variable is false.

placer_disable_auto_bound_for_gated_clock
Determines whether automatic group bounding is disabled for gated clocks created by Power Compiler.

Default value for this variable is true.

placer_disable_macro_placement_timeout
Prevents the coarse placer from timing out during macro placement.

Default value for this variable is false.

placer_dont_error_out_on_conflicting_bounds
Prevents the coarse placer from erroring out when it detects conflicting bounds.

Default value for this variable is true.

placer_enable_enhanced_router
Enables a mode of coarse placement in which congestion removal is done with the global router.

Default value for this variable is false.

placer_gated_register_area_multiplier
Specifies the value of the multiplier used to generate automatic group bounds for gated clocks.

Default value for this variable is 20.

placer_max_cell_density_threshold
Enables a mode of coarse placement in which cells can clump together.

Default value for this variable is -1.

placer_run_in_separate_process

Enables and disables the use of a separate process to perform placement.

Default value for this variable is true.

placer_soft_keepout_channel_width

Specifies a soft keepout distance that is used by the place_opt and create_placement commands.

Default value for this variable is 0.

port_complement_naming_style

Defines the convention the compile command uses to rename ports complemented as a result of using the set_boundary_optimization command.

Default value for this variable is %s_BAR.

power_cg_all_registers

Specifies to the insert_clock_gating command whether to clock gate all registers, including those that do not meet the necessary requirements.

Default value for this variable is false.

power_cg_balance_stages

Controls clock gate stage balancing is on or off during compile [-incremental_mapping] -gate_clock or compile_ultra [-incremental_mapping] -gate_clock.

Default value for this variable is false.

power_cg_cell_naming_style

Specifies the naming style for clock gating cells created during insert_clock_gating.

Default value for this variable is "".

power_cg_derive_related_clock

When *true*, clock domain relationship between registers will be derived from the hierarchical context.

Default value for this variable is false.

power_cg_designware

Performs clock gating on DesignWare sequential components in the design.

The use of power_cg_designware variable will be obsolete in a future release. Clock gating insertion with compile_ultra -gate_clock automatically inserts clock gates in DesignWare modules.

Default value for this variable is false.

power_cg_enable_alternative_algorithm

Specifies to the insert_clock_gating, compile-gate_clock and compile_ultra -gate_clock commands whether to use an alternative algorithm to find gatable registers.

Default value for this variable is false.

power_cg_flatten

Specifies to different ungroup commands whether to flatten Synopsys clock-gating cells.

Default value for this variable is false.

power_cg_gated_clock_net_naming_style

Specifies the naming style for gated clock nets created during insert_clock_gating.

Default value for this variable is "".

power_cg_ignore_setup_condition

When *true*, the setup condition will be ignored for latch-free clock gating.

Default value for this variable is false.

power_cg_inherit_timing_exceptions

Specifies that during compile -gate_clock or compile_ultra [-incr] -gate_clock, timing exceptions defined on registers have to be automatically inferred on to the enable pin of the clock gate that is gating these registers.

Default value for this variable is false.

power_cg_module_naming_style

Specifies the naming style for clock gating modules created during insert_clock_gating.

Default value for this variable is "".

power_cg_print_enable_conditions

When *true*, the enable conditions of registers and clock gates will be reported during clock gate insertion.

Default value for this variable is false.

power_cg_print_enable_conditions_max_terms

Specifies the maximum number of product terms to be reported in the sum of product expansion of the enable condition.

Default value for this variable is 10.

power_cg_reconfig_stages

Controls the reconfiguration of multistage clock gates during compile [-incremental_mapping] -gate_clock or compile_ultra [-incremental_mapping] -gate_clock.

Default value for this variable is false.

power_default_static_probability

Specifies the default static probability value.

Default value for this variable is 0.5.

power_default_toggle_rate

Specifies the default toggle rate value.

Default value for this variable is 0.1.

power_default_toggle_rate_type

Specifies the default toggle rate type.

Default value for this variable is fastest_clock.

power_do_not_size_icg_cells

Controls whether compile does not size the integrated clock-gating cells in a design to correct DRC violations because doing so may result in lower area and power.

Default value for this variable is false.

power_driven_clock_gating

Controls whether switching activity and dynamic power of the register banks should be considered when optimizing the clock gating of the design.

Default value for this variable is false.

power_enable_one_pass_power_gating

When *true*, one-pass flow power gating will be enabled.

Default value for this variable is false.

power_enable_power_gating

When set to true compile will enable the power gating flow which allows the selected retention registers from target library to be used to map sequential elements.

Default value for this variable is false.

power_fix_sdpd_annotation

Specifies whether user-annotated SDPD switching activity annotation is corrected before it is used.

Default value for this variable is true.

power_fix_sdpd_annotation_verbose

Specifies whether verbose messages are reported during fixing of user-annotated SDPD switching activity.

Default value for this variable is false.

power_hdlc_do_not_split_cg_cells

When *true*, nsert_clock_gating does not split clock-gating cells to limit their fanout.

Default value for this variable is false.

power_keep_license_after_power_commands

Affects the amount of time a Power Compiler license is checked out during a dc_shell (Design Compiler) session.

Default value for this variable is false.

power_lib2saif_rise_fall_pd

Specifies whether lib2saif generates forward SAIF files with directives to generate rise/fall dependent path-dependent toggle counts.

Default value for this variable is false.

power_min_internal_power_threshold

Specifies the minimum cell internal power value that can be used in power calculations.

Default value for this variable is "".

power_model_preference

Specifies the preference between the CCS power and the NLPM models in library cells that have power specified in both models.

Default value for this variable is ccs.

power_opto_extra_high_dynamic_power_effort

This variable makes the compile command invoke more dyanmic power optimization algorithms.

Default value for this variable is false.

power_preserve_rtl_hier_names

Preserves the hierarchy information of the RTL objects in the RTL design.

Default value for this variable is false.

power_rclock_inputs_use_clocks_fanout

Specifies whether clock network objects in an input port fanout are used to infer the input port's related clock.

Default value for this variable is true.

power_rclock_unrelated_use_fastest

Specifies whether the fastest clock is set as the related clock of a design object when a related clock is not inferred by the related clock inference mechanism.

Default value for this variable is true.

power_rclock_use_asynch_inputs

Specifies whether the inferred related clock on an asynchronous pin of a flip-flop is used to determine the nferred related clock on the cell's outputs.

Default value for this variable is false.

power_remove_redundant_clock_gates

Specifies to the compile -incremental and physopt -incremental commands whether to remove redundant Synopsys clock gating cells.

Default value for this variable is true.

power_rtl_saif_file

Defines for the rtl2saif command where to store the forward-annotation SAIF file, if you do not specify the -output option.

Default value for this variable is power_rtl.saif.

power_sa_propagation_effort

Specifies the default effort level used when propagating switching activity.

Default value for this variable is low.

power_sa_propagation_verbose

Specifies the default verbose mode used when propagating switching activity.

Default value for this variable is false.

power_same_switching_activity_on_connected_objects

Forces the tool to use the last user-annotated switching activity data on all connected tool objects.

Default value for this variable is false.

power_sdpd_message_tolerance

Specifies the tolerance value for issuing warnings and information messages during fixing of user-annotated SDPD switching activity.

Default value for this variable is 0.00001.

power_sdpd_saif_file

Defines for the lib2saif command where to store the forward-annotation SAIF file, if you do not specify the -output option.

Default value for this variable is power_sdpd.saif.

psyn_onroute_disable_cap_drc

This variable turns on and off the max_cap fixing optimization during route_opt DRC fixing

Default value for this variable is "".

psyn_onroute_disable_fanout_drc

This variable turns on and off the max_fanout optimization during route_opt DRC fixing

Default value for this variable is "".

psyn_onroute_disable_hold_fix

This variable turns on and off the hold fixing optimization during route_opt.

Default value for this variable is "".

psyn_onroute_disable_netlength_drc

This variable turns on and off the max_net_length_fixing optimization during route_opt DRC fixing

Default value for this variable is "".

psyn_onroute_disable_trans_drc

This variable turns on and off the max transition fixing during route_opt DRC fixing

Default value for this variable is "".

psyn_stress_map

Enables generation of stress map. Set this variable to true to generate stress maps from IC Compiler.

Default value for this variable is false.

psynopt_high_fanout_legality_limit

The maximum high fanout threshold for performing optimization tricks before route_opt. This limit value also turns the feature off by setting it to 0.

Default value for this variable is 0.

rc_degrade_min_slew_when_rd_less_than_rnet

Enables or disables the use of slew degradation in min analysis mode during the RCCALC-009 condition.

Default value for this variable is false.

rc_driver_model_mode

Specifies which driver model type to use for RC delay calculation.

Default value for this variable is basic.

rc_input_threshold_pct_fall

Specifies the threshold voltage that defines the startpoint of the falling cell or net delay calculation.

Default value for this variable is 50.000000.

rc_input_threshold_pct_rise

Specifies the threshold voltage that defines the startpoint of the rising cell or net delay calculation.

Default value for this variable is 50.000000.

rc_noise_model_mode

When set to advanced, enables the use of CCS noise, if available in the design library.

Default value for this variable is basic.

rc_output_threshold_pct_fall

Specifies the threshold voltage that defines the startpoint of the falling cell or net delay calculation.

Default value for this variable is 50.000000.

rc_output_threshold_pct_rise

Specifies the threshold voltage that defines the startpoint of the rising cell or net delay calculation.

Default value for this variable is 50.000000.

rc_receiver_model_mode

Specifies which receiver model type to use for RC delay calculation.

Default value for this variable is basic.

rc_slew_derate_from_library

Specifies the derating needed for the transition times in the Synopsys library to match the transition times between the characterization trip points.

Default value for this variable is 1.000000.

rc_slew_lower_threshold_pct_fall
Specifies the threshold voltage that defines the endpoint of the falling slew calculation.

Default value for this variable is 20.000000.

rc_slew_lower_threshold_pct_rise
Specifies the threshold voltage that defines the startpoint of the rising slew calculation.

Default value for this variable is 20.000000.

rc_slew_upper_threshold_pct_fall
Specifies the threshold voltage that defines the startpoint of the falling slew calculation.

Default value for this variable is 80.000000.

rc_slew_upper_threshold_pct_rise
Specifies the threshold voltage that defines the endpoint of the rising slew calculation.

Default value for this variable is 80.000000.

read_db_lib_warnings
Indicates that warnings are to be printed while a technology .db library is being read in with the read command. When false (the default), no warnings are given.

Default value for this variable is false.

read_translate_msff
Indicates (when *true*, the default) that master-slave flip-flops (specified with the clocked_on_also syntax) are to be automatically translated to master-slave latches. When *false*, both master and slave remain flip-flops.

Default value for this variable is true.

register_duplicate

Controls whether compile should invoke Register duplication or not.

Default value for this variable is false.

reoptimize_design_changed_list_file_name

Creates a file in which to store the list of cells that changed and cells and nets that were added during post-layout or in-place optimization.

Default value for this variable is "".

report_default_significant_digits

Sets the default number of significant digits for many reports.

Default value for this variable is -1.

route_layerExtraCostByRC

The route_layerExtraCostByRC variable specifies extra layer cost. It will control the choice of layers for detailed router to reduce RC. If the value is set to 0, user specified extra cost for all layers will be used. If the value is set to 1, extra cost of all poly and metal layers previously defined as 0 will be re-computed based on RC. If the value is set to 2, extra cost of all poly, metal layers, and vias previously defined as 0 will be re-computed based on RC.

routeopt_allow_min_buffer_with_size_only

Allows the post-route hold fixing to add buffers even in size-only mode

routeopt_checkpoint

Writes an intermediate CEL at intervals during the route_opt

Default value for this variable is false.

routeopt_density_limit

The maximum cell density threshold for performing optimization tricks in a window around the location of the given cell or pin.

Default value for this variable is 0.95.

routeopt_disable_cpulimit

The internally defined threshold for the number of changes in one optimzation will be disabled.

Default value for this variable is false.

routeopt_drc_over_timing

Specifies the cost proirity between max_design_rule cost and max_delay cost during DRC fixing inside route_opt.

Default value for this variable is false.

routeopt_preserve_routes

The slight route disturbances caused by routeopt optimization will be reconnected in the appropriate metal layers and the reconnected routes writen to the database.

Default value for this variable is true.

routeopt_skip_report_qor

Skip QoR reports in the last stage during the route_opt

Default value for this variable is false.

routeopt_xtalk_reduction_setup_threshold

The threshold of setup delta delay to perform cross talk reduction

Default value for this variable is 0.1.

rp_shift_column_for_fixed_cells

Determines whether the tool allows the horizontal shifting of relative placement columns in the presence of single tap cells.

Default value for this variable is false.

sdc_write_unambiguous_names

Ensures that cell, net, pin, lib_cell, and lib_pin names that are written to the SDC file are not ambiguous.

Default value for this variable is true.

sdfout_allow_non_positive_constraints

Writes out PATHCONSTRAINT constructs with nonpositive (<= 0) constraint values. This variable will be obsolete in the next release. Please adjust your scripts accordingly.

Default value for this variable is false.

sdfout_min_fall_cell_delay

Specifies the minimum non-back-annotated fall cell delay that the write_timing command writes to a timing file in SDF format. This variable will be obsolete in the next release. Please adjust your scripts accordingly.

Default value for this variable is 0.000000.

sdfout_min_fall_net_delay

Specifies the minimum non-back-annotated fall net delay that write_timing can write to a timing file in SDF format. This variable will be obsolete in the next release. Please adjust your scripts accordingly.

Default value for this variable is 0.000000.

sdfout_min_rise_cell_delay

Specifies the minimum non-back-annotated rise cell delay that write_timing can write to a timing file in SDF format. This variable will be obsolete in the next release. Please adjust your scripts accordingly.

Default value for this variable is 0.000000.

sdfout_min_rise_net_delay

Specifies the minimum non-back-annotated rise net delay that the write_timing command can write to a timing file in SDF format. This variable will be obsolete in the next release. Please adjust your scripts accordingly.

Default value for this variable is 0.000000.

sdfout_time_scale

Specifies the time scale of the delays written to timing files in SDF format. This variable will be obsolete in the next release. Please adjust your scripts accordingly.

Default value for this variable is 1.000000.

sdfout_top_instance_name

Specifies the name prepended to all instance names when writing timing files in SDF format. This variable will be obsolete in the next release. Please adjust your scripts accordingly.

Default value for this variable is "".

sdfout_write_to_output

Specifies whether the write_timing -f sdf command writes interconnect delays between cells and top-level output ports. This variable will be obsolete in the next release. Please adjust your scripts accordingly.

Default value for this variable is false.

search_path

Specifies directories that the tool searches for files specified without directory names.

Default value for this variable is {fIsearch_pathfP + .}.

sh_allow_tcl_with_set_app_var

Allow set_app_var and get_app_var commands to work with application variables

Default value for this variable is Application specific.

sh_allow_tcl_with_set_app_var_no_message_list

Suppress CMD-104 messages for variables in this list

Default value for this variable is Application specific.

sh_arch

Indicates the system architecture of your machine.

Default value for this variable is Platform-dependent.

sh_command_abbrev_mode

Sets the command abbreviation mode for interactive convenience.

Default value for this variable is Application specific.

sh_command_log_file

Specifies the name of the file to which is written a log of the initial values of variables and executed commands.

Default value for this variable is command.log.

sh_continue_on_error

Allows processing to continue when errors occur during script execution with the source command.

Default value for this variable is Application specific.

sh_dev_null

Indicates the current null device.

Default value for this variable is Platform-dependent.

sh_enable_line_editing

Enables the command line editing capabilities. This variable is for use in Tcl mode only.

Default value for this variable is true.

sh_enable_page_mode

Displays long reports one page at a time (similar to the UNIX more command.

Default value for this variable is Application specific.

sh_enable_stdout_redirect

Allow the redirect command to capture output to the Tcl stdout channel.

Default value for this variable is Application specific.

sh_line_editing_mode

Enables vi or emacs editing mode. This variable is for use in Tcl mode only.

Default value for this variable is emacs.

sh_new_variable_message

Controls a debugging feature for tracing the creation of new variables.

Default value for this variable is Application specific.

sh_new_variable_message_in_proc

Controls a debugging feature for tracing the creation of new variables in a Tcl procedure.

Default value for this variable is false.

sh_new_variable_message_in_script

Controls a debugging feature for tracing the creation of new variables within a sourced script.

Default value for this variable is false.

sh_output_log_file

This read-write variable is used to name the file which all console output is captured. It can be set to an empty string to disable output capture.

This variable can be used to capture all console output in a file which can be useful for bug reproduction and reporting.

The first time the variable is set to a valid filename all previously logged output is added to the specified file and all subsequent logged output is appended to this file.

If the variable is subsequently changed to an empty string then all logged output is disabled.

If the variable is subsequently set to an non-empty string that is an invalid filename then the new value is ignored and the old value is restored.

If the variable is subsequently set to an non-empty string that is an valid filename then all subsequent logged output is appended to this file.

Default value for this variable is "".

sh_product_version

Indicates the version of the application currently running.

sh_script_stop_severity

Indicates the error message severity level which would cause a script to stop executing before it completes.

Default value for this variable is Application specific.

sh_source_emits_line_numbers

Indicates the error message severity level which would cause an informational message to be issued listing the script name and line number where that message occurred.

Default value for this variable is Application specific.

sh_source_logging

Indicates if individual commands from a sourced script should be logged to the command log file.

Default value for this variable is Application specific.

sh_source_uses_search_path

Causes the search command to use the search_path variable to search for files. This variable is for use in dc_shell-t (Tcl mode of dc_shell) only.

Default value for this variable is true.

sh_tcllib_app_dirname

Indicates the name of a directory where application-specific Tcl files are found.

sh_user_man_path

Indicates a directory root where the user can store man pages for display with the man command.

Default value for this variable is an empty list.

si_use_partial_grounding_for_min_analysis

Affects the behavior of report_timing and compile with crosstalk effect is enabled. .SH

Default value for this variable is false.

si_xtalk_reselect_delta_and_slack

Reselect nets that satisfy both delta delay and slack reselection criteria.

Default value for this variable is false.

si_xtalk_reselect_delta_delay

Specifies the threshold of net delay change caused by crosstalk analysis, above which IC Compiler reselects the net for subsequent delay calculations.

Default value for this variable is 5.

si_xtalk_reselect_delta_delay_ratio

Specifies the threshold of the ratio of net delay change caused by crosstalk analysis to the total stage delay, above which IC-Compiler reselects a net for subsequent delay calculations.

Default value for this variable is 0.95.

si_xtalk_reselect_max_mode_slack

Specifies the max mode pin slack threshold, below which IC-Compiler reselects a net for subsequent delay calculations.

Default value for this variable is 0.

si_xtalk_reselect_min_mode_slack

Specifies the min mode pin slack threshold, below which IC-Compiler reselects a net for subsequent delay calculations.

Default value for this variable is 0.

single_group_per_sheet

Specifies to the tool to put only one logic group on a sheet.

Default value for this variable is false.

site_info_file

Contains the path to the site information file for licensing.

Default value for this variable is "".

skew_opt_skip_clock_balancing

Controls whether the skew_opt tcl solution file applies set_inter_clock_delay_options commands when sourced.

Default value for this variable is false.

skew_opt_skip_ideal_clocks

Controls whether the skew_opt tcl solution file applies set_clock_latency commands when sourced.

Default value for this variable is false.

skew_opt_skip_propagated_clocks

Controls whether the skew_opt tcl solution file applies set_clock_tree_exceptions commands when sourced.

Default value for this variable is false.

sort_outputs

Sorts output ports on the schematic by port name.

Default value for this variable is false.

suppress_errors

Specifies a list of error codes for which messages are to be suppressed during the current Design Analyzer/dc_shell session.

Default value for this variable is PWR-18 OPT-932 OPT-317 RCCALC-010 RCCALC-011.

symbol_library
Specifies the symbol libraries to use during schematic generation.

Default value for this variable is your_library.sdb.

synopsys_program_name
Indicates the name of the program currently running.

synopsys_root
Indicates the root directory from which the application was run.

syntax_check_status
Reports whether the syntax_check mode is enabled.

Default value for this variable is false.

synthetic_library
Specifies a list of synthetic libraries to use when compiling.

Default value for this variable is "".

systemcout_debug_mode
Default value for this variable is false.

systemcout_levelize
Levelizes and flattens the netlist and replaces standard DesignWare operations with simulatable SystemC, before writing out the netlist, during write -f systemc command activity.

Default value for this variable is true.

target_library

Specifies the list of technology libraries of components to be used when compiling a design.

Default value for this variable is your_library.db.

template_naming_style

Generates automatically a unique name when a module is built.

Default value for this variable is %s_%p.

template_parameter_style

Generates automatically a unique name when a module is built.

Default value for this variable is %s%d.

template_separator_style

Generates automatically a unique name when a module is built.

Default value for this variable is _.

text_editor_command

Specifies the command that executes when the Edit/File menu is selected in the Design Analyzer text window.

Default value for this variable is xterm.

text_print_command

Specifies the command that executes when the File/Print menu is selected in the Design Analyzer text window.

Default value for this variable is lpr.

timing_ccs_load_on_demand

Enables or disables incremental loading of Composite Current Source (CCS) libraries.

Default value for this variable is true.

timing_check_defaults

define the default check list in check_timing command.

Default value for this variable is generated_clock loops no_input_delay unconstrained_endpoints pulse_clock_cell_type no_driving_cell partial_input_delay.

timing_clock_gating_propagate_enable

Allow the gating enable signal delay to propagate through the gating cell.

Default value for this variable is false.

timing_crpr_remove_clock_to_data_crp

Allows the removal of Clock Reconvergence Pessimism (CRP) from paths that fan out directly from clock source to the data pins of sequential devices.

Default value for this variable is false.

timing_crpr_threshold_ps

Specifies amount of pessimism that clock reconvergence pessimism removal (CRPR) is allowed to leave in the report.

Default value for this variable is 20.

timing_disable_cond_default_arcs

Disable the default, non-conditional timing arc between pins that do have conditional arcs.

Default value for this variable is false.

timing_edge_specific_source_latency

Controls whether the generated clock source latency computation will consider edge relationship or not.

Default value for this variable is false.

timing_enable_multiple_clocks_per_reg

Enables or disables analysis of multiple clocks that reach a single register.

Default value for this variable is false.

timing_enable_non_sequential_checks

Enables or disables library non_sequential checks in the design.

Default value for this variable is false.

timing_gclock_source_network_num_master_registers

The maximum number of register clock pins clocked by the master clock allowed in generated clock source latency paths.

Default value for this variable is 1.

timing_input_port_clock_shift_one_cycle

Determines whether or not paths originating at input ports are given an extra cycle to meet their timing constraints. This variable will be obsolete in the next release. Please adjust your scripts accordingly.

Default value for this variable is true.

timing_input_port_default_clock

Determines whether a default clock is assumed at input ports for which you have not defined a clock-specific input external delay.

Default value for this variable is true.

timing_remove_clock_reconvergence_pessimism

Enables or disables clock reconvergence pessimism removal.

Default value for this variable is false.

timing_report_attributes

Specifies the list of attributes to be reported with the report_timing -attributes command.

Note: This variable will be obsolete in the next release. Please adjust your scripts accordingly.

Default value for this variable is {dont_touch dont_use map_only size_only ideal_net}.

timing_self_loops_no_skew

Affects the behavior, runtime, and CPU usage of report_timing and compile.

Note: This variable will be obsolete in the next release. Please adjust your scripts accordingly.

Default value for this variable is false.

timing_separate_clock_gating_group

Specifies if a separate cost group is used for clock gating checks in timing analysis, reports, and optimization.

Default value for this variable is false.

timing_use_clock_specific_transition

Propagate the transition from the specific clock path for latency calculation

Default value for this variable is true.

timing_use_driver_arc_transition_at_clock_source

Uses the backward cell arc to compute a realistic driver model at the driver pin for primary clock sources and also generated clock that can not trace back to its master clock

Default value for this variable is true.

timing_use_enhanced_capacitance_modeling

Specifies the use of the following attributes found on a library pin: rise_capacitance_range(low, high), fall_capacitance_range(low, high), rise_capacitance, and fall_capacitance.

Default value for this variable is false.

trackAssign_XTalkParam

The trackAssign_XTalkParam variable defines the cost for crosstalk prevention. Use this variable when is enabled.

trackAssign_densityDriven

The trackAssign_densityDriven variable specifies the mode of density driven for track assignment.

trackAssign_evenSpaceAdjustment

The trackAssign_evenSpaceAdjustment variable specifies the mode of cost calculation for wire spreading.

trackAssign_minimizeJog

The trackAssign_minimizeJog variable specifies the mode to minimize jogs.

trackAssign_noOffGridRouting

The trackAssign_noOffGridRouting variable specifies the switch for off-grid routing on macro pins.

trackAssign_noiseThreshold

The trackAssign_noiseThreshold variable specifies the noise threshold for track assignment.

trackAssign_parallelLimit

The trackAssign_parallelLimit variable is used to specify parallel lengths limit. Use this variable when is enabled.

trackAssign_parallelLimitMode

The trackAssign_parallelLimitMode variable is set to break long wire mode on or off. When it is on, track assignment breaks the long wire if it exceeds the parallel length or the capacitance limit.

trackAssign_runTimingMode

The trackAssign_runTimingMode variable turns enables or disables the timing-driven track assignment. A value set to timing cost decides the importance of timing relative to wire length during track assignment. By default timing-driven track assignment is disabled.

trackAssign_runXTalkIter

The trackAssign_runXTalkIter variable allows you to specify the number of extra iterations for crosstalk during track assignment. The default number of iterations are determined automatically. Use this variable when is enabled.

trackAssign_runXTalkMode

The trackAssign_runXTalkMode variable is used to enable or disable the crosstalk mode during track assignment.

trackAssign_timingCost

The trackAssign_timingCost variable sets the weight given to timing relative to the wire length during track assignment. This variable is effective only when is set to 1, which runs track assignment in timing-driven mode.

trackAssign_tryGlobalLayerFirst

The trackAssign_tryGlobalLayerFirst variable specifies the mode to use global layer first.

trackAssign_tryGlobalLayerOnly

The trackAssign_tryGlobalLayerOnly variable specifies the mode to use only global layer during track assignment.

trackAssign_variableWidthAdjustment

The trackAssign_variableWidthAdjustment variable specifies the width adjustment for fat wire tracks. The calculation of number of tracks for a fat wire will occupy is sometime too conservative, that is, track assignment will reserve too many tracks for each fat wire. The trackAssign_variableWidthAdjustment variable can help reduce the demand and pack the fat wires more tightly.

ungroup_keep_original_design

Controls ungroup and compile command to keep the original design when a design is ungrouped.

Default value for this variable is false.

uniquify_keep_original_design

Controls uniquify command to keep the original design when a multiply instantiated design is uniqufied in XG mode.

Default value for this variable is false.

uniquify_naming_style

Specifies the naming convention to be used by the uniquify command.

Default value for this variable is %s_%d.

upf_extension

Sets the variable to false to disable writing of UPF extension commands in save_upf.

Default value for this variable is true.

use_port_name_for_oscs

Specifies that when off-sheet connectors for nets also have ports on them, they are given the name of the port.

Default value for this variable is false.

verbose_messages

Causes more explicit system messages to be displayed during the current Design Analyzer dc_shell session.

Default value for this variable is true.

verilogout_equation

Writes Verilog "assign" statements (Boolean equations) for combinational gates, rather than gate instantiations.

Default value for this variable is false.

verilogout_higher_designs_first

Writes Verilog "modules" so that the higher level designs come before lower level designs, as defined by the design hierarchy.

Default value for this variable is false.

verilogout_ignore_case

Instructs the compiler not to consider case when comparing identifiers to Verilog reserved words.

Default value for this variable is false.

verilogout_include_files

Specifies to the write -f verilog command to write an include statement that will have the name of the value you set for this variable.

Default value for this variable is "".

verilogout_no_tri

Declares three-state nets as Verilog "wire" instead of "tri." This variable is useful in eliminating "assign" primitives and "tran" gates in the Verilog output.

Default value for this variable is false.

verilogout_show_unconnected_pins

Instructs the Verilog writer in dc_shell to write out all of the unconnected instance pins, when connecting module ports by name. For example, modb b1 (.A(in),.Q(out),.Qn()).

Default value for this variable is false.

verilogout_single_bit

Instructs the compiler not to output vectored ports in the Verilog output. All vectors are written as single bits.

Default value for this variable is false.

verilogout_unconnected_prefix

Instructs the Verilog writer in dc_shell to use the name SYNOPSYS_UNCONNECTED_ to create unconnected wire names. The general form of the name is SYNOPSYS_UNCONNECTED_%d.

Default value for this variable is SYNOPSYS_UNCONNECTED_.

write_name_nets_same_as_ports

Specifies to the tool that nets are to receive the same names as the ports the nets are connected to.

Default value for this variable is false.

write_sdc_output_lumped_net_capacitance

Determines whether or not the write_sdc command outputs net loads.

Default value for this variable is true.

write_sdc_output_net_resistance

Determines whether or not the write_sdc command outputs net resistance.

Default value for this variable is true.