蘇柏丞 Fossum Su

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https://github.com/Fossum2523

SKILLS

Programming Language

- Verilog (10 / 10)
- C (10 / 10)
- Python (8 / 10)
- Assembly Language (6 / 10)

English Ability

- TOEIC 675

TOOLBOX

- Design Compiler (5 / 10)
- IC Compiler (5 / 10)
- Vivado (7 / 10)
- VCS (6 / 10)
- Verdi (6 / 10)
- NC-Verilog (5 / 10)

CERTIFICATIONS

- TSRI Logic Synthesis with **Design Compiler**
- TSRI Cell-Based IC Physical Design and Verification with **IC Compiler**

EDUCATION

Masters of Electronic Engineering

National Taiwan University of Science and Technology | 2023/09-now

Bachelor of Electronic Engineering

National Taiwan University of Science and Technology | 2019/09-2023/06

COURSES

- FPGA System Design (A+)
- VLSI Systems Design (A+)
- SOC Design Laboratory (A+)
- Advanced Computer Algorithms (A-)
- Advanced Digital Signal Processing (A+)

LEARNING EXPERIENCE

- Thesis - Design and Implementation of a **Hardware Accelerator IP** for Post-Quantum Cryptography **ML-DSA** Compatible with the **AXI-4** Interface
- Design and Implementation of an IP for Synchronous **AES-128 Encryption(TSRI Educational Chip)**
- Design and Implementation of **FFT Based-on Cordic**(**TSRI Educational Chip**)
- Implementaion of Embodied **Recognition Blood Pressure Monitor Based-on ECG**
- Implementation of **16-bit RISC Computer**
- Design and Implementation of **Hardware Accelerator and UART Based-on Caravel SOC**
- **IC Contest 2024**