```
1   /*
2      Bus is the central data transfer mechanism.
3      The read and write ports of each registers are interfaced to the bus.
4      Data placed on the bus is chosen according to control signals respective to each register.
5
6      PHASE 2 EDIT:
7      32-bit vector C_in was added to the input sensitivity list, paired with Cout, its
   corresponding control signal.
8      When C_in is high, the sign-extended immediate value from the IR is placed on the bus.
9   */
10
11  module Bus (
12     // data-out from each register.
13     input [31:0] R0R15_in, // IN refers to the perspective of the Bus
14     input [31:0] HI_in,
15     input [31:0] LO_in,
16     input [31:0] ZHI_in,
17     input [31:0] ZLO_in,
18     input [31:0] PC_in,
19     input [31:0] MDR_in,
20     input [31:0] INPORT_in,
21     input [31:0] C_in,      // C_in for Phase 2
22
23     input R0R15_out, HI_out, LO_out, ZHI_out, ZLO_out, PC_out, MDR_out, INPORT_out, C_out,
   // C_out for Phase 2
24
25     // data-out from the bus
26     output wire [31:0] BusMuxOut
27  );
28
29     reg [31:0] q;
30
31     // Selecting the data to be place on the data lines according to respective control
   signals.
32     always @ (*) begin
33
34        if       (R0R15_out)    q = R0R15_in;
35        else if  (HI_out)       q = HI_in;
36        else if  (LO_out)       q = LO_in;
37        else if  (ZHI_out)      q = ZHI_in;
38        else if  (ZLO_out)      q = ZLO_in;
39        else if  (PC_out)       q = PC_in;
40        else if  (MDR_out)      q = MDR_in;
41        else if  (INPORT_out)   q = INPORT_in;
42        else if  (C_out)        q = C_in;
43        else                    q = 32'b0;
44
45     end
46
47     assign BusMuxOut = q;
48
49  endmodule
50
```