```
// 32-bit adder with 2 adder\_16b instances. This module represents the top-level entity
                     used in the ALU for the ADD and SUB operations.
    3
                     module adder_32b (
                                  input cin, // carry-in (used for subtraction)
input [31:0] x, y, // Summands
output cout, // carry-out (not used in ALU due to fixed register size in reg_file)
output [31:0] s // Result (wire)
   67
    8
   9
10
11
                                   // carry-in signal for each 16-bit sub-adder. We use 'h' to denote a 'hierarchical' carry.
                                  wire [2:0] hc;
12
13
                                   assign hc[0] = cin;
14
15
                                   // 'hierachical' Generate and Propagate signals.
 16
                                   wire [1:0] hP, hG;
17
18
                                   // 2 adder_16b instances, each for a given 16-bit subset of x and y.
19
                                   genvar i;
20
                                   generate
21
                                   for (i=0; i<2; i = i+1) begin : subadders
22
                                               adder_16b subadder (hc[i], x[16*i+15: 16*i], y[16*i+15: 16*i], hP[i], hG[i], s[16*i+15
                      : 16*i]);
23
                                   end
24
                                   endgenerate
25
26
27
                                   // Hierarchical carries according to the lookahead framework.
                                  assign hc[1] = hG[0] \mid hP[0] \& cin;
assign hc[2] = hG[1] \mid hP[1] \& hG[0] \mid hP[1] \& hP[0] \& cin;
28
29
                                   assign cout = hc[2];
30
 31
                     endmodule
32
33
                      //-----Testbench-----//
34
35
                     module adder_32b_testbench();
36
37
                                   reg cin;
reg [31:0] x, y;
38
39
                                  wire cout;
40
                                  wire [31:0] s;
41
42
                                   // Design under test.
43
                                   adder_32b dut (cin, x, y, cout, s);
44
45
                                   // 6 edge-cases are validated for testbench concision.
46
                                   initial begin
                                               47
48
                      32'b00000000000000000000000000001011; #10;
49
                                               sigma = 1: cin = 8b, x = 8b, y = 8b, s = 8b, cout = 8b, cin, x, y, s, cout;
50
                      51
52
53
54
55
                                                // Test 3: Maximum 32-bit values (check carry-out well handled)
56
                                                32'b1111111111111111111111111111111; #10;
                                                sigma = 10^{\circ} \sin x + \sin x = 10^{\circ} \sin x = 10
 58
                                               59
60
                      32'b000000000000000000000000000000001; #10;
                                               sigma = sigm
61
62
                      // Test 5: Large values, no carry-out cin = 0; x = 32'b11110000111100001111000011110000; y = 32'b000011110000111100001111; #10;
63
64
                                               sigma = sigm
65
66
67
                                                // Test 6: zero inputs
68
                                                cin = 0; x = 32'b0; y = 32'b0; #10;
```

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