```
1   /*
2      Bus is the central data transfer mechanism.
3      The read and write ports of each registers are interfaced to the bus.
4      Data placed on the bus is chosen according to control signals respective to each register.
5   */
6
7   module Bus (
8      // data-out from each register.
9      input [31:0] R0R15_in, // IN refers to the perspective of the Bus
10     input [31:0] HI_in,
11     input [31:0] LO_in,
12     input [31:0] ZHI_in,
13     input [31:0] ZLO_in,
14     input [31:0] PC_in,
15     input [31:0] MDR_in,
16     input [31:0] INPORT_in,
17     input [31:0] C_in,      //Added C for Phase 2
18
19     input R0R15_out, HI_out, LO_out, ZHI_out, ZLO_out, PC_out, MDR_out, INPORT_out, C_out,
20
21     // data-out from the bus
22     output wire [31:0] BusMuxOut
23  );
24
25     reg [31:0] q;
26
27     // Selecting the data to be place on the data lines according to respective control
       signals.
28     always @ (*) begin
29
30        if       (R0R15_out)    q = R0R15_in;
31        else if  (HI_out)       q = HI_in;
32        else if  (LO_out)       q = LO_in;
33        else if  (ZHI_out)      q = ZHI_in;
34        else if  (ZLO_out)      q = ZLO_in;
35        else if  (PC_out)       q = PC_in;
36        else if  (MDR_out)      q = MDR_in;
37        else if  (INPORT_out)   q = INPORT_in;
38        else if  (C_out)        q = C_in;
39        else                    q = 32'b0;
40
41     end
42
43     assign BusMuxOut = q;
44
45  endmodule
46
```