```
1   /*
2      register.v is the modular register entity used as a template for all internal Datapath
    registers,
3      including PC, IR, Z, Y, MAR, MDR, HI, LO.
4
5      Clarification: BusMuxOut refers to the data fed to the *input* of the register,
6      while BusMuxIn regers to the data *outputted* by the register.
7      In/Out therefore refers to I/O from the Bus' perspective.
8   */
9
10  module register #(
11        parameter DATA_WIDTH_IN = 32, DATA_WIDTH_OUT = 32, INIT = 32'b0
12        )(
13        input clear, clock, enable,
14        input [DATA_WIDTH_IN-1:0] BusMuxOut,
15        output wire [DATA_WIDTH_OUT-1:0] BusMuxIn
16     );
17
18     // Internal synchronous register.
19     reg [DATA_WIDTH_IN-1:0] q;
20
21     // Initialize Q with default value.
22     initial q = INIT;
23
24     always @ (posedge clock) begin
25        if (clear)
26           q <= {DATA_WIDTH_IN{1'b0}};
27        else if (enable)
28           q <= BusMuxOut;
29     end
30
31     assign BusMuxIn = q[DATA_WIDTH_OUT-1:0];
32
33  endmodule
34
35
```