```
1   /*
2      multiplier_32b is a 32-bit multiplier leveraging both optimization structures: bit-pair
    recoding and carry-save addition.
3      It accepts M and Q as the multiplication and multiplier, respectively.
4   */
5
6
7   module multiplier_32b (
8      input [31:0] M, Q,
9      output [63:0] result
10     );
11
12     // All relevant variations of M for booth augend selection.
13     wire [32:0] Q_shifted = {Q, 1'b0}; // Left shifted Q by 1 such that the i-1 Booth check
    is valid with i = 0.
14     wire [31:0] negM = -M;
15     wire [32:0] Mx2 = {M, 1'b0};
16     wire [32:0] negMx2 = {negM, 1'b0};
17
18     // Augends.
19     reg [63:0] partial_products [15:0];
20
21     integer i;
22     // Perform Booth Augend Selection
23     always @(*) begin
24        for (i = 0; i < 31; i = i+2) begin
25           // Choose variant of M based on partial_products
26           case ({Q_shifted[i+2], Q_shifted[i+1], Q_shifted[i]})
27
28              // All values are properly sign-extended.
29              3'b000: partial_products[i>>1] = 64'b0; // 0 x M
30              3'b001: partial_products[i>>1] = {{32{M[31]}}, M}; // +1 x M
31              3'b010: partial_products[i>>1] = {{32{M[31]}}, M}; // +1 x M
32              3'b011: partial_products[i>>1] = {{31{Mx2[32]}}, Mx2}; // +2 x M
33              3'b100: partial_products[i>>1] = {{31{negMx2[32]}}, negMx2}; // -2 x M
34              3'b101: partial_products[i>>1] = {{32{negM[31]}}, negM}; // -1 x M
35              3'b110: partial_products[i>>1] = {{32{negM[31]}}, negM}; // -1 x M
36              3'b111: partial_products[i>>1] = 64'b0; // 0 x M
37              default: partial_products[i>>1] = 64'b0;
38           endcase
39           // Apply appropriate shift before addition.
40           partial_products[i>>1] = partial_products[i>>1] << i;
41        end
42     end
43
44     // Final operands after reduction process
45     wire [63:0] reduced1, reduced2;
46
47     // 16-to-2 CSA reducer.
48     CSA_tree_16to2 reduction (.augends(partial_products), .reduced1(reduced1), .reduced2(
    reduced2));
49
50     // Final carry-propagate stage, with no carry-in, nor carry-out (result for 32-bit mult.
    is 64-bits)
51     adder_64b carry_propagate (.cin(1'b0), .x(reduced1), .y(reduced2), .s(result)); // No
    cout.
52
53  endmodule
54
55
56  `timescale 1ns / 1ps
57
58  module multiplier_32b_tb;
59      reg signed [31:0] M, Q;
60      wire signed [63:0] result;
61
62      // Instantiate the multiplier
63      multiplier_32b dut (M, Q, result);
64
65     initial begin
66         run_test(32'd0, 32'd0, 32'd0);                    // 0 * 0 = 0
67         run_test(32'd15, 32'd10, 32'd150);                // 15 * 10 = 150
68         run_test(-32'd15, 32'd10, -32'd150);              // -15 * 10 = -150
69         run_test(32'd15, -32'd10, -32'd150);              // 15 * -10 = -150
70         run_test(-32'd15, -32'd10, 32'd150);              // -15 * -10 = 150
71         run_test(32'h7FFFFFFF, 32'd1, 32'h7FFFFFFF);      // Largest positive * 1
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72          run_test(32'h80000000, 32'd1, 32'h80000000);     // Smallest negative * 1
73          run_test(32'hFFFFFFFF, 32'hFFFFFFFF, 32'd1);     // -1 * -1 = 1
74
75          $display("Testbench completed successfully" );
76
77          $stop;
78      end
79
80      task run_test(input signed [31:0] M_in, input signed [31:0] Q_in, input signed [31:0]
    expected_result);
81          begin
82              M = M_in;
83              Q = Q_in;
84              #10; // Wait for computation
85
86              if (result !== expected_result) begin
87                  $display("Test Failed: M=%d, Q=%d -> Expected Result=%d but got Result=%d"  ,
88                           M_in, Q_in, expected_result, result);
89              end
90          end
91      endtask
92
93  endmodule
94
95
```