```
1   /*
2      Ram block implements a modular sized RAM block with a syncronous write and asyncronous
    read
3      Depth and Width parameters can be used to change the capacity and word size respectively
4
5      Design Issue
6      Due to limitation the group faced with readmemh an Absolute path must be used to the
    ram.txt file
7      This must be Changed on every device that runs the project
8   */
9
10
11  module ram #(
12     // for modularity
13     parameter depth = 9,
14     parameter width = 32
15     )(
16     input clk, wr_en,
17     input [depth-1:0] r_addr, w_addr,
18     input [width-1:0] w_data,
19     output [width-1:0] r_data
20     );
21
22     // Internal memory array consisting of 2^depth, width-lengthed registers.
23     // This definition enforces a right-to-left increasing bit significance, and an
    up-to-down addressing scheme.
24     reg [width-1:0] memory_array [0:2**depth-1];
25
26     initial $readmemh(
    "C:/Users/foste/Documents/3rd_Year_24-25/ELEC374/ELEC374_MINI_SRC/ram.txt", memory_array);
27
28     // r_data1/2 are immediately available as r_addr1/2 is presented to the RF
29     // Two read addresses are supported by the register file should we choose to implement a
    3-bus design in later phases.
30     assign r_data = memory_array[r_addr];
31
32     // Data writes are synchronous to clk with wr_en high.
33     always @(posedge clk) begin
34        if (wr_en) memory_array[w_addr] <= w_data;
35     end
36
37  endmodule
38
```