```
 1
 2   module mini_src_group_1 (
 3      input clk, reset, stop,
 4      input [31:0] INPORTin,
 5      output [31:0] OUTPORTout,
 6      output run
 7      );
 8
 9      // Program Execution Control
10      wire clr, CONin, CON, RAM_wr;
11      wire [31:27] IRop;
12
13      // General Purpose Register Control
14      wire Gra, Grb, Grc, Rin, Rout, BAout;
15
16      // Datapath Register Control
17      wire [15:0] DPin, DPout;
18
19      // ALU Control
20
21      wire [15:0] ALUopp;
22
23
24      DataPath DP (clk, clr, CONin, Gra, Grb, Grc, Rin, Rout, BAout, RAM_wr, DPin, DPout,
    ALUopp, INPORTin, OUTPORTout, IRop, CON);
25
26      Control ctrl (reset, stop, clk, CON, IRop, clr, CONin, RAM_wr, Gra, Grb, Grc, Rin, Rout,
    BAout, DPin, DPout, ALUopp, run);
27
28   endmodule
29
30   `timescale 1ns/1ps
31
32   module tl_testbench();
33      reg clk, reset, stop;
34      reg [31:0] INPORTin;
35      wire [31:0] OUTPORTout;
36      wire run;
37
38      mini_src_group_1 uut (clk, reset, stop, INPORTin, OUTPORTout, run);
39
40      initial begin
41         clk <= 0;
42         forever #5 clk <= ~clk;
43      end
44
45      initial begin
46         reset <= 1;
47         @(posedge clk);
48         @(posedge clk);
49
50         reset <= 0;
51
52         while(1) begin
53            @(posedge clk);
54            if(!run) $stop;
55         end
56
57      end
58
59   endmodule
60
```