```
1   /*
2      Modular 2^depth x width memory array with 1 read port and 1 write port.
3      Read port accesses r_data according to address r_addr asynchronously.
4      The single write port writes w_data to address w_addr synchronously.
5   */
6
7
8   module ram #(
9      // for modularity
10     parameter depth = 9,
11     parameter width = 32
12     )(
13     input clk, wr_en,
14     input [depth-1:0] r_addr, w_addr,
15     input [width-1:0] w_data,
16     output [width-1:0] r_data
17     );
18
19     // Internal memory array consisting of 2^depth, width-lengthed registers.
20     // This definition enforces a right-to-left increasing bit significance, and an
   up-to-down addressing scheme.
21     reg [width-1:0] memory_array [0:2**depth-1];
22
23
24     // DESIGN LIMITATION: an absolute path is required to read the contents of ram.txt,
   which needs to be changed based on the device.
25     initial $readmemh("C:/Users/21fje/Desktop/ELEC374_MINI_SRC/ram.txt" , memory_array);
26
27     // r_data is immediately available as r_addr is presented to the RF (asynchronous)
28     assign r_data = memory_array[r_addr];
29
30     // Data writes are synchronous to clk with wr_en high.
31     always @(posedge clk) begin
32        if (wr_en) memory_array[w_addr] <= w_data;
33     end
34
35  endmodule
36
```