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         register.v is the modular register entity used as a template for all internal Datapath
     registers,
 3
         including PC, IR, Z, Y, MAR, MDR, HI, LO.
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         Clarification: BusMuxOut refers to the data fed to the *input* of the register,
         while BusMuxIn regers to the data *outputted* by the register.
         In/Out therefore refers to I/O from the Bus' perspective.
è
10
     module register #(
11
            parameter DATA_WIDTH_IN = 32, DATA_WIDTH_OUT = 32, INIT = 32'b0
12
            input clear, clock, enable,
input [DATA_WIDTH_IN-1:0] BusMuxOut,
13
14
15
            output wire [DATA_WIDTH_OUT-1:0] BusMuxIn
16
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18
         // Internal synchronous register.
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30
         reg [DATA_WIDTH_IN-1:0] q;
         // Initialize Q with default value.
         initial q = INIT;
         always @ (posedge clock) begin
            if (clear)
            q <= {DATA_WIDTH_IN{1'b0}};
else if (enable)</pre>
                q <= BusMuxOut;</pre>
         end
         assign BusMuxIn = q[DATA_WIDTH_OUT-1:0];
33
     endmodule
34
```