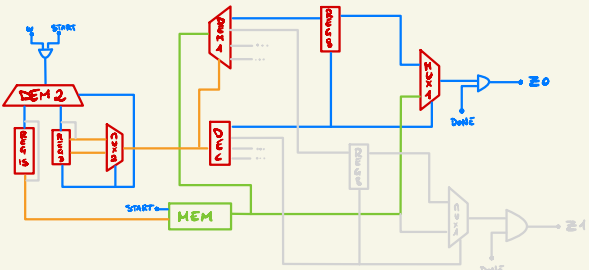
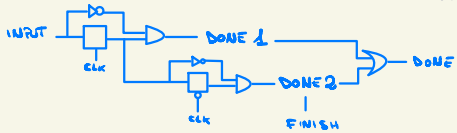
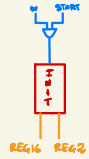
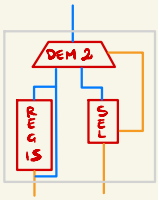
Progetto Reti Logiche



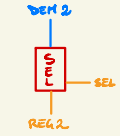


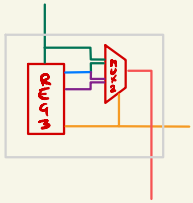
INIT



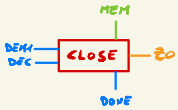


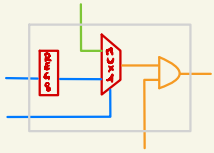
SEL



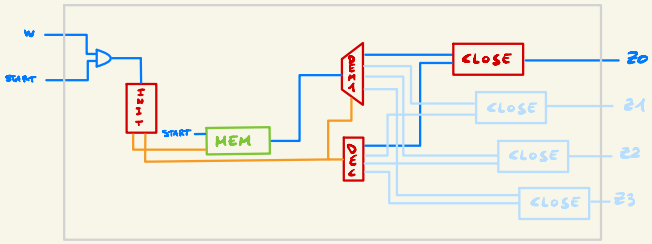


CLOSE





MEM ACCESS



WNS da 86.008 a 3.32 ns

REG 15

RESET = FINISH OR RST
ENABLE = 1

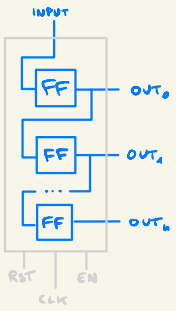
REG 3 RST → "100"

RESET = FINISH OR RST
ENABLE = RST OR (START AND NOT SEL)

REG 8

RESET = RST
ENABLE = RST OR (DONE AND DEC)

SIPO



PIPO