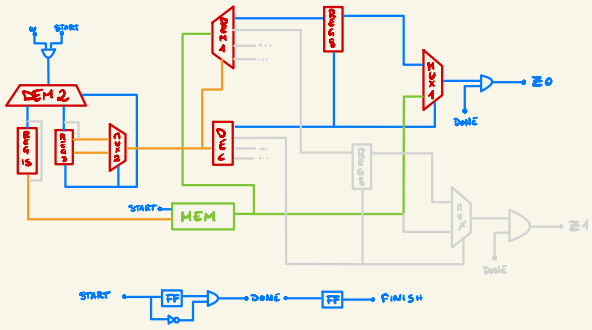
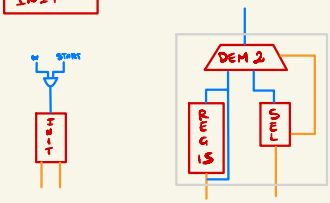
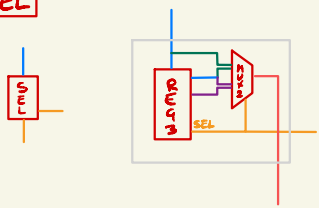
Progetto Reti Logiche



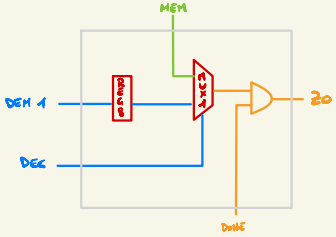
INIT



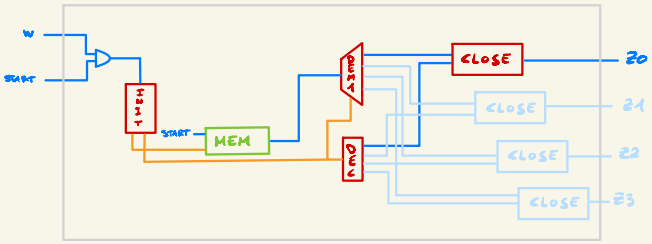
SEL



CLOSE



MEM ACCESS



REG 15

RESET = FINISH OR RST

ENABLE = 1

REG 3 RST → "100"

RESET = FINISH OR RST

ENABLE = RST OR (START AND NOT SEL)

REG 8

RESET = RST

ENABLE = RST OR (DONE AND DEC)