# Temporal Computing

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**Abstract**

This report consists of a review of the literature and a plan for integration related to **temporal computing**, a novel method of computation that uses time intervals as the primary method of storing and manipulating data. The literature review covers a broad range of methods which implement both computation and communication. The plan of further work focuses on assessing the a novel temporally inspired digital implementation of dot product, and a broader more theoretical work on the fundamental building blocks of temporal computing methods.

## 1 Introduction

The ability to perform accurate repetitive computation has been central to numerous scientific and technological advances in the last seventy years. At the heart of this is Moore's Law [41], which states that computational power provided by the silicon based Central Processing Units (CPUs) will double year-on-year for the foreseeable future. Unfortunately, several factors have compounded to make this less likely to continue: heat dissipation, atomic and quantum effects provide practical limits to the miniaturisation and packing of transistors [12], and the limited bandwidth between CPU and memory limits computation speed (the von-Neumann bottleneck [2]). There is also doubt about fabrication processes working below 3nm, although many vendors are issuing in even more miniaturisation which they refer to as the angstrom era (see Figure 1).

At the same time, methods of data processing using learning systems have become significant new architectural components. Of these, Deep Learning (DL) [29] has provided best-in-class performance on many machine learning tasks, and revitalised many areas of pattern recognition, opening up a revolution in new services that were traditionally performed using human intensive processes. Moreover, these methods are not well supported by traditional computer architectures [27] as they require massive parallelism, similarly to the brain. Graphics Processing Units (GPUs) , initially built for video games, have been successfully utilised, but still suffer from high levels of inefficiencies which are many orders of magnitude away from biological systems in energy and ability.

Given this impasse, there is a need to look more broadly at the problem of improving the efficiency **and** accelerating computation. This has resulted in a

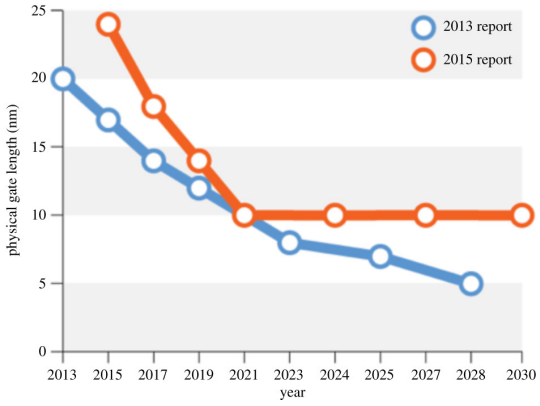


Figure 1: Predicted physical gate size decline over the next five years. Credit: `https://doi.org/10.1098/rsta.2019.0061/`

"Cambrian explosion" [25] of new approaches, and this research focuses on one of these, **temporal computing**.

This new approach represents numbers with a unary encoding (discussed in more detail in Section 3) instead of binary, and uses *time delays* to represent data instead of digital bit manipulation. We are drawn to this area for several reasons.

1. There is a precedence in nature, the human brain uses spike-based information as the main processing encoding [60].

2. Unary is more simplistic than binary to compute with. Tools such as the abacus are among the earliest calculators [44].

3. On the surface, time appears to be a free resource. For a typically coded temporal interval, the is only ever a requirement for two delimiting spikes (See Figure 2 ) [52].

The three capabilities detailed above provide a broad definition of an area of research, but this is yet to be established in the mainstream. Four areas: racelogic, unary processing, oscillatory Computing and neuromorphic compute, utilise time as a medium but do so without explicitly exploiting the above features. This is particularly the case with two areas under review, neuromorphic and oscillatory computing, with methods in these areas often conflating the benefits of hardware and problem specific algorithmic approaches.

The problem of defining temporal computing is further compounded by misuse of the term "stochastic" eg in works [63, 62], and significant oversight in not including previous work from the late sixties on unary compute [44], in discussions.

With this in mind, the agenda of this report is:

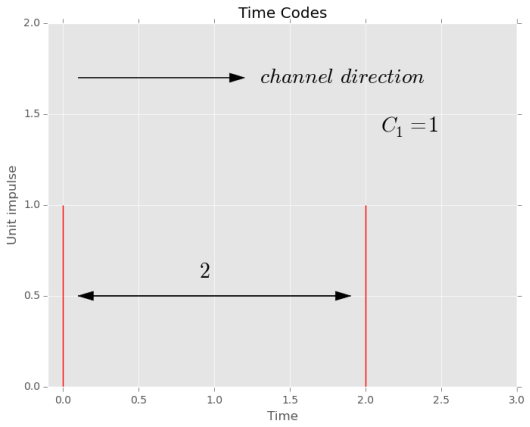


Figure 2: A typical value can be represented as two delimiting spikes.

- To cover all research specifically referenced as "temporal" by the racelogic community (section 2).
- To also include older work on Unary computing including work referred to as temporal/unary but which also could be defined as stochastic. (section 3).
- To also include communication methods that use similar interval encodings and have processing approaches that may be repurposed to compute (Section 4).
- For completeness, include both oscillatory and neuromorphic computing in the discussion (Sections 5 and 6)

This nicely sets the agenda for future work which we define as a mission with a plan and milestones (See separate planning document).

# 2 Racelogic

Racelogic is undoubtedly the most significant area of research in the temporal domain, both computation and memory, and has formed a small community in the US [34].

The central theme of this work is the utilisation of the two timing properties of traditional logic gates. Under a temporal scheme an `AND` gate acts as a `MAX` operation, and the `OR` gate acts as a `MIN` operation (see Figure 3).

Using this a variety of systems have been proposed and implemented [34], most notably to perform minimum and maximum path search on a graph [35].

This work has been extended to utilise a tropical algebra [33] a semi-ring that implements multiplication and addition, and this was referred to as a Temporal

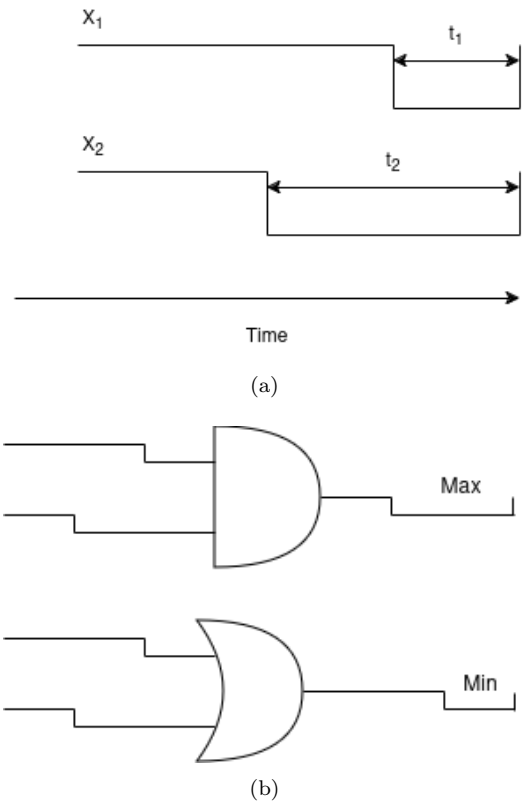


Figure 3: A visual explanation of racelogic. The first diagram shows the representation and second gives the "race" min/max effect

State Machine. Under this scheme various additional graph algorithms including Dikstra's were implemented and benchmarked.

Further work by this group also involved building temporal memories called *Racetracks* [59, 36]. The basis of this is akin to dragging a bucket for a set distance, the time to do this becomes fixed for a set bucket size (see Figure 4). In this work this is implemented on a magnetic platform, with the addition of a recovery track to reset the memory. This is the first known implementation of memory and the "dragging time" approach seems to be something that could be readily applied in many resistive physical mediums.

The logic gate processing format has also been explored by two further parties, in the context of superconducting mediums [57] [58] [56] [61] [51] also as a formulation for a specific supporting algebra. The superconducting work follows a similar pattern and is limited to a constrained view of logic operations applied to temporally organised inputs. This work is excellent proof-of-concept work, but lacks reference to comparable digital algorithms and the nature of space/time trade-offs.

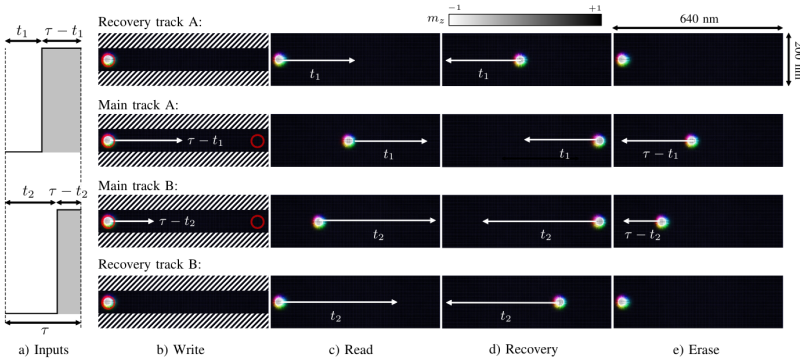


Figure 4: The racetrack memory operations. Taken from [59]

# 3 Unary Computation

Unary number systems ([31] Chapter 7 page 133) were amongst the earliest numerical representations of quantity, with the abacus existing as the earliest calculating device [44]. Unary codes are a simplification, with either binary digit acting as the delimiter. Table 1 gives a breakdown of how unary codes are constructed for the first few decimal numbers. We introduce a further code Discrete Pulse Interval Modulation (DPIM), which is a form of unary code, and is used in the communication community and is discussed in Section 4.

| **Decimal** | Unary (U) | Unary code (UC) | DPIM |
|---|---|---|---|
| **0** | | (0) may delimit | (11) may delimit |
| **1** | 1 | 1 | 101 |
| **2** | 11 | 10 | 1001 |
| **3** | 111 | 100 | 10001 |

Table 1: Coding Schemes related to Temporal Computing

One of the key benefits for all the unary family is that simple arithmetic is easily derived: Addition with unary, as with the abacus, is performed trivially using simple concatenation [17].

Integer multiplication of unary codes is performed by dilating the first unary code by the size of the second code. In a fully clock based architecture this can be performed by changing the relative clock speeds of the sender and receiver of the signal (see [17] section 3.3 for a more detailed explanation) Again, this is a simple operation which requires only basic logic to perform.

The review paper of Poppelbaum [44] explains in some detail first-generation unary computers. There are three types of unary processing: stochastic, burst and pulse gear based approaches. These systems can be summarised as follows:

**Stochastic** where the unary value represents a discrete probabilistic range, sometimes with randomness incorporated. Many machines have been built with this premise, including **RASCEL** [19] **POSTCOMP** [43]. This continues to be an active field of research [1].

**Burst** This is more akin to traditional unary but with a specific bit-width, so for instance 7 out of 10 bits set (`1111111000`) would equal 7. Examples of it's use are **BURST** [44] and **WALSHSTORE** [5].

**Pulse Gear** This again uses burst unary but provides a clever method for shifting and ANDing to perform operations. An example of this is the **UNIFIELD** processor [16].

These largely forgotten systems are all very interesting applications of unary and could be utilised in the design of new processing elements, the Pulse Gear methods, and the use of AND gates and counters have some resonance with methods discussed later in this review.

Two further points should be noted. Firstly, none of these systems use the benefits of redundancy and the delimiting nature of unary codes and are firmly wedded to using many boolean `on` (`1`'s) values. Secondly they are explicitly non-temporal, this means that time is not used to represent data.

More modern work in this area has been performed by Wu [63] [42] [64]. This work is again mainly unary and again not explicitly temporal.

## 3.1 Multiplexed Unary

**Unary codes** have an additional property that a set of non-duplicate values can be efficiently multiplexed. Again to use the abacus analogy, if we have beads of two colours: black (1) and white (0), provided there is no duplication, multiplexing can occur which *reuses white beads*. Again, the logic of this is a simple `OR`ing of the value from a start reference bit. Figure 5 presents this graphically. This system is *genuinely* multiplexing; the two values are overlaid so the values actually forms part of the subsequent data. This is unique to this coding strategy and is unlike any other system of multiplexing. The general algorithm for conversion to this multiplexed domain is as follows:

```
1 for each value I in C do
2 |  At position I in MUX window append 1;
3 end
```

**Algorithm 1:** Encoding Algorithm

Once transformed, signals can be interleaved in such a way that they can be easily recovered. To de-multiplex, the process is reversed, with the MUX channel progressively reconstructs the input values back into separate channels.

A natural extension is to enable the unary coded 1 value to be multi-valent. Although at first this may appear contrived, the motivation for this is the extension of the multiplexing method to incorporate duplicates, and the ability

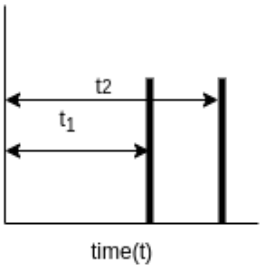


Figure 5: An example of genuine multiplexing

```
1 for 0..I do
2 |  if 1 then
3 |  |  Write I into output channel;
4 |  end
5 end
```

**Algorithm 2:** Decoding Algorithm for DMU

to better encode analog interval channels. This channel also has an additional property that multiplication can be performed, at least within the bounds of the notation, by placing a value $a$ at position $t$, and *also* multiplexing as in Figure 6.

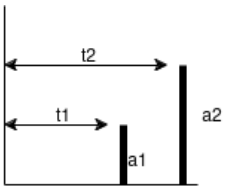


Figure 6: Multi-valent multiplexing for a potential analog implementation

Although not immediately obvious, an uncertainty relationship exists between position and data when "dense" multiplexing is used. To illustrate this let us take the trivial sequence (1,3,2) with knowledge of the prior this could be easily transformed into the densely multiplexed representation of (111) [1] which notionally can be represented with a smaller number of bits, but with a loss of order in the data. Adding positional values via a positional index recovers from the problem but at the cost of extra data, with a different prior distribution.

Clearly, the act of multiplication can be transformed into manipulating the values held in the buckets. This can be easily extended to a dot-product operation and the representation of tuple pairs is somewhat compressive since one

[1] 1=1,2=01,3=001

element of the 2-tuple is specified by a positional index.

Under a simple scheme, tuples can be added arbitrarily to the array at their $t$ index point. A dot product on this multiplexed array can be evaluated efficiently and in a systolic way using the **Multiplicative ADD** (MADD) algorithm (Algorithm 3) as shown in [18]. Figure 7 demonstrates that the algorithm is effectively finding the area of the rectangles $4 \times 10$ and $4 \times 4$ by progressively sweeping in one pass back across the indexed array, counting initially the first $6 \times 4$ and then the remaining $8 \times 4$.

```
1 acc, height ← 0;
2 i ← |mem| − 1;
3 while i > 0 do
4 |   height ← height + mem[i];
5 |   acc ← acc + height;
6 |   i ← i − 1;
7 end
8 return acc
```

**Algorithm 3:** The MADD algorithm

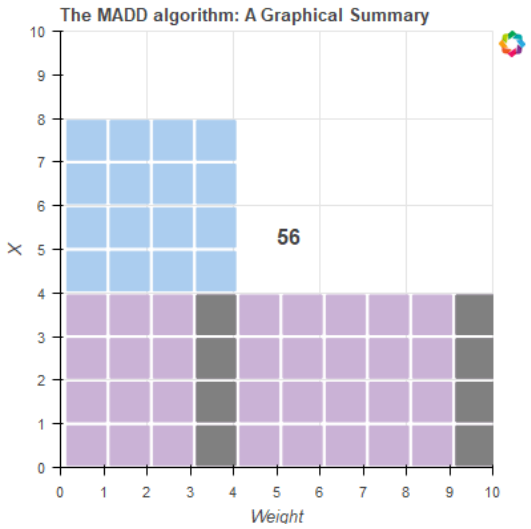


Figure 7: MADD: A description based on a goemetric view of the MADD algorithm. Here we perform the operation $(4 \times 10) + (4 \times 4)$ right to left by accumulating the "height" at the index point

The MADD algorithm originated from the use of discrete memory indexes as a simulation of time delays. As such the MADD algorithm is inspired by the temporal approach, but, its representation does not use time delays directly as

the storage medium. Appendix **??** discusses an extension to this method, called Delta MADD.

# 4 Temporal/Unary for Communication

Interval codes have been exploited in the communication community in the form of DPIM [11], where the pulses delimit both the beginning and end of the encoded value. This method was heavily researched from the late sixties onwards [39] [28] [48] and revisited by the optical community during the nineties [24] [23]. The scheme is very simple, and efficient in terms of the sparsity of the representation, with two spikes being able to represent any magnitude.

There are several further compelling advantages:

**Bandwidth Efficiency** DPIM is more bandwidth-efficient than some other modulation schemes. This is because it doesn't require changes in amplitude or pulse width, which can demand more bandwidth.

**Power Efficiency** Since DPIM doesn't rely on varying amplitude, it can be more power-efficient. Ghassemlooy states:

> For the same packet error performance, 4-bit DPIM has about a 5dB power advantage over OOK, but requires approximately 1dB more power than 4-bit PPM [23].

OOK is traditional bit encoding and PPM is Pulse Position Modulation (the same as DPIM but with a constant bit-width, hence pulses are not self-delimiting).

**Suitability for Optical Communication** DPIM is often used in optical communication systems because it can be implemented as light pulses.

**Simplicity** The circuitry for DPIM can be simpler than other modulation schemes, as it only needs to control the timing of pulses.

However, there has been a lack of adoption based on the following disadvantages:

**Synchronization Complexity** One of the main challenges of DPIM is the requirement for precise synchronization between the transmitter and receiver. As with all temporal systems encoding and decoding require a very stable and accurate clock, which can add complexity and cost to the system.

**Limited Data Rate** While DPIM can accommodate variable data rates, the practical data rate might be limited by the precision of the timing measurements.

**Error Propagation** In some implementations of DPIM, errors in detecting one pulse interval can propagate and affect the detection of subsequent intervals.

One point to note that affects how we might process temporal intervals in a computational setting is the use of ramp functions [48]. A **ramp function**, also known as a saw-tooth wave or ramp waveform, is a type of signal where the voltage or current increases linearly with time, then abruptly drops back to its starting value, and repeats this cycle periodically. Figure 8 gives a typical view of communication system using ramp functions to DPIM encoded data.

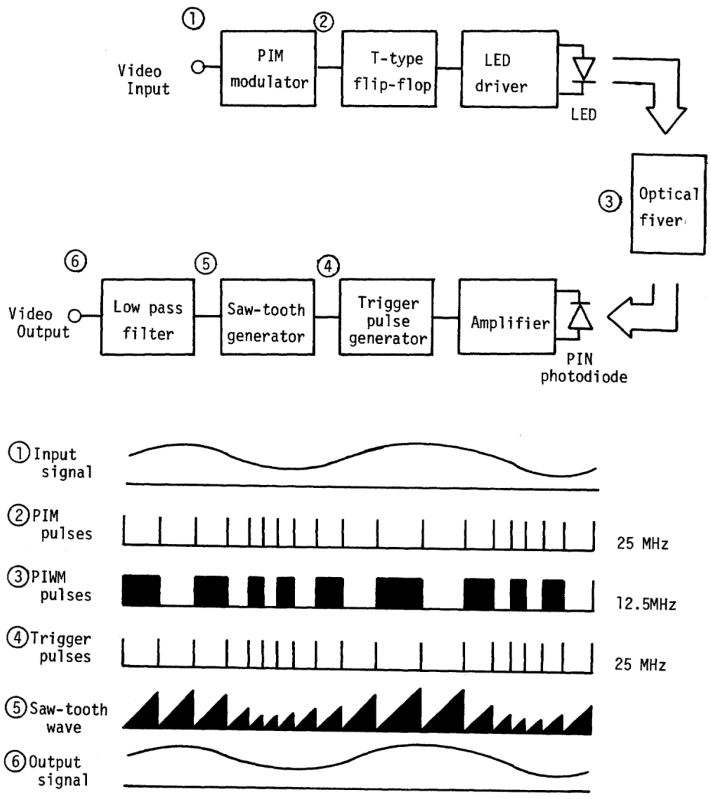


Figure 8: A communication system using ramps to encode and decode data. Taken from [48]

DPIM has served as inspiration for many studies of neural information encoding in Neuroscience [40] [46] [4], Mackay's work [32] focused on the channel capacity of this simple model, and surprisingly they find that for a suitable set of

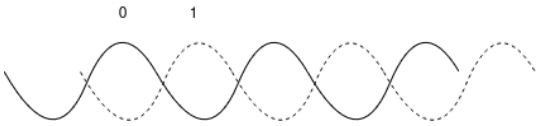


Figure 9: An example of how phase might encode a signal, in this case binary 0 and 1

constraints, time encoding outperforms single bit based information encoding.

# 5 Oscillatory Systems

An oscillatory computer utilises the dynamics of time-based coupled oscillators to perform computation.

Coupled Oscillators are a technique in non-linear dynamics that produce stable and predictable patterns of oscillation from the ensemble behaviours of many oscillators [53]. The classic example of this is the firefly synchronisation problem [6] where fireflies in a forest synchronise their flashing patterns.

Unlike traditional computers, oscillatory computers encode and process information using the phase, frequency, or amplitude of oscillations. This approach is inspired by the observation that many biological systems, including the brain, use oscillatory dynamics for information processing and communication. For a review article and example see [10] and [9]. Example systems include [38] [14] [15] [8] [20] [37].

The advantages of oscillatory computers include:

- Parallelism through the emerging dynamics of coupling.
- Energy Efficiency as they often rely on the natural dynamics of physical systems.
- Robustness to noise and variability, due to the collective dynamics of coupled oscillators.

Some of challenges associated with oscillatory computers include:

**Precision** The precision of computations in oscillatory computers may be limited by the inherent variability and noise in the oscillatory dynamics.

**Programmability** Programming oscillatory computers can be difficult, as it requires the control of the complex dynamics of the coupling.

**Scalability** Scaling up oscillatory computers to large numbers of oscillators can be difficult, as the dynamics can become increasingly complex and hard to control.

**Interfacing** as with many systems discussed in this document interfacing with traditional digital systems is problematic, with similar problems to analog to digital conversion.

# 6 Spiking Neural Networks and Neuromorphic Compute

Spiking Neural Networks (SNNs) [30] are a type of artificial neural network that more closely mimic the behavior of biological neural networks. SNNs are a key component of neuromorphic computing, which aims to develop hardware and software systems that mimic the structure and function of biological neural networks. This is extensive literature on neuromorphic hardware platforms, such as SpiNNaker [21, 22], TrueNorth [49], Loihi [13], and BrainScale [50]. These platforms are optimized for low-power, real-time operation often outperforming their DL cousins in terms of energy usage [45], but at the cost of conjoined hardware and software offerings.

SNNs are explicitly temporal using spikes to define data, their key aspects are:

**Information Encoding** There are a variety of coding schemes, not just the "width" encoding discussed in this document. These are:

- **Rate Coding** Information is encoded in the average firing rate of neurons, similar to traditional ANNs.
- **Temporal Coding** Information is encoded in the precise timing of individual spikes. This can include schemes like Time to First Spike (TTFS) or Rank Order Coding (ROC).
- **Population Coding** Information is encoded in the collective activity of a group of neurons.

See appendix 8 for further discussion.

**Neuron Models** SNNs use more biologically plausible activation functions than ANNs. Some commonly used ones are:

- **Integrate-and-Fire (IF) Neurons** [7] IF neurons integrate incoming spikes and fire an output spike when a threshold is reached. After firing, the neuron's membrane potential is reset.
- **Leaky Integrate-and-Fire (LIF) Neurons** [54] LIF neurons are similar to IF neurons but include a leakage term that causes the membrane potential to decay over time.
- **Hodgkin-Huxley Neurons** [65] The Hodgkin-Huxley model is a detailed biophysical model that describes the dynamics of ion channels in the neuron membrane.

**Synaptic Models** In SNNs, synapses can have dynamic behaviors, unlike the static weights used in traditional ANNs. This gives rise to a computationally richer and more compact pattern processing systems.

One of the most relevant applications of this idea is the work done by Hopfield [26]. Hopfield's key insight was that the correct representation is the key to solving difficult problems:

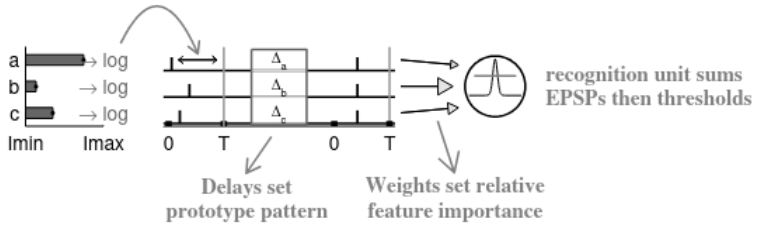


Figure 10: Computing with Action Potentials, taken from [26]

> The choice of information representation is of vital importance in making a computation easy, as is illustrated by the question 'is 3630225 divisible by 7?'. If the number 3630225 is in base 10, answering this takes a bit of work. If the number 3630225 is in base 7, the answer is immediate from inspection of the last digit. The choice of representation for analogue information is equally important for neural computation. [26]

The main focus of this work is to mimic the behaviour of the olfactory system. This particular problem is termed the "analog match" problems, and whilst solvable via traditional logistic methods is more robust when recast as a coincidence problem. Figure 10 shows how the system functions, note that the data is log scaled.

# 7 Critique and Next Steps

The document provides an overview of four emerging areas in computing: race logic, unary, oscillator, and neuromorphic. Each area presents unique challenges and opportunities for advancement in computational technology. To summarise the key points:

**Racelogic** is a practical and promising approach for utilising temporal data in computing. It's highlighted as one of the first methods to effectively a *truly* temporal approach. Also, the work on temporal memories, significantly strengthens the case for this technology, and racelogic has already explored wide-ranging applications. Its scope in terms of arithmetic and compute based operations is currently limited to a few comparison operations, and hence there is a lack of insight into utilising race logic as a general-purpose computer.

**Unary Computing** Despite extensive past research, unary computing has been largely overlooked in recent years. It holds potential for reevaluation in light of advancements in AI and complex computing systems. The primary challenge lies in its memory footprint, as traditional memory doesn't scale

well for unary representations. However, true temporal systems, ones which use time as data directly, are an avenue to alleviate this problem. Future research opportunities also include exploring unary signals with non-linear representations, which increase the efficiency of the subsequent computation.

**Oscillatory Computing** Oscillator computing shows significant promise, with potential for high-speed operations in the range of 50-100 GHz. This technology could potentially offer a 10x improvement over current computing capabilities, however seems to be applicable to specialist problems rather than general compute.

**Neuromorphic Computing** is the most mature technology among those reviewed. However, it is perhaps too literal in mimicking brain functionality, which may limit its potential. Our view is that time-based approaches should be emphasised over biological plausibility the analogy we draw is that of aircraft design, which draws inspiration from birds flight but in no way mimics the wing-flapping approach.

In conclusion, while each area reviewed above faces unique challenges, they all offer promising avenues for future research and development. Therefore the aim of the future work to conducted as a part of this PhD study is to perform some realistic practical assessments on example temporal systems in terms of key performance indicators. The scope of this work will initially focus solely on the more general version of temporal processing applied to neurally inspired architectures, since this is the most important opportunity.

# 8 Time Coding in the Human Brain

The following section describes the major encoding methods utilised by the brain. This serves as background to the biological inspiration of the temporal coding strategy [60].

Rate coding is the "standard" scheme for modelling neural signals computational [47]. The term is self-explanatory it is a count of the rate by which spikes arrive at a computational unit (see Figure 11). Averaging is robust and easy to model as a scalar value on traditional computers, however some questions exist as to whether a more immediate response is required from a (potentially threatening) stimulus, hence investigations into temporal and time to first spike encodings.

## 8.1 Spike Timings

In contrast to rate coding interval or spike coding utilises the exact time between two spikes as the magnitude of the signal. This model was first mentioned in the work of MacKay and McCullough [32] who focused on the channel rate of this simple model. Surprisingly, with neuron specific measurements, a maximum

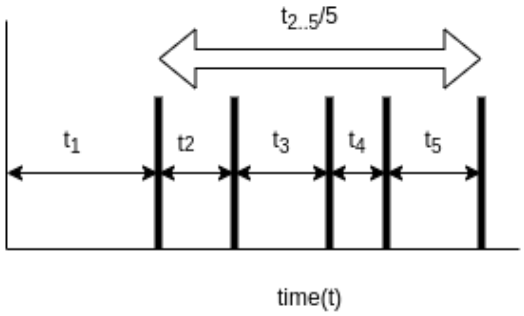


Figure 11: Rate and Time-to-first-spike Coding

selective information capacity of about 2.9bit/msec is produced as opposed to 1bit/msec from a simple single-bit based encoding over a channel, where Information capacity ($C$ in bits/time) is given by:

$$C = \frac{2}{\Delta T(m+r)} log_2(m-r)$$

where $\Delta T$ is the time resolution, $m = (T_m - T_r)/\Delta T$ approximately the range of data, and $r = \frac{T_r}{\Delta T}$ a lower bound.

## 8.2 Time to First Spike Coding

Time to First Spike (TTFS) coding [3] is a form of temporal coding used to represent and process information based on the precise timing of the first spike generated by a neuron in response to a stimulus. This encoding scheme is inspired by the observation that in some biological neural systems, the timing of the first spike can convey significant information about the stimulus. In TTFS coding, information is encoded in the latency or the time it takes for a neuron to generate the first spike after the onset of a stimulus. The stronger the stimulus, the faster the neuron reaches the threshold for generating a spike. This means that the timing of the first spike carries information about the stimulus intensity or other features. TTFS coding relies on the precise timing of spikes, often with millisecond or even sub-millisecond precision. This high temporal resolution allows for rapid and efficient information processing. Since information is conveyed by the timing of the first spike, TTFS coding can be energy-efficient. Once the first spike is generated, the neuron can remain silent until the next relevant stimulus, reducing the number of spikes and thus saving energy. TTFS coding enables fast responses to stimuli, as the system does not need to wait for multiple spikes or a change in the firing rate. This makes it suitable for applications where speed is crucial, such as real-time sensory processing or rapid decision-making tasks.

### 8.3 Order Coding

Rank Order Coding (ROC) [55] is a coding scheme used to represent and process information based on the relative order or rank of spikes generated by a population of neurons in response to a stimulus. Unlike TTFS coding, which focuses on the precise timing of the first spike from individual neurons, ROC considers the sequence or order of spikes across a population of neurons. In ROC, information is encoded in the relative order or rank of spikes generated by different neurons. When a stimulus is presented, the neurons that are most sensitive or selective to the stimulus features will fire first, followed by less sensitive neurons. The order in which neurons fire thus carries information about the stimulus. ROC is invariant to global latency shifts, meaning that the exact timing of the spikes is less critical than their relative order. This property makes ROC robust to variations in the overall response latency, which can be caused by factors such as changes in stimulus intensity or background activity. ROC enables fast processing of information, as the system does not need to wait for multiple spikes or a change in the firing rate. The rank order of the first spikes from a population of neurons can provide a quick and efficient representation of the stimulus.

## References


[1] A. Alaghi and J. P. Hayes. Survey of stochastic computing. *ACM Transactions on Embedded computing systems (TECS)*, 12(2s):1–19, 2013.

[2] J. Backus. Can programming be liberated from the von neumann style?: A functional style and its algebra of programs. *Commun. ACM*, 21(8):613–641, Aug. 1978.

[3] L. Bonilla, J. Gautrais, S. Thorpe, and T. Masquelier. Analyzing time-to-first-spike coding schemes: A theoretical approach. *Frontiers in Neuroscience*, 16:971937, 2022.

[4] A. Borst and F. E. Theunissen. Information theory and neural coding. *Nature neuroscience*, 2(11):947–957, 1999.

[5] E. Bracha. *Walshstore: the application of burst processing to fail-soft storage systems using walsh transforms.* University of Illinois at Urbana-Champaign, 1978.

[6] J. Buck. Synchronous rhythmic flashing of fireflies. ii. *The Quarterly review of biology*, 63(3):265–289, 1988.

[7] A. N. Burkitt. A review of the integrate-and-fire neuron model: I. homogeneous synaptic input. *Biological cybernetics*, 95:1–19, 2006.

[8] E. Corti. Networks of coupled vo2 oscillators for neuromorphic computing. Technical report, EPFL, 2021.

[9] G. Csaba and W. Porod. Perspectives of using oscillators for computing and signal processing. *arXiv preprint arXiv:1805.09056*, 2018.

[10] G. Csaba and W. Porod. Coupled oscillators for computing: A review and perspective. *Applied physics reviews*, 7(1), 2020.

[11] J. Das and P. D. Sharma. Pulse-interval modulation. *Electronics Letters*, 3:288–289, 1967.

[12] R. David. We're not prepared for the end of moore's law. `https://www.technologyreview.com/2020/02/24/905789/were-not-prepared-for-the-end-of-moores-law/`. Accessed: 1 Jan 2024.

[13] M. Davies, N. Srinivasa, T.-H. Lin, G. Chinya, Y. Cao, S. H. Choday, G. Dimou, P. Joshi, N. Imam, S. Jain, et al. Loihi: A neuromorphic manycore processor with on-chip learning. *IEEE Micro*, 38(1):82–99, 2018.

[14] C. Delacour, S. Carapezzi, M. Abernot, G. Boschetto, N. Azemard, J. Salles, T. Gil, and A. Todri-Sanial. Oscillatory neural networks for edge ai computing. In *2021 IEEE computer society annual symposium on VLSI (ISVLSI)*, pages 326–331. IEEE, 2021.

[15] C. Delacour, S. Carapezzi, G. Boschetto, M. Abernot, T. Gil, N. Azemard, and A. Todri-Sanial. A mixed-signal oscillatory neural network for scalable analog computations in phase domain. *Neuromorphic Computing and Engineering*, 3(3):034004, 2023.

[16] A. Dollas. *Architecture and applications of a unifield-type computer*. University of Illinois at Urbana-Champaign, 1987.

[17] J. Edwards, S. O'Keefe, and W. D. Henderson. Unconventional arithmetic: A system for computation using action potentials. In *Proc. of Unconventional Computation and Natural Computation*, pages 155–163, 2014.

[18] J. Edwards, A. Wheeldon, R. Shafik, and A. Yakovlev. A variable bitwidth asynchronous dot product unit. In *IEEE International Symposium on Asynchronous Circuits and Systems*, 2019.

[19] J. W. Esch. *—Rascel—A Programmable Analog Computer Based on a Regular Array of Stochastic Computing Element Logic*. University of Illinois at Urbana-Champaign, 1969.

[20] E. P. Frady and F. T. Sommer. Robust computation with rhythmic spike patterns. *Proceedings of the National Academy of Sciences*, 116(36):18050–18059, 2019.

[21] S. Furber. Large-scale neuromorphic computing systems. *Journal of Neural Engineering*, 13(5):051001, 2016.

[22] S. B. Furber, F. Galluppi, S. Temple, and L. A. Plana. Spinnaker: A million core processor system for highly parallel neural network simulation. *Proceedings of the IEEE*, 102(5):652–665, 2014.

[23] Z. Ghassemlooy and A. Hayes. Digital pulse interval modulation for ir communication systems—a review. *International Journal of Communication Systems*, 13(7-8):519–536, 2000.

[24] Z. Ghassemlooy, A. Hayes, N. Seed, and E. Kaluarachchi. Digital pulse interval modulation for optical communications. *IEEE Communications Magazine*, 36(12):95–99, 1998.

[25] J. L. Hennessy and D. A. Patterson. A new golden age for computer architecture. *Communications of the ACM*, 62(2):48–60, 2019.

[26] J. J. Hopfield. Pattern recognition computation using action potential timing for stimulus representation. *Nature*, 376(6535):33–36, 1995.

[27] W. Jeon, G. Ko, J. Lee, H. Lee, D. Ha, and W. W. Ro. Chapter six - deep learning with gpus. In S. Kim and G. C. Deka, editors, *Hardware Accelerator Systems for Artificial Intelligence and Machine Learning*, volume 122 of *Advances in Computers*, pages 167–215. Elsevier, 2021.

[28] E. D. Kaluarachchi. *Digital pulse interval modulation for optical communication systems*. Sheffield Hallam University (United Kingdom), 1997.

[29] Y. LeCun, Y. Bengio, and G. Hinton. Deep learning. *Nature*, 521(7553):436–444, 2015.

[30] W. Maass and C. M. Bishop. *Pulsed neural networks*. MIT press, 2001.

[31] D. J. C. MacKay. *Information Theory, Inference & Learning Algorithms*. Cambridge University Press, New York, NY, USA, 2002.

[32] D. M. MacKay and W. S. McCulloch. The limiting information capacity of a neuronal link. *The bulletin of mathematical biophysics*, 14(2):127–135, 1952.

[33] A. Madhavan, M. W. Daniels, and M. D. Stiles. Temporal state machines: Using temporal memory to stitch time-based graph computations. *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, 17(3):1–27, 2021.

[34] A. Madhavan, T. Sherwood, and D. Strukov. Race logic: A hardware acceleration for dynamic programming algorithms. *ACM SIGARCH Computer Architecture News*, 42(3):517–528, 2014.

[35] A. Madhavan, T. Sherwood, and D. Strukov. Race logic: abusing hardware race conditions to perform useful computation. *IEEE Micro*, 35(3):48–57, 2015.

[36] A. Madhavan and M. D. Stiles. Storing and retrieving wavefronts with resistive temporal memory. In *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5. IEEE, 2020.

[37] O. Maher, R. Bernini, N. Harnack, B. Gotsmann, M. Sousa, V. Bragaglia, and S. Karg. Highly reproducible and cmos-compatible vo2-based oscillators for brain-inspired computing. *Scientific Reports*, 14(1):11600, 2024.

[38] M. Mandal and B. C. Sarkar. Ring oscillators: Characteristics and applications. *Indian Journal of Pure and Applied Physics*, 48:136–145, 02 2010.

[39] S. Marougi and K. Sayhood. Signal-to-noise performance of the pulse-interval and width-modulation system. *Electronics Letters*, 14(19):528–530, 1983.

[40] M. Meister and M. J. Berry. The neural code of the retina. *Neuron*, 22(3):435–450, 1999.

[41] G. E. Moore. Readings in computer architecture. chapter Cramming More Components Onto Integrated Circuits, pages 56–59. Morgan Kaufmann Publishers Inc., San Francisco, CA, USA, 2000.

[42] Z. Pan and J. S. M. Di Wu. T-mac: Temporal multiplication with accumulation. *TC*, 1:2, 2022.

[43] W. Poppelbaum, C. Afuso, and J. Esch. Stochastic computing elements and systems. In *Proceedings of the November 14-16, 1967, fall joint computer conference*, pages 635–644, 1967.

[44] W. Poppelbaum, A. Dollas, J. Glickman, and C. O'Toole. Unary processing. In M. C. Yovits, editor, *Advances in Computers*, volume 26 of *Advances in Computers*, pages 47 – 92. Elsevier, 1987.

[45] A. Reuther, P. Michaleas, M. Jones, V. Gadepally, S. Samsi, and J. Kepner. Survey of machine learning accelerators. 09 2020.

[46] F. Rieke, D. Bodnar, and W. Bialek. Naturalistic stimuli increase the rate and efficiency of information transmission by primary auditory afferents. *Proceedings of the Royal Society of London B: Biological Sciences*, 262(1365):259–265, 1995.

[47] F. Rosenblatt. The perceptron: a probabilistic model for information storage and organization in the brain. *Psychological review*, 65(6):386, 1958.

[48] M. Sato, M. Murata, and T. Namekawa. Pulse interval and width modulation for video transmission. *IEEE Transactions on Cable Television*, (4):165–173, 1978.

[49] J. Sawada, F. Akopyan, A. S. Cassidy, B. Taba, M. V. Debole, P. Datta, R. Alvarez-Icaza, A. Amir, J. V. Arthur, A. Andreopoulos, et al. Truenorth ecosystem for brain-inspired computing: scalable systems, software, and applications. In *SC'16: Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis*, pages 130–141. IEEE, 2016.

[50] S. Schmitt, J. Klähn, G. Bellec, A. Grübl, M. Guettler, A. Hartel, S. Hartmann, D. Husmann, K. Husmann, S. Jeltsch, et al. Neuromorphic hardware in the loop: Training a deep spiking network on the brainscales wafer-scale system. In *2017 international joint conference on neural networks (IJCNN)*, pages 2227–2234. IEEE, 2017.

[51] C. H. Segal. *Digital Non-binary Spiking Communication and Computation Channel*. University of California, Santa Barbara, 2022.

[52] J. E. Smith. Temporal computer organization. *arXiv preprint arXiv:2201.07742*, 2022.

[53] S. H. Strogatz. Nonlinear dynamics and chaos: with applications to physics, biology, chemistry, and engineering (studies in nonlinearity). *Nonlinear Dynamics and Chaos: With Applications to Physics, Biology, Chemistry, and Engineering (Studies in Nonlinearity)*, 2001.

[54] D. Tal and E. L. Schwartz. Computing with the leaky integrate-and-fire neuron: logarithmic computation and multiplication. *Neural computation*, 9(2):305–318, 1997.

[55] S. Thorpe and J. Gautrais. Rank order coding. In *Computational Neuroscience: Trends in Research, 1998*, pages 113–118. Springer, 1998.

[56] G. Tzimpragos. *Computing with Temporal Operators*. University of California, Santa Barbara, 2022.

[57] G. Tzimpragos, N. Tsiskaridze, K. Huch, A. Madhavan, and T. Sherwood. From arbitrary functions to space-time implementations. In *Proceedings of the 1st Unary Computing Workshop (ISCA'19)*, 2019.

[58] G. Tzimpragos, J. Volk, D. Vasudevan, N. Tsiskaridze, G. Michelogiannakis, A. Madhavan, J. Shalf, and T. Sherwood. Temporal computing with superconductors. *IEEE Micro*, 41(3):71–79, 2021.

[59] H. Vakili, M. N. Sakib, S. Ganguly, M. Stan, M. W. Daniels, A. Madhavan, M. D. Stiles, and A. W. Ghosh. Temporal memory with magnetic racetracks. *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, 6(2):107–115, 2020.

[60] J. D. Victor. How the brain uses time to represent and process visual information. *Brain research*, 886(1-2):33–46, 2000.

[61] J. Volk, A. Wynn, E. Golden, T. Sherwood, and G. Tzimpragos. Addressable superconductor integrated circuit memory from delay lines. *Scientific Reports*, 13(1):16639, 2023.

[62] D. Wu. *Power-Efficient Computer Architecture via Unary and Approximate Computing*. The University of Wisconsin-Madison, 2023.

[63] D. Wu, J. Li, R. Yin, H. Hsiao, Y. Kim, and J. San Miguel. Ugemm: Unary computing architecture for gemm applications. In *2020 ACM/IEEE 47th Annual International Symposium on Computer Architecture (ISCA)*, pages 377–390. IEEE, 2020.

[64] D. Wu and J. San Miguel. usystolic: Byte-crawling unary systolic array. In *2022 IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, pages 12–24. IEEE, 2022.

[65] B. A. y Arcas, A. L. Fairhall, and W. Bialek. Computation in a single neuron: Hodgkin and huxley revisited. *Neural computation*, 15(8):1715–1749, 2003.