Exam Questions on Chapter 3: Computer Architecture

True/False Questions

1. The Program Counter(PC) always points to the next instruction to be executed.
2. In the von Neumann architecture, the CPU can fetch and execute multiple instructions at the same time.
3. A bus is used to carry signals and data between components of a computer.
4. All interrupts must be processed immediately, regardless of their priority.
5. The control bus carries data between the CPU and memory.
6. General-purpose computers rely on hardwired logic for executing programs.
7. Nested interrupts allow higher-priority tasks to interrupt lower-priority ones.
8. The Instruction Register (IR) holds the instruction currently being decoded or executed.
9. A single bus architecture is more efficient than multiple-bus systems.
10. An interrupt handler routine saves the CPU's current state before addressing the interrupt.

Multiple-Choice Questions

1. Which component is responsible for decoding instructions?
   a) ALU
   b) Control Unit
   c) Memory
   d) I/O Unit

2. What does the Program Counter (PC) store?
   a) Current instruction
   b) Address of the next instruction
   c) Address of the current data
   d) Result of the last operation

3. Which bus specifies the location of data in memory?
   a) Data Bus
   b) Address Bus
   c) Control Bus
   d) Memory Bus

4. How many bits are reserved for opcode in a 16-bit instruction format with 12-bit addressing?
   a) 8 bits
   b) 4 bits
   c) 12 bits
   d) None

5. What type of operation does the ALU not perform?
   a) Logical operations
   b) Arithmetic operations
   c) Data storage
   d) Comparisons

6. What is the function of the Instruction Register (IR)?
   a) Store operands
   b) Store memory addresses
   c) Store the current instruction
   d) Store results of operations

7. Which signal informs the CPU to stop its current task and perform another?
   a) Timer
   b) Interrupt
   c) Fetch cycle
   d) Decode signal

8. What is the width of a data bus with a 64-bit transfer capacity?
   a) 32 lines
   b) 64 lines
   c) 128 lines
   d) Depends on the CPU

9. Nested interrupts prioritize:
   a) Tasks randomly
   b) Based on urgency and priority levels
   c) Based on task complexity
   d) First-come, first-served

10. What type of module temporarily stores data exchanged between CPU and I/O?
   a) Cache
   b) I/O Buffer
   c) MAR
   d) IR
11. What does the Control Unit (CU) do in a CPU?
   a) Performs arithmetic operations
   b) Controls and coordinates CPU operations
   c) Stores data temporarily
   d) Transfers data to external devices

12. In a von Neumann architecture, instructions are stored in:
   a) Separate memory from data
   b) A single shared memory with data
   c) The ALU
   d) Registers only

13. Which of the following is an example of a control signal?
   a) Add
   b) Memory Read
   c) Register
   d) Address Bus

14. How is priority determined in nested interrupts?
   a) Randomly
   b) Assigned by the programmer
   c) By hardware or software based on urgency
   d) By alphabetical order

15. What is the role of the MAR (Memory Address Register)?
   a) Stores data read from memory
   b) Holds the memory location to be read or written
   c) Stores the current instruction being executed
   d) Acts as temporary storage for data

16. What happens when the Program Counter (PC) is incremented?
   a) Data is written to memory

b) The next memory address is prepared for fetching
c) A new program starts
d) Interrupts are disabled

17. A CPU executes an instruction after it is:
a) Fetched from I/O
b) Written to memory
c) Decoded
d) Saved to a buffer

18. What is a key disadvantage of a single bus system?
a) High performance
b) Simple design
c) Bottlenecks with multiple devices
d) Limited data storage

19. The data bus width affects:
a) The amount of data that can be transferred at a time
b) The memory size a system can address
c) The number of interrupts a CPU can handle
d) The frequency of instruction execution

20. How are I/O devices addressed in memory-mapped I/O?
a) Using separate ports
b) Using memory addresses
c) Using MAR only
d) Using direct signals

21. Which type of interrupt cannot be ignored by the CPU?
a) Timer interrupt
b) Hardware failure interrupt
c) Program interrupt
d) I/O interrupt

22. Which bus transmits binary commands like "read" or "write"?
a) Address bus
b) Control bus
c) Data bus
d) Interrupt bus

23. What is the main function of cache memory?
a) Store permanent data
b) Speed up access to frequently used data and instructions
c) Transfer data to external devices
d) Perform logical operations

24. What happens if multiple devices try to use the bus at the same time?
a) Data is prioritized based on address size
b) Signals overlap and become garbled
c) The fastest device is given control
d) All devices share control equally

25. Which is a characteristic of multiplexed buses?
a) Separate lines for address and data
b) Shared lines for address and data

c) Better performance in all cases
d) Only used in modern CPUs

Fill in the Blanks

1. The _____ is the main processing unit of the computer that performs all arithmetic and logical operations.
2. The Instruction Register (IR) holds the _____ that is being executed or decoded.
3. _____ architecture uses a single memory for both instructions and data.
4. The CPU communicates with memory using the _____ bus.
5. A bus with 32 lines can address _____ memory locations.
6. Nested interrupts rely on _____ levels to manage multiple tasks.
7. In the basic instruction cycle, the CPU starts by fetching instructions from _____.
8. The _____ specifies the memory address to read or write data.
9. An _____ is a mechanism to signal the CPU for urgent processing.
10. A _____ bus system can reduce performance bottlenecks compared to a single bus system.

Workout Questions

1. Instruction Fetch:
- Assume a computer has a 16-bit instruction format, with 4 bits for the opcode and 12 bits for addressing. If the PC is 300, calculate:
  a) The next instruction address after two fetches.
  b) The total number of unique instructions possible.

2. Interrupt Handling:
- Describe the steps the CPU takes when handling an interrupt, including context saving and restoring.

3. Bus Design:
- If a data bus is 32 bits wide and needs to transfer a 128-bit value, how many cycles are required?

4. Instruction Decoding:
- Given the opcode table below, decode the instruction ‘0x5A1F‘:
  Opcode (4 bits):
  - ‘5‘: ADD
  - ‘A‘: Addressing mode.
  Explain its execution.

5. Data Flow:
- Diagram and explain how data moves between CPU, memory, and an I/O device during a read operation.