

# AR0135ATSM00XUEAH3-GEVB

## AR0135AT Evaluation Board User's Manual



ON Semiconductor®

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### Evaluation Board Overview

The evaluation boards are designed to demonstrate the features of image sensors products from ON Semiconductor. This headboard is intended to plug directly into the Demo 3 system. Test points and jumpers on the board provide access to the clock, I/Os, and other miscellaneous signals.

### Features

- Clock Input
  - ♦ Default – 27 MHz Crystal Oscillator
  - ♦ Optional Demo 3 Controlled MCLK
- Two-wire Serial Interface
  - ♦ Selectable Base Address
- Parallel Interface
- HiSPi (High Speed Serial Pixel) Interface
- ROHS Compliant

### Block Diagram

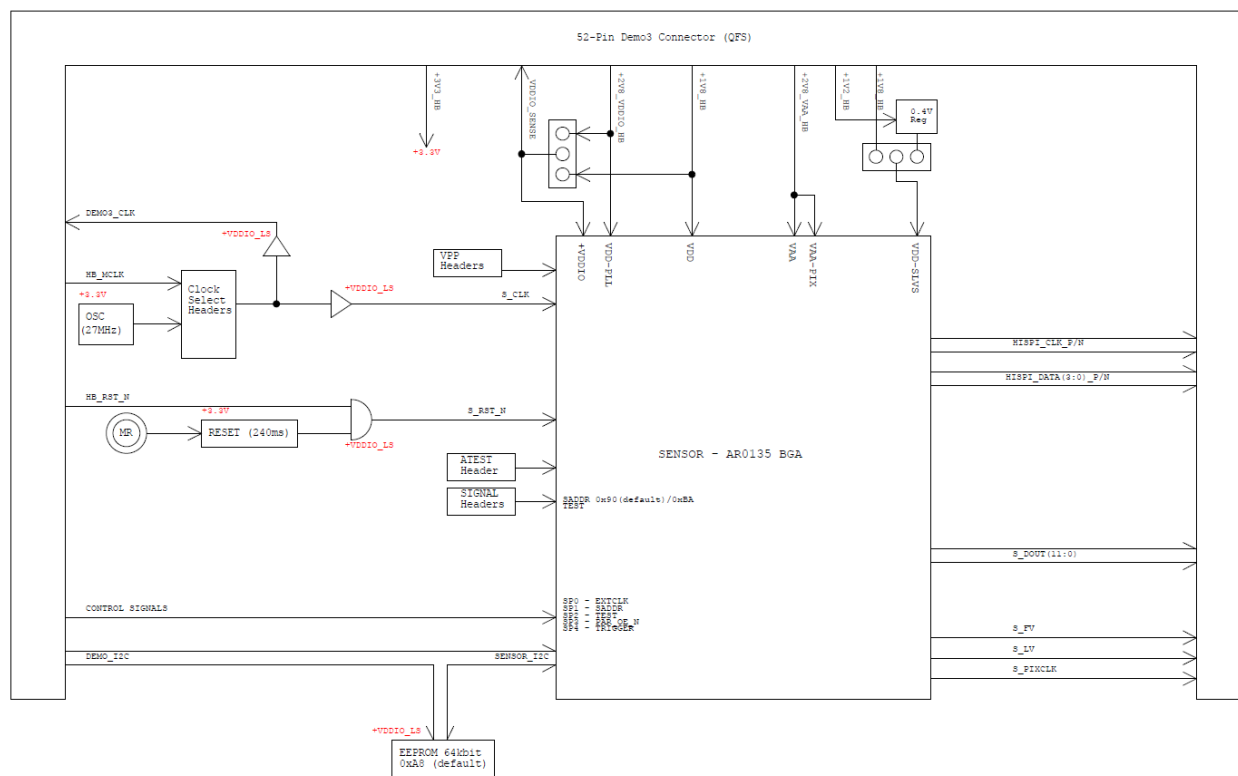


Figure 2. Block Diagram of AR0135ATSM00XUEAH3-GEVB

### EVAL BOARD USER'S MANUAL



Figure 1. AR0135AT Evaluation Board

# AR0135ATSM00XUEAH3-GEVB

## Top View

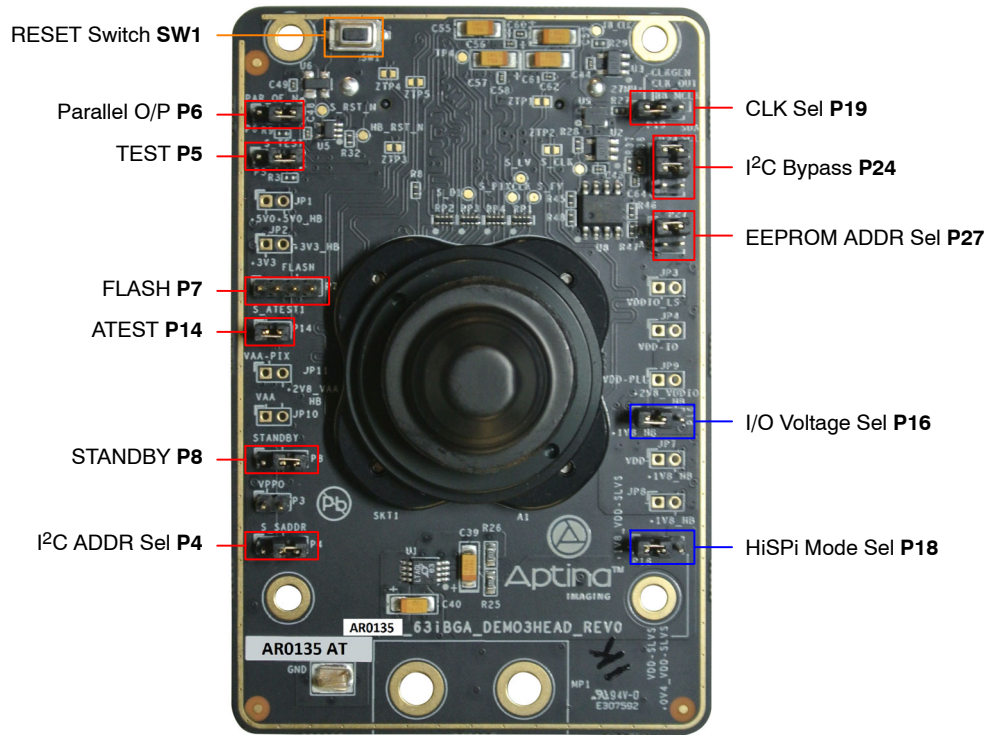


Figure 3. Top View of the Board – Default Jumpers

## Bottom View



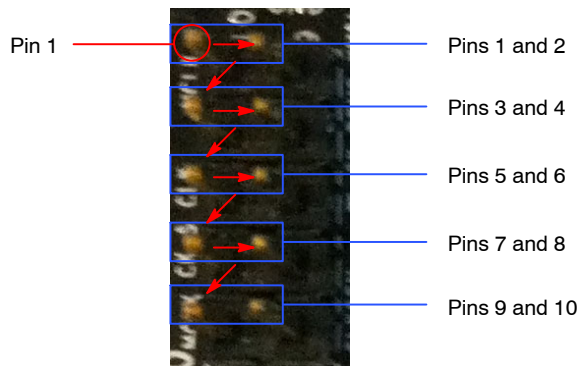
Figure 4. Bottom View of the Board – Connector

### Jumper Pin Locations

The jumpers on headboards start with Pin 1 on the leftmost side of the pin. Grouped jumpers increase in pin size with each jumper added.



**Figure 5. Pin Locations for a Single Jumper. Pin 1 is Located at the Leftmost Side and Increases as it Moves to the Right**



**Figure 6. Pin Locations and Assignments of Grouped Jumpers. Pin 1 is Located at the Top-Left Corner and Increases in a Zigzag Fashion Shown in the Picture**

### Jumper/Header Functions & Default Positions

**Table 1. JUMPERS AND HEADERS**

Jumper/Header No.	Jumper/Header Name	Pins	Description
P3	VPP	Open	OTPM Programming Voltage Not Supplied
P4	SADDR	2-3 (Default)	I <sup>2</sup> C Address Set to 0x20
		1-2	I <sup>2</sup> C Address Set to 0x30
P5	TEST	2-3 (Default)	Set to Normal Mode
		Open	Set to Test Mode
P6	OE_N	2-3 (Default)	Parallel Output Enabled
		Open	Parallel Output Disabled; HiSPi Output Enabled
P7	FLASH	1	+5V0
		2	GND
		3	FLASH
		4	+3V3
P8	STANDBY	2-3 (Default)	Normal Mode
		1-2	Standby Mode
P14	Analog Test	1-2 (Default)	ATEST → GND
P16	VDD_IO	1-2 (Default)	1.8 V Operation of Sensor
		2-3	2.8 V Operation of Sensor
P18	HiSPi Mode	1-2 (Default)	SLVS Mode
		2-3	Hi-VCM Mode

**Table 1. JUMPERS AND HEADERS** (continued)

Jumper/Header No.	Jumper/Header Name	Pins	Description
P19	Master Clock	1–2 (Default)	On-Board Oscillator (27 MHz)
		2–3	AR0140AT Evaluation Board MCLK
P24	I <sup>2</sup> C	1–2 & 3–4 (Default)	Demo 3 SCL & SDA Connected to Sensor SCL & SDA Respectively
P27	EEPROM Addr. Sel	3–4 Open & 1–2 Closed (Default)	EEPROM Address Set to 0xA8
		3–4 Open & 1–2 Closed	EEPROM Address Set to 0xAC
		3–4 Open & 1–2 Closed	EEPROM Address Set to 0xA4
		3–4 Open & 1–2 Closed	EEPROM Address Set to 0xA0
P28	TRIGGER	1–2	Trigger Input Enabled
		Open (Default)	Connect Generator Between Pin 1 and GND
SW1	RESET	N/A	When Pushed, 240 ms Reset Signal will be Sent to AR0135AT

**Interfacing to ON Semiconductor Demo 3 Baseboard**

The ON Semiconductor Demo 3 baseboard has a similar 52-pin connector which mates with J1 of the headboard. The four mounting holes secure the baseboard and the headboard with spacers and screws.

**Shorted Jumpers for Power Measurement**

Different supplies to the evaluation board are provided by trace shorted jumper, for any voltage and power measurements. To conduct current for current measurement on a given power rail, cut the trace between the two pins of their respective JP, and insert an ammeter prior to powering up the system. The figure below shows where the trace to cut is located.

**Table 2. SHORTED JUMPERS FOR POWER MEASUREMENT**

Jumper	Voltage (V)
JP1 (from Demo3)	5.0
JP2 (Peripheral 3.3 V)	3.3
JP3 (VDDIO_LS)	1.8
JP4 (VDDIO)	1.8
JP7 (VDD)	1.8
JP8 (VDD_SLVS)	1.8
JP9 (VDD_PLL)	2.8
JP10 (VAA)	2.8
JP11 (VAA_PIX)	2.8
JP18 (VDD_SLVS)	0.4



**Figure 7. Top and Bottom View of Shorted Jumper.**  
**The Bottom View Shows the Trace Location to Cut for Current Measurement**

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