FPGATORS GBM #2

AGENDA

Introduction

VHDL Workshop 2

Future Workshops

Starting Projects

RCC Tryouts

SPAM GOOGLE FORM

INTRODUCTION

- FPGA Design Workshop 9/25 was pretty good
- VHDL Basics Workshop 10/6 covered combinational logic in 1 hr
- VHDL Basics Part 2 (coding portion) 10/23 @ 5:30pm
- Are these too frequent or not frequent enough…. Thoughts?

VHDL WORKSHOP 2 10/23 @ 5:30PM ONLINE!! AND RECORDED LOL

1. Previously covered FPGA design flow, explained what IDE we commonly use, design suites, and will introduce version control soon
2. Introduced combinational circuits and coding guidelines
3. Will continue to make a coding portion for combinational and then explain sequential logic

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity mux_2x1 is
    port(
        in0    : in  std_logic;
        in1    : in  std_logic;
        sel    : in  std_logic;
        output : out std_logic);
end mux_2x1;

architecture case_statement of mux_2x1 is
begin
    process(in0, in1, sel)
    begin
        case sel is
            when '0' =>
                output <= in0;
            when others =>
                output <= in1;
        end case;
    end process;
end case_statement;
```

FUTURE WORKSHOPS

- What is a Testbench? (continuing after VHDL basics)
- SystemVerilog Basics (for Digital Design knowers)
- Advanced Testbenches (continuing after SV Basics)

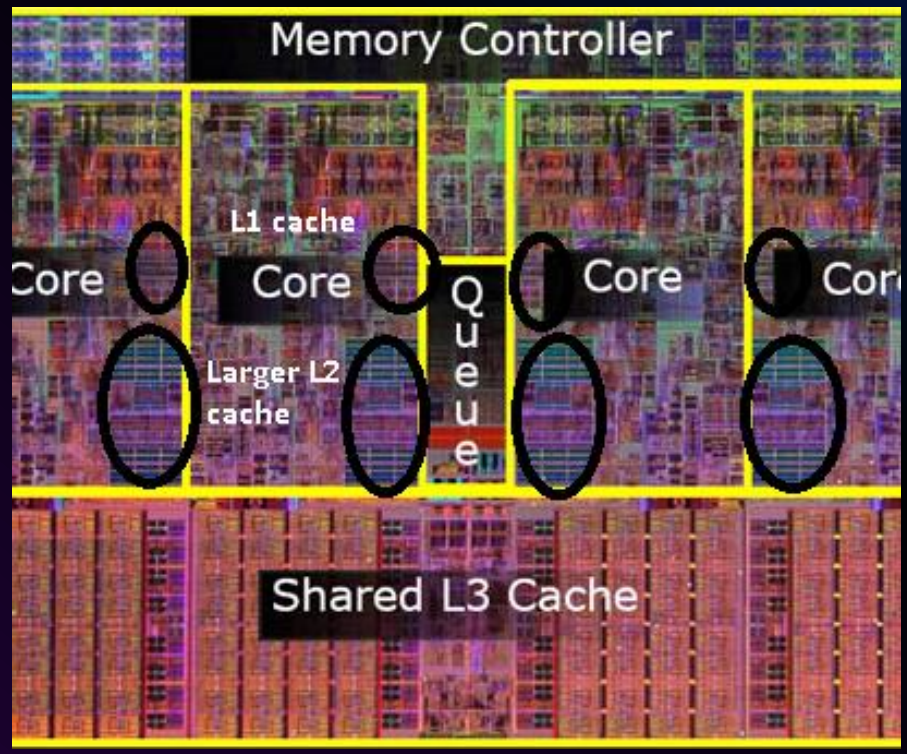
STARTING PROJECTS!!

Pseudo-Random Number Generator (after we cover sequential logic)

Hardware Cache Fundamentals (in VHDL and SV)

Github Classroom is still being set up so be patient pls

DE10-LITE FPGA BOARDS WILL BE PROVIDED TO THOSE WHO WANT TO PARTICIPATE (give it back tho)



RECONFIGURABLE COMPUTING COMPETITION

The 34th IEEE International Symposium On Field-Programmable Custom Computing Machines

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"RCC at FCCM 2026 invites researchers, students, and developers to design and demonstrate innovative self-defined projects on FPGA, AI Engines, or NPU architectures."

BEFORE NOVEMBER 1ST, we ask you to:

- Fill out **Google Form** to gauge interest (looking for people who have taken DD/RC1 already)
- Hold some sort of tryouts to gauge people's skill level and how big the team will be
- Brainstorm potential project ideas

THANK YOU

GO FPGAtors!!!!!!!!

We will have free pizza one day….