FPGAtors — GBM #1

Join us for an **exciting kickoff** to the Fall 2025 semester, where we will explore our goals and upcoming events!

Agenda
(Google form virus link)

01 We'll introduce our **officers** and their roles in FPGAtors.

02 Next, we'll discuss various **workshops** designed to enhance your skills.

03 Finally, learn about exciting **projects** and upcoming ECE events to participate in.

Bro...What is an FPGA

Do you live under a rock.

Workshops Overview

Explore essential topics for FPGA development and design skills.

01

6 Officer-Hosted Workshops to choose from for the Fall semester (the ones with most interest will be held)

02

Trying to cater to noobs and pros

03

Intro to Hardware Description Languages, Testbenches, and general design flow

FPGA Design Flow

Understand the **process:** designing the circuit, writing the code, and putting it on an FPGA

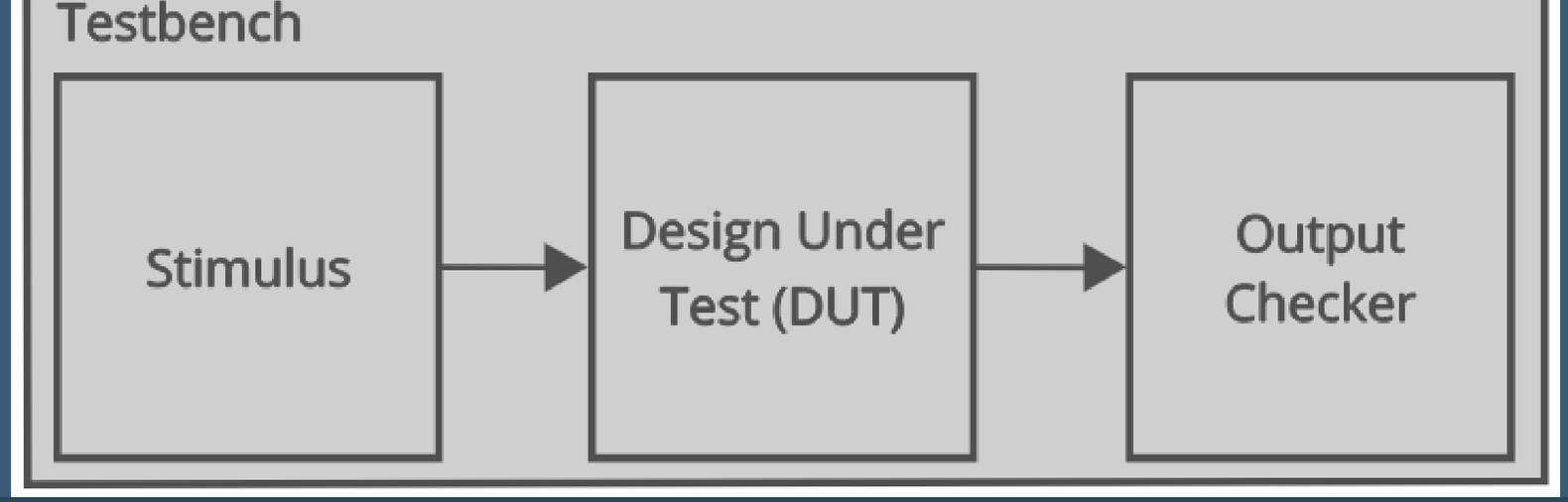
What is an FPGA? What are the applications? What software do I use? How do I program the FPGA? I know NOTHING!
if that’s u this is for u

```
39
40  library ieee;
41  use ieee.std_logic_1164.all;
42
43  entity welcome is
44      port(
45          clk      : in  std_logic;      -- This is the main clock
46          rst      : in  std_logic;
47          data_in  : in  std_logic;
48          data_out : out std_logic
49      );
50  end entity welcome;
```

VHDL Programming Basics

Key concepts to kickstart your VHDL programming journey and design

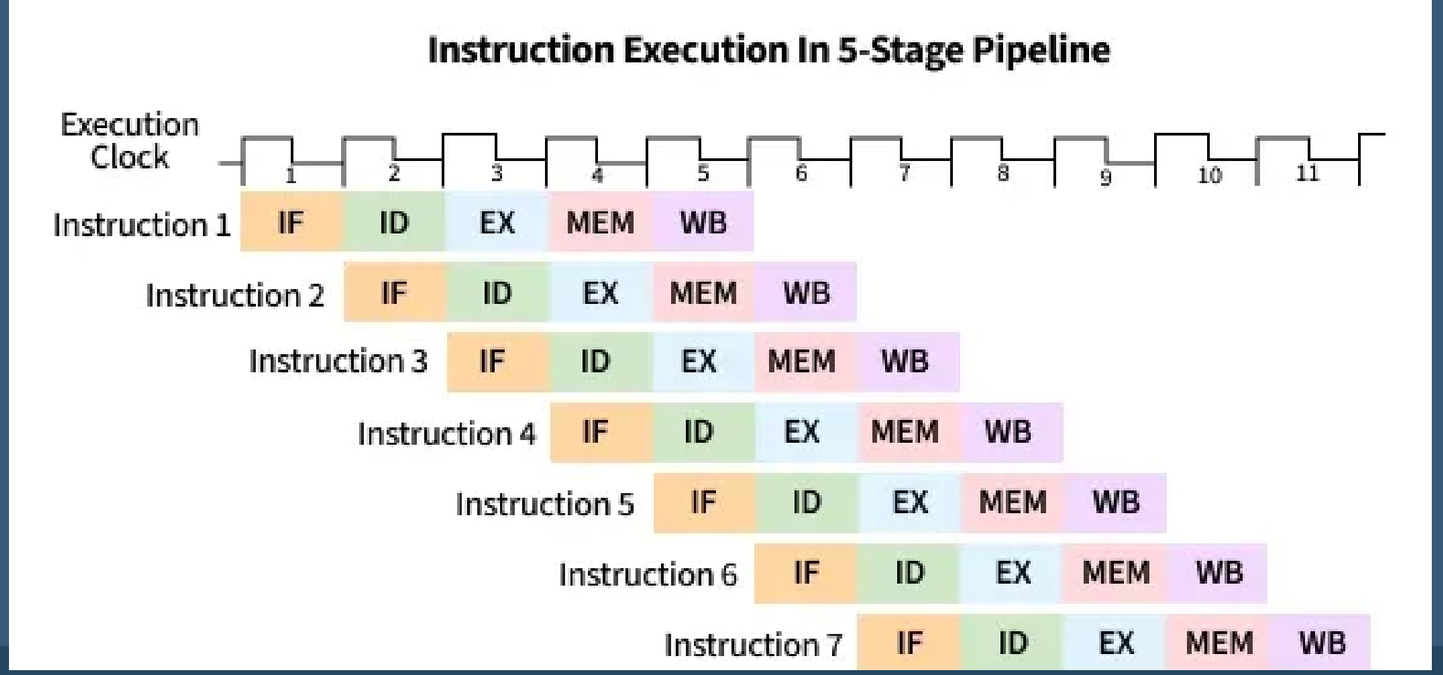
An example of a **Hardware Description Language**; a programming language that designs a circuit depending on how you write your code. Will serve as a tutorial to understanding digital logic represented as an HDL instead of schematic entry.



Basic Testbenches

Crafting simple testbenches for effective verification in FPGA design

If I make a circuit, how do I know if it’s working how I want it to? How do I make sure I test all possible combinations of my circuit? If it’s working incorrectly, how do I debug?
THE ART OF TESTBENCHES



Pipelining Techniques

Boosting performance through effective pipelining in design

Pipelining is a critical technique that allows multiple instruction phases to be processed simultaneously, significantly enhancing overall performance and throughput in digital circuit design. Shoutout GPUs
THROUGHPUT THROUGHPUT THROUGHPUT

SV Basics

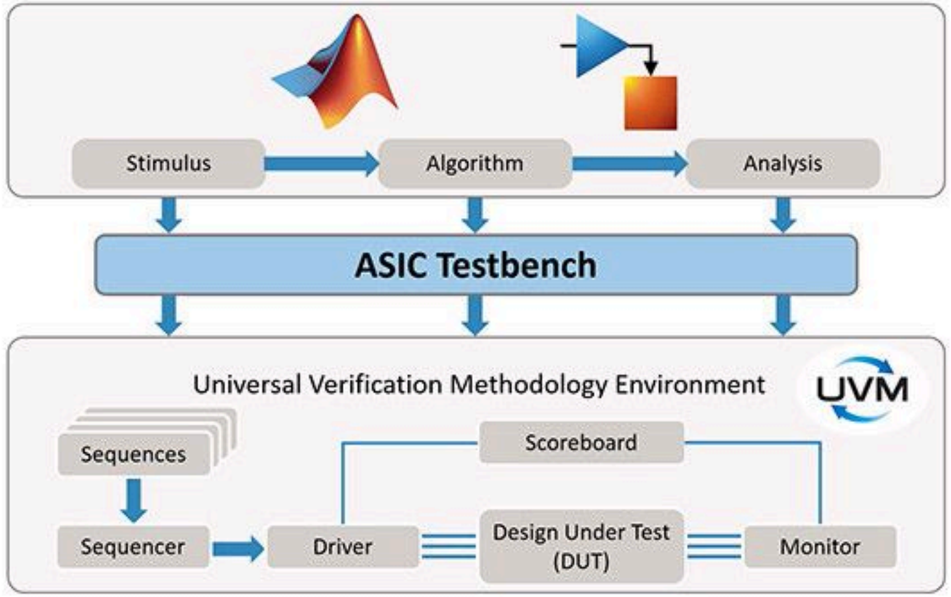
Understanding the Fundamentals of SystemVerilog for Design

```
module FSM( input logic reset,
            input logic X,
           output logic Y );

 always_ff @(posedge clk)
     if(reset) currentState <= A;
     else      currentState <= nextState;

 always_comb
     case(currentState)
         A:  if(X) nextState = C;
             else  nextState = B;
```

Another example of a Hardware Description Language that has syntax similar to C/C++. It’s better to know VHDL before learning in order to understand how to avoid certain behavioral mistakes when writing in SV.



Advanced Testbenches

Creating complex testbenches for thorough validation of FPGA designs

Why is MATLAB in the picture on the top right? I HATE MATLAB
What if I have a circuit too big to test all possible combinations? How do I make sure I thoroughly test my circuit if I can't test everything? What if I have really complex modules inside of my circuit? HOW DO I TEST EVERYTHING???
This is u

Projects Overview

Beginner and advanced tracks available for all members.

01

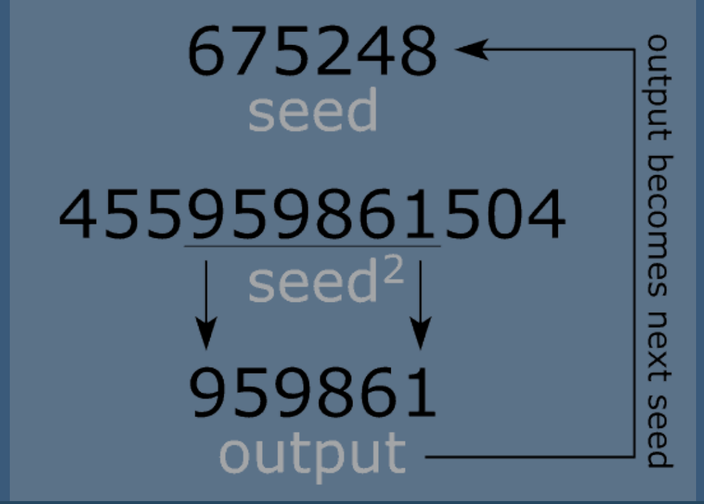
7 Projects to choose from for the Fall semester (the ones with the most interest win)

02

Made to be standalone projects or modules to augment your existing projects

03

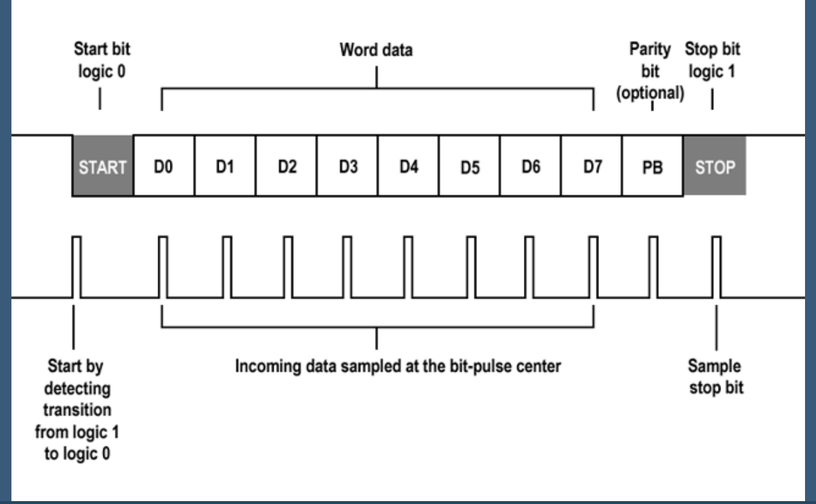
Short projects that last a few days to weeks, Long projects that last a few weeks to months

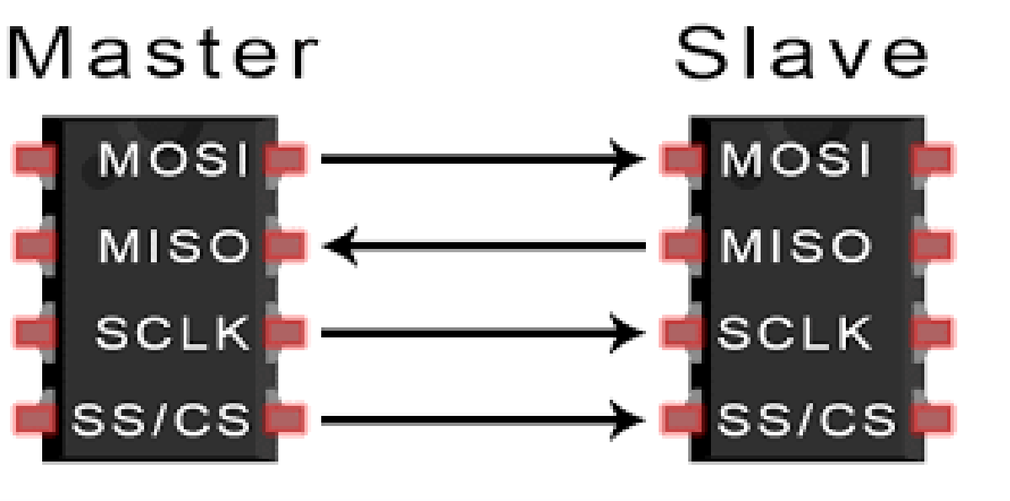


Pseudo-Random Number Generator

Using sequential logic to generate a pseudorandom sequence

What it said above

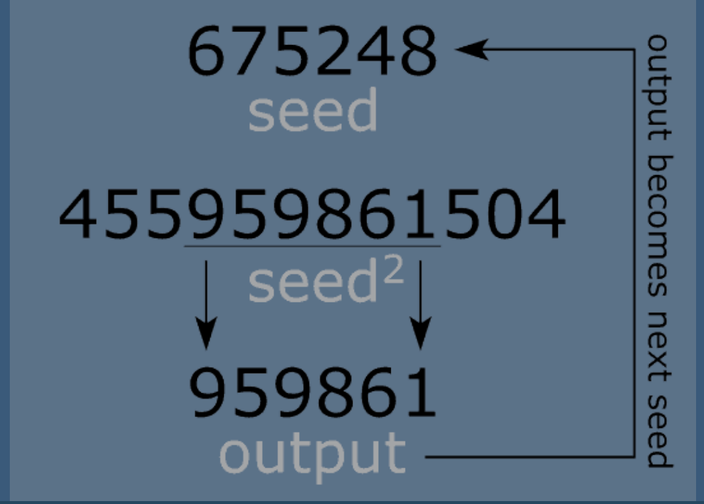




Communication Protocols

Standard protocols used to send and receive data from microcontrollers or sensors

UART (Universal Asynchronous Receiver Transmitter)
SPI (Serial Peripheral Interface)
AXI (Advanced eXstensible Interface)



Divide by 3

Dividing by 2 in hardware is easy, right? RIGHT? Well what makes dividing by 3 so hard? I DON'T KNOW SO LET'S FIND OUT

Longer Projects

Projects that can take longer than a few weeks

Game Emulator (random console) over HDMI
Cryptographic Module
Hardware Cache

Upcoming Events

Join us for exciting **ECE events** this fall semester!

01

ECE Ambassadors GBM **09/10** LAR234 6PM
Apple event **09/12**
https://news.ece.ufl.edu/2025/09/04/apple-guest-lecture/

02

Lockheed Martin 09/16 4PM Connections Room (Ground Level)
Signal Processing Society 09/19 6PM Informatics Institute
Blue Origin 09/23 5PM Connections Room (Ground Level)

03

Rohde & Schwarz Digital Modulation Info Session (Hosted by IEEE) TODAY TURL011 at 6:30PM

Career Fair

Key events to enhance your networking and career opportunities.

01 Attend various career fairs to connect with potential employers and mentors.

02 Prepare your resume and practice your elevator pitch before attending.

03 ECE Career Fair: 09/30
https://www.ece.ufl.edu/career-fair/

Career Fair (Technical Day): 10/01
https://career.ufl.edu/employers/career-showcase/

Questions and Discord!

For any questions regarding our events, membership, or projects, JOIN DA CORD