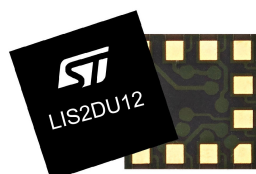


## Ultralow-power accelerometer with antialiasing and motion detection



LGA-12L  
2.0 x 2.0 x 0.74 mm

### Product status link

[LIS2DU12](#)

### Product summary

Order code	LIS2DU12TR
Temperature range [°C]	-40 to +85
Package	LGA-12L
Packing	Tape and reel

### Product resources

[AN5648](#) (device application note)

[TN0018](#) (design and soldering)

### Product label



## Features

- Supply voltage range from 1.62 to 3.6 V with independent IO supply
- Ultralow power consumption
  - Normal mode with antialiasing filter: 6.1  $\mu$ A
  - Ultralow-power mode: 0.47  $\mu$ A
  - One-shot mode: 0.2  $\mu$ A
  - Power-down: 0.02  $\mu$ A
- Low noise down to 181  $\mu$ g/ $\sqrt{\text{Hz}}$
- $\pm 2g/\pm 4g/\pm 8g/\pm 16g$  full scales
- ODR from 1.6 Hz to 800 Hz
- Embedded temperature sensor
- Embedded FIFO: up to 512 samples of accelerometer and temperature data in high resolution or up to 768 samples of acceleration data at low resolution
- High-speed I<sup>2</sup>C/SPI/MIPI I3C<sup>®</sup> digital output interface
- Embedded digital functions (free-fall, wake-up, single/double-tap recognition, activity/inactivity, 6D/4D orientation)
- Self-test
- Small package: 2.0 x 2.0 x 0.74 (max) mm LGA 12-lead
- 10000 g high shock survivability
- [ECOPACK](#) and RoHS compliant

## Applications

- [Wearable devices](#) (wristband and smart watches)
- [Game controllers](#)
- Hearing aids and portable healthcare devices
- True wireless stereo
- Wireless sensor nodes
- Motion-activated user interfaces (screen rotation, tap, double tap)
- [Asset trackers](#)

## Description

The LIS2DU12 is a linear 3-axis accelerometer with advanced digital functions whose MEMS and ASIC have been expressly designed to build an outstanding ultralow-power architecture in which the antialiasing filter operates with a power consumption among the lowest in the market.

The device has user-selectable full scales of  $\pm 2g/\pm 4g/\pm 8g/\pm 16g$  and is capable of measuring accelerations with output data rates from 1.6 Hz to 800 Hz.

The LIS2DU12 has an integrated 128-level FIFO buffer allowing to store a wide range of data, reducing system power consumption.

The embedded self-test capability allows the user to check that the sensor works in the final application.

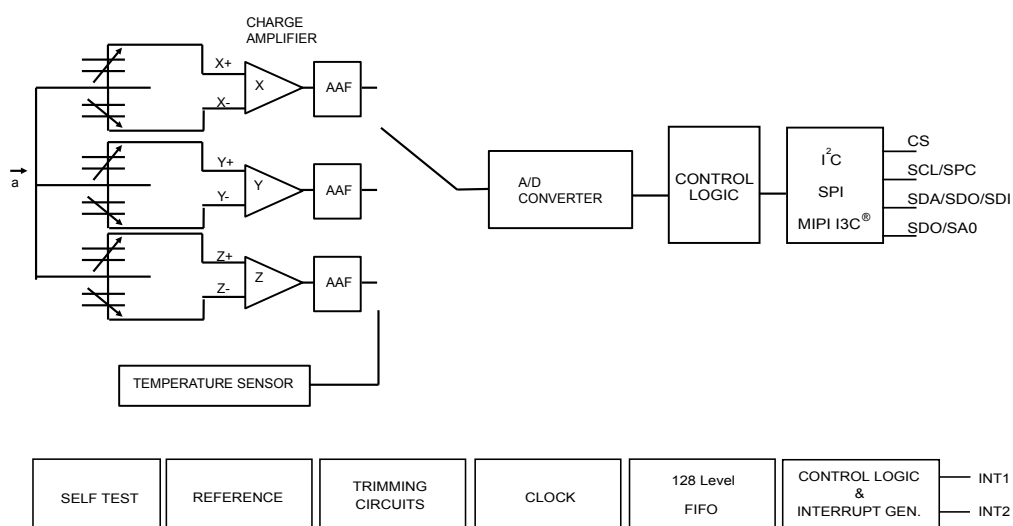
The device has a dedicated internal engine to process motion and acceleration detection including free-fall, wake-up, single/double-tap recognition, activity/inactivity, and 6D/4D orientation.

The LIS2DU12 is available in a small 2.0 x 2.0 mm plastic, land grid array (LGA) package only 0.74 mm thin, which places it among the smallest solution available in the market. It is guaranteed to operate over an extended temperature range from -40°C to + 85°C.

# 1 Block diagram and pin description

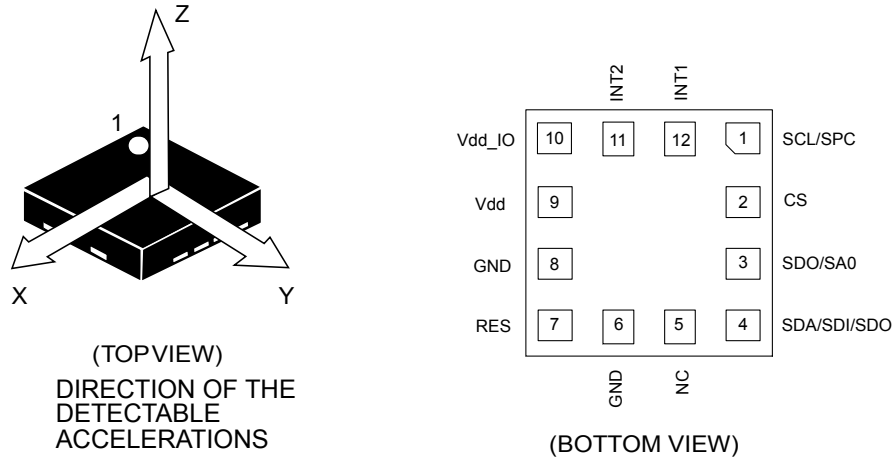
## 1.1 Block diagram

Figure 1. Block diagram



## 1.2 Pin description

**Figure 2. Pin connections**



**Table 1. Pin description**

Pin#	Name	Function
1	SCL SPC	I <sup>2</sup> C/MIPI I3C <sup>®</sup> serial clock (SCL) SPI serial port clock (SPC)
2 <sup>(1)</sup>	CS	SPI/I <sup>2</sup> C/MIPI I3C <sup>®</sup> mode selection (1: SPI idle mode / I <sup>2</sup> C/MIPI I3C <sup>®</sup> enabled; 0: SPI enabled / I <sup>2</sup> C/MIPI I3C <sup>®</sup> disabled)
3 <sup>(1)</sup>	SDO SA0	SPI serial data output (SDO) I <sup>2</sup> C less significant bit of the device address (SA0)
4	SDA SDI SDO	I <sup>2</sup> C/MIPI I3C <sup>®</sup> serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	NC	Internally not connected. Can be tied to Vdd, Vdd_IO, or GND.
6	GND	0 V supply
7	RES	Connect to GND
8	GND	0 V supply
9	Vdd	Power supply
10	Vdd_IO	Power supply for I/O pins
11 <sup>(2)</sup>	INT2	Interrupt pin 2. Clock input when selected in single data conversion on demand.
12 <sup>(2)</sup>	INT1	Interrupt pin 1

1. CS and SDO/SA0 pins are internally pulled up. The pull-up of the CS pin can be disconnected by setting bit CS\_PU\_DIS of register IF\_PU\_CTRL (0Ch) to 1. The pull-up of the SDO pin can be disconnected by setting bit SDO\_PU\_DIS of register IF\_PU\_CTRL (0Ch) to 1.
2. The INT1 and INT2 pins are internally pulled down. The internal pull-down of the INT1 pin can be disconnected by setting the PD\_DIS\_INT1 bit in IF\_CTRL (0Eh) to 1. The internal pull-down of the INT2 pin can be disconnected by setting the PD\_DIS\_INT2 bit in MD2\_CFG (20h) to 1.

## 2 Mechanical and electrical specifications

### 2.1 Mechanical characteristics

@ Vdd = 1.8 V, T = 25°C unless otherwise noted.

The product is factory calibrated at 1.8 V. The operational power supply range is from 1.62 V to 3.6 V.

**Table 2. Mechanical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
FS	Measurement range			±2		g
				±4		
				±8		
				±16		
So	Sensitivity	@ FS ±2 g		0.976		mg/digit
		@ FS ±4 g		1.952		
		@ FS ±8 g		3.904		
		@ FS ±16 g		7.808		
An	Noise density - normal mode	@ FS ±8 g ODR = 800 Hz, BW = ODR/2		287		µg/√Hz
TyOff	Zero-g level offset accuracy <sup>(2)</sup>			±11		mg
TCO	Zero-g offset change vs. temperature			±1		mg/°C
TCS	Sensitivity change vs. temperature			±0.035		%/°C
ST	Self-test positive difference	X-axis	50		700	mg
		Y-axis	50		700	
		Z-axis	200		1200	

1. Typical specifications are not guaranteed.

2. Values after factory calibration test and trimming.

## 2.2 Electrical characteristics

@ Vdd = 1.8 V, T = 25°C unless otherwise noted.

The product is factory calibrated at 1.8 V. The operational power supply range is from 1.62 V to 3.6 V.

**Table 3. Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
Vdd	Supply voltage		1.62	1.8	3.6	V
Vdd_IO	I/O pins supply voltage <sup>(2)</sup>		1.62		Vdd + 0.1	V
IddNM	Supply current in normal mode	FS = ±8 g ODR = 800 Hz, BW = ODR/2 with antialiasing filter		6.1		μA
IddULP	Supply current in ultralow-power mode	FS = ±8 g ODR = 1.6 Hz, BW = ODR/2		0.47		μA
Idd_PD	Supply current in power-down			20		nA
V <sub>IH</sub>	Digital high-level input voltage		0.7*Vdd_IO			V
V <sub>IL</sub>	Digital low-level input voltage				0.3*Vdd_IO	V
V <sub>OH</sub>	Digital high-level output voltage	I <sub>OH</sub> = 4 mA <sup>(3)</sup>	Vdd_IO - 0.2			V
V <sub>OL</sub>	Digital low-level output voltage	I <sub>OL</sub> = 4 mA <sup>(3)</sup>			0.2	V

1. Typical specifications are not guaranteed.

2. It is possible to remove Vdd, maintaining Vdd\_IO without blocking the communication busses. In this condition the measurement chain is powered off.

3. 4 mA is the maximum driving capability, that is, the maximum DC current that can be sourced/sunk by the digital pin in order to guarantee the correct digital output voltage levels V<sub>OH</sub> and V<sub>OL</sub>.

## 2.3 Temperature sensor characteristics

@ Vdd = 1.8 V, T = 25°C unless otherwise noted.

**Table 4. Temperature sensor characteristics**

Symbol	Parameter	Min.	Typ. <sup>(1)</sup>	Max.	Unit
Top	Operating temperature range	-40		+85	°C
Toff	Temperature offset <sup>(2)</sup>	-15		+15	°C
TSDr	Temperature sensor output change vs. temperature		0.045 <sup>(3)</sup>		°C/LSB
TODR	Temperature refresh rate		ODR		Hz

1. Typical specifications are not guaranteed.

2. The output of the temperature sensor is 0 LSB (typ.) at 25°C.

3. 12-bit resolution.

## 2.4 Communication interface characteristics

### 2.4.1 SPI - serial peripheral interface

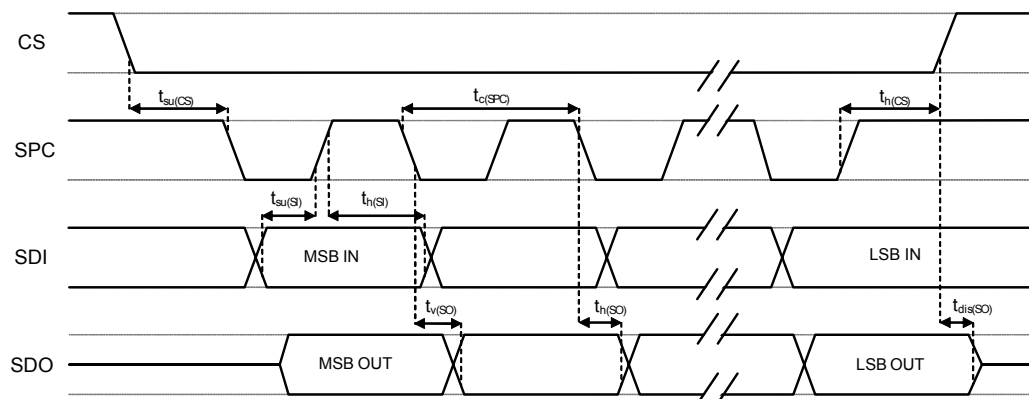
Subject to general operating conditions for Vdd and Top.

**Table 5. SPI slave timing values**

Symbol	Parameter	Value <sup>(1)</sup>		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	40		
$t_{su(SI)}$	SDI input setup time	12		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

**Figure 3. SPI slave timing diagram**



**Note:** Measurement points are done at  $0.3 \cdot V_{dd\_IO}$  and  $0.7 \cdot V_{dd\_IO}$  for both input and output ports.

## 2.4.2 I<sup>2</sup>C - inter-IC control interface

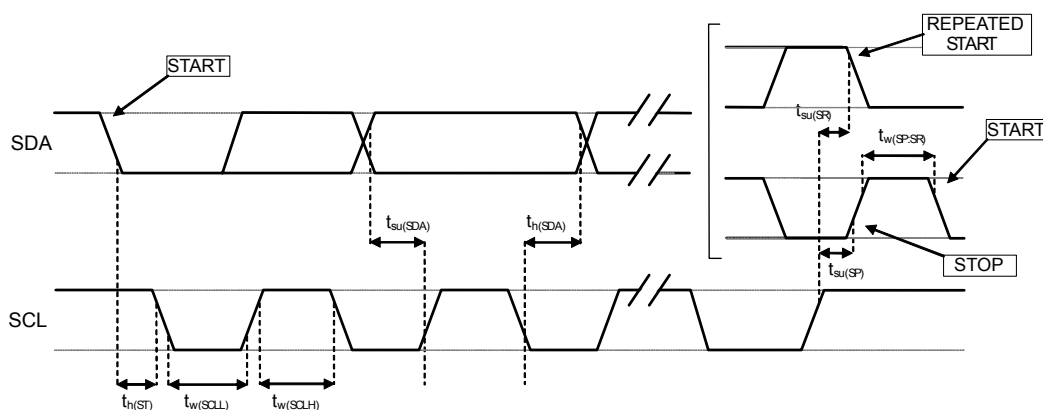
Subject to general operating conditions for V<sub>dd</sub> and Top.

**Table 6. I<sup>2</sup>C slave timing values**

Symbol	Parameter	I <sup>2</sup> C fast mode <sup>(1)(2)</sup>		I <sup>2</sup> C fast mode plus <sup>(1)(2)</sup>		Unit
		Min	Max	Min	Max	
f <sub>(SCL)</sub>	SCL clock frequency	0	400	0	1000	kHz
t <sub>w(SCLL)</sub>	SCL clock low time	1.3		0.5		μs
t <sub>w(SCLH)</sub>	SCL clock high time	0.6		0.26		
t <sub>su(SDA)</sub>	SDA setup time	100		50		ns
t <sub>h(SDA)</sub>	SDA data hold time	0	0.9	0		μs
t <sub>h(ST)</sub>	START/REPEATED START condition hold time	0.6		0.26		
t <sub>su(SR)</sub>	REPEATED START condition setup time	0.6		0.26		
t <sub>su(SP)</sub>	STOP condition setup time	0.6		0.26		
t <sub>w(SP:SR)</sub>	Bus free time between STOP and START condition	1.3		0.5		
	Data valid time		0.9		0.45	
	Data valid acknowledge time		0.9		0.45	
C <sub>B</sub>	Capacitive load for each bus line		400		550	pF

1. Data based on standard I<sup>2</sup>C protocol requirement, not tested in production.
2. Data for I<sup>2</sup>C fast mode and I<sup>2</sup>C fast mode plus have been validated by characterization, not tested in production.

**Figure 4. I<sup>2</sup>C slave timing diagram**



**Note:** Measurement points are done at 0.3·V<sub>dd\_IO</sub> and 0.7·V<sub>dd\_IO</sub> for both ports.



## 2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 7. Absolute maximum ratings**

Symbol	Ratings	Maximum value	Unit
V <sub>dd</sub>	Supply voltage	-0.3 to +4.3	V
V <sub>dd_IO</sub>	I/O pins supply voltage	-0.3 to +4.3	V
V <sub>in</sub>	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to V <sub>dd_IO</sub> +0.3	V
A <sub>UNP</sub>	Acceleration (any axis, unpowered)	3000 g for 0.5 ms	g
		10000 g for 0.2 ms	g
T <sub>OP</sub>	Operating temperature range	-40 to +85	°C
T <sub>STG</sub>	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

**Note:** Supply voltage on any pin should never exceed 4.3 V.



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

## 3 Terminology and functionality

### 3.1 Terminology

#### 3.1.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 g acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so,  $\pm 1$  g acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

#### 3.1.2 Zero-g level offset

Zero-g level offset describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measures 0 g on the X-axis and 0 g on the Y-axis whereas the Z-axis measures 1 g. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from ideal value in this case is called zero-g level offset. Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-g level offset change vs. temperature".

### 3.2 Functionality

#### 3.2.1 Operating modes

The LIS2DU12 has three operating modes: normal, ultralow-power, and one-shot mode. In normal mode, an aggressive antialiasing filter is active regardless, but the overall supply current remains extraordinarily low (refer to Table 3).

#### 3.2.2 Single data conversion on-demand modes

The device features two single data conversion on-demand modes: one-shot triggered by the INT2 pin, and one-shot triggered by the I<sup>2</sup>C/SPI/I<sup>3</sup>C digital interface.

#### 3.2.3 Self-test

Self-test mode allows checking the sensor functionality without moving it, applying an actuation force to the sensor and simulating a definite input acceleration.

### 3.2.4 Activity/inactivity, Android stationary/motion detection functions

The activity/inactivity function recognizes the device's sleep state and allows reducing system power consumption.

When the activity/inactivity function is activated by setting the SLEEP\_ON bit in [WAKE\\_UP\\_THS \(1Ch\)](#), the device automatically goes to the inactivity output data rate selected by the INACT\_ODR[1:0] bits in register [CTRL4 \(13h\)](#).

With this feature the system may be efficiently switched from low-power mode to full performance depending on user-selectable positioning and acceleration events, thus ensuring power saving and flexibility.

The Android stationary/motion detection function only recognizes the device's sleep state.

When the Android stationary/motion detection function is activated by setting to a STATIONARY condition the INACT\_ODR[1:0] bits in register [CTRL4 \(13h\)](#), the device detects acceleration below a fixed threshold but does not change the ODR after sleep state detection.

The activity/inactivity recognition and Android stationary/motion detection functions are activated by writing the desired threshold in the [WAKE\\_UP\\_THS \(1Ch\)](#) register. The high-pass filter is automatically enabled.

If the device is in sleep (inactivity/stationary) mode, when at least one of the axes exceeds the threshold in [WAKE\\_UP\\_THS \(1Ch\)](#), the device goes into a sleep-to-wake state (as wake-up).

For the activity/inactivity function, the device, in a wake-up state, returns to the ODR before sleep state detection.

Activity/inactivity, Android stationary/motion detection threshold and duration can be configured in the following control registers:

[WAKE\\_UP\\_THS \(1Ch\)](#)

[WAKE\\_UP\\_DUR \(1Dh\)](#)

### 3.2.5 High tap/double-tap user configurability

The device embeds the possibility to select the following parameters:

- single axis or multiple axes in [TAP\\_THS\\_Z \(1Ah\)](#)
- axis priority in [TAP\\_THS\\_Y \(19h\)](#)
- threshold value of each axis in [TAP\\_THS\\_X \(18h\)](#), [TAP\\_THS\\_Y \(19h\)](#), and [TAP\\_THS\\_Z \(1Ah\)](#)
- max time threshold between two consecutive taps for double-tap recognition, min time threshold between two consecutive taps to detect a new tap event in [INT\\_DUR \(1Bh\)](#)

### 3.2.6 Interrupt event recognition

The device may be configured to generate interrupt signals coming from an independent inertial wake-up/free-fall event or from the position of the device itself. Thresholds and timing of this interrupt generator are programmable by the end user in runtime.

Automatic programmable sleep-to-wake-up and return-to-sleep functions are also available for enhanced power saving.

The device interrupts signal can behave as:

- Free-fall: 3-axis subthreshold recognition;
- Wake-up: axis recognition;
- Wake-to-sleep: change of state recognition active-sleep (also known as activity-inactivity);
- 6D and 4D orientation detection: change of position recognition;
- Tap-tap: single, double, axis and sign recognition.

All these functions are parallel but during sleep it is not possible to recognize a tap-tap event. All these signals can be driven to the two interrupt pins (INT1 and INT2) through registers [MD1\\_CFG \(1Fh\)](#) and [MD2\\_CFG \(20h\)](#).

All these functions are enabled by setting the INTERRUPTS\_ENABLE bit in register [INTERRUPT\\_CFG \(17h\)](#) to 1.

It is possible to configure the duration of the interrupt using the LIR and INT\_SHORT\_EN bits in [INTERRUPT\\_CFG \(17h\)](#) as shown in the following table.

**Table 8. Configuration of duration of interrupt**

LIR	INT_SHORT_EN	Interrupt type
0	0	Interrupt level mode
1	1	Interrupt latched mode

- Interrupt level mode: the interrupt signal goes high when an interrupt event occurs and is reset when the acceleration data fall below the threshold.
- Interrupt latched mode: the interrupt signal is the OR between the interrupt flags that are monitored on the INT1/INT2 pins. The interrupt signal goes high when interrupt event occurs and is reset when [ALL\\_INT\\_SRC \(24h\)](#) is read. The status flags inside the interrupt source registers are coherent with the behavior of the INT1/INT2 pins. The interrupt generator block is inhibited for 1 ODR after the interrupt event.

### 3.3 Sensing element

A proprietary process is used to create a surface micromachined accelerometer. The technology allows processing suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. In order to be compatible with the traditional packaging techniques, a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase of the plastic encapsulation. When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady-state the nominal value of the capacitors are a few pF and when an acceleration is applied, the maximum variation of the capacitive load is in the fF range.

### 3.4 IC interface

The complete measurement chain is composed of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage using an analog-to-digital converter.

The acceleration data may be accessed through an I<sup>2</sup>C/SPI/MIPI I3C<sup>®</sup> interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LIS2DU12 features a data-ready signal which indicates when a new set of measured acceleration data is available, thus simplifying data synchronization in the digital system that uses the device.

### 3.5 Factory calibration

The IC interface is factory-calibrated for sensitivity (So) and zero-g level offset.

The trim values are stored inside the device in nonvolatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during active operation. This allows using the device without further calibration. If an accidental write occurs in the registers where the trimming parameters are stored, the BOOT bit in [CTRL4 \(13h\)](#) can help to retrieve the correct trimming parameters from nonvolatile memory without the need to switch on/off the device. This bit is automatically reset at the end of the download operation. Setting this bit has no impact on the control registers.

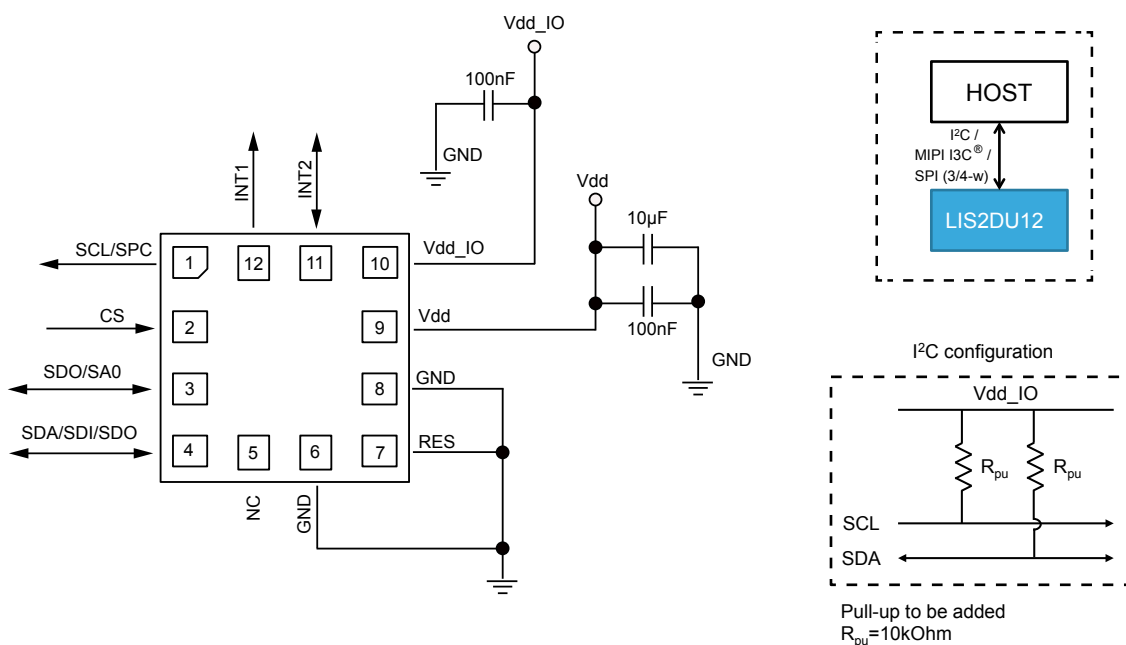
### 3.6 Temperature sensor

The temperature is available in [OUT\\_T\\_L \(2Eh\)](#), [OUT\\_T\\_H \(2Fh\)](#) stored as two's complement data, left-justified in 12-bit mode and duplicated in registers [TEMP\\_OUT\\_L \(30h\)](#) - [TEMP\\_OUT\\_H \(31h\)](#).

Refer to [Table 4. Temperature sensor characteristics](#) for the conversion factor.

## 4 Application hints

**Figure 5. LIS2DU12 electrical connections (top view)**



The device core is supplied through the Vdd line while the I/O pins are supplied through the Vdd\_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to Figure 5). It is possible to remove Vdd while maintaining Vdd\_IO without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data are selectable and accessible through the I<sup>2</sup>C/MIPI I3C<sup>®</sup> or SPI interfaces. When using the I<sup>2</sup>C, CS must be tied high (that is, connected to Vdd\_IO).

The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) can be completely programmed by the user through the I<sup>2</sup>C/MIPI I3C<sup>®</sup>/SPI interface.

**Table 9. Internal pin status**

Pin #	Name	Function	Pin status
1	SCL SPC	I <sup>2</sup> C/MIPI I3C <sup>®</sup> serial clock (SCL) SPI serial port clock (SPC)	Default: input without pull-up
2	CS	SPI/I <sup>2</sup> C/MIPI I3C <sup>®</sup> mode selection 1: SPI idle mode / I <sup>2</sup> C/MIPI I3C <sup>®</sup> enabled 0: SPI enabled / I2C/MIPI I3C <sup>®</sup> disabled	Default: input with internal pull-up
3	SDO SA0	Serial data output (SDO) I <sup>2</sup> C less significant bit of the device address (SA0)	Default: input with internal pull-up
4	SDA SDI SDO	I <sup>2</sup> C/MIPI I3C <sup>®</sup> serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)	Default: (SDA) input without pull-up
5	NC	Internally not connected. Can be tied to Vdd, Vdd_IO, or GND.	
6	GND	0 V supply	
7	RES	Connect to GND	
8	GND	0 V supply	
9	Vdd	Power supply	
10	Vdd_IO	Power supply for I/O pins	
11	INT2	Interrupt pin 2. Clock input when selected in single data conversion on demand.	Default: input with internal pull-down <sup>(1)(2)</sup>
12	INT1	Interrupt pin 1	Default: input with internal pull-down <sup>(3)</sup>

1. The INT2 pin is configured as "push-pull output forced to GND" as soon as it is configured with the interruption bits in the [CTRL3 \(12h\)](#) and [MD2\\_CFG \(20h\)](#) registers.
2. In order to disable the internal pull-down on the INT2 pin, write 1 to the PD\_DIS\_INT2 bit in [MD2\\_CFG \(20h\)](#).
3. The INT1 pin is configured as "push-pull output forced to GND" as soon as it is configured with interruption bits in the [CTRL2 \(11h\)](#) and [MD1\\_CFG \(1Fh\)](#) registers. The internal pull-down can be disconnected by setting the PD\_DIS\_INT1 bit of register [IF\\_CTRL \(0Eh\)](#) to 1. When this is done, the INT1 pin needs to be externally biased. If INT1 = Vdd, only the SPI and I3C interfaces are available. If INT1 = GND, then the I<sup>2</sup>C, I3C and SPI interfaces are active.

## 5 Digital main blocks

### 5.1 FIFO

The LIS2DU12 embeds 128 slots of 12-bit FIFO data for each of the three output channels X, Y and Z of acceleration data and 12-bit FIFO data for temperature data. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

In order to maximize the amount of data collected in FIFO, it is possible to double the slots of FIFO data (from 128 to 256) by writing the FIFO\_DEPTH bit in [FIFO\\_CTRL \(15h\)](#) with 2X depth mode.

When this mode is enabled, the most significant 8 bits for each acceleration axis are stored in FIFO. Each FIFO data word contains data of two consecutive ODRs, the actual and the previous one. The temperature data is no longer stored in FIFO but is available in the [TEMP\\_OUT\\_L \(30h\)](#) and [TEMP\\_OUT\\_H \(31h\)](#) registers.

In high-resolution batch mode, accelerometer and temperature FIFO are stored in FIFO as 12 bits at ODR.

In 2X depth batch mode, each word contains two accelerometer data as 8 bits in FIFO at ODR/2.

The FIFO buffer can work according to six different modes:

- Bypass mode
- FIFO mode
- Continuous mode
- Continuous-to-FIFO mode
- Bypass-to-continuous
- Bypass-to-FIFO

Each mode is selected by the FIFO\_MODE[2:0] bits in the [FIFO\\_CTRL \(15h\)](#) register. A programmable FIFO watermark is selected in the [FIFO\\_WTM \(16h\)](#) register.

FIFO status is available in the [FIFO\\_STATUS1 \(26h\)](#) and [FIFO\\_STATUS2 \(27h\)](#) registers and can be used to generate dedicated interrupts on the INT1 and INT2 pins using the [CTRL2 \(11h\)](#) and [CTRL3 \(12h\)](#) registers.

The FTH bit in [FIFO\\_STATUS1 \(26h\)](#) register goes to 1 when the number of unread samples is greater than or equal to FTH[6:0] in [FIFO\\_WTM \(16h\)](#). If FTH[6:0] is equal to 0, the FTH bit in [FIFO\\_STATUS1 \(26h\)](#) goes to 0.

The FIFO\_OVR bit in [FIFO\\_STATUS1 \(26h\)](#) is equal to 1 if a FIFO sample is overwritten.

FSS[7:0] in [FIFO\\_STATUS2 \(27h\)](#) contains stored data levels of unread samples.

When FSS[7:0] is equal to 00000000, FIFO is empty. When FSS[7:0] is equal to 10000000, FIFO is full and the unread samples are 128.

#### 5.1.1 Bypass mode

In bypass mode [FIFO\\_CTRL \(15h\)](#) (FIFO\_MODE[2:0] = 000), the FIFO is not operational, no data is collected in FIFO memory, and it remains empty with only the actual sample available in the output registers.

Bypass mode is also used to reset the FIFO when in FIFO mode.

For each channel only the first address is used. When new data is available, the old data is overwritten.

#### 5.1.2 FIFO mode

In FIFO mode [FIFO\\_CTRL \(15h\)](#) (FIFO\_MODE[2:0] = 001) data from the output channels are stored in the FIFO memory until it is full. When 128 unread samples are stored in memory, data collecting is stopped.

To reset FIFO content, bypass mode should be selected by writing [FIFO\\_CTRL \(15h\)](#) (FIFO\_MODE[2:0]) to 000. After this reset command, it is possible to restart FIFO mode, writing [FIFO\\_CTRL \(15h\)](#) (FIFO\_MODE[2:0]) to 001.

### 5.1.3 Continuous mode

Continuous mode **FIFO\_CTRL (15h)** (**FIFO\_MODE[2:0] = 110**) provides a continuous FIFO update: when 128 unread samples are stored in memory, as new data arrives, the oldest data is discarded and overwritten by the newer.

A FIFO threshold flag **FIFO\_FTH** bit in **FIFO\_STATUS1 (26h)** is asserted when the number of unread samples in FIFO is greater than or equal to **FTH[6:0]** in **FIFO\_WTM (16h)**.

It is possible to route the **FTH** bit to the **INT1** pin by writing the **INT1\_F\_FTH** bit to 1 in register **CTRL2 (11h)** or to the **INT2** pin by writing the **INT2\_F\_FTH** bit to 1 in register **CTRL3 (12h)**.

If an overrun occurs, the oldest sample in FIFO is overwritten and the **FIFO\_OVR** flag in **FIFO\_STATUS1 (26h)** is asserted.

### 5.1.4 Continuous-to-FIFO mode

In continuous-to-FIFO mode **FIFO\_MODE[2:0] = 011** in the **FIFO\_CTRL (15h)** register, FIFO operates in continuous mode and FIFO mode starts upon an edge trigger event. When the FIFO is full, data collecting is stopped. The trigger event could be single or double-tap, wake-up, free-fall, 6D interrupt or any combination of these events, but every interrupt has to be routed to the corresponding pin to be used as a trigger.

### 5.1.5 Bypass-to-continuous mode

In bypass-to-continuous mode **FIFO\_CTRL (15h)** (**FIFO\_MODE[2:0] = 100**), data measurement storage inside FIFO starts in continuous mode upon an edge trigger event.

The trigger event could be single or double-tap, wake-up, free-fall, 6D interrupt, or any combination of these events, but every interrupt has to be routed to the corresponding pin to be used as a trigger.

The sample that generated the trigger is available in FIFO.

### 5.1.6 Bypass-to-FIFO

In bypass-to-FIFO mode **FIFO\_CTRL (15h)** (**FIFO\_MODE[2:0] = 111**), data measurement storage inside FIFO operates in FIFO mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

The trigger event could be single or double-tap, wake-up, free-fall, 6D interrupt, or any combination of these events, but every interrupt has to be routed to the corresponding pin to be used as a trigger.

The sample that generated the trigger is available in FIFO.

### 5.1.7 Output data read sequence from FIFO

Automatic address increment is provided to minimize interface transfer.

In high-resolution batching mode, if both the accelerometer and temperature data are read from FIFO, a read operation is automatically performed from 8 output registers for every FIFO word (**OUT\_X\_L (28h)** - **OUT\_T\_H (2Fh)**).

If only accelerometer data are read from FIFO, a read operation is automatically performed from 6 output registers for every FIFO word, skipping temperature data (**OUT\_X\_L (28h)** - **OUT\_Z\_H (2Dh)**). The **ROUNDING\_XYZ** bit in the **FIFO\_CTRL (15h)** register must be written to enable this rounding of the read address.

In 2X depth mode, all FIFO words can be read in a single interface transfer from 6 output registers (**OUT\_X\_L (28h)** - **OUT\_Z\_H (2Dh)**). In this case, the rounding of the read address is automatically enabled.

If the **IF\_ADD\_INC** bit of register **CTRL1 (10h)** is set to 1, all FIFO words can be read in a single interface transfer. Different read modes using a single interface transfer supported by the LIS2DU12 are:

- **FIFO\_STATUS\_2** register + N\* **FIFO\_WORDS**
- **FIFO\_STATUS\_1** register + **FIFO\_STATUS\_2** register + N\* **FIFO\_WORDS**
- **TEMP\_OUT** + **FIFO\_STATUS\_1** register + **FIFO\_STATUS\_2** register + N\* **FIFO\_WORDS**



**5.1.8****FIFO empty condition**

When FIFO is emptied, a special value is used in order to recognize an empty condition and no duplicated samples are read.

In high-resolution batch mode, the least significant 4 bits of data read during an empty condition are 1111.

In 2X depth mode the empty condition corresponds to 7Fh code. The accelerometer data are assigned to 7Eh in order to discriminate the empty condition.

## 6 Digital interfaces

The registers embedded inside the LIS2DU12 may be accessed through both the I<sup>2</sup>C, MIPI I3C<sup>®</sup> and SPI serial interfaces. The latter may be software configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pins. To select/exploit the I<sup>2</sup>C/MIPI I3C<sup>®</sup> interface, the CS line must be tied high (that is, connected to Vdd\_IO).

**Table 10. Serial interface pin description**

Pin name	Pin description
CS	SPI/I <sup>2</sup> C/MIPI I3C <sup>®</sup> mode selection 1: SPI idle mode / I <sup>2</sup> C/MIPI I3C <sup>®</sup> enabled 0: SPI enabled / I <sup>2</sup> C/MIPI I3C <sup>®</sup> disabled
SCL	I <sup>2</sup> C/MIPI I3C <sup>®</sup> serial clock (SCL)
SPC	SPI serial port clock (SPC)
SDA	I <sup>2</sup> C/MIPI I3C <sup>®</sup> serial data (SDA)
SDI	SPI serial data input (SDI)
SDO	3-wire interface serial data output (SDO)
SA0	I <sup>2</sup> C address selection (SA0)
SDO	SPI serial data output (SDO)

### 6.1 I<sup>2</sup>C serial interface

The LIS2DU12 I<sup>2</sup>C is a bus slave. The I<sup>2</sup>C is employed to write data into registers whose content can also be read back.

The relevant I<sup>2</sup>C terminology is given in the table below.

**Table 11. I<sup>2</sup>C terminology**

Term	Description
Transmitter	The device that sends data to the bus
Receiver	The device that receives data from the bus
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I<sup>2</sup>C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd\_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I<sup>2</sup>C interface supports fast mode (400 kHz) I<sup>2</sup>C standards as well as fast mode plus (1000 kHz).

In order to disable the I<sup>2</sup>C block, **IF\_CTRL (0Eh)** (I2C\_DISABLE) = 1 must be set.

### 6.1.1 I<sup>2</sup>C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high to low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LIS2DU12 is 001100xb where the x bit is modified by the SA0/SDO pin in order to modify the device address. If the SA0/SDO pin is connected to the supply voltage, the address is 0011001b, otherwise if the SA0/SDO pin is connected to ground, the address is 0011000b. This solution permits to connect and address two different accelerometers to the same I<sup>2</sup>C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I<sup>2</sup>C embedded inside the LIS2DU12 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST), a slave address is sent. Once a slave acknowledge (SAK) has been returned, an 8-bit subaddress (SUB) is transmitted. The 7 LSb represents the actual register address while the CTRL1 (10h) (IF\_ADD\_INC) bit defines the address increment.

The slave address is completed with a read/write bit. If the bit is 1 (read), a repeated start (SR) condition must be issued after the two subaddress bytes. If the bit is 0 (write) the master transmits to the slave with direction unchanged. Table 12 explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

**Table 12. SAD+read/write patterns**

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	001100	0	1	00110001 (31h)
Write	001100	0	0	00110000 (30h)
Read	001100	1	1	00110011 (33h)
Write	001100	1	0	00110010 (32h)

**Table 13. Transfer when master is writing one byte to slave**

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

**Table 14. Transfer when master is writing multiple bytes to slave**

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

**Table 15. Transfer when master is receiving (reading) one byte of data from slave**

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

**Table 16. Transfer when master is receiving (reading) multiple bytes of data from slave**

Master	ST	SAD+ W		SUB		SR	SAD+ R		MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA	

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a slave receiver doesn't acknowledge the slave address (that is, it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low to high transition on the SDA line while the SCL line is high is defined as a stop condition. Each data transfer must be terminated by the generation of a stop (SP) condition.

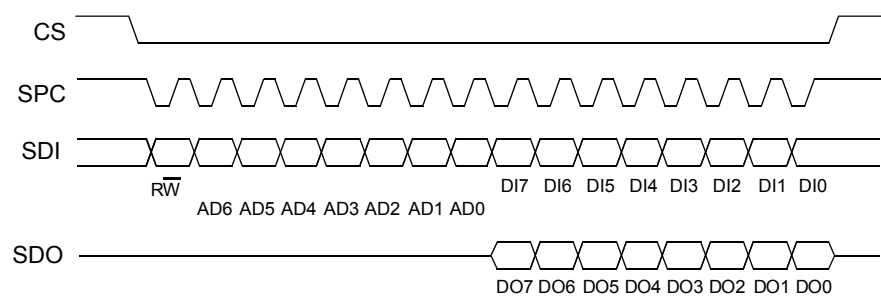
In the presented communication format, MAK is master acknowledge and NMAK is no master acknowledge.

## 6.2 SPI bus interface

The LIS2DU12 SPI is a bus slave. The SPI allows writing to and reading from the registers of the device.

The serial interface interacts with the application using 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

**Figure 6. Read and write protocol**



**CS** enables the serial port and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

**bit 0:**  $\overline{RW}$  bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives SDO at the start of bit 8.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

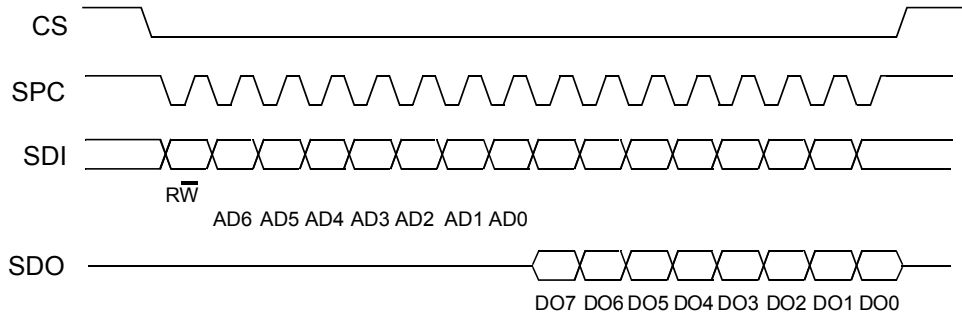
**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands additional blocks of 8 clock periods are added. When the **CTRL1 (10h)** (IF\_ADD\_INC) bit is 0, the address used to read/write data remains the same for every block. When the **CTRL1 (10h)** (IF\_ADD\_INC) bit is 1, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

## 6.2.1 SPI read

**Figure 7. SPI read protocol**



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

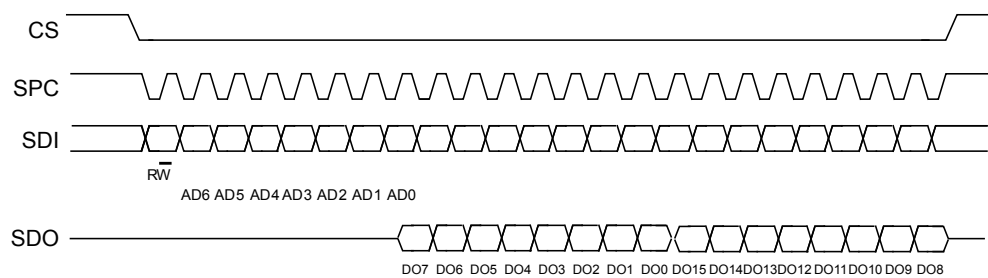
**bit 0:** READ bit. The value is 1.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

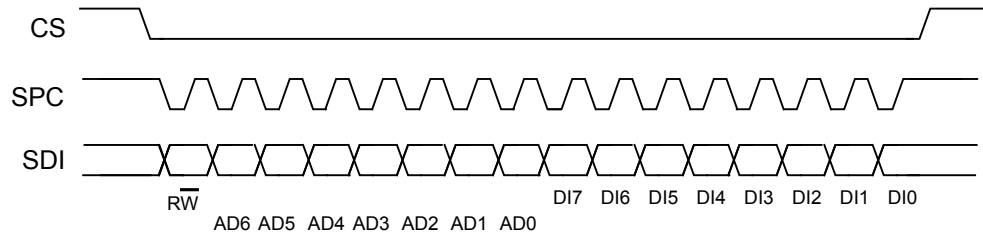
**bit 16-...** : data DO(...-8). Additional data in multiple byte reads.

**Figure 8. Multiple byte SPI read protocol (2-byte example)**



## 6.2.2 SPI write

**Figure 9. SPI write protocol**



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

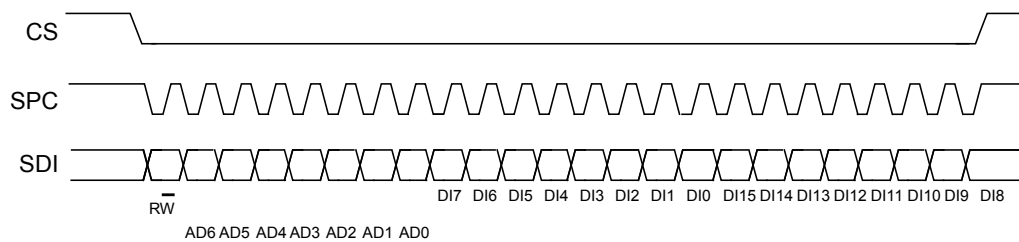
**bit 0:** WRITE bit. The value is 0.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

**bit 16-...** : data DI(...-8). Additional data in multiple byte writes.

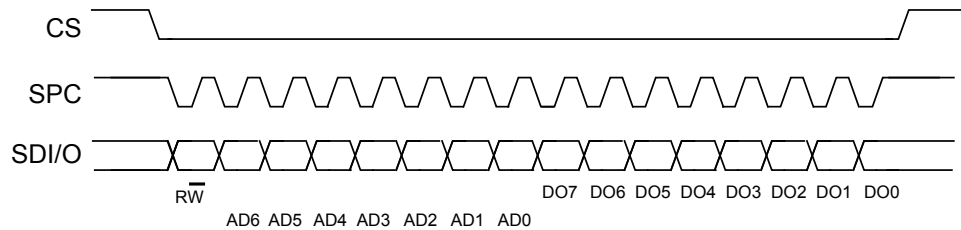
**Figure 10. Multiple byte SPI write protocol (2-byte example)**



### 6.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the **CTRL1 (10h)** (SIM) bit equal to 1 (SPI serial interface mode selection).

**Figure 11. SPI read protocol in 3-wire mode**



The SPI read command is performed with 16 clock pulses:

**bit 0:** READ bit. The value is 1.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

## 6.3 MIPI I3C<sup>®</sup> interface

### 6.3.1 MIPI I3C<sup>®</sup> slave interface

The LIS2DU12 interface includes an MIPI I3C<sup>®</sup> SDR only slave interface able to work up to 8 MHz of the SCL frequency (compliant with release 1.0 of the specification) with MIPI I3C<sup>®</sup> SDR embedded features:

- CCC command
- Direct CCC communication (SET and GET)
- Broadcast CCC communication
- Private communications
- Private read and write for single byte
- Multiple read and write
- In-band interrupt request

Refer to [Section 6.4: I<sup>2</sup>C/I3C coexistence in LIS2DU12](#) for details concerning the choice of the interface when powering up the device.



### 6.3.2 MIPI I3C® CCC supported commands

The list of MIPI I3C® CCC commands supported by the device is detailed in the following table.

**Table 17. MIPI I3C® CCC commands**

Command	Command code	Default	Description
SETDASA	0x87		Assign dynamic address using static address. Static address values are: 0x18/0x19 depending on SDO pin if I2C_SA1 bit in register IF_CTRL (0Eh) is equal to 0.
ENEC	0x80 / 0x00		Slave activity control (direct and broadcast)
DISEC	0x81 / 0x01		Slave activity control (direct and broadcast)
ENTAS0	0x82 / 0x02		Enter activity state (direct and broadcast)
ENTAS1	0x83 / 0x03		Enter activity state (direct and broadcast)
ENTAS2	0x84 / 0x04		Enter activity state (direct and broadcast)
ENTAS3	0x85 / 0x05		Enter activity state (direct and broadcast)
RSTDAA	0x86 / 0x06		Reset the assigned dynamic address (direct and broadcast)
SETMWL	0x89 / 0x08		Define maximum write length during private write (direct and broadcast)
SETMRL	0x8A / 0x09		Define maximum read length during private read (direct and broadcast)
SETNEWDA	0x88		Change dynamic address
GETMWL	0x8B	0x00 0x08 (2 byte)	Get maximum write length during private write
GETMRL	0x8C	0x00 0x10 0x04 (3 byte)	Get maximum read length during private read
GETPID	0x8D	0x02 0x08 0x00 0x45 0x10 0x0B	Device ID register
GETBCR	0x8E	0x07 (1 byte)	Bus characteristics register
GETDCR	0x8F	0x41 default	MIPI I3C® device characteristics register
GETSTATUS	0x90	0x00 0x00 (2 byte)	Status register
GETMXDS	0x94	0x01 0x39 (2 byte)	Return max data speed

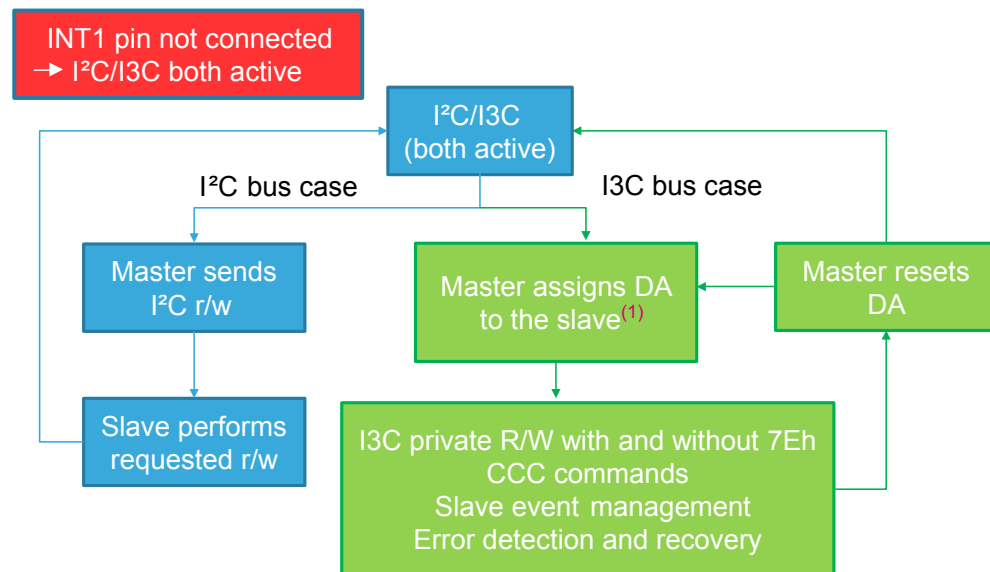
## 6.4 I<sup>2</sup>C/I<sup>3</sup>C coexistence in LIS2DU12

In the LIS2DU12, the SDA and SCL lines are common to both I<sup>2</sup>C and I<sup>3</sup>C. The I<sup>2</sup>C bus requires antispikes filters on the SDA and SCL pins that are not compatible with I<sup>3</sup>C timing.

The device can be connected to both I<sup>2</sup>C and I<sup>3</sup>C or only to the I<sup>3</sup>C bus depending on the connection of the INT1 pin when the device is powered up:

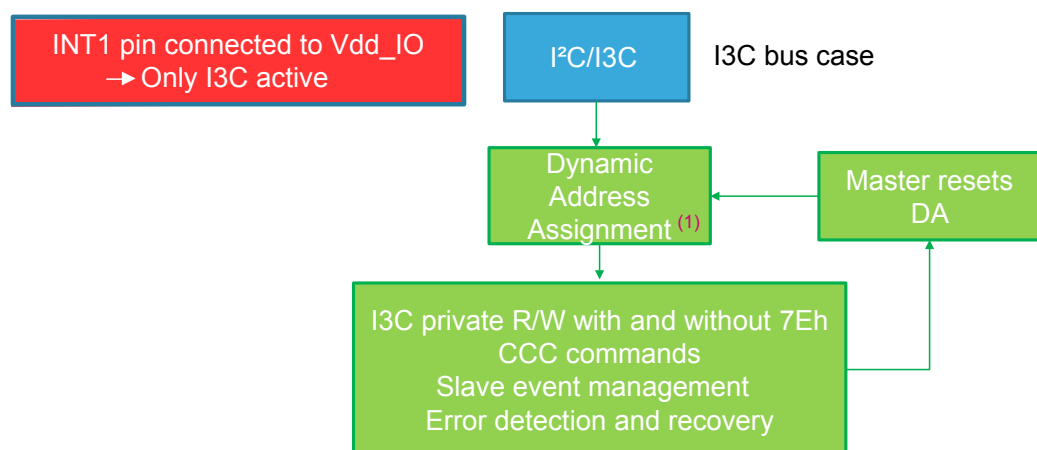
- INT1 pin floating (internal pull-down): I<sup>2</sup>C/I<sup>3</sup>C both active, see Figure 12
- INT1 pin connected to Vdd\_IO: only I<sup>3</sup>C active, see Figure 13

**Figure 12. I<sup>2</sup>C and I<sup>3</sup>C both active (INT1 pin not connected)**



1. Address assignment (SETDASA) must be performed with I<sup>2</sup>C fast mode plus timing. When the slave is addressed, the I<sup>2</sup>C slave is disabled and the timing is compatible with I<sup>3</sup>C specifications.

**Figure 13. Only I<sup>3</sup>C active (INT1 pin connected to Vdd\_IO)**



1. When the slave is I<sup>3</sup>C only, the I<sup>2</sup>C slave is always disabled. The address can be assigned using I<sup>3</sup>C SDR timing.

## 7 Register mapping

The table given below provides a list of the 8-bit registers embedded in the device and the corresponding addresses.

**Table 18. Register map**

Name	Type <sup>(1)</sup>	Register address		Default	Comment
		Hex	Binary		
IF_PU_CTRL	R/W	0C	00001100	00000000	
IF_CTRL	R/W	0E	00001110	00000000	
CTRL1	R/W	10	00010000	00000000	
CTRL2	R/W	11	00010001	00000000	
CTRL3	R/W	12	00010010	00000000	
CTRL4	R/W	13	00010011	00000000	
CTRL5	R/W	14	00010100	00000000	
FIFO_CTRL	R/W	15	00010101	00000000	
FIFO_WTM	R/W	16	00010110	00000000	
INTERRUPT_CFG	R/W	17	00010111	00000000	
TAP_THS_X	R/W	18	00011000	00000000	
TAP_THS_Y	R/W	19	00011001	00000000	
TAP_THS_Z	R/W	1A	00011010	00000000	
INT_DUR	R/W	1B	00011011	00000000	
WAKE_UP_THS	R/W	1C	00011100	00000000	
WAKE_UP_DUR	R/W	1D	00011101	00000000	
FREE_FALL	R/W	1E	00011110	00000000	
MD1_CFG	R/W	1F	00011111	00000000	
MD2_CFG	R/W	20	00100000	00000000	
WAKE_UP_SRC	R	21	00100001	00000000	
TAP_SRC	R	22	00100010	00000000	
SIXD_SRC	R	23	00100011	00000000	
ALL_INT_SRC	R	24	00100100	00000000	
STATUS	R	25	00100101	00000000	
FIFO_STATUS1	R	26	00100110	00000000	
FIFO_STATUS2	R	27	00100111	00000000	
OUT_X_L	R	28	00101000	00000000	
OUT_X_H	R	29	00101001	00000000	
OUT_Y_L	R	2A	00101010	00000000	
OUT_Y_H	R	2B	00101011	00000000	
OUT_Z_L	R	2C	00101100	00000000	
OUT_Z_H	R	2D	00101101	00000000	
OUT_T_L	R	2E	00101110	00000000	
OUT_T_H	R	2F	00101111	00000000	
TEMP_OUT_L	R	30	00110000	00000000	

Name	Type <sup>(1)</sup>	Register address		Default	Comment
		Hex	Binary		
TEMP_OUT_H	R	31	00110001	00000000	
WHO_AM_I	R	43	01000011	01000101	
ST_SIGN	R/W	58	01011000	110XXXXX	

1. R = read-only register, R/W = readable/writable register

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device. The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

## 8 Register description

### 8.1 IF\_PU\_CTRL (0Ch)

R/W

This register contains bits to control the pull-ups of SDO, SDA and CS, modifying a default state.

**Table 19. IF\_PU\_CTRL register**

SDO_PU_DIS	SDA_PU_EN	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	CS_PU_DIS	0 <sup>(1)</sup>	0 <sup>(1)</sup>
------------	-----------	------------------	------------------	------------------	-----------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 20. IF\_PU\_CTRL register description**

SDO_PU_DIS	If 1, disconnects the internal pull-up of the SDO pin.
SDA_PU_EN	If 1, connects the internal pull-up of the SDA pin.
CS_PU_DIS	If 1, disconnects the internal pull-up of the CS pin.

### 8.2 IF\_CTRL (0Eh)

R/W

**Table 21. IF\_CTRL register**

0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	PD_DIS_INT1	I3C_DISABLE	I2C_DISABLE
------------------	------------------	------------------	------------------	------------------	-------------	-------------	-------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 22. IF\_CTRL register description**

PD_DIS_INT1	If 1, pull-down of INT1 is disabled.
I3C_DISABLE	If 1, MIPI I3C® interface is disabled.
I2C_DISABLE	If 1, I²C interface is disabled.

### 8.3 CTRL1 (10h)

R/W

**Table 23. CTRL1 register**

PP_OD	SIM	SW_RESET	IF_ADD_INC	DRDY_PULSED	WU_X_EN	WU_Y_EN	WU_Z_EN
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**Table 24. CTRL1 register description**

PP_OD	Push-pull/open-drain mode for INT pins (0: INT pins in push-pull mode (default); 1: INT pins in open-drain mode)
SIM	SPI 3 or 4-wire mode (0: 4-wire SPI (default); 1: 3-wire SPI)
SW_RESET	Software reset, resets all CTRL registers to their default values. The software reset procedure has to be executed with the accelerometer in power-down mode.
IF_ADD_INC	Register address is automatically incremented during a multiple-byte access with a serial interface. (0: disabled (default); 1: enabled)
DRDY_PULSED	Enables pulsed data-ready mode (0: data-ready latched mode (returns to 0 only after reading over an interface) (default); 1: data-ready pulsed mode (the data-ready pulses are typ. 90 µs long))
WU_X_EN	Enables wake-up event detection status on X-axis. Default value: 0 (0: disabled; 1: enabled)
WU_Y_EN	Enables wake-up event detection status on Y-axis. Default value: 0 (0: disabled; 1: enabled)
WU_Z_EN	Enables wake-up event detection status on Z-axis. Default value: 0 (0: disabled; 1: enabled)

### 8.4 CTRL2 (11h)

R/W

**Table 25. CTRL2 register**

INT1_BOOT	INT1_F_FULL	INT1_F_FTH	INT1_F_OVR	INT1_DRDY	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>
-----------	-------------	------------	------------	-----------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 26. CTRL2 register description**

INT1_BOOT	Enables boot status on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_F_FULL	Enables FIFO full on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_F_FTH	Enables FIFO threshold interrupt on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_F_OVR	Enables overrun interrupt on INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_DRDY	Enables data-ready interrupt on INT1 pin. Default value: 0 (0: disabled; 1: enabled)

## 8.5 CTRL3 (12h)

R/W

**Table 27. CTRL3 register**

INT2_BOOT	INT2_F_FULL	INT2_F_FTH	INT2_F_OVR	INT2_DRDY	0 <sup>(1)</sup>	ST1	ST0
-----------	-------------	------------	------------	-----------	------------------	-----	-----

1. This bit must be set to 0 for the correct operation of the device.

**Table 28. CTRL3 register description**

INT2_BOOT	Enables boot status on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_F_FULL	Enables FIFO full on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_F_FTH	Enables FIFO threshold interrupt on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_F_OVR	Enables overrun interrupt on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY	Enables data-ready interrupt on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
ST[1:0]	These bits enable data acquisition during the self-test procedure.

## 8.6 CTRL4 (13h)

R/W

**Table 29. CTRL4 register**

INACT_ODR1	INACT_ODR0	BDU	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	SOC	BOOT
------------	------------	-----	------------------	------------------	------------------	-----	------

1. This bit must be set to 0 for the correct operation of the device.

**Table 30. CTRL4 register description**

INACT_ODR[1:0]	If the activity/inactivity function is enabled, then these bits select the accelerometer ODR during inactivity status, see Table 31.
BDU	Sensing chain block data update (0: output registers MSByte and LSByte independent continuous update (default); 1: output registers are not updated until MSByte and LSByte have both been read)
SOC	Start of conversion bit. When one-shot mode is enabled, this bit provides the start for the measurement. This bit is automatically cleared.
BOOT	Reboots memory content. Default value: 0 (0: normal mode; 1: reboot memory content) This bit is automatically cleared.

**Table 31. ODR frequency in inactivity state**

INACT_ODR1	INACT_ODR0	Frequency [Hz]
0	0	Stationary/motion detection: when selected, no ODR change is done if inactivity condition is detected
0	1	1.6
1	0	3
1	1	6

## 8.7 CTRL5 (14h)

R/W

**Table 32. CTRL5 register**

ODR3	ODR2	ODR1	ODR0	BW1	BW0	FS1	FS0
------	------	------	------	-----	-----	-----	-----

**Table 33. CTRL5 register description**

ODR[3:0]	ODR selection, see Table 34.
BW[1:0]	Selects the device bandwidth which is dependent on the ODR selected. The available bandwidths are ODR/2, ODR/4, ODR/8, and ODR/16 for ODR ≥ 50 Hz as shown in Table 35. For ODR < 50 Hz, refer to Table 36.
FS[1:0]	Sets the full scale, see Table 37.

**Table 34. Operating modes**

ODR[3:0]	Operating mode
0000	Power-down
0001	1.6 Hz in ultralow-power mode
0010	3 Hz in ultralow-power mode
0011	6 Hz in ultralow-power mode
0100	6 Hz in normal mode
0101	12.5 Hz in normal mode
0110	25 Hz in normal mode
0111	50 Hz in normal mode
1000	100 Hz in normal mode
1001	200 Hz in normal mode
1010	400 Hz in normal mode
1011	800 Hz in normal mode
1110	One-shot using the INT2 pin
1111	One-shot using the interface



**Table 35. Bandwidth selection (ODR  $\geq$  50 Hz)**

ODR [Hz]	BW[1:0]	BW [Hz]	Settling time [samples to be discarded]
50	00	25	1
	01	12.5	2
	10	6	6
	11	3	14
100	00	50	1
	01	25	2
	10	12.5	6
	11	6	14
200	00	100	0
	01	50	2
	10	25	4
	11	12.5	14
400	00	200	0
	01	100	0
	10	50	4
	11	25	8
800	00	400	0
	01	200	0
	10	100	0
	11	50	1

**Table 36. Bandwidth selection (ODR < 50 Hz)**

ODR [Hz]	BW[1:0]	BW [Hz]	Settling time [samples to be discarded]
6	00	-	
	01	-	
	10	-	
	11	3	11
12.5	00	-	
	01	-	
	10	6	5
	11	3	11
25	00	-	
	01	12.5	1
	10	6	5
	11	3	11

**Table 37. Full-scale selection**

FS1	FS0	Full scale
0	0	$\pm 2\text{ g}$
0	1	$\pm 4\text{ g}$
1	0	$\pm 8\text{ g}$
1	1	$\pm 16\text{ g}$

## 8.8

### FIFO\_CTRL (15h)

R/W

ROUNDING_XYZ	FIFO_DEPTH	0 <sup>(1)</sup>	0 <sup>(1)</sup>	STOP_ON_FTH	FIFO_MODE2	FIFO_MODE1	FIFO_MODE0
--------------	------------	------------------	------------------	-------------	------------	------------	------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 38. FIFO\_CTRL register description**

ROUNDING_XYZ	This function is used to auto address the correct registers for a circular continuous read from <a href="#">OUT_X_L (28h)</a> to <a href="#">OUT_Z_H (2Dh)</a> .
FIFO_DEPTH	If 1, enables 2X FIFO.
STOP_ON_FTH	Sensing chain FIFO stop values memorization at threshold level. (0: FIFO depth is not limited (default); 1: FIFO depth is limited to threshold level)
FIFO_MODE[2:0]	Different FIFO modes are enabled as shown in <a href="#">Table 39</a> .

**Table 39. Selection of FIFO mode**

FIFO_MODE2	FIFO_MODE1	FIFO_MODE0	Mode
0	0	0	Bypass mode
0	0	1	FIFO mode: stops collecting data when FIFO is full
0	1	0	Reserved
0	1	1	Continuous-to-FIFO: stream mode until trigger is deasserted, then FIFO mode
1	0	0	Bypass-to-continuous: bypass mode until trigger is deasserted, then continuous mode
1	0	1	Reserved
1	1	0	Continuous mode: if the FIFO is full, the new sample overwrites the older sample.
1	1	1	Bypass-to-FIFO: bypass mode until trigger is deasserted, then FIFO mode

## 8.9 FIFO\_WTM (16h)

R/W

**Table 40. FIFO\_WTM register**

-	FTH6	FTH5	FTH4	FTH3	FTH2	FTH1	FTH0
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**Table 41. FIFO\_WTM register description**

FTH[6:0]	FIFO watermark threshold, maximum value is 127.
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## 8.10 INTERRUPT\_CFG (17h)

R/W

**Table 42. INTERRUPT\_CFG register**

-	INT_SHORT_EN	WAKE_THS_W	-	SLEEP_STATUS_ON_INT	H_LACTIVE	LIR	INTERRUPTS_ENABLE
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**Table 43. INTERRUPT\_CFG register description**

INT_SHORT_EN	In combination with the LIR bit, this bit allows selecting the desired interruption configuration (see <a href="#">Table 8</a> ).
WAKE_THS_W	Weight of 1 LSB of wake-up threshold. Default value: 0 (0: 1 LSB = $FS_{XL} / (2^6)$ ; 1: 1 LSB = $FS_{XL} / (2^8)$ )
SLEEP_STATUS_ON_INT	Sends the sleep status instead of sleep change to INT pins (only if INT1_SLEEP_CHANGE or INT2_SLEEP_CHANGE bits are enabled, respectively in registers <a href="#">MD1_CFG (1Fh)</a> and <a href="#">MD2_CFG (20h)</a> ).
H_LACTIVE	Interrupt active level (0: interrupts active-high (default); 1: Interrupts active-low)
LIR	In combination with the INT_SHORT_EN bit, this bit allows selecting the desired interrupt configuration (see <a href="#">Table 8</a> ).
INTERRUPTS_ENABLE	Enables basic interrupts (6D/4D, free-fall, wake-up, single/double tap, activity/inactivity). Default value: 0 (0: interrupt disabled; 1: interrupt enabled)

## 8.11 TAP\_THS\_X (18h)

R/W

**Table 44. TAP\_THS\_X register**

D4D_EN	D6D_THS1	D6D_THS0	TAP_THS_X_4	TAP_THS_X_3	TAP_THS_X_2	TAP_THS_X_1	TAP_THS_X_0
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**Table 45. TAP\_THS\_X register description**

D4D_EN	Portrait/landscape position detection and face-up/down position enabled (4D orientation)
D6D_THS[1:0]	Thresholds for D4D/D6D function (00: 80 degrees; 01: 70 degrees; 10: 60 degrees; 11: 50 degrees)
TAP_THS_X[4:0]	X-axis recognition threshold. 1 LSB: FS / (2 <sup>5</sup> ). Default value: 0

## 8.12 TAP\_THS\_Y (19h)

R/W

**Table 46. TAP\_THS\_Y register**

TAP_PRIORITY_2	TAP_PRIORITY_1	TAP_PRIORITY_0	TAP_THS_Y_4	TAP_THS_Y_3	TAP_THS_Y_2	TAP_THS_Y_1	TAP_THS_Y_0
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**Table 47. TAP\_THS\_Y register description**

TAP_PRIORITY_[2:0]	Selection of axis priority for TAP detection (see Table 48)
TAP_THS_Y[4:0]	Y-axis recognition threshold. 1 LSB: FS / (2 <sup>5</sup> ). Default value: 0

**Table 48. Selection of axis priority for tap detection**

TAP_PRIORITY_[2:0]	Max priority	Mid priority	Min priority
000	X	Y	Z
001	Y	X	Z
010	X	Z	Y
011	Z	Y	X
100	X	Y	Z
101	Y	Z	X
110	Z	X	Y
111	Z	Y	X

### 8.13 TAP\_THS\_Z (1Ah)

R/W

**Table 49. TAP\_THS\_Z register**

TAP_X_EN	TAP_Y_EN	TAP_Z_EN	TAP_THS_Z_4	TAP_THS_Z_3	TAP_THS_Z_2	TAP_THS_Z_1	TAP_THS_Z_0
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**Table 50. TAP\_THS\_Z register description**

TAP_{X,Y,Z}_EN	Enables tap recognition in {X,Y,Z} direction
TAP_THS_Z_[4:0]	Z-axis recognition threshold. 1 LSB: FS / (2 <sup>5</sup> ). Default value: 0

### 8.14 INT\_DUR (1Bh)

R/W

**Table 51. INT\_DUR register**

LATENCY3	LATENCY2	LATENCY1	LATENCY0	QUIET1	QUIET0	SHOCK1	SHOCK0
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**Table 52. INT\_DUR register description**

LATENCY[3:0]	Maximum time gap for double-tap recognition duration. Default value: 0000 which corresponds to 16 ODR_time Maximum time between two subsequent detected taps to determine a double-tap event (when double-tap recognition is enabled). 1 LSB: 32 ODR_time.
QUIET[1:0]	Expected quiet time after a tap detection. Default value: 00 which corresponds to 2 ODR_time Time after the first detected tap in which there must not be an overthreshold event. 1 LSB : 4 ODR_time.
SHOCK[1:0]	Maximum overthreshold event. Default value: 00 which corresponds to 4 ODR_time Maximum time for an overthreshold signal detection to be recognized as a tap event. 1 LSB : 8 ODR_time.

## 8.15 WAKE\_UP\_THS (1Ch)

R/W

**Table 53. WAKE\_UP\_THS register**

SINGLE_ DOUBLE_TAP	SLEEP_ ON	WK_THS5	WK_THS4	WK_THS3	WK_THS2	WK_THS1	WK_THS0
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**Table 54. WAKE\_UP\_THS register description**

SINGLE_DOUBLE_TAP	Enables single/double-tap event. Default value: 0 (0: only single-tap event enabled; 1: both single and double-tap events enabled)
SLEEP_ON	If 1, activity/inactivity function is enabled.
WK_THS[5:0]	Threshold for wake-up: 1 LSB weight depends on WAKE_THS_W in INTERRUPT_CFG (17h). Default value: 000000

## 8.16 WAKE\_UP\_DUR (1Dh)

R/W

**Table 55. WAKE\_UP\_DUR register**

FF_DUR5	WAKE_ DUR1	WAKE_ DUR0	0 <sup>(1)</sup>	SLEEP_ DUR3	SLEEP_ DUR2	SLEEP_ DUR1	SLEEP_ DUR0
---------	------------	------------	------------------	-------------	-------------	-------------	-------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 56. WAKE\_UP\_DUR register description**

FF_DUR5	Free-fall duration. Default value: 0 In conjunction with FF_DUR[4:0] in FREE_FALL (1Eh). 1 LSB: 1 ODR_time
WAKE_DUR[1:0]	Wake-up duration. Default value: 00 When the WU_DUR_X4 bit in register MD1_CFG (1Fh) is set to 0, 1 LSB of WAKE_DUR = 1 ODR_time, otherwise the following durations are selectable: (00: 3 ODR_time; 01: 7 ODR_time; 10: 11 ODR_time; 11: 15 ODR_time)
SLEEP_DUR[3:0]	Duration to go in sleep mode. Default value: 0000 which corresponds to 16 ODR_time 1 LSB: 512 ODR_time

## 8.17 FREE\_FALL (1Eh)

R/W

**Table 57. FREE\_FALL register**

FF_DUR4	FF_DUR3	FF_DUR2	FF_DUR1	FF_DUR0	FF_THS2	FF_THS1	FF_THS0
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**Table 58. FREE\_FALL register description**

FF_DUR[4:0]	Free-fall duration. Default value: 0 In conjunction with FF_DUR5 in <a href="#">WAKE_UP_DUR (1Dh)</a> 1 LSB: 1 ODR_time
FF_THS[2:0]	Free-fall threshold (000: 156 mg; 001: 219 mg; 010: 250 mg; 011: 312 mg; 100: 344 mg; 101: 406 mg; 110: 469 mg; 111: 500 mg)

## 8.18 MD1\_CFG (1Fh)

R/W

Each bit in this register enables a signal to be carried over INT1; the pin's output is the OR combination of the signals selected here and in register [CTRL2 \(11h\)](#).

**Table 59. MD1\_CFG register**

INT1_SLEEP_CHANGE	INT1_SINGLE_TAP	INT1_WU	INT1_FF	INT1_DOUBLE_TAP	INT1_6D	WU_DUR_X4	-
-------------------	-----------------	---------	---------	-----------------	---------	-----------	---

**Table 60. MD1\_CFG register description**

INT1_SLEEP_CHANGE	Enables sleep change (or sleep status, depending on SLEEP_STATUS_ON_INT bit) on the INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_SINGLE_TAP	Enables routing single-tap event to the INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_WU	Enables routing wake-up event to the INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_FF	Enables routing free-fall event to the INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_DOUBLE_TAP	Enables routing double-tap event to the INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_6D	Enables routing 6D recognition event to the INT1 pin. Default value: 0 (0: disabled; 1: enabled)
WU_DUR_X4	This bit is used to select the resolution of the WAKE_DUR[1:0] bits in register <a href="#">WAKE_UP_DUR (1Dh)</a> . Default value: 0

## 8.19 MD2\_CFG (20h)

R/W

Each bit in this register enables a signal to be carried over INT2; the pin's output is the OR combination of the signals selected here and in register CTRL3 (12h).

**Table 61. MD2\_CFG register**

INT2_SLEEP_CHANGE	INT2_SINGLE_TAP	INT2_WU	INT2_FF	INT2_DOUBLE_TAP	INT2_6D	PD_DIS_INT2	-
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**Table 62. MD2\_CFG register description**

INT2_SLEEP_CHANGE	Enables sleep change (or sleep status, depending on SLEEP_STATUS_ON_INT bit) on the INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_SINGLE_TAP	Enables routing single-tap event to the INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_WU	Enables routing wake-up event to the INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_FF	Enables routing free-fall event to the INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_DOUBLE_TAP	Enables routing the double-tap event to the INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_6D	Enables routing 6D recognition event to the INT2 pin. Default value: 0 (0: disabled; 1: enabled)
PD_DIS_INT2	If 1, disables pull-down of INT2 pin.

## 8.20 WAKE\_UP\_SRC (21h)

R

**Table 63. WAKE\_UP\_SRC register**

-	SLEEP_CHANGE_IA	FF_IA	SLEEP_STATE	WU_IA	X_WU	Y_WU	Z_WU
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**Table 64. WAKE\_UP\_SRC register description**

SLEEP_CHANGE_IA	Detection of change in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
FF_IA	Free-fall event detection status. Default value: 0 (0: free-fall event not detected; 1: free-fall event detected)
SLEEP_STATE	Sleep status bit. Default value: 0 (0: activity status; 1: inactivity status)
WU_IA	Wake-up event detection status. Default value: 0 (0: wake-up event not detected; 1: wake-up event detected)
X_WU	Wake-up event detection status on X-axis. Default value: 0 (0: wake-up event on X-axis not detected; 1: wake-up event on X-axis detected)
Y_WU	Wake-up event detection status on Y-axis. Default value: 0 (0: wake-up event on Y-axis not detected; 1: wake-up event on Y-axis detected)
Z_WU	Wake-up event detection status on Z-axis. Default value: 0 (0: wake-up event on Z-axis not detected; 1: wake-up event on Z-axis detected)



## 8.21 TAP\_SRC (22h)

R

**Table 65. TAP\_SRC register**

-	TAP_IA	SINGLE_TAP_IA	DOUBLE_TAP_IA	TAP_SIGN	X_TAP	Y_TAP	Z_TAP
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**Table 66. TAP\_SRC register description**

TAP_IA	Tap event detection status. Default: 0 (0: tap event not detected; 1: tap event detected)
SINGLE_TAP_IA	Single-tap event status. Default value: 0 (0: single-tap event not detected; 1: single-tap event detected)
DOUBLE_TAP_IA	Double-tap event detection status. Default value: 0 (0: double-tap event not detected; 1: double-tap event detected)
TAP_SIGN	Sign of acceleration detected by tap event. Default: 0 (0: positive sign of acceleration detected by tap event; 1: negative sign of acceleration detected by tap event)
X_TAP	Tap event detection status on X-axis. Default value: 0 (0: tap event on X-axis not detected; 1: tap event on X-axis detected)
Y_TAP	Tap event detection status on Y-axis. Default value: 0 (0: tap event on Y-axis not detected; 1: tap event on Y-axis detected)
Z_TAP	Tap event detection status on Z-axis. Default value: 0 (0: tap event on Z-axis not detected; 1: tap event on Z-axis detected)

## 8.22 SIXD\_SRC (23h)

R

**Table 67. SIXD\_SRC register**

	D6D_IA	ZH	ZL	YH	YL	XH	XL
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**Table 68. SIXD\_SRC register description**

D6D_IA	Source of change in 6D/4D orientation. Default value: 0 (0: change orientation not detected; 1: change orientation detected)
ZH	Z-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
ZL	Z-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
YH	Y-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over-threshold) detected)
YL	Y-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
XH	X-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
XL	X-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)

## 8.23 ALL\_INT\_SRC (24h)

R

**Table 69. ALL\_INT\_SRC register**

-	INT_GLOBAL	SLEEP_CHANGE_IA_ALL	D6D_IA_ALL	DOUBLE_TAP_ALL	SINGLE_TAP_ALL	WU_IA_ALL	FF_IA_ALL
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**Table 70. ALL\_INT\_SRC register description**

INT_GLOBAL	<p>This bit is 1 if one of the following events occur:</p> <ul style="list-style-type: none"> <li>• detection of change in activity/inactivity status</li> <li>• source of change in 6D/4D orientation</li> <li>• double-tap event status</li> <li>• single-tap event status</li> <li>• wake-up event detection status</li> <li>• free-fall event detection status</li> <li>• sleep event status</li> </ul>
SLEEP_CHANGE_IA_ALL	Detection of change in activity/inactivity status. Default value: 0 (0: change in status not detected; 1: change in status detected)
D6D_IA_ALL	Source of change in 6D/4D orientation. Default value: 0 (0: change in orientation not detected; 1: change in orientation detected)
DOUBLE_TAP_ALL	Double-tap event status. Default value: 0 (0: event not detected, 1: event detected)
SINGLE_TAP_ALL	Single-tap event status. Default value: 0 (0: event not detected, 1: event detected)
WU_IA_ALL	Wake-up event status. Default value: 0 (0: event not detected, 1: event detected)
FF_IA_ALL	Free-fall event status. Default value: 0 (0: event not detected, 1: event detected)

## 8.24 STATUS (25h)

R

**Table 71. STATUS register**

-	-	-	-	-	-	PD_STATUS	DRDY
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**Table 72. STATUS register description**

PD_STATUS	Monitors power-down.
DRDY	This bit is 1 when new accelerometer data is available and until the MSB of one of the output registers has been read.

## 8.25 FIFO\_STATUS1 (26h)

R

**Table 73. FIFO\_STATUS1 register**

FTH	FIFO_OVR	-	-	-	-	-	-
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**Table 74. FIFO\_STATUS1 register description**

FTH	FIFO watermark status. The watermark is set through bits FTH[6:0] in FIFO_WTM (16h). (0: FIFO filling is lower than WTM; 1: FIFO filling is equal to or higher than WTM)
FIFO_OVR	FIFO overrun status: equal to 1 if FIFO has overwritten data.

## 8.26 FIFO\_STATUS2 (27h)

R

**Table 75. FIFO\_STATUS2 register**

FSS7	FSS6	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0
------	------	------	------	------	------	------	------

**Table 76. FIFO\_STATUS2 register description**

FSS[7:0]	Number of unread data stored in FIFO
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## 8.27 OUT\_X\_L (28h)

R

**Table 77. OUT\_X\_L register**

OUTX7	OUTX6	OUTX5	OUTX4	OUTX3	OUTX2	OUTX1	OUTX0
-------	-------	-------	-------	-------	-------	-------	-------

**Table 78. OUT\_X\_L register description**

OUTX[7:0]	LSBs of X data output. The last four bits are always zero since the data is 12-bit.
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## 8.28 OUT\_X\_H (29h)

R

**Table 79. OUT\_X\_H register**

OUTX15	OUTX14	OUTX13	OUTX12	OUTX11	OUTX10	OUTX9	OUTX8
--------	--------	--------	--------	--------	--------	-------	-------

**Table 80. OUT\_X\_H register description**

OUTX[15:8]	MSBs of X data output
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## 8.29 OUT\_Y\_L (2Ah)

R

**Table 81. OUT\_Y\_L register**

OUTY7	OUTY6	OUTY5	OUTY4	OUTY3	OUTY2	OUTY1	OUTY0
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**Table 82. OUT\_Y\_L register description**

OUTY[7:0]	LSBs of Y data output. The last four bits are always zero since the data is 12-bit.
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## 8.30 OUT\_Y\_H (2Bh)

R

**Table 83. OUT\_Y\_H register**

OUTY15	OUTY14	OUTY13	OUTY12	OUTY11	OUTY10	OUTY9	OUTY8
--------	--------	--------	--------	--------	--------	-------	-------

**Table 84. OUT\_Y\_H register description**

OUTY[15:8]	MSBs of Y data output.
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## 8.31 OUT\_Z\_L (2Ch)

R

**Table 85. OUT\_Z\_L register**

OUTZ7	OUTZ6	OUTZ5	OUTZ4	OUTZ3	OUTZ2	OUTZ1	OUTZ0
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**Table 86. OUT\_Z\_L register description**

OUTZ[7:0]	LSBs of Z data output. The last four bits are always zero since the data is 12-bit.
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## 8.32 OUT\_Z\_H (2Dh)

R

**Table 87. OUT\_Z\_H register**

OUTZ15	OUTZ14	OUTZ13	OUTZ12	OUTZ11	OUTZ10	OUTZ9	OUTZ8
--------	--------	--------	--------	--------	--------	-------	-------

**Table 88. OUT\_Z\_H register description**

OUTZ[15:8]	MSBs of Z data output
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### 8.33 OUT\_T\_L (2Eh)

R

**Table 89. OUT\_T\_L register**

OUTT7	OUTT6	OUTT5	OUTT4	OUTT3	OUTT2	OUTT1	OUTT0
-------	-------	-------	-------	-------	-------	-------	-------

**Table 90. OUT\_T\_L register description**

OUTT[7:0]	LSBs of temperature data output. The last four bits are always zero since the data is 12-bit.
-----------	---

### 8.34 OUT\_T\_H (2Fh)

R

**Table 91. OUT\_T\_H register**

OUTT15	OUTT14	OUTT13	OUTT12	OUTT11	OUTT10	OUTT9	OUTT8
--------	--------	--------	--------	--------	--------	-------	-------

**Table 92. OUT\_T\_H register description**

OUTT[15:8]	MSBs of temperature data output
------------	---------------------------------

### 8.35 TEMP\_OUT\_L (30h)

R

**Table 93. TEMP\_OUT\_L register**

OUTT7	OUTT6	OUTT5	OUTT4	OUTT3	OUTT2	OUTT1	OUTT0
-------	-------	-------	-------	-------	-------	-------	-------

**Table 94. TEMP\_OUT\_L register description**

OUTT[7:0]	LSBs of temperature data output. The last four bits are always zero since the data is 12-bit.
-----------	---

### 8.36 TEMP\_OUT\_H (31h)

R

**Table 95. TEMP\_OUT\_H register**

OUTT15	OUTT14	OUTT13	OUTT12	OUTT11	OUTT10	OUTT9	OUTT8
--------	--------	--------	--------	--------	--------	-------	-------

**Table 96. TEMP\_OUT\_H register description**

OUTT[15:8]	MSBs of temperature data output
------------	---------------------------------

### 8.37 WHO\_AM\_I (43h)

This register is a read-only register. Its value is fixed at 45h.

**Table 97. WHO\_AM\_I register default values**

0	1	0	0	0	1	0	1
---	---	---	---	---	---	---	---

### 8.38 ST\_SIGN (58h)

R/W

**Table 98. ST\_SIGN register**

STSIGN2	STSIGN1	STSIGN0	Reserved <sup>(1)</sup>	Reserved <sup>(1)</sup>	Reserved <sup>(1)</sup>	Reserved <sup>(1)</sup>	Reserved <sup>(1)</sup>
---------	---------	---------	-------------------------	-------------------------	-------------------------	-------------------------	-------------------------

1. Bits marked as Reserved must not be changed.

**Table 99. ST\_SIGN register description**

STSIGN[2:0]	These bits set the sign of the self-test procedure. (110: positive sign (default); 001: negative sign)
-------------	---

## 9 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 9.1 Soldering information

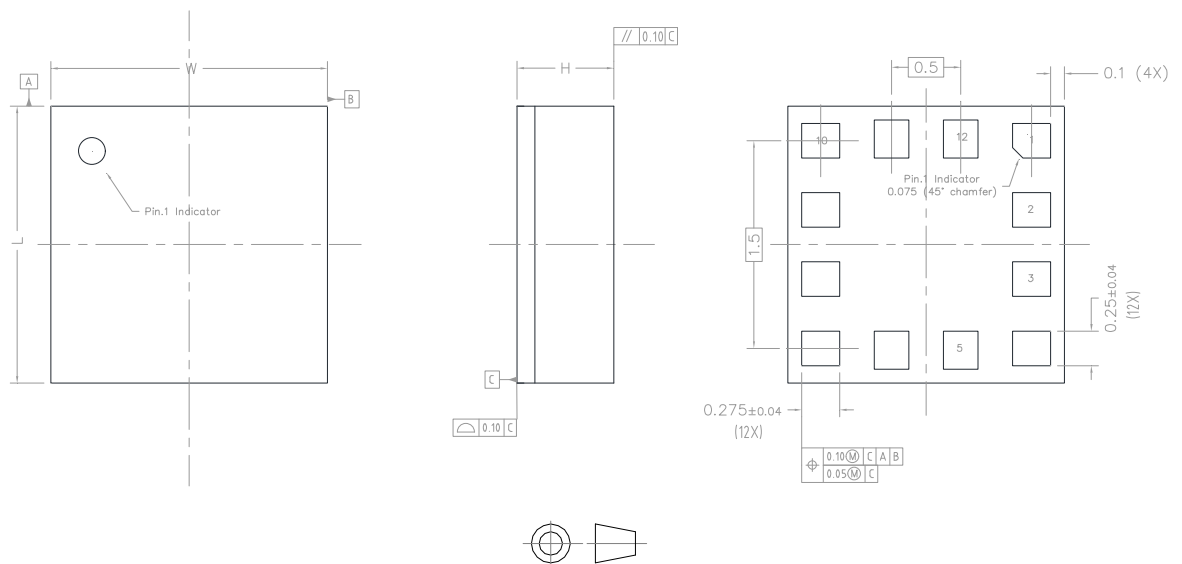
The LGA package is compliant with the **ECOPACK** and RoHS standard.

It is qualified for soldering heat resistance according to JEDEC J-STD-020.

For the land pattern and soldering recommendations, consult technical note **TN0018** available on [www.st.com](http://www.st.com).

### 9.2 LGA-12L package information

**Figure 14. LGA-12L 2.0 x 2.0 x 0.74 mm package outline and mechanical data**



Dimensions are in millimeter unless otherwise specified.  
General Tolerance is  $\pm 0.1$  mm unless otherwise specified.

#### OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2	$\pm 0.1$
Width [W]	2	$\pm 0.1$
Height [H]	0.74 MAX	/

DM00794797\_1



## Revision history

**Table 100. Document revision history**

Date	Version	Changes
09-Nov-2022	4	Minor textual updates
21-Aug-2024	5	Updated product resources on page 1 Updated Table 31. ODR frequency in inactivity state Updated description of the WAKE_DUR[1:0] bits in WAKE_UP_DUR (1Dh) Updated description of the WU_DUR_X4 bit in MD1_CFG (1Fh) Minor textual updates
24-Oct-2024	6	Updated <a href="#">Table 7. Absolute maximum ratings</a>

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