University of Washington

BEE331 Lab 1.2

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Voltage Limiter Circuits; Standard & Zener Diode

Design Objective

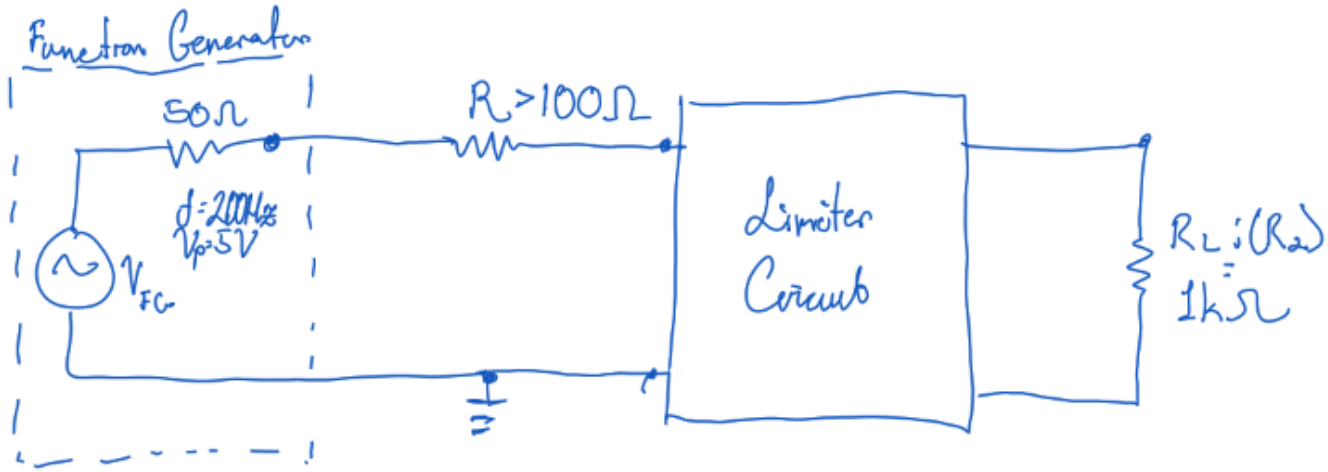
In this lab, we introduce ourselves to two voltage-limiting circuits. One built with standard diodes and the other built with Zener diodes., we characterise its function by the I-V curve.

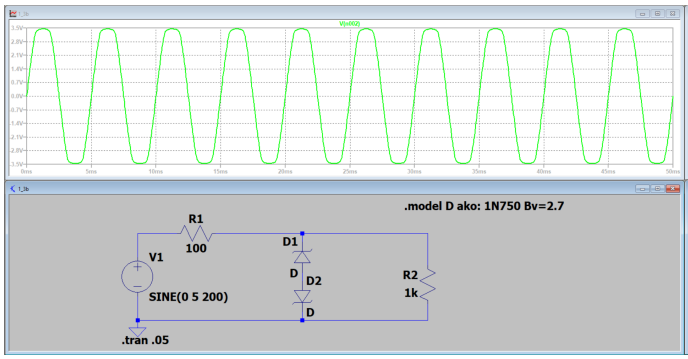
Circuit Design Outline

With a resistor of an arbitrary impedance greater than 100Ω ($R \geq 100\Omega$), and the natural impedance of the Function Generator in series ($R_{TOT} = R_{FG} + R \geq 150\Omega$), the designed High-Level Limiter Circuit is set in series to the resistor; through the function generator. Set the function generator @ f=200kHz and $V_P = 5V, 0.1V, 10V$ in High-Z impedance.

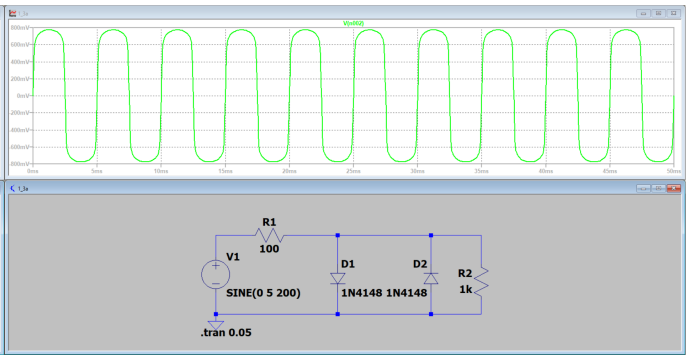
Figure 1: High-Level Limiter Circuit

(a) Rudimentary Generic Schematic of High-level Limiter Circuit

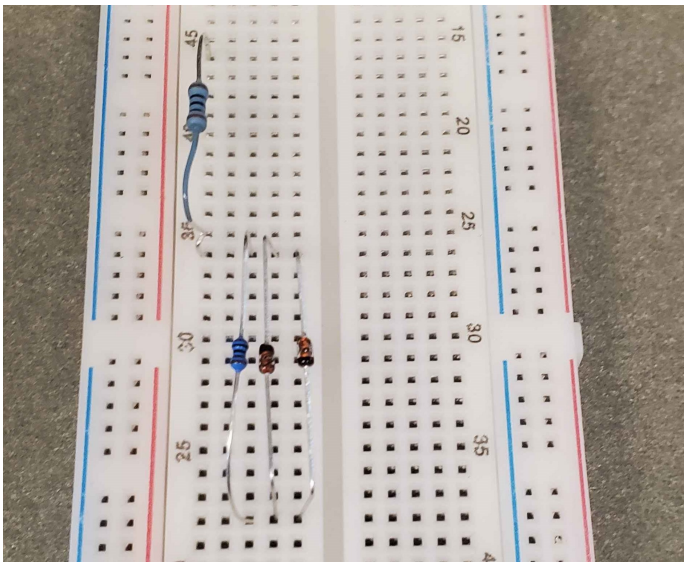




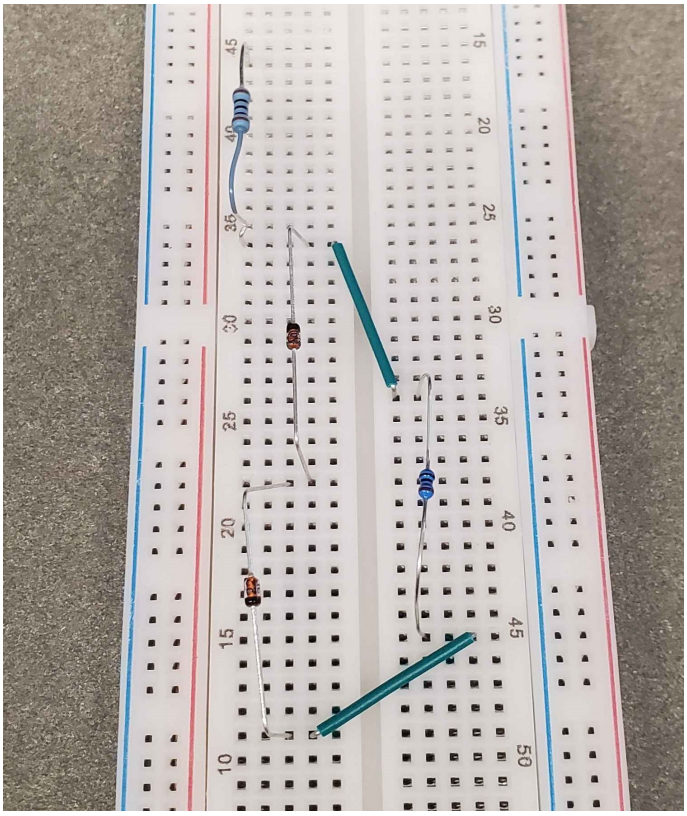
(b) LTSpice + Rudimentary Schematic Parallel Standard Diodes Circuit



(c) LTSpice + Rudimentary Schematic Series Opposing Zener Diodes Circuit



(d) Parallel Standard Diodes Circuit



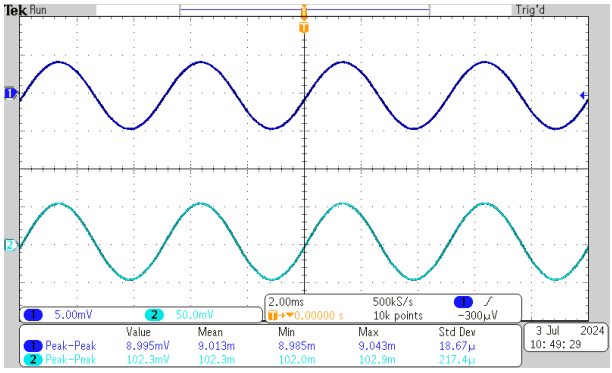
(e) Series Opposing Zener Diodes Circuit

Descriptions of Measurements & Calculations

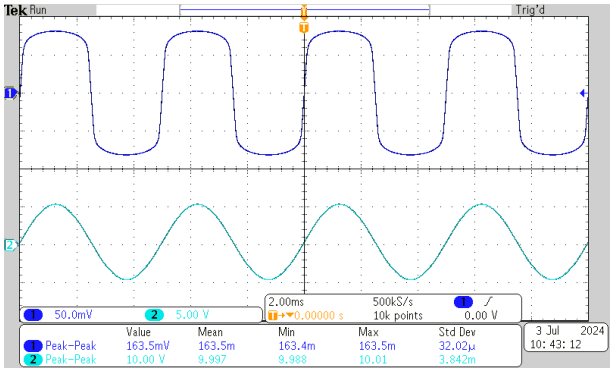
Given the default theoretical calculation for a Diode in forward-bias: $I_D = I_S(e^{\frac{V_D}{V_T}} - 1)$; the dataset is similar in-nature - not exact because the characteristics of this diode differs - from section 1.1 of the lab.
The characteristic of a *Zener* Diode is its relationship to $-V_D$, as I_D enters **Reverse-Breakdown** @ $-V_{Z0}$; the point of breakdown. Because of these characteristics, the Limiter-Circuits meet their respective "off" thresholds to logarithmically degrade the output voltage of V_o.

Figure 0: High-Limiter Circuit

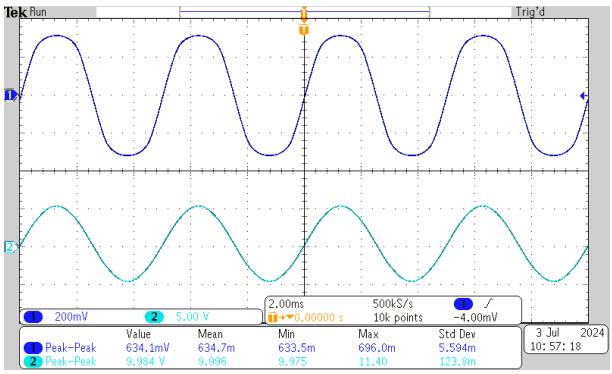
(a) Parallel RDD Circuit @ $0.1V_p$



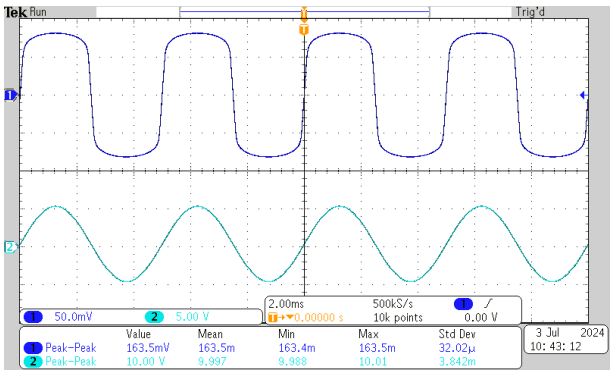
(b) Parallel RDD Circuit @ $10V_p$



(c) Series Opposing-Polarity Zener Diode Circuit @ $0.1V_p$



(d) Series Opposing-Polarity Zener Diode Circuit @ $10V_p$



Summary & Conclusions

Revealed in Figure RDD-Circuit 0A & 0B, the generated oscilloscope readings of the two periodic function do in-fact dampen @ V_{in} (CH2) greatly to V_{out} (CH1). It is similary in the Series D_Z circuit.

Discussion

- **i. Describe how each limiter circuit limits the input voltage based on the output waveform you measured. How are the limiter circuits 1 and 2 different?**

  The first limiter circuit reduces peak voltage showing the behavior of the exponential diodes. This makes the output wave more square than the input wave because it is limiting the input before it can start curving back down. [Reference Above]

- **ii. What is the effect of setting the *Load Impedance to High Z* mode for the function generator?**

  Forward-Bias: $I_D = I_S(e^{\frac{V_D}{V_T}} - 1)$; reference Figure 1b.

  The instrument will display less attenuation when producing the signal; so in ley, less of a impeded signal.

- **iii. What settings did you use in the oscilloscope in order to suppress noises in the output signals??**

  Forward-Bias: The characteristics of the I-V curve of a diode has current I_D exponentially rise towards a cut-off at the threshold, towards the C.V.D @ V_D.

  High-Fine, Auto-range, 50% auto-trigger, AC-Coupling.

- **iv. For the limiter Circuit 1, can you make the output signal the same as the input signal by changing** v_{peak}

  You should be able to make the output signal the same by staying in the region where both diodes are in an "off" state. This will cause the circuit to not be limited by current through the diodes.

Bibliography

Cited:

- Lab 1 Manual
- Sedra, Adel, and Kenneth Smith. Microelectronic Circuits. S.L., Oxford Univ Press Us, 2019.
- "How Do You Calculate, a Silicon Junction Diode with N = 1 Has v = 0.7 v al I = 1 MA. What Is the Voltage Drop at I=0.1 MA and I=10 MA.?" Quora, 2024, appliedmathematics.quora.com/How-to-calculate-A-silicon-junction-diode-with-n-1-has-v-0-7-V-al-I-1-mA-What-is-the-voltage-drop-at-I-0-1-mA-an?top_ans=223007030. Accessed 15 July 2024.

(a) Look at her, she's perfect.