# PROJECT COVER

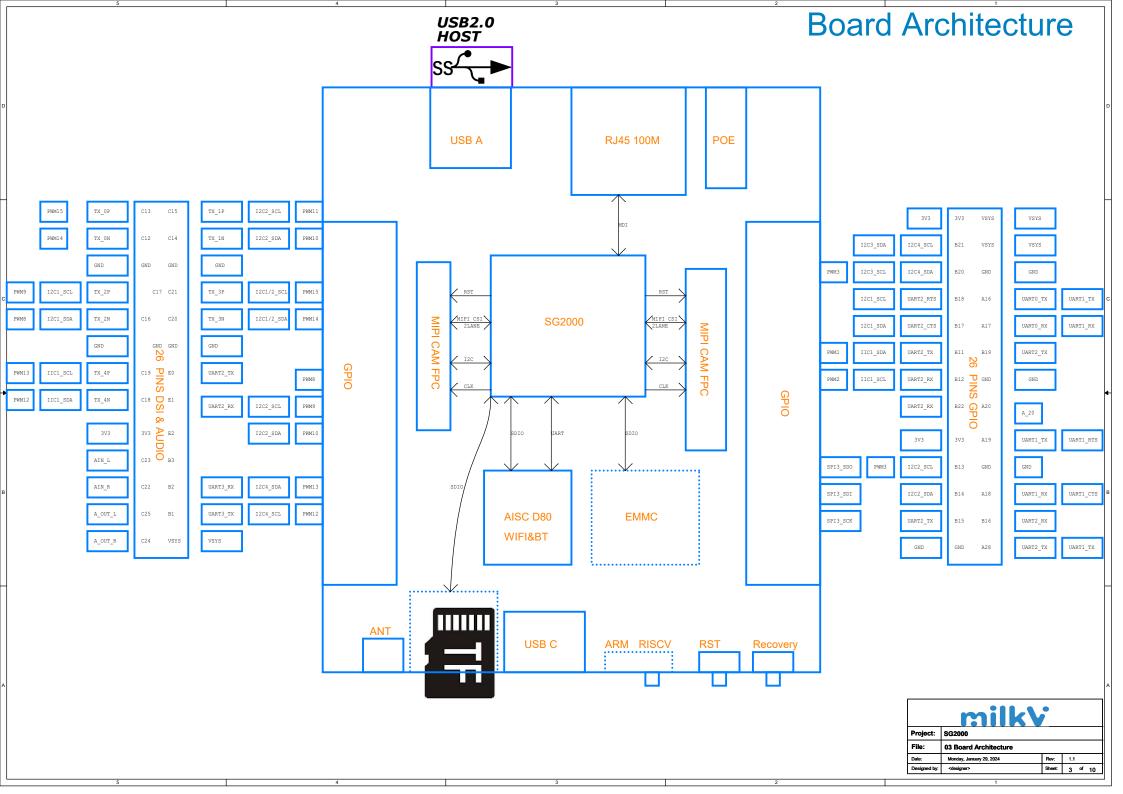
Board Name	DUO S
Board Version	V1.1
Designer	
Reviewed by	

milkV				
Project:	Project: SG2000			
File: 01 Project Cover				
Date:	Monday, January 29, 2024	Rev:	1.1	
Designed by:	<designer></designer>	Sheet:	1 of 10	

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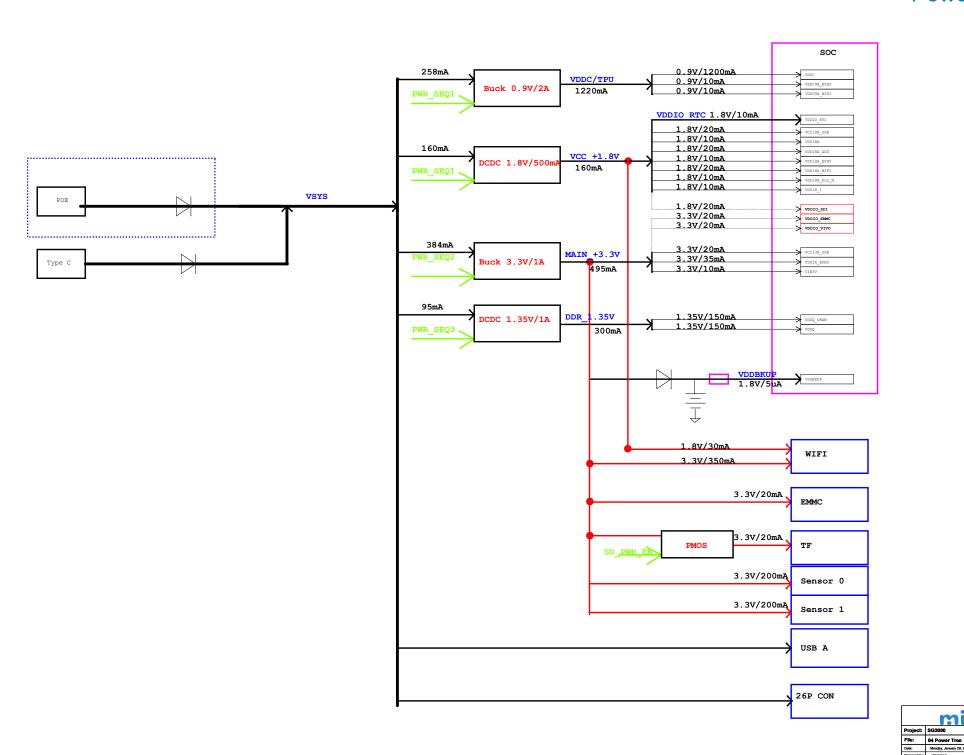
	milkV				
Project:	roject: SG2000				
File:	File: 02 Content				
Date:	Monday, January 29, 2024	Rev:	1.1		
Designed by:	<designer></designer>	Sheet:	2 <sup>of</sup> 10		
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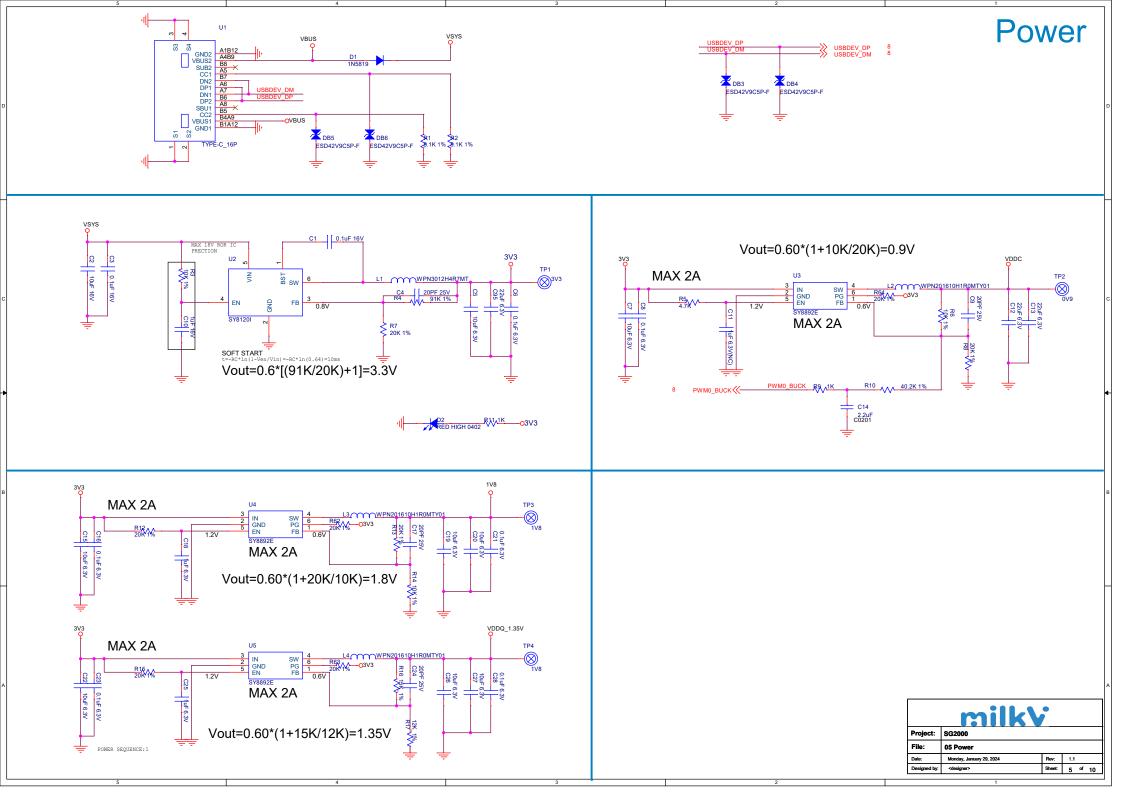


### **Power Tree**

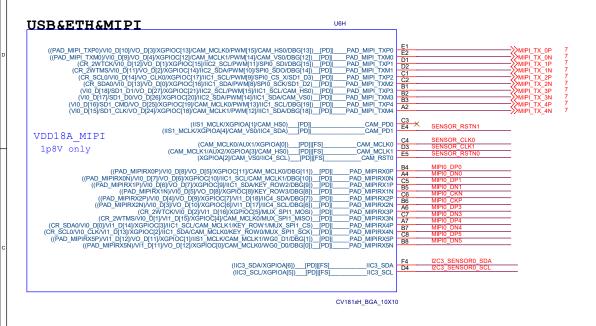
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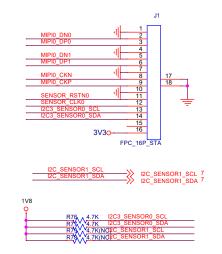
Monday, January 29, 2024

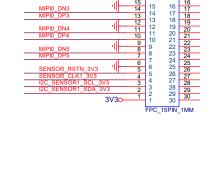




## SG2000 PART I

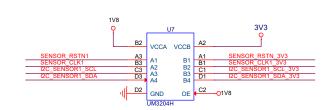






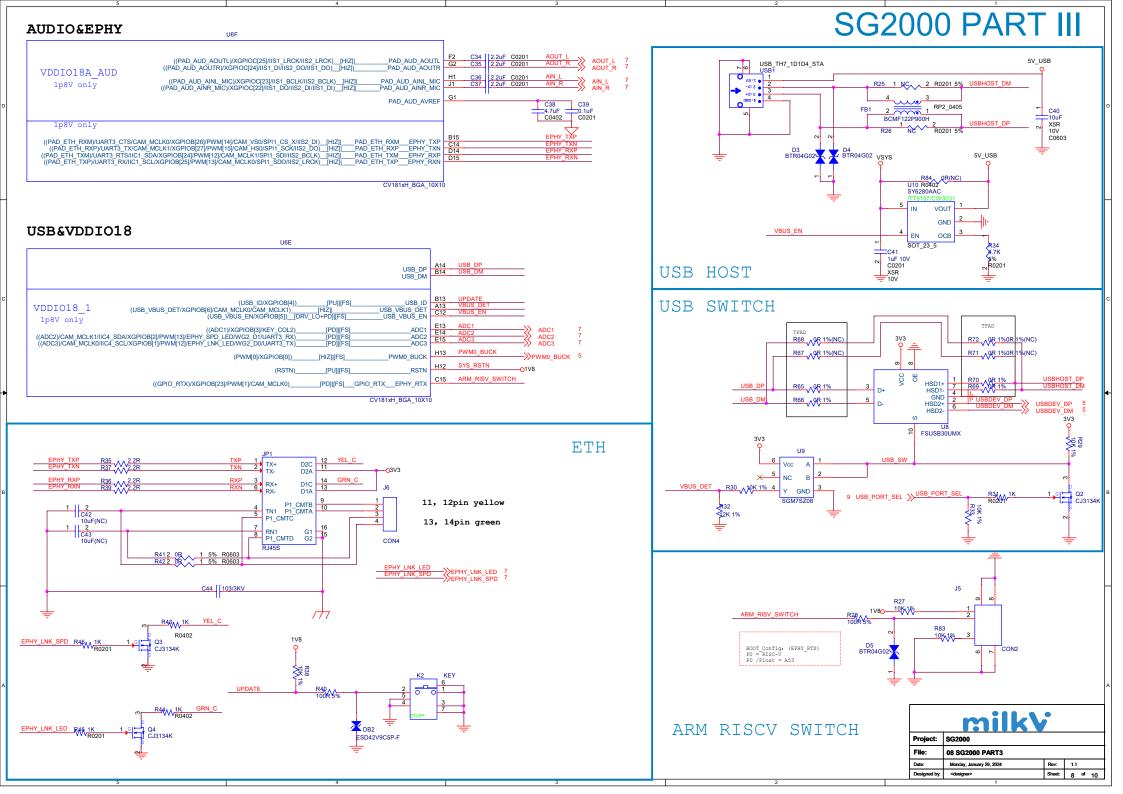
#### VDDIO\_SD1

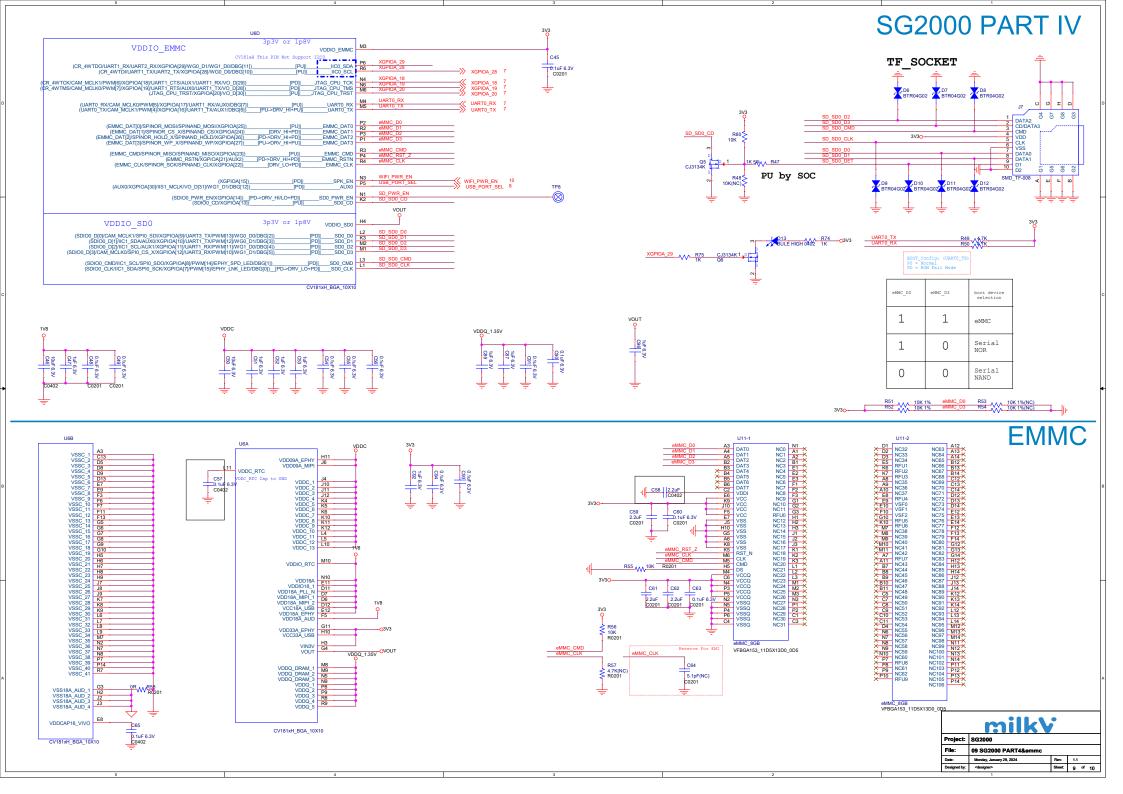




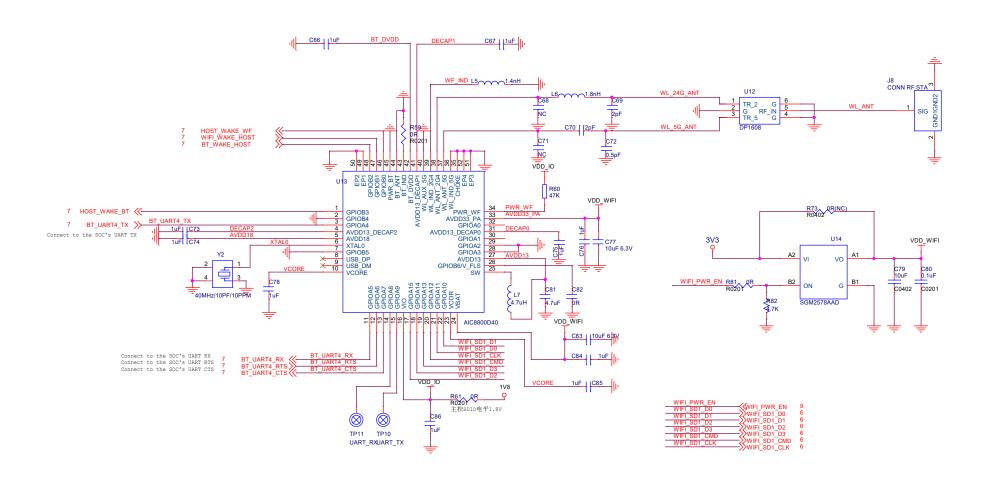
milkV					
Project: SG2000					
File: 06 SG2000 PART1					
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#### SG2000 PART II VDDIO RTC (PWR\_SEQ1/PWR\_GPIO[3])\_\_[PD->DRV+PD][[FS] (PWR\_SEQ2/PWR\_GPIO[4])\_\_[PD->DRV+PD][ (PWR\_SEQ3/PWR\_GPIO[5])\_\_[PD->DRV+PD][[FS] HOST\_WAKE\_WF 1p8V only PWR SEQ2 PWR SEQ3 (PWR\_WAKEUP0/PWR\_IR0/PWR\_UART0\_TX/PWR\_GPI0[6](PWR\_IIC\_SDA)/UART1\_TX/IIC4\_SCL/EPHY\_LNK\_LED/WG2\_D0) (PWR\_WAKEUP1/PWR\_IR1/PWR\_GPI0[7]/UART1\_TX/IIC4\_SCL/EPHY\_LNK\_LED/WG0\_D0) PWR WAKEUPO PWR\_WAKEUP1 PWR VBAT DET PWR\_VBAT\_DET C.I3134K (PWR\_GPIO[0]/UART2\_TX/PWR\_UART0\_RX/PWM[8])\_ [PD][[FS]\_ (PWR\_GPIO[1](PWRSAR1.VIN2)/UART2\_RX/EPHY\_LNK\_LED/PWM/9]/PWR\_IIC\_SCL/IIC2\_SCL/CR\_SDA0(PWR\_GPIO[2](PWRSAR.VIN1)/TEPHY\_SPD\_LED/PWM[10]/PWR\_IIC\_SDA/IIC2\_SDA/IC2\_ZWTCK PWR\_GPI01 PWR\_GPI02 ₹ DB1 (IIC2\_SDA/PWM[15]/PWR\_GPIO[13]/UART2\_TX/IIS1\_MCLK/IIS2\_MCLK/KEY\_COL3) (IIC2\_SCL/PWM[14]/PWR\_GPIO[12]/UART2\_RX/KEY\_COL2 I2C\_SENSOR1\_SDA I2C\_SENSOR1\_SCL ESD42V9C5P-F BT UART4 RX (UART2\_RX/PWM[10]/PWR\_UART1\_RX/PWR\_GPIO[16]/KEY\_COL3/UART4\_RX/IIS2\_DI/WG2\_D1) (UART2\_TX/PWM[11]/PWR\_UART1\_TX/PWR\_GPIO[14]/KEY\_ROW3/UART4\_TX/IIS2\_BCLK/WG2\_D0] UART2\_RX UART2 T BT UART4 TX (UART2\_CTS/PWM[9]/PWR\_GPIO[17]/KEY\_ROW1/UART4\_CTS/IIS2\_LRCK/WG1\_D1) (UART2\_RTS/PWM[8]/PWR\_GPIO[15]/KEY\_ROW0/UART4\_RTS/IIS2\_DO/WG1\_D0) UART2 CTS BT HART4 CTS UART2\_RTS HOST\_WAKE\_BT (CLK32K/AUX0/CR\_SCL0/PWR\_GPIO[10]/PWM[2]/KEY\_COL0/CAM\_MCLK0/DBG[0] HOST WAKE BT BT WAKE HOST (CLK25M/AUX1/CR\_2WTMS/PWR\_GPIO[11]/PWM[3]/KEY\_COL1/CAM\_MCLK1/DBG[1]) CLK25M PWR\_RSTN R22 4.7K (PWR\_RSTN)\_ PWR\_RSTN (PWR\_ON/PWR\_GPIO[9]/UART1\_RX/IIC4\_SDA/EPHY\_SPD\_LED/WG0\_D1)\_ EPHY LNK SPD (PWR\_BUTTON1/PWR\_GPIO[8](PWR\_IIC\_SCL)/UART1\_RX/IIC4\_SDA/EPHY\_SPD\_LED/WG2\_D1) PWR\_BUTTON1 XTAL\_XIN XTAL\_XOUT (PWR PTEST) [PD]|[FS]\_\_GPIO\_ZQ\_\_PAD ZQ XGPIOB\_20/I2C4\_SCL3V3O-((GPIO\_ZQ)/PWR\_GPIO[24]/PWM[2]) 3V/3 1V8 12C-SDA GND2 GPIO1 UART2-TX N14 GPIO2 GPIO3 **VDDBKUF VDDBKUP** PWM C29 RTC\_XIN RTC\_XOUT 0.1uF GPI05 GPI06 XGPIOB\_13/SPI3 SDO3V3O-GPI07 SPI-TXD GND4 GPI08 SPI-CLK SPI-CSN0 SPI-CSN1 GND1 CON26A VDDIO VIVO 3p3V or 1p8V (V12\_D[0]/V11\_D[0]/VO\_D[13]/XGPIOB[21]/RMII0\_TXCLK/IIC3\_SCL/WG1\_D0/IIC4\_SDA)\_\_PD]\_ (V12\_D[1]/V11\_D[1]/V0\_D[14]/XGPIOB[20]/RMII0\_RXDV/IIC3\_SDA/PWM[3]/IIC4\_SCL\_\_[PD]\_ (V12\_D[2]/V11\_D[2]/V0\_D[15]/XGPIOB[18]/RMII0\_TXD1/IC4\_MCLK1/FWM[2]/UART2\_TX\_\_IFD]\_ (V12\_D[3]/V11\_D[3]/V0\_D[16]/XGPIOB[18]/RMII0\_TXD0/IIC1\_SCL/UART2\_RTS/CAM\_HS0)\_\_PD]\_ \_VIVO\_D1 (VI2\_D[4]/VI1\_D[4]/VO\_D[17]/XGPI0B[17]/RMII0 MDC/IIC1\_SDA/UART2\_CTS/CAM\_VS0]\_\_[PD]\_ (VI2\_D[5]/VI1\_D[5]/VO\_D[18]/XGPI0B[15]/RMII0\_RXD0/SPI3\_CS\_X/UART2\_RX/CAM\_HS0]\_\_[PD]\_ (VI2\_D[6]/VI1\_D[6]/VO\_D[19]/XGPI0B[15]/RMII0\_RXD0/SPI3\_CS\_X/UART2\_TX/CAM\_VS0]\_\_[PD]\_ (VI2\_D[7]/VI1\_D[7]/VO\_D[20]/XGPI0B[14]/RMII0\_RXD1/SPI3\_SD/IIC2\_SDA/CAM\_HS0]\_\_[PD]\_ VIVO\_D4 VIVO\_D5 VIVO\_D6 VIVO\_D7 (PWM(3)/VI \_D(8)/VO \_D(2)(1)XSPIOB(13)/RMII0 \_MOIO/SPI3 \_SDOIII(2 \_SCLICAM \_VS) \_ PDI \_ (PWM(2)/VI \_D(9)/VO \_D(2)/XSPIOB(12)/CAM \_MCLK/III(C \_SCLICATE \_RX \_PDI \_ (PWM(1)/VI \_ D(9)/VO \_D(2)/XSPIOB(11)/RMII0 \_RO(CAM \_MCLK/III(C \_SDAUART2 \_RX \_PDI \_ RX \_PDI \_ NO \_PDI VIVO D9 (VI2\_CLK/VI1\_CLK/VO\_CLK1/XGPIOB[22]/RMII0\_TXEN/CAM\_MCLK0/WG1\_D1/UART2\_RX)\_\_[PD]|\_\_\_\_VIVO\_CLK CV181xH\_BGA\_10X10 1/ 19 17 21 21 23 23 3V30 20 22 21 23 25 CON26A XGPIOA\_18 XGPIOA\_19 XGPIOA 20 XGPIOA 30 AOUT\_L AOUT\_R OSC\_SM2\_2D0X1D2 32.768KHz/12.5pF AIN\_L AIN\_R UART0\_TX UART0\_RX MIPI\_TX\_0P MIPI\_TX\_0N MIPI\_TX\_1P milkV C0201 \_12PF 25V C33 Project: SG2000 MIPI\_TX\_3N MIPI\_TX\_4P 07 SG2000 PART2 SYS XTAL Rev: 1.1 MIPI\_TX\_4N Sheet: <designer>





# WIFI&BT



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