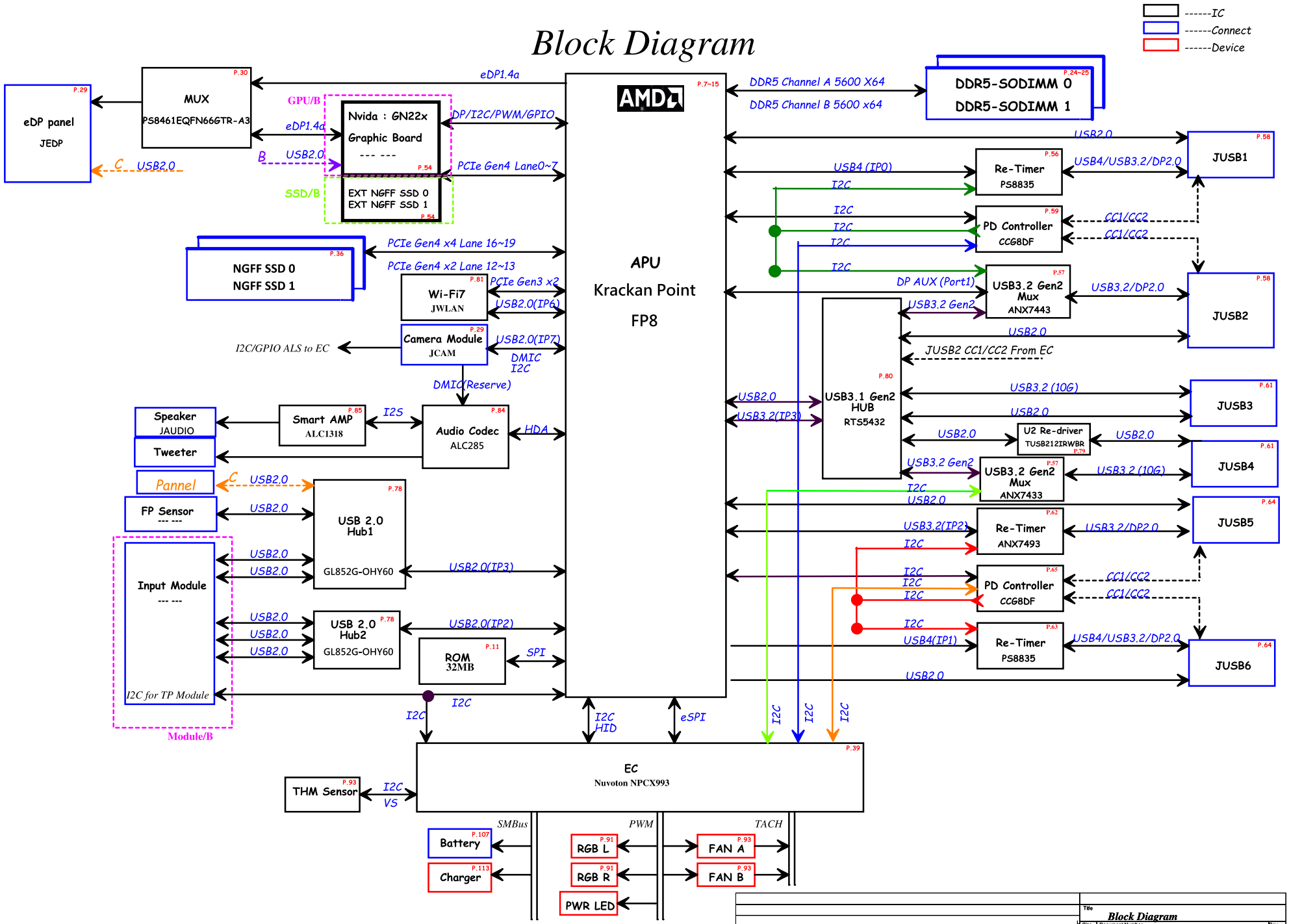
# Block Diagram




| | |
|---|---|
| Title | Block Diagram |
| Size | |
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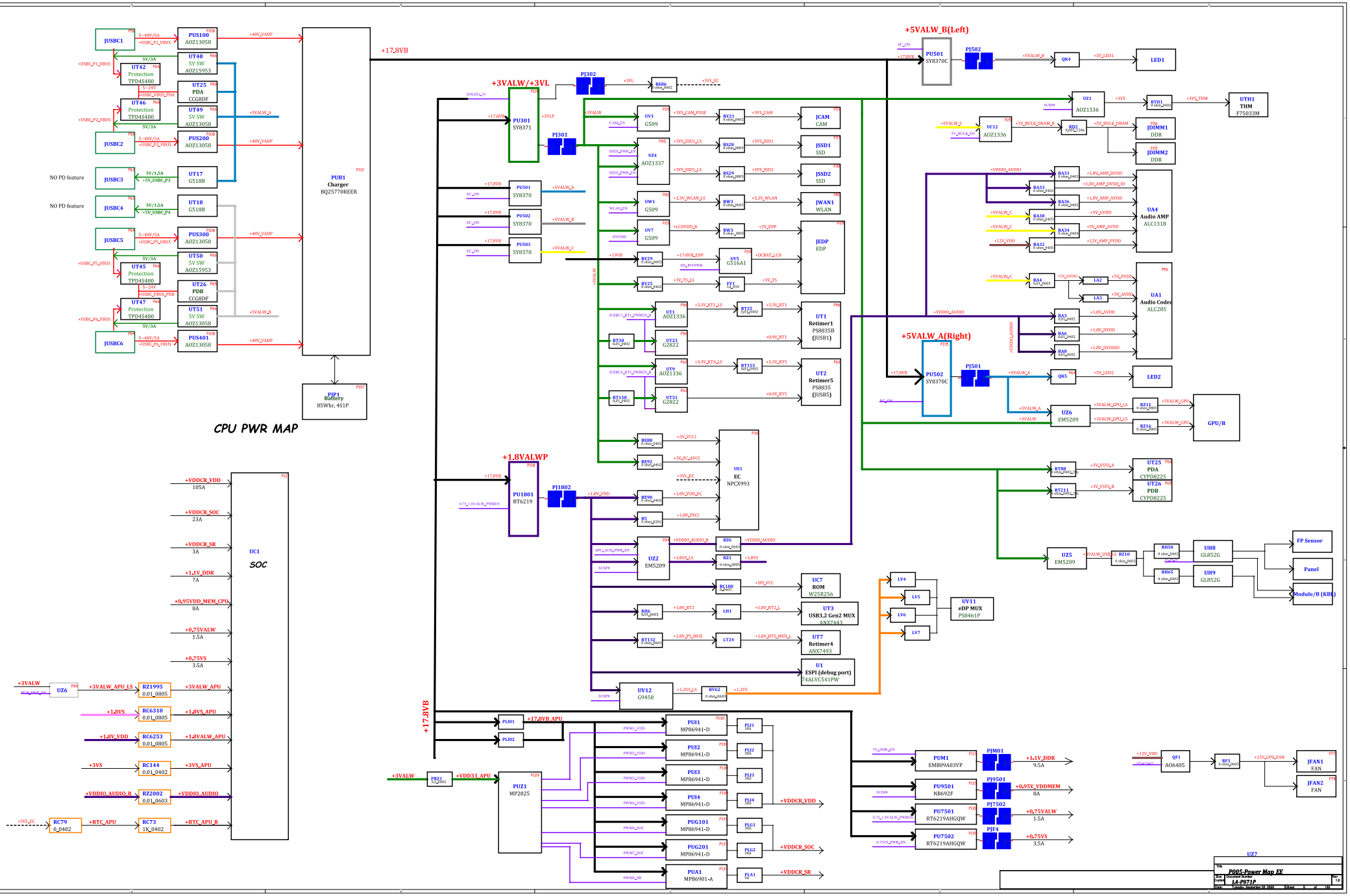


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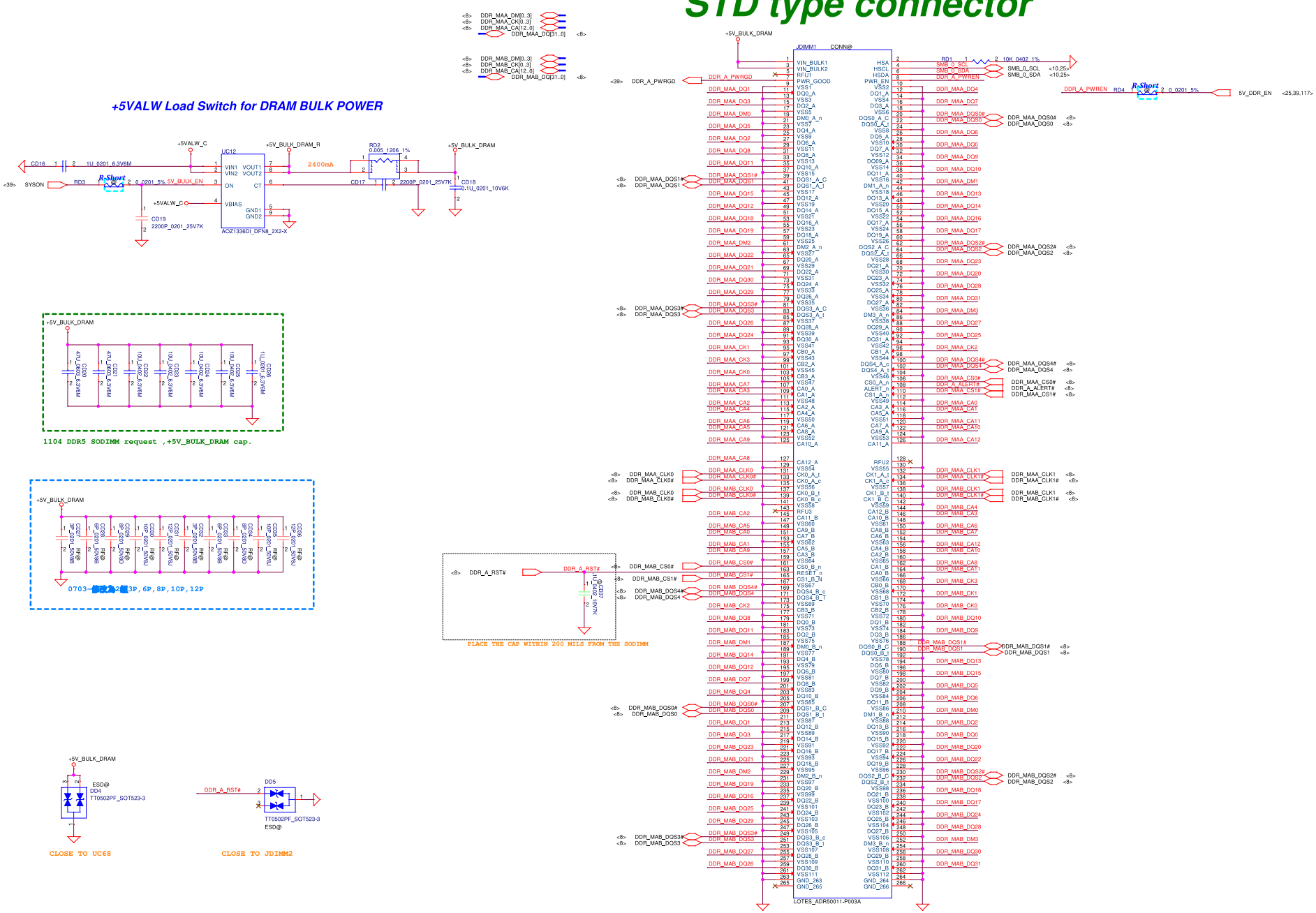
Main Func = DDR

# STD type connector




| Title | P024-DDR5 M0_EE | |
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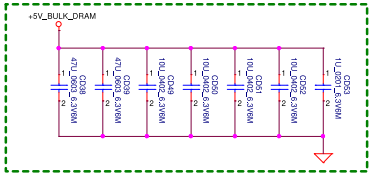
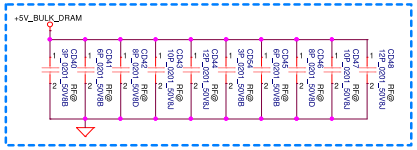
**Main Func = DDR**

# Reverse type connector

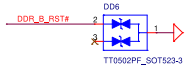
Layout Note:
Place near JDIMM2




1104 DDR5 SODIMM request ,+5V_BULK_DRAM cap.



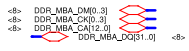

0703-[redacted]3P,6P,8P,10P,12P

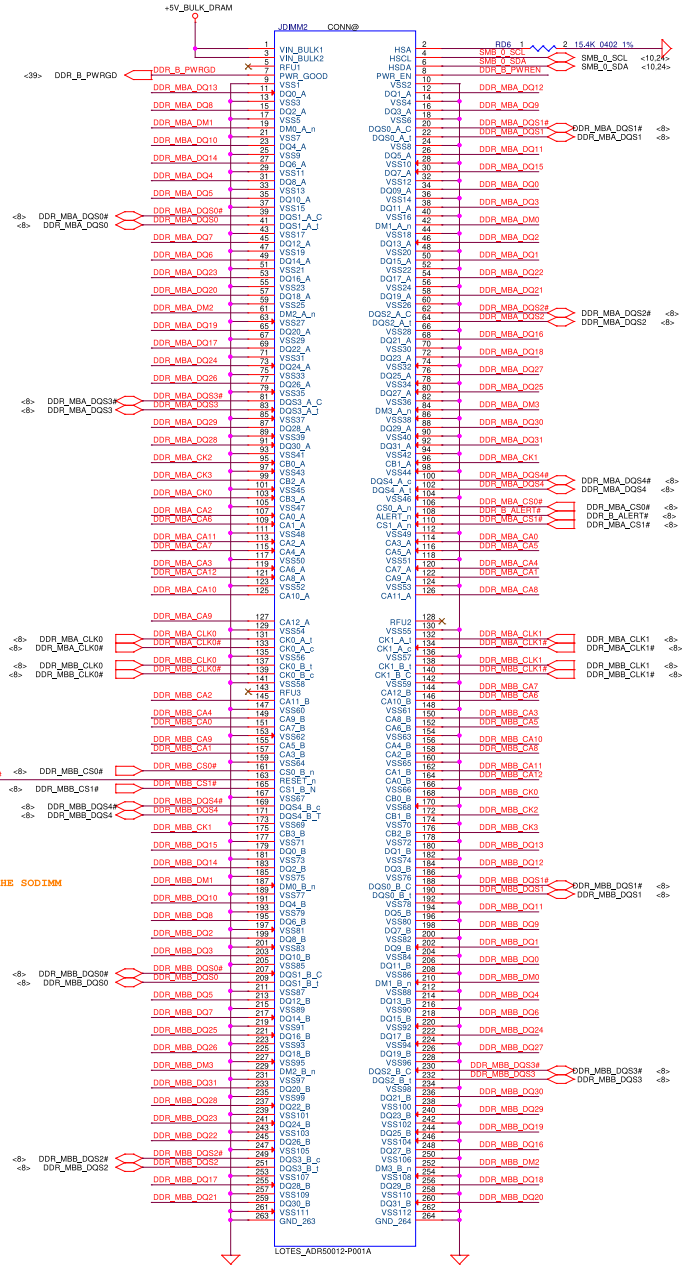



ESD@

CLOSE TO JDIMM1

PLACE THE CAP WITHIN 200 MILS FROM THE SODIMM






| | |
|---|---|
| Title | P025-DDR5 M1_EE |
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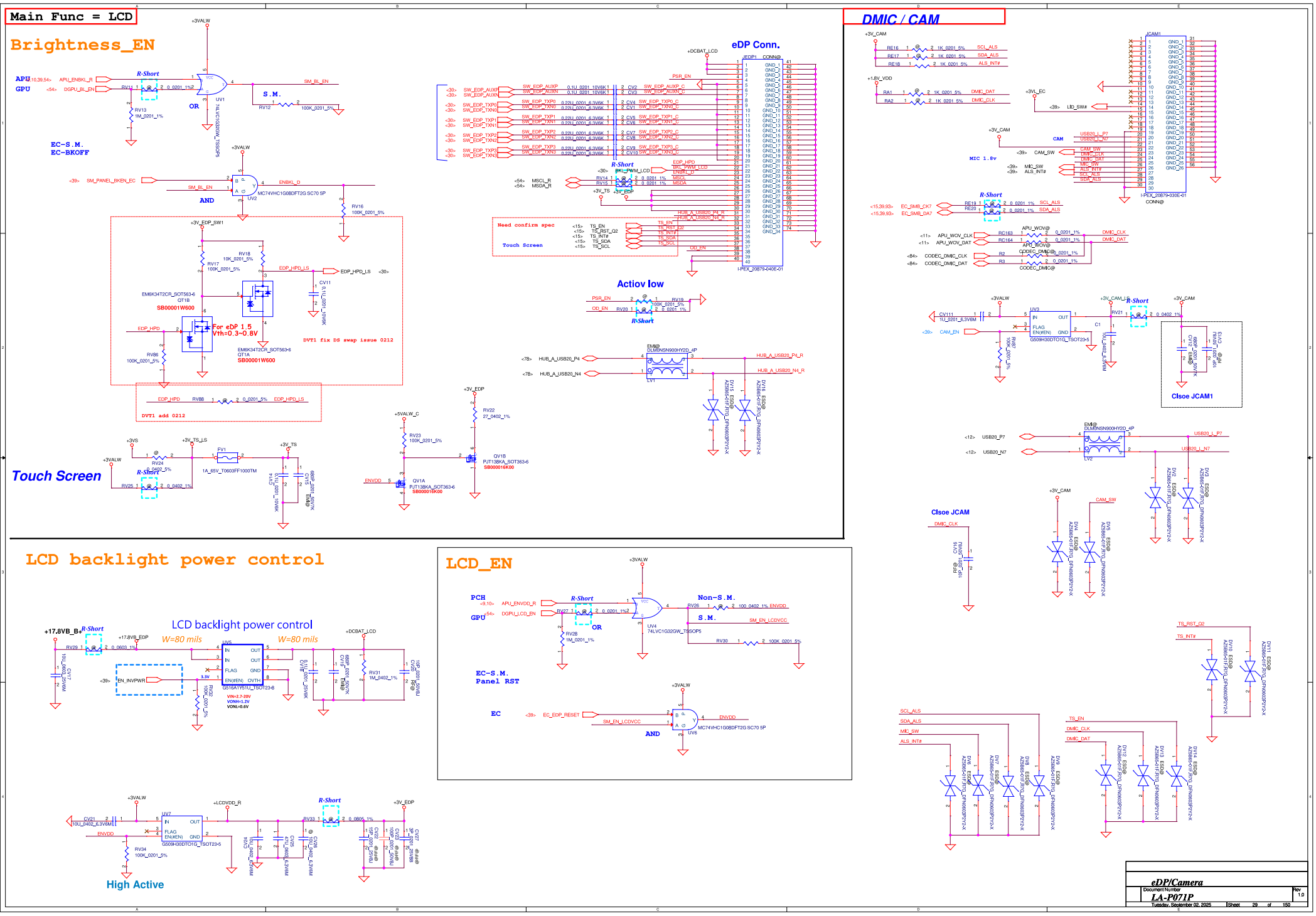


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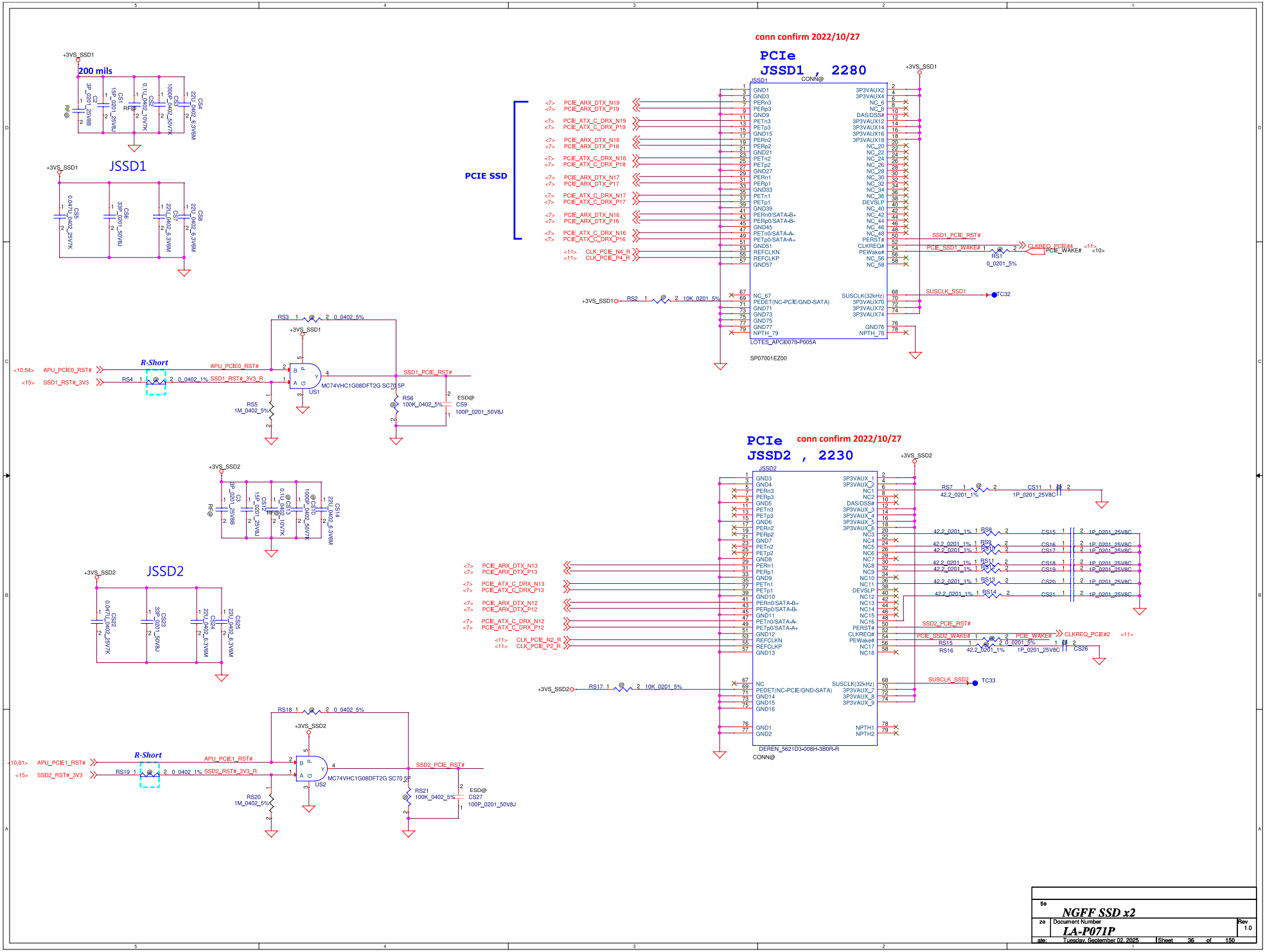


| | | |
|---|---|---|
| tle | NGFF SSD x2 | |
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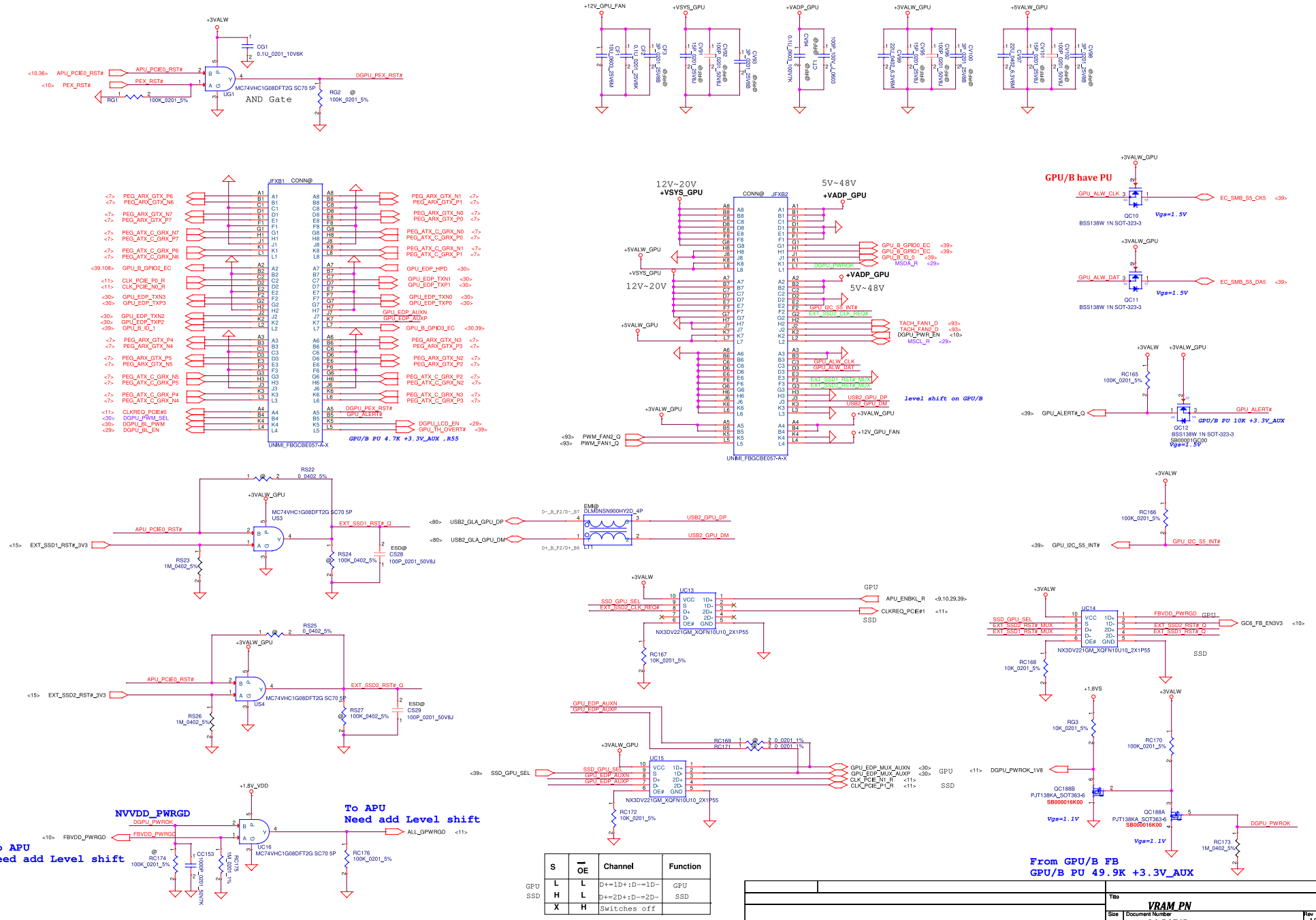
## Main Function:




| S | OE | Channel | Function |
|---|---|---|---|
| GPU L | L | D+=1D+;D-=1D- | GPU |
| SSD H | L | D+=2D+;D-=2D- | SSD |
| X | H | Switches off | |

| Title | VRAM_PN | |
|---|---|---|
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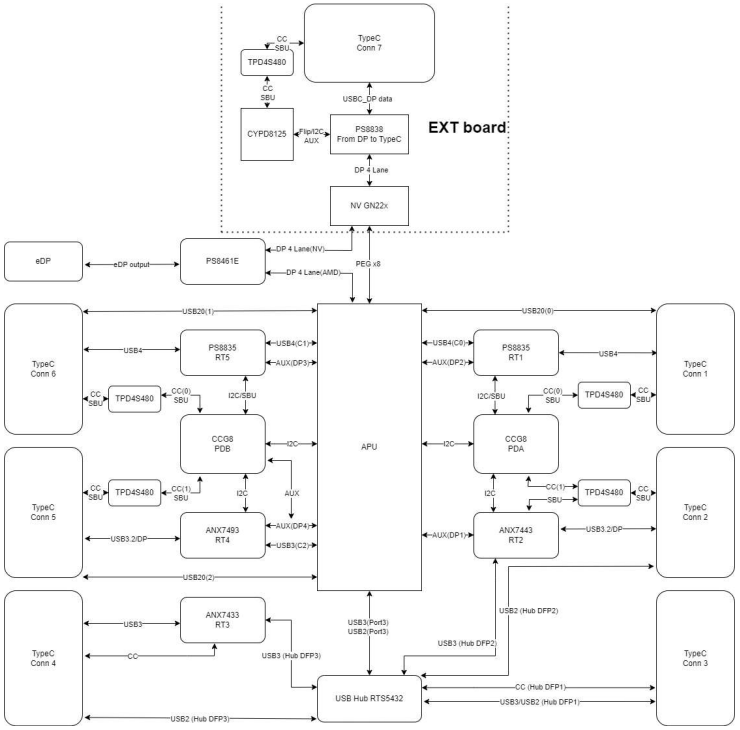
**Main Function:**




## PD I2C/SMBUS Address Table

| PD_SMBUS Port | | Power Rail | Device | 8bit Address | 7bit Address |
|---|---|---|---|---|---|
| PDA | I2C_SCL0<br>I2C_SDA0 | +3VALW | RT1_PS8835 | 0x40-0x5F | 0x20-0x2F |
| | | +3VALW | ANX7443 | 0x22 | 0x11 |
| PDB | I2C_SCL0<br>I2C_SDA0 | +3VALW | ANX7493 | 0x7C | 0x3E |
| | | +3VALW | RT5_PS8835 | 0x20-0x3F | 0x10-0x1F |

P055-USB Map & Sequence_EE

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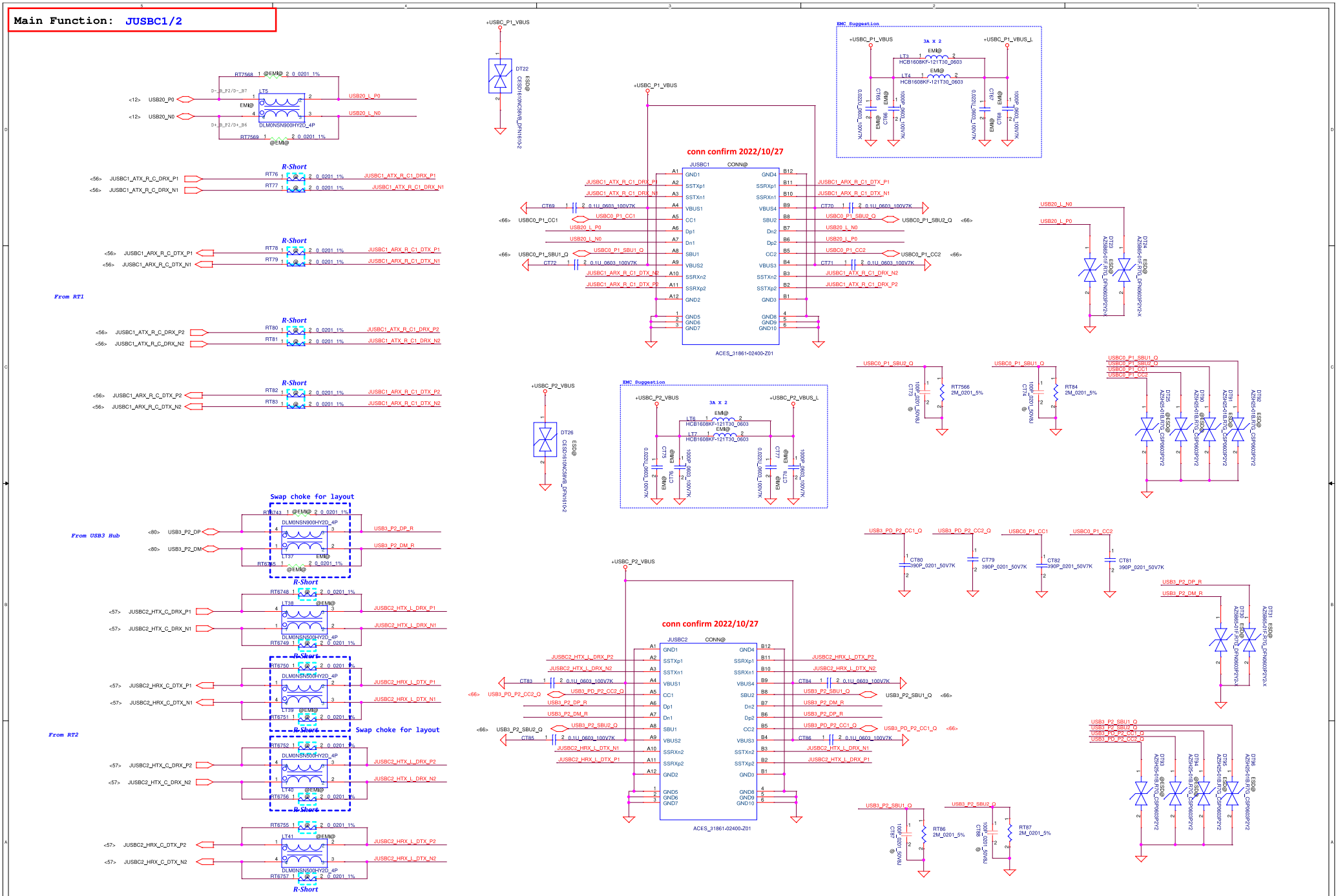
# Main Function: JUSBC1/2

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| | | |
|---|---|---|
| Title | TypeC CONN | |
| Size | Document Number: LA-P071P | Rev 1.0 |
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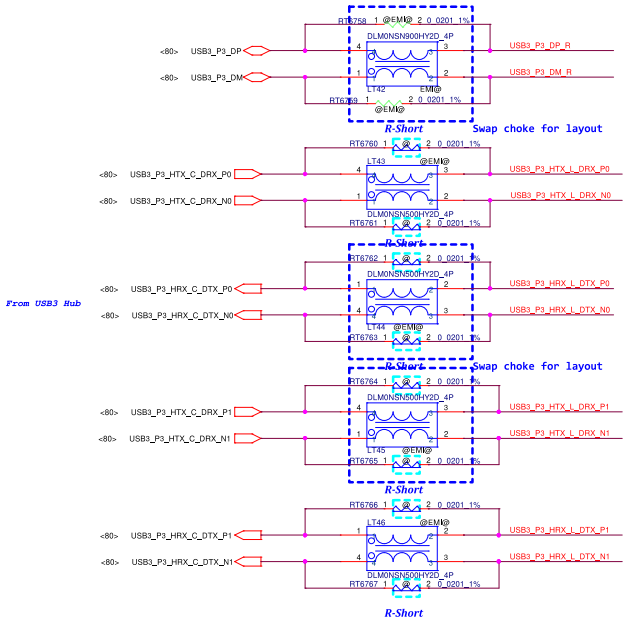
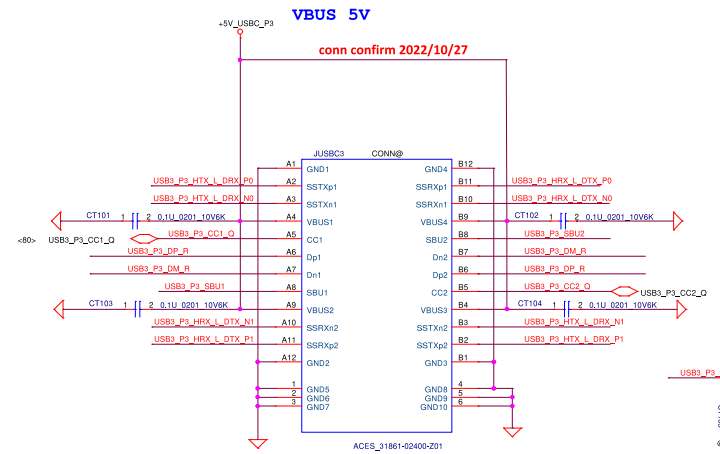
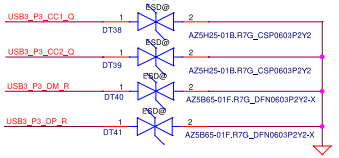
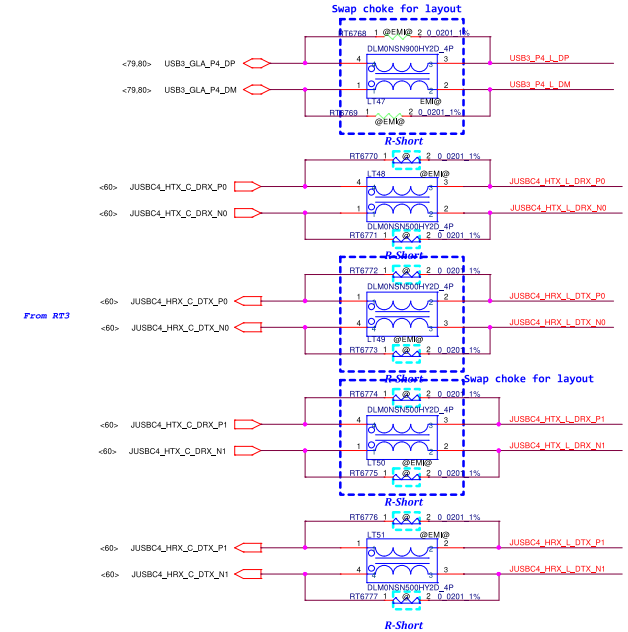
**Main Function: JUSBC3/4**

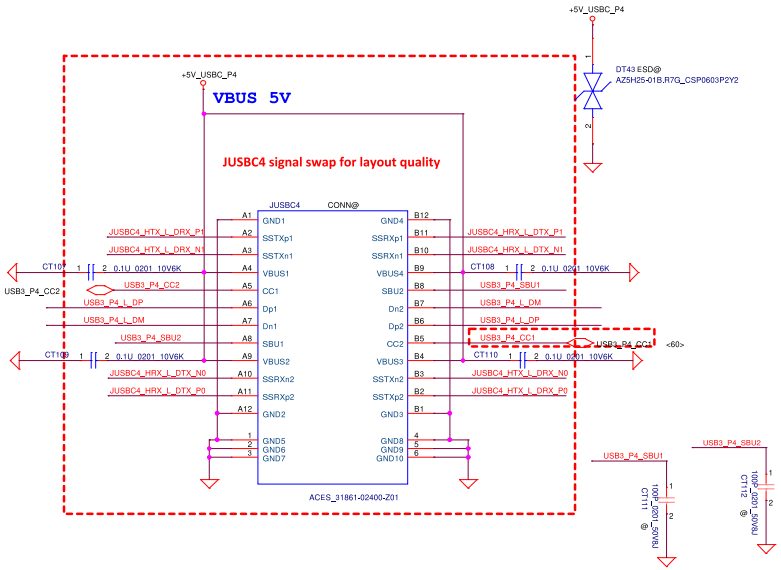


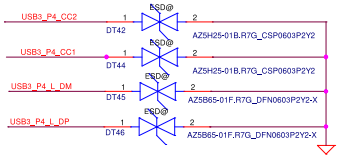

**SC400008100 Change to SC40000EC00**




**SC400008100 Change to SC40000EC00**




| | | |
|---|---|---|
| Title | RSV | |
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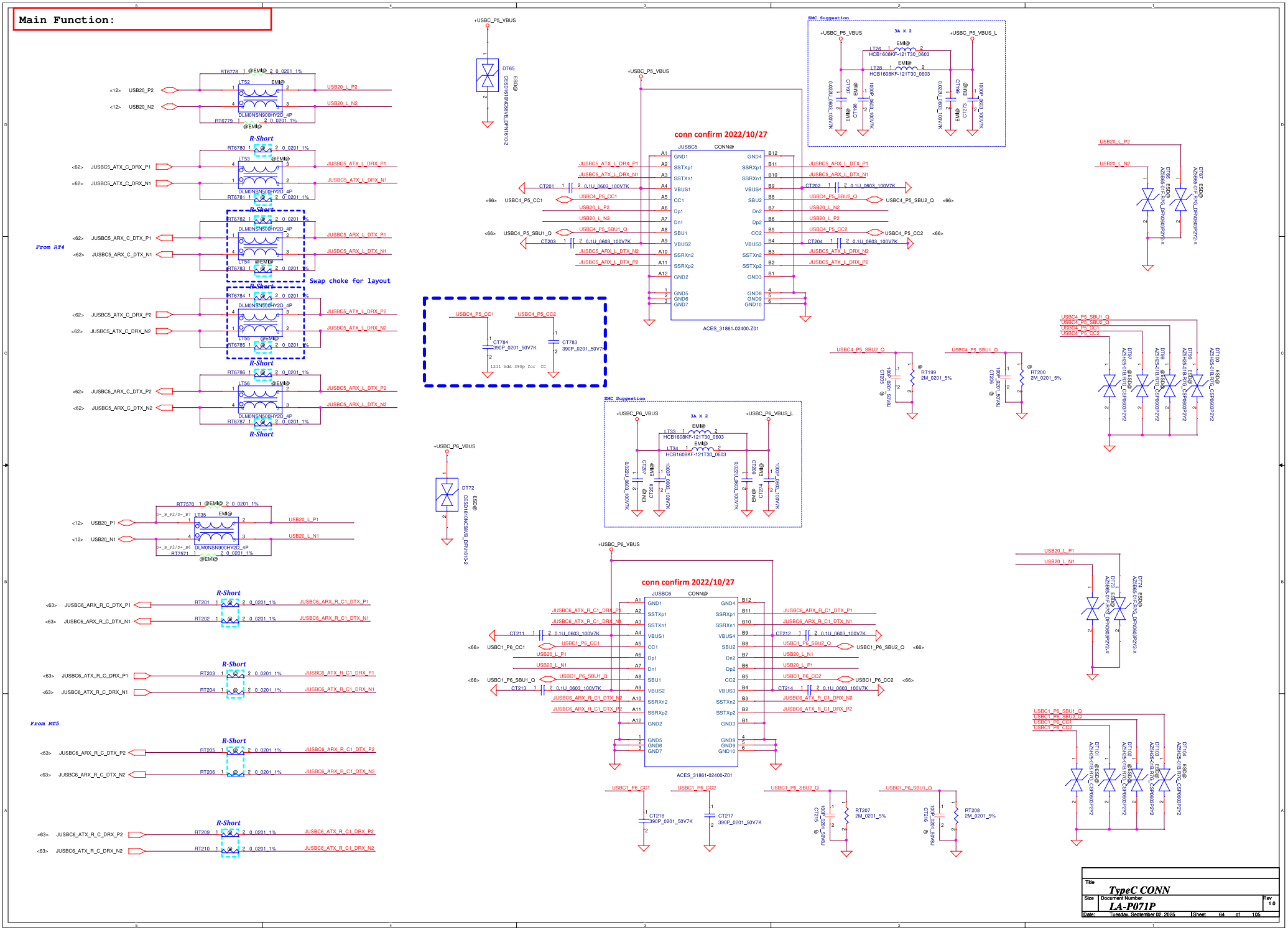
## Main Function:

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| | | | |
|---|---|---|---|
| Title | TypeC CONN | | |
| Size | Document Number | | Rev |
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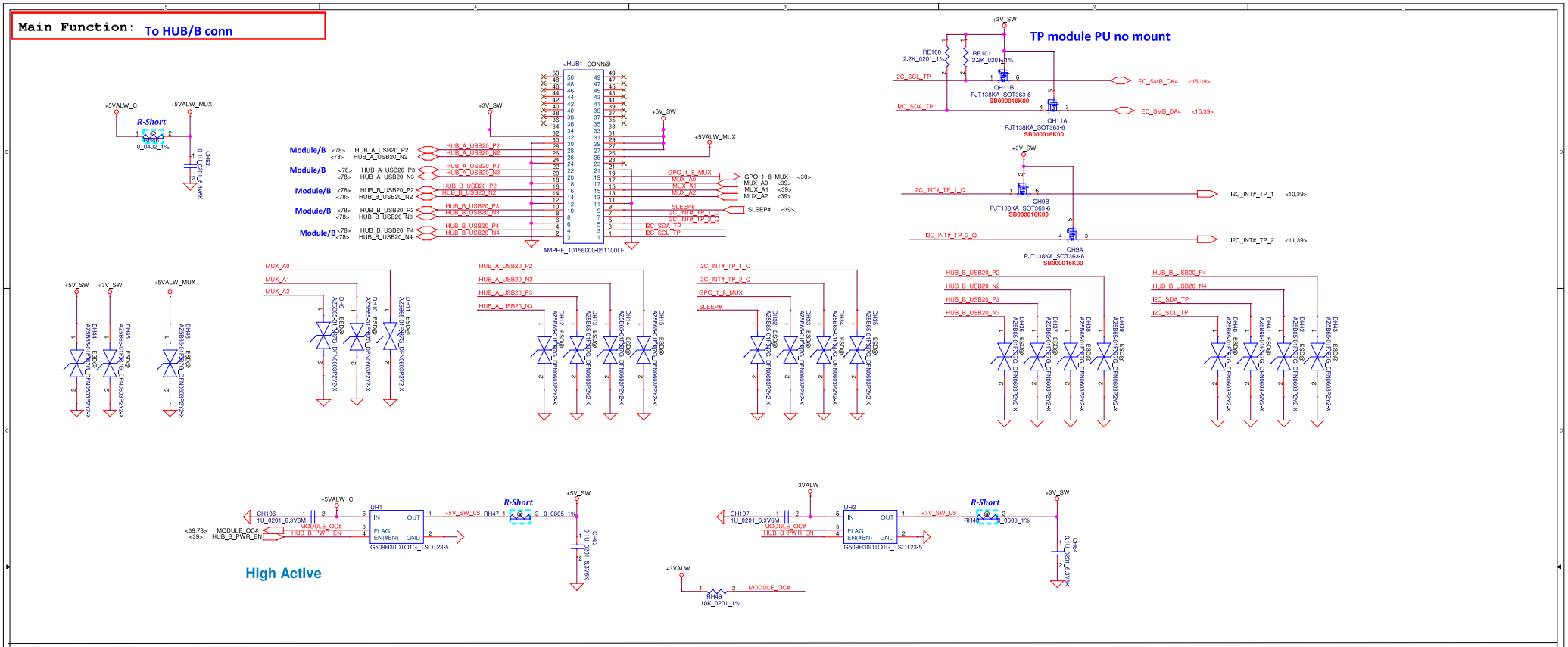


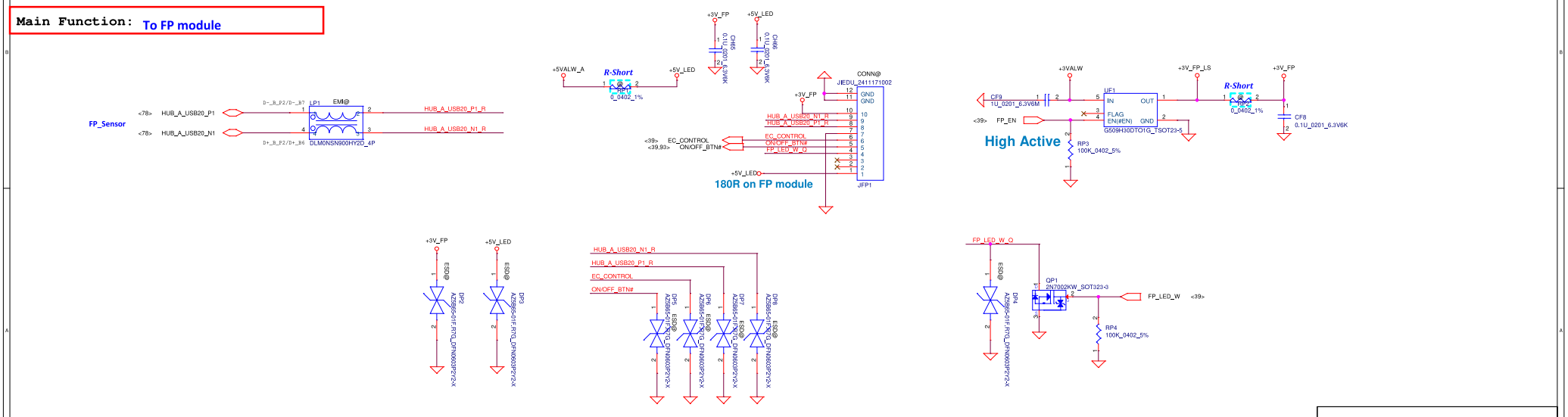


| | |
|---|---|
| Title | HUB/B FP feature |
| Size | |
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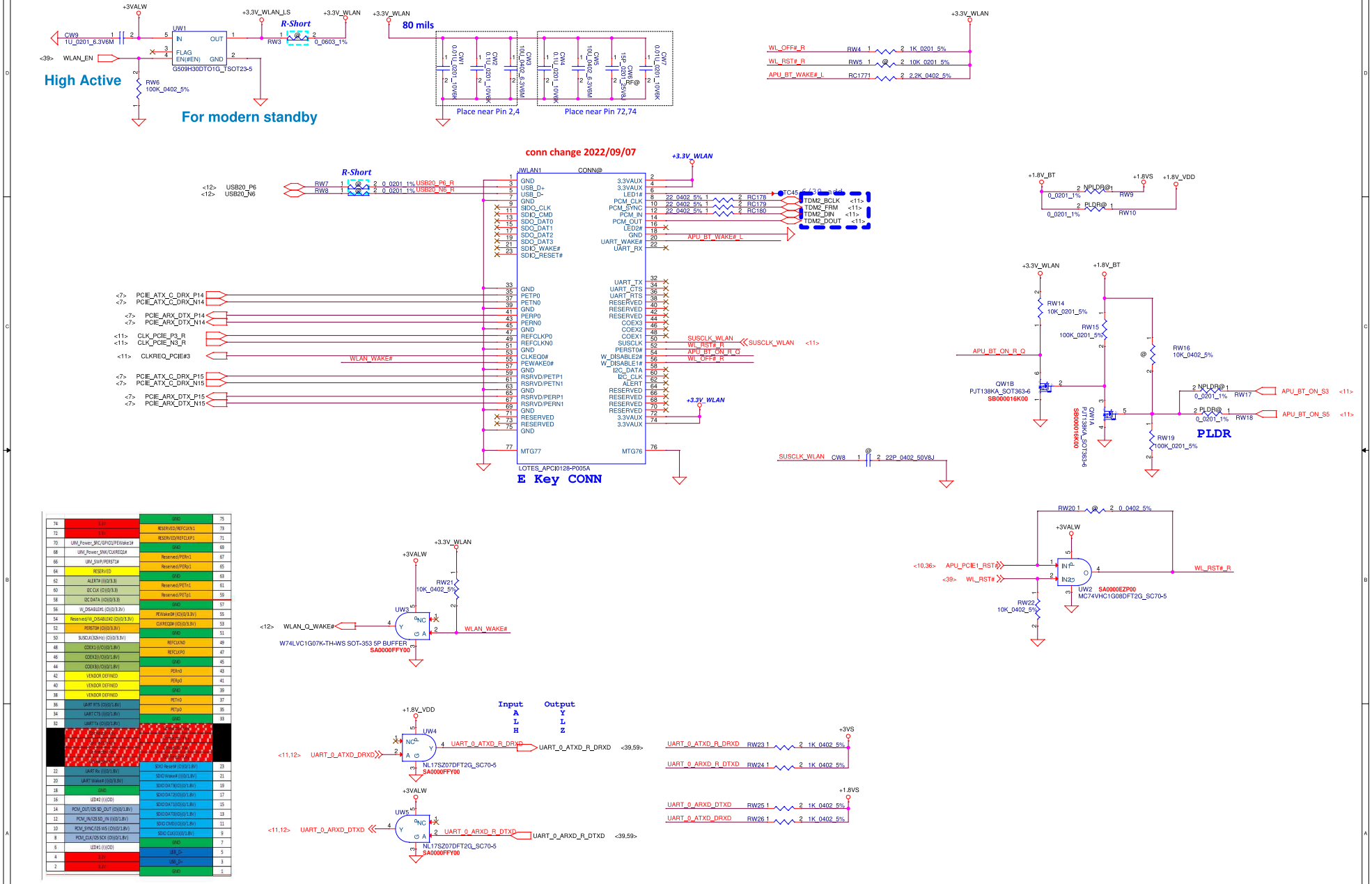
# Main Func = WLAN M.2




| | | | |
|---|---|---|---|
| 76 | 3.3V | GND | 75 |
| 72 | 3.3V | RESERVED/REFCLKN1 | 73 |
| 70 | UIM_Power_SNC/GPIO2/PEWake1# | RESERVED/REFCLKP1 | 71 |
| 68 | UIM_Power_SNK/CLKREQ1# | GND | 69 |
| 66 | UIM_SWP/PERST1# | Reserved/PETn1 | 67 |
| 64 | RESERVED | Reserved/PETp1 | 65 |
| 62 | ALERT# (I)(O)(3.3) | GND | 63 |
| 60 | I2C CLK (O)(0.3.3) | Reserved/PETn1 | 61 |
| 58 | I2C DATA (I)(O)(3.3) | Reserved/PETp1 | 59 |
| 56 | W_DISABLE1 (O)(0.3.3V) | GND | 57 |
| 54 | Reserved/W_DISABLE2 (O)(0.3.3V) | PEWake0# (IO)(0/3.3V) | 55 |
| 52 | PERST0# (O)(0.3.3V) | CLKREQ0# (IO)(0/3.3V) | 53 |
| 50 | SUSCLK(32kHz) (O)(0/3.3V) | GND | 51 |
| 48 | COEX1 (I/O)(0/1.8V) | REFCLKN0 | 49 |
| 46 | COEX2) (O)(0/1.8V) | REFCLKP0 | 47 |
| 44 | COEX3) (O)(0/1.8V) | GND | 45 |
| 42 | VENDOR DEFINED | PERn0 | 43 |
| 40 | VENDOR DEFINED | PERp0 | 41 |
| 38 | VENDOR DEFINED | GND | 39 |
| 36 | UART RTS (O)(0/1.8V) | PETn0 | 37 |
| 34 | UART CTS (I)(0/1.8V) | PETp0 | 35 |
| 32 | UART Tx (O)(0/1.8V) | GND | 33 |
| | [illegible] | [illegible] | |
| 22 | UART Rx (I)(0/1.8V) | SDIO Reset# (O)(0/1.8V) | 23 |
| 20 | UART Wake# (I)(0/3.3V) | SDIO Wake# (I)(0/1.8V) | 21 |
| 18 | GND | SDIO DATA3(I/O)(0/1.8V) | 19 |
| 16 | LED#2 (I)(OD) | SDIO DATA2(I/O)(0/1.8V) | 17 |
| 14 | PCM_OUT/I2S SD_OUT (O)(0/1.8V) | SDIO DATA1(I/O)(0/1.8V) | 15 |
| 12 | PCM_IN/I2S SD_IN (I)(0/1.8V) | SDIO DATA0(I/O)(0/1.8V) | 13 |
| 10 | PCM_SYNC/I2S WS (O)(0/1.8V) | SDIO CMD(I/O)(0/1.8V) | 11 |
| 8 | PCM_CLK/I2S SCK (O)(0/1.8V) | SDIO CLK(I/O)(0/1.8V) | 9 |
| 6 | LED#1 (I)(OD) | GND | 7 |
| 4 | 3.3V | USB_D- | 5 |
| 2 | 3.3V | USB_D+ | 3 |
| | | GND | 1 |

| | |
|---|---|
| tle | WLAN/BT (w/ CNVi) M.2 |
| ze | Document Number LA-P071P Rev 1.0 |
| te: | Tuesday, September 02, 2025 Sheet 81 of 150 |

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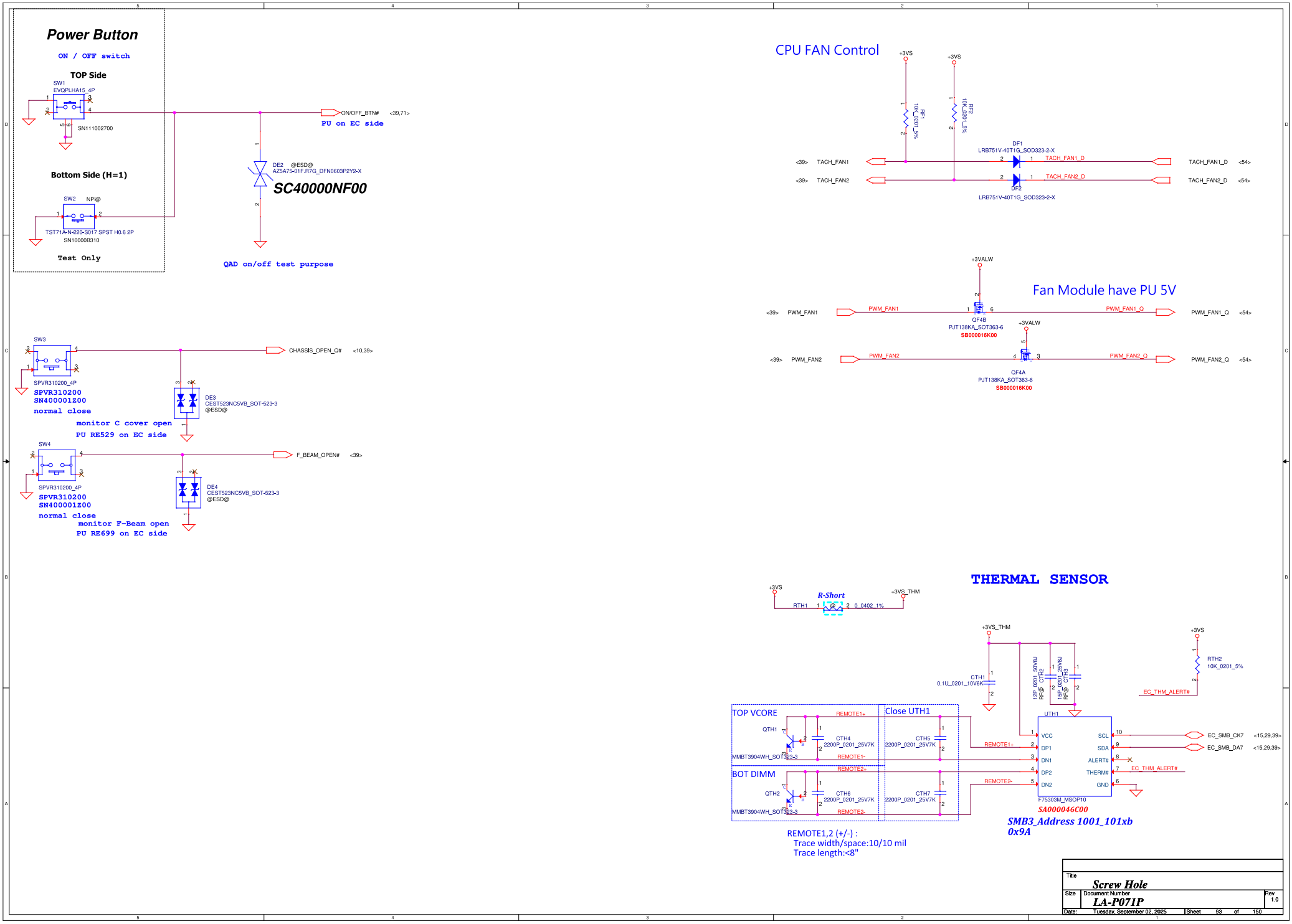


| | | |
|---|---|---|
| Title | Screw Hole | |
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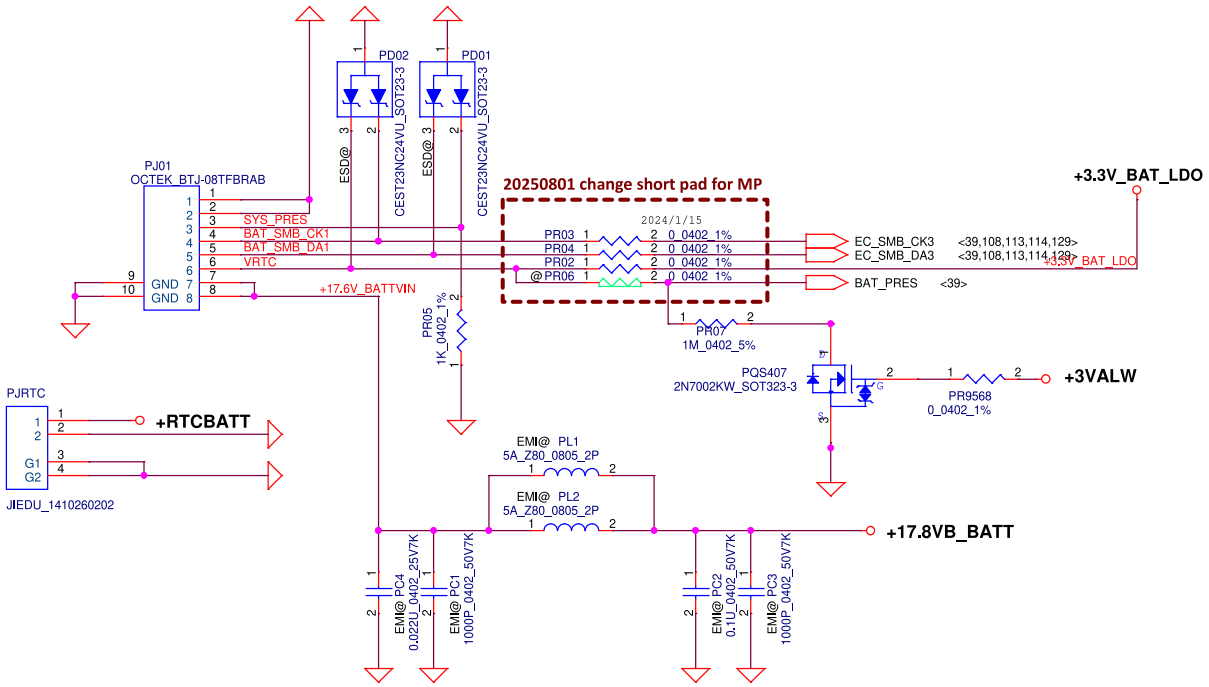


| | | | |
|---|---|---|---|
| Title | **BATT conn** | | |
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