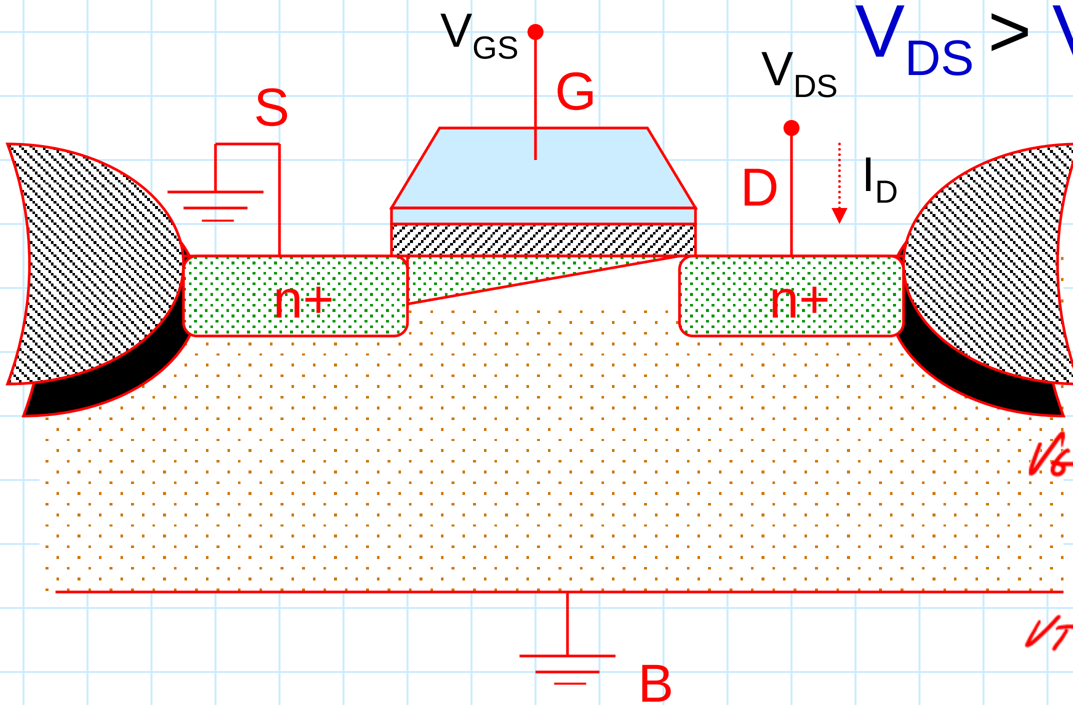
Operating regions: saturation region

Assuming $V_{GS} > V_T$

$V_{DS} > V_{GS} - V_T$

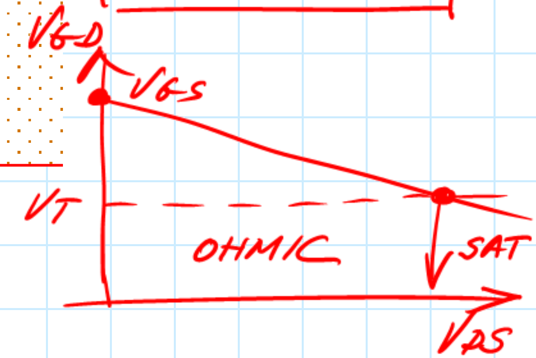


$V_{GD} < V_T$

$V_{GD} = V_{GS} - V_{DS}$

$V_{GS} - V_{DS} < V_T \Rightarrow$

$\boxed{V_{DS} > V_{GS} - V_T}$



The channel is pinched-off (small channel near D), and the current remains constant

Operating regions: saturation region(2)

Condition: $V_{DS} > V_{GS} - V_T$

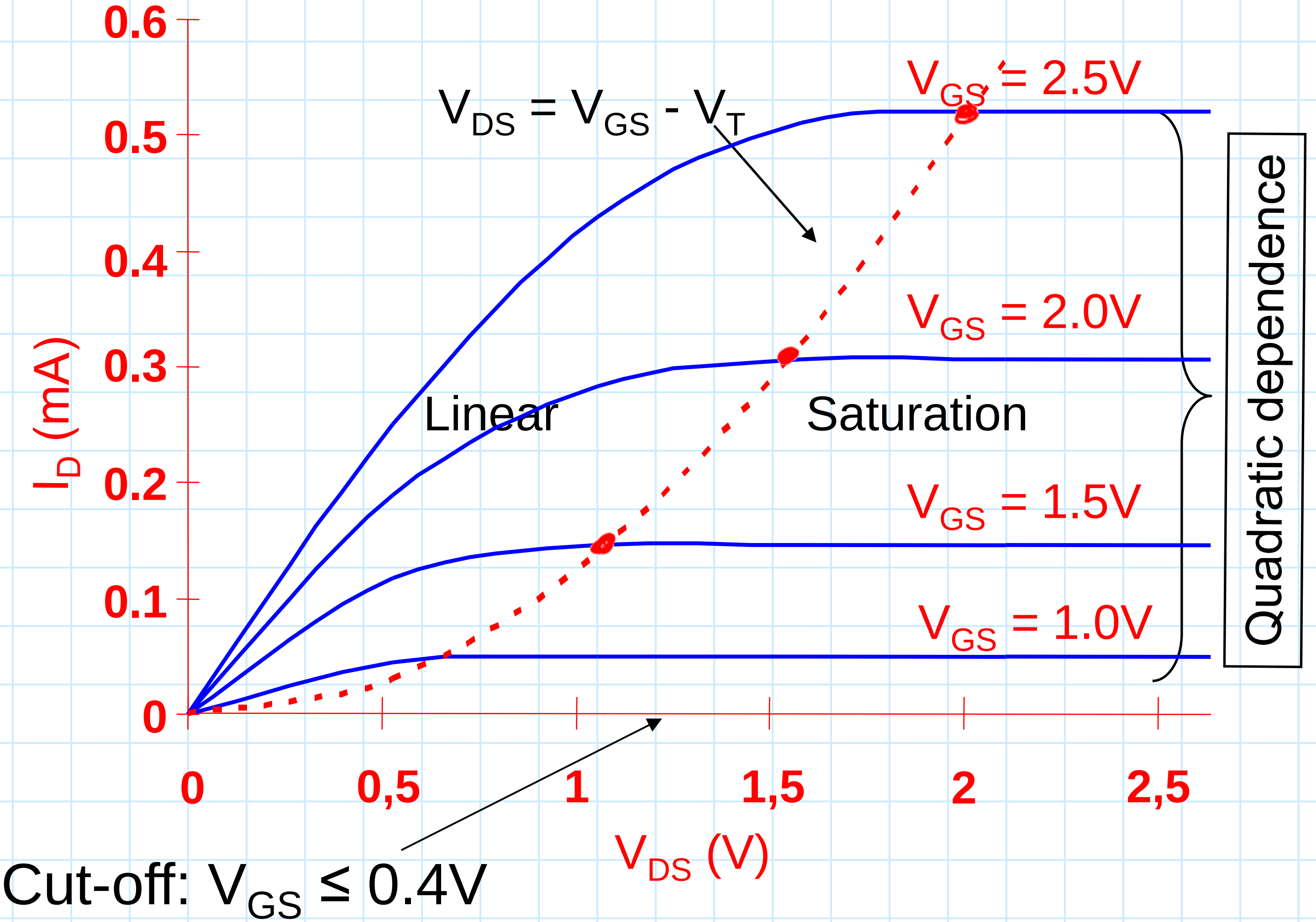
V/I function: $I_{DS} = K\,(V_{GS} - V_T)^2$ (Saturation parable)

The channel is *pinched-off* →

For a fixed VGS, the current $I_{DS} \approx$ constant, and indep. of V_{DS}

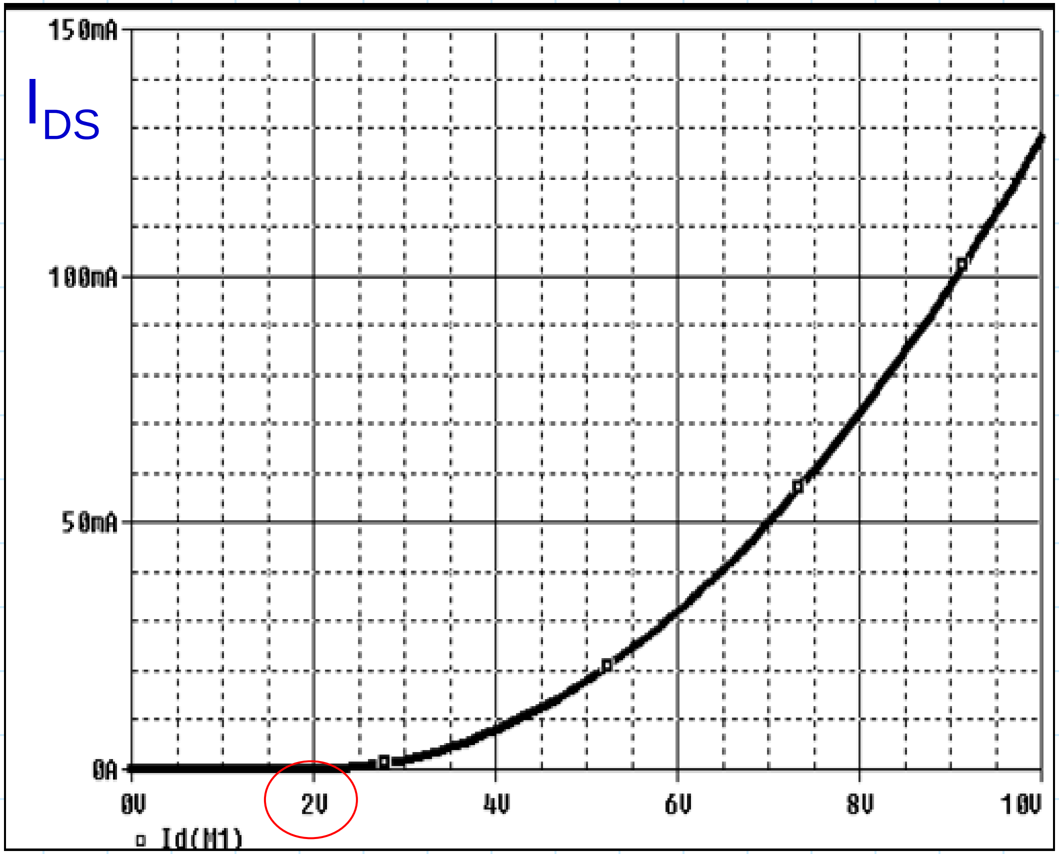
The Mosfet is equivalent to a current source (I_{DS}) controlled by voltage (V_{GS})

I-V curves of the NMOS



Example: NMOS Transistor: $V_T = 0.4V$ $K = 0.12mA/V^2$

I_{DS} versus V_{GS} in saturation region



V_{GS}

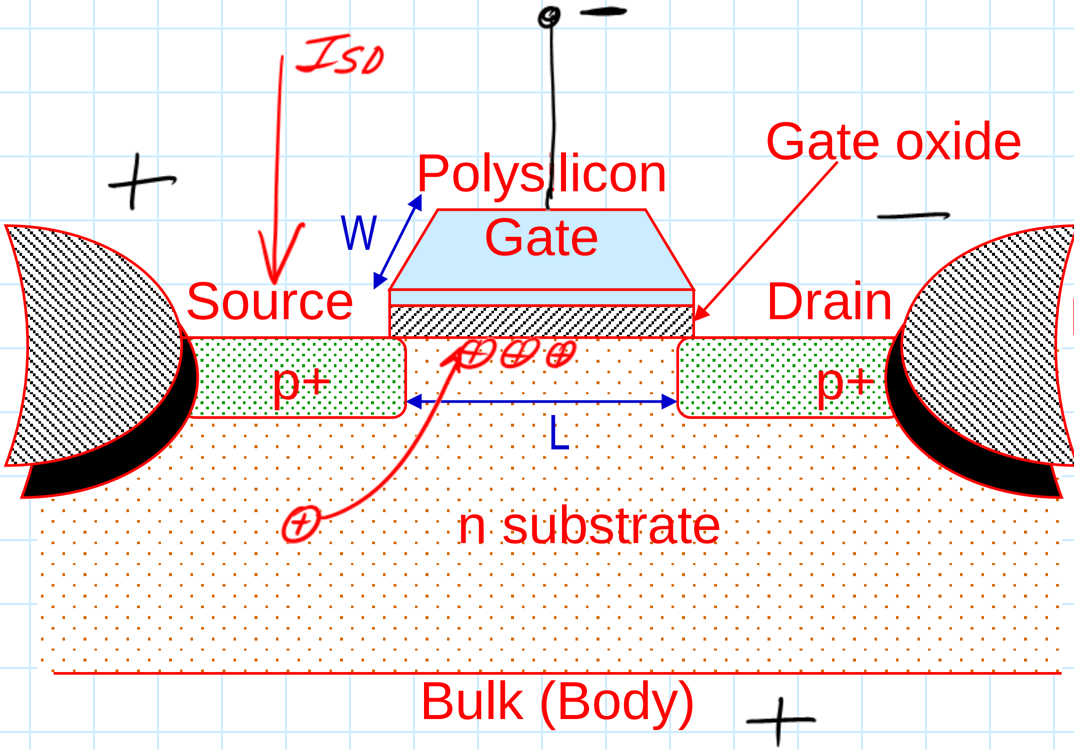
Saturation parable:

$$I_{DS} = K\,(V_{GS} - V_T)^2$$

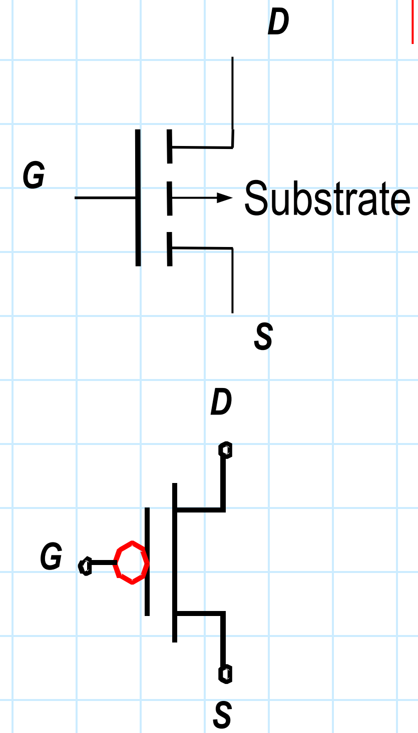
$V_T = 2V$

$$V_{GS} \leq V_T \rightarrow I_D = 0$$

PMOS Transistor: cross section

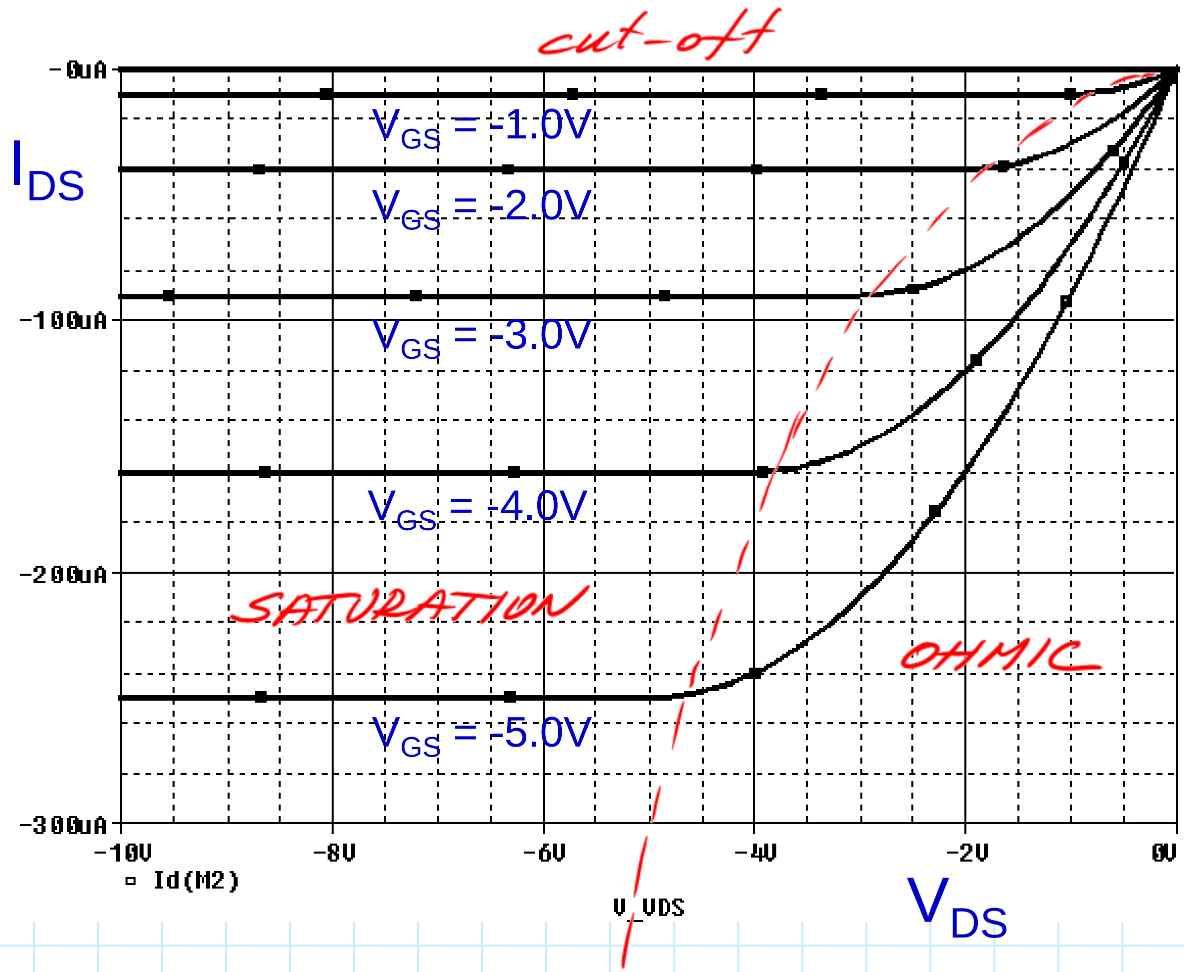


Symbols



$V_{GS} < -V_T \Rightarrow T_{ON}$

PMOS. Characteristic curves



All variables are negative!

$V_{GS} < 0$, $V_{DS} < 0$,

$I_{DS} < 0 \rightarrow I_{SD} > 0$

Conduction: $V_{GS} < -V_T$

The PMOS transistor: summary

- Cut-off: $V_{GS} \geq -V_T$
- Saturation:

  $V_{DS} < V_{GS} + V_T$

  $I_{SD} = K\,(V_{GS}+V_T)^2$
- Ohmic:

$V_{DS} \geq V_{GS} + V_T$

$I_{SD} = K\,[2(V_{GS}+V_T)V_{DS} - V_{DS}^2]$

$V_{DS} \downarrow \Rightarrow \quad I_{SD} = 2K(V_{GS}+V_T)V_{DS}$

$$R_{ON} \approx \left| \frac{1}{2 \cdot K(V_{GS} + V_T)} \right|$$

(considering K and V_T as absolute values, $V_{GS} < 0$, $V_{DS} < 0$)

- Less use than N-channel MOSFETS, as holes mobility is smaller than electrons mobility: $K = \frac{1}{2} K_p \frac{W}{L}$
  - Slower than the NMOS $\rightarrow (K_p)_p = \mu_p C_{ox}$; $\mu_p < \mu_n$; $(K_p)_p < (K_p)_n$
  - They need more W/L → bigger than NMOS (more space occupied)

MOSFET: Summary of some formulas

NMOS		PMOS
$V_{GS} > V_T$	CONDUCTS	$V_{GS} < -V_T$
$V_{DS} > V_{GS} - V_T$	SATURATION condition	$V_{DS} < V_{GS} + V_T$
$I_{DS} = K\,(V_{GS} - V_T)^2$	SATURATION	$I_{SD} = K\,(V_{GS} + V_T)^2$
$I_{DS} = K\,[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$ $V_{DS} \le V_{GS} - V_T$ $R_{ON} \approx \dfrac{1}{2 \cdot K(V_{GS} - V_T)}$	OHMIC or LINEAR	$I_{SD} = K\,[2(V_{GS} + V_T)V_{DS} - V_{DS}^2]$ $V_{DS} \geq V_{GS} + V_T$ $R_{ON} \approx \left\lvert \dfrac{1}{2 \cdot K(V_{GS} + V_T)} \right\rvert$

(Taking the absolute value of V_T and K in all formulas)

Equivalences and differences between Mosfet-BJTs

Terminals

MOSFET	BJT
DRAIN	COLLECTOR
SOURCE	EMITTER
GATE	BASE

BJT: $I_B > 0$ for conducting

Mosfet: $I_G = 0$ always!

Working regions

MOSFET	BJT
CUT-OFF REGION	CUT-OFF REGION
SATURATION REGION	ACTIVE REGION
OHMIC \ LINEAR REGIN	SATURATION REGION

Mosfet's Saturation : maximum I_{DS} for a given V_{GS}

BJT's saturation: maximum I_C for a given biass circuit

Enhancement MOSFET Biassing (1)

Equations to analyze the Mosfets biassing circuits

1.- Input loop: G-S → loop equation with V_{GS}

2.- Assuming saturation → saturation equation

NMOS: $I_{DS} = K\,(V_{GS} - V_T)^2$ PMOS: $I_{SD} = K\,(V_{GS} + V_T)^2$

(With VGS, checkout if MOSFET is conducting)

3.- Output loop D-S → loop equation with V_{DS}

4.- Checkout of saturation

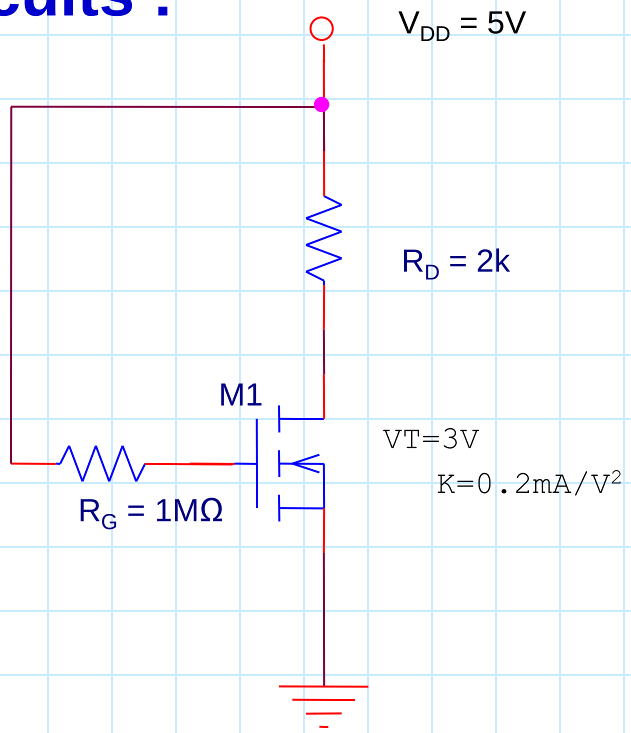
NMOS: $V_{DS} > V_{GS} - V_T$ PMOS: $V_{DS} < V_{GS} + V_T$

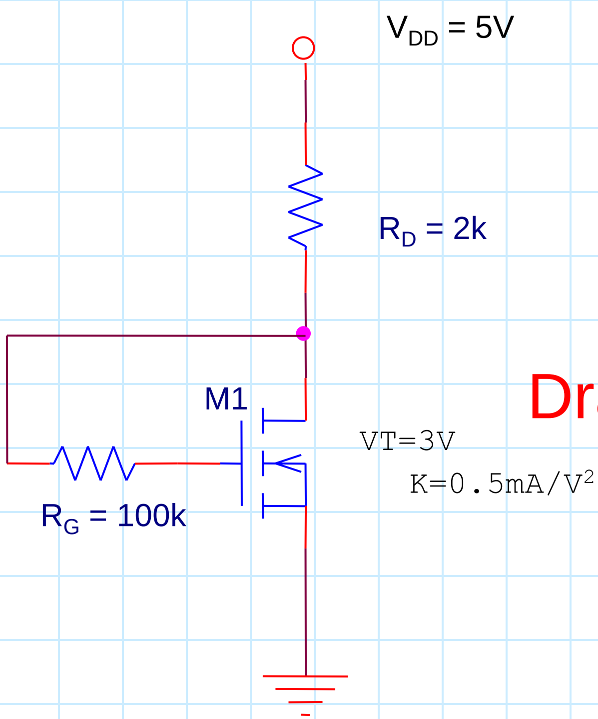
(If not satisfied, return to step 2, using the equation of the linear region, and redo the calculations)

Enhancement MOSFET. Biassing (2)

Examples of Biassing circuits :

Fixed biassing

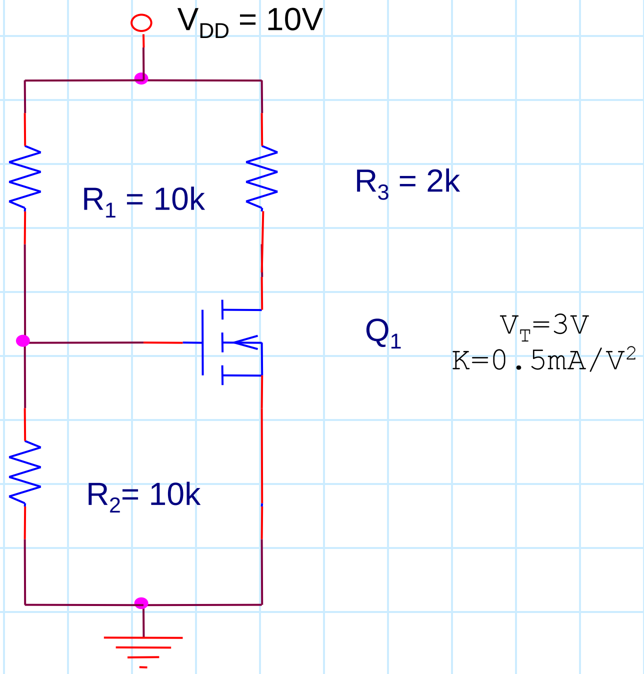




Drain feedback

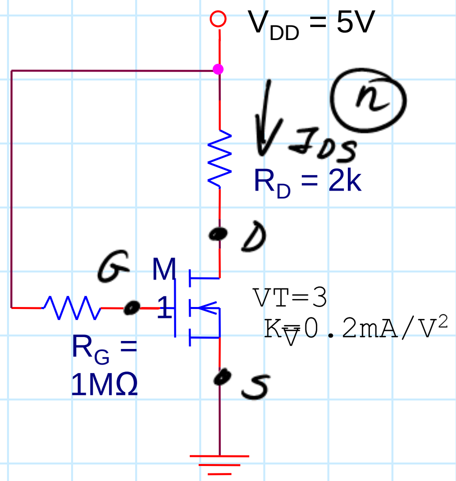
Enhancement MOSFET. Biassing (3)

Biassing with resistor divider



2 solutions for I_{DS} → you choose the one for which $V_{GS} > V_T$

Enhancement MOSFET. Biassing (2)



Fixed biassing

$V_G = V_{DD} \Rightarrow V_{GS} = V_{DD} = 5V > V_T \Rightarrow T\ ON$

assume saturation

$I_{DS} = K(V_{GS} - V_T)^2 = 0.2(5-3)^2 = 0.8mA$

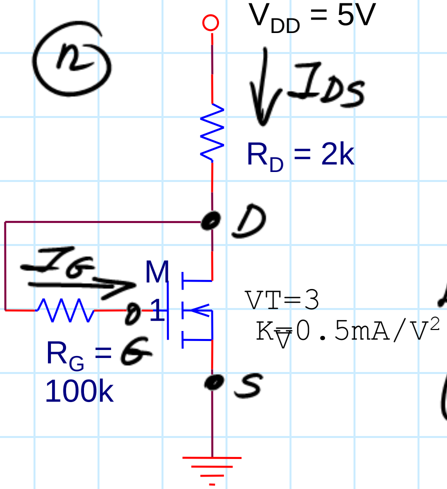
Output loop:

$V_{DS} = V_{DD} - I_{DS} R_D - 5 - 0.8 \cdot 2 = 3.4V$

as $V_{DS} = 3.4V > V_{GS} - V_T = 2V \Rightarrow$ T is saturated $\Rightarrow$

$$\boxed{Q\,(V_{GS} = 5V,\ I_{DS} = 0.8mA,\ V_{DS} = 3.4V)}$$

Enhancement MOSFET. Biassing (2)



$I_G=0 \Rightarrow V_D=V_G \Rightarrow V_{DS}=V_{GS}$

as $V_{DS} > V_{DS}-V_T = V_{GS}-V_T \Rightarrow$ T SATURATED.

a) $I_{DS}=K(V_{GS}-V_T)^2 = K(V_{DS}-V_T)^2 = 0.5(V_{DS}-3)^2$

b) Output loop:

$$I_{DS}=\frac{V_{DD}-V_{DS}}{R_D}=\frac{5-V_{DS}}{2}$$

Drain feedback

From a) and b): $\frac{5-V_{DS}}{2}=0.5(V_{DS}-3)^2$

$5-V_{DS}=V_{DS}^2-6V_{DS}+9$

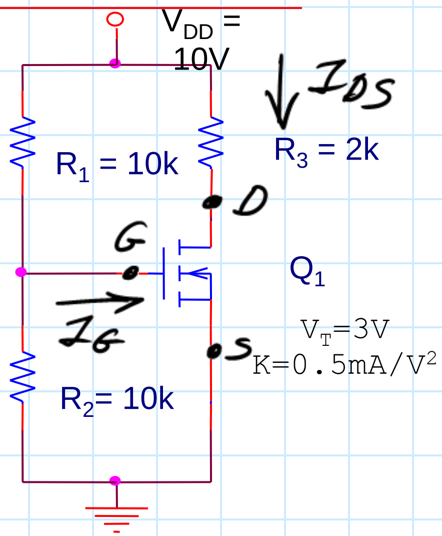
$V_{DS}^2-5V_{DS}+4=0 \Rightarrow V_{DS}=\frac{5\pm\sqrt{25-16}}{2}=\frac{5\pm3}{2}$ → 4 (*), 1

(*) Correct, $V_{DS}=V_{GS}>V_T$ (T ON)

$I_{DS}=\frac{5-V_{DS}}{2}=\frac{5-4}{2}=0.5mA$

$\boxed{Q\ (V_{GS}=4V;\ I_{DS}=0.5mA;\ V_{DS}=4V)}$

Enhancement MOSFET. Biassing (3)



Biassing with resistor divider

$I_G = 0 \Rightarrow V_G = 10 \dfrac{R_2}{R_1+R_2} = 5V = V_{GS} > V_T \Rightarrow T\ ON$

Assume SAT

$I_{DS} = K(V_{GS}-V_T)^2 = 0.5(5-3)^2 = 2mA$

output loop: $V_{DS} = V_{DD} - I_{DS} R_3 = 10 - 4 = 6V$

$V_{DS} > V_{GS} - V_T = 5-3 \Rightarrow T$ is saturated

$\boxed{Q(V_{GS}=5V, I_{DS}=2mA, V_{DS}=6V)}$