Lab 5: NMOS logic gates. Pspice simulation.

Objectives

At the end of this lab, the student should:

Know the different aspects of NMOS logic gates, based on N-channel enhancement MOSFET transistors and load resistors. To analyze the circuits of NMOS logic gates we will use electronic simulation with Pspice.

Contents

Material

PC and PSpice simulation program for Windows (from Orcad). There is a student version in PoliformaT.

Development

Log in with your user of the ALUMNO domain and start PSpice by double clicking on the PSPICE icon on the desktop. Save the created files in the folder W:\TCO\ Prac5.

VERY IMPORTANT: when you save the circuit, put a **different** file name to schematic1, schematic2, etc.

If you have problems in the libraries of simulator, check that within the schematics environment, in **Analysis / Library and Include Files** library is at least included **nom.lib ***

1. The NMOS inverter

We will simulate a single inverter with a NMOS and a drain resistor R_D, as can be seen in Figure 1.

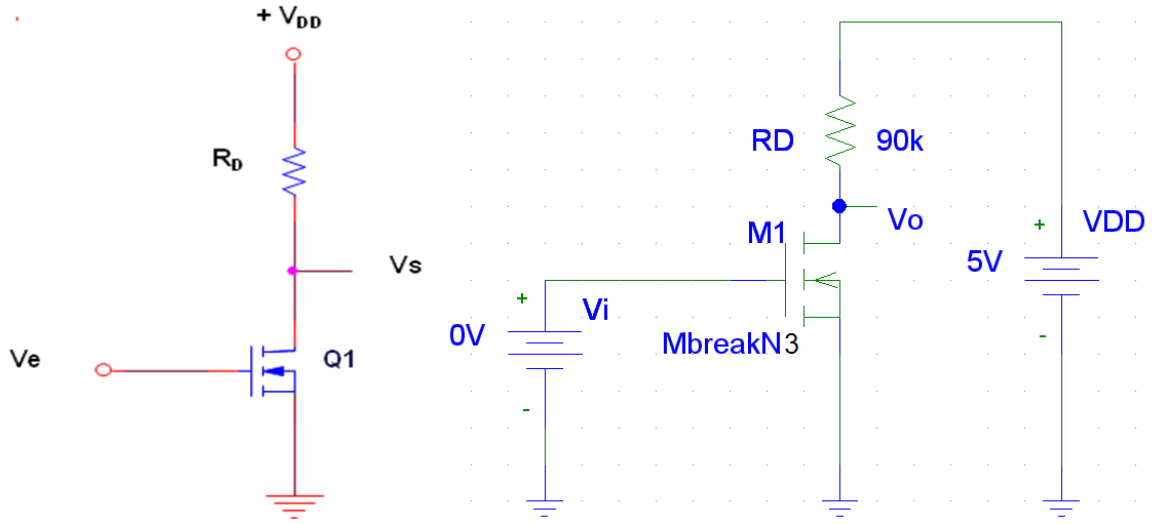


Figure 1. NMOS inverter with RD, and its PSpice schematic.

1.1 We will use the command **Draw/Get New Part** to get the various components: **VDC** for DC voltage sources Ve and V_{DD}, **EGND** for ground and **MbreakN3** for the NMOS transistor. Give the values V_{DD} = 5V and R_D = 90K. The output is just a wire and a text label written with the command **Draw/Text**.

To specify the parameters of the transistor, we first click the NMOS symbol (it becomes red), and then use the command **Edit/Model/Edit Instance Model (text)**. Specify as parameters: Kp = 50u, Vto = 1V in the editing window (see Figure 2). Then double click on the symbol of the NMOS and write the values of channel length and width: L = 1u, W = 2u. Remember that *u* indicates *micro* (10^{-6}) and *m* indicates *milli*(10^{-3}) prefix, V_T=Vto and K = (W / L) Kp / 2.

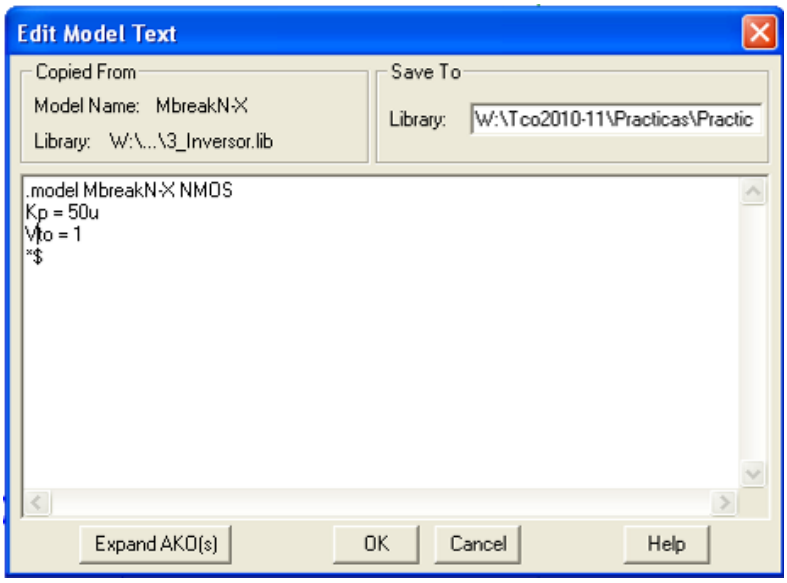


Figure 2. Model editing window.

1.2 Specify a **DC Sweep** simulation in **Analysis/Setup**. We will generate the transference curve Vs = f(Ve) of the inverter. To do this, select Ve as sweep variable, and define a variation between 0 and 5V with increments of 0.01V.

1.4 Use next the command **Analysis/simulate (F11)** to start the simulation. PROBE is activated and with the command **Trace/Add Trace (Insert)** we select the output voltage. The output is on the drain of the transistor, then a way to specify it is as V (M1:d), where M1 would be the name of the transistor (caution, look at the name of the transistor in your schematic). You should see the transference curve of the inverter, that looks like the shown in Figure 3. We can also see him putting a voltage marker  in the drain (D) of MOSFET.

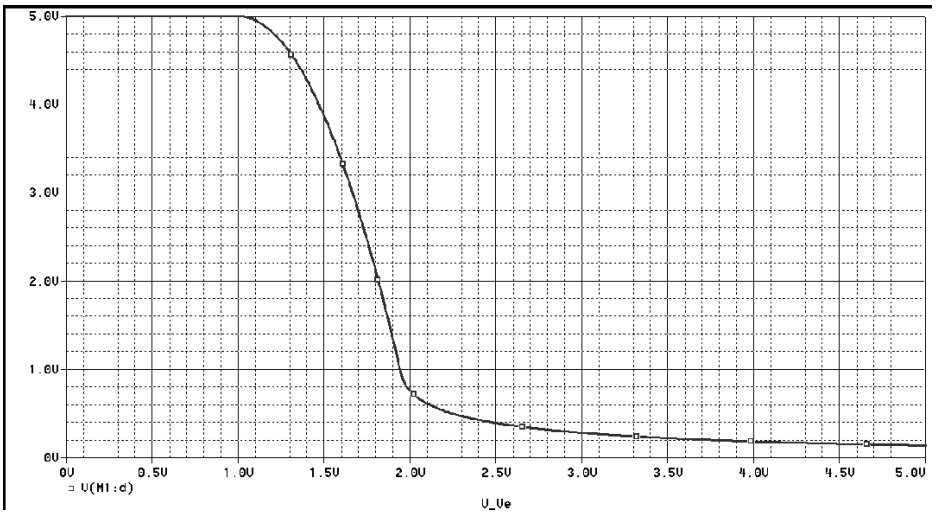


Figure 3. Transference curve of NMOS inverter.

Question 1: Measure V_{OH} and V_{OL} in the transference curve (i.e, the high and low output voltage levels, respectively), corresponding to Ve = Ve = 0V and 5V. We recommend using the **cursors**.

1.4 Plot a graph of the inverter current consumption in function of its input voltage. To do this, without leaving PROBE, add a new graph with the command **Plot/Add Plot to Window**. Select current ID(M1) which corresponds to I_{DS}, and is equivalent to the current provided by the voltage source V_{DD}.

Question 2: Measure the current in the two states using the cursors. In what state is the circuit consuming current, the "0 " or the "1"? Why?

1.5 Go back to *Schematics* and vary the value of R_D to 10k and 200k. Simulate and analyze the influence on the output logic levels and power consumption.

Question 3: What value of R_D enhances the V_{OL} logical level? Discuss the response taking into account the resistive divider formed between R_D and R_{ON}:

$$V_{\mathrm{OL}} = \frac{\mathrm{R}_{\mathrm{ON}}}{R_{ON} + R_D} \times V_{DD}$$

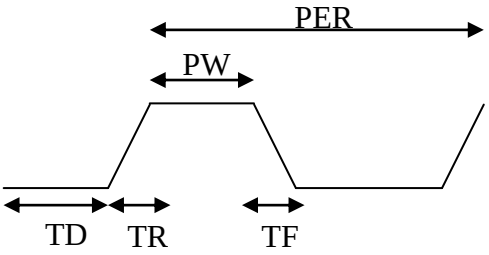
Question 4: What value of R_D improves (reduces) the current consumption? Discuss the response using the current flowing through the loop DS:

$$I_{DS} = \frac{V_{DD}}{R_{ON} + R_D}$$

To view the power dissipated by the transistor, we can insert into **Probe** the following expression: V (M1:d) * ID (M1), corresponding to P = V_{DS} * I_{DS}. One can see that between 1V and 2V, the dissipation is higher due to higher V_{DS} despite a less I_{DS}. This explains why a MOSFET transistor in switching mode is heated more than in steady state.

1.6 We want now to see the **response time** of the inverter. We will supply the input with a square wave, and analyze the output. Replace **VDC** input source (Ve) with a source of type **VPULSE**. Specify the following parameters:

- V1 = 0V (High level)
- V2 = 5V (Low level)
- TD = 10n (Initial delay)
- TR = 2n (Rise time)
- TF = 2n (Fall time)
- PW = 40n (Pulse Width-High level time)
- PER = 100n (Period –high level plus low level time)



Do not change the rest of parameters.

Place two separate voltage markers (**Voltage/Level Marker**) at the input and output.

1.7 Select a **Transient** simulation and deactivate the DC Sweep option, using the command **Analysis/Setup /Transient**. Indicate, in Transient window a **Print step** = 1n, **Final time** = 120n. *Print step* and *Final time* specify the temporal resolution and the total duration of the simulation, respectively.

1.8 Simulate the circuit with Analysis**/Simulate** command. The input and output signals are automatically displayed.

Question 5: How is the output signal with respect to the input? What is the logic function of the circuit?

1.9 Connect a **0.1pF** capacitor between the output and ground (see Figure 4). This parasitic capacitor models the transistor and the output wires capacities. Vary R_D (10k, 90k, 200k) and repeat the previous Transient analysis, visualizing the input and output signals. Look at the **delay** of output signal with respect to the input signal. Figure 5 illustrates how to measure the delay of the two transitions in a generic case.

Question 6: What happens with the delay if we increase R_D? Which of the 2 delays are more influenced by R_D: the delay in the transition L→H (t_{PLH}) or in H→L (t_{pHL}) of the output signal? Measure using the cursors both delays for R_D= 90k.

We can observe that the delay t_{PLH} increases with increasing R_D. This is because in the transition L→H, the capacitor is charged through R_D, increasing exponentially its voltage up to $V_{DD,}$ as shown in the following charge equation: $V_s = V_{DD}\left(1 - e^{-t/R_D C_1}\right)$. The time for charging the capacitor is proportional to the product $R_D C_1$ (time constant).
However, in a H→L transition the capacitor is discharged by the MOSFET transistor, which operates in linear region with a very small equivalent resistance R_{ON}. In this case the discharge equation is the following: $V_s = V_{DD} e^{-t/R_{on}C_1}$. The time constant is now $R_{ON}C_{1,}$ and the discharge time is proportional to this constant. Due to the fact that R_{on} << R_D, the delay t_{PHL} in this case is smaller than t_{PLH} and it does not depend on R_D.

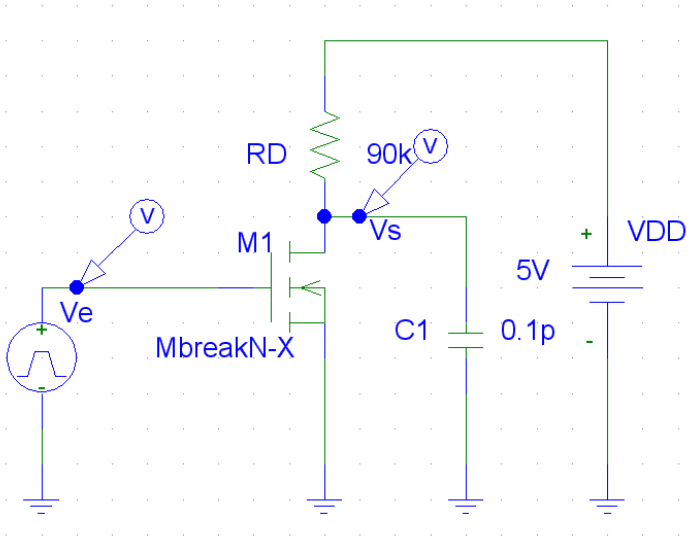


Figure 4. Inverter with a parasitic capacitor.

Question 7: Why is it said that the value of R_D is chosen looking for a compromise between power consumption, logic levels and speed?.

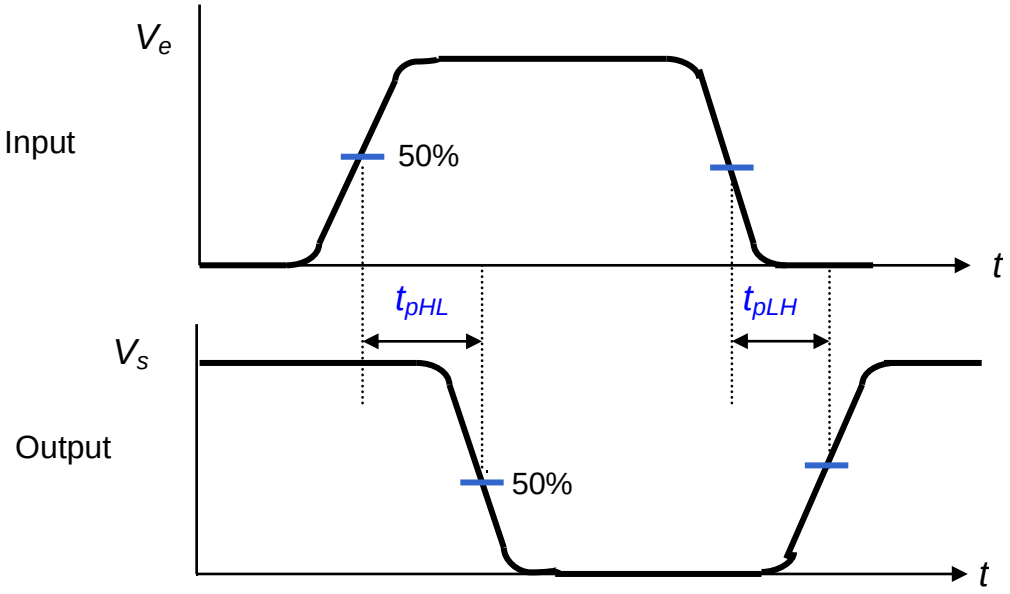


Figure 5. Delays of he output signal with respect to the input signal.

2. Other NMOS gates

We will now simulate an NMOS gate, such as in Figure 6.

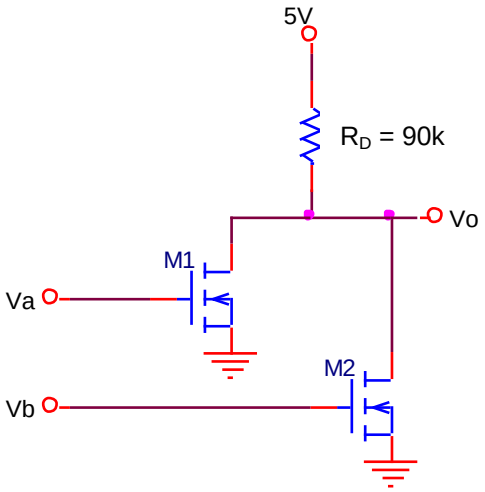


Figure 6. Two input NMOS gate.

2.1 Edit the circuit using *Schematics*. Use the same model for NMOS transistors than viewed in the inverter of section 1. Connect two **VPULSE** sources in Va and Vb. One of them will have the same parameters than the used in the inverter case (see Section 1.6). Modify the other to get the 4 logical combinations of Va and Vb: 00, 01, 10, 11. You can do this for example, by a temporal scrolling (delay) of 20nS (the same parameters except **TD = 30n**).

2.2 Make a **Transient** analysis type, with a **Print step** = 1n, **Final time** = 100n

We will add in **Probe** a plot for each signal (**Plot / Add plot to Window**), to display the three signals (two inputs and the output) without overlapping them. After that, we will select in each plot the corresponding signal: V(Va: +), V(Vb: +) and V (M1: d).

Question 8: What logic function is performed?

Question 9: Measure the Vo value using the cursors, for the input combinations 01, 10 and 11. Have you noticed something different? Justify the results given that the NMOS transistor works as an R_{on} resistor when the input is "1. "

WARNING, before turning off the computer, delete any file that is stored locally (My Documents, Desktop, etc.).