Computer Architecture and Engineering - 3rd Year - ETSINF - UPV
Exercises of Unit 2. "Pipelined computers"

Basic pipelining

MIPS data path

Ejercicio 2.1. A MIPS64-compatible processor integrates a pipeline of 5 stages:

IF: Instructions fetch.

ID: Instructions decoding and reading of register operands.

EX: ALU operation and PC updating in branch instructions.

M: Memory access in load and store instructions.

WB: Writing results back to registers

The machine solves control hazards using the delayed branching. It also integrates two separated caches, one for instructions and another for data, and a register file providing two read and one write ports.

n iterations of the following loop are executed on the processor:

```
        ...
L :     ld $t1,X($t2)
        dadd $t1,$t1,$t3
        sd $t1,X($t2)
        daddi $t2,$t2,8
        daddi $t4,$t4,-1
        bnez $t4,L
        nop
        nop
```

1. Draw a diagram indicating, for each instruction the clock cycle and the stage it has under completion. Consider only the first loop iteration. Compute the CPI and the execution time obtained according to the number of iterations n. Consider the following cases:

   a) Data hazards are solved using stalls.

   b) Data hazards are solved using short circuits.

Ejercicio 2.2. The following high-level code is available:

```
typedef struct elem
            int x[1..10];
            *elem next;
          ;

  int cont;
  *elem p;

...
```

```
do
  cont = cont + 1;
  p = (*p).next;
 while (p != NULL);
...
```

The type `int` and pointers take 32 bits. Constant `NULL` is represented with a 0. The compiler produces a loop as the following one:

```
; cont is located in R2
; p is located in R1
...
eti: add r2, r2, #1
     lw r1, 40(r1)
     bnez r1, eti
     nop          ; as many nops as necessary
```

This code executes on different versions of a processor pipelined in the following 5 stages:

IF: Instruction fetch.

ID: Instruction decoding and reading of register operands (during the 2^{nd} part of the clock cycle).

EX: ALU operation.

ME: Memory access in loads and stores.

WB: Result is written back to the destination register (during the 1^{st} part of the clock cycle).

The processor works at 100 MHz. It solves data hazards using the short-circuit technique and control hazards using delayed branching.

Compute, for each one of the following cases, the *branch delay slot* (i.e. how many instructions are affected by the delayed branch) and the CPI, MIPS and execution time of the processor. Assume in your computation that the loop is executed 10.000 times:

1. The computation of the effective address and the branch condition, and the update of the PC are performed during the ID stage. A *Harvard* architecture is available (i.e. data and instructions cache are separated).

2. The computation of the effective address and the branch condition, and the update of the PC are performed during the ID stage, but a shared instruction and data cache is used.

3. The computation of the effective address and the branch condition is performed during the EX stage, and the update of the PC is carried out during the MEM stage. In this case, a *Harvard* architecture is considered.

Ejercicio 2.3. A 2000$ computer incorporates a MIPS/LC processor. This processor has a MIPS-like pipelined instruction unit with 5 stages (IF : instruction fetch, ID : instruction decode, EX : execution, MEM : memory access, and WB : write into the register file). It incorporates a single cache for data and instructions, its *branch slot* is of 1 instruction, it works at 80MHz and it solves data hazards using the short-circuiting technique. A public domain compiler is installed in the considered computer. It compiles the following code:

```
do {
  if (v[i] != 0) {
    temp = v[i];
    v[i] = w[i];
    w[i] = temp;
  }
  i = i-1;
} while (i != 0);
```

and generates the following one:

```
etii:   ld r2,v(r1)
        beqz r2,etii2
        nop
        ld r3,w(r1)
        sd r3,v(r1)
        sd r2,w(r1)
etii2:  dadd r1,r1,-8
        bnez r1,etii1
        nop
```

The loop is typically applied on vectors containing a 80 % of components whose value is 0.

1. Compute the average CPI for handling vectors with big sizes (with n elements).
2. Assume that the original loop represents a normal workload of this computer. In order to improve the performance of the system, two options are considered:

   - Replace the existing processor with the new version MIPS/ST, which incorporates separate data and instruction caches. The resulting computer increases its price in 200$.
   - Buy a new commercial compiler, whose cost is of 200$, able to optimize the generated code by reducing in 3 clock cycles each loop iteration in which $v[i] \neq 0$ and in 2 cycles each iteration in which $v[i] = 0$. The number of instructions is not modified.

   Is any one of these options interesting? If it is, which one should be applied? Reason your answers from a cost/performance perspective, and assume that only 200$ are available for investment.

Ejercicio 2.4. The instruction cycle of an non-pipelined *load/store* processor is defined in terms of the following phases, whose duration is provided within a parenthesis:

- LI (10 ns): instruction fetch.
- DI (5 ns): instruction decoding and source register read.
- EXE (10 ns): computation of effective addresses in L/S instructions, operations in ALU instructions, condition and new PC value in branch instructions.
- EPC (5 ns): PC update in a branch instructions.
- MEM (10 ns): Memory access in L/S instructions
- ER (5 ns): Write the value of destination registers in store and ALU instructions.

The control circuitry manages the aforementioned phases according to the operation code of each instruction. The clock works at 200 MHz, so certain phases executes in 1 cycle and others in 2 cycles. All instruction cycles start with phases LI and DI but depending on the type of instruction, the other phases are (the frequency of each type of instruction is indicated in parenthesis):

- Load instructions (20 %): EXE, MEM and ER
- Store instructions (10 %): EXE and MEM
- ALU instructions (50 %): EXE and ER
- Branch instructions (20 %): EXE and EPC

This processor is expected to be pipelined, by using registers with 2 ns of delay and a clock with a null skew. The WPC phase disappears and all the branch-related logic is moved to the DI stage, whose duration is increased to 10 ns. So, the pipelined version of the processor integrates 5 stages LI, DI, EXE, MEM y ERB. Real measures are obtained from this new processor and it is observed that (i) 5 % of load instructions generate 1 stall due to a data hazard and, (ii) the compiler fills 10 % of the *branch delay slot* cases with a `nop` instruction.

Taking this information into account, compute:

1. CPI of the non-pipelined processor.
2. Clock frequency of the pipelined processor.
3. Number of instructions executed by the pipelined processor with respect to the non-pipelined one.
4. CPI of the pipelined processor.
5. Speed-up obtained through pipelining.

Ejercicio 2.5.

A 5-stage pipelined processor is available (IF: instruction fetch; ID: instruction decoding and register file read; EX: ALU operation; MEM: memory access and WB: write to the register file). The processor integrates the MIPS instruction set and it has a separate instruction and data cache. Its clock frequency is of 200 MHz. Data and control hazards are solved using respectively the *forwarding* technique and inserting 2 stalls each time a branch instruction appears.

Programs execute, in average, 18 % of branch, 39 % of load/store and 43 % of arithmetic instructions. Loads are 2 times more frequent than stores. *bytes* and *halfwords* accesses are 20 % of all memory accesses. The frequency of data hazards between a LOAD instruction and another following one consuming the data loaded from memory is the following one:

Frequency: 25 %	Frequency: 15 %
`LOAD R1, ...` Instructions reading `R1` ...	`LOAD R1, ...` Instruction not reading `R1` Instruction reading `R1`

In order to improve the performance, the following modifications are proposed:

- Remove from the instruction set those instructions providing access to *bytes* and *halfwords*. As a result, programs requiring such functionality must use other processor instructions:

`LB R1,x`
or
`LH R1,x`
	`LW R1,x'`
	`SRL R1,R1,#pos`
	`AND R1,R1,#masc`

`SB R1,x`
or
`SH R1,x`
	`LW R2,x'`
	`SLL R1,R1,#pos`
	5 more ALU instrutcions
	`SW x',R1`

- Since the processor design has been simplified, increase its clock frequency.

Answer the following questions:

1. CPI of the original processor.
2. Number of instructions of the modified processor.
3. CPI of the modified processor.
4. The minimum clock frequency that should be attained in order to justify the inclusion of the proposed modifications.

Ejercicio 2.6. A computer with memory-register architecture has a 6-stage pipelined instruction cycle:

- F: Instruction fetch and PC increment.
- RF: Decoding and register file read (2^{nd} part of the clock cycle).
- ALU1: Computation of the effective address in memory accesses and branches.
- MEM: Memory access.
- ALU2: Arithmetic operation, evaluation of branch conditions and new PC updating.
- WB: Write to the register file (1^{st} part of the clock cycle)

All instructions are executed in 6 stages. There are two types of arithmetic instructions:

Type R: ALUop Rd,Rs,Rt

Type M: ALUop Rd,Rs,desp(Rt)

1. In order to avoid structural hazards, how many adders are (at least) required for pipelining purposes? Determine the minimum number of read/write ports in the file register and in the memory, in order to avoid structural hazards.
2. If the machine uses the delayed branch technique, which is the value of its delay- slot?
3. Is it interesting to apply a *predict-taken* strategy towards positions in the code preceding the branch? If it is, how many clock cycles of penalty are induced by correctly predicted branches?

Ejercicio 2.7.

The following instruction-time diagrams correspond to the execution of various code fragments from various computers. Determine for each of them, which technique is used for solving data hazards (stall insertion or short-circuit) and control hazards (stall insertion, *predict-not-taken* or delayed branch), and in which stage is the PC updated.

1.
```
L      LW r2,a(r1)    IF ID EX M  WB
L+4    ADD r3,r2,r3      IF ID ID EX M  WB
L+8    ADD r3,r4,r3         IF IF ID EX M  WB
L+12   SUB r1,r1,#4               IF ID EX M  WB
L+16   BNEZ r1, L                    IF ID EX M  WB
L+20   SW z(r0), r3                     IF ID
L+24   ADD r3,r0,r0                        IF
L      LW r2,a(r1)                            IF ID EX M  WB
```

2.
```
L     LW r2,a(r1)    IF ID EX M  WB
L+4   ADD r3,r2,r3      IF ID ID EX M  WB
L+8   ADD r3,r4,r3         IF IF ID EX M  WB
L+12  SUB r1,r1,#4            IF ID EX M  WB
L+16  BNEZ r1, L                 IF ID EX M  WB
L+20  SW z(r0), r3                  IF IF IF
L     LW r2,a(r1)                             IF ID EX M  WB
```

3.
```
L     LW r2,a(r1)    IF ID EX M  WB
L+4   SUB r1,r1,#4      IF ID EX M  WB
L+8   ADD r3,r2,r3         IF ID ID EX M  WB
L+12  BNEZ r1, L              IF IF ID EX M  WB
L+16  ADD r3,r4,r3                IF ID ID EX M  WB
L     LW r2,a(r1)                    IF IF ID EX M  WB
```

Multicycle operators

Ejercicio 2.8. A MIPS processor is available. It supports the following multi-cycle instructions:

- Pipelined Adder / Subtracter (Tev=2, IR=1)
- Pipelined Multiplier (Tev=3, IR=1)
- Conventional Divider (Tev=4, IR=1/4)

In this processor, structural and data hazards are detected during the ID stage, inserting stall cycles when necessary. Short-circuits are also used.

Show the execution diagram of the following fragment of code:

```
L.D    F1, 0(R1)
DIV.D  F4, F0, F1
ADD.D  F2, F3, F4
L.D    F4, 4(R1)
MULT.D F3, F4, F2
L.D    F5, 8(R1)
```

The supplied diagram must represent the stages crossed by each instruction using the following notation: IF (fetching stage), ID (decoding stage), EX (monocyle execution stage), A1, A2 (adder/subtracter execution stages), M1, M2, M3 (multiplier execution stages), D1, D2, D3, D4 (divider execution stages), ME (memory access stage) and WB (register writing stage).

Ejercicio 2.9.

A processor executes the following loop computing $\vec{z} = A\vec{x} + B\vec{y}$:

```
loop: l.d F0,x(r10)
      l.d F1,y(r11)
      mult.d F4,F2,F0;  F2 contains A.
      mult.d F5,F3,F1;  F3 contains B.
      add.d F6,F4,F5
      daddi r14,r14,-1
      daddi r10,r10,8
      daddi r11,r11,8
```

```
s.d F6,z(r12)
daddi r12,r12,8
bnez r14,loop
nop
```

The processor provides two register files to store integer and floating point data. In addition, the following multi-cycle operators are available for floating point operations:

- A pipelined multiplier with $T_{ev} = 5$ and $IR = 1$, with stages M1, M2, etc.
- A non-pipelined adder with $T_{ev} = 3$ and $IR = 1/3$, with stages A1, A2, etc.

Other instructions are executed using a classic pipeline of 5 stages (IF,ID,EX,ME,WB). Data hazards are solved using short-circuits and inserting stalls whenever necessary. Conditional branches use the *predict-not-taken* technique. Branch condition and destination address are computed along ID stage. If the branch is taken, then the PC is updated with the new destination address at the end of such stage.

It is required:

1. The instructions-time diagram of the first loop integration and the first instruction of second loop iteration.
2. Assuming the equality of all loop iterations, compute the average loop CPI for n iterations.
3. In order to speed up the loop execution, two alternatives are under study: a) replace the non-pipelined adder by a pipelined one with $Tev = 3$ and $IR = 1$, of b) replace the pipelined multiplier by a non-pipelined one with $Tev = 2$ and $IR = 1/2$. Which option is the most suitable one for reducing the loop execution time? Justify your answer.

Static instruction scheduling

Ejercicio 2.10. A computer providing an MIPS-compatible instruction ser is available. The following sequence of code is executed in this computer:

```
i1       L.D F0,X(R1)
i2       MULT.D F0,F0,F4
i3       L.D F2,Y(R1)
i4       ADD.D F0,F0,F2
i5       S.D F0,Y(R1)
i6       DSUB R1,R1,#8
i7       BNEZ R1,L
i8       L.D F0,X(R1)
i9       MULT.D F0,F0,F4
i10      L.D F2,Y(R1)
i11 L:   DADD R1,R0,#dir
```

Identify at least two dependencies of each type in the above fragment of code.

Ejercicio 2.11. Consider the following MIPs assembler code:

```
loop:   L.D F0, 0(R1)
        MULT.D F0, F0, F10
        ADD.D F0, F0, F11
        S.D F0, 0(R1)
        DADD R1, R1, #8
        BNE R1, R3, loop
```

This code is executed on a MIPS where integer instructions traverse the following pipeline: IF (instruction fetch), ID (instruction decoding, source register reading and hazard detection) EX (execution), M (memory access) y WB (writeback), while floating point instructions follow these stages: IF, ID, En (execution in the corresponding multicycle operator) and WB. Data hazards can be solved using short-circuits, inserting the necessary stalls in ID, and control hazards through *predict-not taken*, updating the PC in ID.

The processor works at 4 GHz and the CPI for ALU instructions is 1.

Multi-cycle functional units have the following features:

Operator	Number	Latency	Type
Multiplication	1	3 cycles	Pipelined
Add/Sub	1	3 cycles	Pipelined

1. Identify a data dependency, an antidepency, and output dependency and a control dependency in the original code.

2. Provide the instructions–time diagram for the first loop iteration. Compute the execution time for n iterations.

3. Show the code resulting from the use of the *loop-unrolling* technique. Without providing the instructions–time diagram, compute the execution time of the resulting code and the speed-up (if any) wrt the original one.

Dynamic branch prediction

Ejercicio 2.12.

A processor has a dynamic branch predictor of type BTB (*Branch Target Buffer*) that delivers its prediction during the instruction fetch stage. The target address and branch condition are computed at the 3rd stage of the instruction cycle. The probability that a branch is found in the table is 80 % and the predictor accuracy is 90 %. The branches are effective in 60 % of the cases. Questions:

1. Show the instructions that will be fetched after the branch and their i–t diagram for the following options:

   - There is no entry in the prediction table and the branch is **not taken**.
   - There is no entry in the prediction table and the branch is **taken**.
   - The predictor predicts that the branch is **not taken** and the branch is finally **not taken**.
   - The predictor predicts that the branch is **not taken** and the branch is finally **taken**.
   - The predictor predicts that the branch is **taken** and the branch is finally **not taken**.
   - The predictor predicts that the branch is **taken** and the branch is finally **taken**.

   The instructions should be represented as **Branch**, the branch instruction, **PC+i** (i= 1, 2, ...), the subsequent instructions after the branch, **Dest**, the branch target instruction, and **Dest+i** (i= 1, 2, ...), the subsequent instructions after the branch target instruction. The instruction stages should be represented as **F1**, **F2**, etc.

2. Compute the average CPI for branch instructions.

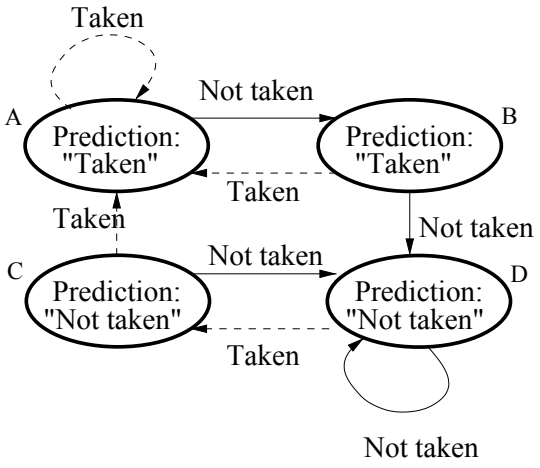
3. Suppose we can modify the BTB design in two ways. The first one increases the number of table entries, so that it stores 90 % of the executed branches. The second one uses a 2-bit predictor so that the prediction accuracy is raised to 95 %. Which modification is able to reduce the CPI of branch instructions?

Ejercicio 2.13.

Consider a processor with an instruction set similar to MIPS and a pipelined unit consisting of the following stages:

- **IF** Instruction fetch.
- **ID** Instruction decode and register read.
- **ALU** Computation of the branch target and memory access addresses.
- **MEM** Memory access.
- **EX1** First execution stage and computation of branch condition.
- **EX2** Second execution stage.
- **WB** Register write.

Two branch prediction schemes are considered for implementation in the processor. The predictors that have to be evaluated are: A *Branch Prediction Buffer* and a *Branch Target Buffer*, both of them delivering their prediction at the end of the ID stage. Both mechanisms are implemented with 4 entries in the *buffer* and use a 2-bit predictor whose operation is illustrated in the figure:



For evaluating the prediction mechanisms a test program is used, from which a fragment is shown below:

```
Address       Instructions
...
0x03          add r1, r0, r0
      lfor:
...
0x05          beqz r1, lendif
...
      lendif:
...
      ldo:
0x09          sub r8, r8, r2
0x0A          slt r3, r2, #2
0x0B          seq r4, r1, r0
0x0C          and r5, r3, r4
0x0D          beqz r5, lbreak
```

```
Address       Instructions

...
0x10          add r2, r2, #1
0x11          slt r4, r2, #3
0x12          bnez r4, ldo
      lbreak:
...
0x15          add r1, r1, #1
0x16          slt r6, r1, #2
0x17          bnez r6, lfor
0x18          sw z(r0), r8
```

Initially the *Branch Prediction Buffer* contains all entries in state "D", and all the *Branch Target Buffer* entries are empty. When a new entry is added to the *Branch Target Buffer*, its status will be "A" if the branch has been taken, and "D" if the branch has not been taken.

The final statistics of the execution of the test program are: 15 % of the instructions are conditional branches, 60 % of the branches are taken, the *Branch Prediction Buffer* succeeds in predicting 75 % of the cases, and the *Branch Target Buffer* succeeds in predicting 90 %, including cases in which there is no entry in the table (which are predicted as "not taken").

It is requested:

1. Obtain a trace of the execution of the code fragment until the "`sw z(r0), r8`" instruction is completely executed. It should show the contents of the entries of both predictors after each branch ("`beqz r1, lendif`", "`beqz r5, lbreak`", "`bnez r4, ldo`" and "`bnez r6, lfor`"). Labels should be used to record the target addresses.

Branch `beqz r1, lendif`. (r1 = 0)

BPB

Index	State
00	
01	
10	
11	

BTB

Index	Target address	State

Branch `beqz r5, lbreak`. (r5 = 1)

BPB

Index	State
00	
01	
10	
11	

BTB

Index	Target address	State

Branch `bnez r4, ldo`. (r4 = 1)

BPB

Index	State
00	
01	
10	
11	

BTB

Index	Target address	State

Branch `beqz r5, lbreak`. (r5 = 1)

BPB

Index	State
00	
01	
10	
11	

BTB

Index	Target address	State

Branch `bnez r4, ldo`. (r4 = 1)

BPB

Index	State
00	
01	
10	
11	

BTB

Index	Target address	State

Branch `beqz r5, lbreak`. (r5 = 0)

BPB

Index	State
00	
01	
10	
11	

BTB

Index	Target address	State

Branch `bnez r6, lfor`. (r6 = 1)

BPB

Index	State
00	
01	
10	
11	

BTB

Index	Target address	State

Branch `beqz r1, lendif`. (r1 = 1)

BPB

Index	State
00	
01	
10	
11	

BTB

Index	Target address	State

Branch `beqz r5, lbreak`. (r5 = 0)

BPB

Index	State
00	
01	
10	
11	

BTB

Index	Target address	State

Branch `bnez r6, lfor`. (r6 = 0)

BPB

Index	State
00	
01	
10	
11	

BTB

Index	Target address	State

2. Analyze the behavior of the BTB predictor when it mispredicts, indicating which instructions are executed after the branch. The number of lost execution cycles should be indicated. Canceled instructions should be represented as **X** in the corresponding cycle. The instructions following the branch will be represented as **pc+1**, **pc+2**, ... and the branch target instructions as **dest**, **dest+1**, etc.

3. Compute the average number of cycles per instruction (CPI) for the test program, using the BTB prediction scheme. Assume that instructions that are not branches are executed with CPI=1.

Ejercicio 2.14.

Assume the code of function `ones`, which returns (in `$v0`) the number of bits equal to 1 in *a*rgument register (`$a0`). The way to proceed is to obtain the LSB of the argument (with `andi $t1,$a0,1`), to increase the count in case that LSB==1 (with `daddi $v0,$v0,1`), and then to shift right 1 bit (using `dsrl $a0,$a0,1`). These operations are repeated 64 times to complete the job.

```
ones:  li $t0,64        # Number of iterations
       li $v0,0         # Initial count = 0
loop:  andi $t1,$a0,1   # $t1 = LSB of register $a0
       beqz $t1,next    # if (LSB!=0 )
       daddi $v0,$v0,1  #    $v0++ /* Increase count - LSB=1 */
next:  dsrl $a0,$a0,1   # Shift right $a0 1 bit
       daddi $t0,$t0,-1 # Pending iterations
       bgtz $t0,loop    # Next iteration
       jr $ra           # Exit of the function
```

Note that the code contains two conditional branches and one jump instruction:

`beqz $t1,next` taken each time that LSB==0

`bgtz $t0,loop` closes the loop

`jr $ra` unconditional jump.

The processor pipeline consists of the typical 5 stages, and implements a branch predictor. PC is written at stage *EX* (i.e., the branch latency is 2 cycles long). Note that no stall cycle appears due to structural or data hazards.

Obtain the number of executed instructions, the number of stall cycles, and the execution time (in processor cycles) of the function in the following cases:

1. Assuming a *predict-not taken* predictor and `$a0`$=-1$ (0xFFF...FFF).
2. The processor implements a BTB for (conditional) branches with a 1-bit predictor, which predicts the target address at *IF* stage and applies *predict-not taken* for return of function `jr $ra`. Function `ones` is called the first time with `$a0`$=-1$ (0xFFF...FFF)
3. The previous BTB uses a 2-bit hysteresis branch predictor. Function `ones` is called the first time with `$a0`=0x8080 8080 8080 8080

Dynamic instruction scheduling and speculation

Hardware speculation

Exercise 2.15.

A MIPS processor applies dynamic instruction scheduling with speculation to all instructions. Thus, all instructions traverse the following stages:

- **IF** Instruction fetch.

- **I** Instruction decoding and issue following the Tomasulo algorithm with speculation.
- **Ei** Execution in the corresponding operator.
- **WB** Transfer of results through the internal bus.
- **C** Commit stage. Results are written to the corresponding destination register.

All stages take 1 cycle, except the **Ei** stage whose duration varies from one operator to another. The processor has a BTB predictor whose prediction is obtained during the **IF** stage.

The main characteristics of the functional units of the processor are:

Type	Units	Latency (cycles)	Additional info
Integer arithmetic	1	1	4 reservation stations
FP Multiplication	1	3	Pipelined, 4 reservation stations
FP Add/Sub	1	2	Pipelined, 4 reservation stations
Load/Store	1	2	Pipelined 2 load buffers, 2 write buffers

The following code is under execution on the considered processor:

```
      l.d f1,d(r0)
      l.d f3,n(r0)
loop: sub.d f4,f2,f1
      mul.d f1,f1,f4
      mul.d f3,f3,f4
      c.lt.d f1,f0
      bc1t loop      ; Jumps if f1 < f0
      s.d f3,q(r0)
      ...
```

Instruction `c.lt.d f1,f0` is evaluated in the add/sub unit, and writes its result in an internal register (floating point state register). Instruction `bc1t loop` jumps if the floating point state register is *true*, thus computing the branch target address and evaluating the condition in the integer unit.

When the code starts its execution, the *reorder buffer* and the operators are empty. The register file and the memory contain the following values:

F0	F1	F2	F3	F4	d(r0)	n(r0)
1.0	0.0	2.0	0.0	0.0	1	0.25

Take into account that, for obtaining the considered results, each instruction in the loop must be executed only once. However, assume the predictor **incorrectly** predicts that the branch instruction `bc1t loop` is **taken** .

1. Draw the instructions-time diagram from the cycle when instruction `l.d f1,d(r0)` executes the **IF** stage until the cycle when instruction `s.d f3, q(r0)` finishes completely.
2. Show the state of the *reorder buffer*, the reservation stations, the read and write buffers, and the register file at the end of the cycle when the instruction `sub.d f4,f2,f1` of the first loop iteration is committed (it executes its **C** stage).

Note: In order to depict the various stages in the instructions-time diagram use the following notation: `M1,M2,...` for the multiplication/division stages, `A1,A2,...` for the add/sub stages, `AC,L1,L2,...` for the load/store unit, and `E1,E2,...` for the integer unit.

Exercise 2.16. A MIPS64 binary compatible processor applies dynamic instruction scheduling with *hardware* speculation. Instructions traverse the following pipeline stages:

- **IF** Instruction fetch.
- **I** Instruction decoding and Instruction issue following the Tomasulo algorithm with speculation.
- **Ei** Execution in the corresponding operator.
- **WB** Transfer of results through the internal bus (the transferred result is not available until the next cycle).
- **C** Commit stage. Results are written to the destination register.

All stages take one cycle, except the **Ei** stage whose duration varies from one operator to another. The processor has a perfect branch predictor that obtains the prediction and the branch target address during the **IF** stage.

The main functional units of the processor have the following characteristics:

Type	Units	Latency (cycles)	Additional info
Integer arithmetic	1	1	3 reservation stations (e1..e3)
FP add/sub	1	2	Pipelined, 3 reservation stations (a1..a3)
FP multiplication	1	4	Pipelined, 2 reservation stations (m1..m2)
Load/Store	1	2	Non Pipelined 3 read buffers (l1..l3), 3 write buffers (s1..s3)

On such processor it is considered the execution of the following fragment of code:

```
        l.d     f0, A(r0)
loop:   l.d     f2, X(r1)
        mult.d  f4, f2, f0
        l.d     f6, Y(r1)
        sub.d   f4, f4, f6
        s.d     f4, Z(r1)
        dsub    r1, r1, #8
        bnez    r1, loop
```

When the code starts its execution, the *reorder buffer* and the operators are empty. The initial value of register R1 is 80. The values accessed from vector X and Y are represented by `x1`, `x2`, ... and `y1`, `y2`, ... respectively. The value that is located at the address `Mem[r0 + A]` is `a`.

Show the instructions-time diagram for the first two iterations of the loop, and the state of the various data structures of the processor at the end of the cycle where the branch "`bnez r1, loop`" is fetched for the second time. Compute the MFLOPS that the execution of the considered piece of code may reach if it was executed on a 150 MHz processor.

Note: Represent the execution stages **Ei** following this notation: EX for integer operations, Ai for floating point additions and substractions, Mi for floating point multiplications, and AC, Li for load and stores, where the subindex indicates the number of cycles in execution (1, 2 , ...).

Exercise 2.17.

In order to evaluate the performance of a certain computer, the following loop code is used $\vec{y} = a \cdot \vec{x}$. This computer has a processor similar to MIPS but implements hardware speculation for all the instructions. The instructions execute the following stages:

- **IF** Instruction fetch.
- **I** Instruction decode and issue following Tomasulo's algorithm with speculation.
- **Ei** Execution at the corresponding operator.

- **WB** Result transfer through the common data bus.
- **C** Commit stage. Result writing into the destination register. Prediction checking and instruction canceling, if necessary.

All stages last one clock cycle, except stage **Ei** whose duration depends on the operator. The processor has a **two**-bit branch predictor of type *branch target buffer* that delivers the prediction at the end of stage **IF**.

The characteristics of the functional units of the processor are:

Type	Units	Latency (cycles)	Additional info
Integer arithmetic	1	1	3 reservation stations
FP multiplication	1	3	Pipelined, 3 reservation stations
Load/Store	1	2	Non pipelined, 3 load + 3 store buffers

The code generated by the compiler for the loop is:

```
loop:   l.d f2,x(r1)
        mult.d f2,f2,f0
        s.d f2, y(r1)
        dsub r1,r1,#8
        bnez r1,loop
        trap 0
```

The state of the registers and memory before the last iteration, is as follows:

Reg.	R1	F0	F2	Mem	x	x+8	y	y+8
Value	8	3	2	Value	100	102	10	12

1. Draw an instructions-time diagram showing the execution of the instructions that are issued in the last loop iteration, until the cycle in which the `trap 0` instruction is fetched. Note that the predictor will **incorrectly** predict the `bnez r1, loop` instruction (predict taken and finally not taken). In order to represent the execution stages in the diagram, please use: `M1, M2` and `M3` for the multiplication stages, `AC, L1` and `L2` for the load/store unit, and `EX` for the integer unit. For simplicity, assume that the ROB and the reservation stations are empty before starting the last iteration, and that there is no instruction in the pipeline (in other words, assume that all the instructions in previous iterations already committed).

2. Assuming that the ROB and the reservation stations are empty, and that there is no instruction in the pipeline (i.e., the *reorder buffer* and the *rob* fields in the register file are empty) before executing the last iteration, show the state of the *reorder buffer*, the register file, and memory at the end of the clock cycle in which the `s.d f2, y(r1)` instruction executes the **Commit** stage.

3. Assume now that the `bnez r1, loop` branch is not stored in the table when the loop execution begins, and that the initial value of `R1` is 160. Indicate, justifying the response, the loop execution time in cycles. Consider that the loop ends when the branch instruction in the last iteration reaches the *Commit* stage.

Multiple instruction issue

Exercise 2.18.

The code of the loop $\vec{y} = a\vec{x} + b\vec{y} + c$ is used to evaluate the performance of a given computer. Such computer has a **2-way** superscalar processor applying dynamic instruction scheduling with speculation to all instructions. The instruction pipeline has the following stages:

- **IF** Instruction Fetch.
- **I** Instruction decoding and issuing.
- **Ei** Execution in the corresponding operator.
- **WB** Result transfer through the internal bus.
- **C** Commit stage. Results are written to the destination register.

All stages take one clock cycle, except stage **Ei** whose duration depends on the operator. The processor has a *branch target buffer* predictor obtaining the prediction at the end of stage **IF**. Each transfer through the common data buses takes 1 clock cycle.

The main characteristics of the processor functional units are:

Type	Units	Latency (cycles)	Additional info
Integer arithmetic	2	1	6 reservation stations
FP Mult	1	4	Pipelined, 4 reservation stations
FP Add/Sub	1	2	Pipelined, 4 reservation stations
Load/Store	2	2	2 read buffers, 2 write buffers

The code generated by the compiler for the considered loop is the following one:

```
loop:   l.d f2,x(r1)
        l.d f4,y(r2)
        mult.d f2,f2,f0
        mult.d f4,f4,f1
        add.d f6,f3,f2
        add.d f6,f6,f4
        s.d f6,y(r2)
        dsub r1,r1,#8
        dsub r2,r2,#8
        bnez r1,loop
        trap #0
```

The state of registers and memory is the following one:

R1	R2	F0	F1	F2	F3	F4	F5	F6	x+32	x+24	y+40	y+32
32	40	3.0	0.5	2.0	2.0	0.0	0.0	0.0	100	102	10	12

1. Draw the instructions-time diagram for the first two loop iterations. Assume the predictor predicts **correctly** that instruction `bnez r1, loop` is **taken**. Detail in which stage is each instruction under execution in each cycle. Represent execution stages in the diagram using the following notation: `M1, M2, M3` and `M4` for multiplication stages, `A1, A2` for add/sub stages, `AC, L1, L2` for the load/store unit and `EX` for the integer unit.

2. Show the state of the *reorder buffer*, the reservation stations and buffers, the register file and the memory at the end of the cycle when the instruction `bnez r1,loop` of the second iteration executes stage **IF**.

Ejercicio 2.19.

Consider a superscalar processor that is binary-compatible with MIPS, able to fetch and issue up to two instructions per clock cycle. Clock frequency is 900 MHz, it has integer and floating point instructions, and it applies dynamic instruction scheduling with speculation for all the instructions. Instruction execution is split into the following stages:

IF Instruction fetch.

I Instruction decode and issue.

En Execution at the corresponding operator.

WB Result transfer through the shared data bus (the transferred result will not be available until the next cycle).

C Instruction commit stage. Result writing into the destination register. Prediction checking and instruction canceling, if necessary. Issue of memory write operations.

All stages last one clock cycle, except stage **En** whose duration depends on the operator. The execution unit has the following independent operators:

Type	Units	Latency (cycles)	Additional info
Integer/branches	2	1	6 reservation stations
Load/Store	2	2	Pipelined (linear), 6 buffers
Floating point	2	3	Pipelined (linear), 6 reservation stations

The processor solves the control hazards by using a perfect predictor with zero clock cycles penalty. Each register file has four read ports and two write ports. One clock cycle is needed to transfer the data through the shared data buses in the execution unit.

This processor executes the code obtained from the compilation of $\vec{B}(i) := x + \vec{A}(i)$:

```
loop:  DSUB R1,R1,#8
       L.D F0, A(R1)
       ADD.D F4, F0, F2
       S.D F4, B(R1)
       BNEZ R1,loop
```

Draw a diagram that indicates, for each instruction and clock cycle, what stage of the instruction is being executed. Consider only the first and second loop iteration. For representing multicycle operation stages $\mathbf{E}_{\mathrm{n}}$ in the timing diagram, please use: EX for integer operations, Ai for floating point, and AC, Li for loads and stores; where i indicates the number of the cycle under execution (1, 2, ...).

Assuming that the second iteration is representative of what happens in the rest of iterations, compute the average CPI and the MFLOPS achieved by the computer running this code fragment.

Ejercicio 2.20.

A given program spends most of its execution time performing the following vector operations:
$\vec{Y} = \vec{X} * \vec{Y} + b$
$\vec{X} = a * \vec{X}$

Such program is executed on a MIPS/S processor working at 3GHz. It applies a dynamic instruction scheduling technique based on the use of the Tomasulo algorithm with *hardware* speculation. The stages in the processor pipeline are: IF (instruction fetch), I (*issue*), En (execution), WB (1-cycle transfer through the shared data buses), and C (*Commit*). The processor is a 2-way superscalar processor and its instruction cache (stage IF) delivers two instructions aligned on an even address to stage I. Whenever only one of the two instructions is required, the other one is cancelled at stage I and it is not decoded.

The MIPS/S integrates the following multicycle pipelined operators:

MIPS/S	
Pipelined load/store units	2 operators, 2 cycles, 6 load buffers 6 store buffers
Pipelined adders	2 operators, 2 cycles, 4 buffers
Pipelined multipliers	2 operators, 3 cycles, 4 buffers
Integer/branch units	2 operators, 1 cycle, 6 buffers

and it uses a 1-bit BTB predictor that obtains its prediction during the IF stage.

Assume that the compiler has allocated the constants in registers `f0` and `f1` and it has generated the following code using a MIPS-like instruction set:

```
        .text 0x400000
  loop: l.d f2,X(r1)
        l.d f3,Y(r1)
        mul.d f3,f3,f2
        add.d f3,f3,f1
        s.d f3,Y(r1)
        mul.d f4,f0,f2
        s.d f4,X(r1)
        dadd r1,r1,#8
        bne r1,r4,loop
        trap #0 ; End of program
```

Before executing the last iteration, the ROB is empty and the state of registers and memory is the following one:

Reg.	r1	r4	f0	f1	f2	f3	Mem	x+16	x+24	x+32	y+16	y+24	y+32
Value	24	32	10	20	0.5	-1	Value	88	96	104	188	196	204

Answer the following questions and justify your answers:

1. Draw the instructions-time diagram of the **last loop iteration** for the MIPS/S. Show only those instructions reaching the *Commit* stage.
2. Indicate the number of cycles spent for running an iteration when the predictor hits and when it misses.
3. Detail in which clock cycle, from the beginning of the iteration, it can be considered that the variable `X` has been updated in memory. One of the instructions `trap #0` is not finally cancelled, in which cycle is it fetched?
4. Consider the clock cycle when instruction `l.d f2,X(R1)` is *committed* and show:
   a) The state of register f3 at the end of that cycle.
   b) The state of multiply operators at the end of that cycle.
   c) The content of the ROB entry corresponding to instruction `bnez r1,r4,loop` at the end of that cycle.
5. If the loop executes 500 times, compute the execution time (in cycles), the resulting CPI, and the execution speed in MFLOPS. Assume that, initially, the instruction at the end of the loop has never been executed before.

Ejercicio 2.21. The following assembly code for a MIPS processor implements the operation $\vec{Z} = a\vec{X} + b\vec{Y}$ conditional to the contents of the mask vector $\vec{M}$.

```
loop:   LD R3, M(R1)
        BEQZ R3, endif     ; The branch is taken if M[i] == 0
        L.D F2, X(R1)      ; Initial value of R1 = 0
        L.D F3, Y(R1)
        MULT.D F3, F1, F3  ; F1 contains b = 5.0
        MULT.D F2, F0, F2  ; F0 contains a = 2.5
        ADD.D F4, F2, F3
        S.D F4, Z(R1)
endif:  DADD R1, R1, #8
        BNE R1, R2, loop   ; R2 contains 64 * 8
```

The code is executed on a **2-way superscalar** processor that applies dynamic instruction scheduling with hardware speculation. Instruction execution is split into the following stages:

- IF - Instruction fetch.
- I - Instruction decode and issue.
- En - Execution at the corresponding operator.
- WB - Result transfer through the common data buses.
- C - Instruction commit stage.

All stages last one clock cycle, except stage `Ei`, whose duration depends on the operator. The processor solves the control hazards by using a 1-bit dynamic branch predictor of type *Branch Target Buffer*. The predictor obtains its prediction at the end of the IF stage and **updates its prediction at the Commit stage**. The register files have 4 read ports and 2 write ports. The transfer time through the common data buses is 1 cycle.

The characteristics of the functional units of the processor are:

Type	Operators	Latency	Characteristics
Integer arithmetic	2	1	8 reservation stations
Load/Store	1	2	Pipelined, 4 read + 4 write buffers
FP Add/Subtract	1	2	Pipelined, 4 reservation stations
FP Multiplication	1	4	Pipelined, 4 reservation stations

Assume that the initial content of the vector $\vec{M}$ is $1, 0, 1, 0, ...$ Thus, in the first iteration, the branch `BEQZ R3, endif` **will not be taken**. The initial predictor state is:

Branch	Prediction
`BEQZ R3, endif`	Taken
`BNE R1, R2, loop`	Taken

Questions:

1. Draw the instructions-time diagram for the first loop iteration (until the cycle in which the branch `BNE R1, R2, loop` executes the Commit stage). Show only those instructions that fit on the answer sheet. In order to represent the execution stages (En) in the diagram, please use `M1`, `M2`, `M3` and `M4` for the multiplication stages, `A1` and `A2` for the add/subtract stages, `AC`, `L1` and `L2` for the load/store stages, and `E` for the execution stage of the integer unit.

2. Show the state of the F2, F3, and F4 registers at the end of the Commit stage for the instruction `L.D F2, X(R1)` from the first iteration. The initial value of those registers is 2, 3, and 4, respectively. Show the contents of the `value` and `rob` fields. The contents of vector $\vec{X}$ is $100, 108, ...$ and the one for $\vec{Y}$ is $10, 11, ...$

Exercise 2.22.

The following figure shows the simplified instructions–time diagrams for the execution of two applications A and B on a 3-way superscalar processor. It is considered that a high latency stall happens whenever instruction issue is interrupted during two or more cycles.

0	1	2	3	4	5	6	7	8
		A						
A		A					A	A
A	A	A	A			A	A	A

0	1	2	3	4	5	6	7	8
				B				
	B			B	B	B		
B	B			B	B	B	B	B

In order to improve the processor resource utilization, the execution of multiple *threads* is under consideration.

1. From the viewpoint of how processor resources are shared, explain which are the main differences between a fine-grain, coarse-grain and simultaneous (*SMT*) multithreading.

2. Show a possible instructions–time diagram, similar to those already shown, corresponding to the execution of applications A and B on fine-grain, coarse-grain and simultaneous multithreading processors.