5.2.3 Design of general functions in CMOS Complementary Logic (1)

General case:

- NMOS and PMOS blocks are dual

  Series structures → · (AND)
  Parallel structures → + (OR)
  } → Intermediate function G

- NMOS block

  connected to ground

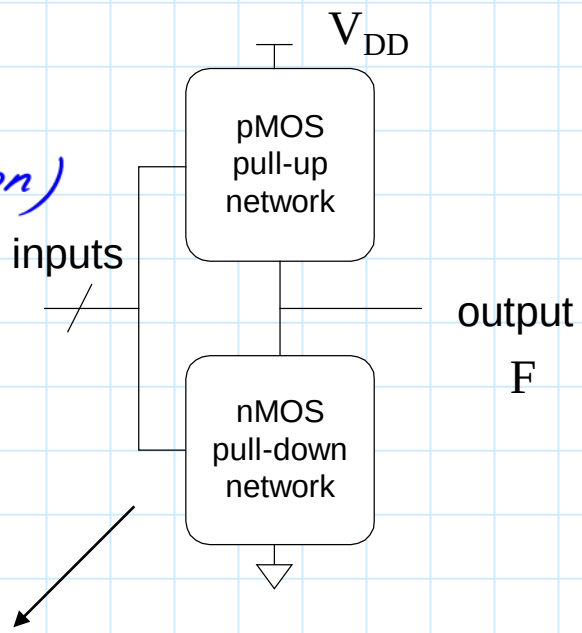
  F = $\overline{G}$ (use inverted function)

- PMOS block

  connected to VDD

  F = G, but inverted inputs

  (use direct function)

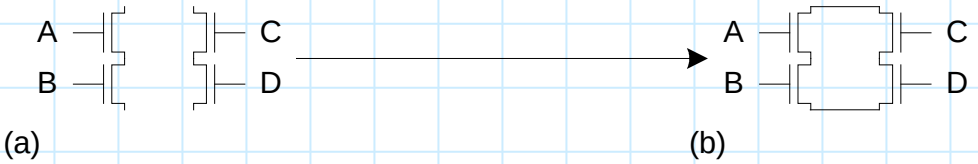


CMOS complementary logic

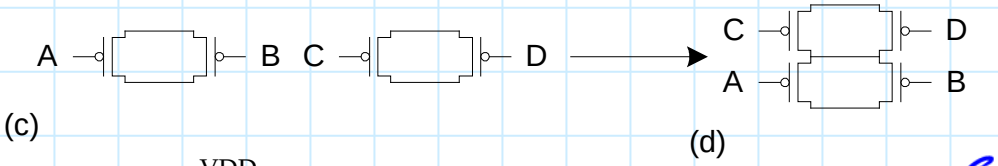
5.2.3 Design of general functions in CMOS Complementary Logic (2)

- Any inverted function can be implemented
- Ex: $Y = \overline{(A.B)+(C.D)}$ (AND-OR-INVERT-22)

$G = AB + CD$

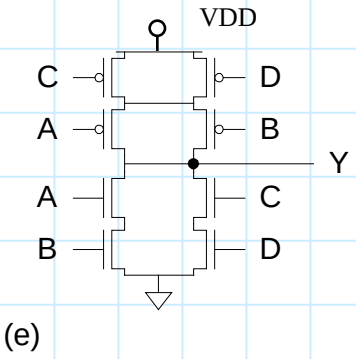


NMOS block



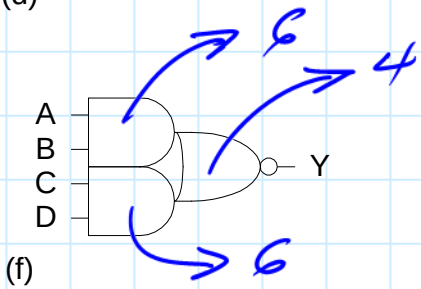
Dual structure:

PMOS block



8 transistors

Chip area and power reduction



16 transistors (double!)

5.2.3 Design of general functions in CMOS Complementary Logic (3)

Example: OAI-31

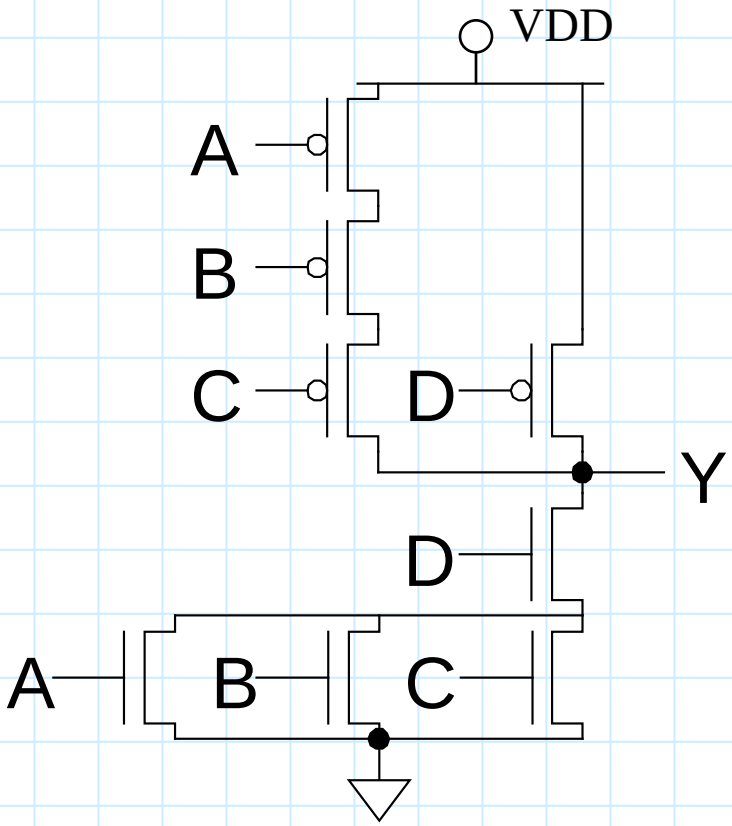
$$Y = \overline{(A + B + C) \cdot D}$$ → Take $G = (A+B+C) \cdot D$

and draw first NMOS network

5.2.3 Design of general functions in CMOS Complementary Logic (4)

Example: OAI-31

$$Y = \overline{(A + B + C).D}$$



5.2.3 Design of general functions in CMOS Complementary Logic (5)

- If the function is not inverted:
- We have two solutions:
  1. Transform it to an equivalent inverted function, applying involution and De Morgan laws:
     - NMOS block design
     - PMOS block design with dual structure of NMOS block.
  2. Design from PMOS block, inverting the inputs. NMOS block is designed with the dual structure of the PMOS.
- Example: design the carry out function of a full-adder:

$$F = AB + AC + BC$$

5.2.3 Design of general functions in CMOS Complementary Logic (3)

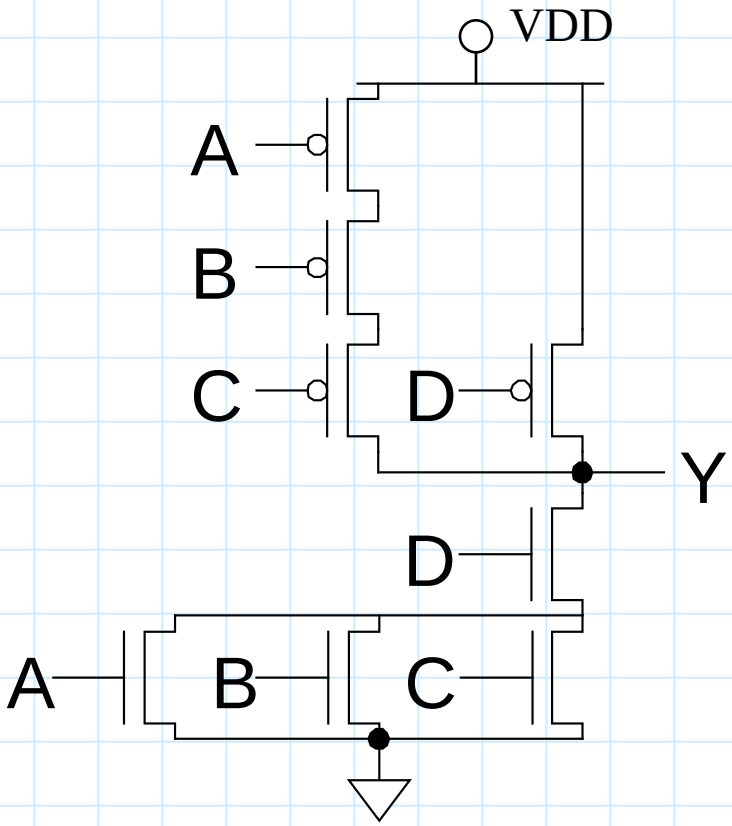
Example: OAI-31

$$Y = \overline{(A + B + C) \cdot D}$$

5.2.3 Design of general functions in CMOS Complementary Logic (4)

Example: OAI-31

$$Y = \overline{(A + B + C).D}$$



5.2.3 Design of general functions in CMOS Complementary Logic (5)

- If the function is not inverted:
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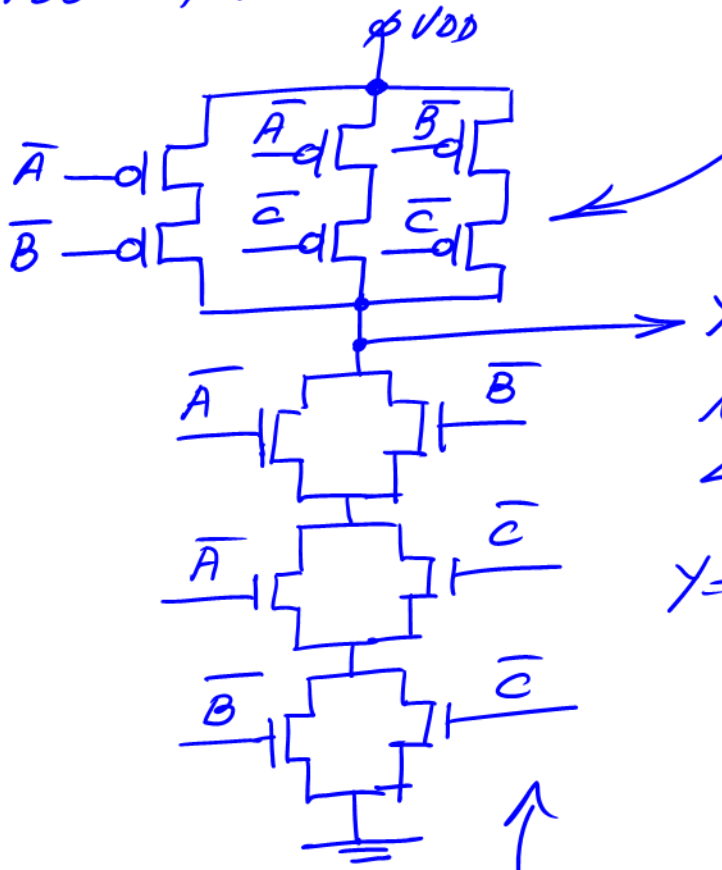
     - NMOS block design
     - PMOS block design with dual structure of NMOS block.
  2. Design from PMOS block, inverting the inputs. NMOS block is designed with the dual structure of the PMOS.
- Example: design the carry out function of a full-adder:

$$F = AB + AC + BC$$

$Y = AB + AC + BC$; $G = AB + AC + BC$ and draw first pMOS net inverting inputs



Note: Applying de Morgan Laws:

$$Y = \overline{\overline{AB + AC + BC}} = \overline{\overline{AB} \cdot \overline{AC} \cdot \overline{BC}} = \overline{(\bar{A}+\bar{B}) \cdot (\bar{A}+\bar{C}) \cdot (\bar{B}+\bar{C})}$$

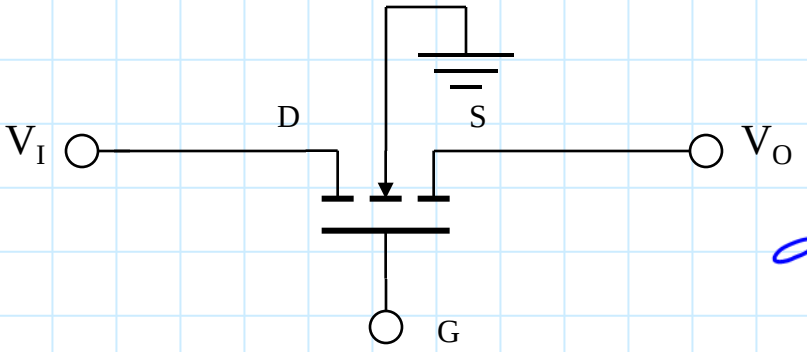
and we can design before NMOS net

5.2.4 Transmission gates (1): NMOS

- Bi-directional switch that opens or closes controlled by an external signal
  - NMOS transmission gate:
    - If $V_G = 0V \rightarrow$ Open Switch $\rightarrow V_O = 0V$
    - If $V_G = V_{DD} \rightarrow$ Closed Switch
      The transmission of "1" degrades V_T volts
      The transmission of "0" is not degraded

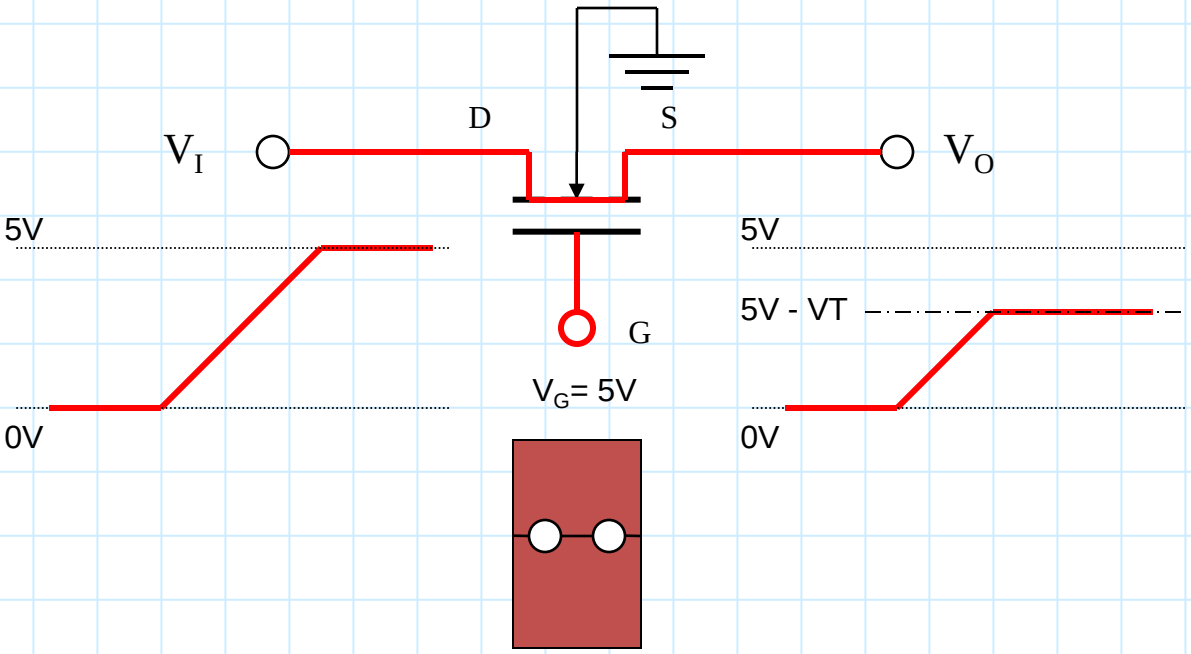
$V_O = V_I$?

$T_{ON} \Rightarrow$
$V_{GS} > V_T \Rightarrow$
$V_G - V_S > V_T \Rightarrow$
$V_S < V_G - V_T$
$V_O < V_G - V_T$



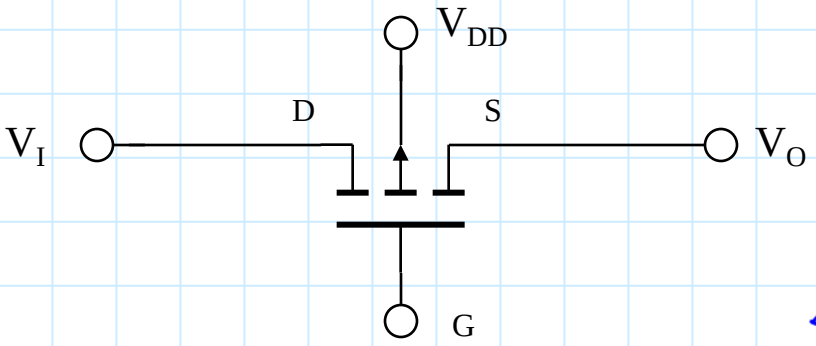
Bidirectional
$V_i \rightleftarrows V_o$
analog switch

5.2.4 Transmission gates (2): NMOS



5.2.4 Transmission gates (3): PMOS

- PMOS transmission gate
  - If $V_G = V_{DD}$ → Open Switch → $V_O = 0V$
    If $V_G = 0V$ → Closed Switch
    The transmission of "1" is not degraded
    The transmission of "0" is degraded VT



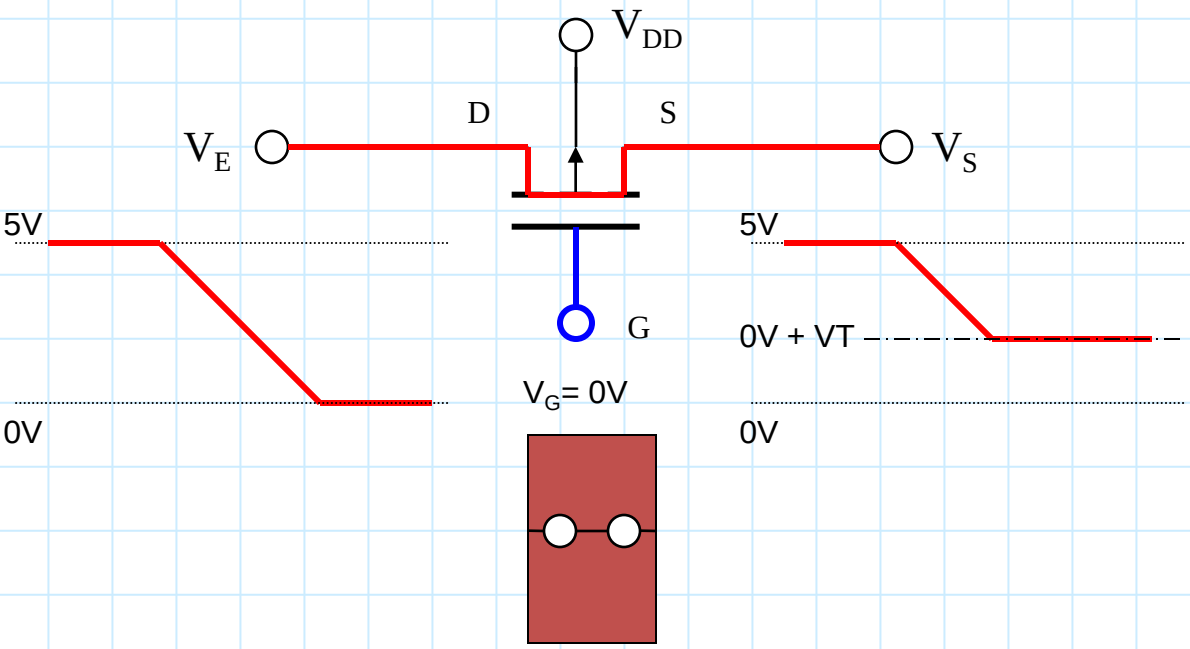
$T_{ON} \Rightarrow V_{GS} < -V_T \Rightarrow$

$V_G - V_S < -V_T \Rightarrow$

$V_S > V_G + V_T = V_T$

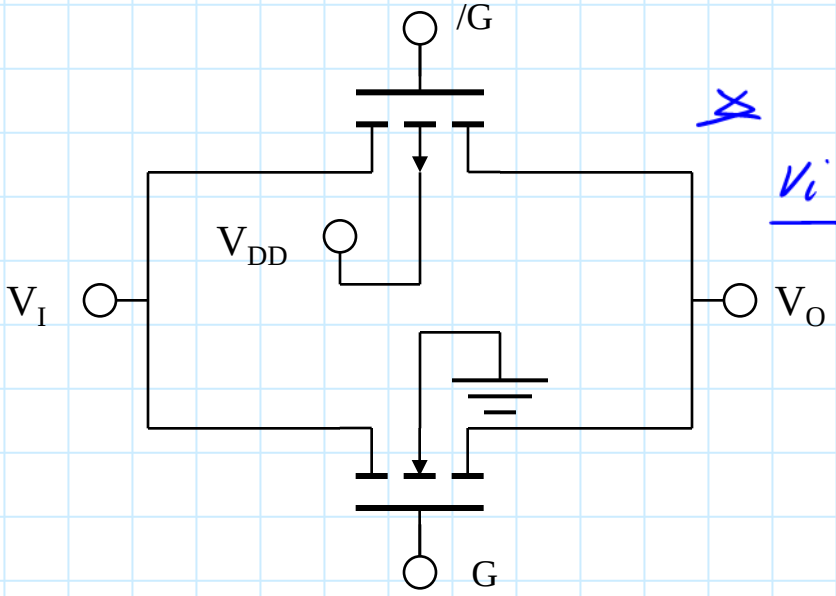
Bidirectional
Vi ⇄ Vo
analog switch

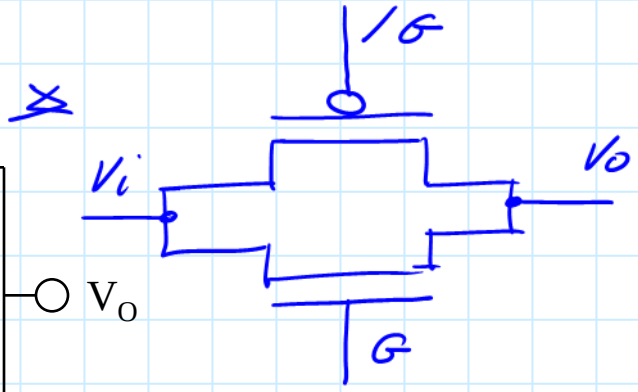
5.2.4 Transmission gates (4): PMOS



5.2.4 Puertas de transmisión (5): CMOS

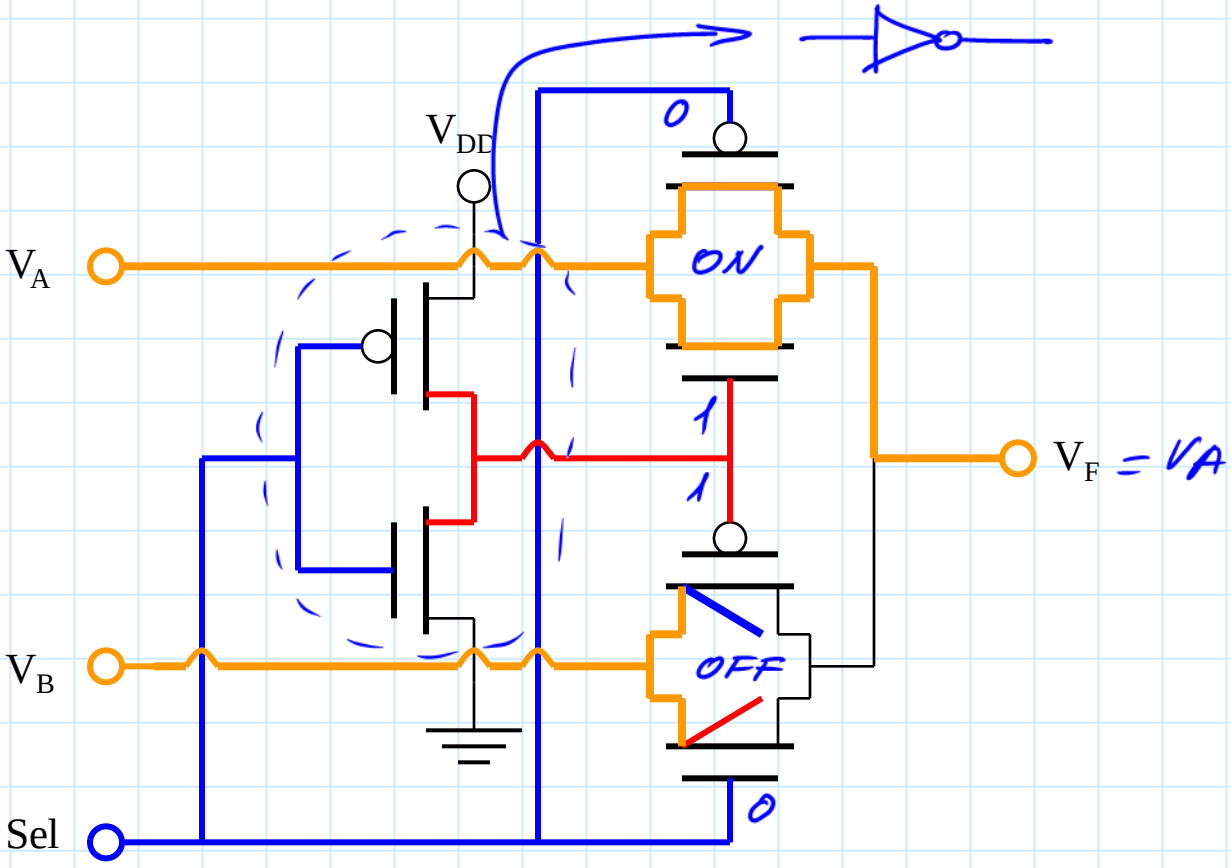
- They join the characteristics of the two gates (NMOS and PMOS), not degrading the output
  - If V_G = 0V →NMOS and PMOS **OFF** →V_O = 0V
  - If $V_G = V_{DD}$ → NMOS and PMOS **ON**
    The NMOS transmits the "0" without degradation
    The PMOS transmits the "1 " without degradation





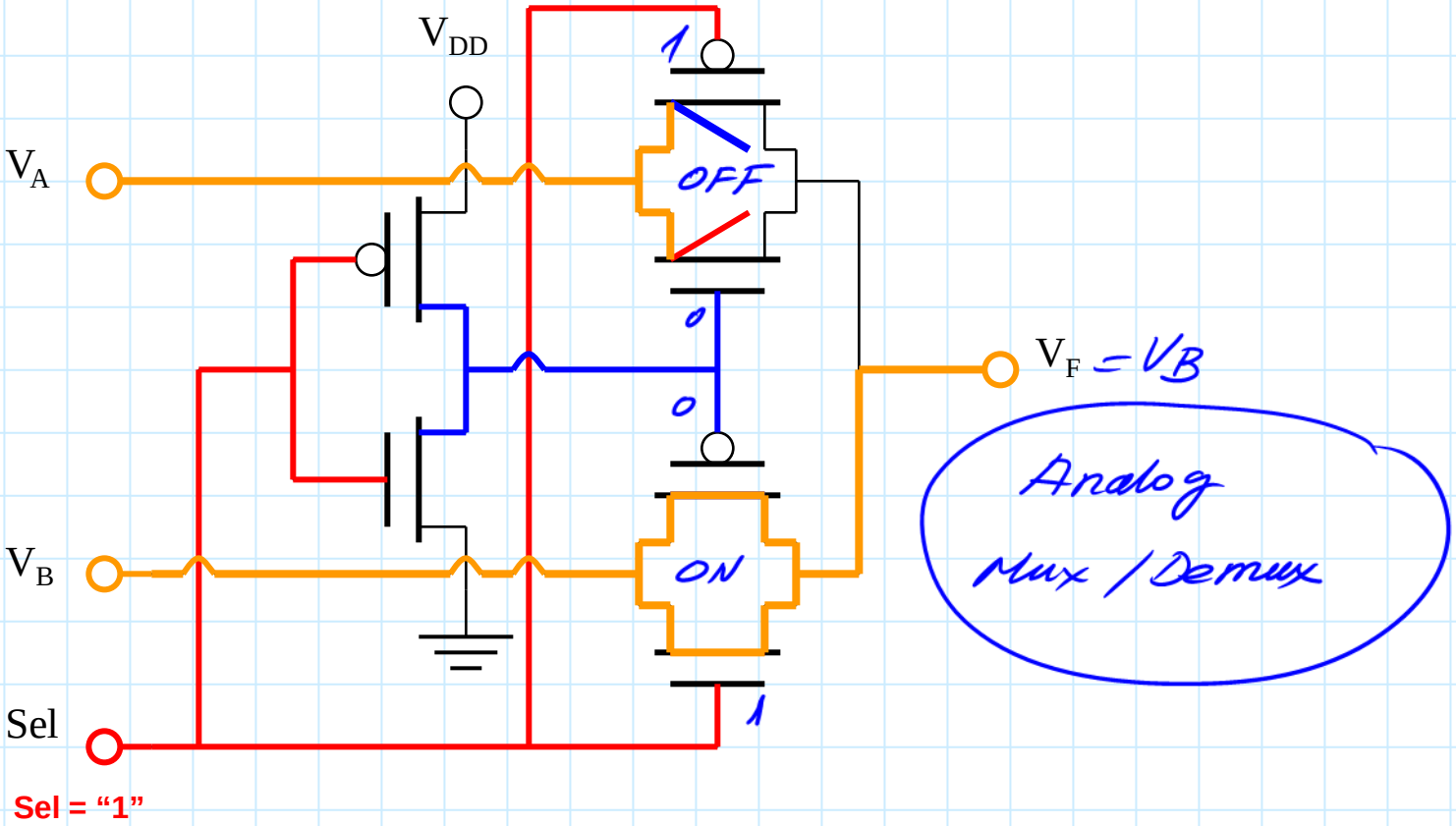
5.2.4 Transmission gates (6): Multiplexer

- Analog multiplexer
  - Inputs V_A, V_B, selection Sel, output V_F



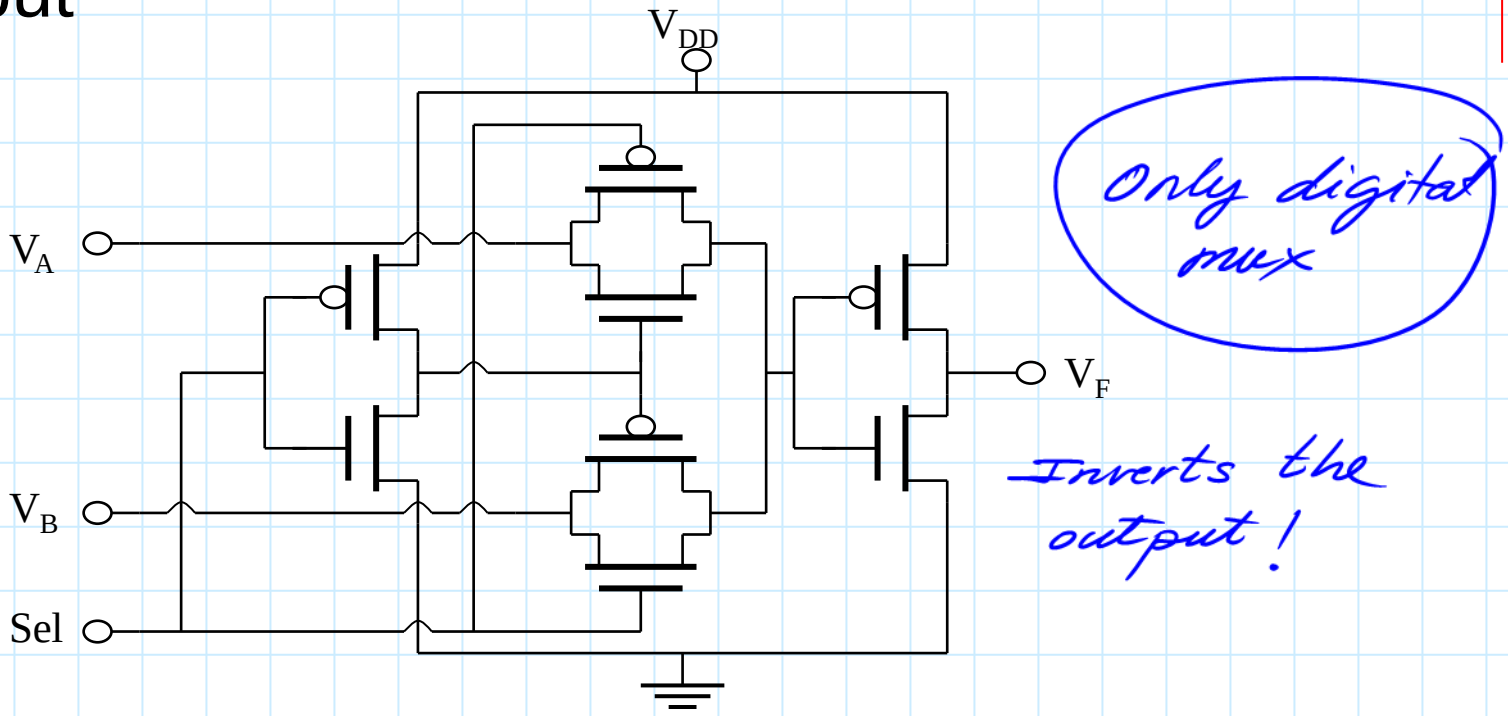
Sel = “0”

5.2.4 Transmission gates (7): Multiplexer



5.2.4 Transmission gates (8): Multiplexer

- Digital multiplexer: CMMOS inverter at the output

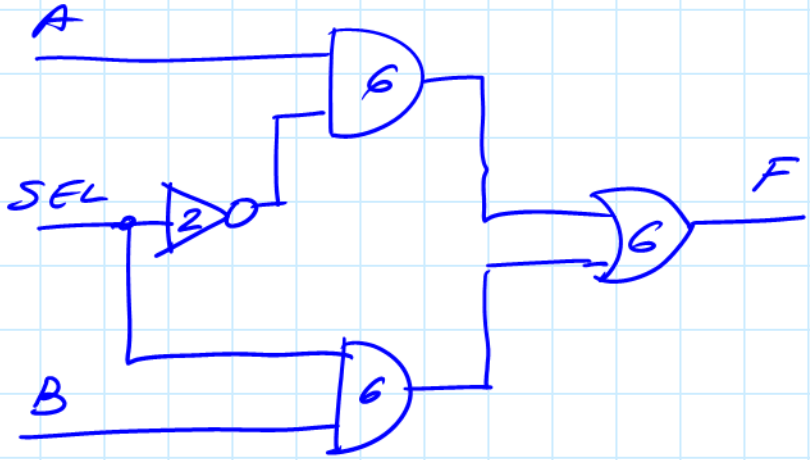


- 8 transistors → area and consumption saving, compared to a traditional design

5.2.4 Transmission gates (9): Multiplexer

- Design of the multiplexer with basic gates:
- How many transistors do we need? (exercise)

$$F = B \cdot Sel + A \cdot \overline{Sel}$$



Total: 20 transistors!