FUNDAMENTALS OF COMPUTER

Practice 1

Managing of the logical trainer

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Generalities

The logical trainer is a workbench that allows to study/analyze logical circuits without use exterior instrumentation. It contains basic logic-gates (AND, OR, NOT) and more complex circuits formed from these. The logic-gates are powered internally and only his inputs and outputs are accessible from the exterior. To realize the necessary interconnections and to construct the circuits we will use cables with *terminuses* in the ends; the above mentioned terminals fit in the *binding posts* arranged in the inputs and outputs of the logic-gates.

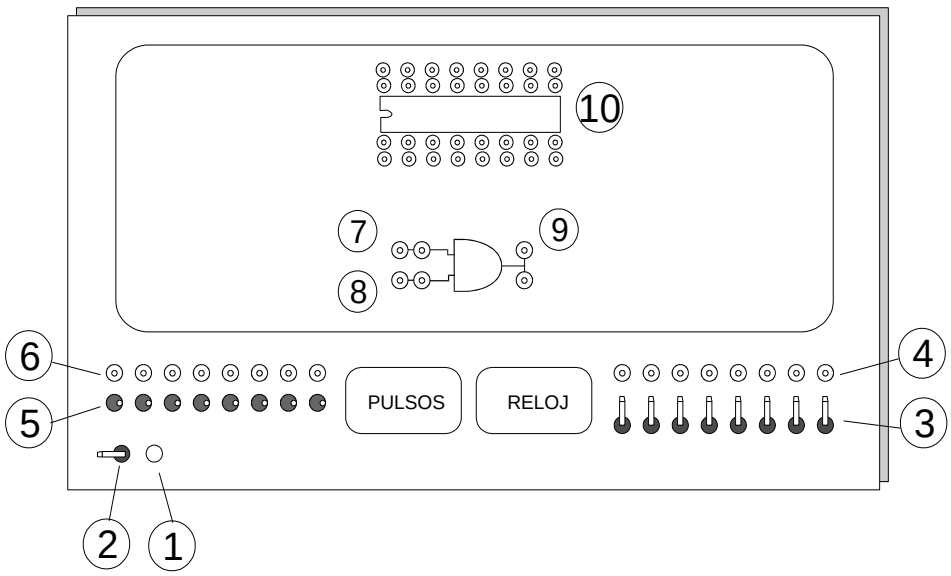


Figure 1. Basic diagram of the trainer.

Description of the logical trainer.

Figure 1 shows a basic outline of the trainer. Below are described the most important elements that compose it.

1. **LED**. If this LED is ON, the trainer is turned on**. <u>THAT IS VERY IMPORTANT as it assembles a logic circuit the trainer should not be turned-off (LED off).</u>**
2. **Switch:** To turn on/off the trainer.
3. **Programming Switchboards of logic levels:** Each one of these switchboards has associated a programmable terminal (4). Depending on the position of the lever of the switchboard, we can force in the associated point a high level (5 Volts) if the lever is towards the top part or a low level (0 Volts) if it is towards the low part of the trainer.
4. **Programmable Terminals:** From these terminals are made necessary input signals to the logic circuit.
5. **Output Indicators logic:** If the terminal associated with the indicator (6) reaches a high level (5 volts), the output indicator will be on and when it reaches a low level (0 Volt) will be

off.
6. **Input terminals of logic status indicators:** In these terminals usually are connected the output(s) of a logic circuit.
7 and 8. **Inputs A and B of the logic gate. Note that each entry door has two terminals arranged in horizontal. THIS IS THE SAME ELECTRIC POINT, IT IS SHOWN BY THE HORIZONTAL LINE.**
9. **Logic gate output. PLEASE NOTE that also each output has two output terminals arranged, in this case, vertically, and that there is a line that joins them.**
10. **Socket:** The trainer sockets are used to plug in integrated circuits. Through the associated terminals have access to the pins of the integrated circuit. TTL circuits must be powered with 5V, Vcc pin connecting to the socket pin +5 V and GND to 0V socket. **IN THE TRAINER, THESE TERMINALS ARE ON TOP AND ONE PAIR IS RED (+5 V) AND BLACK (GND).**

It should be noted that although each one of the inputs and outputs of logic-gates have two terminals they are internally connected. Having two connection points facilitates the assembly of complex.

Testing a logic circuit

A logic function can be represented i) by an algebraic expression, 2) a truth table or a 3) logic circuit. Usually, when dealing with the design of a new circuit, the design begins writing its truth table from a description. Once the truth table is made, the next step is to get the algebraic expression associated to it. And finally it is implemented a logic circuit using logic-gates.

How can you verify that the implemented logic circuit is associated with the original truth table?

The answer, “in a case of pen and paper”, is to be given to the inputs all possible combinations of values and, by analyzing the circuit, determine the value of the output(s) of the circuit. We thus obtain a truth table (from the circuit) to be compared with the truth table of departure (obtained from the description of the desired behavior of the circuit).

The work that it is necessary to do to verify that a logical circuit has a certain truth table associate indeed, using the logical trainer, is the same. The difference is that the analysis of the circuit is unnecessary, since the output indicators show us directly the value of the outputs. This work is made as follows:

1) Assemble the logic circuit using logic gates available in the trainer and the necessary cables. The circuit inputs have to be connected to , and the outputs have to be connected to the input terminals of the *status indicators*.
2) Set a specific VALUATION INPUTS in the circuit. The values that should take the inputs can be generated from the levers of programmable switches (switches on the bottom right of Figure 1).
3) Visualize and write down the value of the output(s) of the circuit. To see what values take the exits for each combination of input values must use the terminals associated with logic *output indicators* (indicators on the bottom left of Figure 1).
4) Repeat steps 2) and 3) to exhaust all possible input combinations.

The truth table is obtained programming all possible combinations of input values and observing the output or outputs of the circuit. If the truth table obtained coincides with the original circuit operation is correct, otherwise incorrect. NOTE: This last is not entirely true, as there are functions (those with indifferent input combinations) in which the circuit can return a result 0 or 1 (choice made by the designer of the circuit).

In Figure 2 we can see the connections that would be required if you want to check the operation of a circuit composed only of a two-input AND gate.

Repeat steps 2) and 3) to exhaust all possible input combinations.

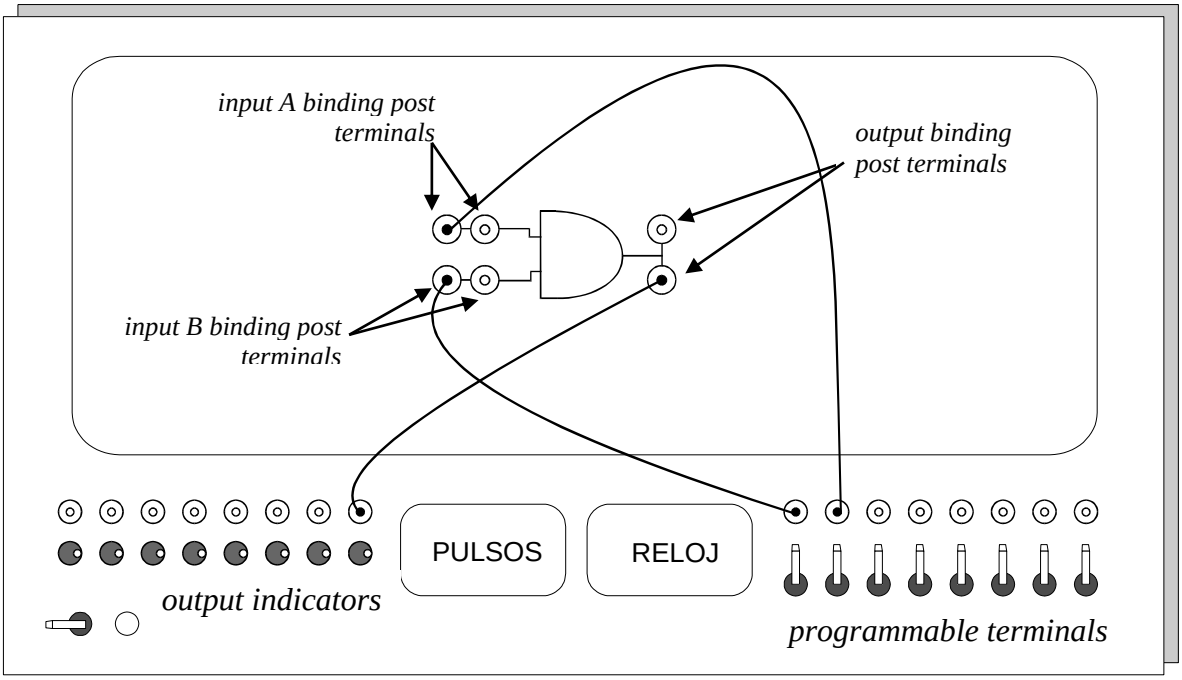


Figure 2. Necessary Connections to verify the operation of an AND gate.

Managing of the logical trainer

Question 1. Complete the truth table of a two-input NAND gate. Using the trainer verify it.

B	A	NAND (A,B)
0	0	1
0	1	1
1	0	1
1	1	0

Table 1. Truth-table of the NAND gate.

Question 2. Analyze the circuit shown in figure 3 and write it's truth table in Table 2.

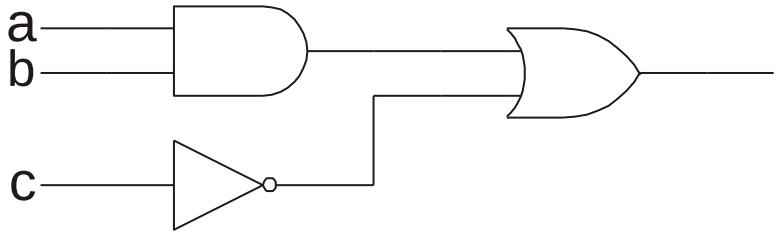


Figure 3. Circuit I.

c	*b*	*a*	*a AND b*	*NOT c*	*(a AND b) OR (NOT c)*
0	*0*	*0*	0	1	1
0	*0*	*1*	0	1	1
0	*1*	*0*	0	1	1
0	*1*	*1*	1	1	1
1	*0*	*0*	0	0	0
1	*0*	*1*	0	0	0
1	*1*	*0*	0	0	0
1	*1*	*1*	1	0	1

Table 2. Truth table of circuit I.

Question 3. Using the trainer implements the circuit shown in Figure 3 and verify the equivalence with the truth table written in Table 2.

The following circuits contain typical errors. Please answer for each case what is the error. **(NOTE: These circuit MUST NOT be mounted).**

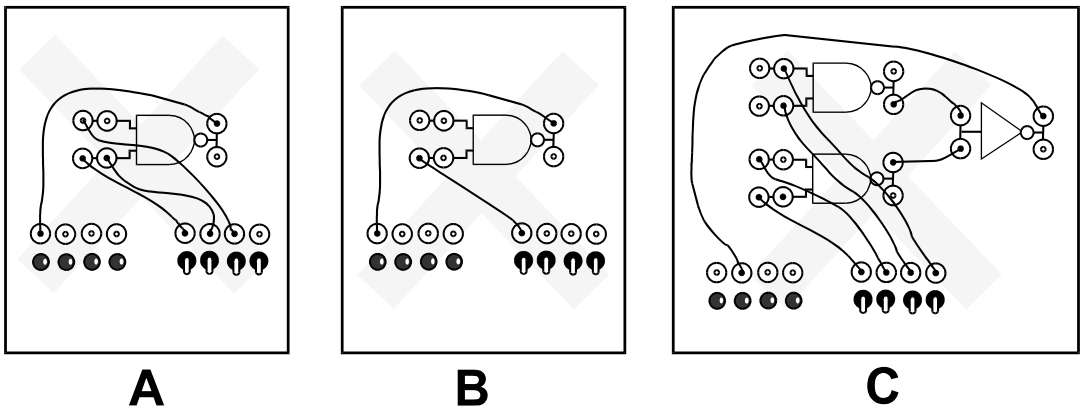


Figure 4. Erroneous circuits.

Question 4. Answer the following questions:

A Circuit Error:
We have connected 2 inputs to one of the AND gates' inputs. That's a shortcircuit. .....
.....
B Circuit Error:
We only have connected 1 input to the AND gate. The circuit doesn't run. .....
.....
C Circuit Error:
We have connected 2 outputs. That's a shortcircuit.....
.....

Use of integrated circuits

To use integrated circuits in the trainer, it is also necessary to place them in one of the sockets in the trainer, and to know what is the pin's distribution of inputs and outputs at the terminals of the circuit.
Remember also that all integrated circuits must be powered. To power a circuit with TTL technology, connect Vcc-pin socket to the +5 V socket (red binding post terminal) of the trainer. And the GND-pin to the 0V socket (black binding post terminal) of the trainer.
Figure 5 shows the pin layout of the 74LS02 integrated circuit as shown in the manufacturer's catalog.

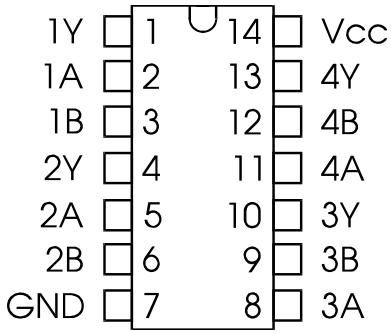


Figure 5. Pin layout of the 74LS02 IC.

The notch shown between pins 1 and 14 is present in the plastic packaging, and it is used to identify the orientation of the chip once mounted on the trainer. In some chips from other manufacturers that mark may be accompanied (or replaced) by a circular mark next to pin number 1.

Question 5. Answer the following questions:

- Indicate the pin number that corresponds to Vcc-pin: pin 14
- Indicate the voltage at which the Vcc-pin should be connected: 5V
- Indicate the pin number that corresponds to GND-pin: pin 7
- Indicate the voltage at which the GND-pin should be connected: 0V

The circuit 74LS02 contains four NOR gates (numbered 1 to 4), each with two inputs (A and B). The outputs are labeled with the letter Y. As an example, with the convention used, the pin labeled 2B refers to the B input of gate 2, and the output of the gate NOR is 2Y = 2A 2B.

Question 6. Answer the following questions:

- Indicate the pin numbers of the inputs of the gate 3: 3A and 3B
- Indicate the pin number of the output of the gate 3: 3Y
- Draw the gate number 3 indicating the pin number of inputs and the pin number of the output.

Question 7. Verify the operation of a 74LS02 integrated doors. To do this, complete theoretically the truth table in column A NOR B of Table 3. Then, using a 74LS02 integrated doors, make sure your output corresponds to the **NOR** gate function previously calculated.

B	A	A NOR B	Y
0	0	1	
0	1	0	
1	0	0	
1	1	0	

Table 3. Truth table of a NOR gate.

Question 8. Complete the truth table of circuit II.

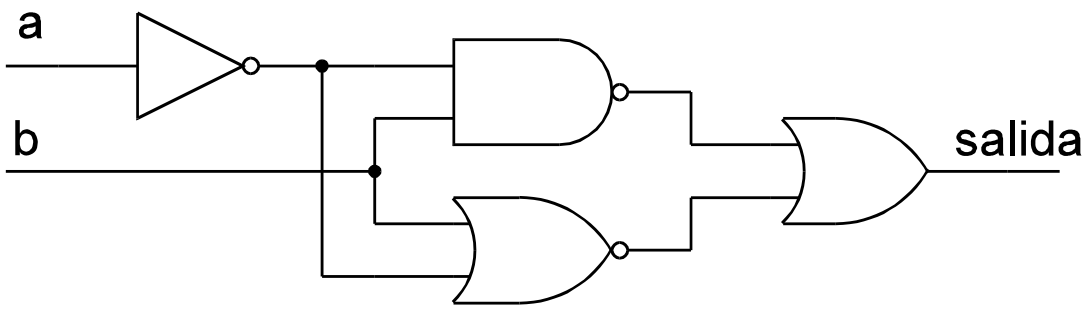


Figure 6. Circuit II.

b	a	NOT a	(NOT a) NAND b	(NOT a) NOR b	Output
0	0	1	1	0	1
0	1	0	1	1	1
1	0	1	0	0	0
1	1	0	1	0	1

Table 4. Truth table of the circuit II.

Plug-in the ICs 7402 and 7400 in the trainer. Connect the inputs VCC and GND of the two ICs. Implement the circuit shown in figure 6 using:

- One NOT-gate from the trainer
- One OR-gate from the trainer
- One NAND-gate from the IC 7400
- One NOR-gate from the IC 7402

Once the circuit is mounted write the value of the output for each one of the 4 valuations.

b	a	Salida
0	0	
0	1	
1	0	
1	1	

Tabla 5. Truth table for the circuit I.

Do truth tables 4 and 5 are equivalent?

Question 9. What is the level of the implemented circuit?_____

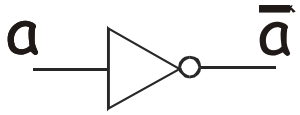
Optional: Boole's Algebra

This section will be analyzed through the use of Boole's algebra properties of the different gates and logic circuits. It is suggested as an exercise to obtain different logic gates using only 2-input NAND GATES.
For each one of the gates:

1. Perform the steps required to get an equivalent implementation.
2. Indicate in each step the properties and / or axioms of Boole's algebra that have been used.
3. Implement both circuits on the trainer, proving their equivalence.

Question 10. **NOT gate**. Implemented through the use of two-input NAND gates function $f = \overline{a}$, checking for proper operation.

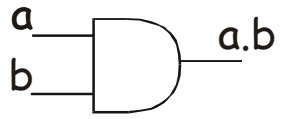
	Step	*Property*
$f = \overline{a}$	=	



NOT gate | Equivalent circuit

Question 11. **AND gate.** Implemented through the use of two-input NAND gates function $f = a.b$, checking for proper operation.

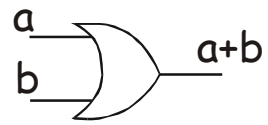
	Step	*Property*
$f = a.b$	=	



AND gate | Equivalent circuit

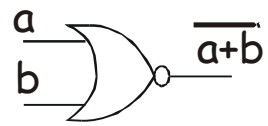
Question 12. OR GATE. Using 2-input NAND gates it must be obtained an equivalent circuit of the function: $f = a + b$. Verify that the obtained circuit works properly.

	Step	*Property*
$f = a + b$	=	

	
Puerta OR	Equivalent circuit

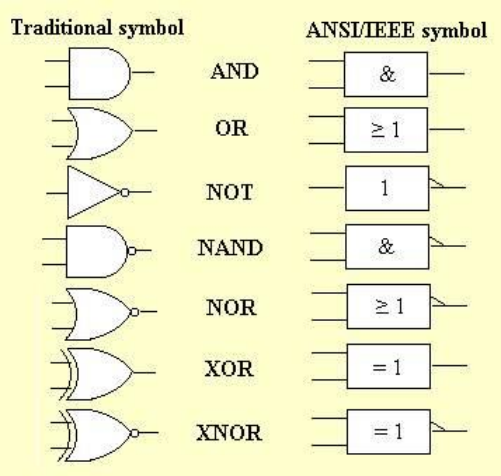
Question 13. **NOR GATE**. Using 2-input NAND gates it must be obtained an equivalent circuit of the function $f = \overline{a + b}$. Verify that the obtained circuit works properly.

	Step	*Property*
$f = \overline{a + b}$	=	

	
NOR gate	Equivalent circuit

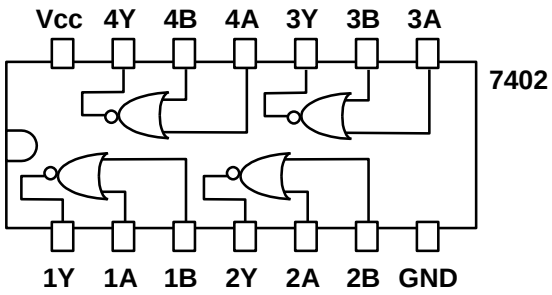
Annexe A

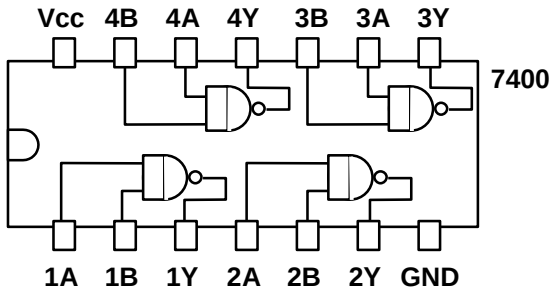
The graphic symbols used in class to represent logic gates are called "classical" or traditional nomenclature. There are other ways to represent logic gates, among which stands out for its importance is the standard format standard, which is used by the trainer course. The following figure shows the correspondence between the traditional nomenclature and ANSI / IEEE standard symbols for basic logic gates:



Note that in this trainer, the inverter gate INV has been called instead of NOT.

Annexe B





Description: each one of the gates contained in an integrated circuit has a number assigned. The inputs of every gate are called A and B. The output is called Y.

IMPORTANT: The VCC-pin must be connected to 5 volts (1 in the trainer). The GND-pin is the pin of mass, and must be connected to 0 volts (0 in the trainer). Any mistake in the hookup of these pins (included his not connection) can cause the destruction of the integrated circuit.