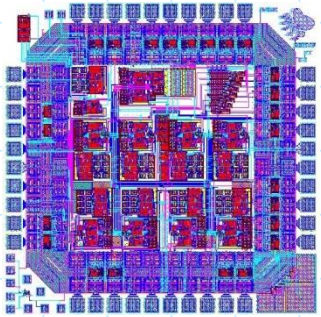
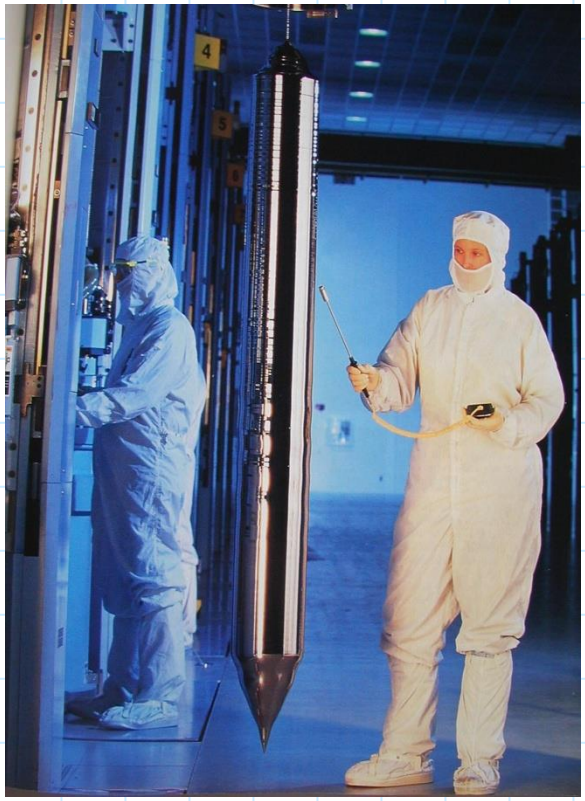
4.7 VLSI design foundations

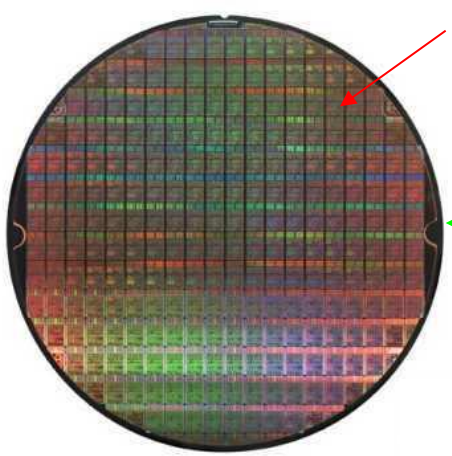
- Manufacturing Process:
  - CMOS transistors are manufactured in thin silicon wafers
  - Photo-lithographic process:
    - Sequence of photographic and chemical steps
    - At each step, different materials are deposited or printed
  - In each step, different materials are settled or engraved



4.7.1 Manufacturing Process

- Chip manufacturing in wafers:



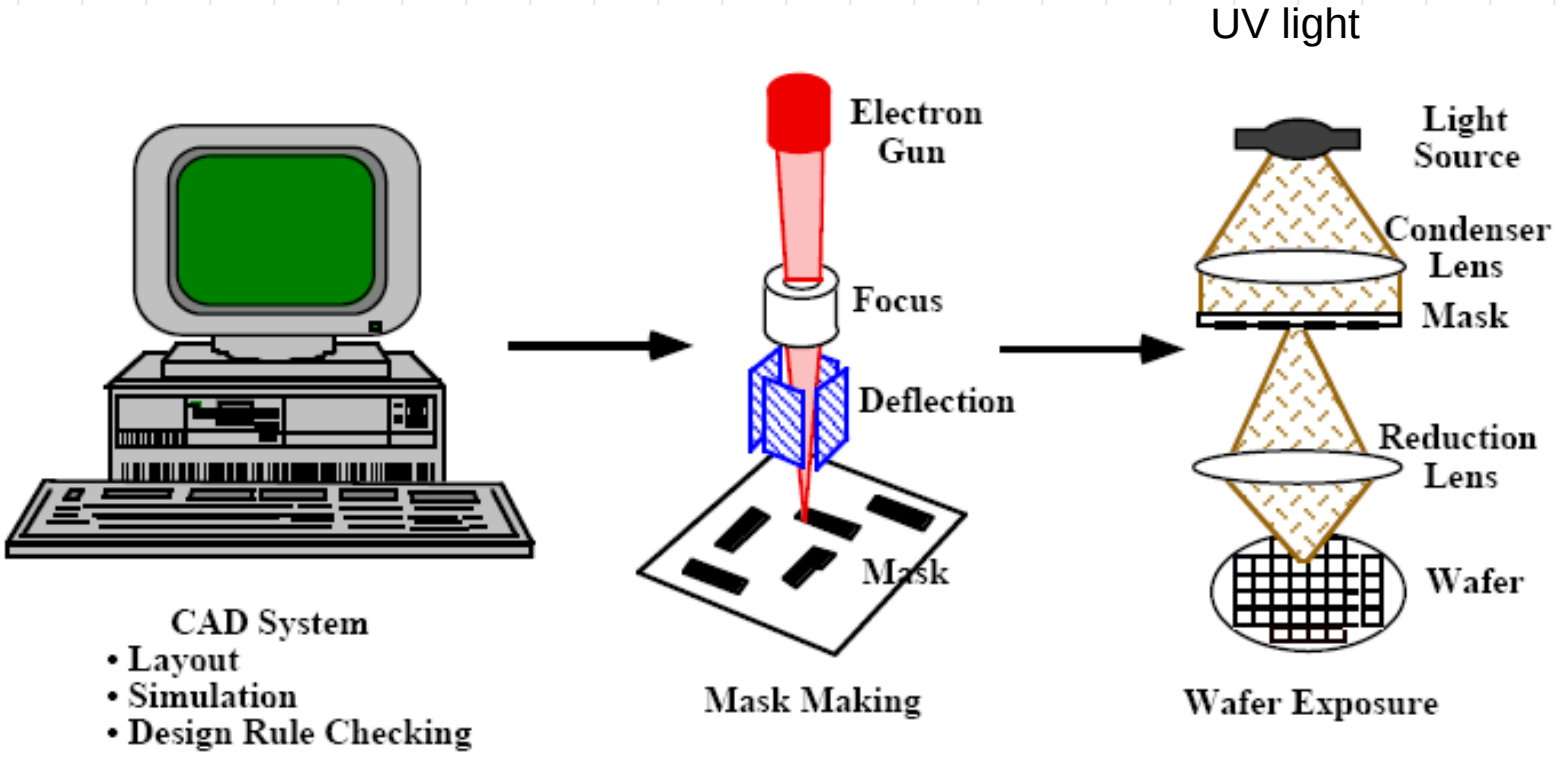


Diameter: 75-300 mm

Thickness: ~1mm

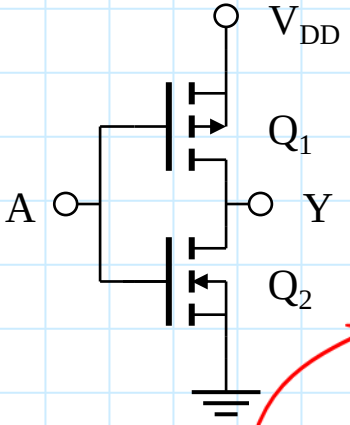
4.7.1 Manufacturing Process

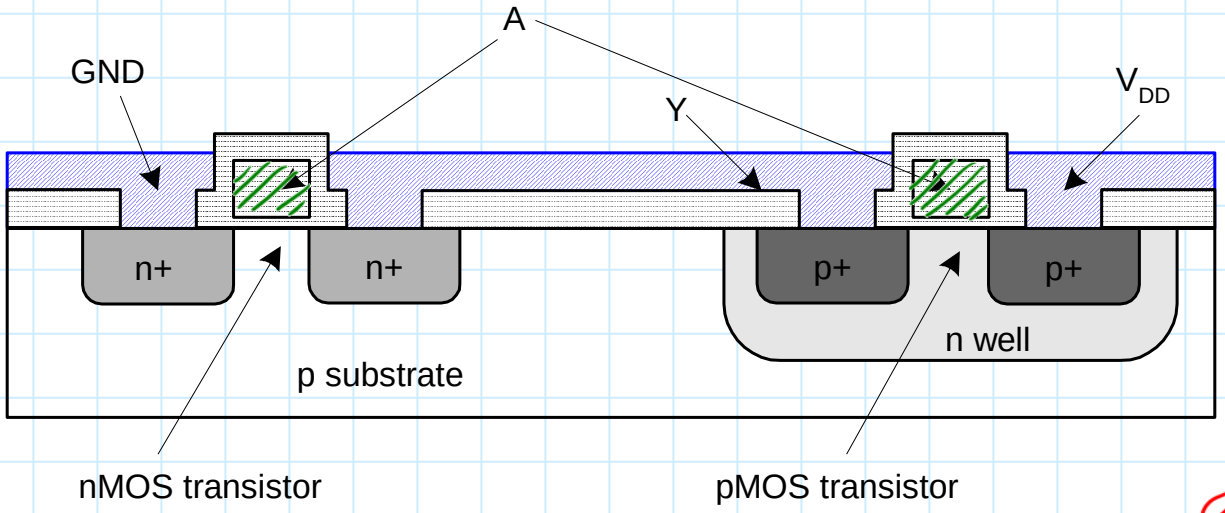
- CAD design→ masks→photolithography



4.7.2 Cells layout: layers

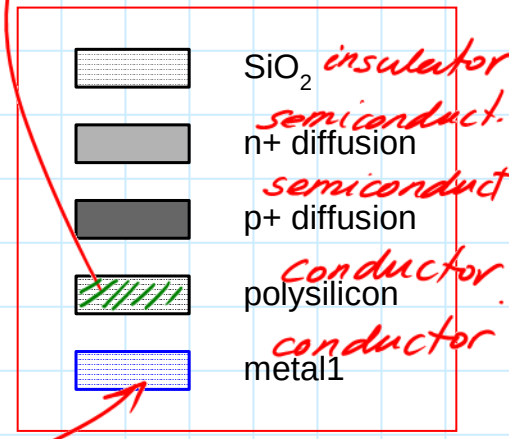
- CMOS inverter on the wafer. Layers of materials (1):
  - Cross section of the inverter
  - P-substrate typically used for nMOS transistors
  - Requires n-well as a substrate of pMOS transistors





highly doped Si

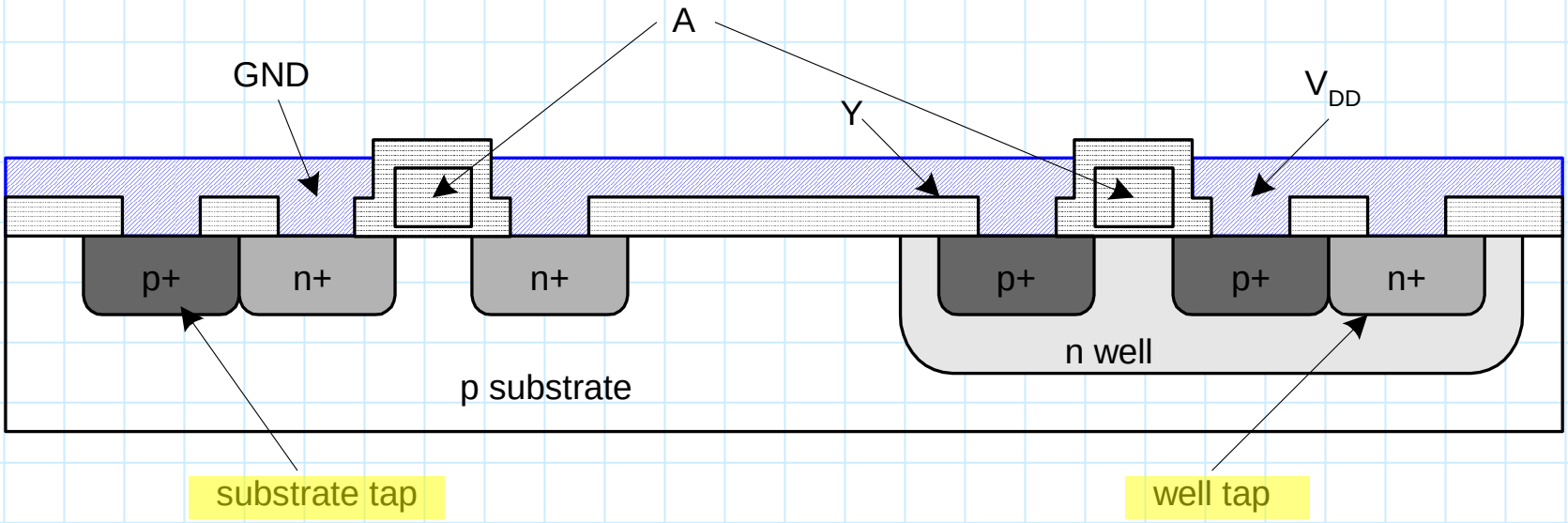
Layers



al, Cu

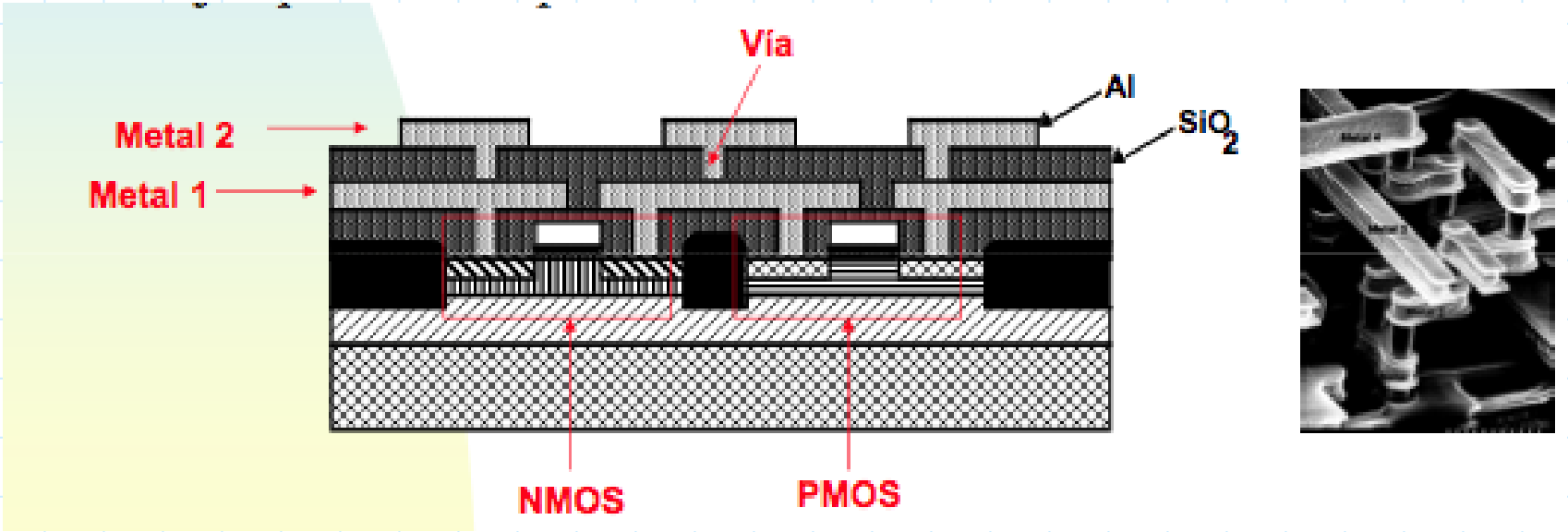
4.7.2 Cells layout: layers

- CMOS inverter on the wafer. Layers of materials (2):
  - Well and substrate contacts
    - The substrate must be connected to GND and the n-well to VDD
    - Contacts (taps) are made with heavily doped Si in substrate and the n-well



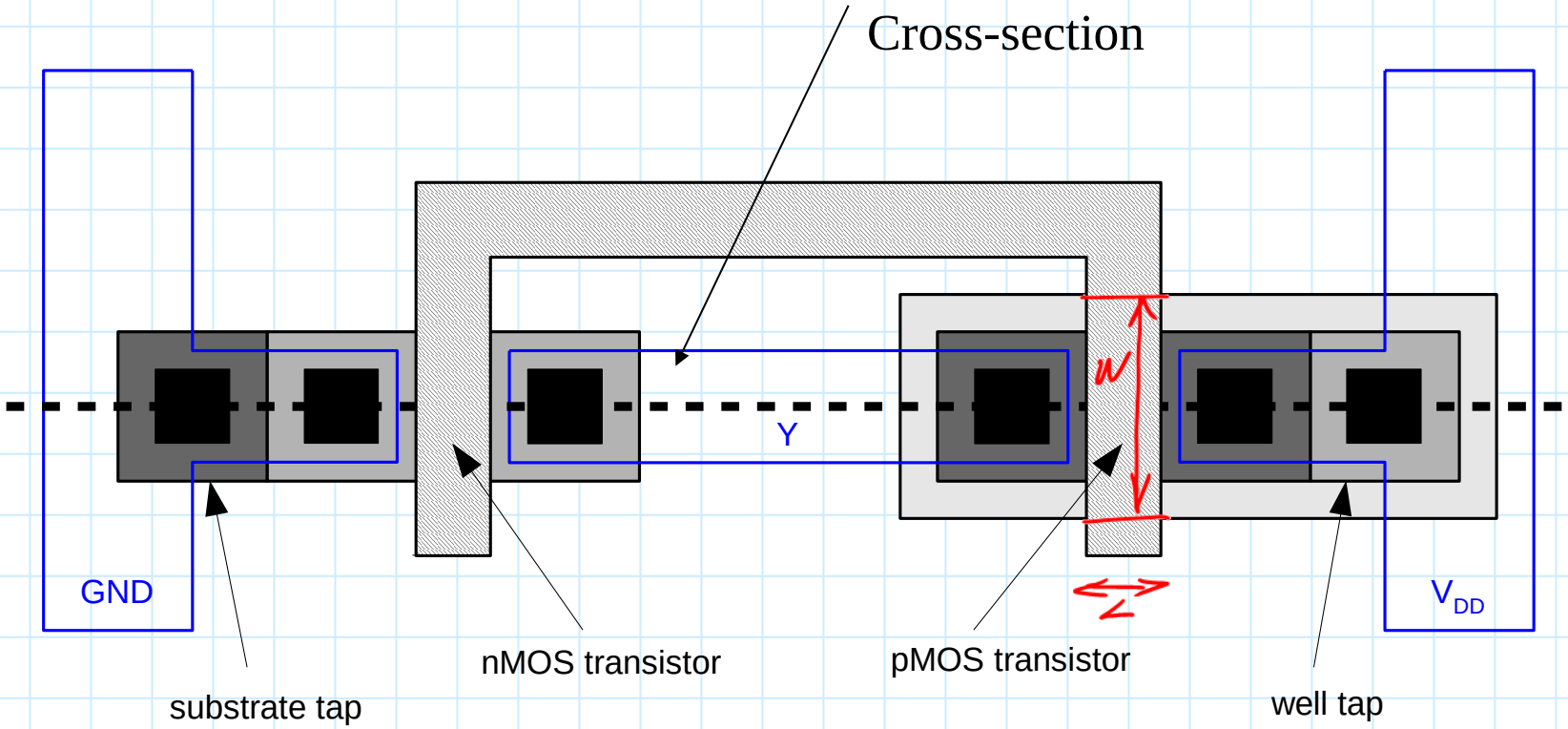
4.7.2 Cells layout: layers

- Normally, there are several metal layers:
  - Interconnections
  - V_{DD}, GND
  - Clock
- Example with 2 metal layers

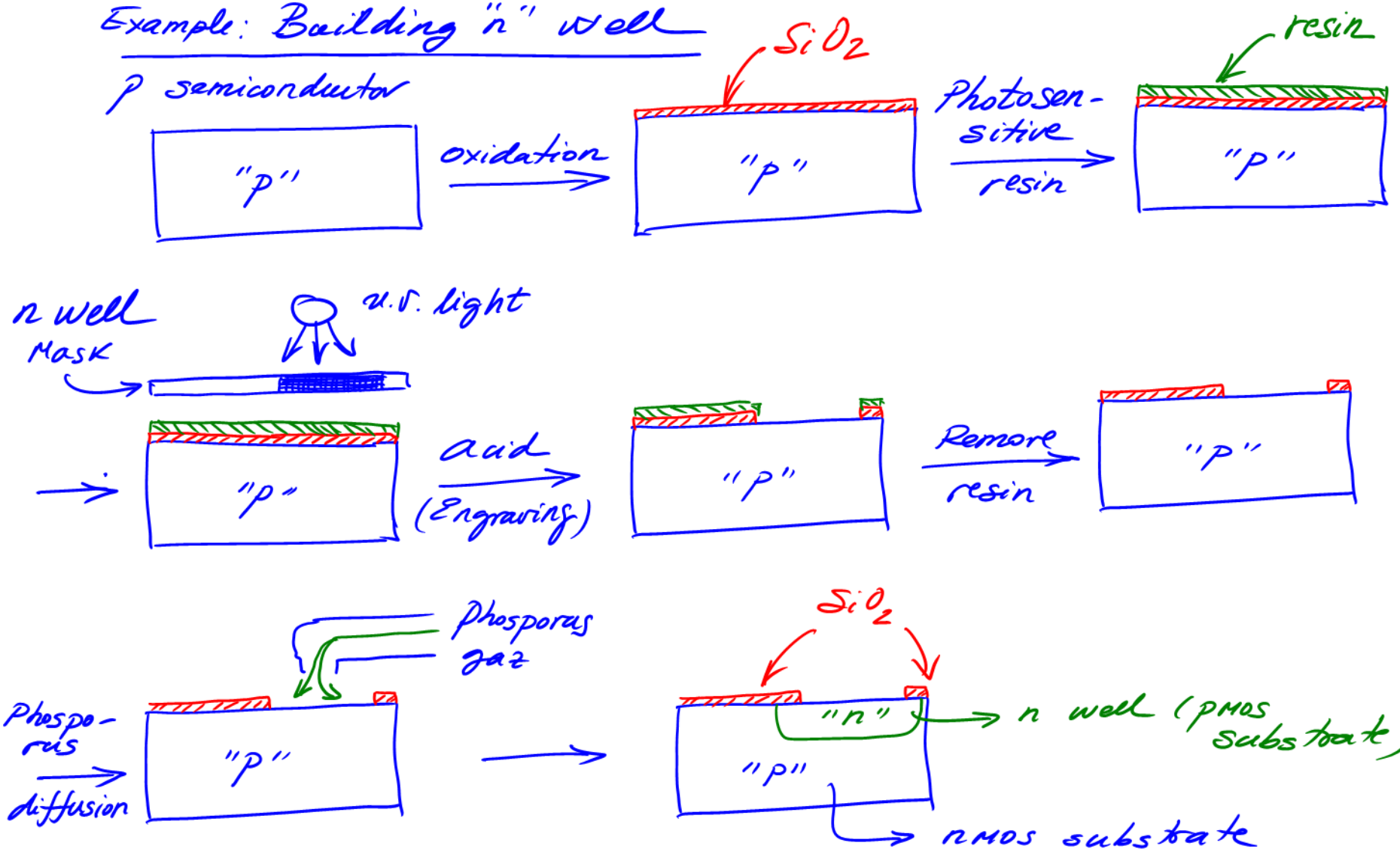


4.7.2 Cells layout: masks

- CMOS inverter. Masks
  - Transistors and connections are defined by masks
  - Top view:

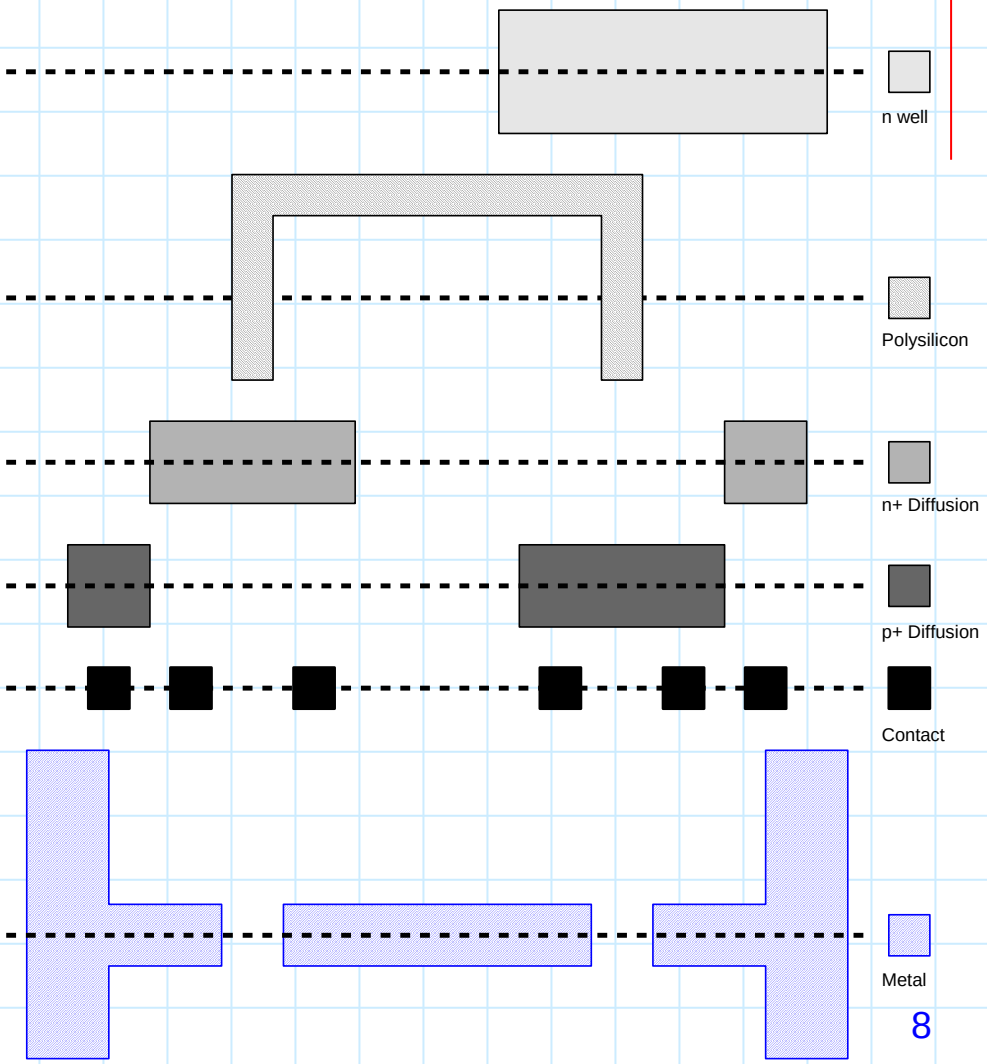


Example: Building "n" well



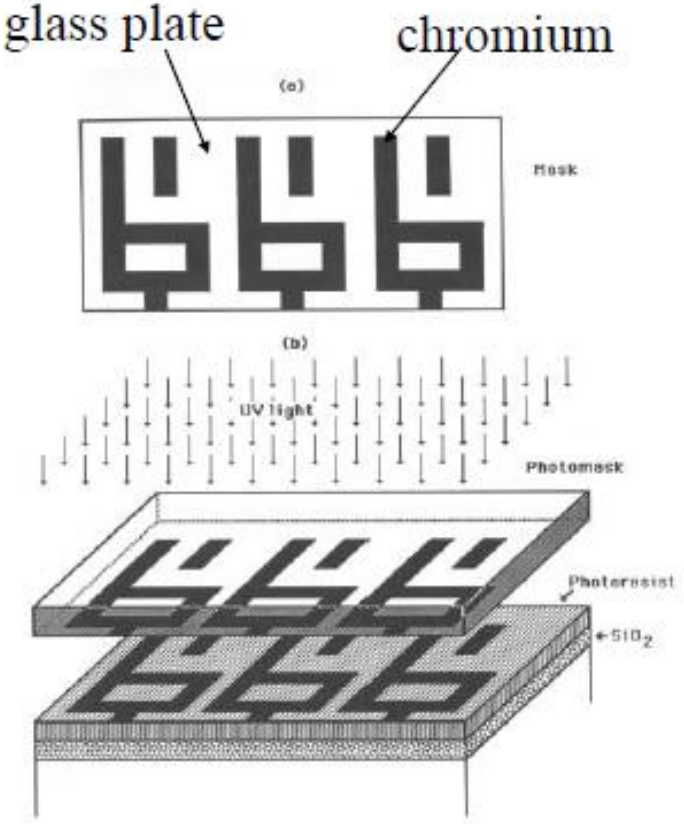
4.7.2 Cells layout: masks

- Example: 6 masks
- n-well
- Polysilicon
- n+ diffusion
- p+ diffusion
- Contact
- Metal



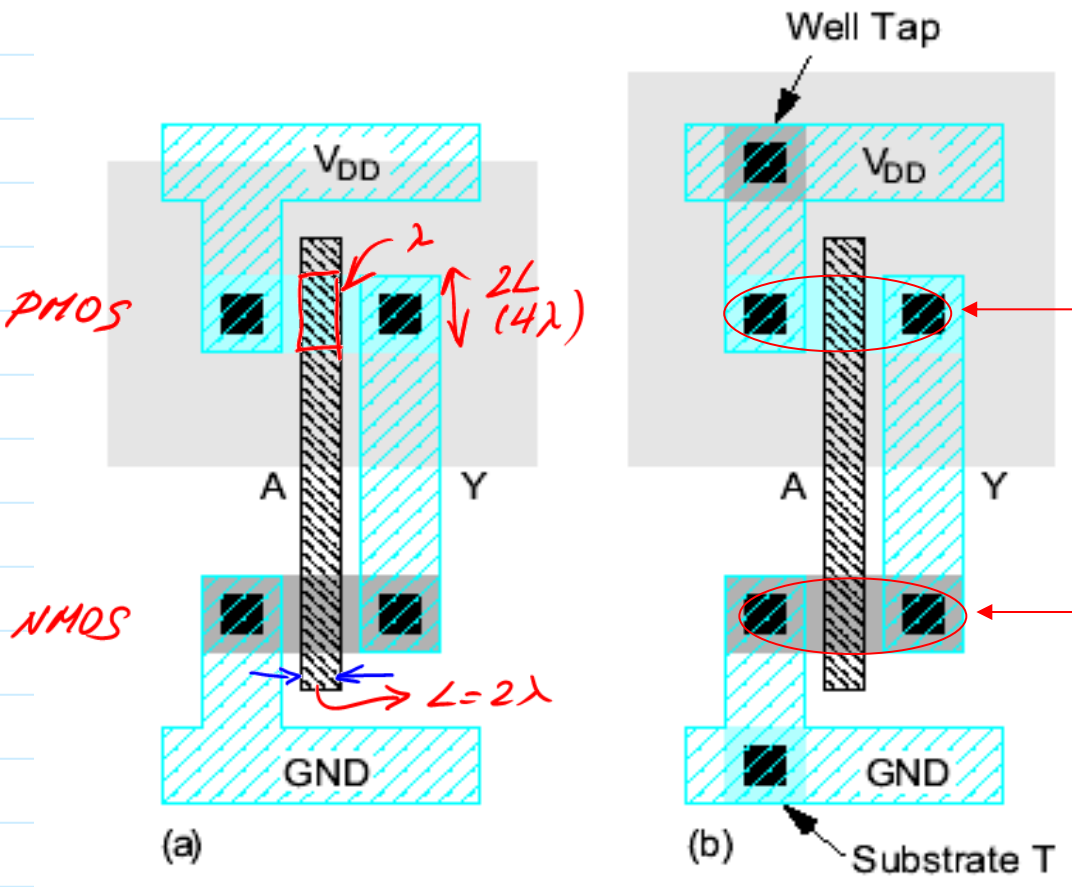
4.7.2 Photolitography

- Masks are projected over the wafer
- The parts on shadow are eliminated (Engrave)
- In the eliminated parts materials are settled (Place)



4.7.2 Cells layout: Inverter layout

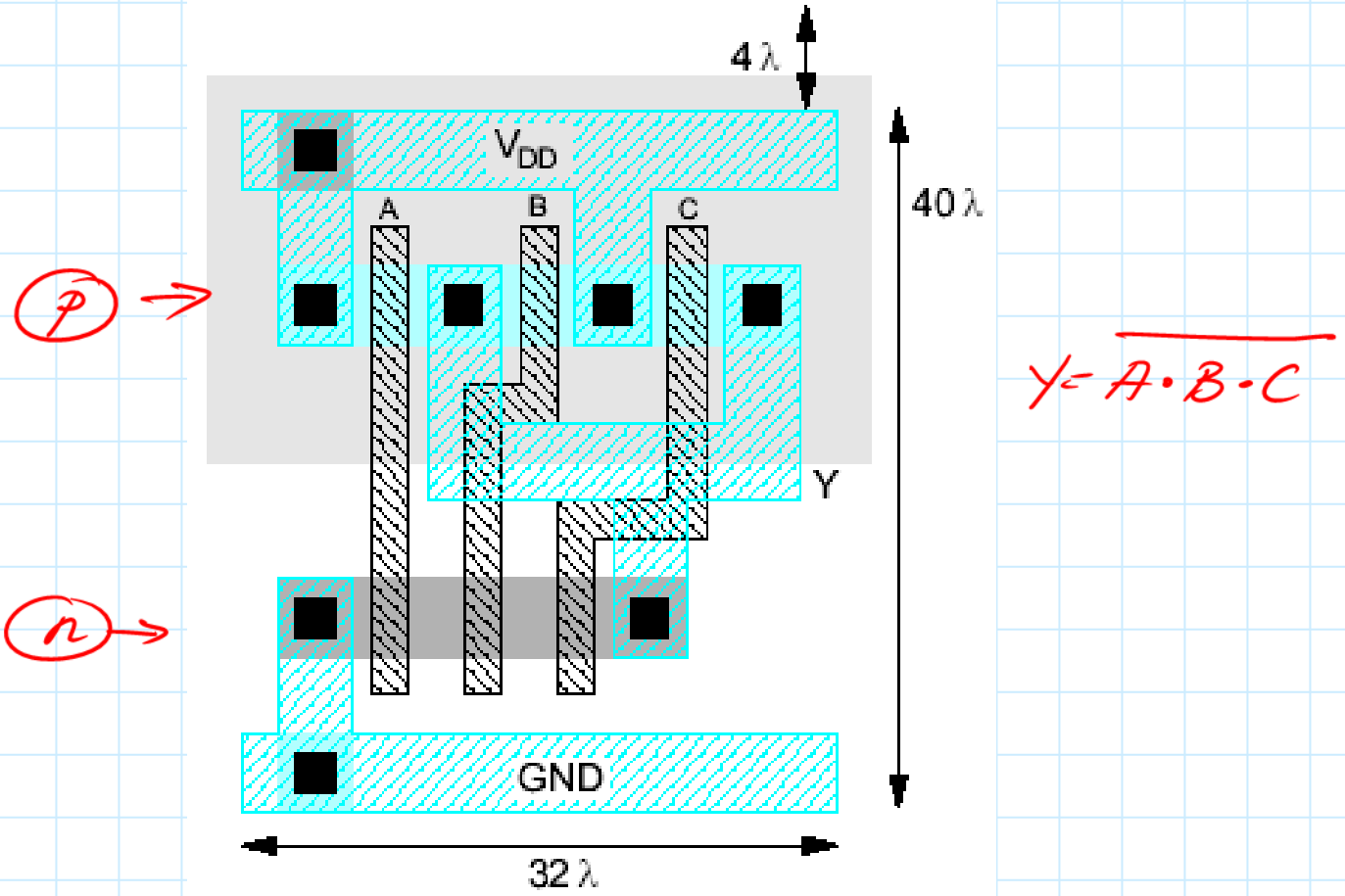
Sizes
$\lambda = \frac{L}{2}$
$L \rightarrow$ feature size



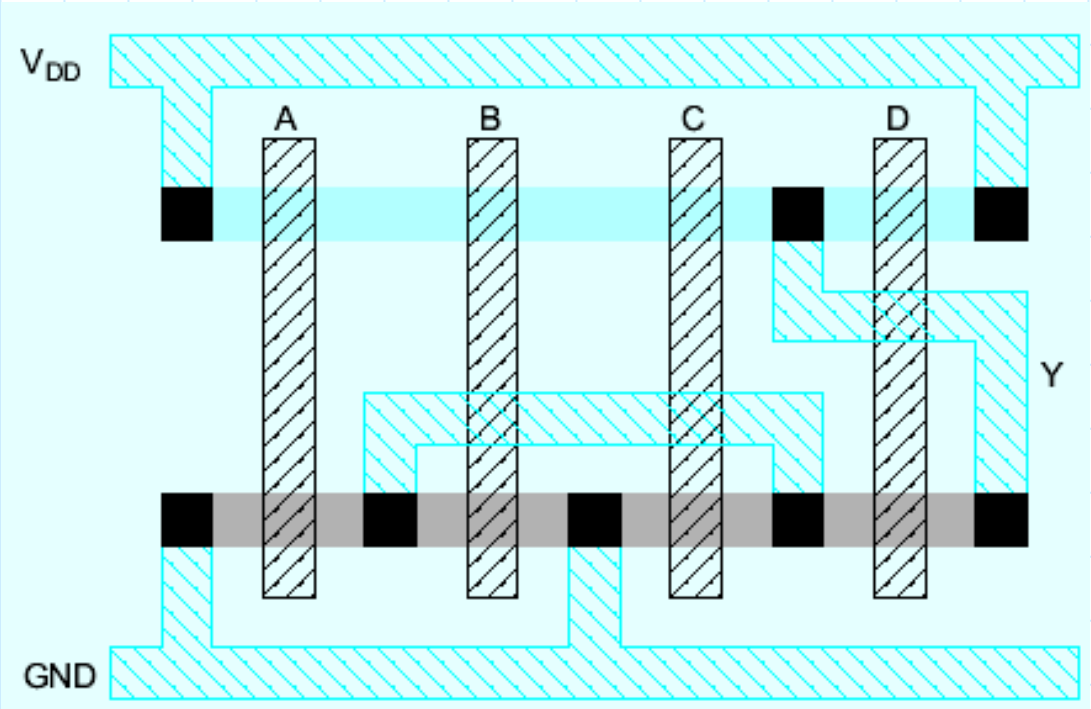
PMOS Transistor:
Poly-P^+diffusion cross

NMOS Transistor :
Poly-N^+diffusion cross

4.7.2 Cells layout: 3 input NAND

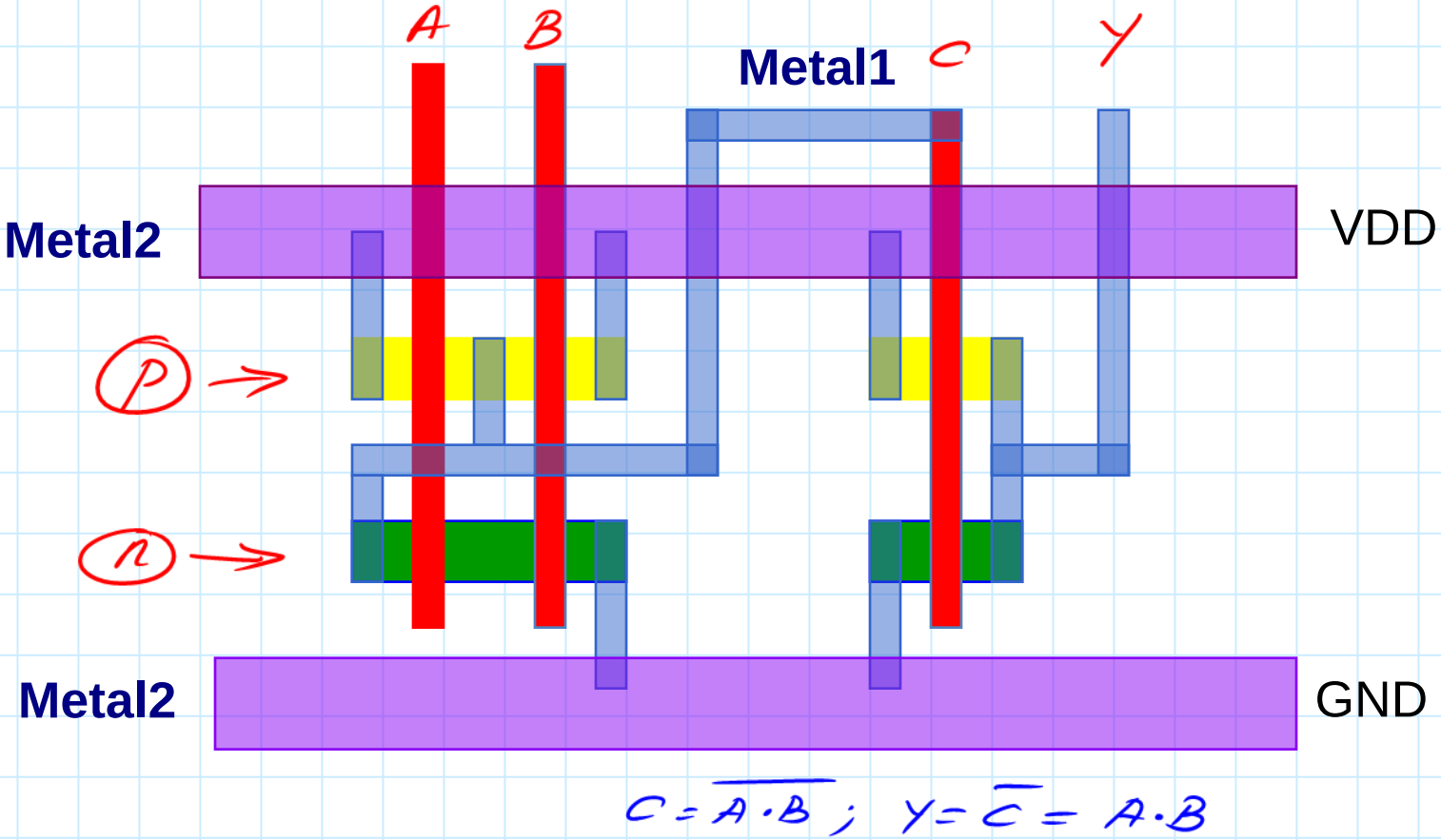


4.7.2 Cells layout



$$Y = \overline{(A + B + C).D}$$

5.7.2 Cells layout: Exercise



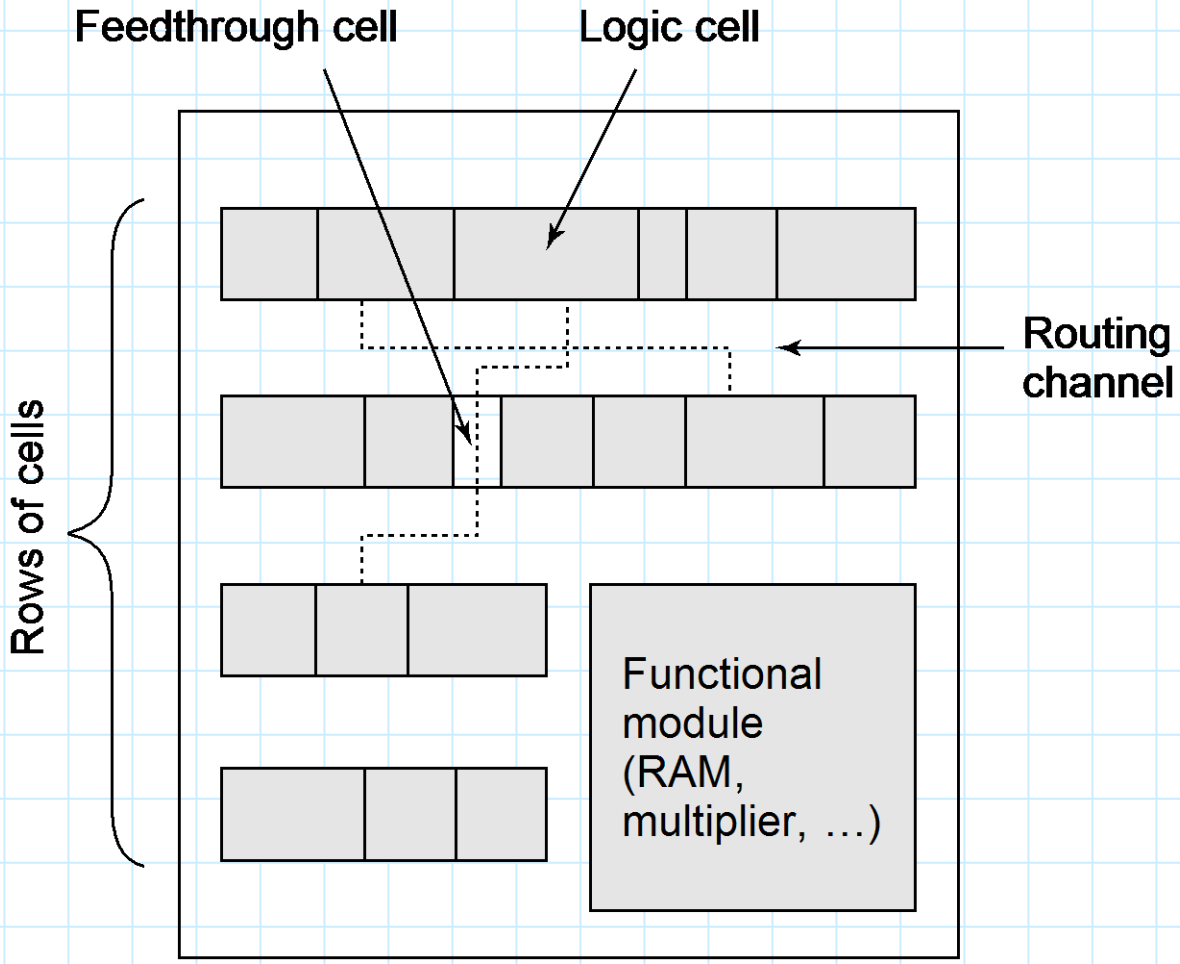
- Which function implements this layout?

4.7.3 Design flow with standard cells

- Layouts of simple circuits
  - Logic gates, FF, full-adder, multiplexers, cell input / output,
- Cells stored in cell libraries
- Different sizes and output currents
- Predesigned and verified (area, delay, power consumption)
- Deposited on the chip to form more complex designs
  - Computer Aided Design (CAD): place and route
  - Reusability
  - Modularity
- Automatic design of macro-cells (macro-modules) memory modules, multipliers, ...

4.7.3 Design flow with estándar cells

- Provision of standard cells on the chip:

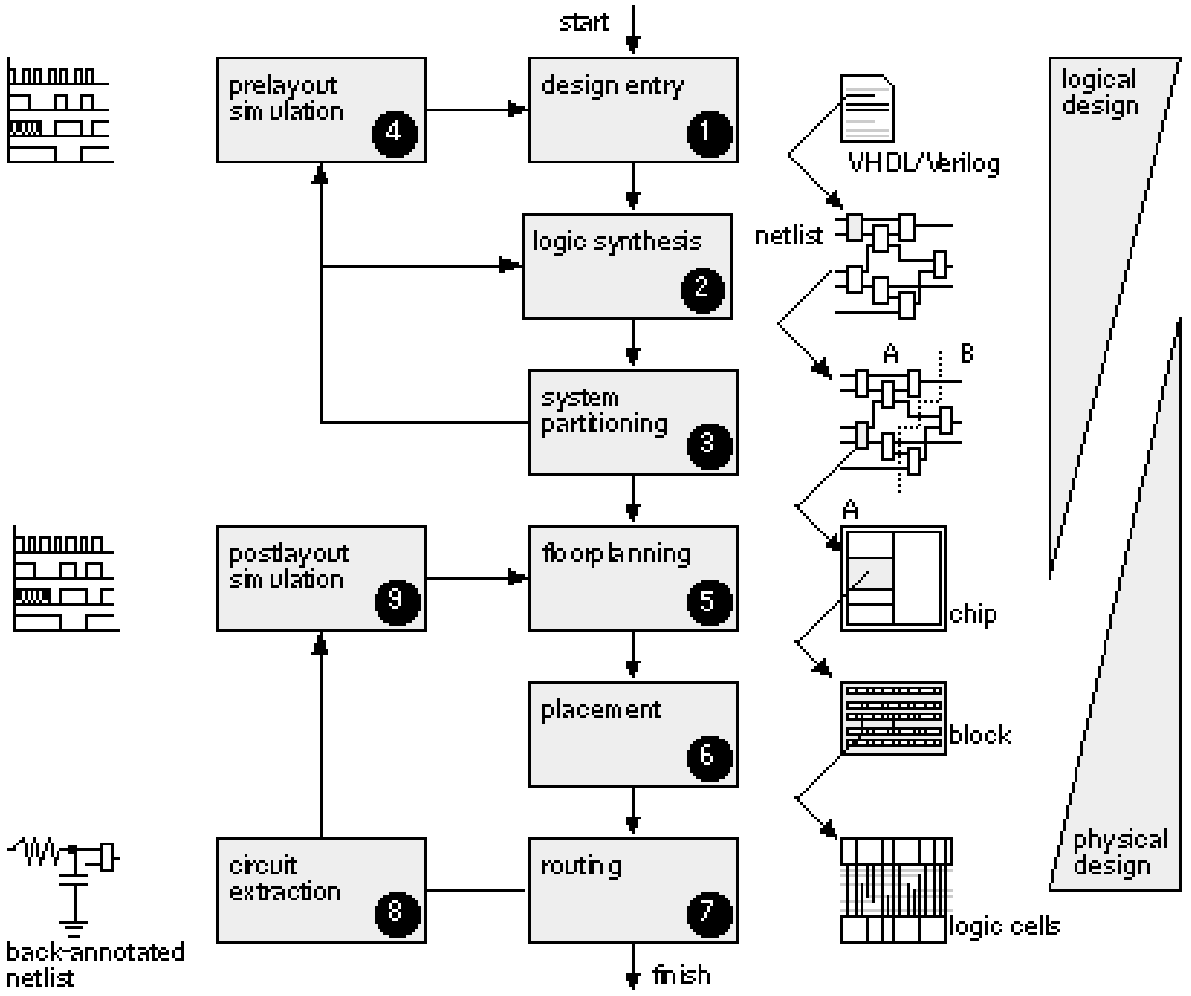


Cells arranged in rows, with the same height and variable width
V_{DD} and GND shared

The interconnecting channels are reduced by increasing the presence of more metallization layers

4.7.3 Design flow with estándar cells

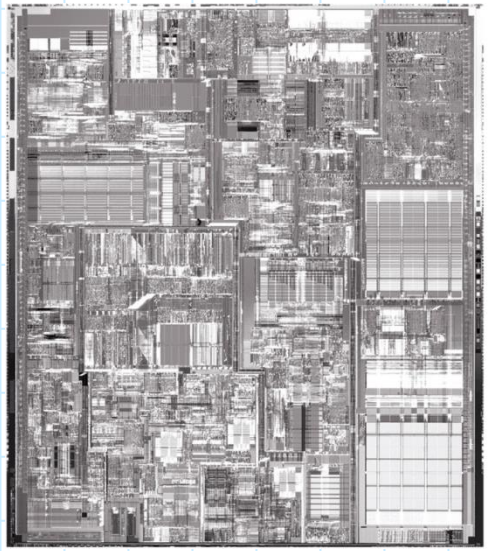
- Design flow based on standard cells



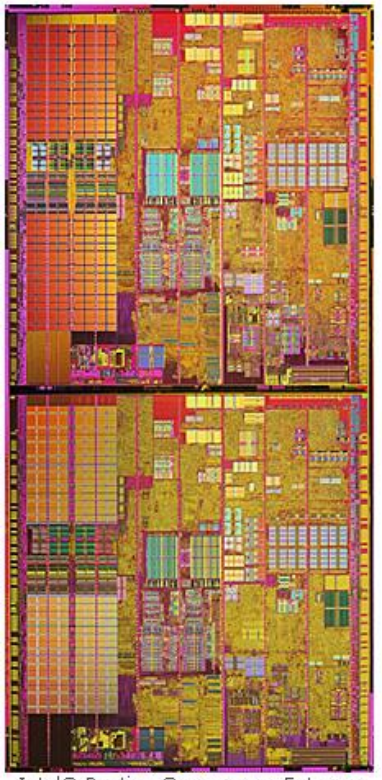
4.7.3 Design flow with estándar cells

- Steps in the flowchart
  - 0. System specification using a natural or formal language
  - 1. Initial description of the design. Behavioral description using HDL languages -Hardware Description Languages-(Verilog, VHDL).
  - 2. Logic synthesis. It automatically generates the netlist-description of the standard cells needed and the connections between them.
  - 3. System partition. Divides a large system into blocks.
  - 4. Pre-layout simulation. Verification of correct operation. Approximate temporal verification based on the cells delays.
  - 5 .Floor planning. Organize (place) blocks in the chip netlist.
  - 6. Placement. Deciding the location of cells within a block.
  - 7.Routing. Make connections between cells and block
  - 8.Extraction. Determine the resistance and capacitance of interconnecti ons.
  - 9. Post-layout simulation. Verification of timing requirements with the R and C values of the actual interconnections.

4.7.3 Design flow with estándar cells: examples



Pentium 4



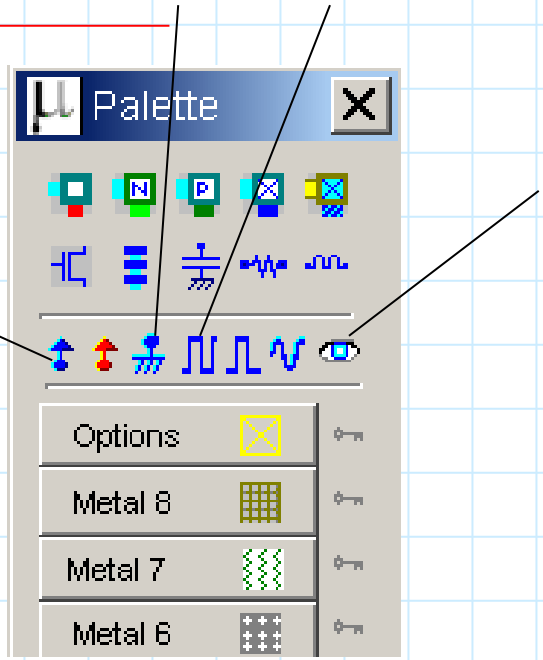
Intel® Pentium® processor Extreme Edition processor die

Dual-Core Processors

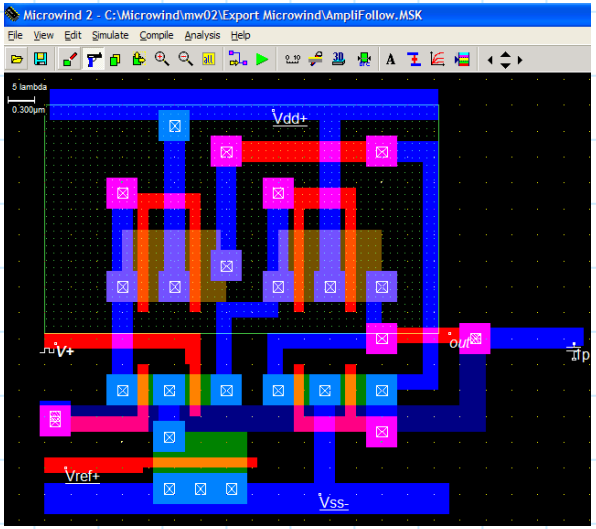
4.7.4 Full-custom design

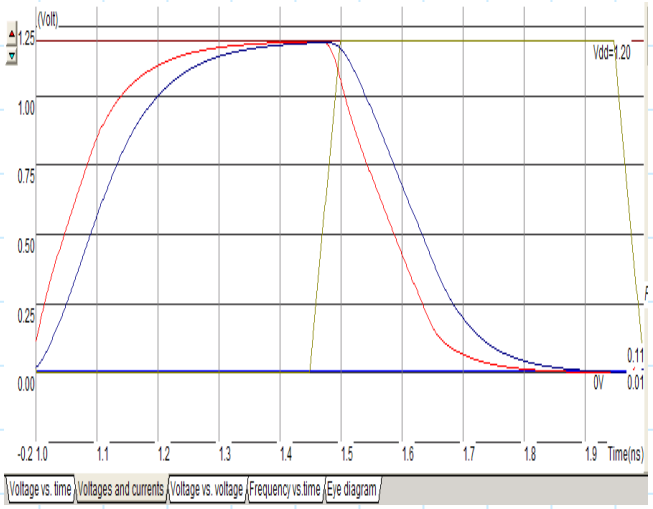
- Some cells or parts of the design require optimal features of the area, consumption or speed
  - Clock circuits (PLL, drivers, ...)
  - High-speed arithmetic circuits (floating point, ...)
  - Input / Output Drivers
  - ...
- For these cases, a full-custom design is used
  - Mask-level design (geometric)
  - More optimal design than based on Standard Cells (semi-custom)
  - For critical parts of small size
  - CAD Tools:
    - Graphical layout editor
    - Primitives: transistors, contacts, wires, ports
    - Automatic verification

4.7.4 Full-custom design



Layout editor

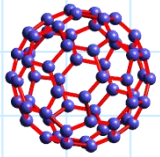


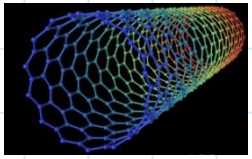


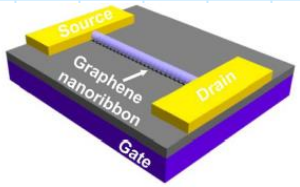
Post-Layout Simulation

4.7.5 VLSI design: current and future trends

- Historical evolution:
  - 4004: 10 μm technology
  - ....
  - Pentium 4: 0.13 μm technology, 90nm (submicron)
  - Dual-core, 4-cores, 8 cores, ... (thousands of millions of transistors)
- Current technologies: 90nm, 65nm, 45nm, 32nm, 22 n
- Current trends: technological and design **improvements in CMOS**
  - (www.intel.com /technology, ITRS 09)
  - New materials
  - New designs
- Future Trends: Research in **Nanotechnology** (ITRS 09)
  - Nanotubes, nanowires, graphene, spintronics, SET, molecular, quantum







4.7.4 VLSI design: New trends of today and future

Year	2009	2012	2015	2018	2021
Feature size (nm)	34	24	17	12	8.4
L_{gate} (nm)	20	14	10	7	5
V_{DD} (V)	1.0	0.9	0.8	0.7	0.65
Billions of transistors/die	1.5	3.1	6.2	12.4	24.7
Wiring levels	12	12	13	14	15
Maximum power (W)	198	198	198	198	198
DRAM capacity (Gb)	2	4	8	16	32
Flash capacity (Gb)	16	32	64	128	256

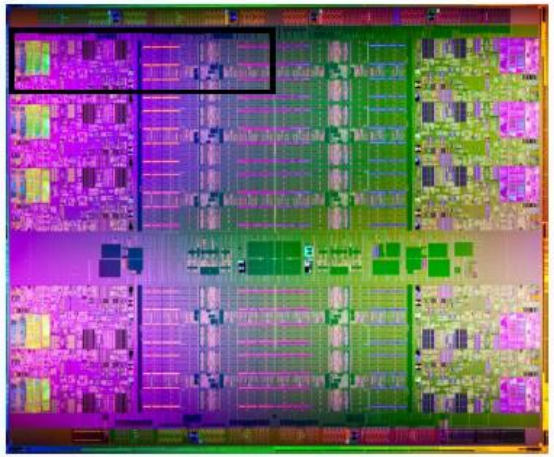
4.7.4 VLSI design: New trends of today and future

- *Multicore era*
  - Simpler Core microprocessors
  - Less voltage and frequency
  - More performance as there are more cores/chip

e.g. Intel 10 Core Xeon Westmere-EX

- 1.73-2.66 GHz (vs. previous Xeons at 4 Ghz)

1 core →



Summary

- In the first part of the unit we have introduced the structure and operation of CMOS basic gates (NOT, NAND, NOR, ...) .
- After that, we have addressed the design of generic combinational circuits using the complementary CMOS logic methodology.
- Then, the transmission gates have been introduced, studying their use in several logic circuits, such as multiplexers and flip-flops.
- We have also addressed the special CMOS outputs (open drain and tri-state), which allow for bus connections.
- We have also described the main characteristic parameters of the CMOS family and subfamilies, discussing the high-speed and low voltage CMOS subfamilies.
- Subsequently, we have seen a summary of the fundamentals of VLSI design and manufacturing.
- Finally, we have commented on the current and future trends in the design and manufacture of VLSI chips.