

Computer Architecture and Engineering Syllabus

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Course Goals

- Understanding the concept of computer architecture. Identifying suitable design and configuration decisions and tradeoffs to improve the performance of computer architectures.
- Enumerating the different aspects impacting the design of computer instruction sets.
- Analyzing the mission of vector computer instruction sets. Understanding the behavior and use of vector instructions in current computers.

Course Goals (cont.)

- Reviewing the concept of pipelining. Studying the benefits and challenges of pipelining computer instruction units. Understanding the techniques required to address these challenges.
- Understanding how pipelining techniques are applied to computer instruction units. Analyzing techniques and tradeoffs to improve performance through static and dynamic instruction scheduling. Understanding the concept of superscalar processors.
- Understanding the techniques and tradeoffs typically considered during the design of high-performance memory subsystems.

Lectures

UT 1 Introduction to computer architecture.

- 1 Concept of computer architecture
- 2 Performance analysis
- 3 Instruction set architecture design

UT 2 Pipelining

- 1 Pipelining instruction units
- 2 Multicycle units and static instruction scheduling
- 3 Branch prediction
- 4 Dynamic instruction scheduling and speculation
- 5 Multiple instruction Issue

UT 3 Memory subsystem

- 1 Memory subsystem performance evaluation
- 2 Cache performance improvement
- 3 Main memory performance improvement

Labs

- 1 Performance analysis.
- 2 Design of an instruction pipeline unit:
 - 1 Part I.
 - 2 Part II.
- 3 Static instruction scheduling.
- 4 Dynamic instruction scheduling:
 - 1 Part I.
 - 2 Part II.

Grading criteria

Lectures will be evaluated through two partial exams, while only one exam will be proposed for lab evaluation. All exams can be made up and the best grade, among each exam and its corresponding make-up exam, will be retained for grading.

Lectures (80%)

- (10%) 4 tests will be proposed through poliformaT in order to check your progression through the course. Test will contain both theory and exercises. Test results will impact the weight of partial exams.
- (70% – 80%) 2 partial exams, each one with a minimum individual weight of 35% on the final grade.
 - The aforementioned weight can be increased up to 40% attending to the test results.

Grading criteria (cont.)

- First partial is a midterm term exam, while second partial is scheduled for the end of the semester.
- Every partial can be individually made up at the end of the term. No minimum grade is required for retaking any of the partial exams. The best result obtained between each partial and its corresponding make-up exam will be the one finally retained for grading.

Grading criteria (cont.)

Labs (20%)

- 1 lab exam, which can be retaken in case of need. No minimum grade is required .
- Lab attendance is mandatory (minimum attendance required of 80%) in order to be able to sit the lab exam.
- If a student has successfully passed the AIC labs in the past (grade of 5 or greater), then she/he can ask for a lab grade of 5 this year.

Make-up exams The best grade between each partial and its corresponding make-up exam will be retained for grading.

Grading criteria (cont.)

Students with class exemption (dispensa académica) They will be evaluated through the aforementioned theory and lab exams. The attendance requirement will not be applied to them.

Scheduling

Calendar 2019-20

		Theory				
		Monday	Tuesday	Wednesday	Thursday	Friday
2 Sep	6 Sep		1	1	1	1
9 Sep	13 Sep	1	2	2	2	2
16 Sep	20 Sep	2	3	3	3	3
23 Sep	27 Sep	3	4	4	4	4
30 Sep	4 Oct	4	5	5	5	5
7 Oct	11 Oct	5	6 (Wednesday)		6	6
14 Oct	18 Oct	6	6	7	7	7
21 Oct	25 Oct	7	7	8	8	Partial 1
28 Oct	1 Nov					
4 Nov	8 Nov	8	8	9	9	8
11 Nov	15 Nov	9	9	10	10	9
18 Nov	22 Nov	10	10	11	11	10
25 Nov	29 Nov	11	11	12	12	11
2 Dec	6 Dec	12	12	13	12 (Friday)	
9 Dec	13 Dec	13	13	14	13	13
16 Dec	20 Dec	14	14	14 (Friday)	14	
23 Dec	27 Dec					
30 Dec	3 Jan					
6 Jan	10 Jan					
13 Jan	17 Jan	Partial 2				
20 Jan	24 Jan					Recov. T+P

Labs	
Week	Session
1	
2	
3	
4	
5	1
6	2a
7	2b
8	2b
9	3
10	Tut. Prác
11	4
12	5
13	5
14	Tut.

	Holidays
	Period of exams
	Theory partial
	Lab exam
	Recovery exam

Bibliography



John L. Hennessy and David A. Patterson.
Computer Architecture, Fifth Edition: A Quantitative Approach.
Morgan Kaufmann Publishers Inc., San Francisco, CA, USA, 5
edition, 2012.



John L. Hennessy and David A. Patterson.
Computer Architecture, Fourth Edition: A Quantitative Approach.
Morgan Kaufmann Publishers Inc., San Francisco, CA, USA, 4
edition, 2006.



M. Beltrán and A. Guzmán.
Diseño y evaluación de arquitectura de computadoras.
Pearson Educación, 2010.

Bibliography (cont.)



J.L. Baer.

Microprocessor Architecture: From Simple Pipelines to Chip Multiprocessors.

Cambridge University Press, 2009.



J. Ortega, M. Anguita, and A. Prieto.

Arquitectura de computadores.

Thomson, 2005.



J.P. Shen.

Modern Processor Design: Fundamentals of Superscalar Processors.

McGraw-Hill Series in Electrical and Computer Engineering.
McGraw-Hill, 2004.

Bibliography (cont.)

 **David A. Patterson and John L. Hennessy.**

Computer Organization and Design, Fourth Edition: The Hardware/Software Interface (The Morgan Kaufmann Series in Computer Architecture and Design).

Morgan Kaufmann Publishers Inc., San Francisco, CA, USA, 4th edition, 2008.