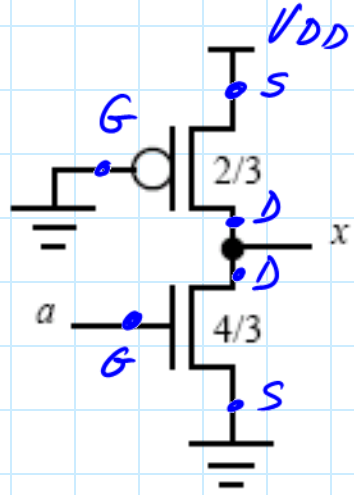
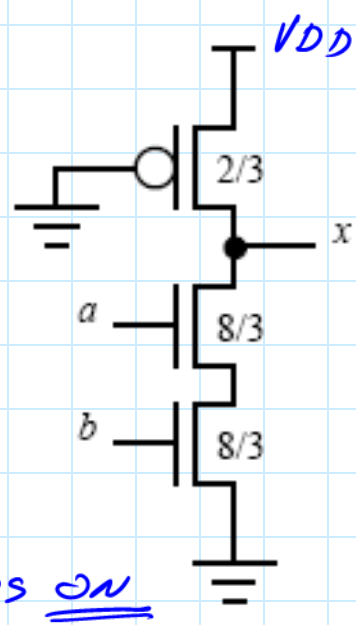
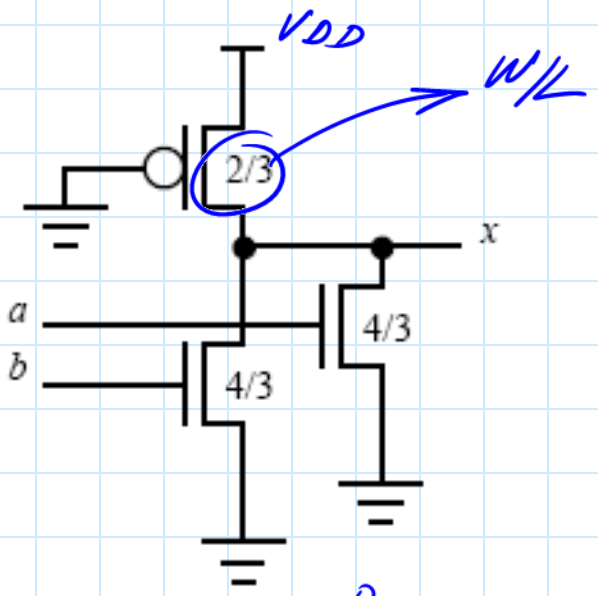
Active loads. Pseudo-NMOS Logic







$V_G = 0$; $V_S = V_{DD}$

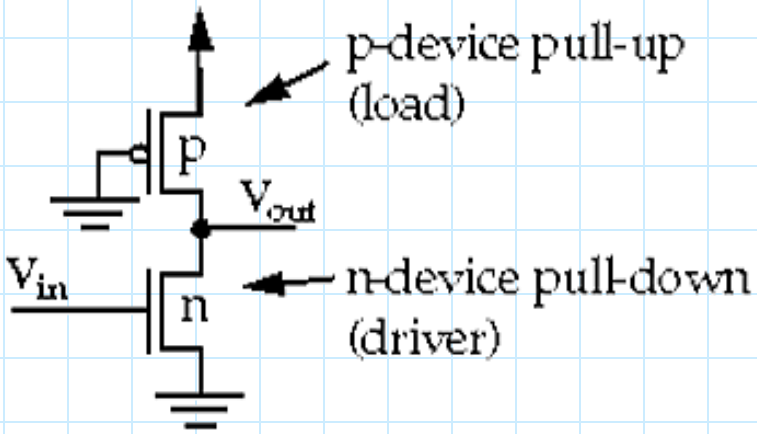
$V_{GS} = -V_{DD} < -V_T \Rightarrow$ PMOS ON

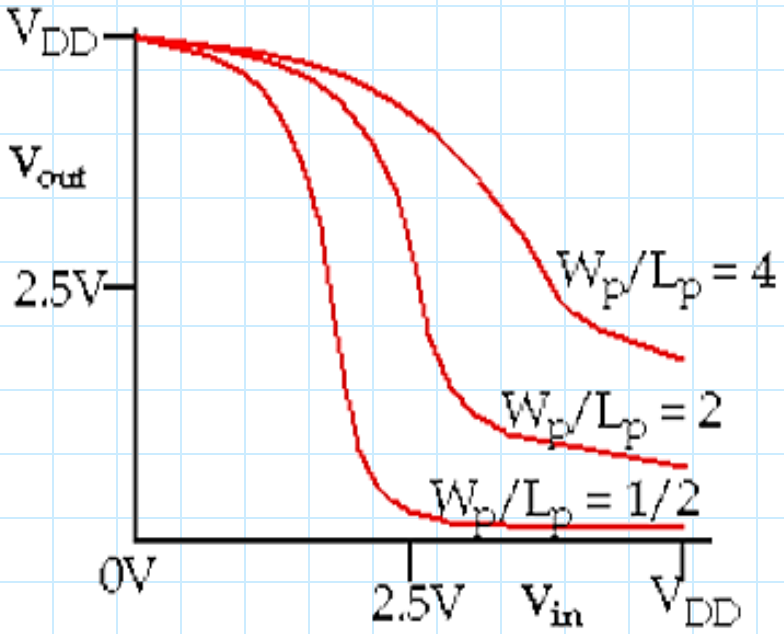
Inverter NAND NOR

PMOS smaller but it is allways conducting $\Rightarrow$ No switching

- PMOS trasistor always conducting
- Saving Silicon area (no Rpull-up necessary)
- Used in ROM, PLA and FLASH

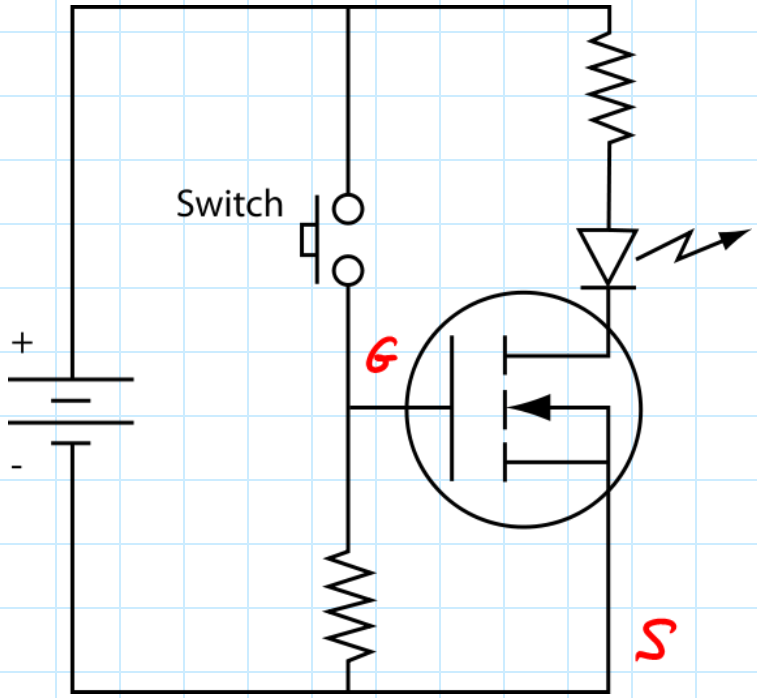
Active loads. Pseudo-NMOS Logic





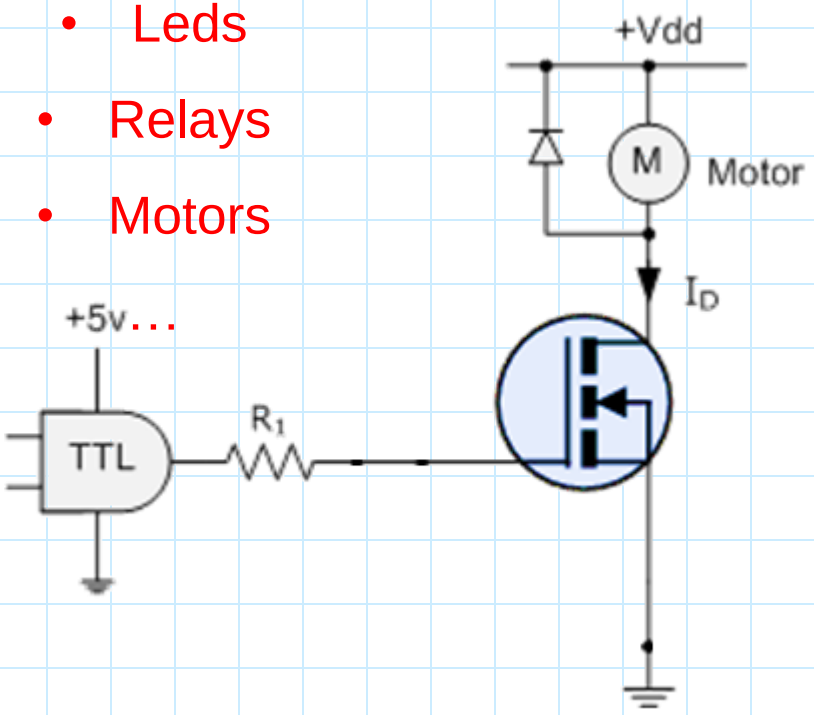
Transference curve versus channel size (W/L)

The MOSFET in switching mode. Applications



We can control:

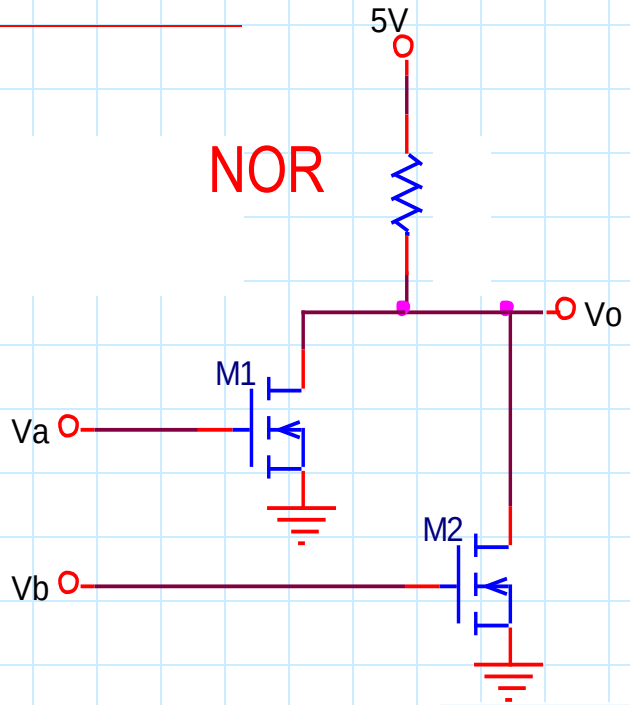
- Leds
- Relays
- Motors



Switch pushed→ VGS = VDD → Mosfet On (closed switch) → LED ON

Switch released→ VGS = 0 → Mosfet off (open switch) → LED OFF

2.4 NMOS logic gates



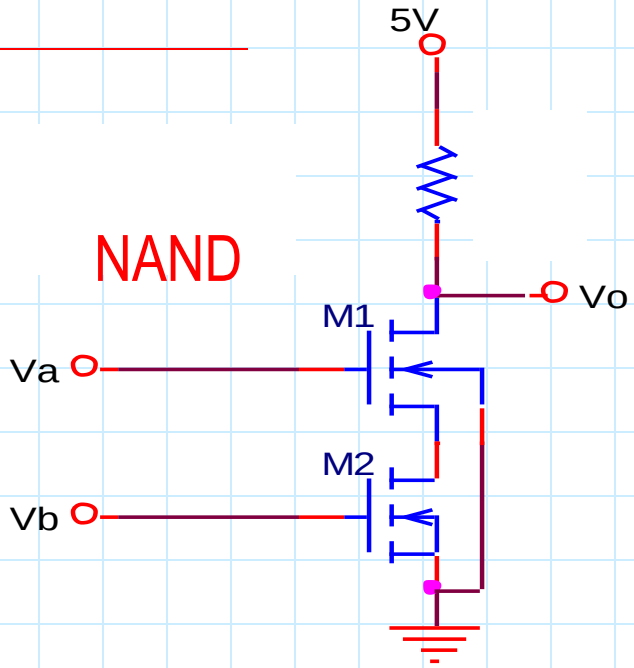
Let's assume:
"0" = 0V
"1" = 5V

$O = \overline{A + B}$

Transistors in parallel

Va	Vb	M1(OFF/ON)	M2 (OFF/ON)	Vo
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0

2.4 NMOS logic gates



Let's assume:
"0" = 0V
"1" = 5V

$O = \overline{A \cdot B}$

Transistors in series

Va	Vb	M1(OFF/ON)	M2 (OFF/ON)	Vo
0	0	OFF	OFF	1
0	1	OFF	OFF	1
1	0	OFF	OFF	1
1	1	ON	ON	0