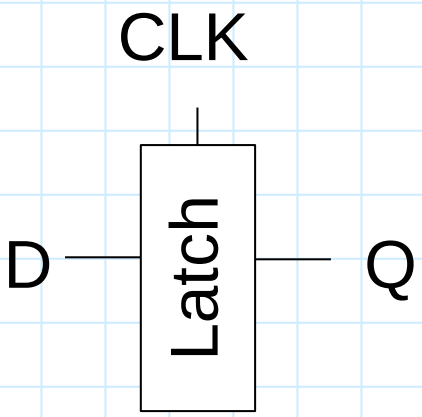
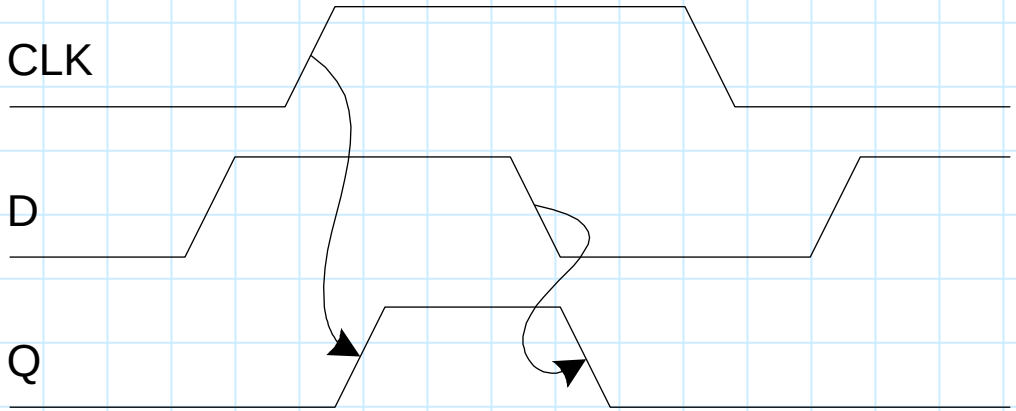
4.3 Latches and Flip-flops (1): The D Latch

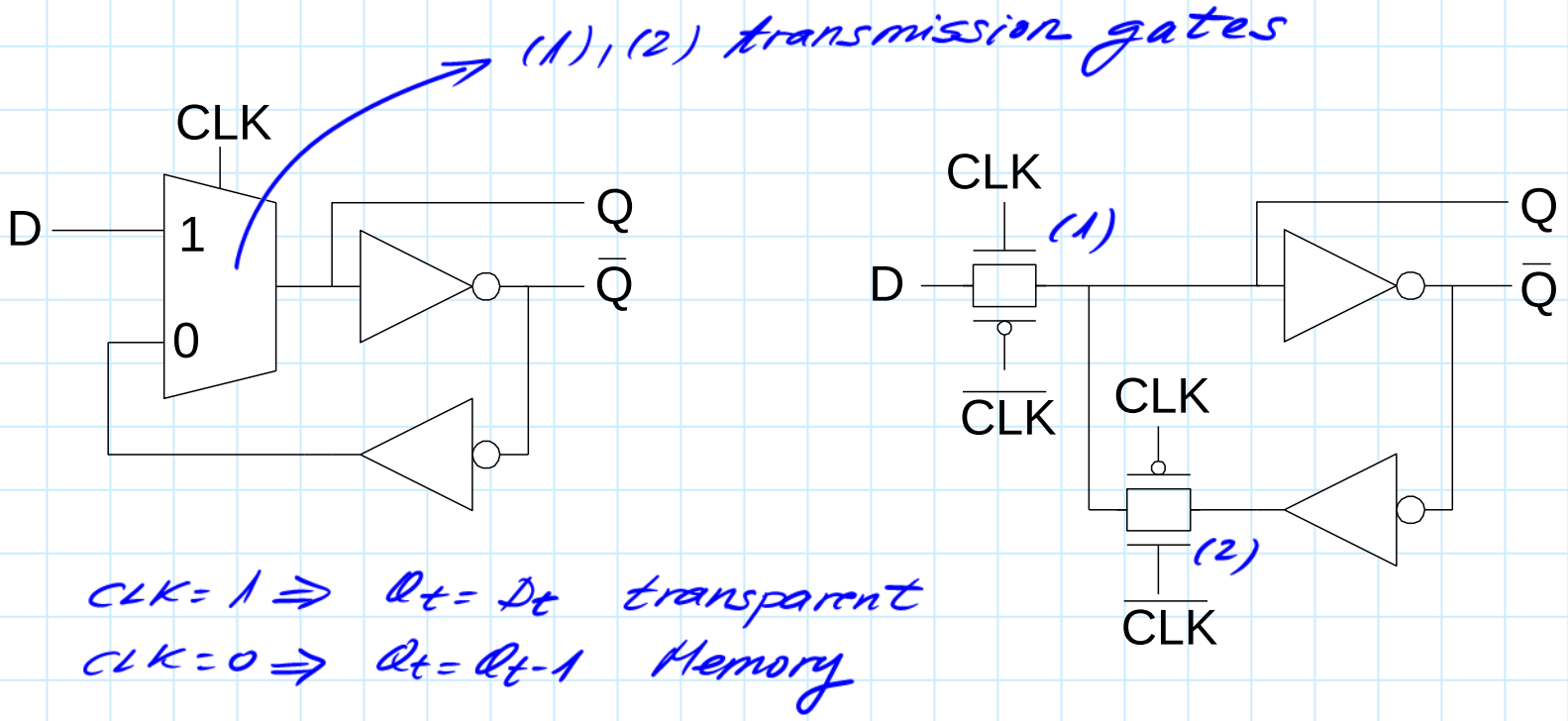
- If CLK = 1, the latch is transparent → enabled ($Q_t = D_t$)
  - (we can see D from Q)
  - D is transmitted to Q as in a buffer
- If CLK = 0, the latch is opaque → disabled
  - (we can see nothing from Q)
  - Q stores the old value independently of D → Memory ($Q_t = Q_{t-1}$)
- Also called transparent or level-triggered latch



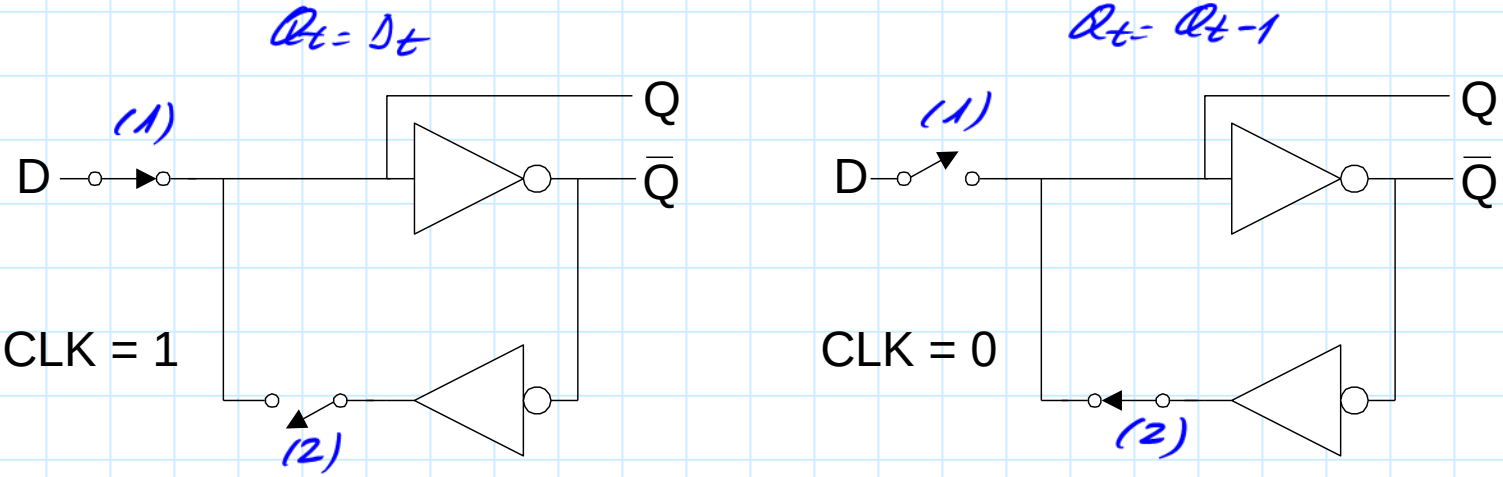


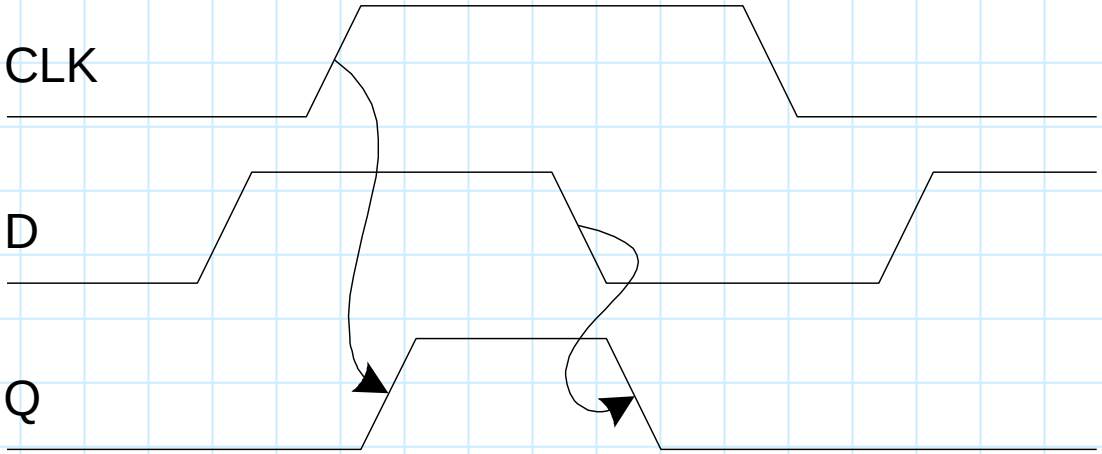
4.3 Latches and Flip-flops (2): Design of a D Latch from transmission gates

- Multiplexer selects D or holds Q



4.3 Latches and Flip-flops (3): Latch D operation

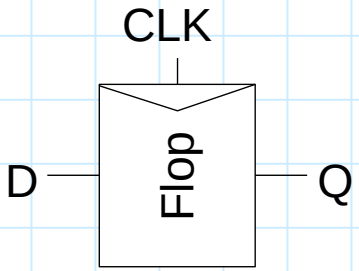


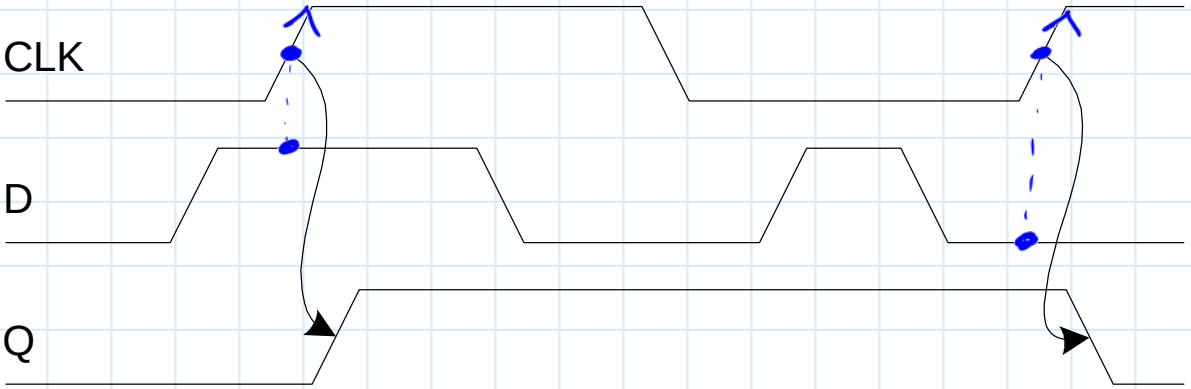


4.3 Latches and Flip-flops (4): The D Flip-flop

$Q_t = D_t$

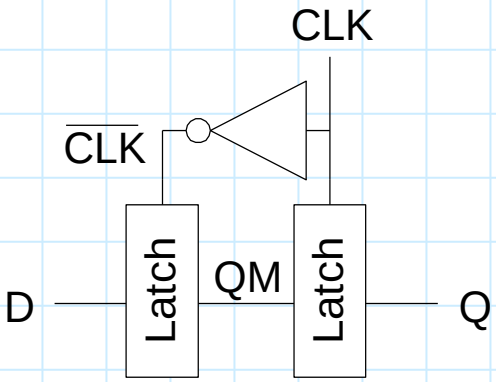
- When CLK has a rising edge, D passes to Q
- Otherwise, Q holds its old value ($Q_t = Q_{t-1}$)
- Also called edge-triggered flip-flop, master-slave flip-flop → Implementation as a master–slave

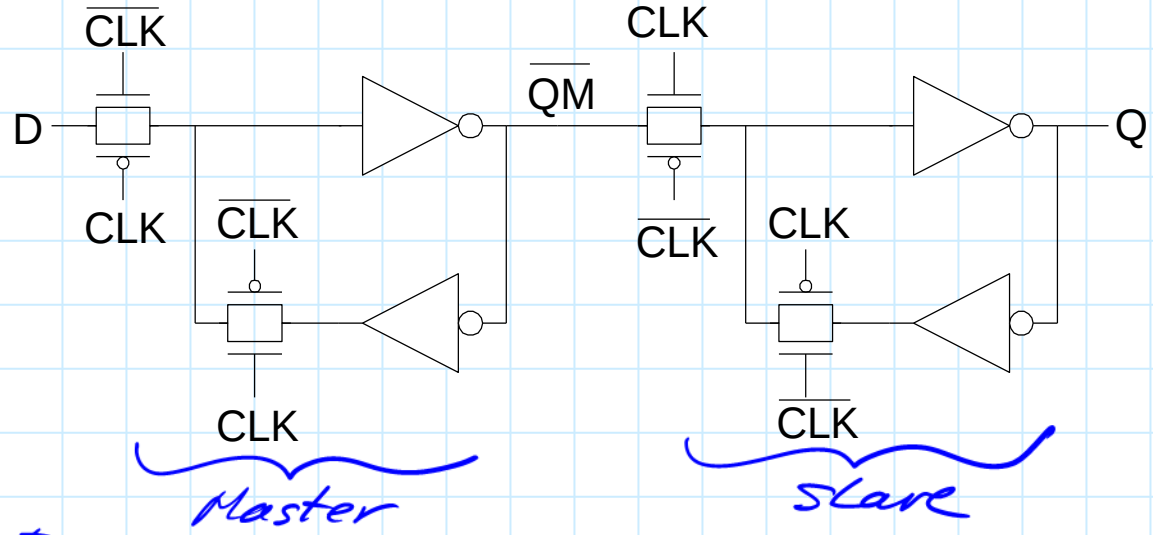




4.3 Latches and Flip-flops (6): Design of a D Flip-flop

- Master-slave design from latches:

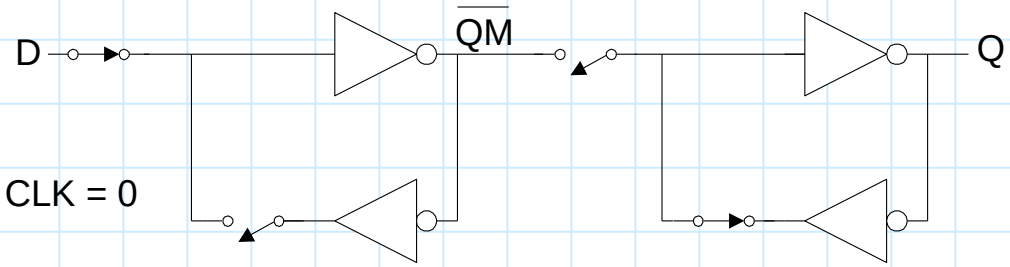


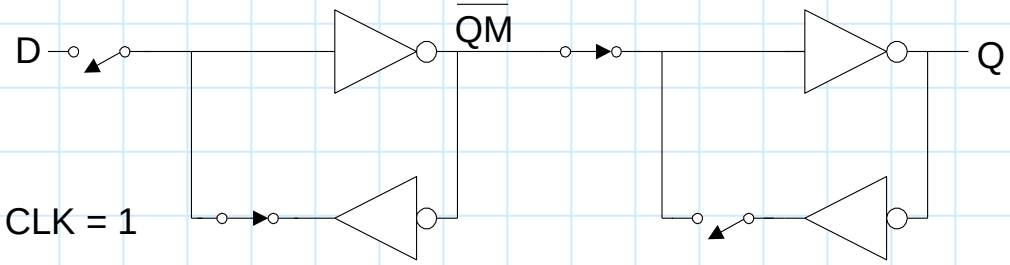


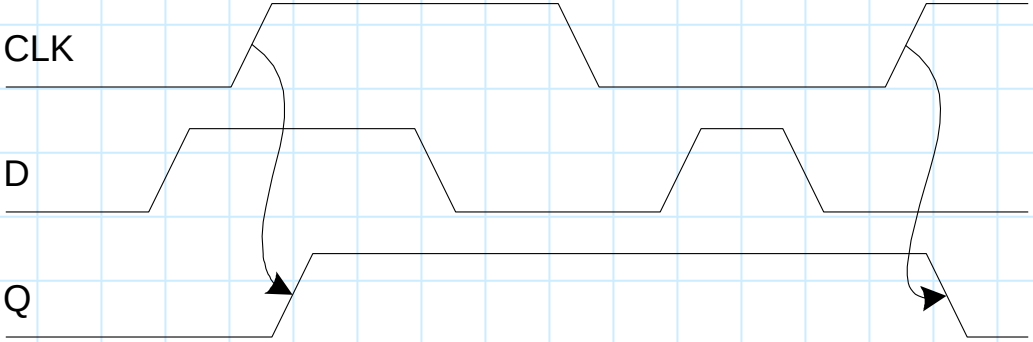
CLK { 0 → Master transparent
1 → Slave transparent

↑ ⇒ Info passes to output

4.3 Latches and Flip-flops (6): D Flip-flop operation

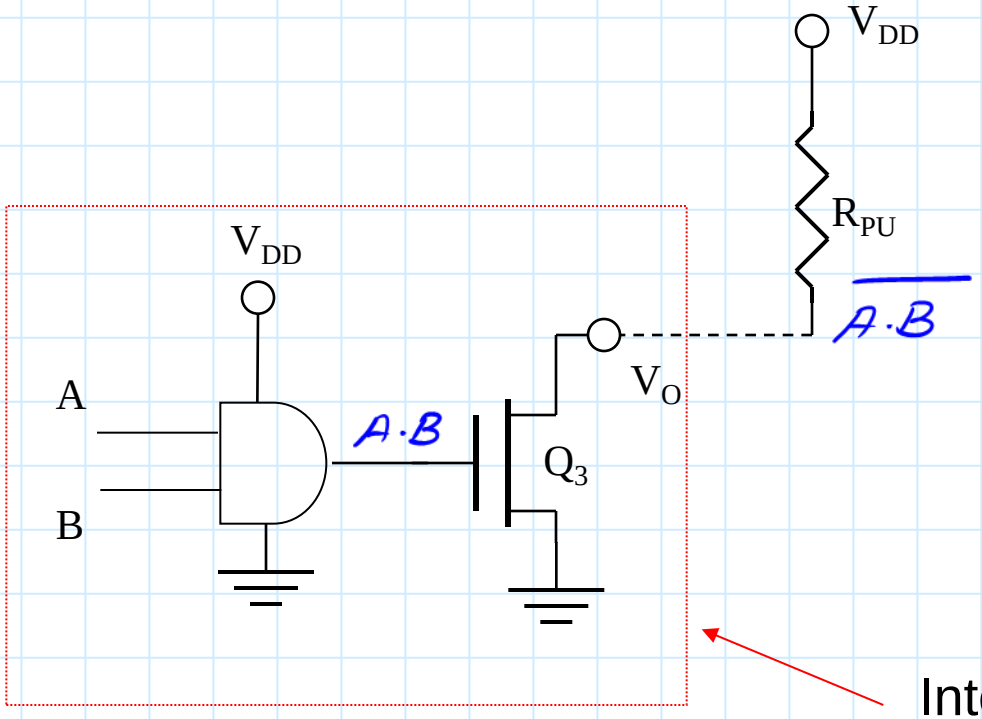






4.4 CMOS special outputs (1)

- Open-drain output (o.d)
- Open-drain CMOS NAND
- R_{PU} is required

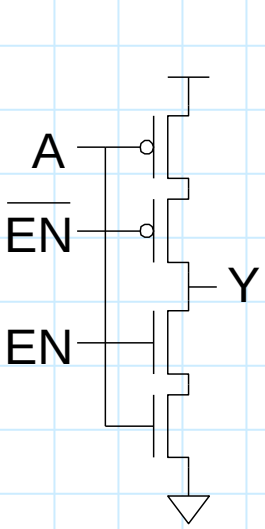


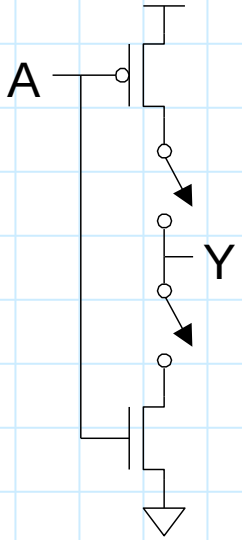
Remember: Wired AND when connecting several (o.d.) outputs

4.4 CMOS special outputs (2)

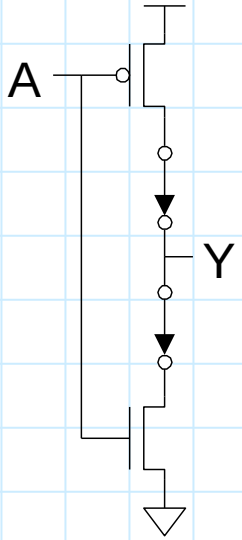
- Tri-state output:
  - Tri-state inverter

EN → Enable

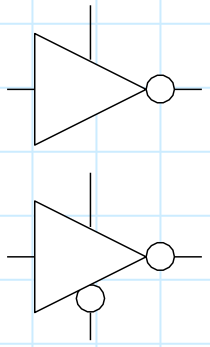




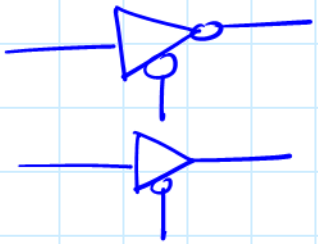
EN = 0
Y = 'Z'



EN = 1
Y = $\overline{A}$



other:



- Tri-state buffer (not inverting buffer):
  - Inverter+Tri-state inverter