# Lab 8: The CMOS inverter. Operation and characteristic parameters

## *1. Contents*



## *2. Objectives*

- To study the basic gate of CMOS family: the inverter.
- To analyze the characteristic parameters in CMOS family: power consumption, transference curve, delays, etc.
- To compare the electrical characteristics of CMOS and TTL logic families.

## *3. Required Material*

- PC and PSpice program for Windows. There is a student version uploaded in PoliformaT.

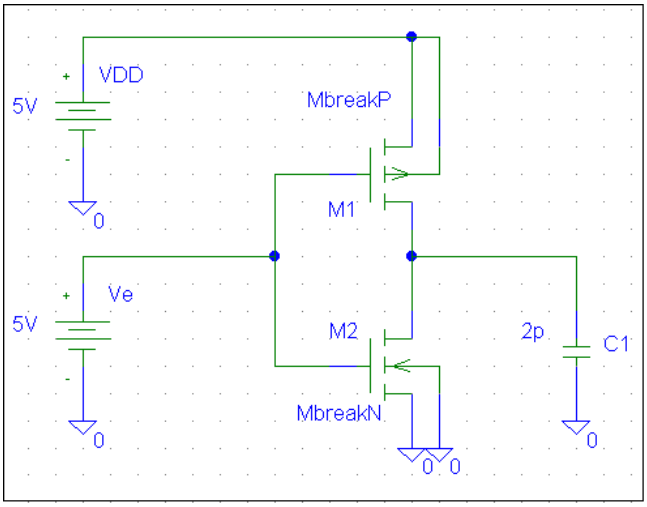
# *3. Practical Development*

Log in with your user of the ALUMNO domain and start PSpice by double clicking on the PSPICE icon on the desktop. Save the created files in the folder W:\TCO\ Prac8.

VERY IMPORTANT: when you will keep the circuit, put a different file name to schematic1, schematic2, etc.

## 3.1 Static operation. Logical values and power consumption

- Edit with the Schematics program the following circuit of a CMOS inverter:




- Note: To import the components, follow the path *Draw→Get New Part→Part Name* in the Edit menu.
  - MbreakP (PMOS transistor)
  - MbreakN (NMOS transistor)
  - AGND (ground)
  - VDC (DC voltage for the input and supply voltage)
  - C (output parasitic capacitance).
  - To position correctly the components in the schematic, note that you can rotate (CTRL-R) and flip (CTRL-F) them.

- Change the names and adjust the values of Ve and $V_{DD}$ (+5 V) voltage sources, as well as the value of capacitor C1 (2p). 1pF (picofarad) = $10^{-12}$ F. C1 is the addition of the drain-source capacitance of M2, the input capacitance of any circuit connected to the output, and the capacitance of (metallic) interconnection wiring.

  NOTE: Please note that unlike the family TTL, **CMOS supply voltage may be different from +5 V (1V, 2.5V, 3.3V, 9V, 12V, ...)**. In practice, we will work with +5 V, to compare the CMOS and TTL behaviors.

- Edit the MOSFET transistor model:

- Using the commands *Edit→Model→Edit Instance Model (Text)*, set Kp (transconductance) and Vto (threshold voltage):

| model MbreakP PMOS | model MbreakN NMOS |
|---|---|
| vto=-1 ($V_T$ voltage) | vto=1 |
| kp=15u (transconductance) | kp=15u |
| *$ | *$ |

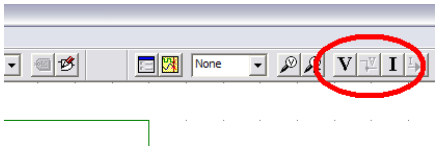
- Specify the width (W) and lenght (L) of the MOSFET channel clicking twice on the symbol of the transistor and changing its attributes: W = L = 1u., where 1u = 1 micron = $10^{-6}$. Observe that we have assigned the same values of Kp and (W/L) to both transistors, for the purpose of more simplicity.

- Enable the type of analysis as *Bias Point Analysis*. (*Analysis -> setup … -> **Bias point detail***). This is a DC (direct current) analysis.

- Run the simulation (press F11 key or *Analysis-> Simulate*).

- Check, by clicking the **V** icon in the editing program, that we have an output voltage that can be identified as a logic "0". This voltage is **$V_{OL}$**.

  * **$V_{OL}$ =** _____




  - Repeat the previous step, changing the input voltage Ve to **0V** ("0") and verify that the displayed output voltage can be identified as a logic “1”. This voltage is **$V_{OH}$**.

    * **$V_{OH}$ =** _____

  - Measure the static current consumption in both cases. To do this, click the **I** icon. Check that the current exiting $V_{DD}$ is almost **negligible**. This corresponds to **leakage currents ($I_{leakage}$)**.

    * **$I_{stat\ (H)}$ =** _____
    * **$I_{stat\ (L)}$ =** _____

- Obtain the static power consumption: $P_{stat} = V_{DD} \times I_{stat} = V_{DD} \times \frac{1}{2}(I_{estH} + I_{estL})$ p8
- D(D(
  * **$P_{stat}$=** _____mW

NOTE: The main differences with respect to TTL technology you should have observed are the following:

- The CMOS voltage levels $V_{OH}$ and $V_{OL}$ are very near of the limits, it is to say, they are very similar to $V_{DD}$ and GND, respectively. For TTL, the output high level is about 4.5V, and the low level is about 0.15V.
- The static consumption is negligible in CMOS. In TTL, the $I_{CC}$ static currents are of the order of several mA.

## *3.2* Transference curve. Noise margins.

To obtain the transfer curve we should **sweep the input voltage** between 0V and 5V, and represent the output voltage depending on this input. Let us see how you can do this in the Pspice:

- Enable the type of analysis such as ***DC Sweep***. (*Analysis -> setup … -> DC Sweep*). Specify the range of variation of Ve between 0 and 5V, with increments of 0.01V. Select a linear sweep (*linear*) of Ve

- Run the simulation (F11 key or *Analysis-> Simulate*).

- Once completed, the Probe window will be automatically opened, allowing signals to be graphically represented. To make the selection of the signal, activate the *Trace→Add Trace* option. In our case, we must choose the output voltage, which corresponds to the drain of M2 transistor. Therefore, choose V (M2:d) out of all that are shown. **Caution¡: the name of the transistor in your schenmatic could be different to M2. Be sure of the name seeing the schematic.**

NOTE: An alternative way to display the output voltage without having to select it in PROBE is to put a voltage probe  in the output voltage (in the schematic).

- When doing so, you should see the CMOS inverter transfer curve, where you can measure the voltage parameters. Figure 1 shows the shape of a generic inverter transfer curve.

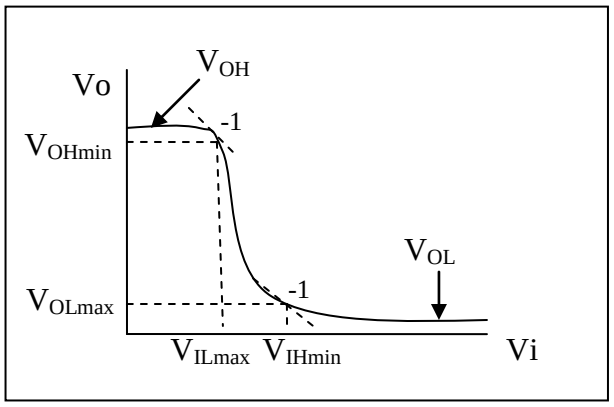



Figure 1. Transfer curve of an inverter.

- Measure, using the cursors in PROBE, the **output voltages** (**$V_{OH}$ y $V_{OL}$**).
  - **$V_{OH}$ = _____**

- **$V_{OL}$ = _____**

- Measure approximately the Ve values corresponding to the the elbows of the transfer curve (-1 slope) . The approximate values of **$V_{ILmax}$ y $V_{IHmin}$** correspond to the middle of each elbow of the transfer curve.
- **Warning:** The elbow is quite broad, making it difficult to pinpoint the exact value of voltages. Representing the derivative (Add_Plot → función D(V(M2)) in Trace) of the curve, the voltage values correspond to the points with derivative -1, that can be easily located.

  - **$V_{IHmin}$ =** _____
  - **$V_{ILmax}$ =**
  - **$V_{OHmin}$ =**
  - **$V_{OLmax}$ =**_____

- Calculate approximately the **noise margins**:

  - **$NM_H$** ≈ $V_{OH}$ - $V_{IHmin}$ = _____
  - **$NM_L$** ≈ $V_{IL}$ - $V_{OLmax}$ = _____

- Verify that this is a **pretty ideal transfer curve**, very symmetrical, with output voltages very near the limits and with **large noise margins**. The transition takes place approximately in $V_{DD}/2$ (about 2.5V).

NOTE: Observe that the noise margins and output voltage levels are better than in TTL family (the TTL NM is about 0.4V).

## 3.3 Dynamic consumption on the transitions

We can display the current consumption through MOSFET transistors to check that there is only comsumption during the transition from one state to another, while there is no consumption when we have a high or low level stabilized at the output, as theory predicts.

- To watch it, put a new curve on top of the previous transfer curve. Use the command *Plot→Add Plot to window* and add as signal to display the drain current of NMOS transistor (ID (M2)).

- Note that the current consumption is concentrated in the **transition zone**, where **both transistors conduct simultaneously**. This consumption is also called short-circuit current (short-circuit power dissipation), since it involves the activation of a conduction path between $V_{DD}$ and GND. It is due to the finite duration of the edges of the input signal. Figure 2 illustrates this dynamic consumption, for a generic inverter.

    - Measure the maximum current value in the transition, using the cursors. Calculate the power in mW.

        - $I_{sc}$ = _____(mA)

        - $P_{sc} = V_{DD} \times I_{sc}$ = _____(mW)

    This power consumption occurs in every input transition (rising or falling). The more transitions per time unit are produced, there is more consumption. It is therefore **directly proportional to the frequency** of the input signal. It is also **proportional to the duration of the rising and falling edges** of the input signal.

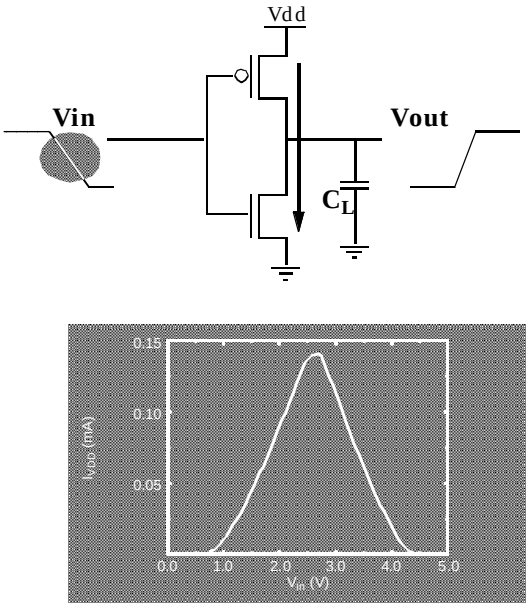



Figure 2. Dynamic consumption in the transitions.

## *3.4* Propagation delays

We will introduce a positive input pulse and measure the delay of the inverted pulse at the output. The delay is due to the intrinsic capacities of MOS transistors and to the **load capacity $C_L$**, the latter due to the loads (inputs) connected to the output, and at to the interconnection wiring.

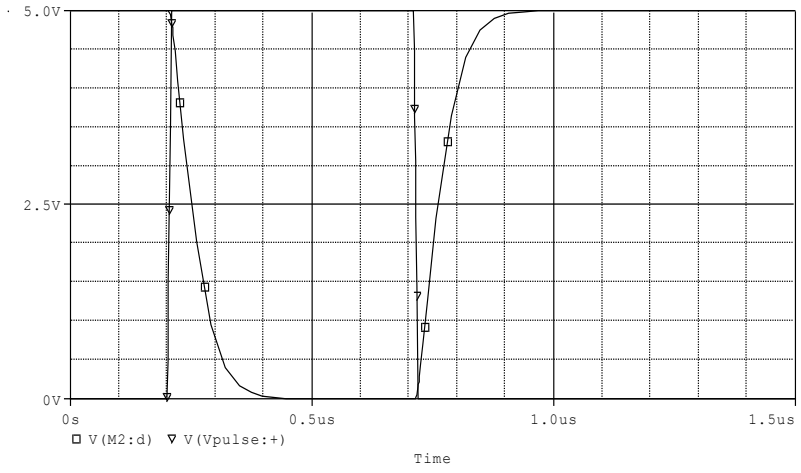
- First, replace the DC input at Ve with a **pulse generator, *Vpulse***. After entering this component, edit its attributes, setting up the following values:

  DC=0; AC=0; V1=0; V2=5; TD=200n; TR=10n; TF=10n; PW=500n

  This sets a positive pulse with an initial time of 200 ns, a rise time of 10ns, a pulse width of 500ns and a fall time of 10ns.

- Then proceed to change the simulation mode (*Analysis→ Setup…**Transient Analysis***), adjusting the background timescale value to 1500ns and the *Print step* in default. After that, you can start the simulation (*Analysis→Simulate)*.

- The following is to add two traces to be displayed in Probe: the input pulse voltage V(Vpulse:+) and output voltage: V(M2:d). Alternatively, in the schematic can be placed voltage probes at the inlput and output. The resulting graph obtained should be similar to the one shown below. Note the exponential edges due to the charge and discharge of $C_L$.




- After that, we can measure on this graph the **$tp_{LH}$ and $tp_{HL}$ delay times**. They should be measured from the midpoint of the input and output edges, as illustrated in Figure 3. We recommend the use of cursors. To measure them better, you can zoom in the area of the edges.

  * $tp_{HL}$ = _____ ns
  * $tp_{LH}$ = _____ ns

- Compare $tp_{HL}$ and $tp_{LH}$. As both transistors are defined with the same parameters, it appears that the delays should be approximately equal. This is **different in the TTL family**, where delays are asymmetric ($tp_{LH}$> $tp_{HL}$).

- To check the **effect of $C_L$**, change on the schematic its value, setting it for example to 10 pF. Run a new simulation and observe the change of delay times. Justify the obtained result.

  * $tp_{HL}$ = _____ ns
  * $tp_{LH}$ = _____ ns

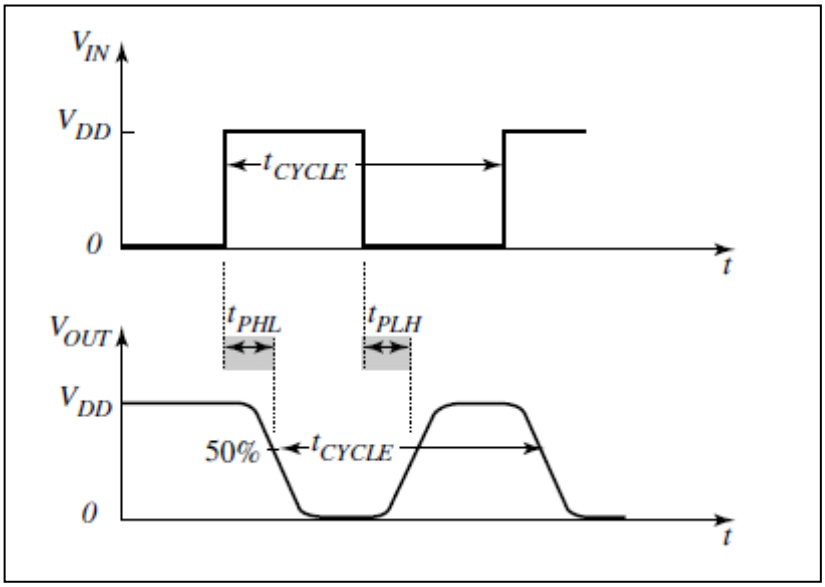



Figure 3. Propagation delays.

**Caution:** Please note that perhaps the exponential rise of the output signal is not fully seen, as soon as it is slower. For vilualising it correctlly, please increase the duration of the Transient simulation to 2000 ns.

- Delays decrease with increasing kp (transconductance of transistors), (W/L) (size of transistors) and VDD. You can optionally verify this influence.

## *3.5* Dynamic power consumption due to the charge of parasitic capacitances.

• Study the effect of $C_L$ on **dynamic consumption**. Change $C_L$ = 2 pF in the schematic. Simulate again and represent the value of the consumed current (IS (M1)) versus time. You need to activate Plot → Add Plot to window to create a new graph.

Do you see the same consumption in the two transitions?

Please note that relevant consumption occurs in the transition L → H, where $C_L$ is charged with current supplied by the power supply. In H→L transition, $C_L$ discharges through the NMOS transistor and there is no current consumption from the power supply.

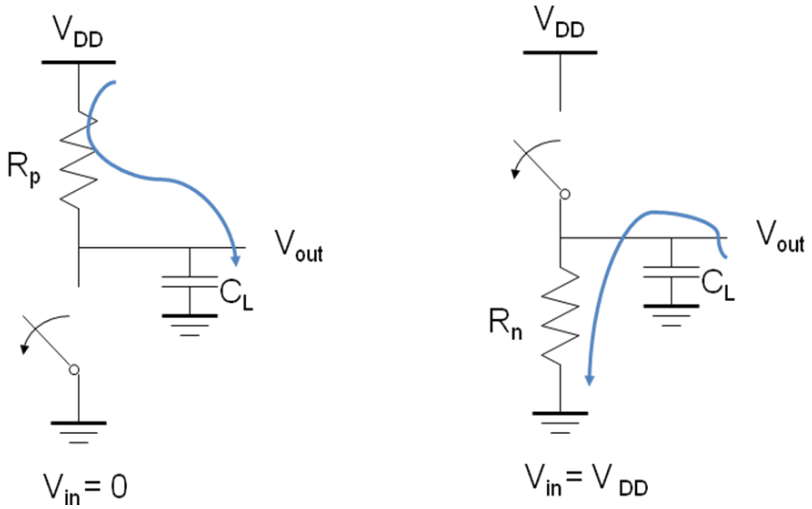



Figure 4. Dynamic consumption due to the load $C_L$