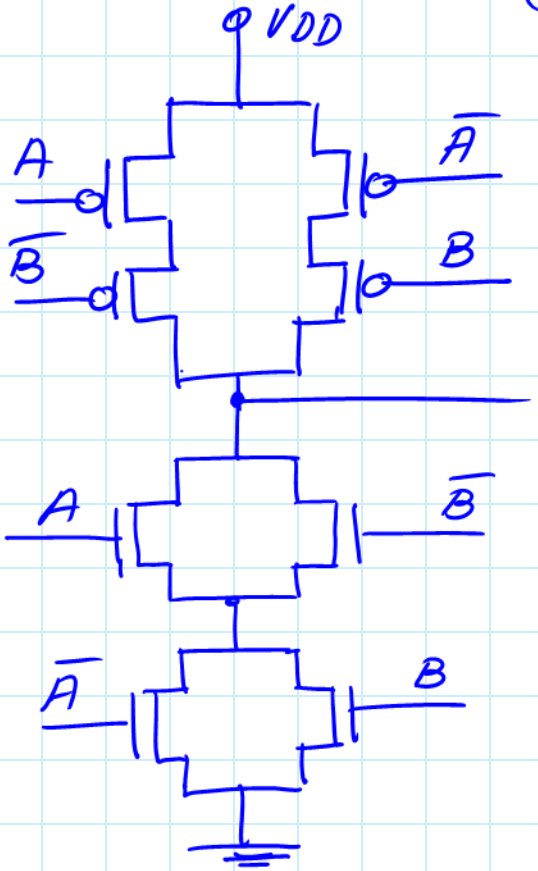
UNIT 4. CMOS

1.4. Design a XOR function with complementary CMOS logic. Estimate the number of transistors and compare with a traditional design based on logic gates.

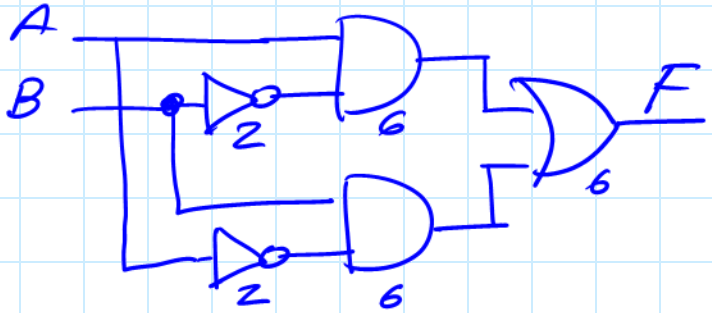
Note: $F = A \oplus B = \overline{A}B + A\overline{B}$

$F = \overline{\overline{A}B + A\overline{B}} = \overline{(A+\overline{B})\cdot(\overline{A}+B)}$



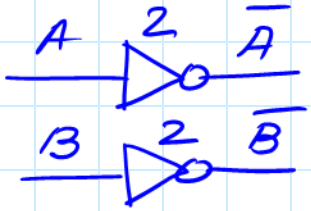
12 transistors

Traditional:



22 transistors

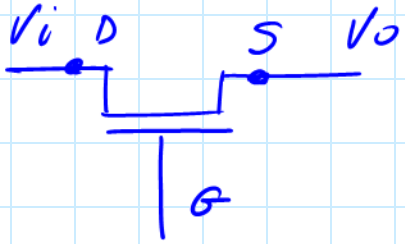
We save 10 designing directly using transistors!



UNIT 4. CMOS

2.1. Given a NMOS transmission gate with a transistor of |VT| = 1.5V. A voltage of 0V is applied to the input and 5V to gate terminal G. What voltage is obtained at its output?:

A) 5V
B) 0V
C) 3.5V
D) 1.5V



$V_{GS} > V_T \Rightarrow V_G - V_S > V_T \Rightarrow$

$V_S < V_G - V_T$; $V_o < V_G - V_T = 3.5V$