PRESENTATION FOR:

"ESTRUCTURA DE COMPUTADRES"

Computer Organization

Course 2018-2019

ETS Ingeniería Informática

Universitat Politècnica de València

Contacting me

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  - Note: “3N-1” stands for **3**rd floor, **N**orth corridor, office **1**
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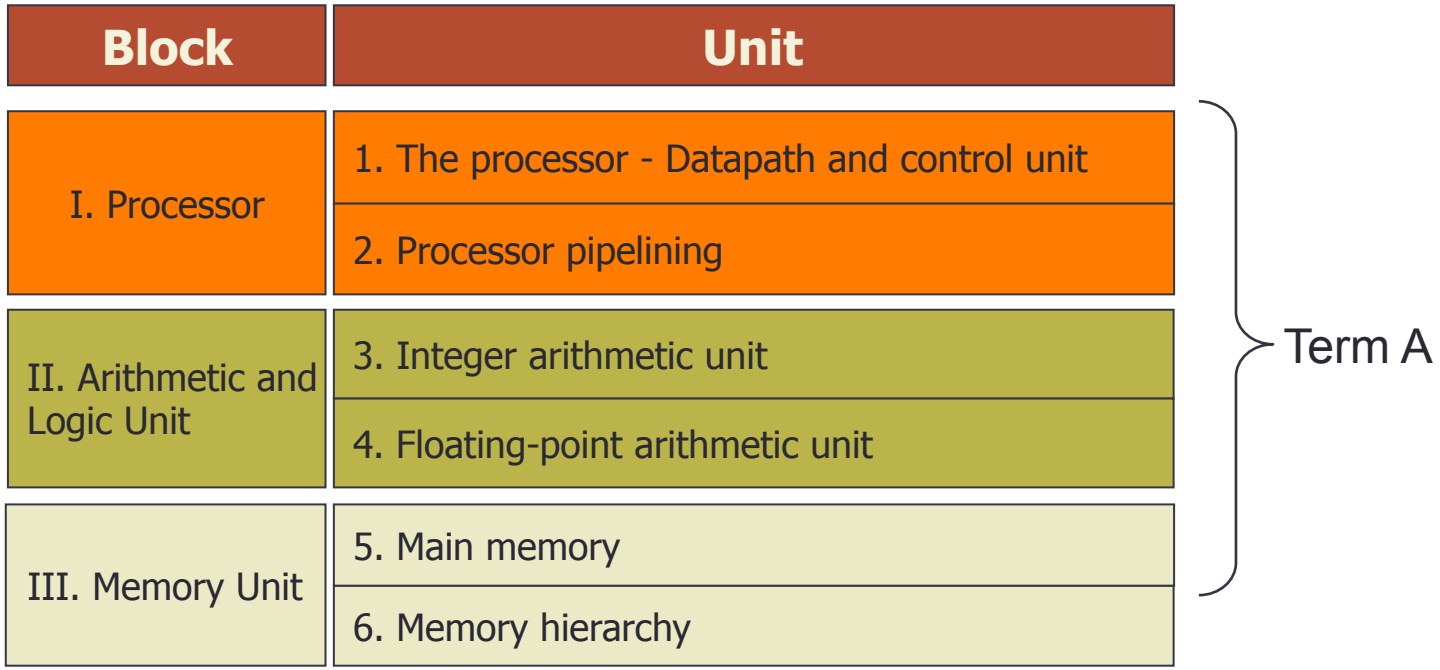
Subject goals

- To give a view of all functional units in a computer and how they interact
  - Central Processing Unit (CPU) or simply *the processor*
  - Arithmetic circuits in the ALU and their performance
  - The memory system – main memory and memory hierarchy
  - The I/O unit, including peripherals and busses
- Special emphasis on how hardware supports software and how computer organization helps improving performance

- EC builds on the 1st year's Computer Fundamentals and Computer Technology (*Fundamentos de Computadores* and *Tecnología de Computadores*)

Programme: theory



Programme: theory

Block	Unit
III. Memory Unit	5. Main memory
	6. Memory hierarchy
IV. I/O Unit	7. I/O interfaces and adapters
	8. Synchronization mechanisms
	9. I/O Transfer techniques
V. Busses and Peripherals	10. Peripheral devices
	11. Interconnection busses

Term B

Programme: lab (term A)

Lab session
1. Assembly language (I)
2. Datapath and control unit
3. Assembly language (II)
4. Pipelined processor
EVALUATION (I)
5. Arithmetics (I)
6. Arithmetics (II)
7. Arithmetics (III)
EVALUATION (II)
8. Configuration of memory modules

Note: all sessions have a duration of 1:30h

Programme: lab (term B)

Lab session
9. Assembly language (III)
10. Cache memory (I)
11. Cache memory (II)
EVALUATION (III)
12. Polling synchronization
13. Interrupt synchronization
14. System functions (I)
15. System functions (II)
EVALUATION (IV)
16. Magnetic disks

All sessions have a duration of 1:30h

Laboratory

- Group E (ARA group):
- Sessions will be starting on Tuesday 18th September

Lab sessions will take place at the

Laboratorio de Estructura de Computadores

Building 1G, 2nd Floor, North-East side

1st term: Prof. Ana Pont

2nd term: Prof. Alberto González

Lab schedule

1st term

Septiembre 2018

L	M	X	J	V	
3	4	5 (INICIO)	6	7	
10	11	12	13	14	
17	18	19	20	21	P1
24	25	26	27	28	P2

Octubre 2018

L	M	X	J	V	
1	2	3	4	5	P3
8 MARTES	9	10	11	12	
15	16	17	18	19	P4
22	23	24	25	26	EVAL I
29	30	31			

Noviembre 2018

L	M	X	J	V	
			1	2	
5	6	7	8	9	
12	13	14	15	16	P5
19	20	21	22	23	P6
26	27	28	29	30	P7

Diciembre 2018

L	M	X	J	V	
3	4	5 JUEVES	6	7	
10	11	12	13	14	EVAL II
17	18	19	20	21	P8 (task)
24	25	26	27	28	

2nd term

Febrero 2019

L	M	X	J	V	
				1	
4	5	6	7	8	P9
11	12	13	14	15	P10
18	19	20	21	22	P11
25	26	27	28		EVAL III

Marzo 2019

L	M	X	J	V	
				1	EVAL III
4	5	6	7	8	
11	12	13	14	15	
18	19	20	21	22	
25	26	27	28	29	

Abril 2019

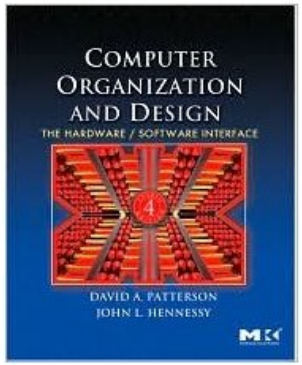
L	M	X	J	V	
1	2	3	4	5	P12
8	9	10	11	12	P13
15	16	17	18	19	
22	23	24	25	26	
29	30				

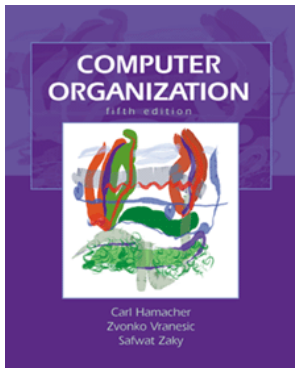
Mayo 2019

L	M	X	J	V	
		1	2	3	P14
6	7	8	9	10	P14
13	14	15	16	17	P15
20	21	22	23	24	EVAL IV

Base Bibliography

- D. Patterson, J. Hennessy. *Computer organization and design. The hardware/software interface*. 4th edition. 2009. Elsevier
- C. Hamacher, Z. Vranesic, S. Zaky. *Computer Organization*. 5th edition. 2001. McGraw-Hill
- W. Stallings. *Computer Organization and Architecture. Designing for Performance*. 7th edition. 2006. Prentice Hall





Subject evaluation

- Three aspects will be considered:
  - Written exams (60%)
  - Lab sessions (25%)
  - On-site and off-site student's work (15%)

- **Written exams (60%)**
  - 1st partial exam: 7 January 2019 (units 1-5)
    - Resit 1st partial exam: 4 February 2019
  - 2nd partial exam: 4 June 2019 (units 6-11)
    - Resit 2nd partial exam: 14 June 2019
  - Both exams have the same weight (50% each)

Subject evaluation

- **Lab sessions (25%)**
  - There are 4 evaluation sessions scheduled. Evaluation is individual, but you may form groups of two for regular sessions
  - IMPORTANT
    - Sessions must be **prepared in advance**
    - **No admittance** in the lab after 10 min past the start time
    - There will be **no resit sessions**
    - Four individual evaluation sessions
    - Presence control at the lab, with minimum attendance requirements:
      - 3 full sessions out of sessions 1 to 4 for evaluation 1
      - 2 full sessions out of sessions 5 to 7 for evaluation 2
        - Eval. 2 contributes 7/10 points. The remaining 3/10 points come from session 8 (Memory module configuration) consisting of a deliverable task assignment
      - 2 full sessions out of sessions 9 to 11 for evaluation 3
      - 3 full sessions out of sessions 12 to 15 for evaluation 4
        - Lab session 16 (magnetic disks) will be evaluated based on a deliverable task and as part of the 2nd term exam

Subject evaluation

- **Student's on-site and off-site work (15%)**
  - 0.5 points assignment on magnetic disks (2nd term)
  - 1 point (0.5 points/term), based on:
    - Short written tests at the classroom
    - Problem solving – *deliverable assignments*
    - On-line questionnaires
    - …

Final Mark

Final Mark = (Exams × 0.60) + (Lab × 0.25) + (Work × 0.15)

- No minimal mark required in any of the three aspects
  - “Exams” refers to the two written exams
  - “Lab” refers to the four lab evaluations
  - “Work” considers exercises proposed as continued work
- For further recommendations and norms, see the document available in PoliformaT (folder “Organización”)
- Materials specific to group E will be available in PoliformaT under:

Recursos → Grupos → E

Competences

- ETC is control point for the "Continued Learning" competence (*Aprendizaje Permanente*)
- Mark:
  - A – Excellent
  - B – Adequate
  - C – In progress
  - D – Not fulfilled
- Evaluation will be based on the marks of two deliverable tasks (memory module configuration and magnetic disks)
- Failing to deliver both assignments will result in mark D in this competence