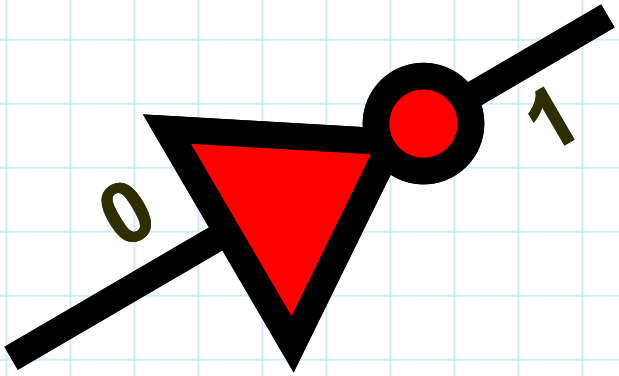

Unit 3: Introduction to integrated logic families

Objectives

At the end of this Unit, the student should:

- Understand the definition of the states of logic gates.
- Know and understand the behavior of input and output terminals of a logic circuit.
- Understand the characteristic parameters of a logic gate, both at electrical and temporal level.
- Understand the problem of interconnecting integrated logic circuits with different technologies, solving some case studies of interconnection.
- Know the different TTL subfamilies

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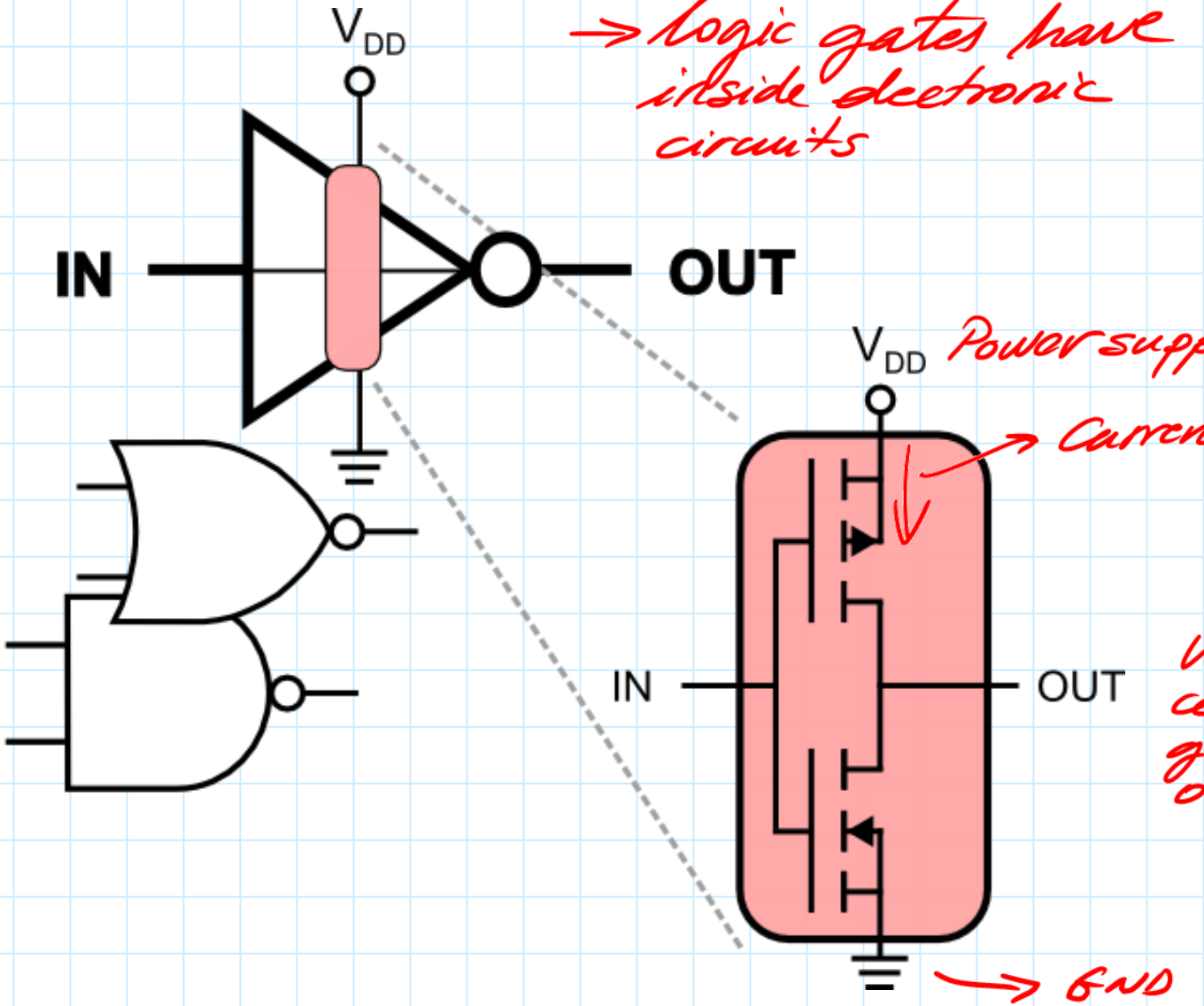
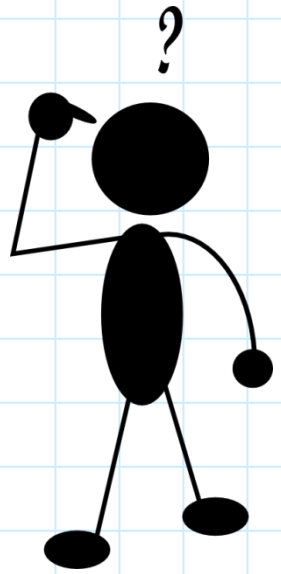
Contents

Introduction.
The logic gate



→ Logic gates have inside electronic circuits



V_{DD} Power supply

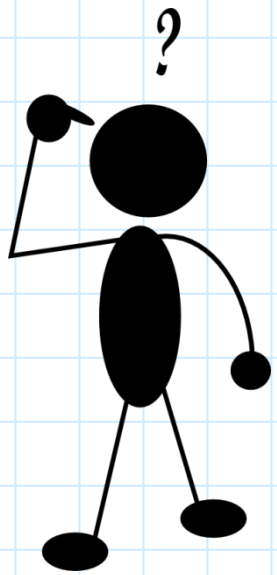
→ current consumption

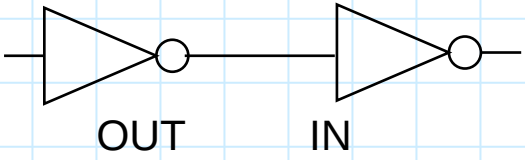
We can't connect ∞ gates at the output!

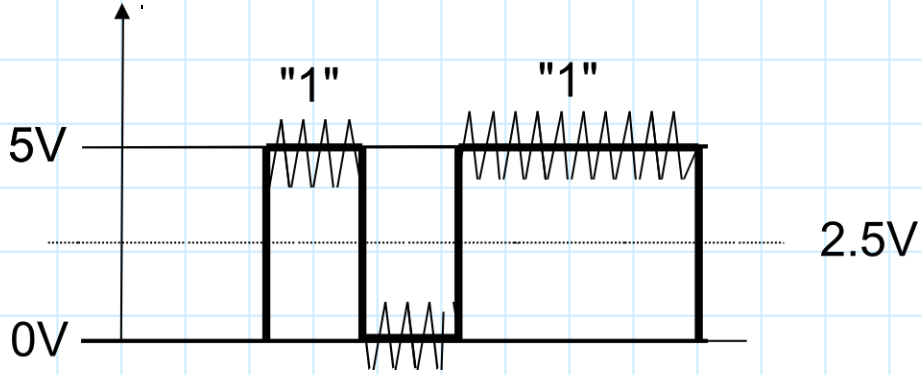
→ GND

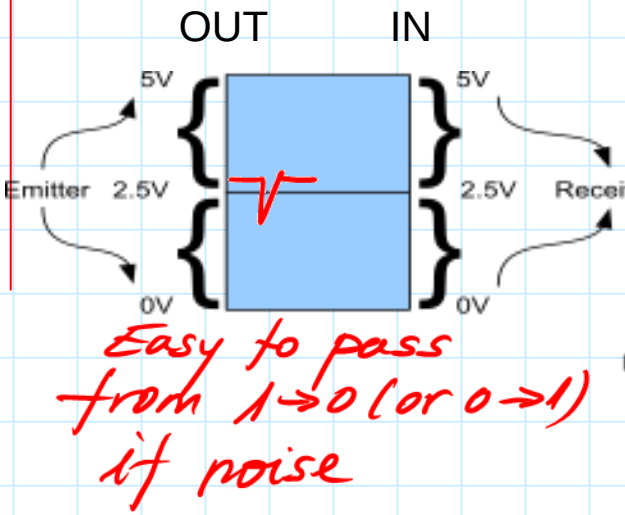
Introduction. Abstraction of “0” and “1”

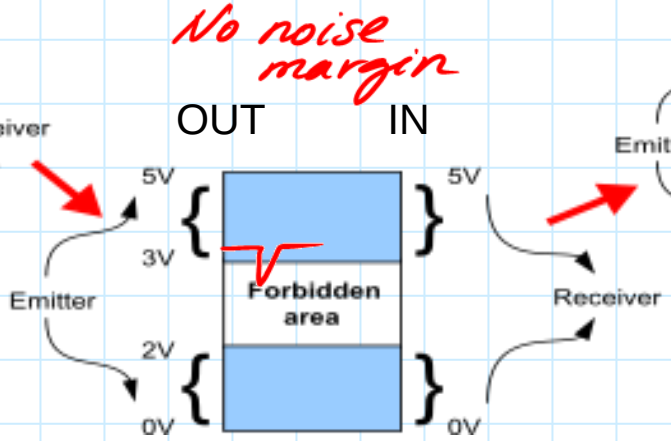
Logic levels "0" and "1" are not fixed voltage values, each one is associated with a different voltage range

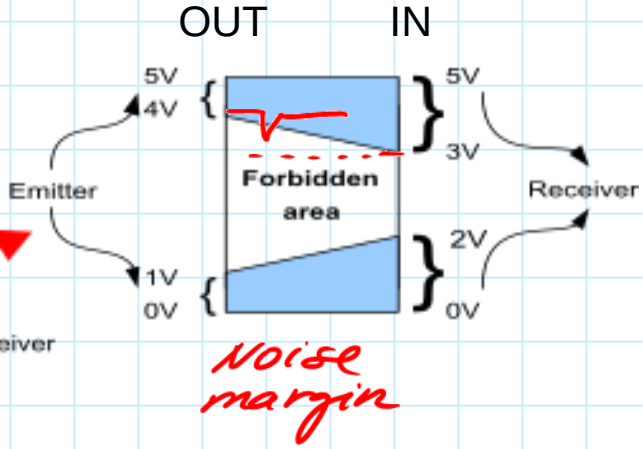












Introduction.
What is a logic family?

Logic family

– Set of functional elements (logic gates, biestables, decoders, counters, ...) with the same base circuit and the same manufacturing technology

– Electric compatibility, direct interconnection

all family members understand themselves

Main logic families

– Bipolar
  - Transistor Transistor Logic (**TTL, LSTTL**, STTL, ASTTL, ALSTTL, FAST)
  - Emitter Coupled Logic (ECL) (old)

Standard (old)

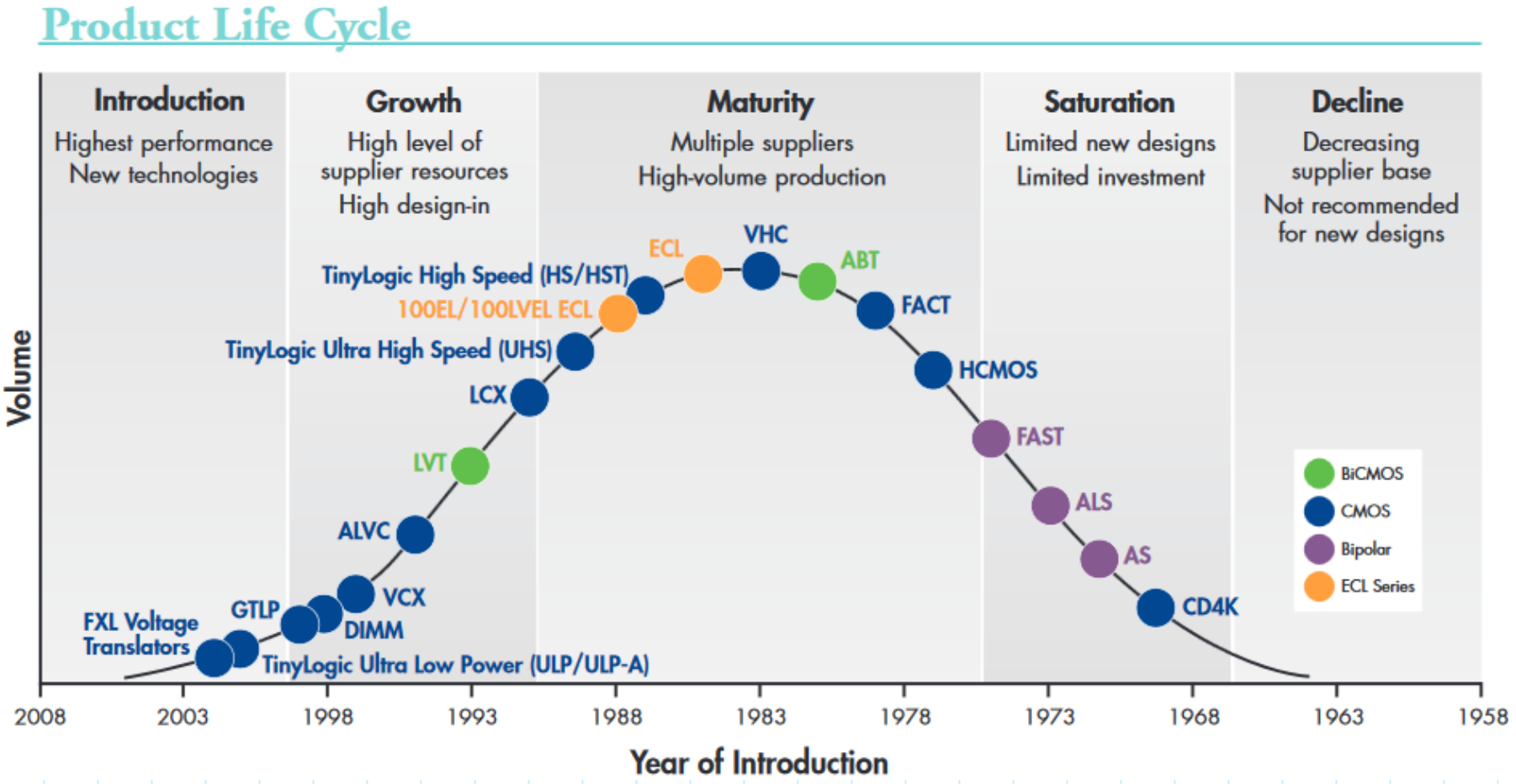
– MOS
  - **PMOS, NMOS**
  - **CMOS**
  - **Pass-transistor CMOS**
  - Dynamic CMOS (Domino)

} CMOS: high integration density

– BiCMOS (Bipolar- CMOS) High output current

– Ga As (Gallium Arsenide) High Speed

Introduction.
Logic families evolution



Source: https://www.fairchildsemi.com/collateral/Logic-Selection-Guide.pdf (2008)

Introduction. Integration scales

SSI (Small Scale of Integration): up to 10 gates (*simple gates, flip-flops*)

MSI (Medium Scale of Integration): 10 to 100 gates (*decoders, multiplexers, adders, counters, registers, ...)*

LSI (Large Scale of Integration): 100 to 1000 gates (*microprocessors (8bits), memories, …)*

VLSI (Very Large Scale of Integration): 1000 to 100000 gates (*memories, microprocessors and big PLDs*) Normaly, this is used today

ULSI (Ultra Large Scale of Integration): more than 100K gates *(microprocessors* (32+), *FPGA, microcontrollers, SoC* ...

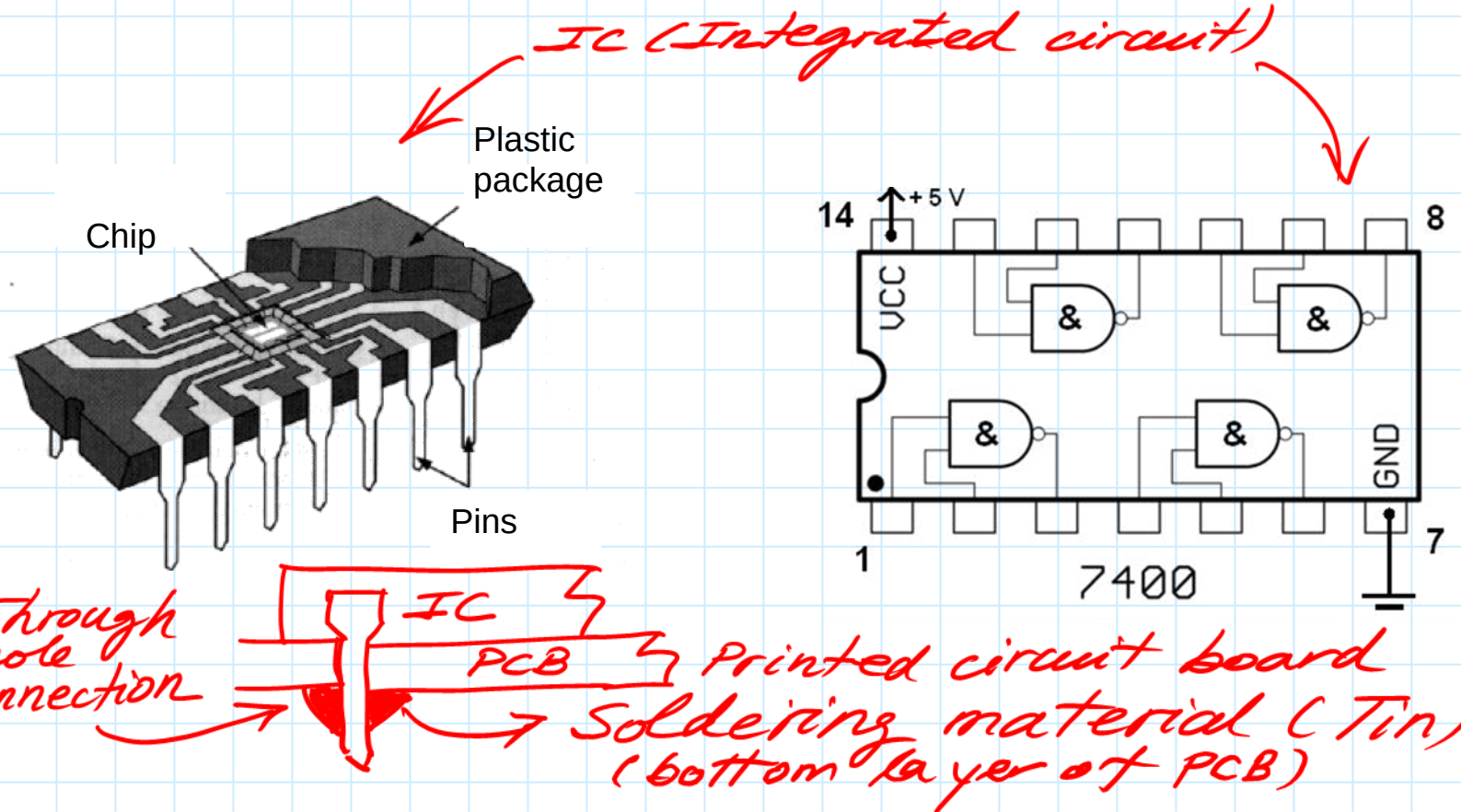
GSI*:* (Giga Scale of Integration). More than 1M gates.

Today : 1 billion transistor / chip or more

Approx. Conversion Factor: For CMOS technology: 6 transistors/gate

Introduction
Packages

To place the integrated circuit in an electronic system built on a printed circuit board (eg. a motherboard of a modern computer) is necessary to insert the chip in a protective shell called package.



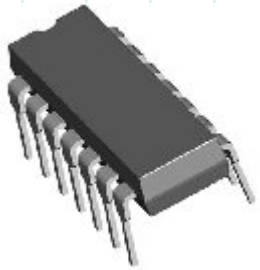
Introduction Packages

Soldered in upper layer

SMD : Surface Mount Device

Packaging technology has followed a development parallel to the integration density

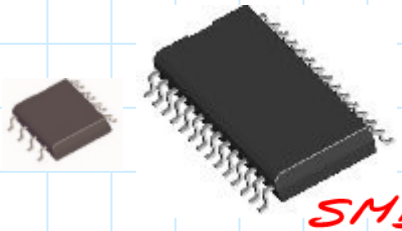
Dual-In-Line Package (DIP ó DIL) (until 80 pins)



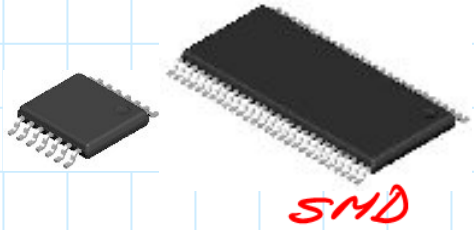
Plastic Leaded Chip Carrier (PLCC) (until 84 pins)

SMD

Small Outline Integrated Circuit (SOIC) / *Shrink Small Outline Package* (SSOP), *Thin Shrink Small Outline Package* (TSSOP)

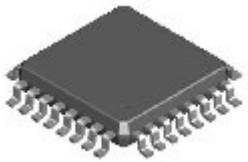


SMD



SMD

Quad Flat Pack (QFP) *Thin Quad Flat Package* (TQFP) (until 300 pins)



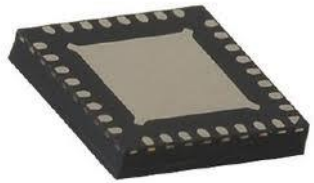
SMD

Pin Grid Array (PGA) (until 400 pins)

Ball Grid Array (BGA) (greater pin number)

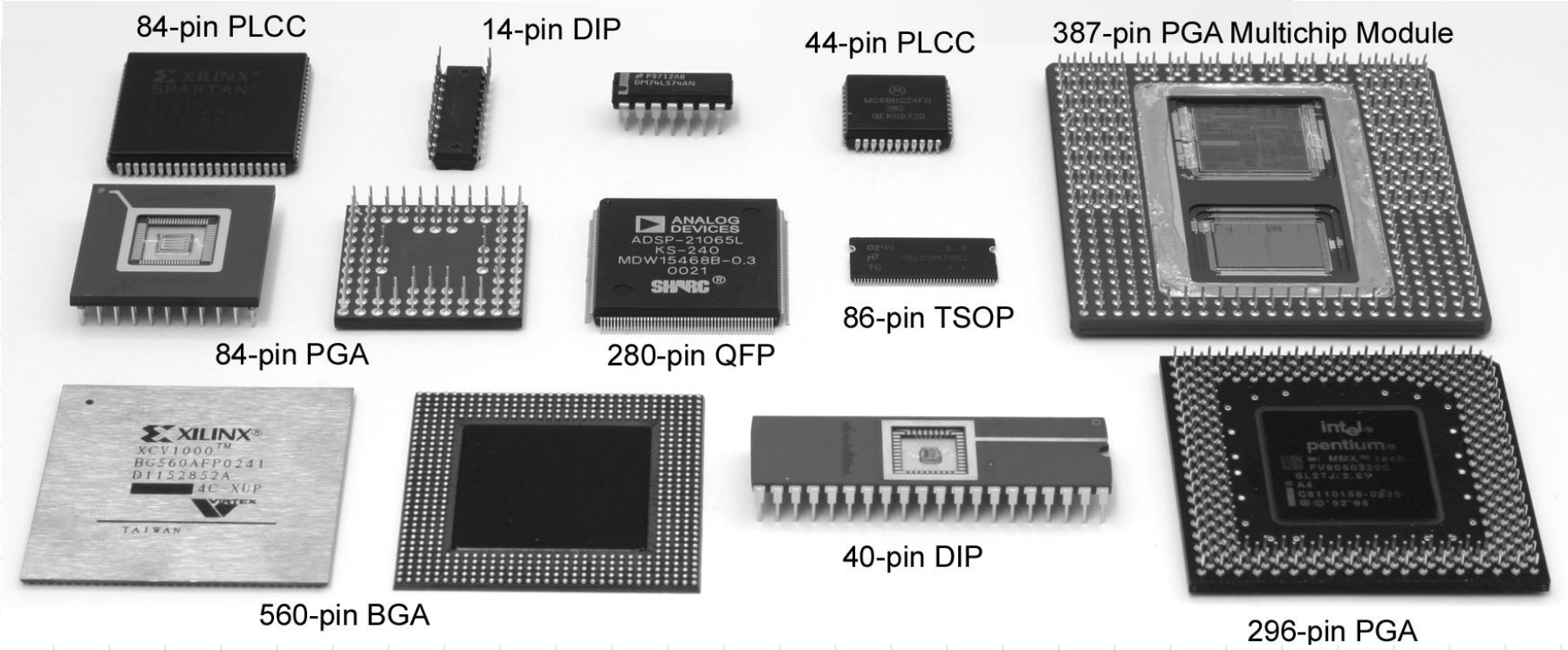
SMD

Quad Flat No-Lead Plastic Package (QFN)



SMD

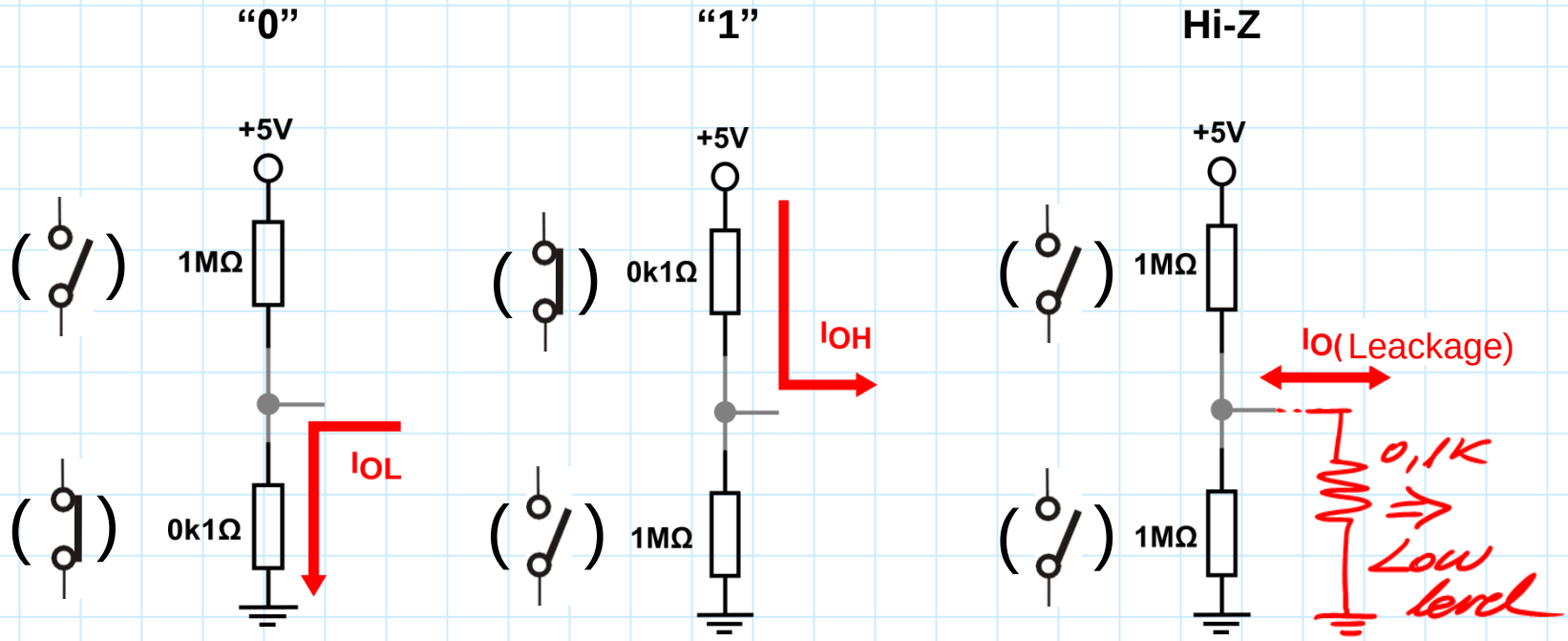
Introduction
Packages



Output types
State of one terminal

One output can have 3 different states: “0”, “1” and Hi-Z (or “Z”)

- Hi-Z: High impedance output; voltage established **without force**
- “0”, “1”: Low impedance outputs; voltage established **with force**



IBIS model. I/O Buffer Information Specification. Employed by manufacturers to offer a model of their circuits hiding its internal design (SPICE). I/V tables and V/t tables.

Output types

Output types in terms of possible output values:

"**0" and "1." Standard Output, Totem-Pole**.

↳ Standard TTL

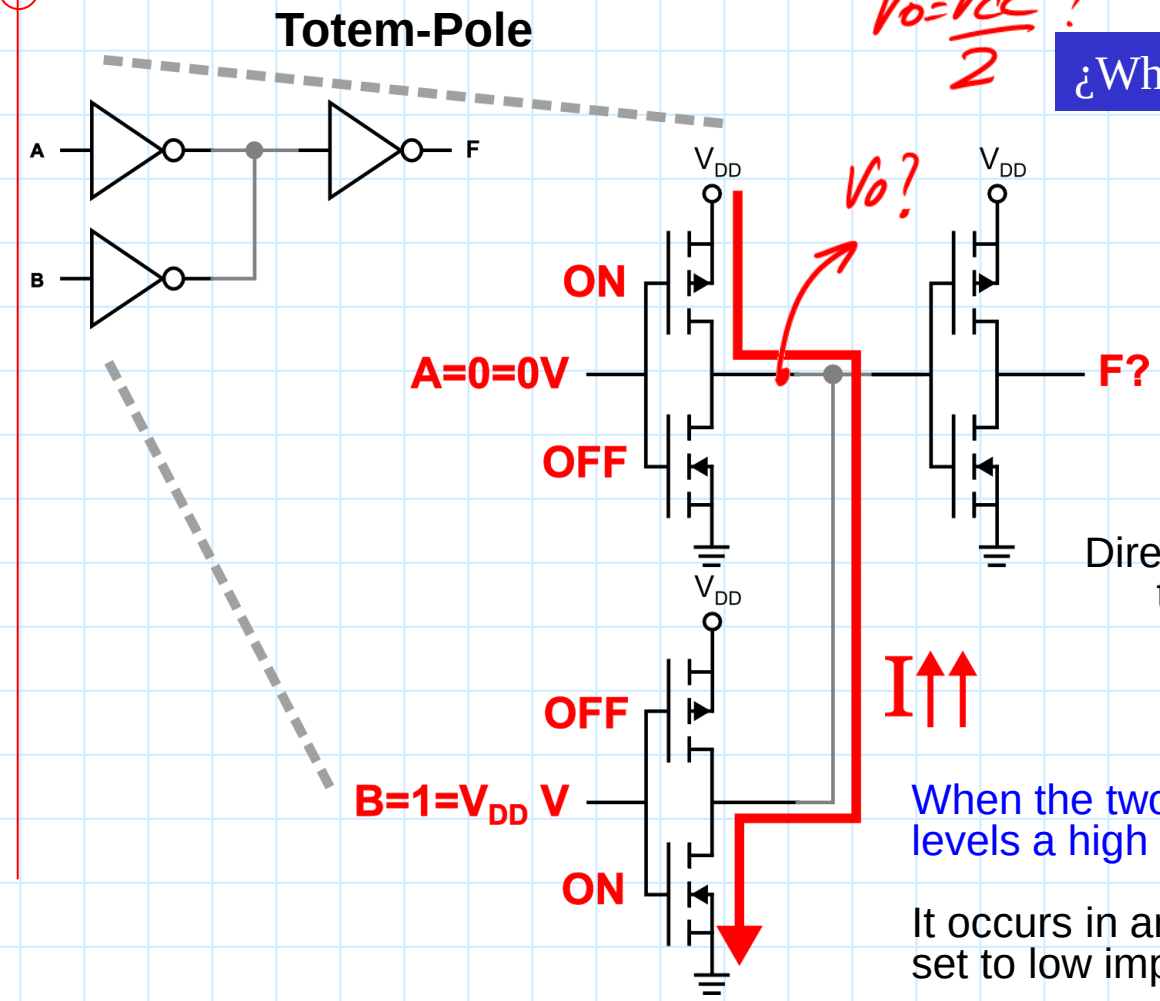
"0" and Z. Open collector and open drain.

Used in processor interrupt lines, serial communication buses such as I2C, lines of digital I/O in μControlers

"0", "1" and "Z". Tri-state outputs

Used on data buses in a single-processor computers, and on address buses in systems with multiple processors.

Output types. Totem-pole/Standard ("0" and "1")



$V_o = \frac{V_{cc}}{2}$? ⇒ undefined !

¿What value has F (0,1)?

A totem-pole output of a logic gate imposes "strongly" voltage value on the interconnection line.

Direct connection among outputs of two different gates not allowed

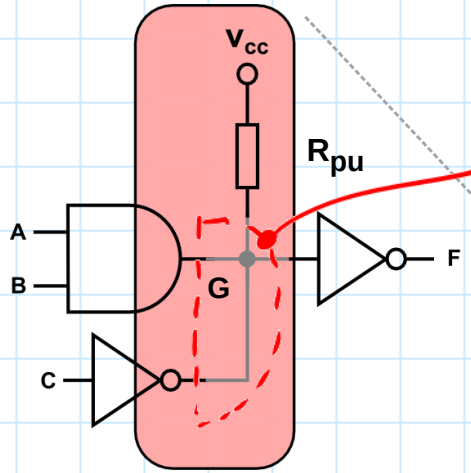
When the two outputs have different logic levels a high current path(s) are set!

It occurs in any technology whose outputs are set to low impedance.

Output types.
Open collector/drain ("0" and "Z")

1. Allows the wired-logic
2. It is necessary an external "Pull-up"-resistor (R_{pu}), to obtain the High level
3. The outputs implement a wired-AND

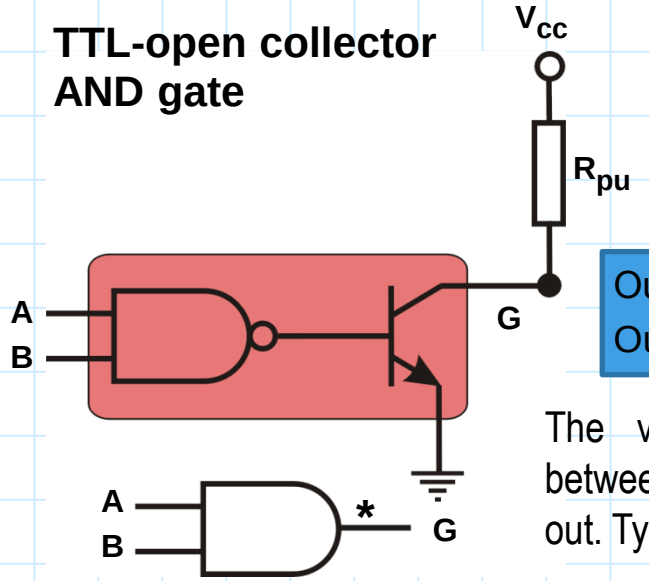
¿What is the value of F (1,0,1)?



$G = (A \cdot B) \cdot \overline{C}$

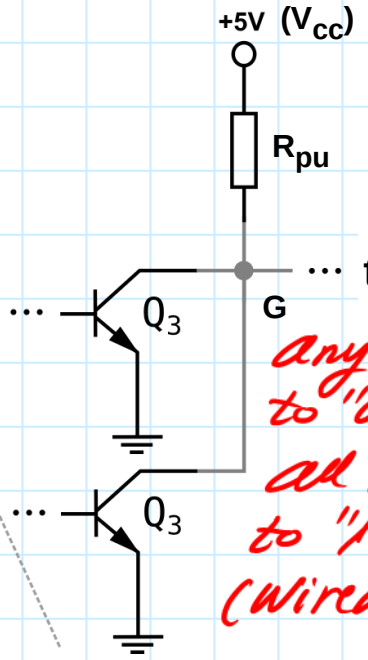
$F = \overline{G}$

TTL-open collector AND gate

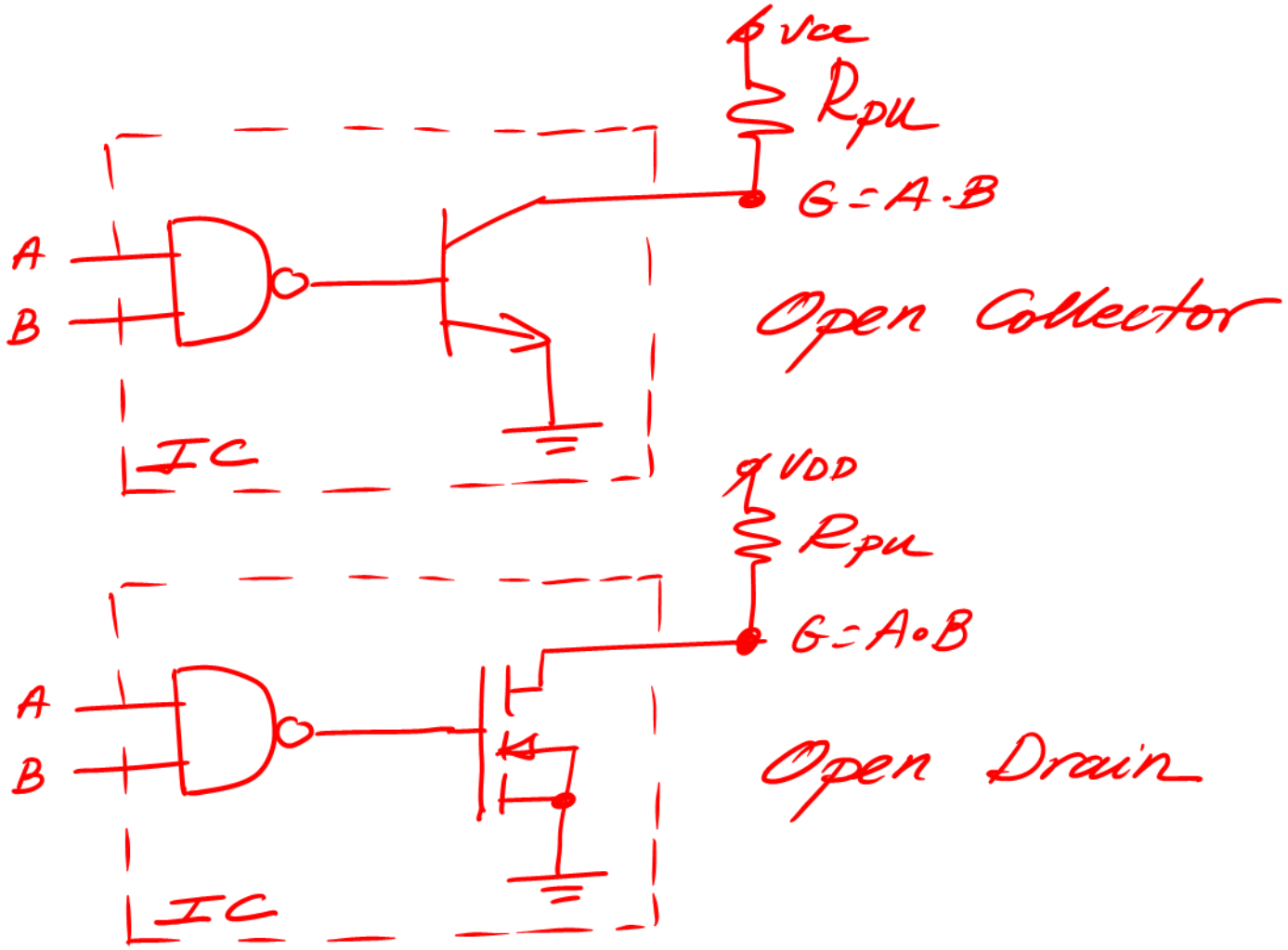


Output "0"→ Transistor ON
Output "1"→ Transistor OFF

The value of R_{pu} is a compromise between speed, power dissipation and fan out. Typical values of the order of kΩ.



any output to "0" ⇒ G=0
all outputs to "1" ⇒ G=1
(Wired-AND)



Rpu is outside IC (Integrated circuit)

Output types
Open collector/drain (“0” and Z)

Used in the interruption lines of computers

Open Collector/Drain outputs