5 Questions of THEORY (7.5 points) . Grading: PASS +1.5 pts., FAIL -0.37 pts, N.A: 0 pts.

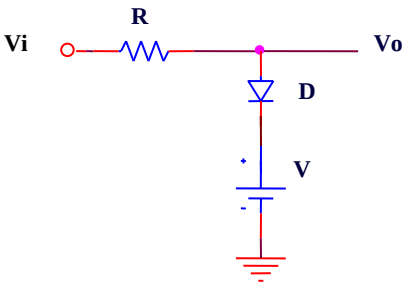
1. Signal the **FALSE** statement among the following related to the circuit with ideal diodes:

[A] If the diode conducts, it is necessary to know the voltage drop in resistor R, to obtain the value of the output voltage (Vo). ✗ Vo = V (fixed)

[B] If the input voltage (Vi) is negative, the diode does NOT conduct, and the output Vo is equal to Vi. ✓

[C] When the input voltage (Vi) is positive and greater than V, the output Vo is constant and independent of the value of Vi. ✓

[D] When the input voltage (Vi) is positive and greater than V, the value of the current through the diode increases as Vi increases. ✓



Vi ≤ V ⇒ D OFF, Vo = Vi
Vi > V ⇒ D ON; Vo = V

2. It is intended to design the adequate resistor R for the LEDs of figure to shine properly. Signal the **CORRECT** answer:

Data: V_{LED} = 1.5V; I_{LED} = 15mA.

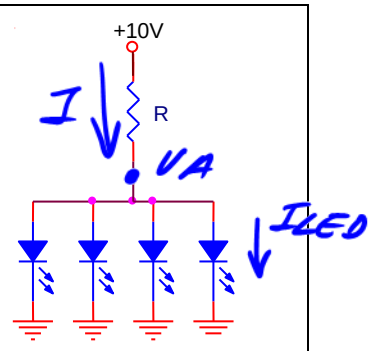
[A] R can have any value, greater or equal than R ≥ 0,142kΩ. ✗

[B] For example, R can be equal to R = 140Ω. ✓

[C] As the LEDs are in parallel, the voltage at the node (common anode) is 6V. ✗ $V_A = V_{LED} = 1.5V$

[D] None of the above is correct. ✗

$R = \frac{10 - V_{LED}}{4 I_{LED}} = 141.6\,\Omega$; 140 is correct



I = 4 ILED
VA = VLED

3. Given the clipping circuit of the figure, and taking into account a Vγ of 0.7V for the diodes, calculate the value of Vs when Ve = 4V and V1=3V.

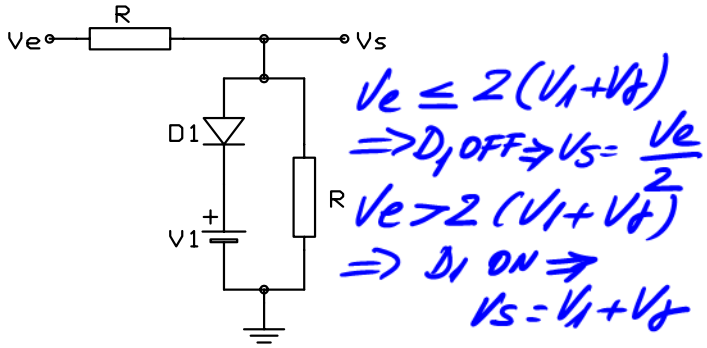
[A] 0V

[B] 1V

[C] 3,7V

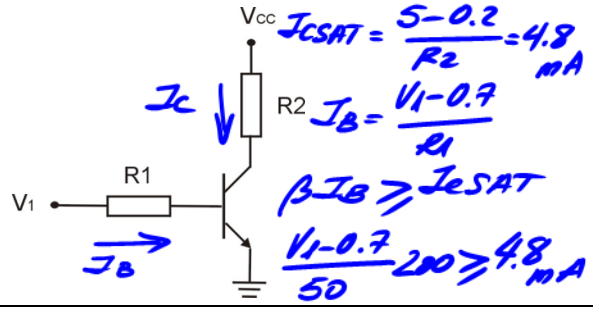
[D] 2V

Ve = 4 < 2(V1+Vγ) ⇒ Vs = Ve/2 = 2V



Ve ≤ 2(V1+Vγ) ⇒ D1 OFF ⇒ Vs = Ve/2
Ve > 2(V1+Vγ) ⇒ D1 ON ⇒ Vs = V1 + Vγ

4. The circuit of the figure is a logic inverter. What is the minimum value of the input voltage in order to reach the transistor the saturation region (V1MIN (SAT))?.

[A] $V1_{MIN(SAT)}$ = 5 V [B] $V1_{MIN(SAT)}$ = 2.7V [C] $V1_{MIN(SAT)}$ = 3.1V [D] $V1_{MIN(SAT)=}$ 1.9V	Data: β= 200 R1= 50k R2= 1k Vcc= 5V $V_{BE(ON)}$= 0.7, $V_{CE(SAT)}$ = 0.2V	

$I_{CSAT} = \frac{5-0.2}{R_2} = 4.8\ mA$

$I_B = \frac{V_1-0.7}{R_1}$

$\beta I_B \geq I_{CSAT}$

$\frac{V_1-0.7}{50} 200 \geq 4.8\ mA$

$V_1 \geq 0.7 + \frac{4.8}{4} = 1.9V$

5. For the transistor circuit of the figure, and for the data, the transistor curves and the load line shown, point out the **TRUE** answer:

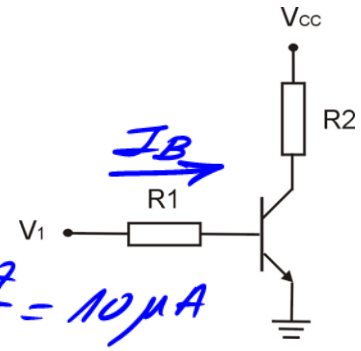
[A] Transistor is saturated, with I_B= 20uA, V_{CE}= $V_{CE(SAT)}$, I_C=7.8mA

[B] Transistor is in active region, with I_B= 10uA, V_{CE}=3V ,I_C= 5mA.

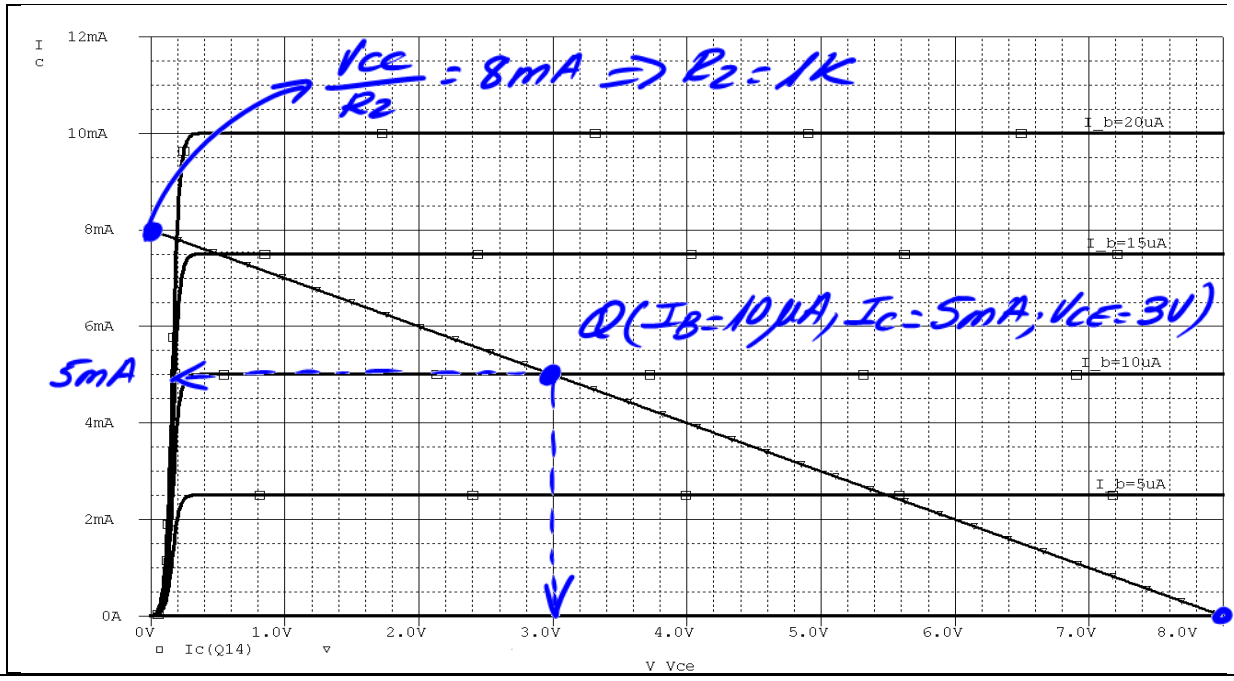
[C] Transistor is in active region, with I_B= 15uA, V_{CE}=0.5V , I_C=7.5 mA

[D] Transistor is in cut-off region.

Data:
$V_{BE(ON)}$=0.7V;
$V_{CE(SAT)}$=0.2V;
V1= 2.7V;
R1=200k;
β = 500



$I_B = \frac{2.7-0.7}{200} = 10\mu A$

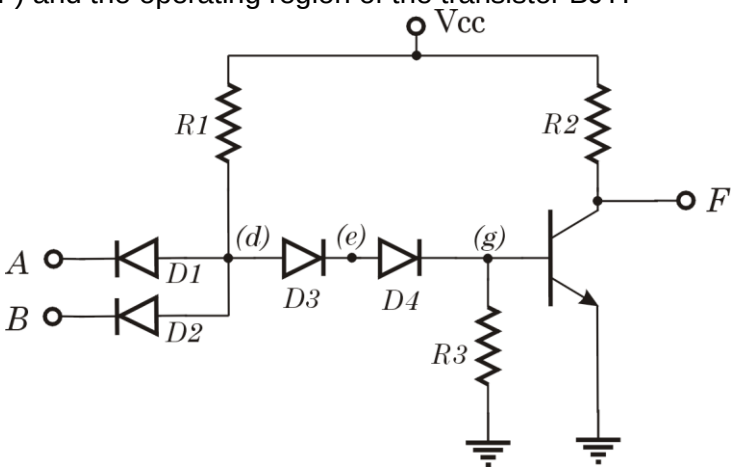


1 Problem (2.5 points).

The following figure represents a logic circuit of DTL (Diode Transistor Logic) logic family.
For each of the input combinations (A, B), justify the behavior of the circuit, completing the table below. That is, the logic value and voltage value (Volts) at node F, the voltages at nodes *d, e, and g*, as well as the status of the diodes (ON/OFF) and the operating region of the transistor BJT.

Data:

R1 = 3,4K
R2 = 4,8K
R3= 1,6K
V_{cc} = 5V
$V_{BE(ON)}$ = 0.7V; $V_{CE(SAT)}$ = 0.2V
β=200
V_γ = 0.7V

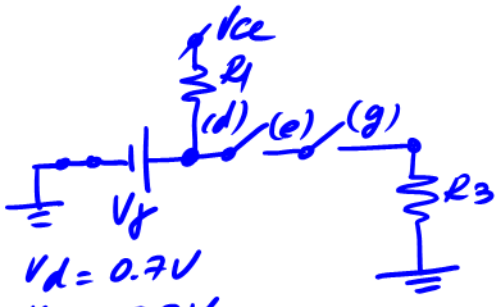


	V_A (Volts)	A	B	V_B (Volts)	D1	D2	D3	D4	V_d (Volts)	V_e (Volts)	V_g (Volts)	BJT	F	V_F (Volts)
1)	0V	0	0	0V	ON	ON	OFF	OFF	0.7	<0.7	0	OFF	1	5
	0V	0	1	5V	ON	OFF	OFF	OFF	0.7	<0.7	0	OFF	1	5
	5V	1	0	0V	OFF	ON	OFF	OFF	0.7	<0.7	0	OFF	1	5
2)	5V	1	1	5V	OFF	OFF	ON	ON	2.1	1.4	0.7	SAT	0	0.2

Obtain F in function of the inputs A and B:

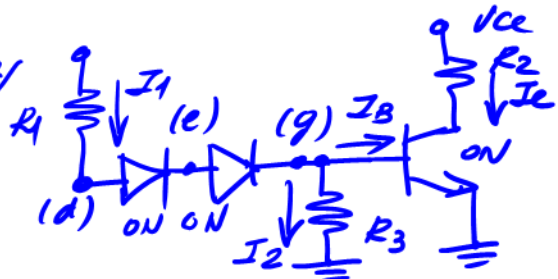
$$F(A,B) = \overline{A \cdot B}$$

1)



$V_d = 0.7V$
$V_e < 0.7V$
$V_g = 0$

2)



Assume SAT
$I_{C_{SAT}} = \frac{V_{CC} - 0.2}{R_2}$
$I_{C_{SAT}} = 1mA$

$V_g = V_{BE(ON)} = 0.7V$
$V_e = V_{BE(ON)} + V_\gamma = 1.4V$
$V_d = V_{BE(ON)} + 2V_\gamma = 2.1V$

$I_1 = \frac{5 - V_d}{R_1} = 0.853mA$
$I_2 = \frac{0.7}{R_3} = 0.437mA$

$I_B = I_1 - I_2 = 0.416mA$
$\beta I_B = 83.2mA > I_{CSAT} \Rightarrow$ Transistor SAT
$V_F = 0.2V = V_{CE(SAT)}$