Characteristic parameters of digital components

1. A TTL logic subfamily has the specifications listed in the table below. Calculate the noise margins at low level and at high level of the family.

V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
4 V	2 V	4.5 V	1 V

2. A CMOS logic family with a voltage supply of 3.3 V has the specifications listed in the table below. Calculate the noise margins at low level and at high level of the family.

V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
2.3 V	1 V	3.2 V	0.1 V

3. In the attached tables some of the electrical characteristics of two generic logic families A and B can be seen:

Afamily			
V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
2 V	0.8 V	2.4 V	0.4 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
40 μA	-1.6 mA	-400 μA	16 mA

Bfamily			
V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
2 V	0.8 V	2.7 V	0.5 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
20 μA	-0.36 mA	-400 μA	8 mA

From these tables, calculate:
a) The fan-out B ->A (number of inputs in A family components that can be connected to the output of a component of the family B).
b) The fan-out A ->B (number of inputs in B family components that can be connected to the output of a component of the family A).
The obtained values are, respectively:

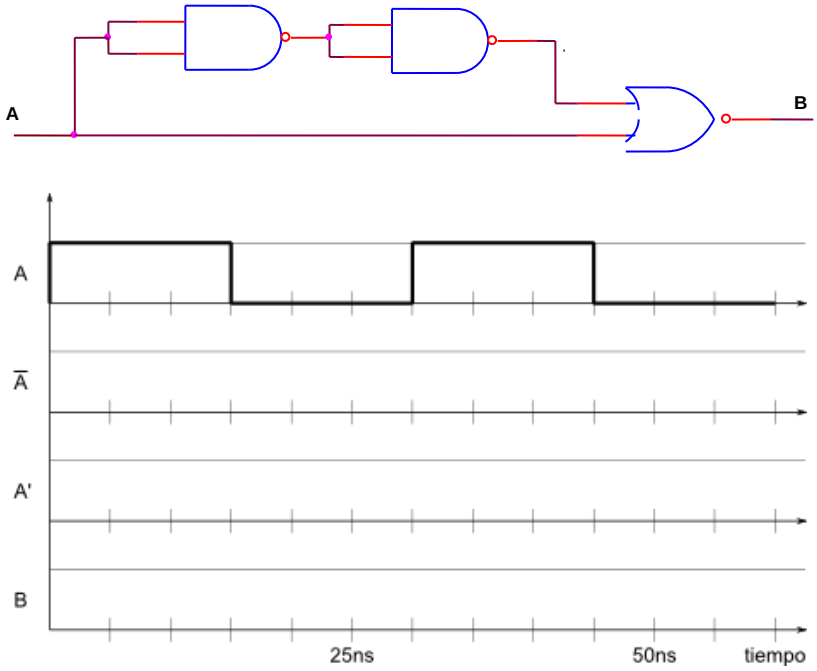
[A] 10 and 20.
[B] 5 and 20.
[C] 44 and 20.
[D] 2 and 1.

4. What is the *fan-out* of the logic family whose specifications are in the following table?

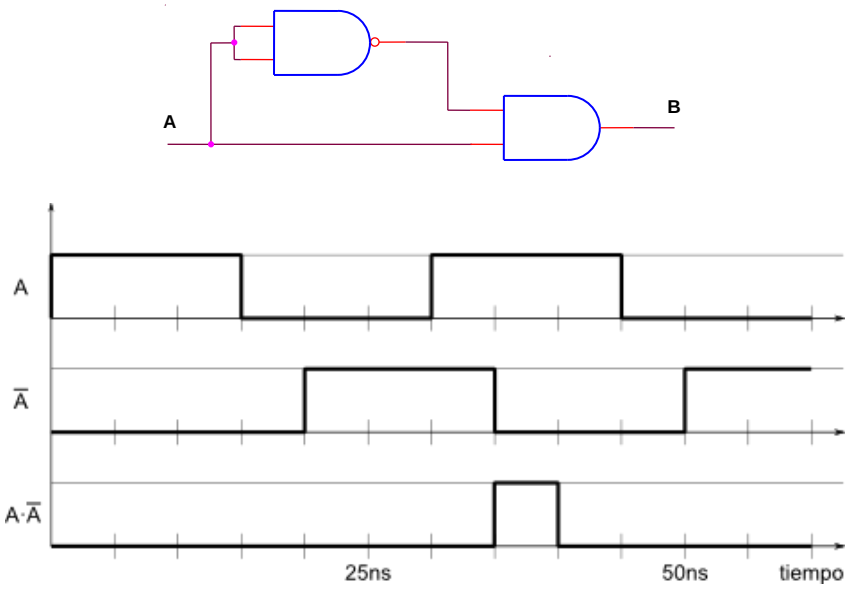
V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
2 V	0.8 V	2.7 V	0.5 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
20 μA	-0.36 mA	-400 μA	8 mA

[A] 10.
[B] 22.
[C] 20.
[D] The manufacturer recommends 50 to not cause excessive propagation times.

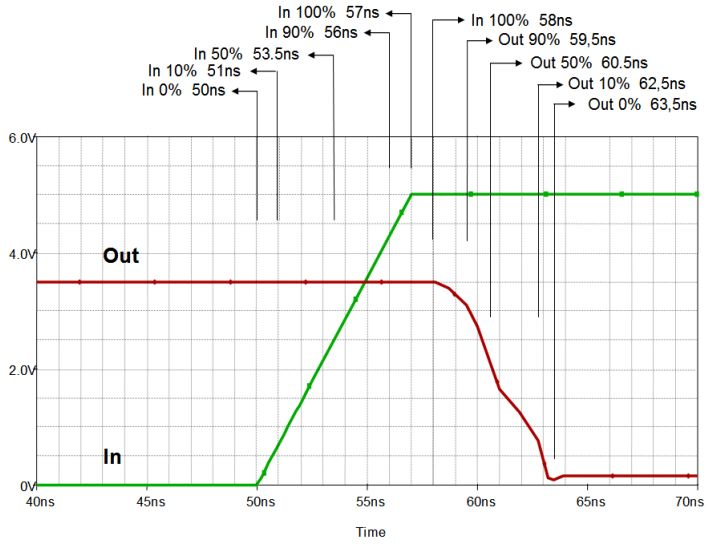
5. The gates (both types) of the circuit seen in the figure have a typical propagation delays t_{PLH} and t_{pHL} of 10 ns. Draw the chronogram at the output B if the signal at input A has the chronogram of the figure:



6. Taking into account the following chronogram, calculate the propagation delay t_{pd} of the gates.

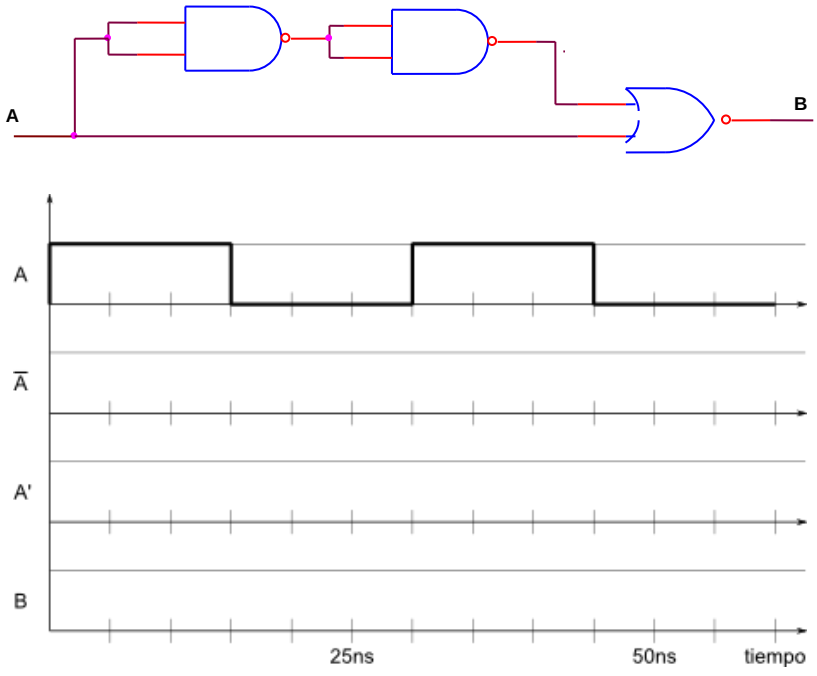


7. The following graph corresponds to the input and output of an inverter as a function of time, signal which of the following statements to is TRUE:

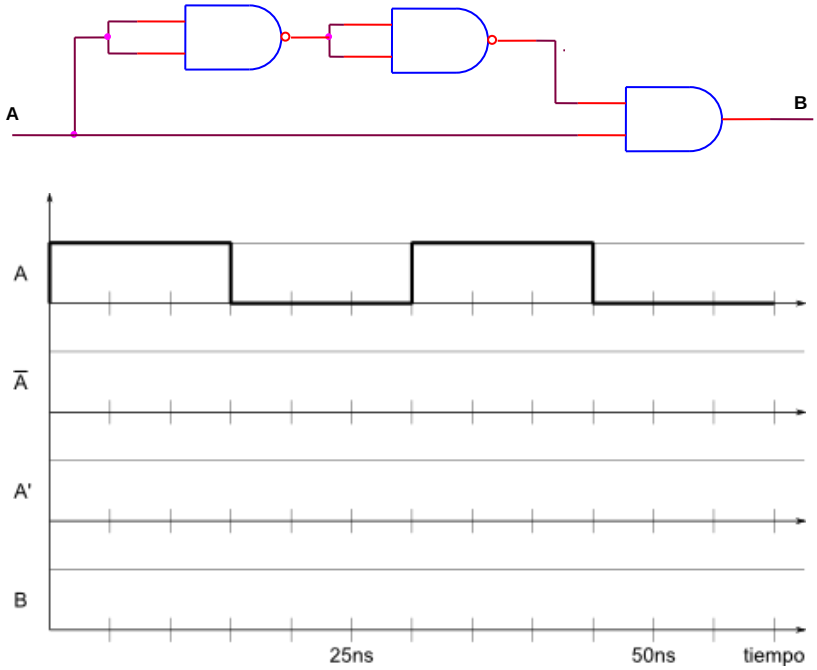


[A] The propagation delay $t_{pd(HL)}$ of inverter is 7 ns.
[B] The propagation delay $t_{pd(HL)}$ of inverter is 5.5 ns.
[C] The propagation delay t_{pd} of inverter is 13.5 ns.
[D] There are no enough data.

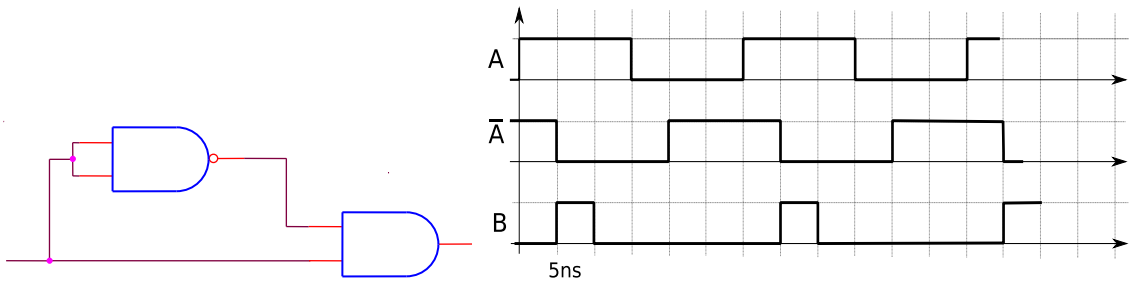
8. If the logic gates of the circuit of the figure are implemented with TTL technology, with I_{CCL} = 4.5 mA, and I_{CCH} = 0.5 mA, calculate the maximum static power consumed by the circuit given the input value A as indicated in the chronogram.



9. If the logic gates of the circuit of the figure are implemented with TTL technology, with I_{CCL} = 6 mA, and I_{CCH} = 2 mA, calculate the average static power consumed by the circuit given the input value A as indicated in the chronogram.



10. The figures show a digital circuit and its associated chronogram. A is the input and B the output. Each vertical mark corresponds to 5 ns. Choose the CORRECT statement:



Data:
V_{CC} = 5V; I_{CCL} = 6mA and I_{CCH} = 2mA. The average propagation delay of one gate is 5ns. Choose the correct statement:

[A] The average static power consumed by the NAND gate is 40mW.
[B] The average static power consumed by the AND gate is 20mW.
[C] The average static power consumed by the circuit is 46.67mW.
[D] To calculate the average static power consumed, we need to know the frequency of the input signal.

11. What is the PDP (power x delay product) of a TTL component with the following characteristics?: I_H (current consumption with output High) = 1 mA, I_L (current consumption with output Low) = 3.18 mA, t_{pHL} = 1.4 ns t_{PLH}= 3.2 ns. NOTE .- Consider as negligible the dynamic power consumption.

[A] 5.86 pJ
[B] 26.79 pJ
[C] 6.07 pJ
[D] 24.04 pJ

12. The datasheet of a given flip-flop indicates a minimum duration of clock signal of 30ns for HIGH level, and 37ns for LOW level. ¿What is the maximum frequency of the clock?

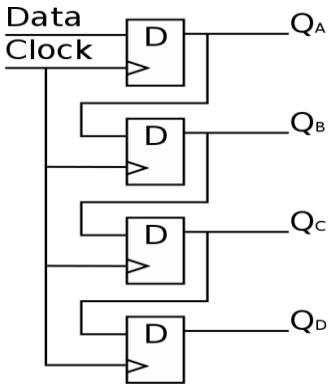
[A] 30MHz
[B] 15MHz
[C] 33.3MHz
[D] 15GHz

6. Which of the following statements related to the same logical family is FALSE?:

[A] $V_{OHmin}>=V_{IHmin}$ is always true.
[B] Noise margin is defined as NM=min(NML,NMH)
[C] Input currents are always positive, however, output currents are always negative.
[D] If the times of t_{su} (setup) and t_h (hold) are not met during the writing operation of a flip-flop, it may enter in metastable mode and do not correctly store correctly the input data.

14. We have a synchronous shift register designed with 4 flip flops. The timing parameters of each flip-flop, are: t_{su}=5ns, t_h=2ns, tp_{LH}=10ns, tp_{HL}=8ns. What is the maximum operating frequency? Does it depend on the number of flip-flops?

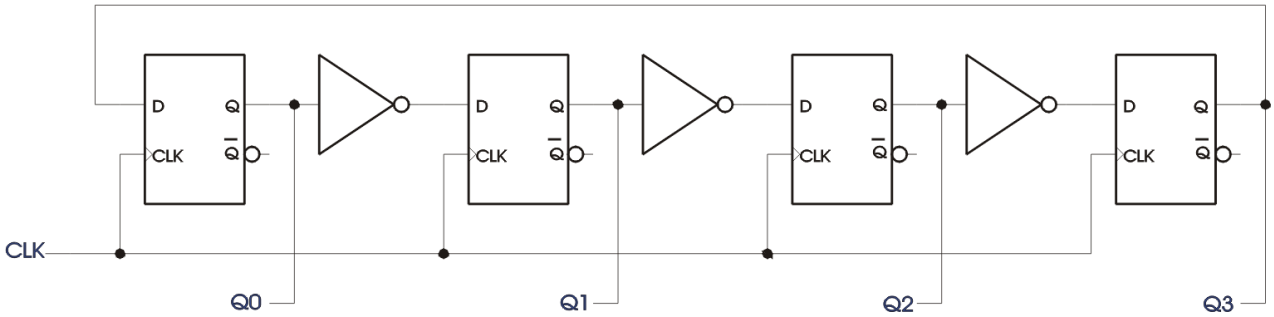
[A] 10MHz
[B] 100MHz
[C] 66.7MHz
[D] 62.5MHz



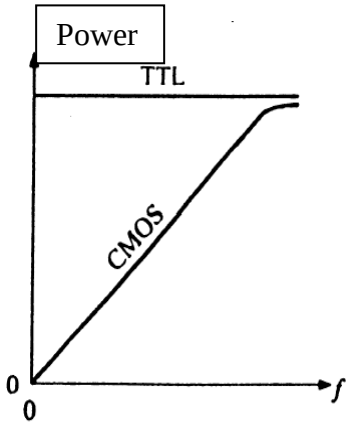
15. Given the following sequential circuit, implemented with D flip-flops, signal the CORRECT statement:

Temporal parameters: Biestables: (Set up: tsu = 10 ns, Hold: th = 5 ns, Delay: tpd(màx) = 20 ns), NOT gates: (Delay: tpd(máx) = 20 ns).

[A] The operating frequency should not exceed 20MHz.
[B] [B] The operating frequency must be greater than 15 MHz.
[C] The clock period must not exceed 50ns
[D] The circuit does not work properly because it has a very low hold time.



16. Indicate the FALSE statement related to the following figure:



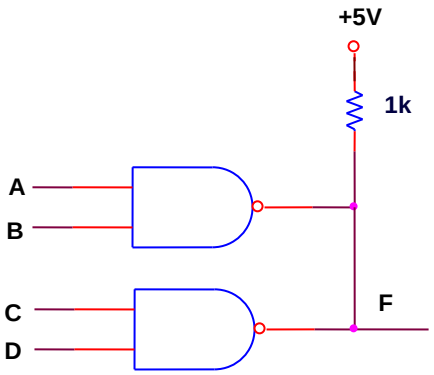
[A] The static power of CMOS digital circuits grows with frequency.
[B] TTL logic circuits present static consumption, independently of frequency.
[C] The CMOS logic circuits have a negligible static consumption.
[D] The dynamic consumption of the CMOS logic circuits is directly proportional to the frequency.

17. Indicate the CORRECT statement about some logical families:

[A] The pseudo-NMOS family is the most used in the VLSI chips due to its low consumption.
[B] The pseudo-NMOS family is a variant of the NMOS that substitutes the RD resistance for an NMOS transistor, in order to reduce the area of silicon.
[C] The LSTTL subfamily uses Schottky transistors to increase speed.
[D] The NMOS family presents static consumption when the output is '1'.

Special outputs

18. Given the circuit of the figure, implemented with TTL gates with open-collector outputs, indicate what of the following logical expressions of the function F is the CORRECT:



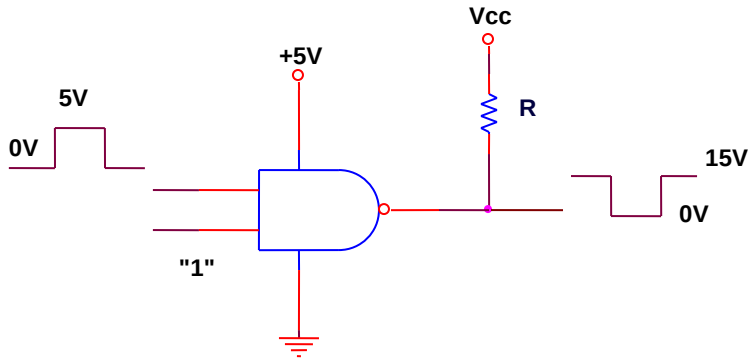
[E] $F = \overline{(A.B.C.D)}$

[F] $F = \overline{(A+B+C+D)}$

[G] $F = \overline{(A.B)} + \overline{(C.D)}$

[H] It is not possible to connect the gates as in the figure.

19. The circuit attached is to generate pulses of +15 V from +5 V pulses.If the gate has an open-collector output, with $I_{OH} \approx 0$ mA, $V_{OL} \approx 0$ V, $I_{OLmax} \approx 16$ mA, which of the following proposals for the pull-up circuit is valid?



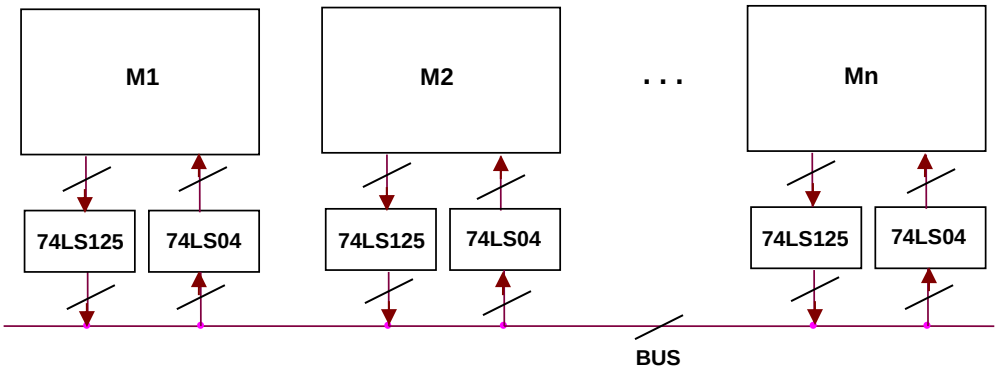
[A] V_{CC} = 5 V y R = 1 kΩ.

[B] V_{CC} = 15 V y R = 0.5 kΩ.

[C] V_{CC} = 15 V y R = 1 kΩ.

[D] This type of connection is not valid for an open-collector gate.

20. We have implemented a circuit using TTL components. The 74LS125 integrated circuit consists of tri-state output buffers. These buffers, when enabled, can sink 24 mA at low level, and to give 2.6 mA at high level. When disabled (high impedance state), the output has a leakage current of ± 20 μA (+ sign if the output is '1 ', - if the output is '0'). The figure shows a system designed with multiple modules connected to a bus, where each module consists of a 74LS125 buffer to provide information to bus and an inverter 74LS04 (with an input currents I_{IL} = -0.4 mA and I_{IH} = 20 μA) to receive information from the bus. What is the maximum number of modules that can be connected to the bus without exceeding the 74LS125specifications?

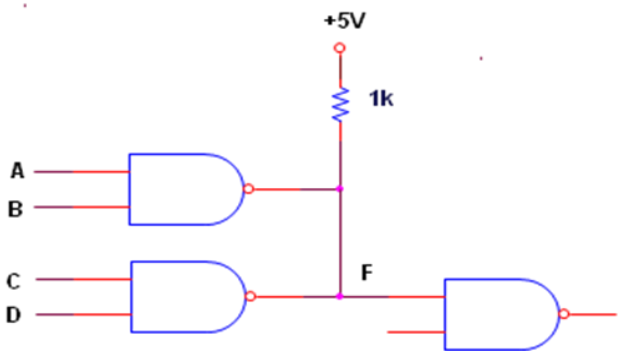


[A] 10.
[B] 57.
[C] 65.
[D] 30.

21. The circuit of the figure is composed of NAND gates with open collector outputs. From the specifications of the table (voltages and currents) and for the inputs (A=4V, B=0.2V, C=4.5V, D=0.6V), CALCUATE the voltage in F.

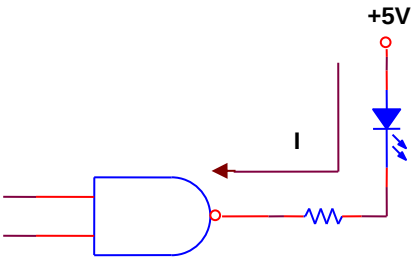
V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
2.5 V	0.8 V	3.0 V	0.5 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
600 μA	-0.36 mA	200 μA	7 mA

[A] F=0.5V
[B] F=3.0V
[C] F=4.0V
[D] F=5.0V



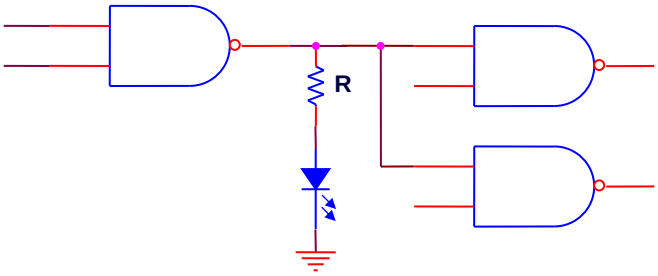
Powering LEDs

22. We want that the LED of the following circuit has the maximum possible brightness. Taking into account the values of the parameters of logic gate in the table below, and Vγ (LED) = 2.2 V, calculate the value of R so that the logic gate operates within specifications.



V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
2.5 V	0.8 V	3.0 V	0.5 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
20 μA	-0.36 mA	-100 μA	7 mA

23. The LED of figure with a resistor R of 50 Ω, is inserted in the digital circuit to display an internal variable. Taking into account the specifications of the logic gates as detailed in the following table, and $V\gamma_{(LED)}$=1.8V, a) Is this connection correct? If it is correct, how many inputs can be connected in total? If not, what is the value of R which allows connecting up to four inputs?



V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
2.5V	0.8 V	2.3 V	0.2 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
1 mA	-3.5 mA	-16 mA	25 mA

24. To display an internal variable of a digital circuit is introduced a LED with a resistor Rpu in the circuit of the figure. Calculate the Rpu resistor. Consider these data:

Circuit:

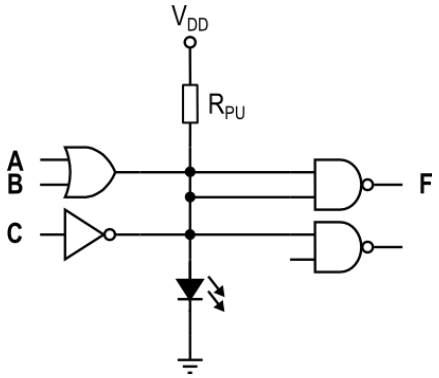
V_{DD}=5V

Gates:

Output type: Open collector for OR and NOT.
Voltages: V_{IHmin}=1.5V, V_{ILmax}=0.8V, V_{OHmin}=3V, V_{OLmax}=0.2V
Currents: I_{IHmax}=1mA, I_{ILmax}=-3.5mA, $I_{OHmax(leackage)}$=0.5mA, I_{OLmax}=35mA

LED:

$V\gamma_{(LED)}$ = 1.8 V
Current for acorrect illumination I_{LED}=10mA.



Interconnection of logic families

25. We want to connect the outputs of 2 standard components of a logic family with a voltage supply of 5V, to 3 inputs of components of the same family. The specifications of the family are shown in the following table:

V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
2 V	0.8 V	2.4 V	0.4 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
40 μA	-1.6 mA	0.25 mA	16 mA

To make correctly this connection:
[A] We do not need to add anything more.
[B] It should be added a pull-up resistor between the output and the voltage supply, with a range of possible values between 0.4 kΩ and 13.6 kΩ.
[C] It cannot be done the connection of the outputs, since it would cause an undetermined voltage and the degradation of the output transistors.
[D] It should be added a pull-up resistor between the output and the voltage supply, with a range of possible values between 10 kΩ and 20.5 kΩ.

26. We want to connect the outputs of 2 components with open-collector outputs of a logic family with a voltage supply of 5V, to 3 inputs of components of the same family. The specifications of the family are shown in the following table (taking into account that I_{OHmax} = 100 μA for the open-collector components):

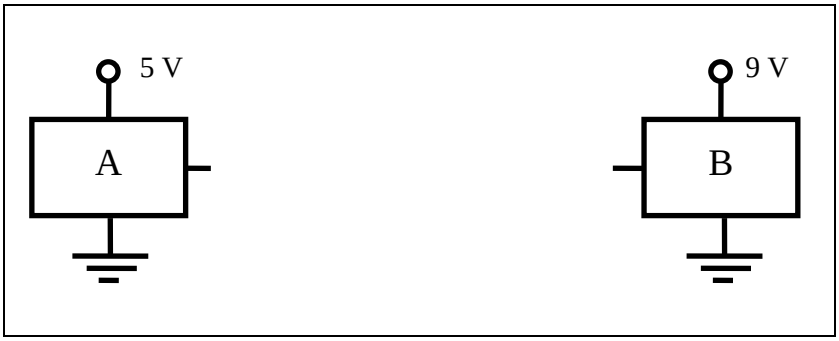
V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
2 V	0.8 V	2.4 V	0.4 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
40 μA	-1.6 mA	0.25 mA	16 mA

To make correctly this connection:
[A] We do not need to add anything more.
[B] It should be added a pull-up resistor between the output and the voltage supply, with a range of possible values between 0.41 kΩ and 8.12 kΩ.
[C] It cannot be done the connection of the outputs, since it would cause an undetermined voltage and the degradation of the output transistors.
[D] It should be added a pull-up resistor between the output and the voltage supply, with a range of possible values between 0.41kΩ and 11.82 kΩ.

27. Make the connection of the components of the figure from the specifications of the families A and B in the attached tables. In case you have to add a component, it is not necessary to do the calculations.

Afamily			
V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
2 V	0.8 V	2.4 V	0.4 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
40 μA	-1.6 mA	-400 μA	16 mA

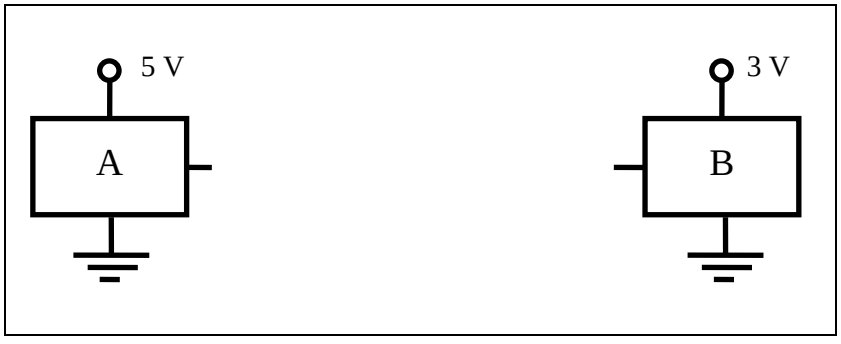
Bfamily			
V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
6.3 V	2.7 V	8.9 V	0.1 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
20 pA	-20 pA	-0.5 mA	0.5 mA



28. Make the connection of the components of the figure from the specifications of the families A and B in the attached tables. In case you have to add a component, it is not necessary to do the calculations.

Afamily			
V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
2 V	0.8 V	2.4 V	0.4 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
40 μA	-1.6 mA	-400 μA	16 mA

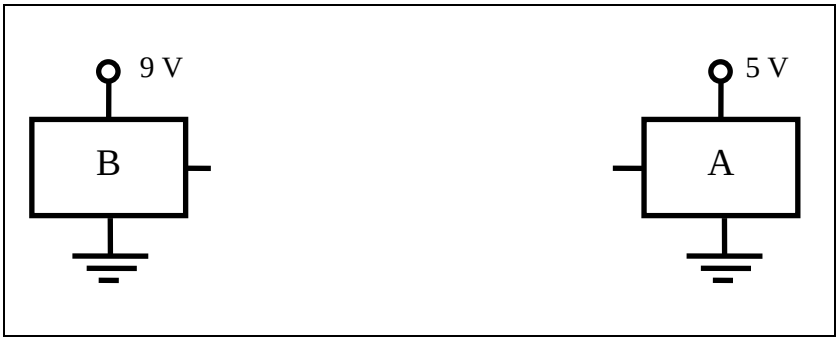
Bfamily			
V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
2.1 V	0.9 V	2.9 V	0.1 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
1 pA	-1 pA	-0.5 mA	0.5 mA



29. Make the connection of the components of the figure from the specifications of the families A and B in the attached tables. In case you have to add a component, it is not necessary to do the calculations.

Afamily			
V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
2 V	0.8 V	2.4 V	0.4 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
40 μA	-1.6 mA	-400 μA	16 mA

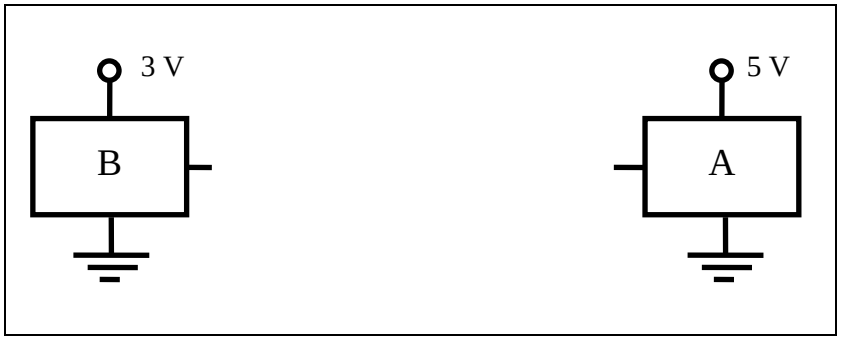
Bfamily			
V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
6.3 V	2.7 V	8.9 V	0.1 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
20 pA	-20 pA	-0.5 mA	0.5 mA



30. Make the connection of the components of the figure from the specifications of the families A and B in the attached tables. In case you have to add a component, it is not necessary to do the calculations.

Afamily			
V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
2 V	0.8 V	2.4 V	0.4 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
40 μA	-1.6 mA	-400 μA	16 mA

Bfamily			
V_{IHmin}	V_{ILmax}	V_{OHmin}	V_{OLmax}
2.1 V	0.9 V	2.9 V	0.1 V
I_{IHmax}	I_{ILmax}	I_{OHmax}	I_{OLmax}
1 pA	-1 pA	-0.5 mA	0.5 mA



31. We want to connect a TTL open collector output with an input of a CMOS logic circuit powered to + 9V. Indicate the CORRECT answer:

Family A (TTL open collector)			Family B (CMOS +9V)			
V_{OLmax}	$I_{OHmax\ (fugas)}$	I_{OLmax}	V_{IHmin}	V_{ILmax}	I_{IHmax}	I_{ILmax}
0.4 V	100 μA	16 mA	6.3 V	2.7 V	0.1 μA	-0.1 μA

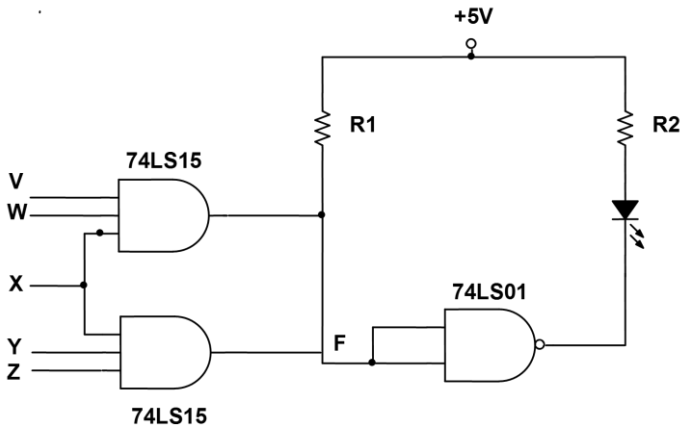
[A] It is necessary to connect a pull-up resistor between the output and the power supply. of + 9V. The value of the resistance must be between 0.54KΩ and 26.97KΩ.

[B] We can connect both famílies directly.

[C] It is necessary to insert a TTL buffer to make the current compatible at low level.

[D] It is necessary to connect a pull-up resistor between the output and the power supply. of + 9V. The value of the resistance must be between 2.1KΩ y 41.4KΩ.

32. The following circuit uses logic gates with open collector output (within the 74LS01 and 74LS15 integrated circuits) to implement a "wired AND", and to activate the LED output.



A. Write a logical expression for the function implemented by the circuit in the signal F.
B. When F = '1 ', Is the LED on or off?.
C. Design R2, assuming that the current through the LED when it lights is $I_{LED\ (on)}= I_{OLmax}$ and $V_{LED\ (on)}= 1.2V$.
D. Taking into account the following features for 74LS01 and 74LS15 integrated circuits, calculate the range of values allowed for R1:

Vcc	**V_{IHmin}**	**V_{ILmax}**	**V_{OLmax}**	**I_{IHmax}**	**I_{OHmax} (Leakage)**	**I_{OLmax}**	**I_{ILmax}**
5 V	2.5V	0.8 V	0.5 V	20 μA	100 μA	7 mA	-0.36 mA