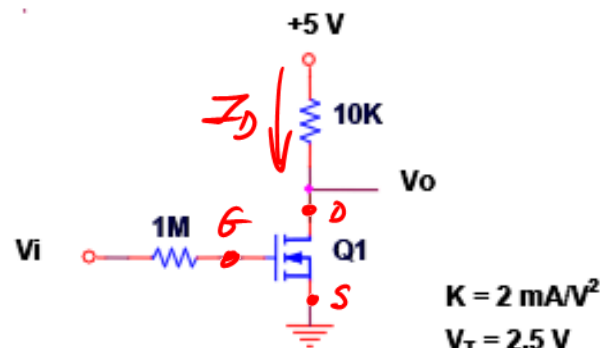


UNIT 2. MOSFETS: OPERATING POINT

5.10 From the following NMOS inverter circuit: Calculate the limit values of the input voltage V_i to make the transistor working in switching mode: V_i between cut-off and saturation and V_i between saturation and ohmic region. Note: in this second point, we recommend using the saturation equation.



a) Low level (cut off - saturation)

$$V_{GS} = V_i \leq V_T = 2.5V \Rightarrow Q1 \text{ OFF}$$

$$V_o = 5V$$

b) High level (saturation - ohmic)

In limit \rightarrow

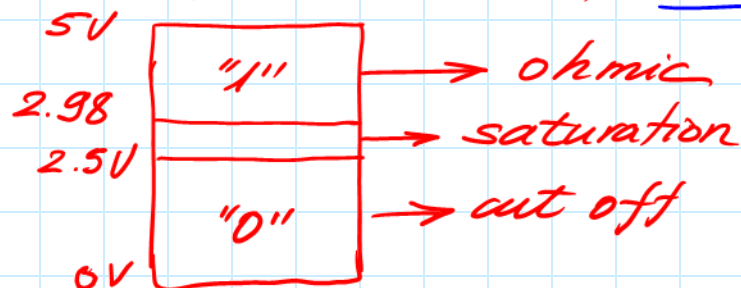
$$\left. \begin{array}{l} a) V_{DS} = V_{GS} - V_T \\ b) I_{DS} = K (V_{GS} - V_T)^2 = 2 V_{DS}^2 \\ c) I_{DS} = \frac{5 - V_{DS}}{10} \end{array} \right\} 2 V_{DS}^2 = \frac{5 - V_{DS}}{10}$$

$$20 V_{DS}^2 + V_{DS} - 5 = 0$$

$$V_{DS} = \frac{-1 \pm \sqrt{1 + 400}}{40} = \frac{-1 \pm 20.02}{40}$$

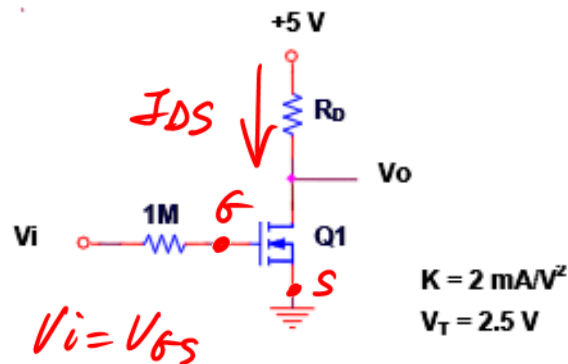
$\nearrow 0.48V$
 $\searrow -0.53V \times$

$$V_{DS} = 0.48V = V_{GS} - V_T; \quad V_{GS} = V_i = 0.48 + V_T = \underline{2.98V}$$



UNIT 2. MOSFETS: OPERATING POINT

5.11 From the following NMOS inverter. Obtain the value of R_D , in order to reach the ohmic region from saturation region, when $V_i = 4V$. Note: We recommend using the saturation equation.



ohmic region $V_{DS} \leq V_{GS} - V_T$ \rightarrow in limit

In limit $\rightarrow \begin{cases} V_{DS} = V_{GS} - V_T & (1) \\ I_{DS} = K(V_{GS} - V_T)^2 & (2) \end{cases}$

output loop $\rightarrow I_{DS} = \frac{5 - V_{DS}}{R_D} \quad (3)$

(2) $I_{DS} = K(V_i - V_T)^2 = 2(4 - 2.5)^2 = 4.5 \text{ mA}$

(1) (3) $R_D = \frac{5 - V_{DS}}{I_{DS}} = \frac{5 - (V_{GS} - V_T)}{I_{DS}} = \frac{5 - (4 - 2.5)}{4.5} = \frac{3.5}{4.5} = \underline{\underline{777.7 \Omega}}$

$R_D > 777.7 \Omega \Rightarrow Q_1$ in OHMIC region

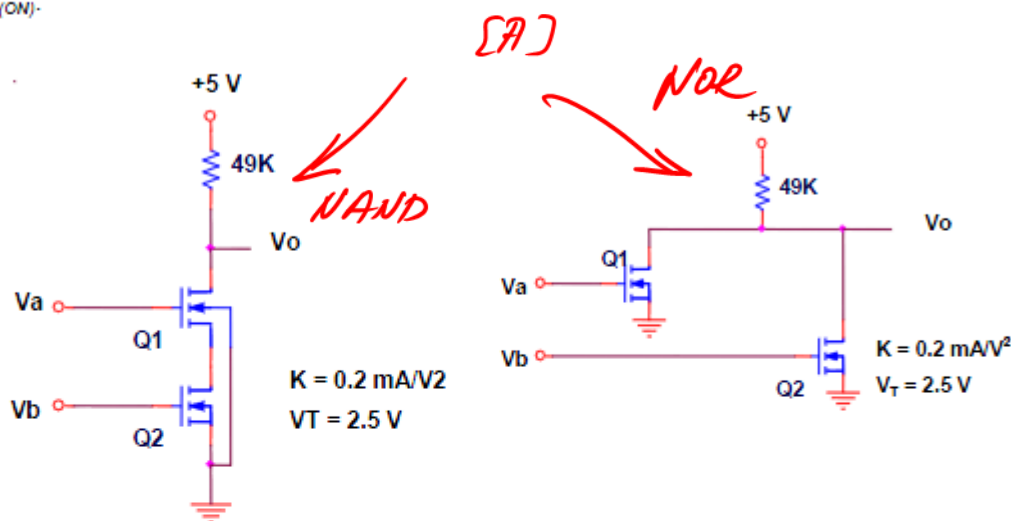
UNIT 2. MOSFETS: OPERATING POINT

5.5 The following circuits are two-input NMOS gates.

Note: For the left circuit, do the calculations for one or two transistors conducting. Use the simplified expression for the ohmic region $R_{DS(ON)}$.

[A] ¿Which type of logic gates are?

[B] Obtain the V_o voltage for each output state. Assume 5V as high input level and 0V as low level.



In addition to theoretical analysis, simulate the circuit using PSpice. Use the parts: VDC, EGND, r, MbreakN3. Double click on MOSFET symbol and fix: $L = 1\mu$, $W = 2\mu$. To specify V_T and K , see exercise 3.1. V_o is just a label, do not place any VDC at that point.

We will replace the DC source VDC of inputs (V_a y V_b) for a source of type VPULSE. Specify the following parameters:

$V1 = 0\text{V}$ (low level)

$V2 = 5\text{V}$ (high level)

$TD = 10\text{n}$ for V_a and 30n for V_b (initial delay time)

$TR = 2\text{n}$ (rise time)

$TF = 2\text{n}$ (fall time)

$PW = 40\text{n}$ (high level duration-pulse width)

$PER = 100\text{n}$ (period time)

Do not modify the rest of parameters

Put two separate voltage markers (Voltage / Level Marker) at the input and the output.

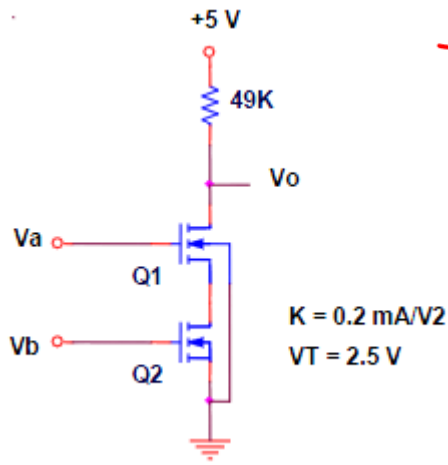
Select Transient simulation type and disable DC Sweep, using the Analysis / Setup / Transient menu.

In Transient window, indicate Print step = 1n , Final time = 120n .

Simulate and observe all combinations of input and output values.

This type of simulation is particularly suitable for digital gates, which have inputs and outputs. It is also highly recommended to simulate other circuits of this set of exercises. See Laboratory 5 as reference.

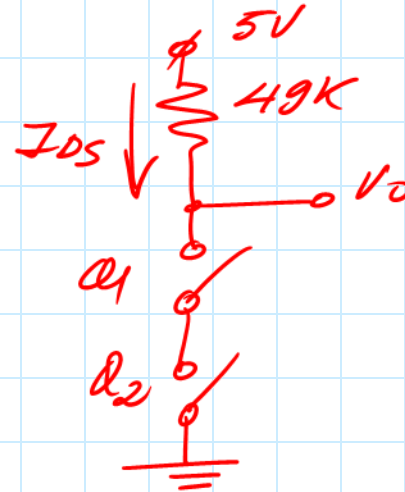
UNIT 2. MOSFETS: OPERATING POINT



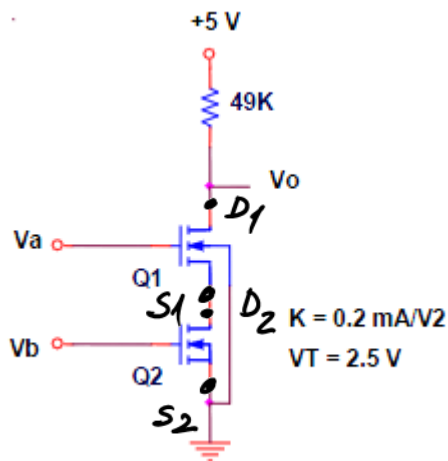
$a) \left\{ \begin{array}{l} V_A = V_B = 0 \\ V_A = 0; V_B = 1 \\ V_A = 1; V_B = 0 \end{array} \right\} \begin{array}{l} Q1 \text{ OFF} \\ Q2 \text{ OFF} \end{array}$

~~X~~

$I_{DS} = 0 \Rightarrow V_o = 5\text{ V}$



UNIT 2. MOSFETS: OPERATING POINT

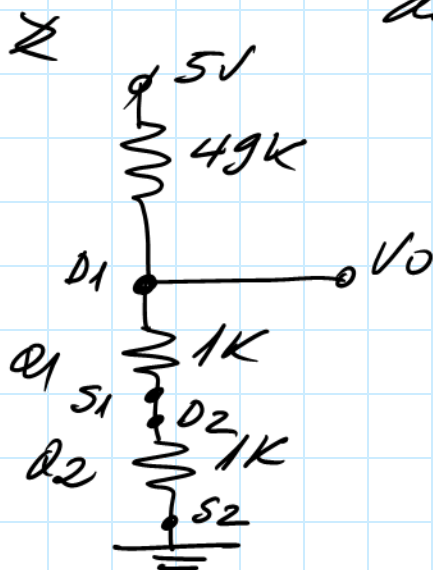


$$b) V_A = V_B = 5V > V_T \Rightarrow \begin{cases} Q_1 \text{ ON} \\ Q_2 \text{ ON} \end{cases}$$

assume linear region \Rightarrow

$$R_{ON} \approx \frac{1}{2K(V_{GS} - V_T)} = \frac{1}{2 \cdot 0.2(5 - 2.5)} = 1K$$

(assuming both $V_{GS} = 5V$, $R_{ON1} = R_{ON2} = R_{ON}$ actually $R_{ON1} > R_{ON2}$, as $V_{GS1} < V_{GS2}$, as S_2 is connected to ground, and S_1 has some voltage. However, we can neglect this difference).

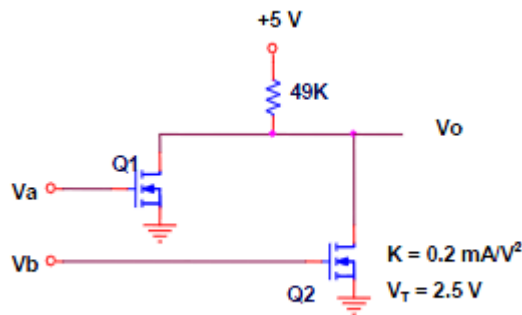


$$V_O = 5 \frac{2}{49 + 2} = 0.20V$$

$$V_{DS1} = V_{DS2} = \frac{V_O}{2} = 0.1V; \text{ In both cases:}$$

$V_{DS} < V_{GS} - V_T = 2.5V \Rightarrow$ OK in linear region.

UNIT 2. MOSFETS: OPERATING POINT

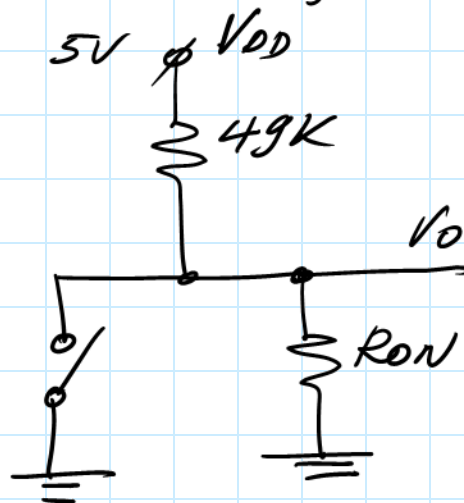


a) $V_A = V_B = 0 < V_T \Rightarrow \begin{cases} Q_1 \text{ OFF} \\ Q_2 \text{ OFF} \end{cases}$

$I = 0$

$V_O = 5V$

b) $V_A = 1; V_B = 0$ or $V_A = 0; V_B = 1$ } one trans. ON } \Rightarrow Assume linear region
 one " OFF }



$$R_{ON} = \frac{1}{2K(V_{GS} - V_T)} = \frac{1}{2 \cdot 0.2(5 - 2.5)}$$

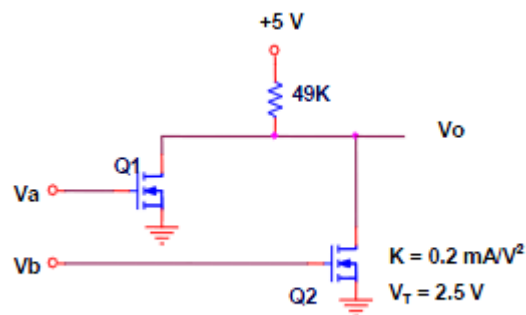
$$R_{ON} = 1K \Rightarrow$$

$$V_O = 5 \frac{R_{ON}}{49 + R_{ON}} = 5 \frac{1}{50}$$

$$V_O = 0.1V$$

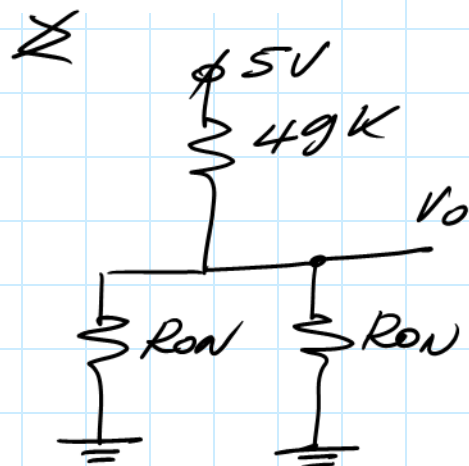
$$V_O = V_{DS} < V_{GS} - V_T = 2.5V \Rightarrow \text{OK linear region}$$

UNIT 2. MOSFETS: OPERATING POINT



$$c) \quad V_A = V_B = 1 \Rightarrow \begin{cases} Q_1 \text{ ON} \\ Q_2 \text{ ON} \end{cases}$$

$R_{ON1} = R_{ON2} = 1K$ (see previous paragraphs)



$$V_o = 5 \frac{R_{ON}/2}{49 + R_{ON}/2} = 5 \frac{0.5}{49 + 0.5}$$

$$V_o = 0.05V$$

Summary:

$V_a(V)$	$V_b(V)$	$V_o(V)$
0	0	5V
0	5	0.1V
5	0	0.1V
5	5	0.05V

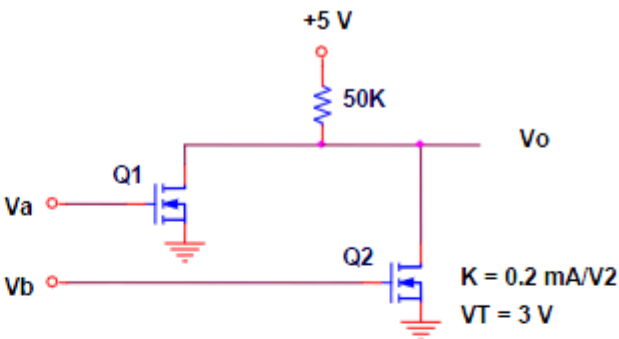
UNIT 2. MOSFETS: OPERATING POINT

6.3The circuit of the figure is a simple MOSFET transistor-based logic gate. It is requested:

Data:

Sat: $I_{DS} = K (V_{GS} - V_T)^2$

Ohmic: $I_{DS} = 2K (V_{GS} - V_T)V_{DS}$



[A] Calculate the value of the output voltage Vo when Va = 3.5V and Vb = 0.5V, and the state of each transistor (Justify the answer).

Vo =	
M1 region:	
M2 region:	

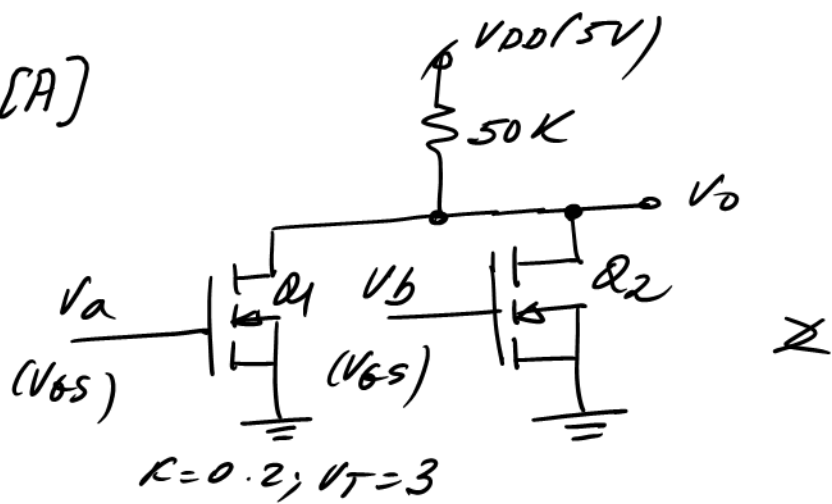
[B] If Vb = 0V and the output Vo = 0.2V, what is the value of the input voltage that produces this output voltage? (Assume transistor M1 in ohmic region, and calculate the equivalent resistance value of transistor RDS(ON))

RDS(ON) =	
Va =	

[C] As already mentioned, the circuit corresponds to a logic gate. Indicate the logic function of the output Vo in terms of inputs Va and Vb, and the logic family to which it belongs..

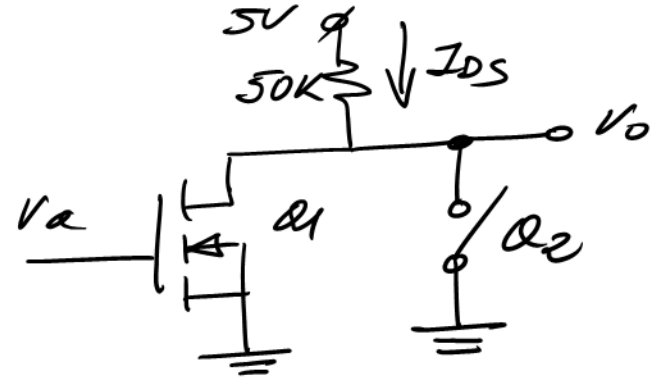
Logic function:	
Logic Family: (TTL, CMOS, NMOS o PMOS)	

[A]



$$V_a = 3.5V > V_T \Rightarrow Q_1 \text{ ON}$$

$$V_b = 0.5V < V_T \Rightarrow Q_2 \text{ OFF}$$



Assume Q_1 saturated

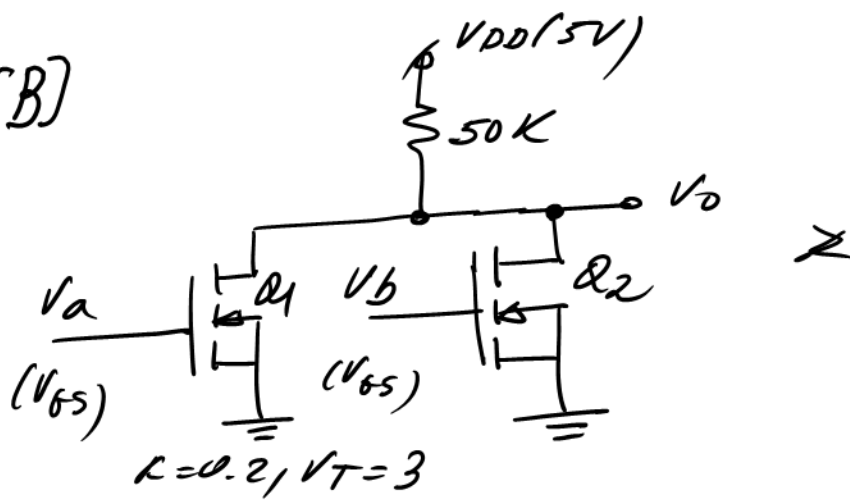
a) $\underline{I_{DS} = K(V_{GS} - V_T)^2 = 0 = 0.2(3.5 - 3)^2 = 0.05 \text{ mA}}$

b) $\underline{V_o = V_{DS} = V_{DD} - 50I_{DS} = 5 - 50 \cdot 0.05 = 2.5V}$

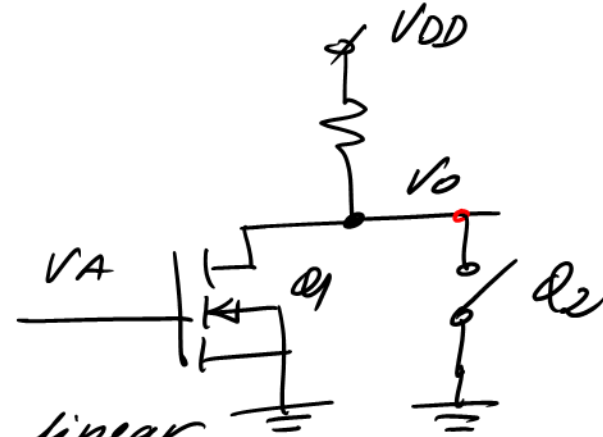
$V_{DS} > V_{GS} - V_T = 0.5V \Rightarrow \text{Saturated}$

$V_o = 2.5V$
 $Q_1 \rightarrow \text{saturated}$
 $Q_2 \rightarrow \text{cut-off}$

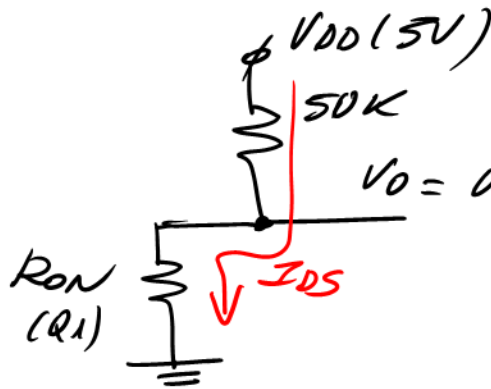
[B]



$$V_o = 0 \Rightarrow Q_2 \text{ OFF}$$



$V_o = 0.2 = V_{DS} \Rightarrow Q_1 \text{ ON, assume linear}$
because $V_{DS} \ll V_{gs} - V_T \Rightarrow r_{ON} = \frac{1}{2k(V_{gs} - V_T)} = \frac{1}{2k(V_a - V_T)} \quad (1)$



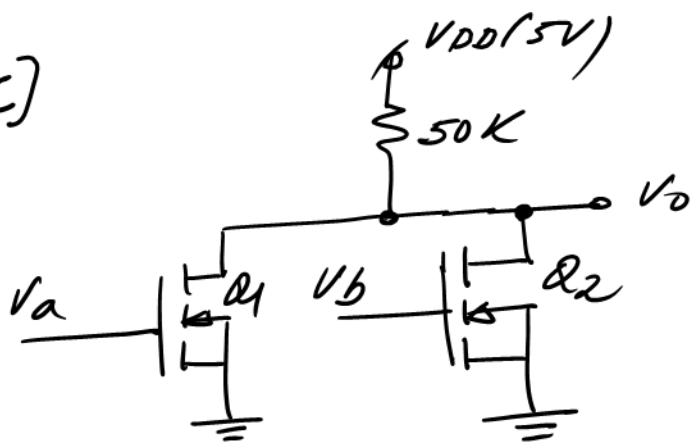
$$V_o = 0.2 \Rightarrow I_{DS} = \frac{5 - 0.2}{50} = 0.096 \text{ mA}$$

$$r_{ON} = \frac{0.2}{I_{DS}} = 2.08 \text{ K}$$

$$(1) \quad 2.08 = \frac{1}{2 \cdot 0.2 (V_i - 3)} \Rightarrow V_i = 3 + \frac{1}{2 \cdot 0.2 \cdot 2.08} = 4.20 \text{ V}$$

$V_i = V_{gs} \Rightarrow V_{DS} = V_o = 0.2 < V_{gs} - V_T = 4.2 - 3 \Rightarrow Q_1 \text{ linear}$
OK

[C]



V_a	V_b	Q_1	Q_2	V_o
0	0	OFF	OFF	"1"
0	5	OFF	ON	"0"
5	0	ON	OFF	"0"
5	5	ON	ON	"0"

$$O = \overline{A+B}$$

(NOR)