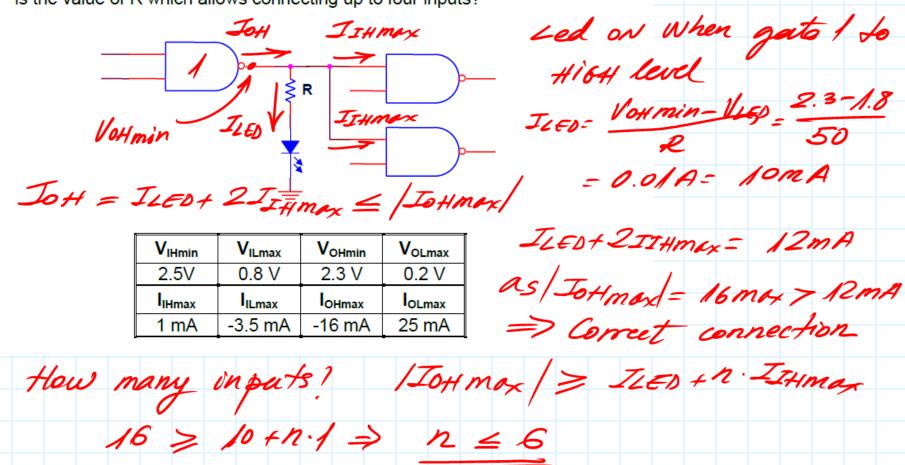
23. The LED of figure with a resistor R of 50 Ω, is inserted in the digital circuit to display an internal variable. Taking into account the specifications of the logic gates as detailed in the following table, and V_(LED)=1.8V, a) Is this connection correct? If it is correct, how many inputs can be connected in total? If not, what is the value of R which allows connecting up to four inputs?



25. We want to connect the outputs of 2 standard components of a logic family with a voltage supply of 5V, to 3 inputs of components of the same family. The specifications of the family are shown in the following table:

VIHmin	V _{ILmax}	V OHmin	V _{OLmax}
2 V	0.8 V	2.4 V	0.4 V
Illmax	I _{ILmax}	I _{OHmax}	I _{OLmax}
40 μΑ	-1.6 mA	-400uA	16 mA

Vot min > Vit min ? => OK 2.4 2 S Volmax & VIL mex? => OK 0.8 0.4 Voltage compatible

To make correctly this connection:

[A] We do not need to add anything more.

[B] It should be added a pull-up resistor between the output and the voltage supply, with a range of possible values between 0.41 k Ω and 8,12 k Ω .

[C] It cannot be done the connection of the outputs, since it would cause an undetermined voltage and the degradation of the output transistors.

[D] It should be added a pull-up resistor between the output and the voltage supply, with a range of possible values between $0.41~\text{k}\Omega$ and $11.82~\text{k}\Omega$.

Currents: Jolmax > 3/JILMOX/? =>OK (> Current 1.6)

JOHMAN > 3-IJHMOX ? ->OK)

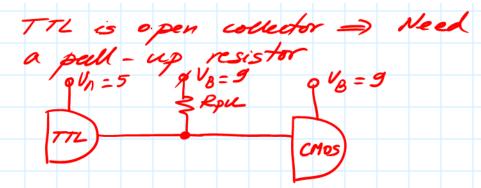
480 µ 40 µ

31. We want to connect a TTL open collector output with an input of a CMOS logic circuit powered to + 9V. Indicate the CORRECT answer:

Family A (TTL open collector)			Family B (CMOS +9V)			
V _{OLmax}	I _{OHmax (fugas)}	I _{OLmax}	V_{IHmin}	V _{ILmax}	I _{IHmax}	I _{ILmax}
0.4 V	100 μΑ	16 mA	6.3 V	2.7 V	0.1 μΑ	-0.1 μA

[A] It is necessary to connect a pull-up resistor between the output and the power supply. of + 9V. The value of the resistance must be between $0.54K\Omega$ and $26.97K\Omega$.

- [B] We can connect both famílies directly.
- [C] It is necessary to insert a TTL buffer to make the current compatible at low level.
- [D] It is necessary to connect a pull-up resistor between the output and the power supply. of + 9V. The value of the resistance must be between $2.1 \text{K}\Omega$ y $41.4 \text{K}\Omega$.

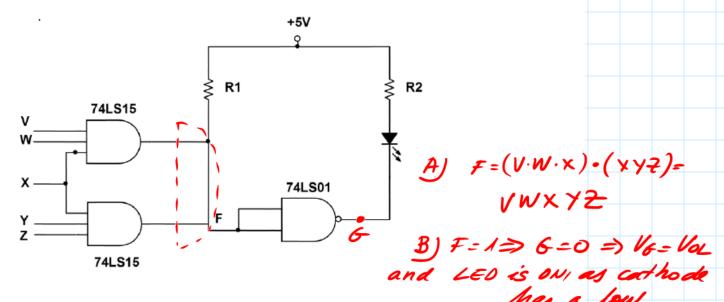


$$P_{pu} \leq \frac{V_{B} - V_{IHmin}}{J_{OHmax} + J_{IHmax}} = \frac{9 - 6.3}{0.1 + 0.0001}$$

$$Rpu > \frac{V_B - V_{OLMAX}}{J_{OLMAX} - |J_{ILMAX}|}$$
 $Rpu > \frac{9 - 0.4}{16 - 0.0001} = 0.538K$

0.538K < Lpn < 26.97K

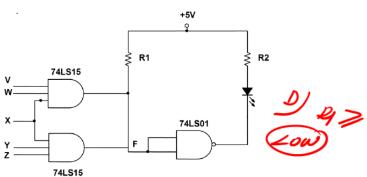
32. The following circuit uses logic gates with open collector output (within the 74LS01 and 74LS15 integrated circuits) to implement a "wired AND", and to activate the LED output.



- A. Write a logical expression for the function implemented by the circuit in the signal F.
- **B.** When F = '1', Is the LED on or off?.
- **C.** Design R2, assuming that the current through the LED when it lights is $I_{LED\ (on)} = I_{OLmax}$ and $V_{LED\ (on)} = 1.2V$.
- **D.** Taking into account the following features for 74LS01 and 74LS15 integrated circuits, calculate the range of values allowed for R1:

Vcc	V _{IHmin}	V _{ILmax}	V _{OLmax}	l _{IHmax}	l _{OHmax} (Leakage)	lOLmax	lLmax
5 V	2.5V	0.8 V	0.5 V	20 μΑ	100 μΑ	7 mA	-0.36 mA

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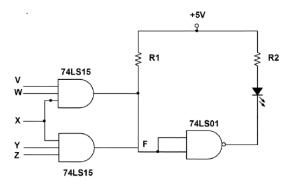
Vcc	V _{IHmin}	V _{ILmax}	V _{OLmax}		lOHmax (Leakage)	lOLmax	lLmax
5 V	2.5V	0.8 V	0.5 V	20 μΑ	100 μΑ	7 mA	-0.36 mA

R1 = Vce-V3+1min = Z JOHMA +2 JIHMA

 $\frac{5-2.5}{0.1+2\cdot0.02}=10.417k$

0.717K = P1 = 10.417K

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5 V	2.5V	0.8 V	0.5 V	20 μΑ	100 μΑ	7 mA	-0.36 mA