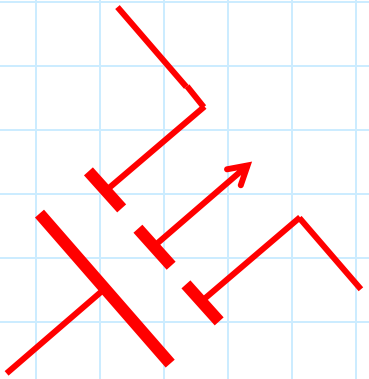
Unit 2: THE MOSFET transistor



Objectives

At the end of this chapter, the student should:

- Know the importance of MOSFET transistors in the development of computers, knowing their characteristics and their relationships with the success of the digital world.
- Know the operating principles of MOSFET transistors, their characteristic curves and operating regions.
- Solve simple DC circuits with one or more transistors.
- Understand MOSFET operation inside basic circuits and digital switching systems.
- Known protection techniques for MOSFETs inputs

Unit 2: Contents

Bibliography

THEORY:

- A.R.Hambley, “Electronics” (2ª Ed.)”, Prentice Hall, 2002.
- M.H.Rashid, “Microelectronic circuits. Analysis and design”, Thomson, 2002.
- N. R. Malik, “Electronic circuits: analysis, simulation and design”, Prentice Hall, 2000.
- R. Boylestad, L. Nashelsky, “Electronics, circuit theory”, Pearson, 2009.
- A.P. Malvino, D.J. Bates, “Electronic principles”, Mc Graw Hill, 2007.

PROBLEMS:

- G. Benet, J. V. Benlloch, V. Busquets, D. Gil, P. Pérez: “Ejercicios resueltos de Tecnología de Computadores”, 2006.916

2.1 Introduction

FET = *Field Effect Transistor*
Current controlled by an electric field
Unipolar device

JFET (Junction FET), Shockley, 1952
MOSFET (Metal-Oxide-Semiconductor FET)
Kahn y Atalla, 1960

- Deplexion
- Enhancement

- N Channel (NMOS Transistor)
- P Channel (PMOS Transistor)

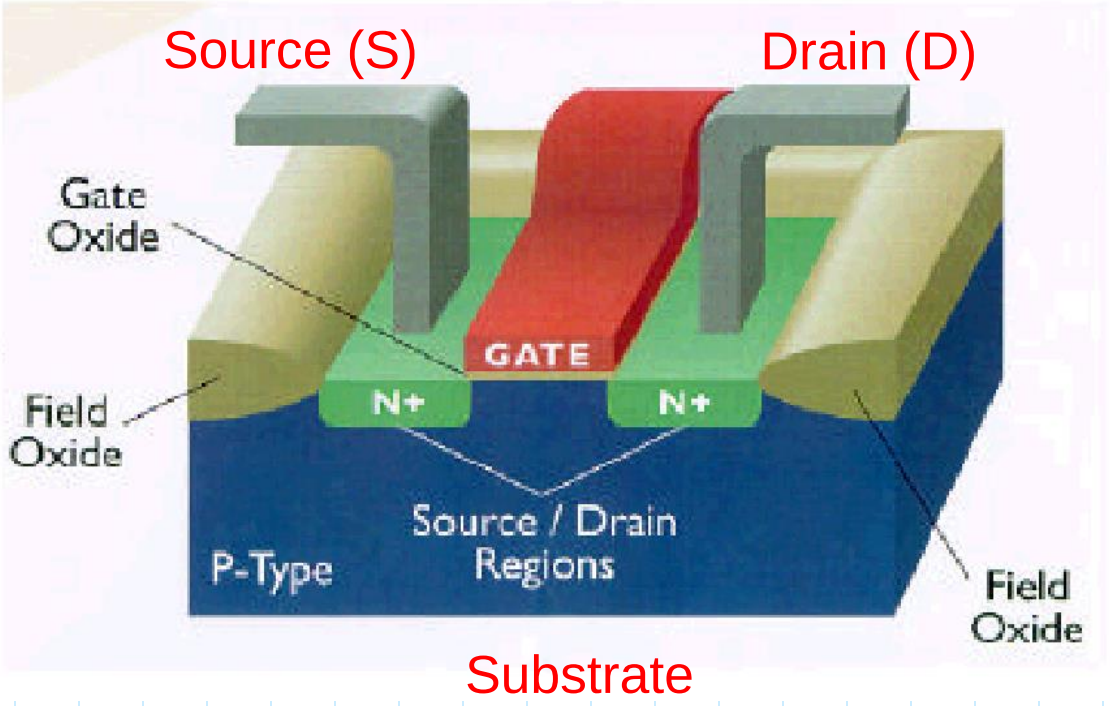
2.1 Introduction(2)

- Some advantages:
  - High integration density=> VLSI
  - Versatility: R, C, switch,
  - Low power
  - High input impedance
- Some drawbacks:
  - Slower than BJT
  - Less linearity

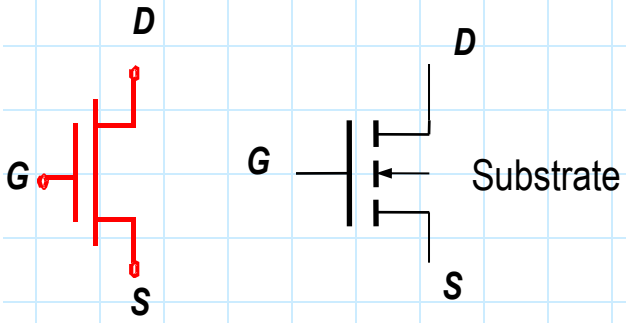
2.2 Basic principles of operation

Internal structure:

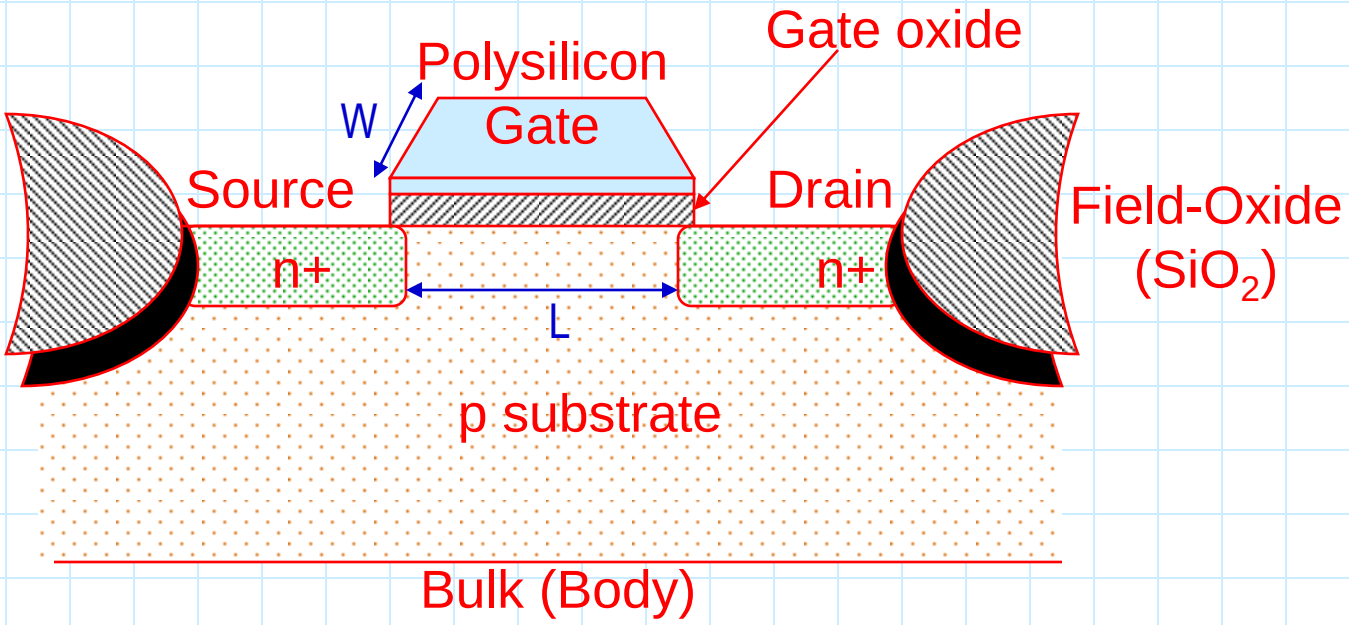
N-channel Enhancement MOSFET (NMOS transistor):



Symbols



NMOS Transistor: cross section

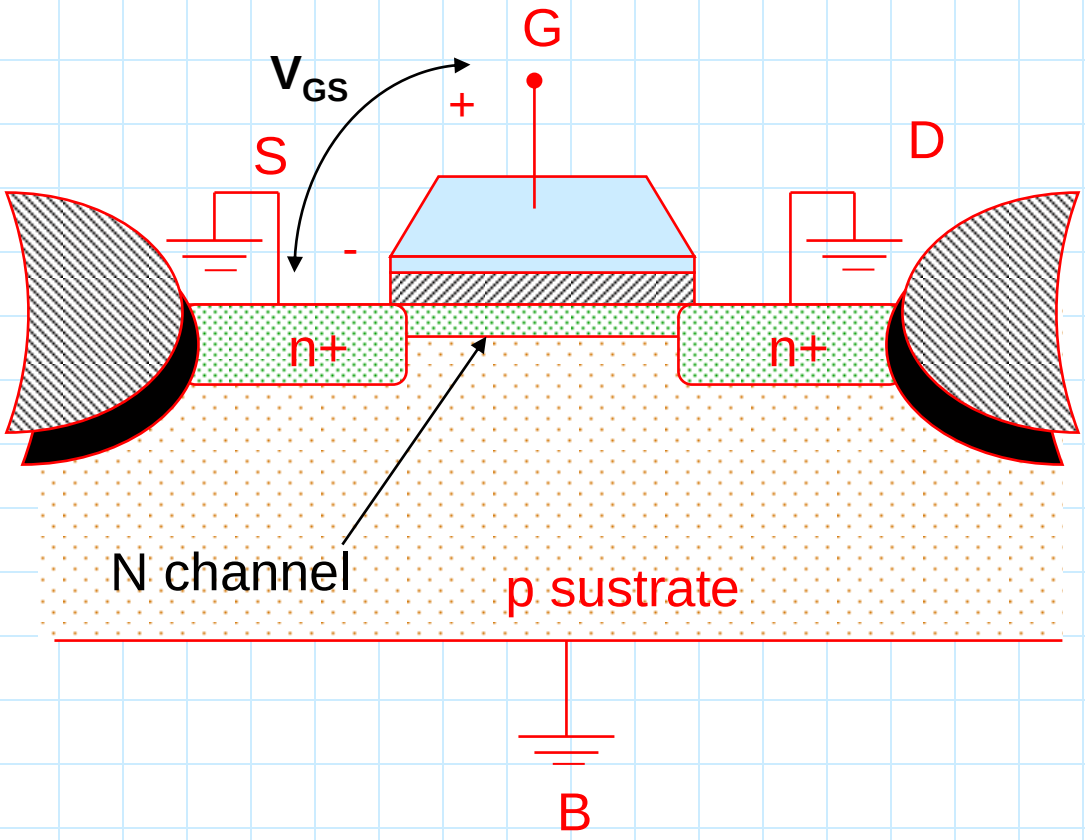


Constants:

K (mA/V^2) *Pspice: K = (W/L) Kp / 2*

V_T (V) *Pspice: V_T = vto*

Operating regions: channel formation



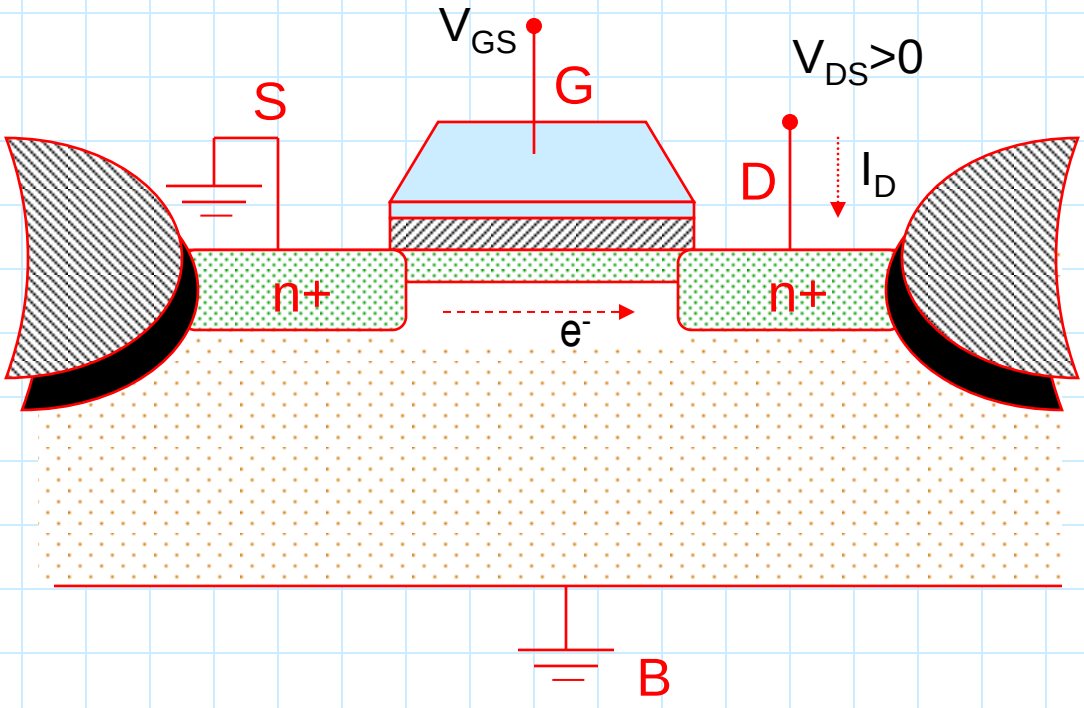
Channel formation:

$V_{GS} > V_T$: a N-type channel is formed between S and D

$V_{GS} \leq V_T$: no channel is formed→ CUT-OFF

Operating regions : ohmic region

Assuming $V_{GS} > V_{T:}$



Conducting condition:

$V_{DS} > 0 \rightarrow I_{DS} > 0$

Working principles: linear region (2)

Condition: $V_{DS} \leq V_{GS} - V_T$

V/I function: $I_D = K\,[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$

For small V_{DS}:

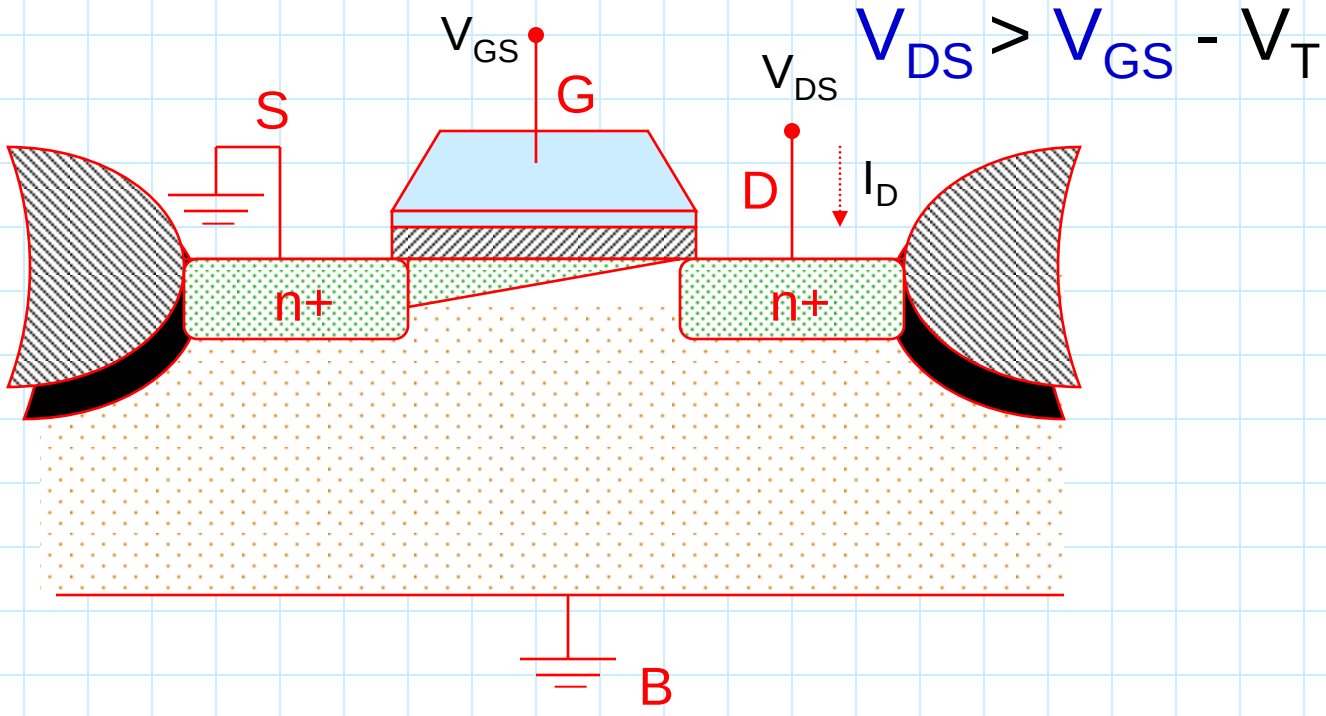
$$I_D \approx K\,[2\,(V_{GS}\text{-}V_T)\,V_{DS}\,]$$

$$R_{DS(on)} = R_{ON} \approx \frac{1}{2 \cdot K(V_{GS} - V_T)}$$

The MOSFET resistance decreases when K and V_{GS} increase

Operating regions: saturation region

Assuming $V_{GS} > V_T$



The channel is pinched-off (small channel near D), and the current remains constant

Operating regions: saturation region(2)

Condition: $V_{DS} > V_{GS} - V_T$

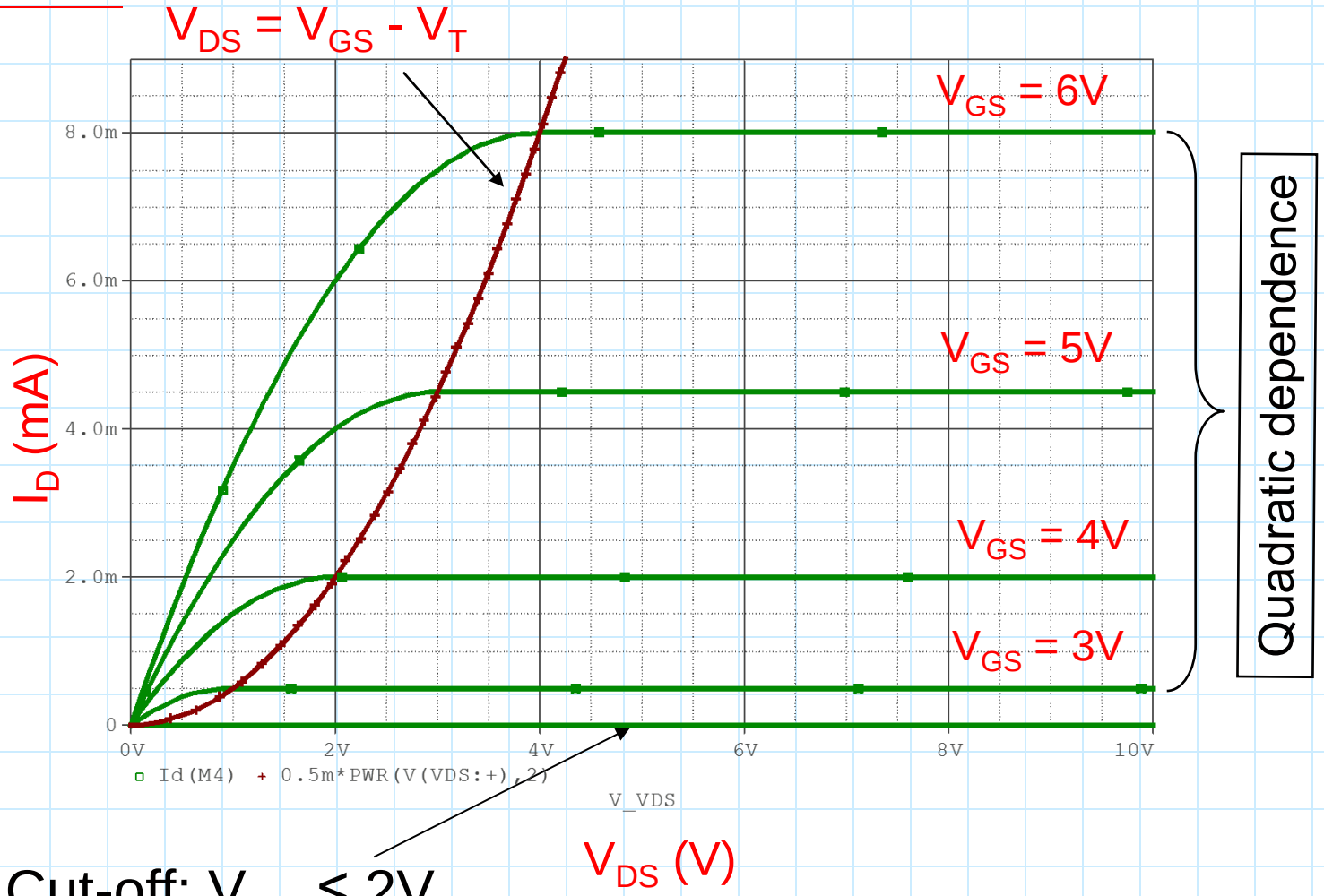
V/I function: $I_{DS} = K (V_{GS} – V_T)^2$ (Saturation parable)

The channel is *pinched-off* →

For a fixed VGS, the current $I_{DS} \approx$ constant, and indep. of V_{DS}

The Mosfet is equivalent to a current source (I_{DS}) controlled by voltage (V_{GS})

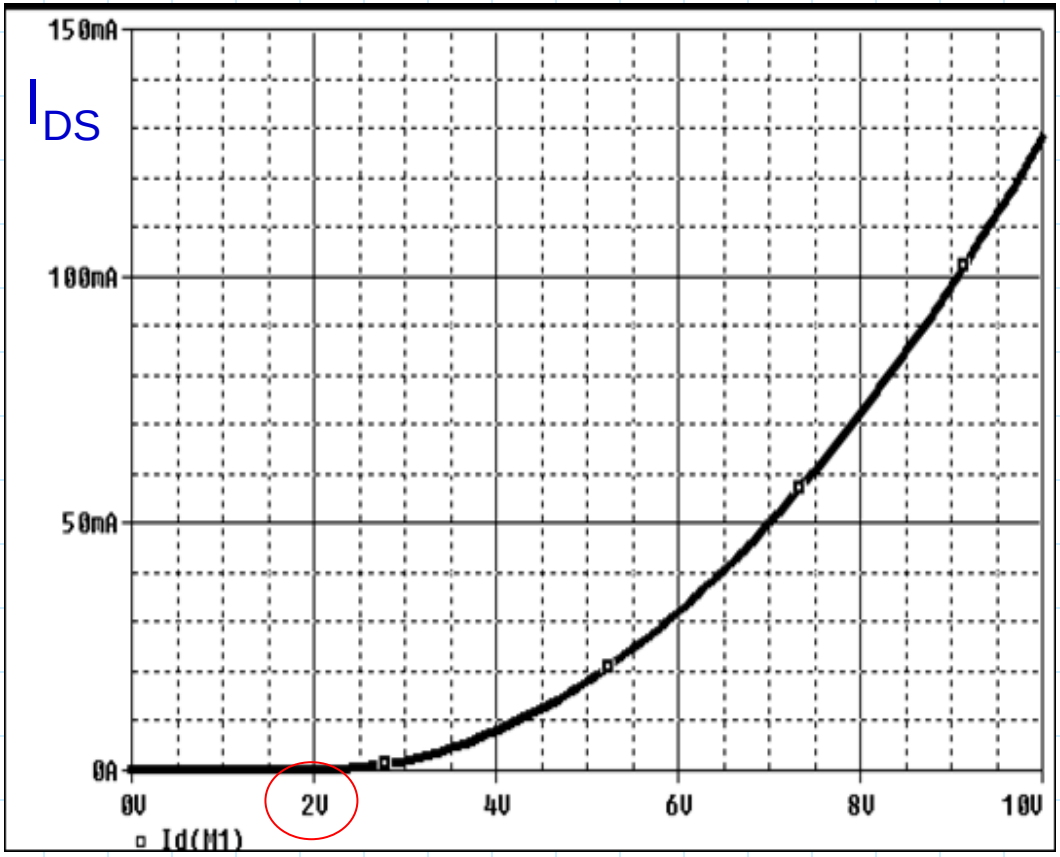
I-V curves of the NMOS



Cut-off: $V_{GS} \leq 2V$

Example: NMOS Transistor: $V_T = 2V$ $K = 0.5mA/V^2$

I_{DS} versus V_{GS} in saturation region



V_{GS}

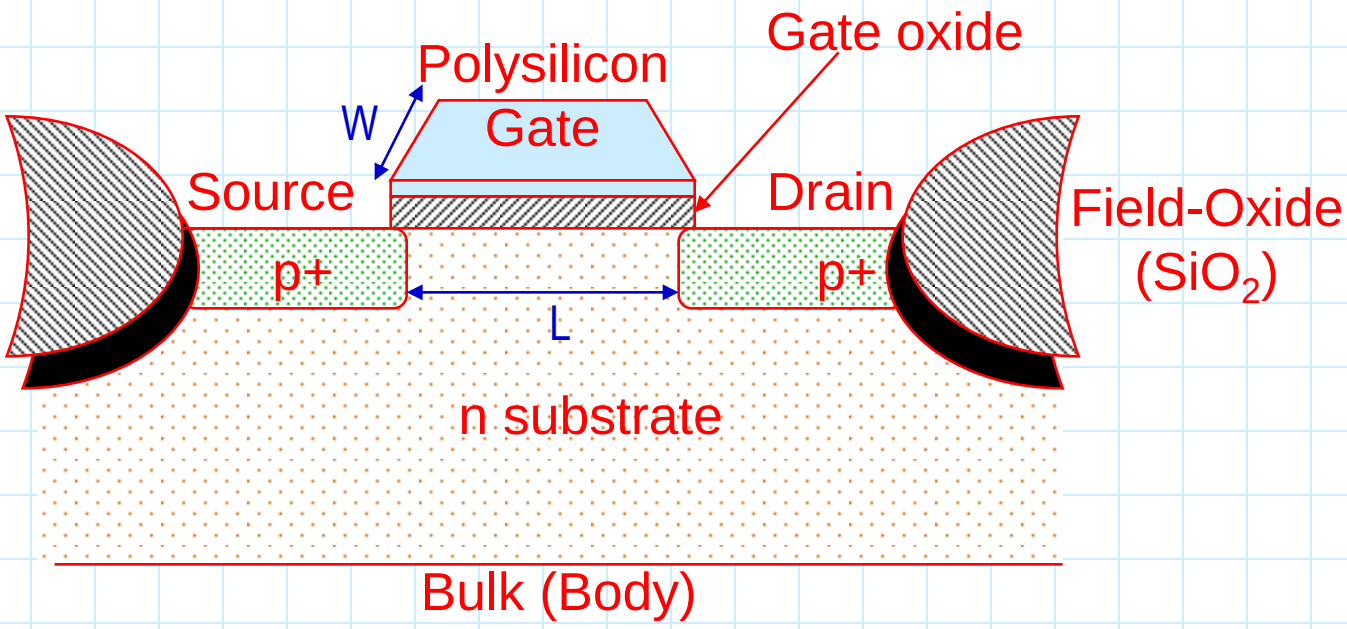
V_T= 2V

Saturation parable:

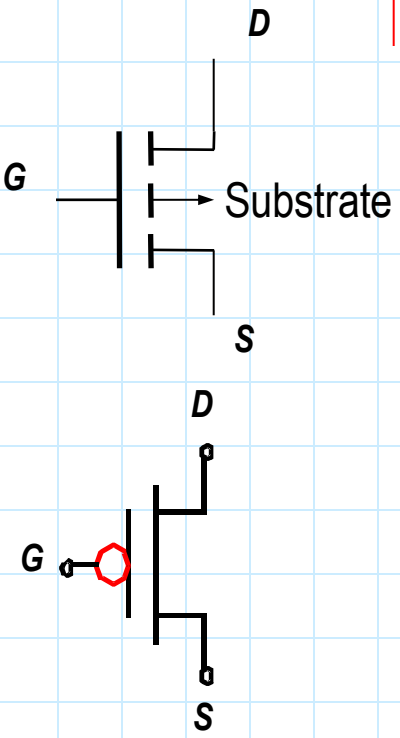
$$I_{DS} = K (V_{GS} - V_T)^2$$

$V_{GS} \leq V_T \rightarrow I_D = 0$

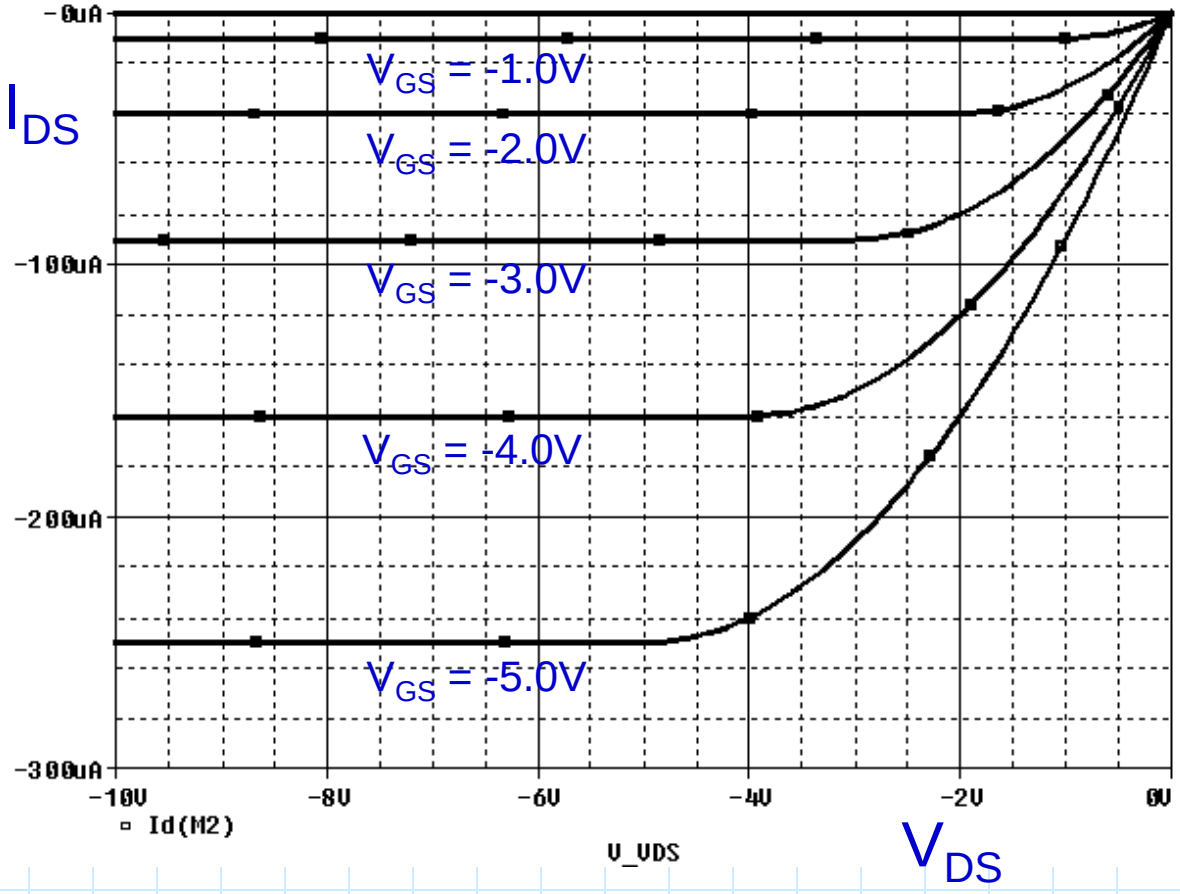
PMOS Transistor: cross section



Symbols



PMOS. Characteristic curves



All variables are negatives!

$V_{GS} < 0$, $V_{DS} < 0$,

$I_{DS} < 0 \rightarrow I_{SD} > 0$

Conduction: $V_{GS} < -V_T$

The PMOS transistor: summary

- Cut-off: $V_{GS} \geq -V_T$
- Saturation:

  $V_{DS} < V_{GS} + V_T$

  $I_{SD} = K (V_{GS} + V_T)^2$
- Ohmic:

$$R_{ON} \approx \left| \frac{1}{2 \cdot K(V_{GS} + V_T)} \right|$$

(considering K and V_T as absolute values, $V_{GS} < 0$, $V_{DS} < 0$)

- Less use than N-channel MOSFETS, as holes mobility is smaller than electrons mobility:
  - Slower than the NMOS
  - They need more W/L → bigger than NMOS (more space occupied)

MOSFET: Summary of some formulas

NMOS		PMOS
$V_{GS} > V_T$	CONDUCTS	$V_{GS} < -V_T$
$V_{DS} > V_{GS} - V_T$	SATURATION condition	$V_{DS} < V_{GS} + V_T$
$I_{DS} = K (V_{GS} - V_T)^2$	SATURATION	$I_{SD} = K (V_{GS} + V_T)^2$
$I_{DS} = K [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$ $R_{ON} \approx \frac{1}{2 \cdot K(V_{GS} - V_T)}$	OHMIC or LINEAR	$I_{SD} = K [2(V_{GS} + V_T)V_{DS} - V_{DS}^2]$ $R_{ON} \approx \left\lvert \frac{1}{2 \cdot K(V_{GS} + V_T)} \right\rvert$

(Taking the absolute value of V_T and K in all formulas)

Summary NMOS regions

NMOS	Equation	Check
CUT-OFF	$I_{DS} = 0$	$V_{GS} < V_T$
SATURATION	$I_{DS} = K (V_{GS} - V_T)^2$	$V_{DS} > V_{GS} - V_T$
OHMIC or LINEAR	$I_{DS} = K [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$ $R_{ON} \approx \frac{1}{2 \cdot K(V_{GS} - V_T)}$	$V_{DS} < V_{GS} - V_T$

(Taking the absolute value of V_T and K in all formulas)

Equivalences and differences between Mosfet-BJTs

Terminals

MOSFET	BJT
DRAIN	COLLECTOR
SOURCE	EMITTER
GATE	BASE

BJT: $I_B > 0$ for conducting

Mosfet: $I_G = 0$ always!

Working regions

MOSFET	BJT
CUT-OFF REGION	CUT-OFF REGION
SATURATION REGION	ACTIVE REGION
OHMIC \ LINEAR REGIN	SATURATION REGION

Mosfet's Saturation : maximum I_{DS} for a given V_{GS}

BJT's saturation: maximum I_C for a given biass circuit

Enhancement MOSFET Biassing (1)

Equations to analyze the Mosfets biassing circuits

1.- Input loop: G-S → loop equation with V_{GS}

2.- Assuming saturation → saturation equation

NMOS: $I_{DS} = K (V_{GS} - V_T)^2$ PMOS: $I_{SD} = K (V_{GS} + V_T)^2$

(With VGS, checkout if MOSFET is conducting)

3.- Output loop D-S → loop equation with V_{DS}

4.- Checkout of saturation

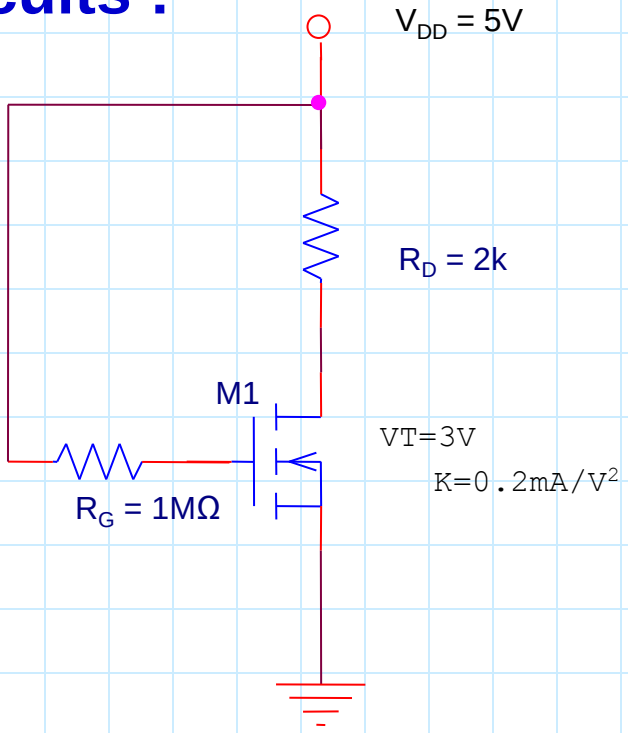
NMOS: $V_{DS} > V_{GS} - V_T$ PMOS: $V_{DS} < V_{GS} + V_T$

(*If not satisfied, return to step 2, using the equation of the linear region, and redo the calculations)*

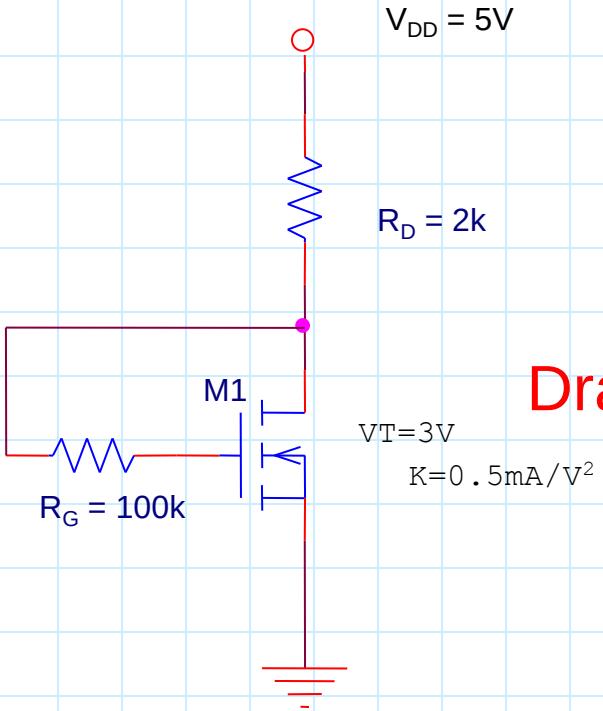
Enhancement MOSFET. Biassing (2)

Examples of Biassing circuits :

Fixed biassing

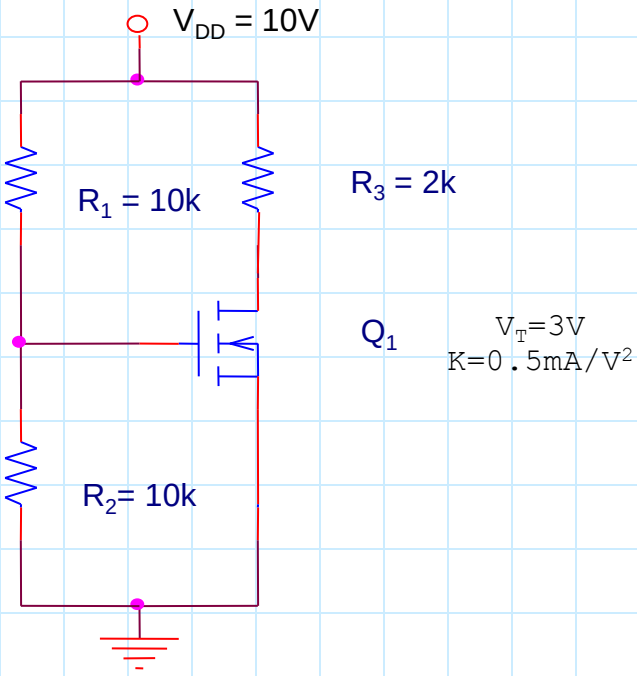


Drain feedback



Enhancement MOSFET. Biassing (3)

Biassing with resistor divider

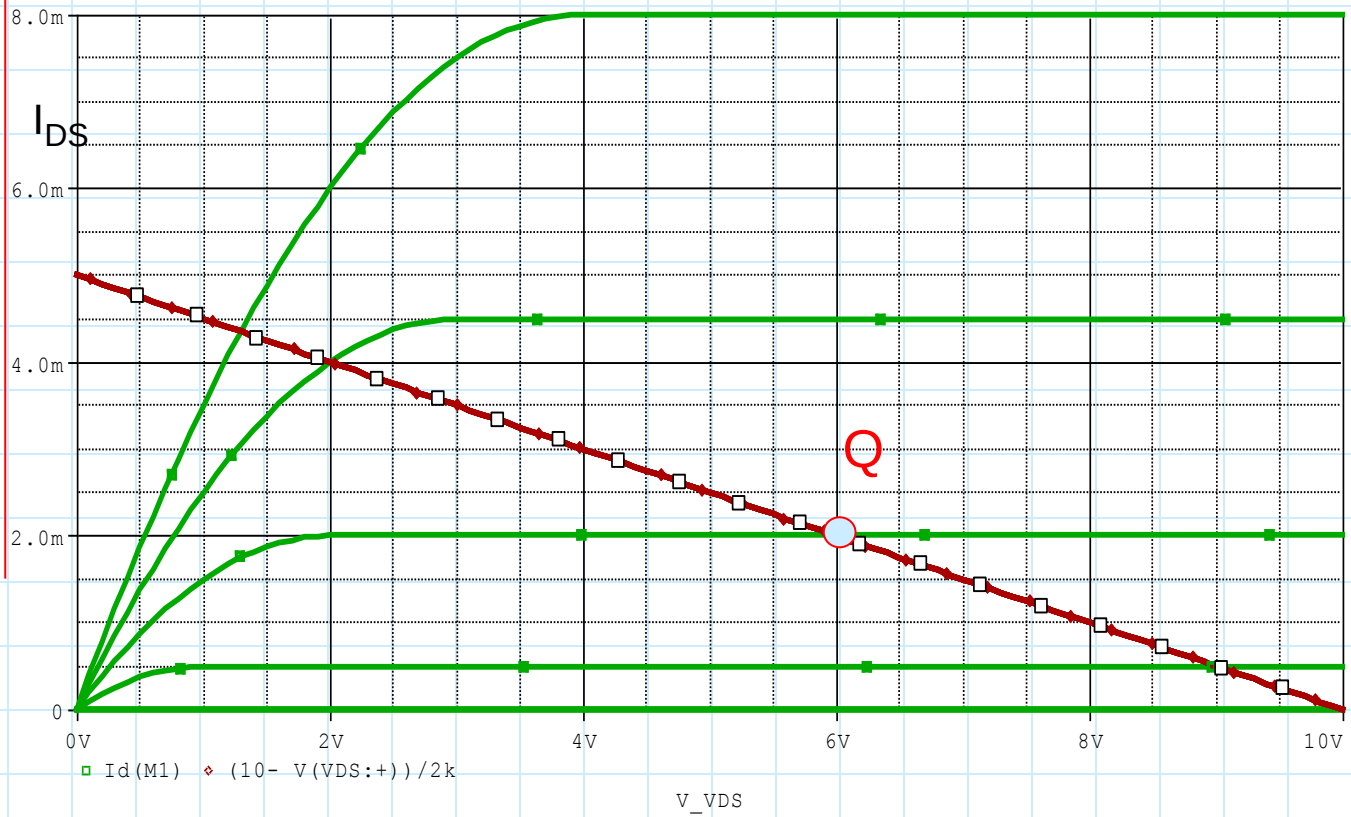


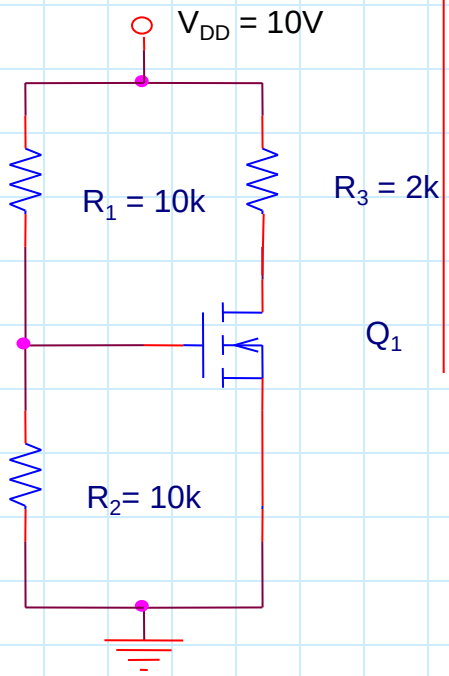
2 solutions for I_{DS} → you choose the one for which $V_{GS} > V_T$

The load line

Load line: $V_{DS} = V_{DD} - I_{DS} \times R_D$

The quiescent point (Q) is determined by intersecting the characteristic curve of MOSFET and the load line.



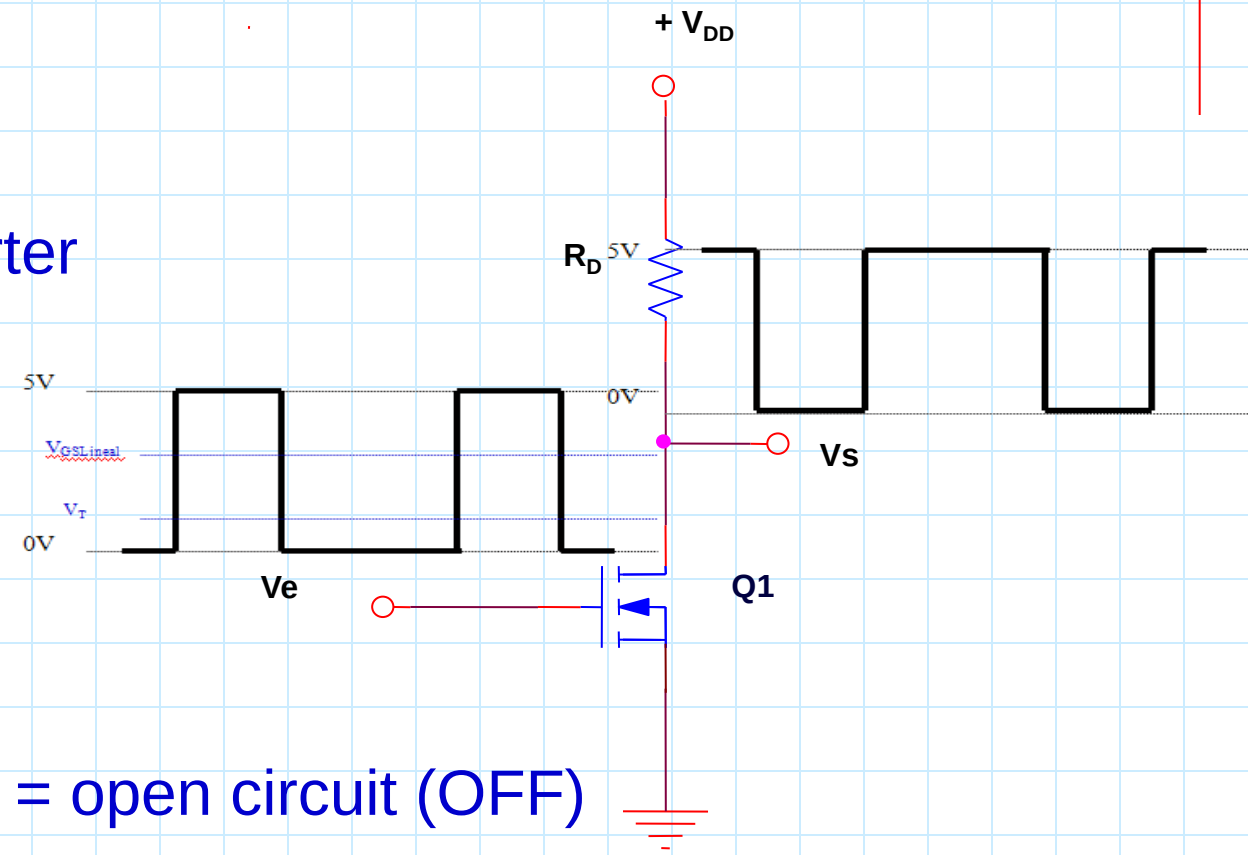


V_T=3V
K=0.5mA/V^2

2.3 The MOSFET in switching mode

- The transistor operates between cut-off and linear regions

NMOS inverter



$Ve = V_{GS}$

Two state:

$Ve < V_T$ → Mosfet = open circuit (OFF)

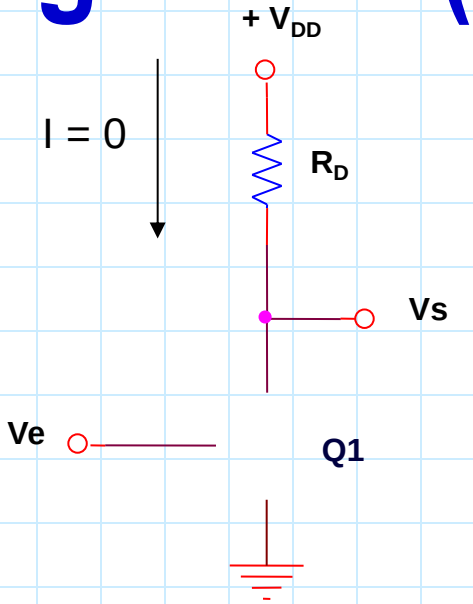
$Ve = V_{DD}$ → Mosfet ≈ R_{on} (very low resistance - ideally a closed switch-ON)

The MOSFET in switching mode (2)

$Ve = V_{GS}$

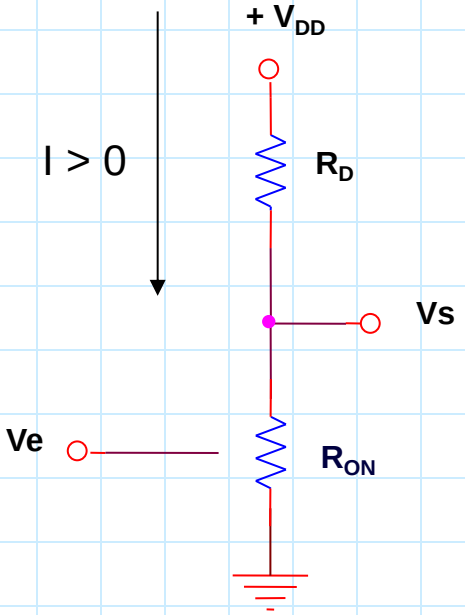
Two state:

- $Ve < V_T \rightarrow$ Cut-off $\rightarrow V_{OH} = V_{DD} =$ "1"



- $Ve = V_{DD} \rightarrow$ Mosfet $\approx R_{on}$

$$R_{ON} \approx \frac{1}{2 \cdot K(V_{GS} - V_T)} \; ; \; V_{OL} = V_{DD} \times \frac{R_{ON}}{R_D + R_{ON}}$$

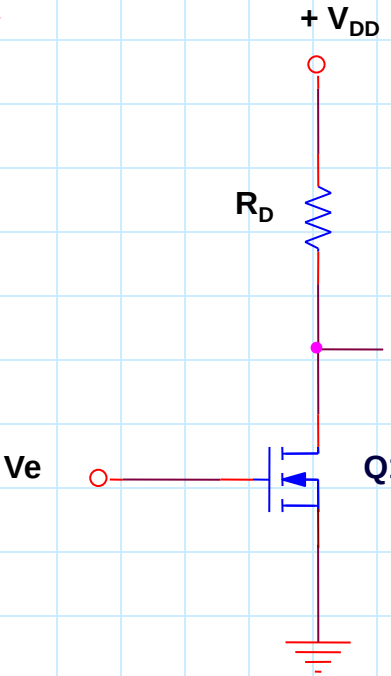


if $R_{on} << R_D \rightarrow V_{OL} \approx 0V =$ "0"

There is static power consumption (I > 0)

The MOSFET in switching mode (3)

NMOS inverter:



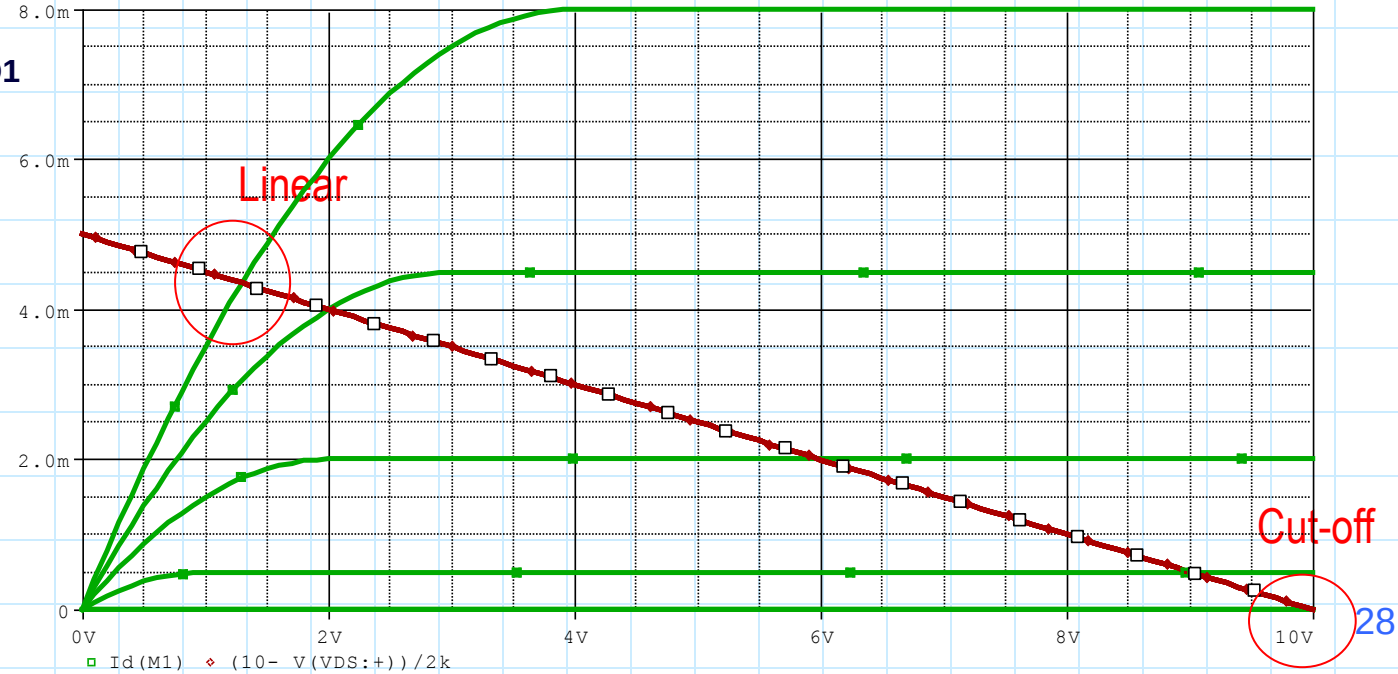
Load line= Loop D-S equation

$V_{DD} = I_D R_D + V_{DS}$

Intersection points:

Vertical axis→ $I_D = V_{DD}/R_D$

Horizontal axis→ $V_{DS} = V_{DD}$



The MOSFET in switching mode (4)

Example:
Design an NMOS inverter with pull-up resistor

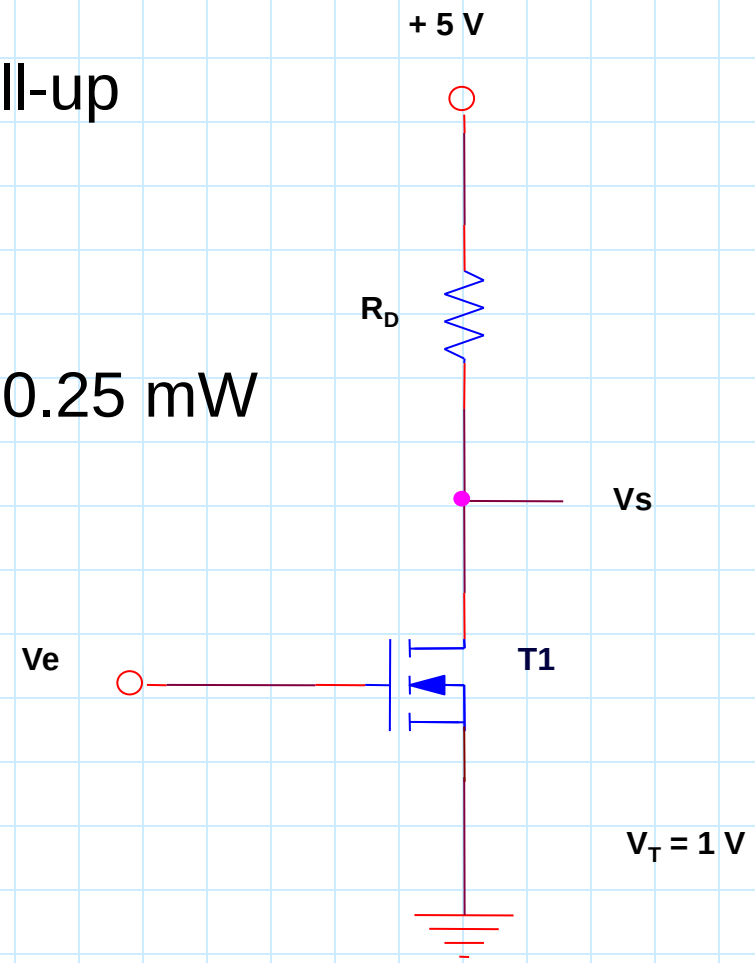
Data:

Power consumption at low level = 0.25 mW

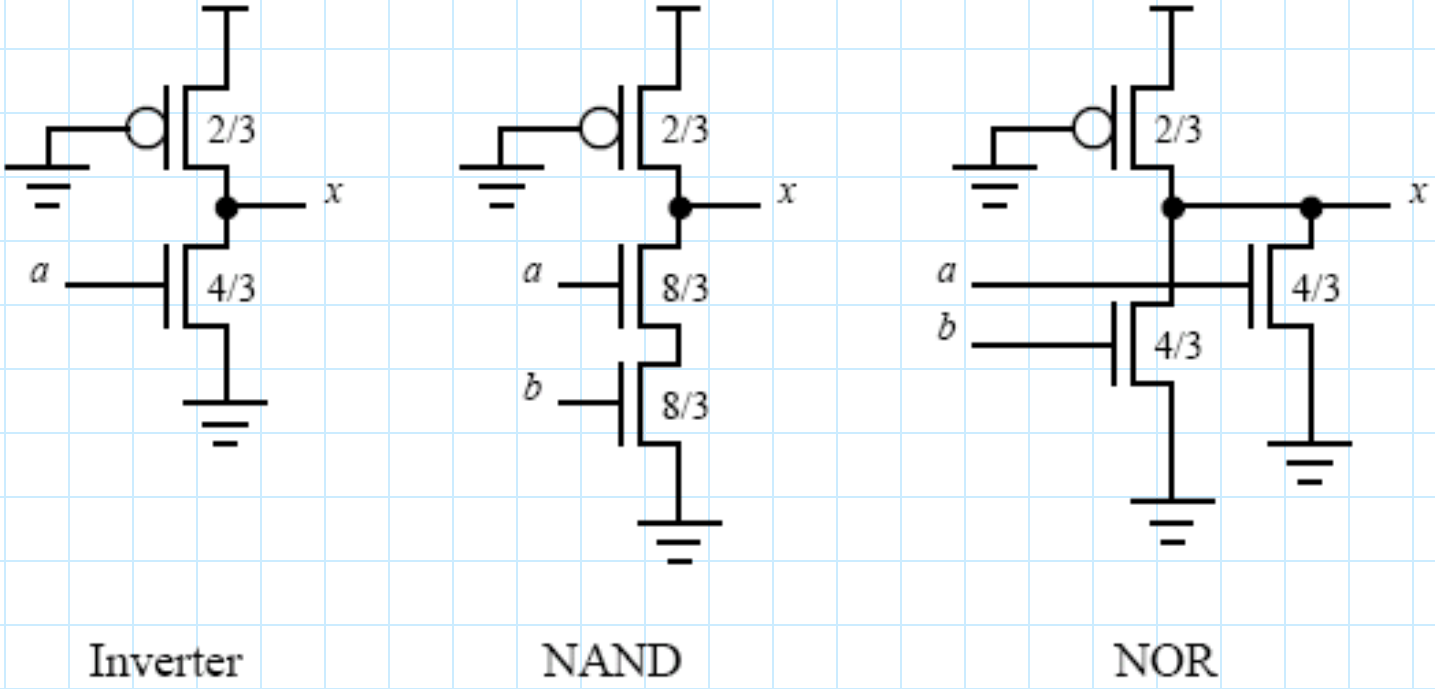
V_{OL} = 0.5V, V_{OH} = V_{DD} = 5V

Transistor: V_T = 1V

Find out R_{on} and K



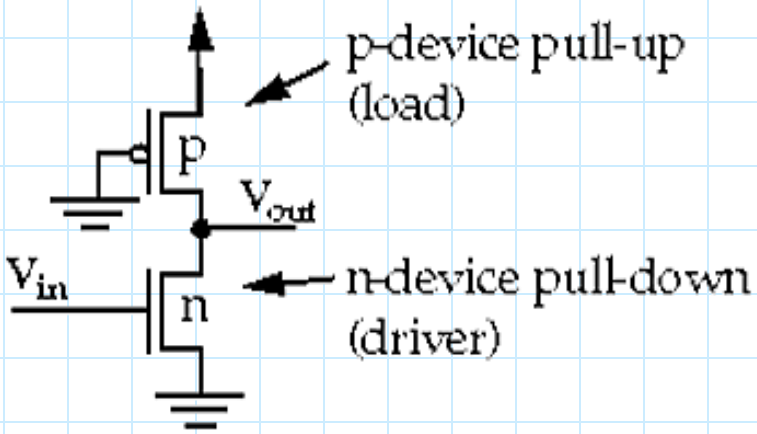
Active loads. Pseudo-NMOS Logic

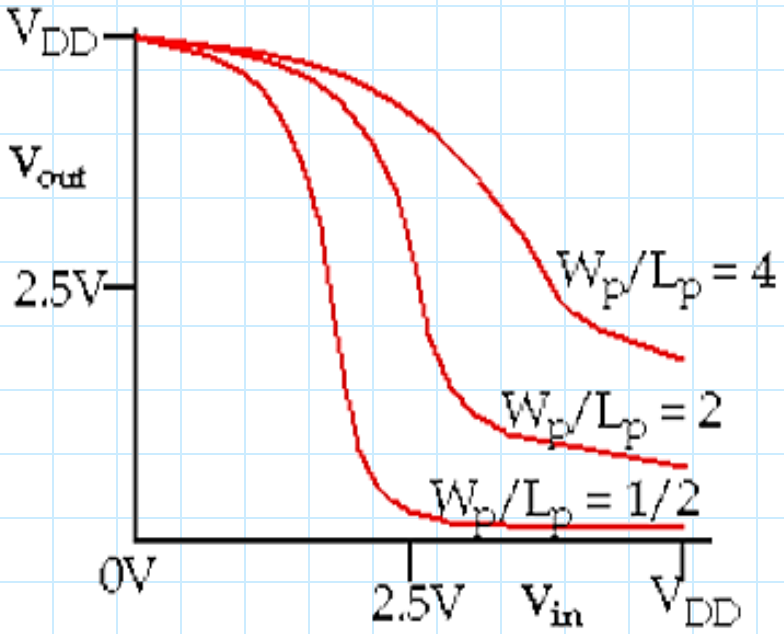


Inverter NAND NOR

- PMOS trasistor always conducting
- Saving Silicon area (no Rpull-up necessary)
- Used in ROM, PLA and FLASH

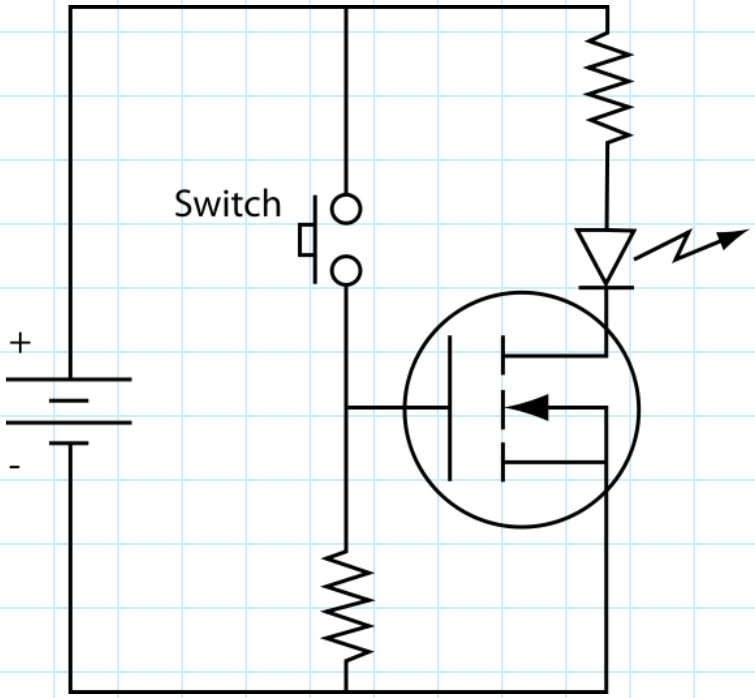
Active loads. Pseudo-NMOS Logic





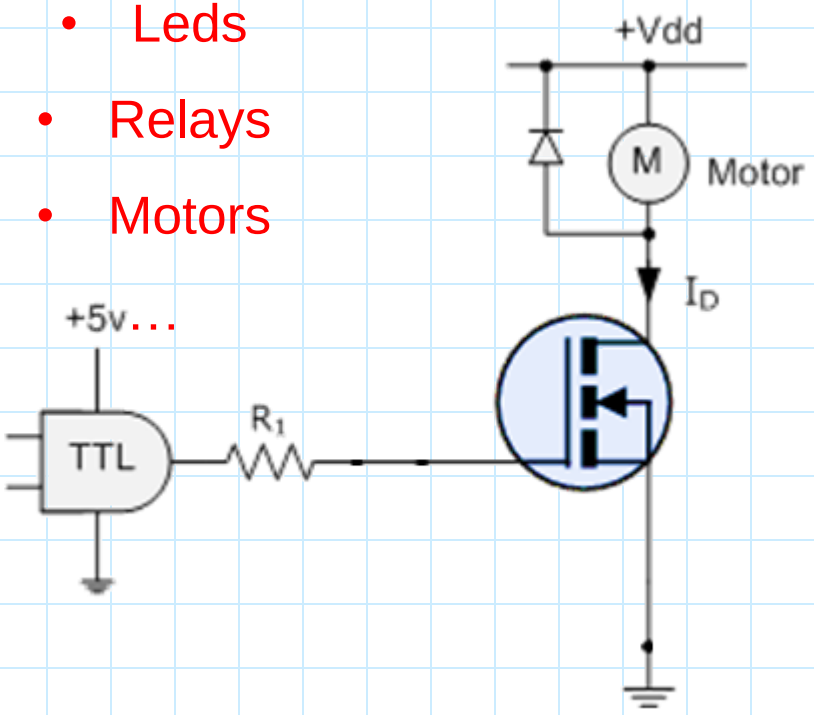
Transference curve versus channel size (W/L)

The MOSFET in switching mode. Applications



We can control:

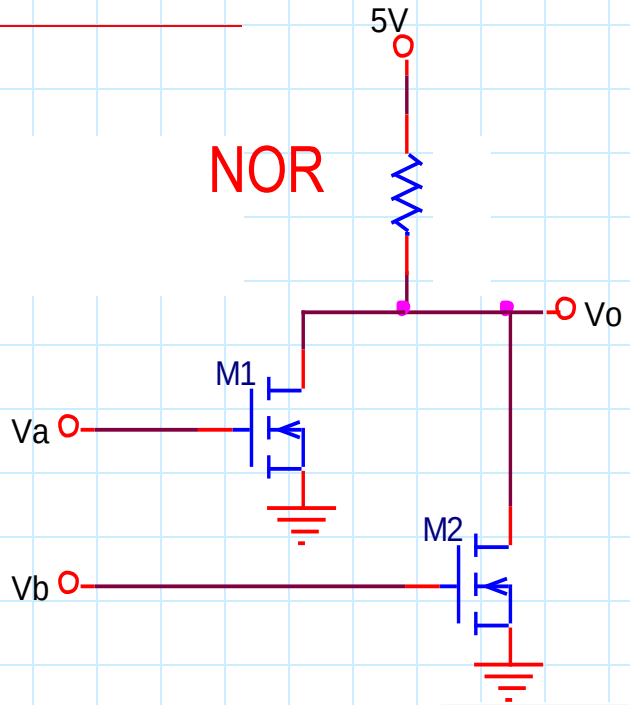
- Leds
- Relays
- Motors



Switch pushed→ VGS = VDD → Mosfet On (closed switch) → LED ON

Switch released→ VGS = 0 → Mosfet off (open switch) → LED OFF

2.4 NMOS logic gates

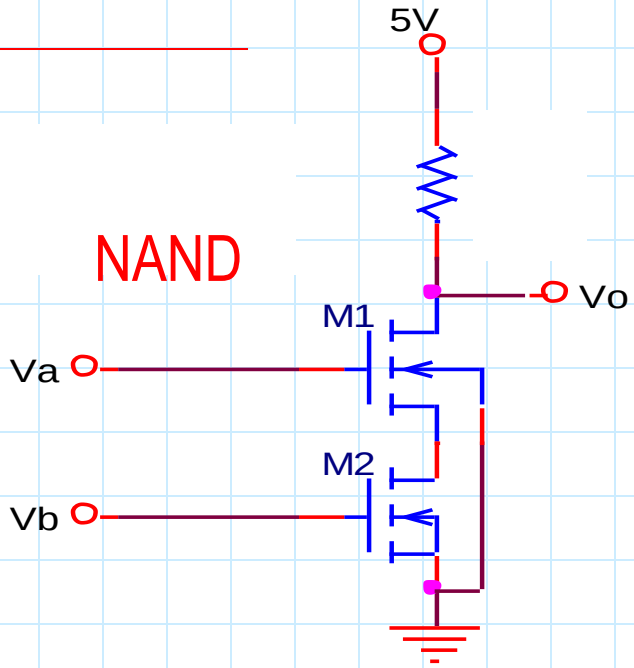


Let's assume:
"0" = 0V
"1" = 5V

Transistors in parallel

Va	Vb	M1(OFF/ON)	M2 (OFF/ON)	Vo
0	0			
0	1			
1	0			
1	1			

2.4 NMOS logic gates

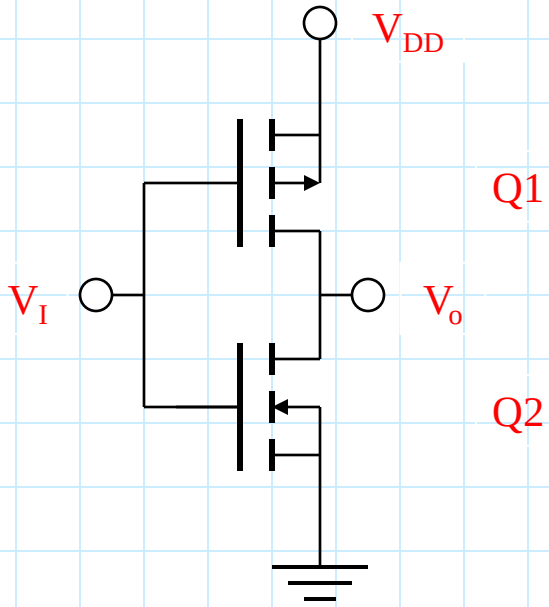


Let's assume:
"0" = 0V
"1" = 5V

Transistors in series

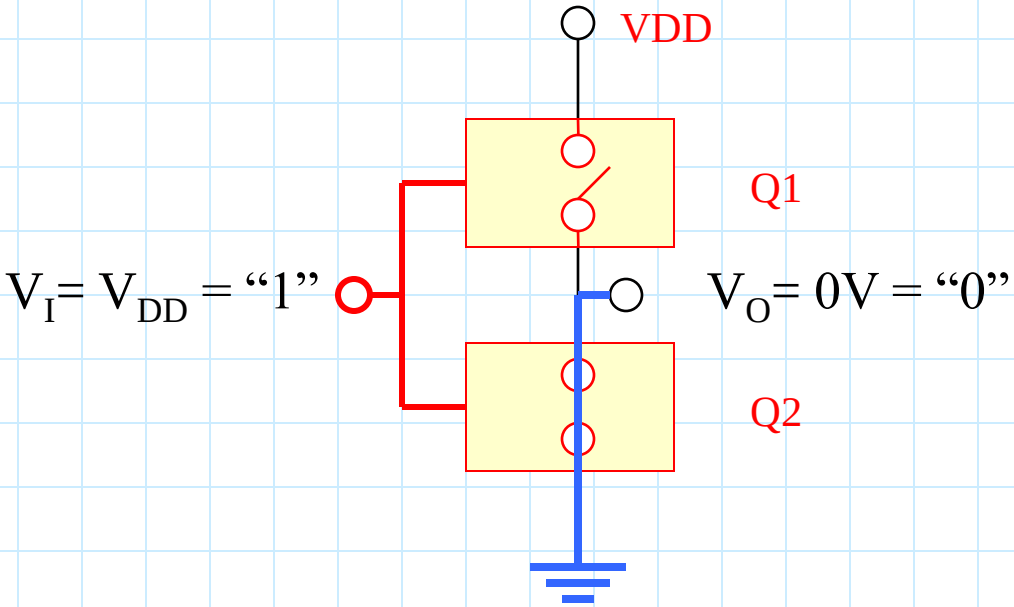
Va	Vb	M1(OFF/ON)	M2 (OFF/ON)	Vo
0	0			
0	1			
1	0			
1	1			

2.5. The CMOS inverter



Digital input: $V_I = 0V$ = “0”; $V_I = V_{DD}$ = “1”

2.5. The CMOS inverter (2)

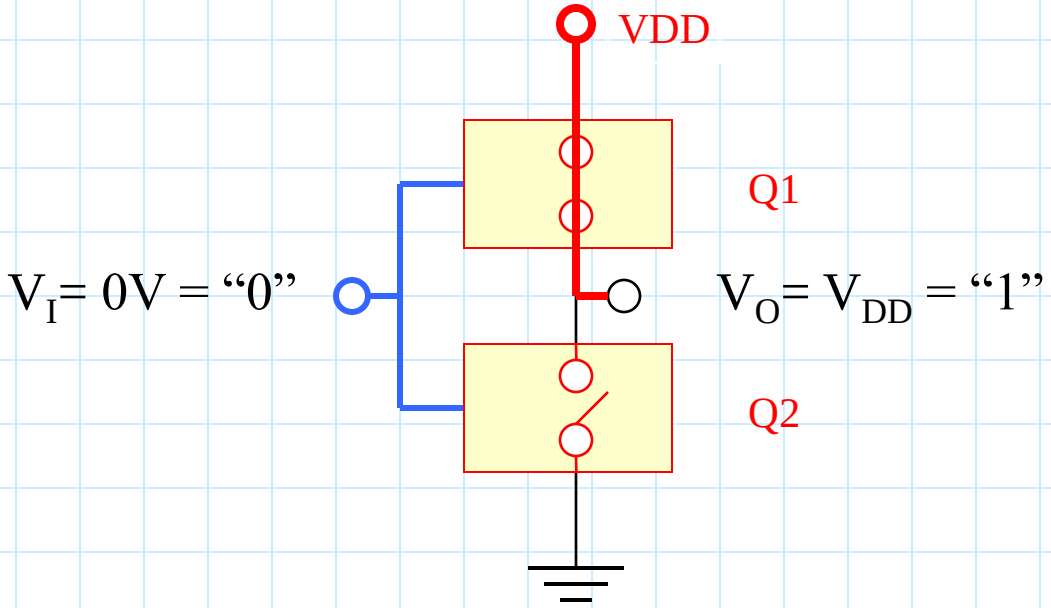


$V_{GS1} = V_{DD} - V_{DD} = 0V > -V_T$ ⇨ PMOS cut-off

$V_{GS2} = V_{DD} - 0V = V_{DD} > V_T$ ⇨ NMOS conducts

The static consumption is = 0

2.5. The CMOS inverter (3)



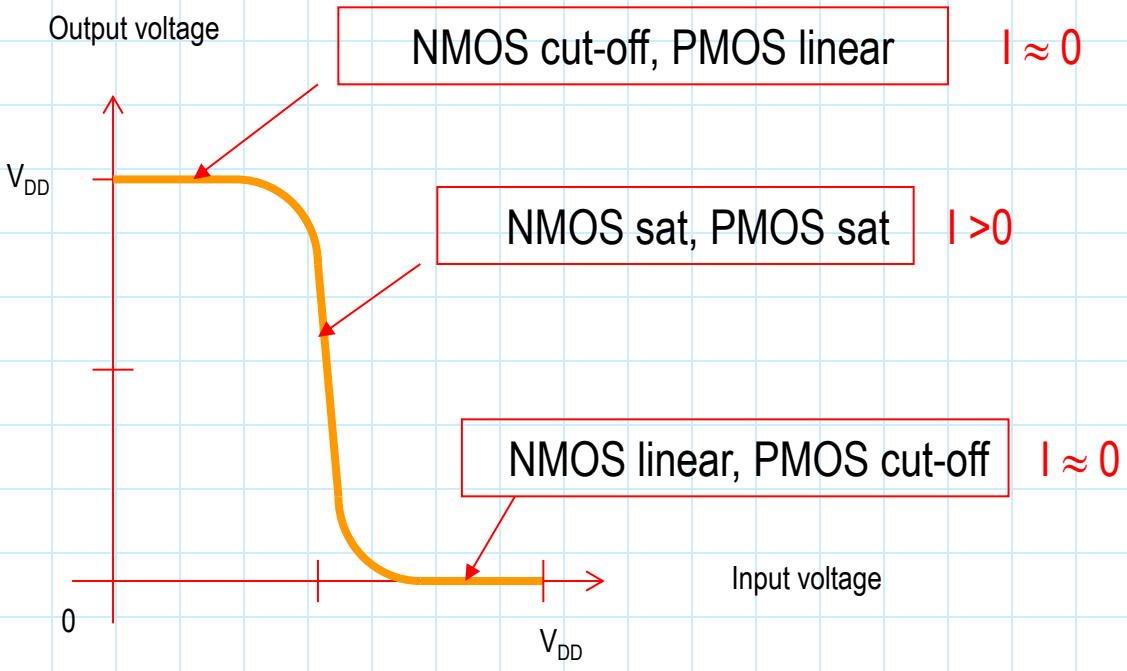
V_{GS1}= 0V -V_{DD}= -V_{DD} < -V_T ⇨ PMOS conducs

V_{GS2}= 0V - 0V = 0V < V_T ⇨ NMOS cut-off

The static consumption is = 0

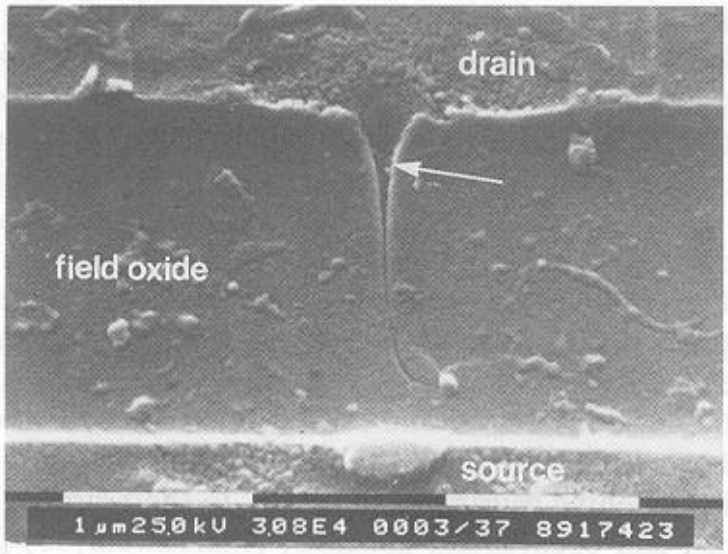
2.5. The CMOS inverter (4)

Transference curve:



2.6. Protection of MOSFET transistors (1)

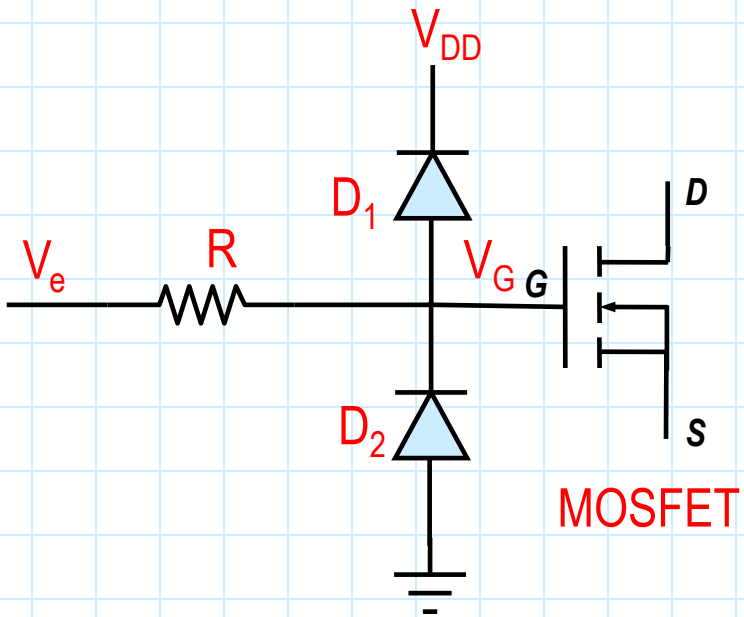
- MOSFET are sensitive to:
  - Overvoltages
  - Overcurrents
  - High electrostatic potentials
  - Radiations
- *thinox* layer: very thin, < 40Å in VLSI (1Å = 0.1 nm)

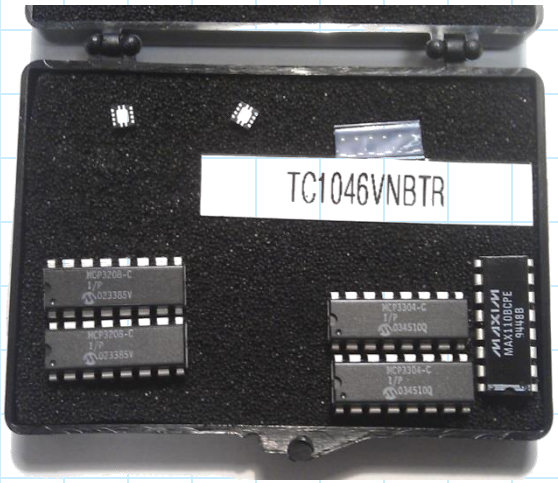


Thinox layer breakdown caused by electrostatic potentials at the gate

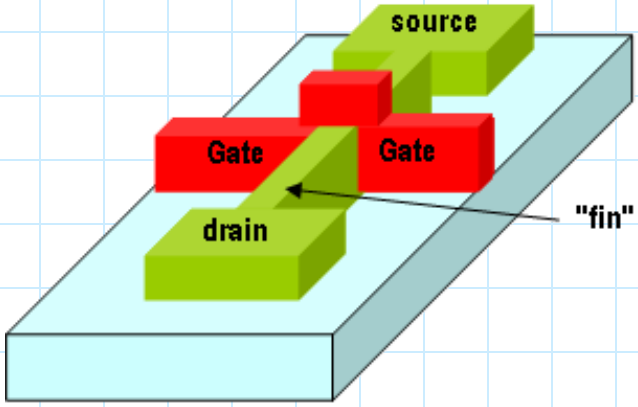
2.6. Protection of MOSFET transistors (2)

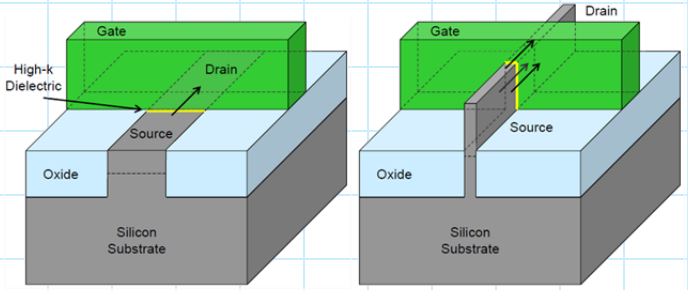
- Precautions when handling MOSFETs :
  - Storage in conducting material
  - Careful human manipulation
  - In operation, connect unused inputs to ground or to V_{DD}.
- Clamping circuits





Latest developments : FinFET, tri-gate





Traditional 3D FinFET

- Higher speed
- Less consuption
- New material for isolators and semiconductors
  - Isolators: HfO_2, ZrO_2, Si_3N_4
  - More mobility in channel, using different materials than Si: InGaAS, ….

2.7 Summary

- We have introduced the features that have made the MOSFET transistor the most important device of the digital age. We have assessed the importance and applications of this transistor.
- We have studied the internal functionement of enhancement MOSFETs, their structure, equations, curves and operating regions .
- We have learn how to solve DC circuits based on one or more MOSFET transistors.
- We know the switching mode of the MOSFETs, the states and the conditions of the transistor in this mode.
- We have introduced the main logic gates based on MOSFETs
- We have studied the basic techniques to protect these devices.