4.2. With respect to the CMOS logic family, indicate which of the following statements is FALSE:

A) The dynamic consumption is linearly dependent on frequency. ✓ $P_D = V_{DD}^2 \cdot C_L \cdot f_i$

B) The BCT gates (BiCMOS) are made only with MOSFET transistors. ✗ TTL as well

C) The subfamily HCT is CMOS, but with TTL-compatible inputs. ✓

D) The noise margins depend linearly on VDD. ✓ $NM \simeq 0.3 V_{DD}$

4.3. A specific computer chip contains 50,000 gates, each one having a zero static power dissipation. In the worst case, the output of each gate has a switching frequency of 200MHz. The total dynamic power dissipation allowed for the chip is 10W. The supply voltage is VDD = 5V. Determine the allowable load for each gate.

$$P_D = V_{DD}^2 \cdot C_L \cdot f_i \qquad C_L = \frac{P_D}{V_{DD}^2 \cdot f_i} = \frac{10}{5^2 \cdot 200 \cdot 10^6}$$

$$C_L = 2pF$$

$$C_L/gate = \frac{2pF}{50.000} = 40fF \quad (40 \cdot 10^{-15} F)$$

4.5. A given CMOS processor has 20M transistors dedicated to combinational and sequential logic and 180M transistors dedicated to the memory. The average activity factor is 0.1 for logic and 0.05 for the memory. If the average capacity per transistor is 1 fF (1 femtofarad = 10^{-15} F), the supply voltage is 1.2V and the clock frequency is 1GHz, calculate the power consumtion.

$P_D = P_{D\,logic} + P_{D\,memory}$;

$P_{D\,logic} = (V_{DD}^2 \cdot C_L \cdot \alpha f)_{logic}$

$= 1.2^2 \cdot (20 \cdot 10^6 \cdot 10^{-15}) \cdot 0.1 \cdot 10^9$

$= 2.88\,W$

$P_{D\,memory} = (V_{DD}^2 \cdot C_L \cdot \alpha \cdot f)_{memory}$

$= 1.2^2 (180 \cdot 10^6 \cdot 10^{-15}) \cdot 0.05 \cdot 10^9$

$= 12.96\,W$

$P_D = 15.84\,W$

UNIT 4. CMOS

4.6 Given the following electrical specifications of a HCMOS gate, powered at +5 V, calculate:

* $V_{IHmin} = 3.15V$, $V_{ILmax} = 1.35V$
* $V_{OHmin} = 3.84V$, $V_{OLmax} = 0.33V$
* $I_{IHmax} = 1\mu A$, $I_{ILmax} = -1\mu A$
* $I_{OHmax} = -4mA$, $I_{[redacted]} = 4mA$ (OL max)
* $I_{CC(typ)} = 2\ \mu A$
* $T_{pd(typ)} = 9$ ns
* Cpd (gate capacity, without load) = 22pF

A) The noise margin
B) The fan-out
C) The dynamic consumption assuming that the inputs switch at an average frequency of 100 MHz and the output is empty (not connected to anything).
D) The static consumption mW
E) The maximum frequency of [redacted] inputs: 12

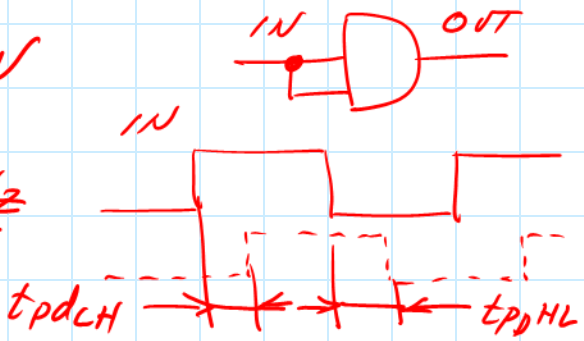
A) $NM = \min[(3.84-3.15), (1.35-0.33)] = 0.69V$

B) $Four = \min\left(\frac{4m}{1\mu}, \frac{4m}{1\mu}\right) = 4000$

C) $P_D = V_{DD}^2 \cdot C_L \cdot f_i = 5^2 \cdot 22 \cdot 10 \cdot 100 \cdot 10^6 = 55mW$

D) $P_E = V_{DD} I_{DD} = V_{DD} I_{cc} = 5 \cdot 2\mu A = 10\mu W$

E) $f_{max} = \frac{1}{t_{PHL} + t_{PLH}} = \frac{1}{2 t_{PD}} = 55MHz$



UNIT 4. CMOS

4.8 Given the transference curve of a standard CMOS inverter:

1. Identify the V_{OH}, V_{OL}, and V_{ilmax} V_{IHmin}
2. Indicate in which area of the curve there is current consumption and of what type.