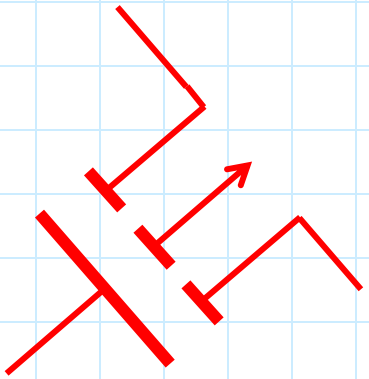
Unit 2: THE MOSFET transistor



Objectives

At the end of this chapter, the student should:

- Know the importance of MOSFET transistors in the development of computers, knowing their characteristics and their relationships with the success of the digital world.
- Know the operating principles of MOSFET transistors, their characteristic curves and operating regions.
- Solve simple DC circuits with one or more transistors.
- Understand MOSFET operation inside basic circuits and digital switching systems.
- Known protection techniques for MOSFETs inputs

Unit 2: Contents

Bibliography

THEORY:

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- A.P. Malvino, D.J. Bates, “Electronic principles”, Mc Graw Hill, 2007.

PROBLEMS:

- G. Benet, J. V. Benlloch, V. Busquets, D. Gil, P. Pérez: “Ejercicios resueltos de Tecnología de Computadores”, 2006.916

2.1 Introduction

FET = *Field Effect Transistor*

Current controlled by an electric field (Voltage Control)

Unipolar device (Only ONE type of carriers ("n" or "p")

Symmetric

JFET (Junction FET), Shockley, 1952

MOSFET (Metal-Oxide-Semiconductor FET)

Kahn y Atalla, 1960

Deplexion

Enhancement (Used in digital apps)

→ N Channel (NMOS Transistor)

→ P Channel (PMOS Transistor)

} Both used in CMOS

2.1 Introduction(2)

- Some advantages:
  - High integration density=> VLSI
  - Versatility: R, C, switch,
  - Low power
  - High input impedance
- Some drawbacks:
  - Slower than BJT
  - Less linearity

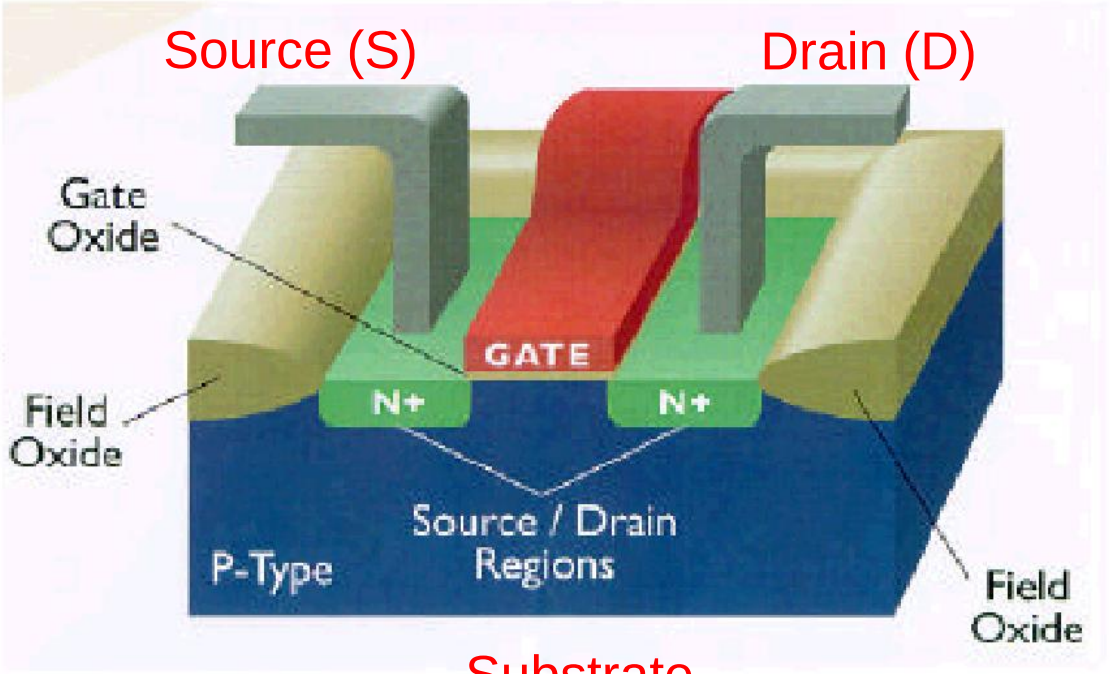
↳ Very Large Scale of Integration (Today 1 billion trans/chip)

$I_S \neq \beta I_G$ (Voltage control)

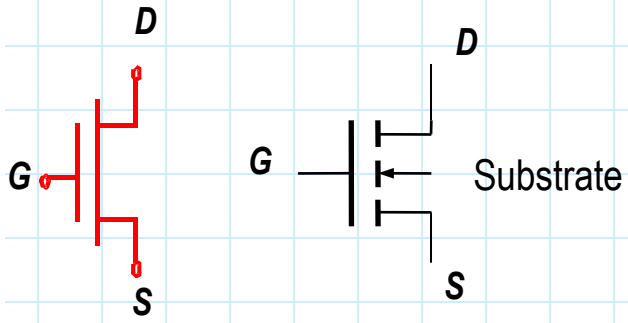
2.2 Basic principles of operation

Internal structure:

N-channel Enhancement MOSFET (NMOS transistor):



Symbols

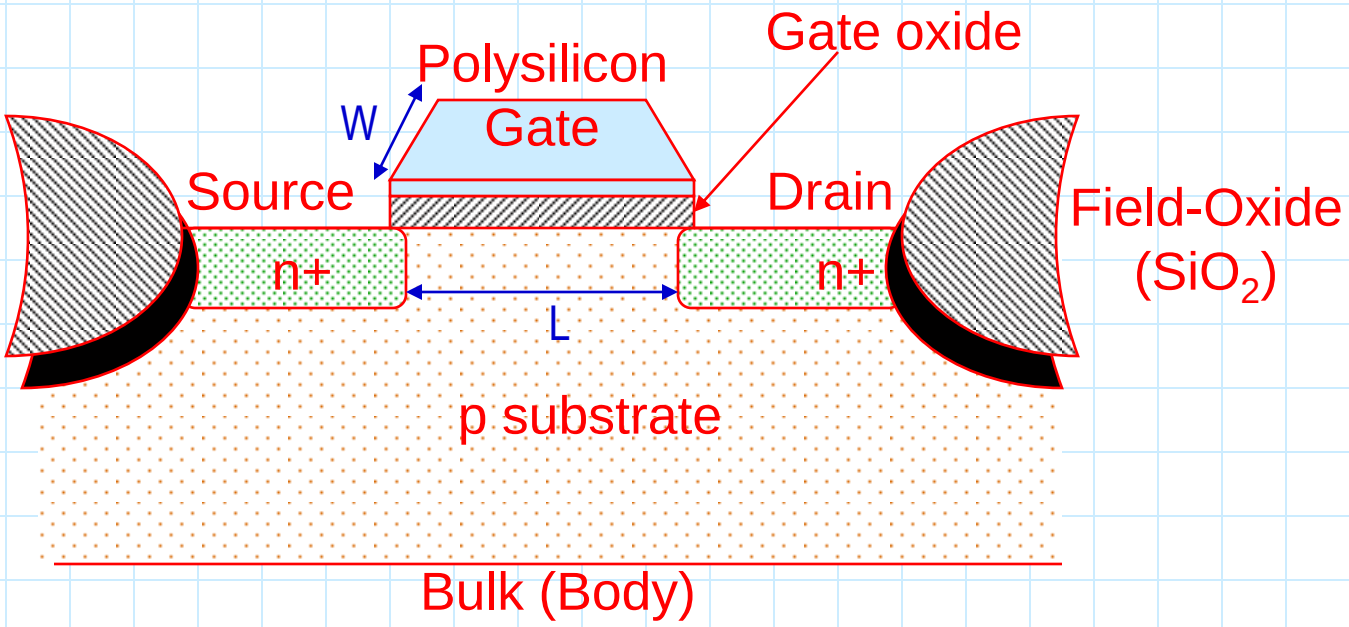


Gate: PolySilicon (High doped Si ⇒ conductor)

Oxide: SiO_2 ⇒ Insulator

NMOS Transistor: cross section

L → Lenght } of channel (45nm / 22nm)
W → Width



Constants:

Transconductance K (mA/V^2) *Pspice: K = (W/L) Kp / 2*

Threshold voltage V_T (V) *Pspice: V_T = vto*

↳ not constant (In bipolar $V_{BE(ON)} = 0.7 = cte$)

$K = \left(\frac{W}{L}\right)\frac{K_p}{2}$; $K_p : \mu C_{ox}$

C_{ox} → gate capacity

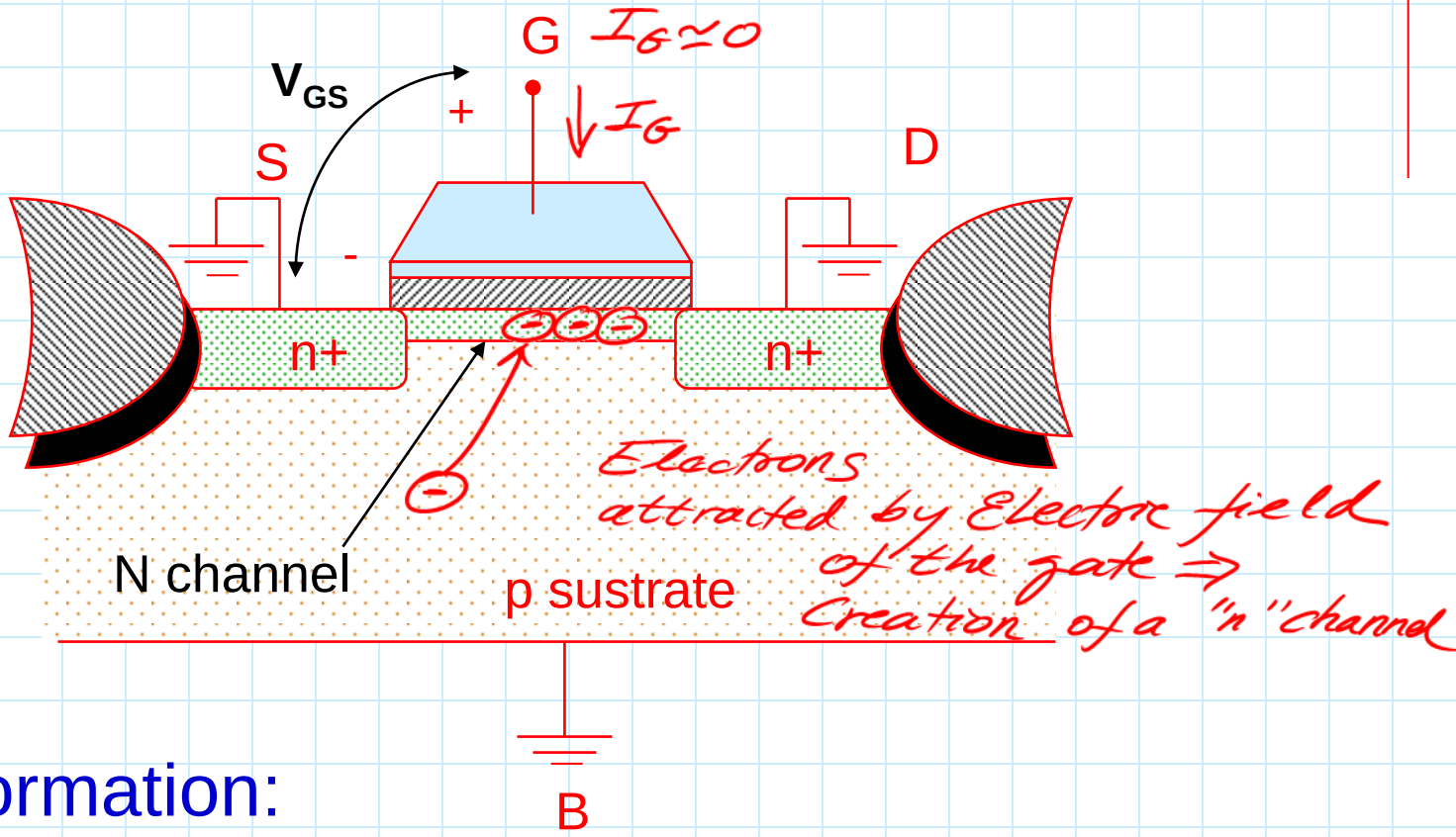
μ → Mobility of carriers

$\mu \begin{cases} \mu_n \rightarrow \text{electrons (n channel)} \\ \mu_p \rightarrow \text{holes (p channel)} \end{cases}$

$\mu_n > \mu_p$; (Si) $\Rightarrow \mu_n \simeq 3\mu_p \Rightarrow$ Smaller (narrower)

"n" channel transistors conducts as much as bigger (wider) "p" channel transistors.

Operating regions: channel formation



Channel formation:

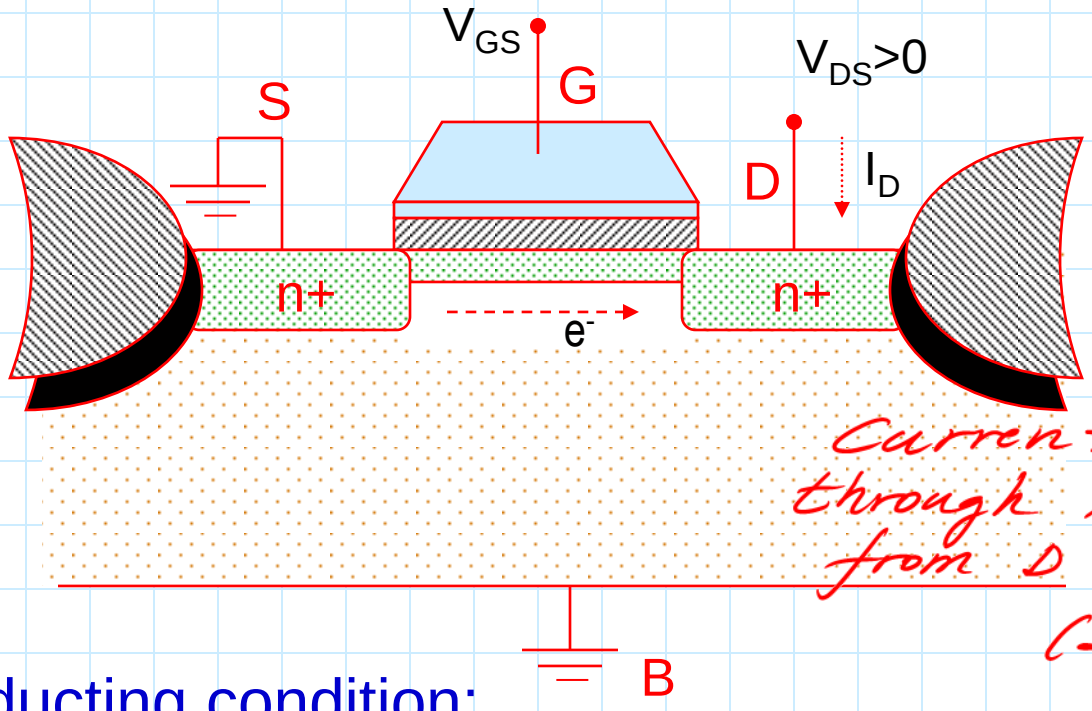
$V_{GS} > V_T$: a N-type channel is formed between S and D

$V_{GS} \leq V_T$: no channel is formed → CUT-OFF

Operating regions : linear region

↳ ohmic

Assuming $V_{GS} > V_T$:



Current flows through the channel from D to S ($I_{DS} = -I_D$)

Conducting condition:

$V_{DS} > 0 \rightarrow I_{DS} > 0$

Working principles: linear region (2)

Condition: $V_{DS} \leq V_{GS} - V_T$

V/I function: $I_D = K\,[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$

(I_{DS})

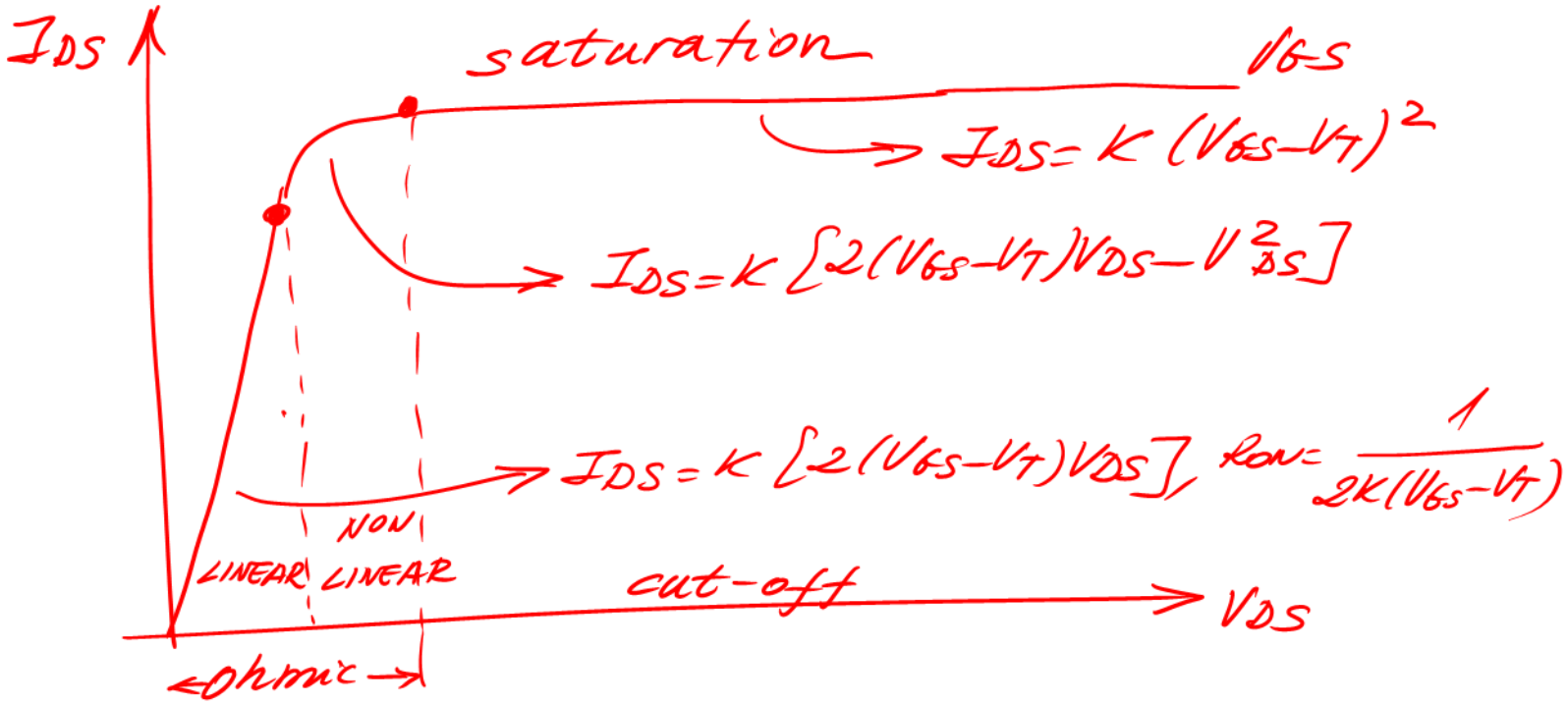
For small V_{DS}:

$$I_D \approx K\,[2\,(V_{GS}\text{-}V_T)\,V_{DS}\,]$$

$R_{DS} = \frac{V_{DS}}{I_{DS}}$

$$R_{DS(on)} = R_{ON} \approx \frac{1}{2 \cdot K(V_{GS} - V_T)}$$

The MOSFET resistance decreases when K and V_{GS} increase


I_{DS}
saturation
V_{GS}
$I_{DS} = K(V_{GS} - V_T)^2$
$I_{DS} = K[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$
$I_{DS} = K[2(V_{GS} - V_T)V_{DS}]$, $R_{ON} = \frac{1}{2K(V_{GS} - V_T)}$
NON LINEAR
LINEAR
cut-off
V_{DS}
ohmic