1- MOSFET´s theory

1.1 What of the following statements on the MOSFET transistor is FALSE?

[A] It has an insulated gate made by a thin SiO_2 layer
[B] In the ohmic region, the transistor is equivalent to a resistance that increases if $|VGS|$ increases
[C] In the saturation region, the current increases on a quadratic law with $|VGS|$
[D] The PMOS transistor is slower than the NMOS.

1.2 Indicate the FALSE statement among the following related to a P channel enhancement Mosfet, and assuming the threshold voltage VT in absolute value,

[A] The substrate is of N type.
[B] The channel formation is obtained with voltages VGS <-VT
[C] The transistor operates in linear or ohmic region when VDS <VGS + VT
[D] It is slower than the NMOS because the mobility of the holes is smaller than the electrons.

1.3 Indicate the FALSE statement among the following related to the enhancement MOSFET:

[A] It has an insulated gate.
[B] It is a unipolar and symmetrical device.
[C] In linear region, it works as a variable resistor dependent on the gate-source voltage VGS.
[D] In the saturation region, the current has a linear dependence on gate-source voltage VGS.

1.4 What of the following statements on the MOSFET transistor is FALSE?

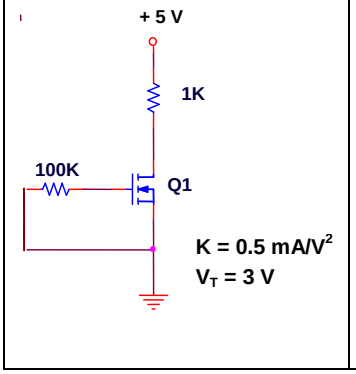
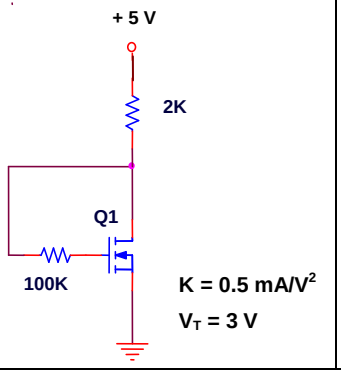
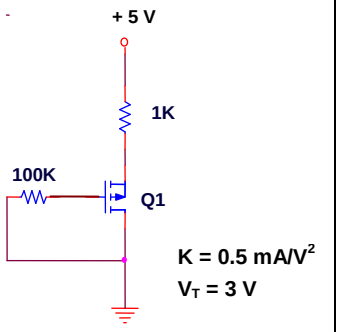
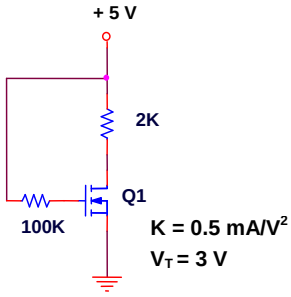
[A] The gate current I_G is always zero since it is isolated..
[B] An N-channel MOSFET will be saturated when $V_{DS} < (V_{GS}-V_T)$
[C] I_{DS} will be constant for a given V_{GS}in the saturation zone, though V_{DS} be variable.
[D] In the ohmic region, for low values of V_{DS}, the MOSFET behaves like a resistor dependent on a voltage V_{GS}.

1.5 Which of the following statements about the N-channel accumulation MOSFET transistor N is FALSE?

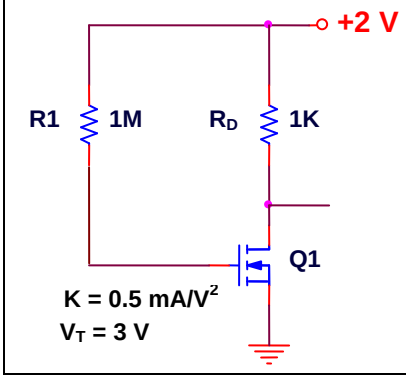
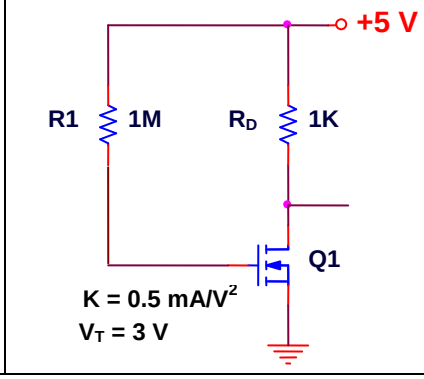
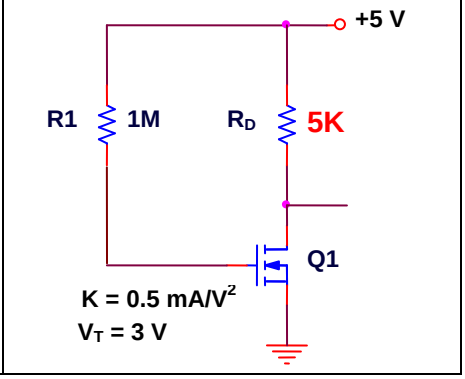
[A] The source and drain are highly doped N-type semiconductor regions, while the substrate is a P-type semiconductor.
[B] The gate is attached to a very thin insulator layer, which justifies the current through this terminal is considered null. ($I_G = 0$).
[C] If one terminal of a MOSFET transistor which is conducting (ON) (IDS> 0) is connected to substrate, we can assure that this terminal is the drain.
[D] One MOSFET transistor which is conducting (ON) (IDS> 0), can behave as a resistor (in ohmic /linear region) or as a current source (saturation).

2- OPERATING REGIONS

2.1 Indicate the operating region of the MOSFET transistors of the following circuits:

A	B	C	D
			

2.2 Indicate the operating region of the MOSFET transistors of the following circuits:

A	B	C
		

2.3 Which of these transistors work in saturation? Suppose for all of them:K = 0.25 mA/V^2, |VT| = 1 V:

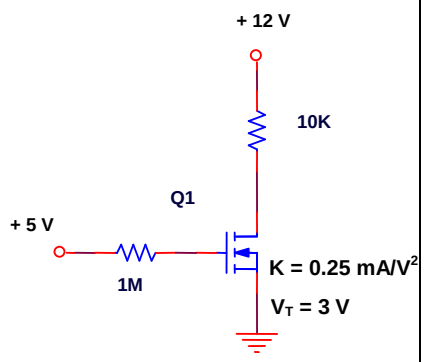
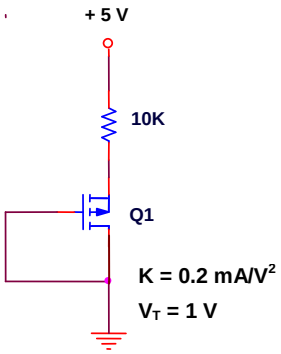
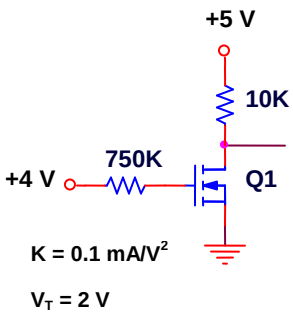
[A] NMOS: V_{DS} = 5 V, V_{GS} = 0 V
[B] PMOS: V_{DS} = -1 V, V_{GS} = -3 V
[C] PMOS: V_{DS} = -4 V, V_{GS} = -4 V
[D] NMOS: V_{DS} = 5 V, V_{GS} = 7 V

2.4 In saturation region of a P channel enhancement MOSFET, can be stated that: (May 2012):

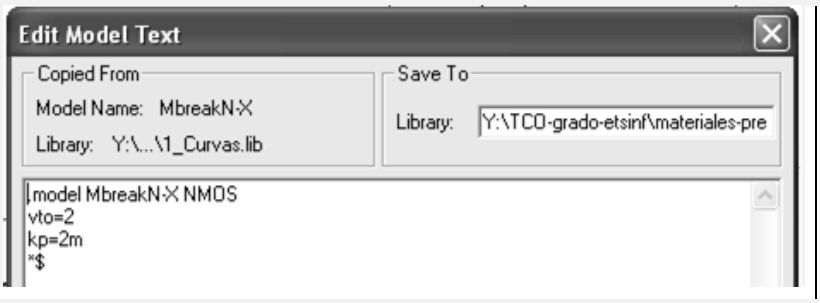
[A] V_{GS} is negative, V_{DS} is positive and I_{DS} is negative
[B] V_{GS} ks positive, V_{DS} is positive and I_{DS} is negative
[C] V_{GS} ks negative, V_{DS} ks negative and I_{DS} is negative
[D] I_{DS} is always null, as in these type of transistors the channel can not be formed.

3- OPERATING POINT

3.1 Analyze the operating point Q (V_{GS}, I_{DS}, V_{DS}) of the MOSFETs of the following circuits:

A	B	C
		

In addition to theoretical analysis, simulate using PSpice all circuits. Use the parts: ***VDC, EGND, r, MbreakN3 y MbreakP3****. Double click on MOSFET symbol and fix:* ***L = 1u, W = 2u****.*

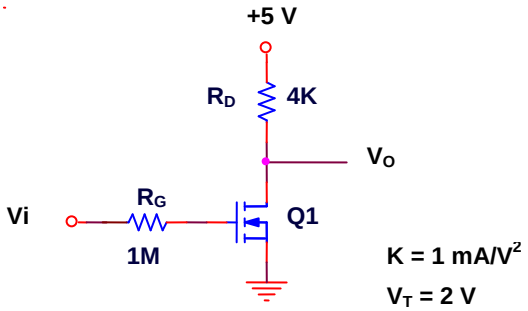


To specify VT and K, click first on NMOS symbol (it turns red), and then on the menu ***Edit/Model/Edit Instance Model (Text)****. Insert two lines for* ***vto*** *and* ***kp,*** *as seen on figure.* V_T *is represented in PSpidce as Vto, and the relationship among K and Kp is:* ***K = (W/L) Kp/2.*** *Using the previous W and L values, K = Kp.*

*Simulate the bias point: (****Analisys/Setup/Bias Point Detail****).*
Next, use the command ***Analysis/simulate (F11)*** *to start the simulation, and activate the V and R buttons to display all currents and voltages in the circuit.*
This type of simulation is particularly suitable for static analysis of any circuit, and allows us to observe the behavior of circuit when we change voltages, resistances, or transistor parameters. It is also highly recommended to simulate other circuits of this set of exercises.

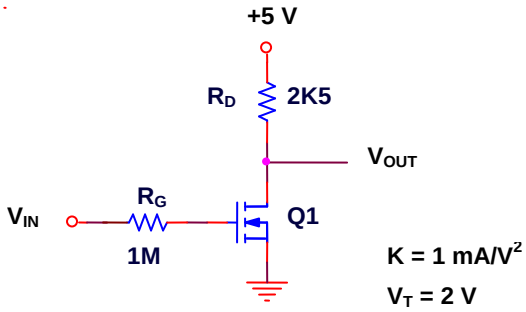
3.2 Determine the input voltage in the circuit of the figure, if the output is 4V.

[A] Ve = 1.5V
[B] Ve = 2V
[C] Ve = 2.25V
[D] Ve = 2.5V



3.3 In the circuit of the figure, what value of V_{IN} will cause the transistor works on the boundary between the saturation and ohmic regions?

[A] V_{IN} = 3.54 V.
[B] V_{IN} = 3.23 V.
[C] V_{IN} = 2.86 V.
[D] None of the above answers is true. If the transistor conducts, it will always be saturated.

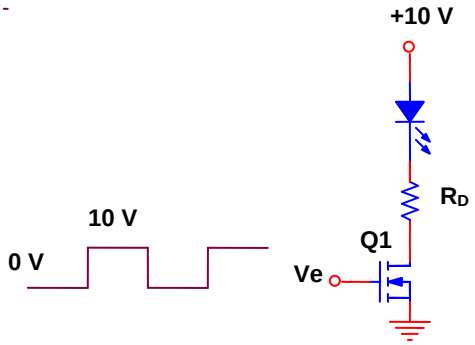


3.4 Calculate the value of R_D In the circuit of the figure, if LED brights with a current I_{LED} of 20mA. Assume that when the MOSFET is ON, it is in linear or ohmic region.

[A] RD = 500 kΩ
[B] RD = 500 Ω
[C] RD = 353 Ω
[D] RD = 2.2 kΩ

Data LED:
I_{LED} = 20mA
V_{LED} = 1.7 V

Data Mosfet:
V_T = 2 V
K = 1 mA/V2
Linear region -> $I_{DS} = 2K (V_{GS} - V_T)V_{DS}$



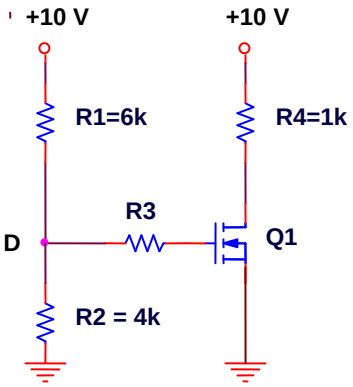
3.5 In the following circuit:

Transistor:

Sat:$I_{DS} = K (V_{GS} - V_T)^2$

Ohmic: $I_{DS} = 2K (V_{GS} - V_T)V_{DS}$

V_T = 2 V
K =1 mA/V^2



[A] Calculate the voltaje in D
[B] Calculate the quiescent point Q (V_{GS}, I_{DS}, V_{DS})
[C] Recalculate the value of resistor R4 to place the quiescent point of the circuit on the boundary between saturation and ohmic region.

3.6 The MOS transistor in the circuit of Figure B has a characteristic curve as shown in Figure A. Answer the following questions.

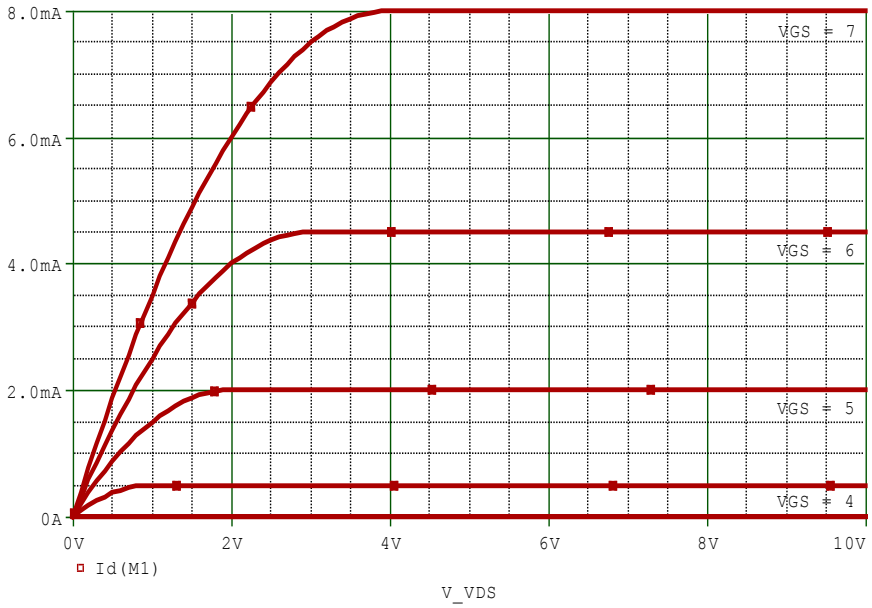


Figure A

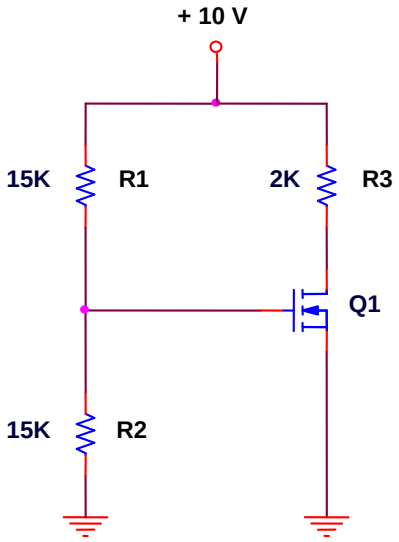


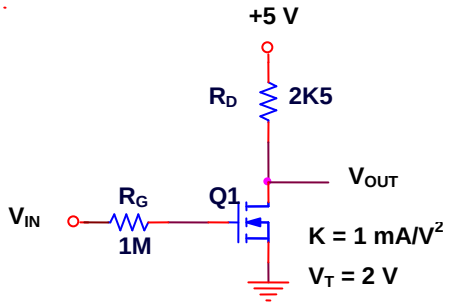
Figure B

QUESTIONS	ANSWERS
1. Indicate the type of transistor:	
2. V_T value	(Volts)
3. K value	(mA/V^2)
4. Obtain thevoltage V_{GS}in the circuit.	(Volts)
5. Obtain the current I_D.	(mA)
6. Obtain the voltage V_{DS}.	(Volts)
7. ¿What is the limit value of $R_3$to puttheMOSFET in the ohmic region?	(kΩ)

In addition to theoretical analysis, simulate the circuit using PSpice. See indications on exercise 3.1. To generate the characteristic drain curves as shown in the figure, see Laboratory 4. Use the parts: ***VDC, EGND, r, MbreakN3*** *and perform a simulation of the bias point (****Bias Point Detail****).*

3.7 Obtain the quiescent point Q (V_{DS}, I_{DS}) of the following transistor when V_{IN}= 3V

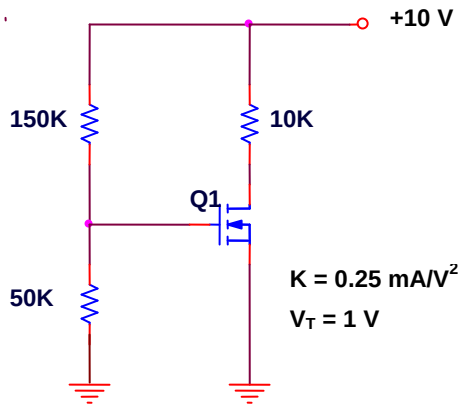
[A] V_{DS} = 1.5 V, I_{DS} = 1.4 mA.
[B] V_{DS} = 3 V, I_{DS} = 0.8 mA.
[C] V_{DS} = 2.5 V, I_{DS} = 1 mA.
[D] V_{DS} = 0.2 V, I_{DS} = 1.92 mA.



In addition to theoretical analysis, simulate using PSpice the circuit. Use the parts: ***VDC, EGND, r, MbreakN3****. Double click on MOSFET symbol and fix:* ***L = 1u, W = 2u****. To specify VT and K, see exercise 3.1.* ***Vo*** *is just a label, do not place any* ***VDC*** *at that point.*
Specificity ***DC Sweep*** *simulation in* ***Analysis / Setup****. We will generate on this way the transference curve Vo = f (Vi) of the circuit. To do so, select Vi as sweep variable, and define a variation between 0 and 5V, with 0.01V increments.*
Next, use the ***Analysis / Simulate*** *(F11) command to start the simulation. PROBE is activated and using* ***Trace / Add trace*** *command (Insert), select the output voltage. The output is connected at the drain of the transistor, then a is a way to specify the output is V (M1: d) where M1 is the name of the transistor.*
This type of simulation is particularly suitable for digital gates, which have inputs and outputs. It is also highly recommended to simulate other circuits of this set of exercises. See Laboratories 4 and 5 as references.

3.8 The quiescent point of the transistor of the following circuit is:

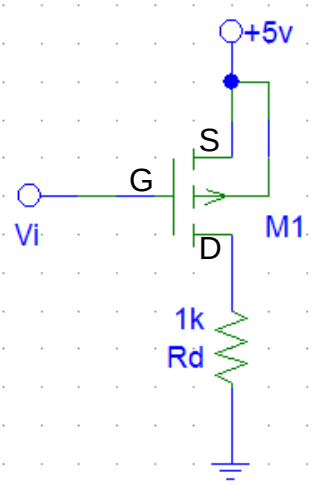
[A] V_{GS} = 2.5 V, V_{DS} = 5 V, I_{DS} = 1 mA.
[B] V_{GS} = 2.5 V, V_{DS} = 4.4 V, I_{DS} = 0.56 mA.
[C] V_{GS} = 5 V, V_{DS} = 4.5 V, I_{DS} = 1.5 mA.
[D] V_{GS} = 1 V, V_{DS} = 10 V, I_{DS} = 0 mA.



3.9. Indicate the CORRECT answer among the following related to the bias circuit of a PMOS transistor shown in the figure:

[A] If Vi = 0, the transistor is in cut-off.
[B] If Vi = 2V, the transistor is in saturation.
[C] If Vi = 2V, the transistor is in ohmic region.
[D] For Vi = 2V, VGS = 2V

Data: V_T = 1V, K = 0.5 mA/V^2

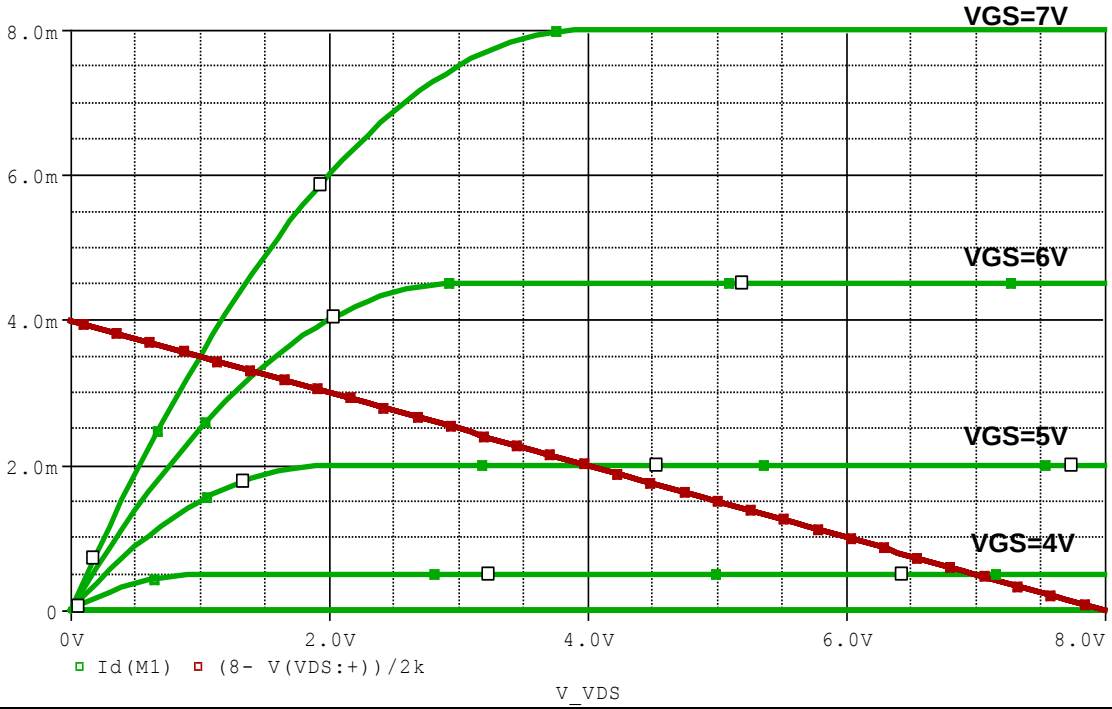


Additional work: Obtain the Q point for the following Vi values: 5V, 4V, 3V, 0V, and obtain also the operating region in each case.

4-LOAD LINE

4.1 The figure includes both the characteristic curves of an NMOS transistor and the load line of the biasing circuit. Complete the following table.

PREGUNTAS	RESPUESTAS
1. Indicate the type of transistor:	
2. $V_T$value	(Volts)
3. K value	(mA/V^2)
4. Obtain V_{DD}.	(Volts)
5. Obtain R_D.	(kΩ)
6. Determine V_{DS} and I_{DS} indicating the working region for V_{GS} = 5V	(Volts) (mA)
7. Determine V_{DS} e I_{DS} e indicating the working region for V_{GS} = 6V	



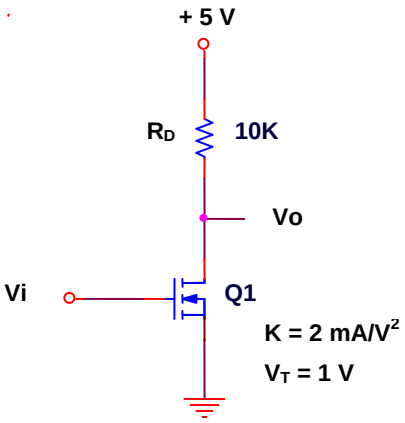
4.2 Taking into account the previous figure:

a) If V_{GS} = 7V, what value of R_D makes VDS equal to 2V?
b) If V_{GS} = 5V and R_D=1K, what value of VDD puts the transistor among ohmic and saturation regions?
c) If V_{DD} = 3V and R_D=0.5K, from what value of V_{GS} is reached IDS = 2mA?
d) If V_{DD} = 3V and V_{GS} = 6V, can be achieved the saturation region for any value of R_D?
e) [Switching] If V_{DD} = 5V and R_D=0.5K, ¿could the circuit behave as an inverter with a control voltage of V_{GS} = 0V for a "0" and V_{GS} = 5V for a "1"?. What will be the output (V_{DS}) for each case?
f) In the case of the load line drawn in figure, which is the dissipated power of the MOSFET and the output resistor for V_{GS} = 5? And for V_{GS} = 4V?

5- SWITCHING

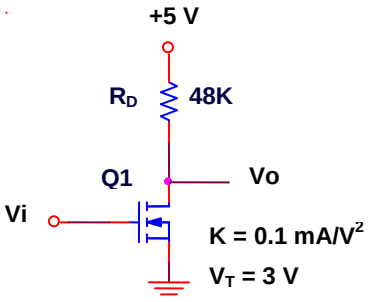
5.1 Indicate the output voltage levels of the logic inverter of figure if Vi is a square wave with values from 0V to 5V. Use the approximate expression for the ohmic region of transistor: $I_{DS} \approx 2K(V_{GS}-V_T)V_{DS}$.

[A] 5 V y 1 V
[B] 5 V y 0.03 V
[C] 5 V y 0.5 V
[D] 2.5 V y 0.5 V



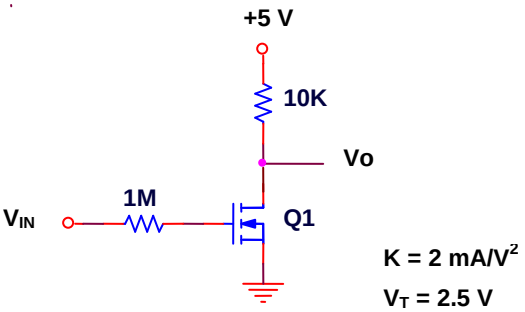
5.2 Obtain the minimum and maximum voltage levels of output Vo in the logic inverter of figure, if Vi is a square wave with minimum and maximum values of 0V and 5V.[Assume that in the ohmic region, the $R_{DS\ (ON)}$ of MOSFET can be approximated by $R_{DS(ON)} \approx 1/(2K(V_{GS}-V_T))$]

[A] 5V y 0.05V
[B] 5V y 0.2V
[C] 5V y 0.5V
[D] 2.5V y 0.5V



5.3 From the following NMOS inverter circuit:

[A] Get the equivalent R_{ON} of the transistor with a high level input (Vi = 5V). Use the simplified expression of the resistive (ohmic) zone.
[B] Obtain V_{GS}, I_{DS}, V_{DS} and V_O with the input to high level (V_i = 5V)
[C] Obtain V_{GS}, I_{DS}, $V_{DS}$and V_O with the input to low level (V_i = 0V)
[D] We want to improve the output voltage at low level, so that is less than or equal to0.1V. Calculate the new value of the drain resistance
[E] Get the range of values of Vi that the inverter considers to be “0”. Consider $V_{OH(MIN)}$ = 4.5V and the R value obtained in [D]
[F] Get the range of values of Vi that the inverter considers to be "1. " Consider $V_{OL(MAX)}$= 0.5V and the R obtained in [D].



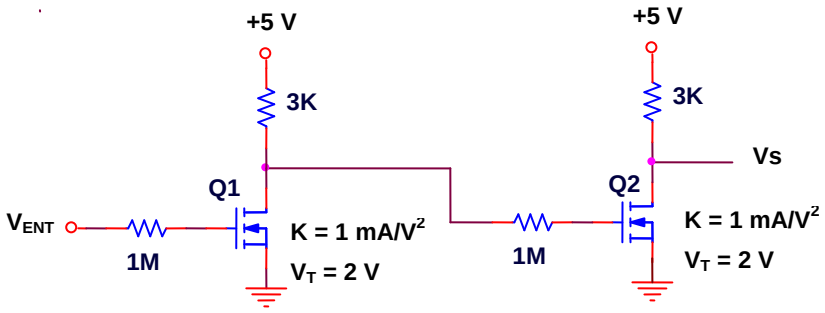
5.4 Given the following non-inverting gate built from two identical NMOS inverter circuits, indicate the values obtained at the output from an input consisting of a pulse train varying from 0V to 5V (low to high logic levels). Use the approximate expression for the ohmic region: $I_{DS}=2K(V_{GS}-V_T)V_{DS}$

[A] 0V and 5V.

[B] 0.26V and5V.

[C] 0.35V and 5V.

[D] 0.1V and 5.5V.

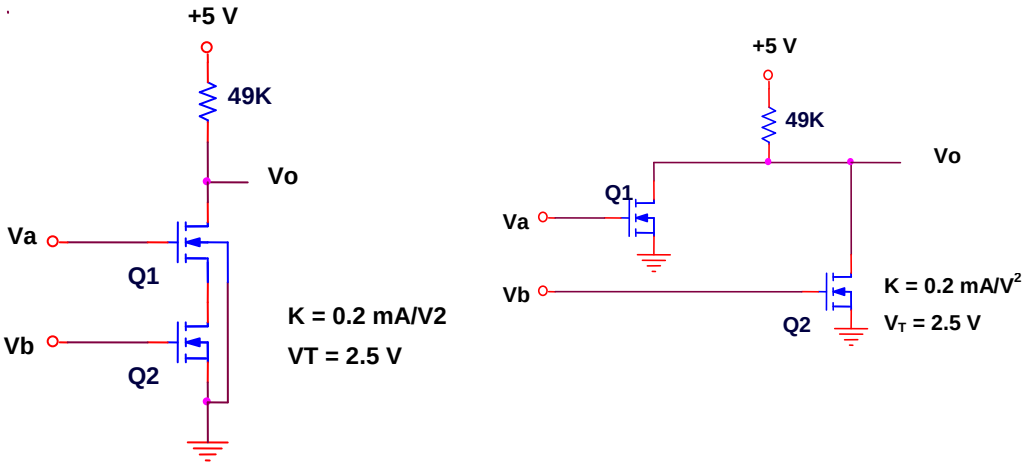


5.5 The following circuits are two-input NMOS gates.

Note: For the left circuit, do the calculations for one or two transistors conducting. Use the simplified expression for the ohmic region $R_{DS(ON)}$.

[A] ¿Which type of logic gates are?

[B] Obtainthe $V_O$voltage for each output state. Assume 5Vas high input level and 0V as low level.



*In addition to theoretical analysis, simulate the circuit using PSpice. Use the parts: **VDC, EGND, r, MbreakN3**. Double click on MOSFET symbol and fix: **L = 1u, W = 2u**. To specify VT and K, see exercise 3.1. **Vo** is just a label, do not place any **VDC** at that point.*

*We will replace the DC source **VDC** of inputs (Va y Vb) for a source of type **VPULSE**. Specify the following parameters:*

V1 = 0V (low level)	*TF = 2n (fall time)*
V2 = 5V (high level)	*PW = 40n (high level duration-pulse widht)*
TD = 10n for Va and 30n for Vb (initial delay time)	*PER = 100n (period time)*
TR = 2n (rise time)	*Do not modify the rest of parameters*

*Put two separate voltage markers **(Voltage / Level Marker)** at the input and the output.*
*Select **Transient** simulation type and disable **DC Sweep**, using the **Analysis / Setup / Transient** menu.*
*In Transient window, indicate Print **step** = 1n, **Final time** = 120n.*
Simulate and observe all combinations of input and output values.
This type of simulation is particularly suitable for digital gates, which have inputs and outputs. It is also highly recommended to simulate other circuits of this set of exercises. See Laboratory 5 as reference.

5.6 Given that the input voltage (V_{IN}) is 10 V for both transistors, indicate which of the following statements regarding the output voltage (V_{OUT}) is TRUE:

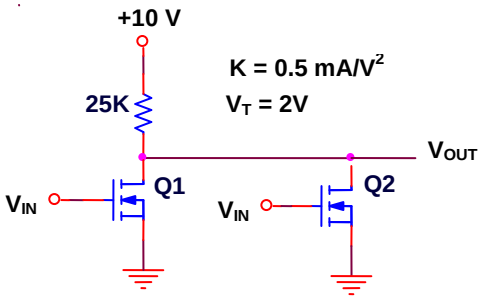
Note. In the ohmic region, use the expression:$I_{DS} = 2K(V_{GS} – V_T) V_{DS}$, and in saturation: $I_{DS} = K(V_{GS} – V_T)^2$.

[A] Both transistors are cut-off, then$V_{OUT} \approx 0.025V$ (due to leackage currents)

[B] Both transistros are ON, then$V_{OUT} \approx 0.025$ V.

[C] The transistors make an wired AND in this circuit, then $V_{OUT} \approx 10$ V (alogic “1”).

[D] It is not recommended to make the connection shown, as the output value is indeterminate.

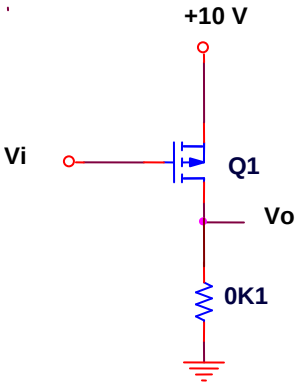


5.7 Given the switch of the figure, with a control input Vi which is a square wave varyingbetween 0 and V_{DD}, answer the following questions:

[A] Considering the transistor as a voltage-controlled variable resistor, calculate its resistance value when closed, so that the value of the output voltage is 0.01 V.

[B] If $V_T$of transistor is 2 V, find the value of K of the transistor. To do so, consider that in the ohmic region (also called linear region) the current value I_{DS} can be approximated by the following expression:

$$I_{SD} \approx K [2 (V_{GS}+V_T) V_{DS}].$$



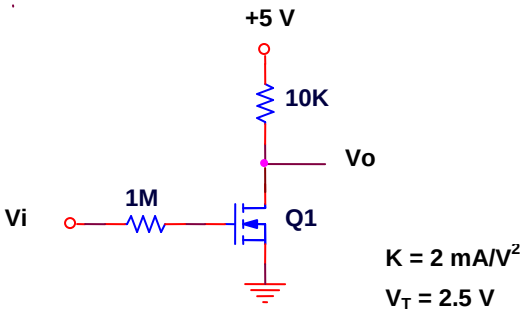
5.8 Design a NMOS inverter with a pull-up resistor R_D,with the following requirements:

- Static power consumption when the output is low = 0.10 mW
- $V_{OL} = 0.5V$
- $V_{OH} = V_{DD} = 5V$
- Transistor: $V_T = 1V$

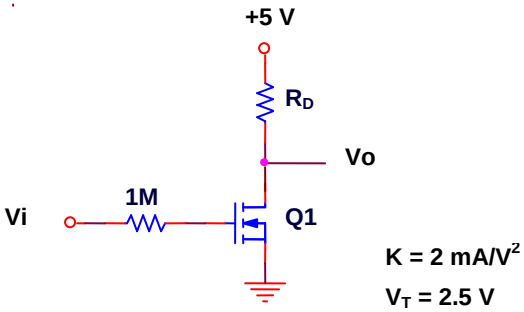
Obtain $R_D$and K of transistor.

5.9 Indicate how the value of R_D affects in the parameters of power consumption, occupied area, logic levels and speed, of NMOS logic circuits.

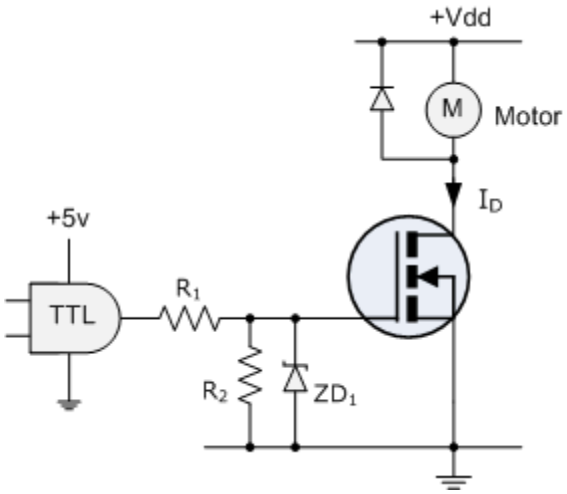
5.10 From the following NMOS inverter circuit: Calculate the limit values of the input voltage Vi to make the transistor working in switching mode: Vi between cut-off and saturation and Vi between saturation and ohmic region. Note: in this second point, we recommend using the saturation equation .



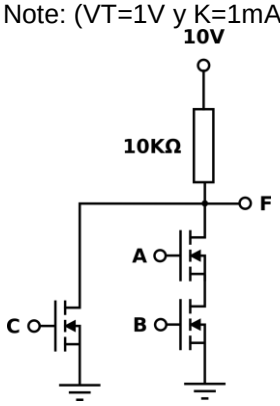
5.11 From the following NMOS inverter: Obtain the value of R_D, in order to reach the ohmic region from saturation region, when Vi = 4V. Note: We recommend using the saturation equation.



5.12 In a small robot we want to control the wheel motors with a TTL logic circuit (0V and 5V levels). As the electrical motor consumes more current than the gates are capable to supply, the following circuit with a power MOSFET is added to supply the motor. The motor voltage is 12V and it consumes 60mA. R_1, R_2 and Zener diode ZD_1 form a limitation circuit (optional), as far as the gate of the MOSFET reach only a voltage from 0V and 5V from TTL gate. Remember that the current in the gate is IG = 0. What output level of the TTL gate starts the engine?. Calculate the MOSFET R_{ON}. Calculate the power dissipated by the motor and the MOSFET when the TTL output is 0V and when is 5V. Data: V_T = 1 V, K = 5 mA/V^2, Vdd = 13.5V



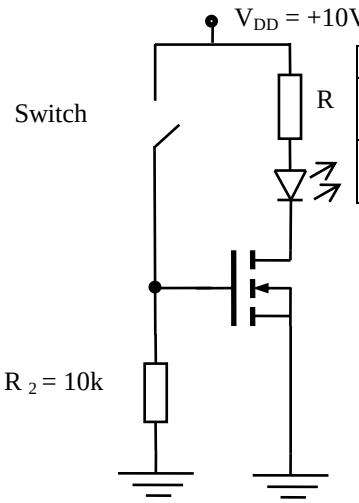
5.13 Given the following circuit, indicate the CORRECT answer. (May 2012)
Note: (VT=1V y K=1mA/V2)



[E] The logical function is: F(A,B,C)=(A+B)·C
[F] This is a 3-input XOR.
[G] The logical function is: F(A,B,C)=A+(B·C)
[H] If the inputs are C=0V, B=10V and A=0V, the output F is 10V.

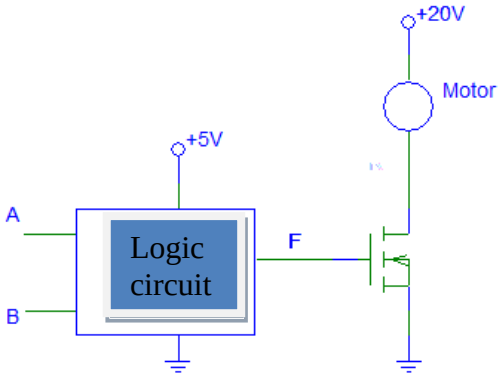
5.14 The following circuit turns on a LED using a switch. Complete the table and calculate the resistance of R for a suitable brightness of the LED. Justify the answer. (Note: It is recommended to replace the transistor in linear region with its equivalent resistance, Ron. After that, check that the transistor operates in linear region). (June 2012).

Data LED: I_{LED}= 10mA, V_{LED}=1.5V
Data Mosfet: V_T=3V, K=1mA/V^2



Switch	V_{GS}	I_{DS}	LED (ON/OFF)
Open			
Closed			

5.15 We want to control an electric motor using a given logic circuit, as shown in the figure. The motor works with a voltage of 18V and a current of 60mA. The Mosfet parameters are: V_T = 0.5 V, K = 0.1 mA/V^2



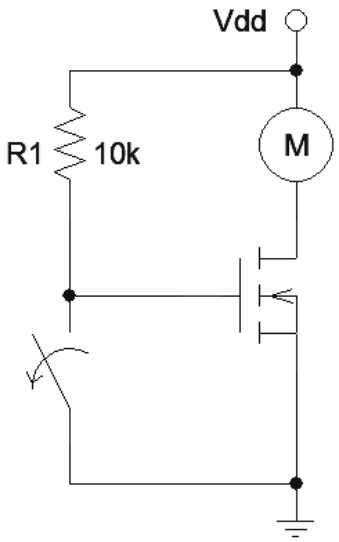
Fill the following table (justify the calculations):

F	Motor (ON/OFF)	Power consumed for the motor (mW)	Power disipated in the transistor (mW)
"0"			
"1"			

Indicate the value of Ron of the transistor:

5.16 We want to use a MOSFET as a control switch for controlling a small electric motor, as shown in figure. VDD = 8V. The motor works with 7.5V and 2mA. The MOSFET conducts in ohmic zone. Fill the following table, justifying analytically the answers.

If we want the motor to be ON, what is the positon of the control switch (open or closed)?:_____
Justify your answer.

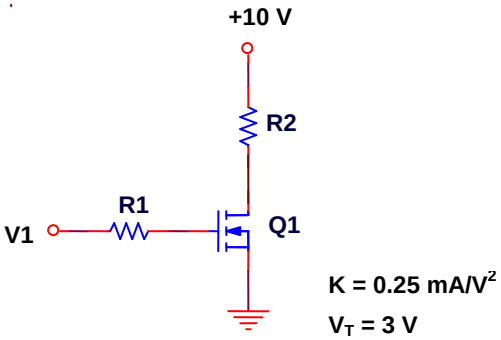


VDS	V
IDS	mA
RON (MOSFET)	kΩ
Power consumed by the motor: PMOTOR = Vmotor Imotor	mW
Power consumed by the MOSFET: PMOSFET= VDS IDS	mW

6-PROBLEMS

6.1 The following circuit uses a MOSFET whose data are shown. Knowing that R2=10kΩ and R1= 1MΩ, is requested:

Note: In ohmic región, use the expression: $I_{DS} = 2K(V_{GS} - V_T)\,V_{DS}$, and in saturation: $I_{DS} = K(V_{GS} - V_T)^2$.



[A] (0.5p) Calculate the operating point of the transistor when the input voltage is V1 = 4V.

Answer:	V_{GSQ} =	V_{DSQ} =	I_{DSQ} =

[B] (0.5p) Calculate the operating point of the transistor when the input voltage is V1=6V.

Answer:	V_{GSQ} =	V_{DSQ} =	I_{DSQ} =

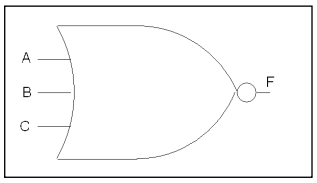
6.2 We want to design a 3-input NOR gate with NMOS transistors and other additional elements:

Parameters of the NMOS transistors: K=0.5 mA/V^2 , V_T=3V
Power supply of the logic gate: V_{DD} = 5V

Assume the following input voltage values: "0" = 0V, "1" = 5V

Note : In ohmic region, use the expression: $I_{DS} \approx 2K(V_{GS} - V_T) V_{DS}$, and in saturation region: $I_{DS} = K(V_{GS} - V_T)^2$

a)) Draw the circuit with transistors and the truth table (with "1"s and "0"s) of the gate. **[0.5P]**



b) Calculate the voltage in F when A=B=C="0". **[0.5P]**

- Justify the operating region of transistors.
- Justify the voltage in F.
- Justify the currents of transistors.

c) Calculate the voltage in F when A="1", B=C="0". Consider R_D = 4k. **[0.5P]**

- Justify the operating region of transistors.
- Justify the voltage in F.
- Justify the currents of transistors.

d) Design R_D for $V_{OL} \leq 0.25V$. **[0.5P]**

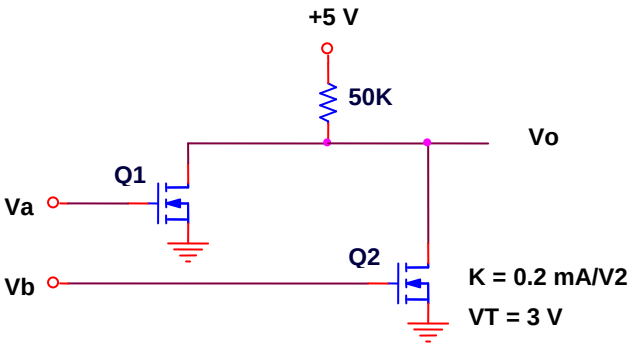
Assume at the beginning one transistor conducting.
¿How does V_{OL}vary when more than one transistor is conducting? Obtain the new V_{OL}

6.3 The circuit of the figure is a simple MOSFET transistor-based logic gate. It is requested:

Data:

Sat: $I_{DS} = K (V_{GS} - V_T)^2$

Ohmic: $I_{DS} = 2K (V_{GS} - V_T)V_{DS}$



[A] Calculate the value of the output voltage Vo when Va = 3.5V and Vb = 0.5V, and the state of each transistor (Justify the answer).

Vo =	
M1 region:	
M2 region:	

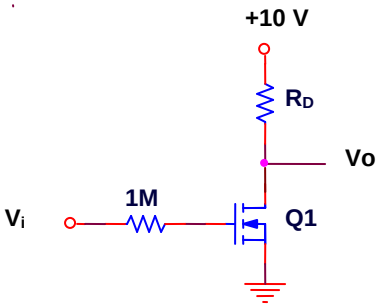
[B] If Vb = 0V and the output Vo = 0.2V, what is the value of the input voltage that produces this output voltage? (Assume transistor M1 in ohmic region, and calculate the equivalent resistance value of transistor $R_{DS(ON)}$)

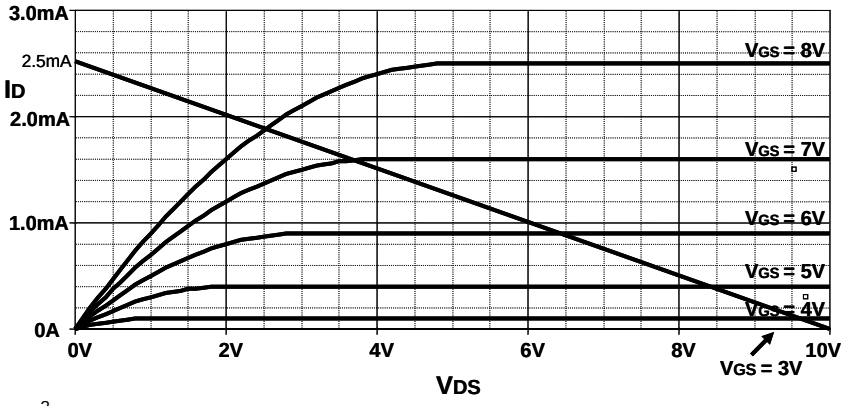
R_{DSON} =	
Va =	

[C] As already mentioned, the circuit corresponds to a logic gate. Indicate the logic function of the output Vo in terms of inputs Va and Vb, and the logic family to which it belongs..

Logic function:	
Logic Family: (TTL, CMOS, NMOS o PMOS)	

6.4 For the transistor circuit of the figure and the attached graph withthe load line, it is requested:





Saturation region equation: $I_D=K\,(V_{GS}-V_T)^2$
Ohmic region equation: $I_D = K\,[2(V_{GS} – V_T)V_{DS} – V_{DS}^2]$
Simplified ohmic region equation: $I_D=2K\,(V_{GS}-V_T)\,V_{DS}$

[A] Obtain the value of VT and K parameters of the MOSFET.

[B] What is the value of the resistance RD of the circuit? Justify your answer. (Hint: Use the load line)

[C] Derive analytically the value of the drain current ID for a Vent = 6.5V and indicate on the graph the quiescent point. What region is the transistor working on? Justify your answer and indicate the values of quiescent point (IDQ, VDSQ and VGSQ)

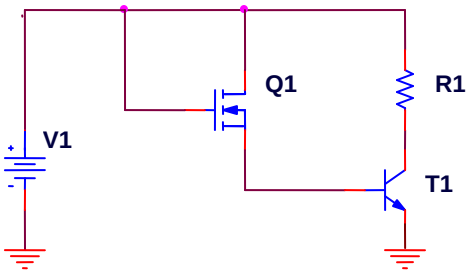
[D] Obtain the limit values of the input voltage Vent to make the transistor of figure work in switching mode (Vent (cut-off) and Vent (ohmic)). Justify your answer.

6.5 For the following circuit:

Data:
R1 = 1KΩ
V1 = 10V

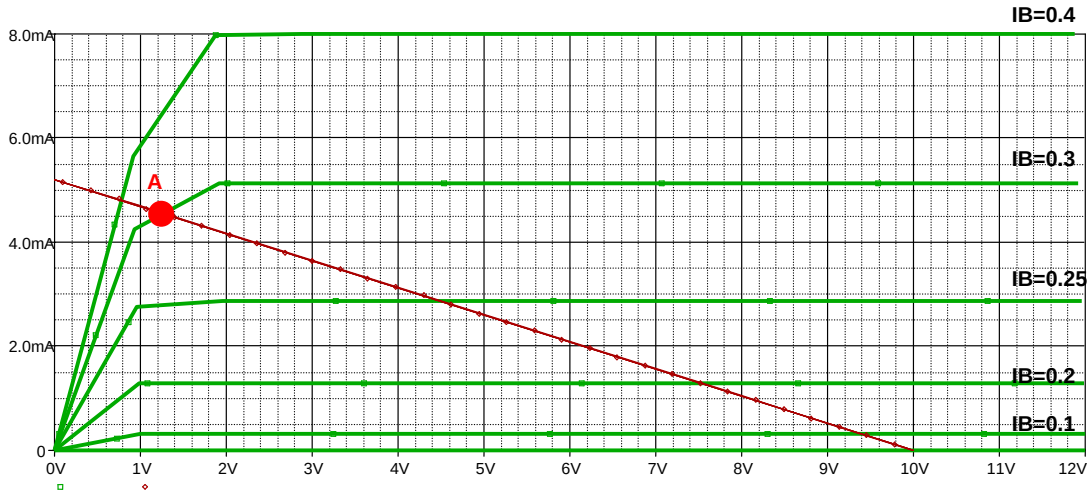
MOSFET:
K = 0.01 mA/V^2
V_T = 4.3V

Bipolar :
$V_{BE(ON)}$ = 0.7V
$V_{CE(SAT)}$ = 0.2V
β = 20



[A] Calculate the voltage with respect to ground at the collector of bipolar transistor. Justify the value obtained.
[B] If the MOSFET transistor is replaced by a resistor R2, so that the operating point of bipolar transistor was like in the previous section. What is the value of resistance?
[C] Using the graph and considering the base current calculated in paragraph A, obtain an approximate minimum value for R1 to make the bipolar transistor saturated.

***Note**: If you have not resolved paragraph A, assume an hypothetical value of I_B = 0.35 mA.*



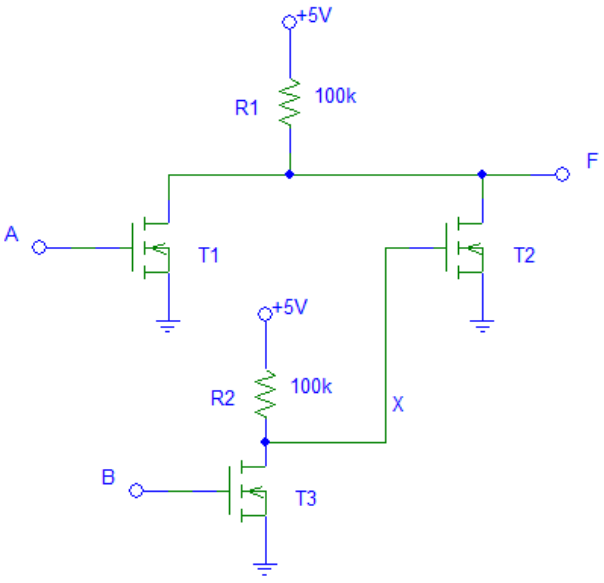
[D] If the MOSFET gate is connected to the base of bipolar transistor (assuming that at the same time, is disconnected from power), obtain the quiescent point of bipolar transistor. Justify the new quiescent point of bipolar transistor.

6.6

The digital circuit of figure, designed with MOSFET transistors, has the inputs A and B, and the output F.

Note: In ohmic region, use the approximate expression $R_{ON} \approx$

Transistor parameters:
VT = 0.5 V
K = 0.1 mA/V2



[A] Complete the following truth table and enter the logical expression of F in function of the inputs A and B:

A	B	X	F
0	0		
0	1		
1	0		
1	1		

[B] Assuming A = 0V (logic '0') and B = 5V (logic '1'):

Note: Since the circuit is digital, transistors operate in switching mode (between cut-off and linear region (Ron).

- Draw the equivalent circuit (replace each transistor for a Ron or an open switch) and perform calculations to fill the following table.

Ron (kΩ)	T1 region	T2 region	T3 region	VX (Volt)	VF (Volt)	Static consumption (mA)	Static consumption (mW)

[C] Assuming A = 5V (logic '1') and B = 0V (logic '0'):

- Draw the equivalent circuit (replace each transistor for a Ron or an open switch) and perform calculations to fill the following table:

Ron (kΩ)	T1 region	T2 region	T3 region	VX (Volt)	VF (Volt)	Static consumption (mA)	Static consumption (mW)