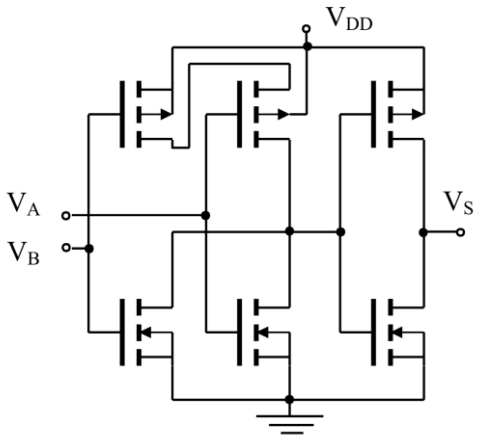
Unit 4: CMOS TECHNOLOGY FOUNDATIONS. PROPOSED QUESTIONS AND EXERCISES

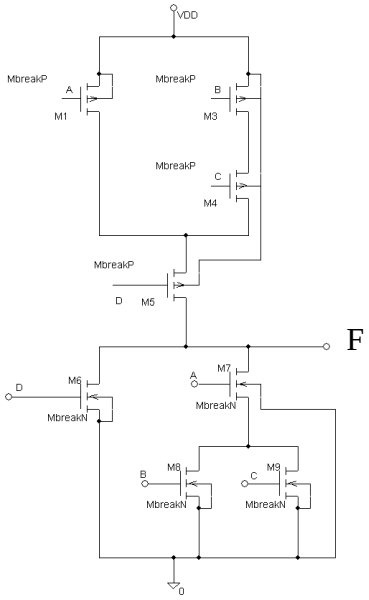
1. CMOS Complementary logic

1.1 ¿ What function does the following logic gate?

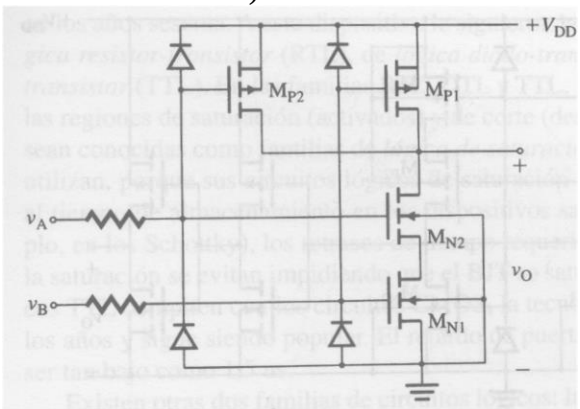
A) AND
B) NAND
C) OR
D) NOR



1.2. Find the Boolean expression for F in terms of A, B, C y D.



1.3. A) What type of logic gate is the following? B) For V_{DD} = 15V, what would be the output if Va = Vb = 100V? C) What is the output if Va = Vb =-120V? (assume a Vγ= 0.7V for the diodes)



1.4. Design a XOR function with complementary CMOS logic. Estimate the number of transistors and compare with a traditional design based on logic gates.

Note: $F = A \oplus B = \overline{A}B + A\overline{B}$

1.5. Design the function $F = AB + AC + BC$ (it corresponds to the carry out of a Full-Adder) with complementary CMOS logic. Estimate the number of transistors and compare with a traditional design based on logic gates.

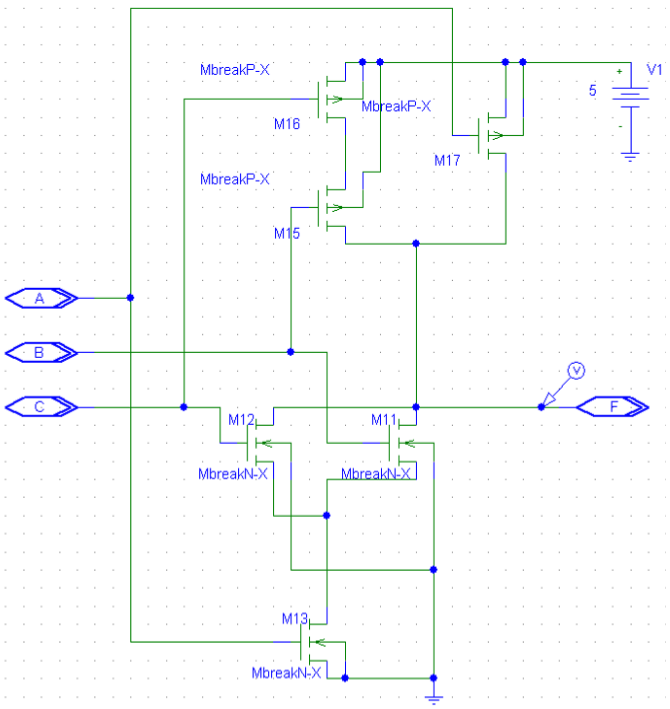
1.6 Obtain the logic function of the following CMOS circuit:

[A] F= A.(B+C)

[B] $F = \overline{A.(B+C)}$

[C] $F = \overline{(B+C)}$

[D] $F = B.C + A$

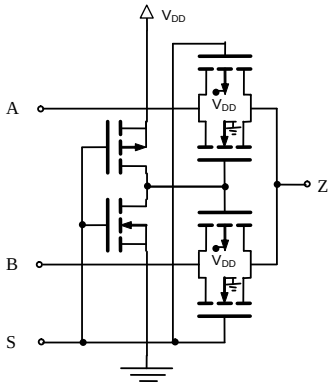


2. Transmission gates and applications

2.1. Given a NMOS transmission gate with a transistor of |VT| = 1.5V. A voltage of 0V is applied to the input and 5V to gate terminal G. What voltage is obtained at its output?:

A) 5V
B) 0V
C) 3.5V
D) 1.5V

2.2. Given the following circuit and assuming that A and B have digital levels, which of the statements is TRUE:



A) The circuit is a multiplexer with inverted output.

B) The logic function implemented is:

$$Z = S \cdot \overline{B} + \overline{S} \cdot \overline{A}$$

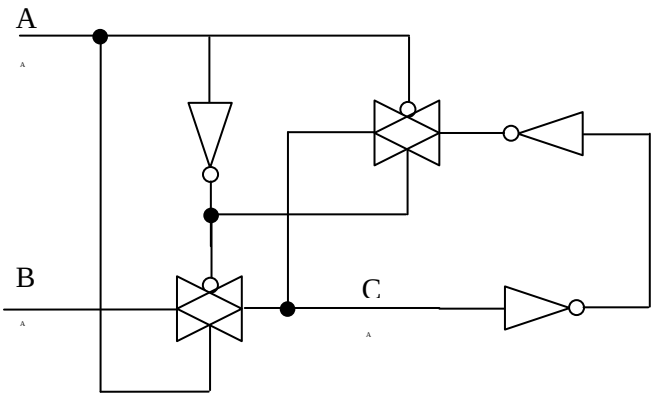
C) The logic function implemented is:

$$Z = S \cdot B + \overline{S} \cdot A$$

D) Transmission gates degrade circuit the logic levels.

2.3. Make a design of two-input XOR gate based on CMOS transmission gates and additional logic gates if necessary. Tip: Use the basic structure of a 2-channel multiplexer.

2.4. Analyze the following circuit based on CMOS transmission gates. This is a:



A) XOR gate with inputs A and B
B) Two-channel (A and B) multiplexer with a selection input C
C) D latch , with data input B, enable input A and state variable Q=C
D) RS latch, with R=A, S=B and state variable Q=C

2.5 Design a 4-channel analog multiplexer, using CMOS transmission gates and some digital circuitry if necessary for control. Consider the decoder as a block, without going into its internal design with transistors.

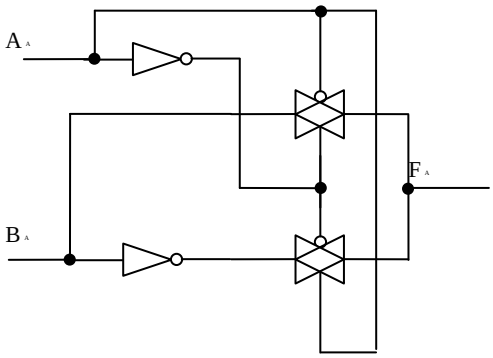
2.6 The CMOS circuit of figure behaves as:

[A] A buffer.

[B] An inverter with tri-state output.

[C] A 2*1 multiplexer, with channels A and B.

[D] An XOR function of A and B.



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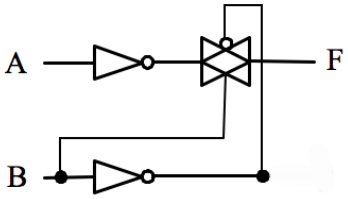


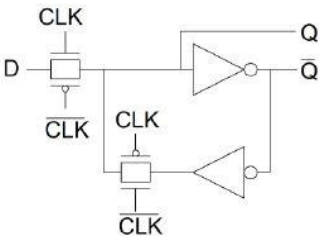
2.8 Regarding the circuit of Figure, indicate which of the following statements is FALSE:

[A] When CLK = 0 the circuits holds the value of Q.

[B] If the left transmission gate is open, the other is closed, and vice versa.

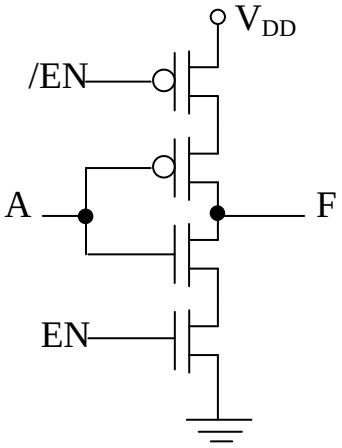
[C] When CLK = 1 the logic value of D is transmitted to the output Q.

[D] This is an edge-triggered D flip-flop.



3. Special outputs: tristate and open drain

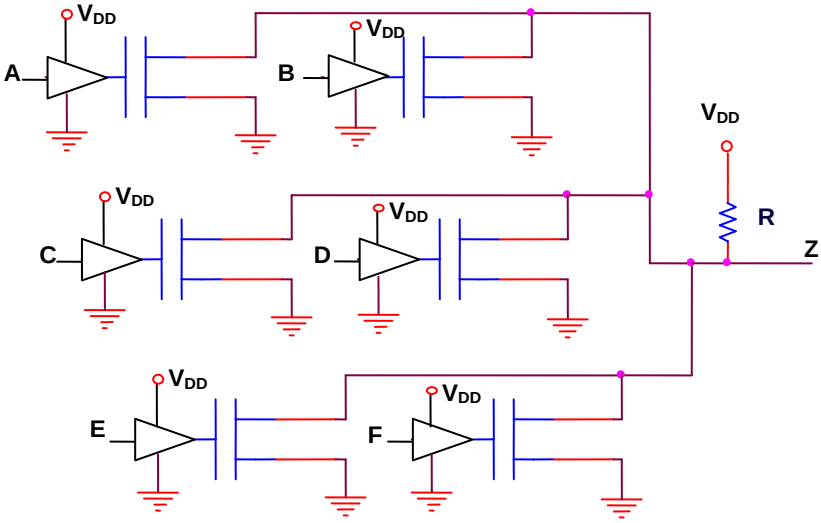
3.1. The CMOS circuit of figure is:



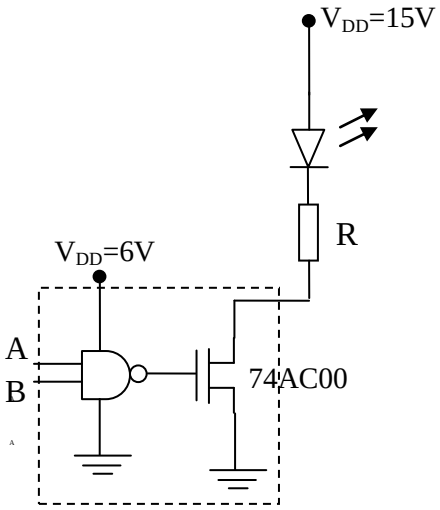
A) An inverter
B) A tri-state inverter
C) A tri-state buffer
D) An open-drain buffer

3.2. Indicate the logical expression of the wired function Z. The gates have an open-drain output. Suppose that R is a pull-up resistor of appropriate value.

[A] $Z = A + B + C + D + E + F$
[B] $Z = \overline{A + B + C + D + E + F}$
[C] $Z = (A + B).(C + D).(E + F)$
[D] $Z = A.B.C.D.E.F$



3.3. The following Figure shows the control circuit of a LED with a NAND gate with open-drain output. 74AC gates have been used for this purpose, as they provide enough current to the LED (74HC gates have a maximum output current of only 4 mA). Designin the appropriate value of resistor R so that the LED lights properly.



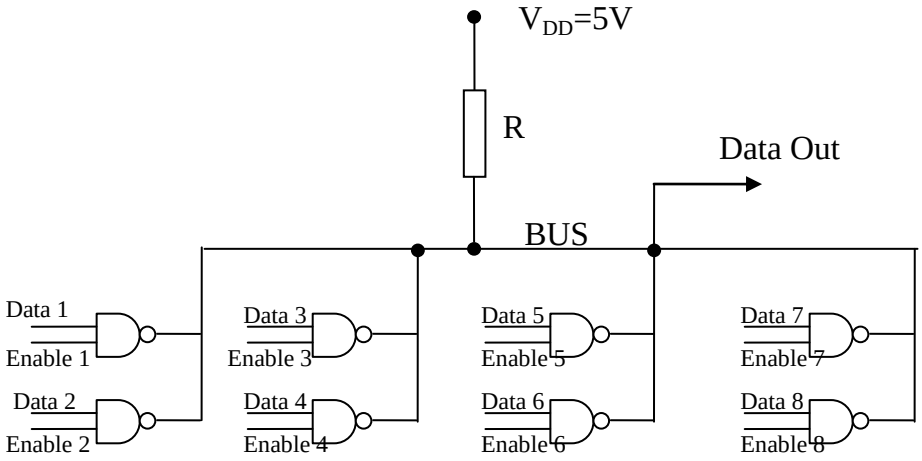
Data of 74AC00
I_{OLmax} = 24 mA
V_{OLmax} = 0.37V

Data of LED
I_{LED} = 10 mA
V_{LED} = 1.6V

A) R = 130Ω
B) R = 3k3
C) R = 1.3KΩ
D) None of the previous answers is correct

3.4. The figure shows 8 open-drain outputs connected to a bus. Only one gate is enabled at a time, remaining the other with a high level at the output. Indicate the maximum and minimum pull-up resistor R, according to the following specifications of the logic gates:

(74HC gates specifications):
I_{OLmax} = 4mA,
V_{OLmax} = 0.33V
V_{OHmin} = 3.84V
I_{OHmax} = 5μA (leakage current at the output when High)



A) 0.5K ≤ R ≤ 4K7
B) 0.5K ≤ R ≤ 10K
C) 1.5K ≤ R ≤ 3K3
D) 1.17K ≤ R ≤ 29K

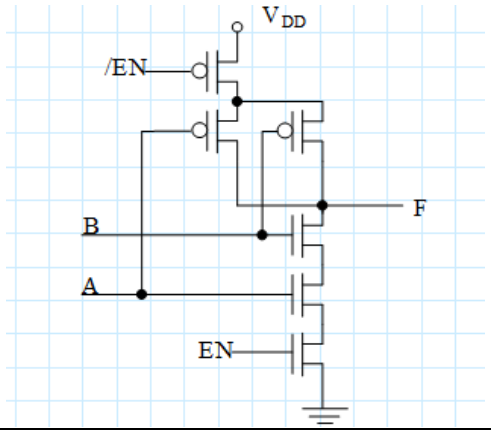
3.5 In the CMOS circuit of figure:

[A] If EN = ”0”, $F = \overline{A.B}$

[B] If EN = ”1”, $F = \overline{A+B}$

[C] If EN = ”0”, F = H.Z (high impedance)

[D] $F = \overline{A.B}$ always.



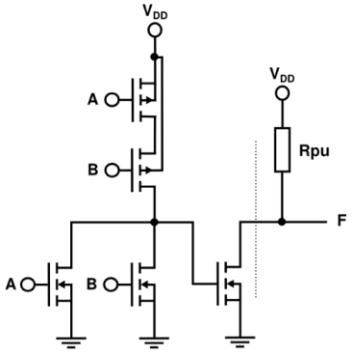
3.6 What is le logic function F(A,B) of CMOS circuit of figure?.

[A] F(A,B)= $A+B$

[B] F(A,B)= $\overline{A+B}$

[C] F(A,B)= $A.B$

[D] F(A,B)= $\overline{A.B}$



4. Characteristic parameters / CMOS subfamilies

4.1. With respect to the CMOS logic family, indicate which of the following statements is FALSE:
A) The 74CXXX chips are electrically compatible with TTL family.
B) The noise margin increases with decreasing supply voltage.
C) The fan-out is limited to 50 CMOS inputs, due to increased switching delays.
D) The dynamic consumption increases in a quadratic form with supply voltage.

4.2. With respect to the CMOS logic family, indicate which of the following statements is FALSE:
A) The dynamic consumption is linearly dependent on frequency.
B) The BCT gates (BiCMOS) are made only with MOSFET transistors.
C) The subfamily HCT is CMOS, but with TTL-compatible inputs.
D) The noise margins depend linearly on VDD.

4.3. A specific computer chip contains 50,000 gates, each one having a zero static power dissipation. In the worst case, the output of each gate has a switching frequency of 200MHz. The total dynamic power dissipation allowed for the chip is 10W. The supply voltage is VDD = 5V. Determine the allowable load for each gate.

4.4. A given manufacturing process of CMOS chip has an average capacity of 150 pF/mm2. It is intended to synthesize a chip with logic circuits using an activity factor 0.1. Estimate the power consumed by the chip, if it has an area of 70 mm2 and operates at 450 MHz with a supply voltage of 0.9V.

4.5. A given CMOS processor has 20M transistors dedicated to combinational and sequential logic and 180M transistors dedicated to the memory. The average activity factor is 0.1 for logic and 0.05 for the memory. If the average capacity per transistor is 1 fF (1 femtofarad = 10-15 F), the supply voltage is 1.2V and the clock frequency is 1GHz, calculate the power consumtion.

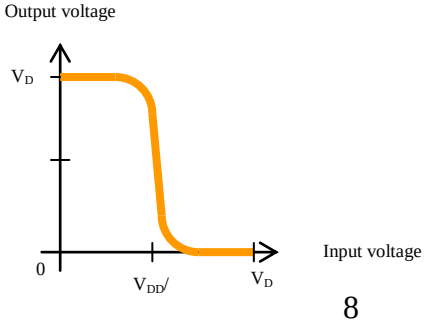
4.6 Given the following electrical specifications of a HCMOS gate, powered at +5 V, calculate:

- VIHmin = 3.15V, VILmax = 1.35V
- VOHmin = 3.84V, VOLmax = 0.33V
- IIHmax = 1μA, IILmax = -1μA
- IOHmax = -4mA, IIHmax = 4mA
- ICC(typ) = 2 μA
- Tpd(typ) = 9 ns
- Cpd (gate capacity, without load) = 22pF

A) The noise margin
B) The fan-out
C) The dynamic consumption assuming that the inputs switch at an average frequency of 100 MHz and the output is empty (not connected to anything).
D) The static consumption mW
E) The maximum frequency of entries

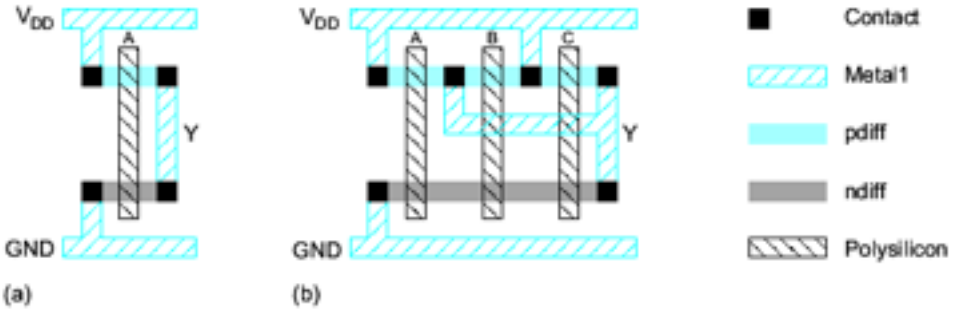
4.7 How can we improve the speed of the previous gate? (indicate True / False)
A) Increasing the parasitic capacitance of the gate
B) Increasing the supply voltage
C) Decreasing the ratio (W / L) of transistors
D) Increasing the constant K of transistors

4.8 Given the transference curve of a standard CMOS inverter:
1. Identify the VOH, VOL, and Vilmax VIHmin
2. Indicate in which area of the curve there is current consumption and of what type.

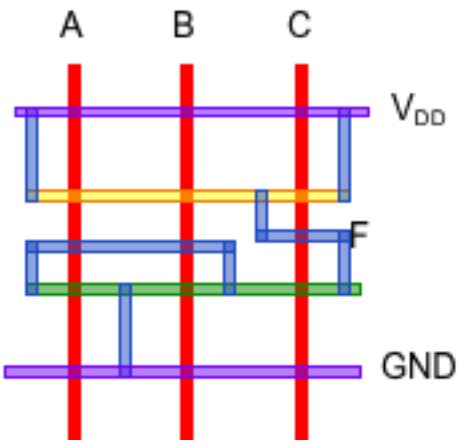


5. VLSI design foundations

5.1. Indicate the logic function that implements the standard cell with the layouts of the figure:



5.2. From layout diagram of the figure, indicate the logic function that implements the standard cell.



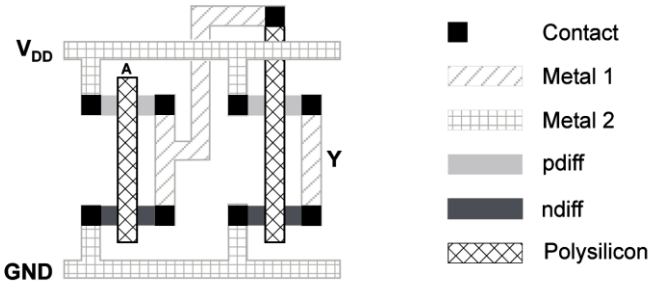
Violet → metal 2 (VDD y GND)
Blue→ metal 1 (internal connections)
Green → N-diffusion
Yellow → P-diffusion
Red → polisilicon (transistor gates)

5.3. Indicate whether they are true (V) or false (F) the following statements on the photolithographic manufacturing process of CMOS IC:
a) Usually, a circular silicon wafers are used as substrate
b) Each wafer contains a single chip
c) They are deposited layers (layers) of different materials in a bottom-up way
d) The typical order in the deposition of layers is: 1) n + and p + areas of S and D, 2) metal interconnections, 3) thin insulating layer of gate, 4) polysilicon of the gate
e) UV light is used to project the masks on the wafer
f) Once you have the chips on the wafer substrate, they are cut, tested and encapsulated

5.4. If we compare the standard cell based design with full-custom design, we can say that:
A) The semi-custom design based on cells optimizes the speed and silicon occupied area.
B) The full-custom design is getting more automated, minimizing the design time
C) The full-custom design is done with layout editors, making the geometric description of the masks
D) In the cell design, the smallest units of design are the transistors, which are stored in libraries

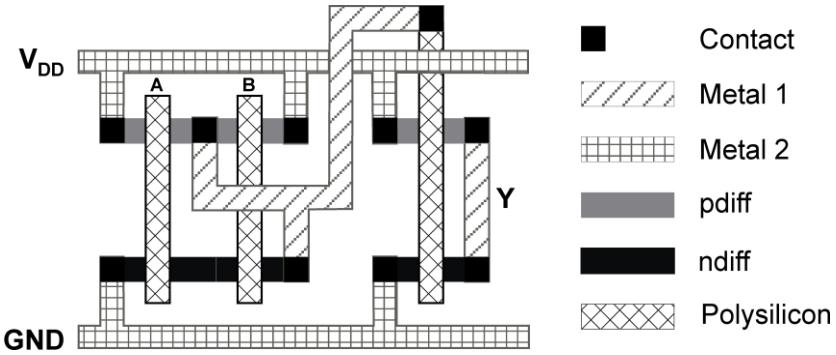
5.5. Indicate what is the Placement and Routing in the VLSI design flow, and why it is very important in today's chips.

5.6. What logic circuit implements the layout of figure?



[A] A tristate inverter.
[B] A buffer.
[C] A tristate buffer.
[D] A CMOS transmission gate.

5.7 What logic circuit implements the layout of figure?



[A] A three- input NOR gate.
[B] A two-input OR gate.
[C] A three-input NAND gate.
[D] A two-input AND gate.