COMPUTERS FUNDAMENTALS

Practice 2

Circuit Implementation

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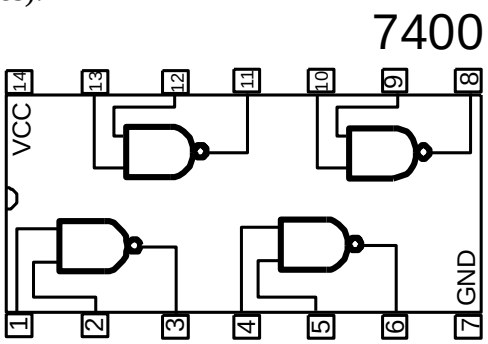
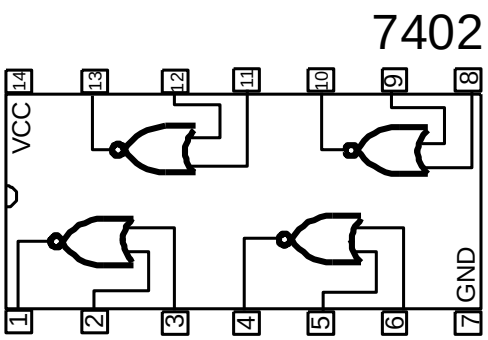
General

The objective in this practical session is that the student participates in every step that involves the implementation of a logic circuit. The specification of the desired circuit is the starting point. From the specifications it is obtained the truth table. The truth table is used to obtain the canonical forms of the desired logic circuit. Departing from the canonical forms, simplifications are made applying Boole's Algebra or using Karnaugh's maps. Finally, the simplified expression is implemented using logic gates.

The implementation of the circuit is made using commercial chips that encapsulate logic-gates. In particular, we use integrated circuits 7402 (4 NOR gates) and 7400 (four NAND gates).



7400 Integrated Circuit



7402 Integrated Circuit

Circuit Implentation

The purpose of this section is to apply the knowledge acquired writing canonical forms and circuit's simplification using Karnaugh's maps.

Two circuits will be implemented. The first one is a *comparator circuit* and the second one is a circuit to obtain the *complement to 9* of a BCD number . Starting from the functional specifications, for each one of the 2 circuits, it must be obtained.

- The truth table.
- The canonical forms (Sum of products and product of sums).
- Simplification using Karnaugh's maps.
- Design of the resulting circuit using logic-gates.
- Using the logical trainer, the circuit must be built and verified its functionality.

Circuit 1. Comparator Circuit

It is desired to design a comparator circuit of two two-bit binary numbers each one, A (a0 a1) and B (b1 b0). The circuit has two outputs, S0 and S1 (both high-level active). S0 output should be activated if (A < B) and the output S1 when (A = B). The diagram shown in Figure 2 represents the inputs and outputs to the circuit.

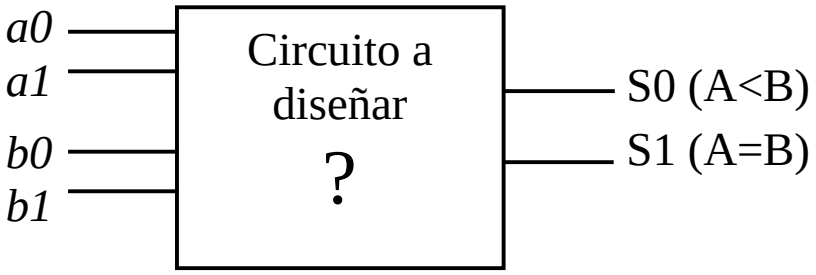


Figura 2. Comparator circuit.

Question 1. Write the associated truth table of the comparator circuit.

b1	b0	a1	a0	S0	S1
0	0	0	0	0	1
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	1	0	0	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	0	1	1	0	0
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	0	1

Table 2. **Truth table of the comparator circuit.**

Question 2. From the truth table of the previous section obtains the canonical expression both as a **sum of products** (disjunctive canonical form). And as a **product of sums** (conjunctive canonical form) for the S0 and S1 outputs.

S0 (disjunctive canonical form)	$S0 = \sum_{(\ b1,b0,a1,a0\ )} (4,8,10,12,13,14)$
S0 (conjunctive canonical form)	$S0 = \prod_{(\ b1,b0,a1,a0\ )} (0,1,2,3,,5,6,7,9,11,15)$
S1 (disjunctive canonical form)	$S1 = \sum_{(\ b1,b0,a1,a0\ )} (0,6,9,15)$
S1 (conjunctive canonical form)	$S1 = \prod_{(\ b1,b0,a1,a0\ )} (1,2,3,4,5,7,8,10,11,12,13,14)$

Question 3. Get the logic functions of S0 and S1 expanding minterms and maxterms.

S0 (minterm)	S0 =
S0 (maxterms)	S0 =
S1 (minterm)	S1 =
S1 (maxterms)	S1 =

Question 4. Draw Karnaugh's maps for output S0. Use the left table for minterms (‘1’) and the table to the right for maxterms (‘0’).

	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

Simplification of S0 using minterms.

S0=.....

Simplification of S0 using maxterms.

S0=.....

Question 5. **(0.5 points) For output S0**. From the two previous simplifications, draw and then implement the circuit with lower cost (using less number of logic-gates with less number of entries). For the implementation of the circuit can use any available gates on the trainer. **VERIFY** that the circuit gets the same output values as the truth table written in table 2.

Circuit that implements S0.

Question 6. Draw Karnaugh's maps for output S0. Use the left table for minterms (‘1’) and the table to the right for maxterms (‘0’).

	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

Simplification of S0 using minterms.

S1=.....

	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

Simplification of S0 using maxterms.

S1=.....

Question 7. From the two previous simplifications, draw and then implement the circuit with lower cost (using less number of logic-gates with less number of inputs). For the implementation of the circuit can be used any available logic-gates on the trainer. **VERIFY** that the circuit gets the same output values as the truth table written in table 2.

Circuit that implements S1.

Circuit 2. Circuit that computes the complement to 9.

It is desired to design a circuit that computes the complement to 9 (CA9) of a number X represented in BCD. The result should be connected to a BCD to one of the 7 segments decoders of the trainer. The result can be seen on the display of 7 segments of the trainer.
The CA9 of a number is defined as follows: $Ca9(X) = 9 - X$, where $0 \leq X \leq 9$

Question 8. Write the truth table associated with the circuit that computes the complement to 9 (CA9) of a number X represented in BCD.

d	c	b	a	D	C	B	A
0	*0*	*0*	*0*				
0	*0*	*0*	*1*				
0	*0*	*1*	*0*				
0	*0*	*1*	*1*				
0	*1*	*0*	*0*				
0	*1*	*0*	*1*				
0	*1*	*1*	*0*				
0	*1*	*1*	*1*				
1	*0*	*0*	*0*				
1	*0*	*0*	*1*				
1	*0*	*1*	*0*				
1	*0*	*1*	*1*				
1	*1*	*0*	*0*				
1	*1*	*0*	*1*				
1	*1*	*1*	*0*				
1	*1*	*1*	*1*				

Table 3. Truth table of the comparator circuit that computes the CA9 of a number X represented in BCD

Question 9. Draw Karnaugh's maps. In this exercise is left to the student the simplification using only minterms or maxterms.

	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

Simplification of D.

D=.....

	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

Simplification of C.

C=.....

	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

Simplification of B.

	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

Simplification of A.

B=.....

A=.....

Question 10. **(1.0 points)** Draw and then implement the circuit using the necessary logic-gates. **VERIFY** that the circuit gets the same output values as the truth table written in table 3.

Circuit that computes the CA9 of a number X represented in BCD