2.2. Given the following circuit and assuming that A and B have digital levels, which of the statements is TRUE:

A) The circuit is a multiplexer with inverted output. ✗

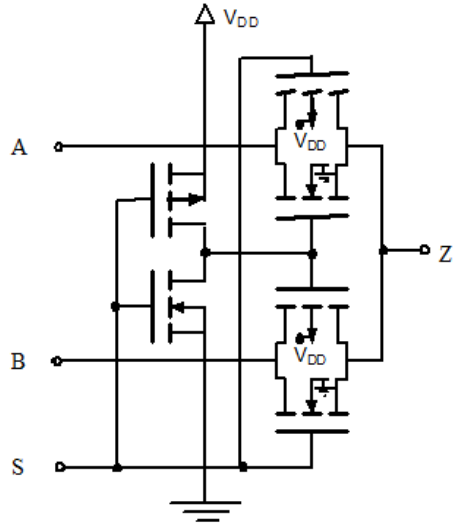
B) The logic function implemented is:

$$Z = S \cdot \overline{B} + \overline{S} \cdot \overline{A}$$ ✗

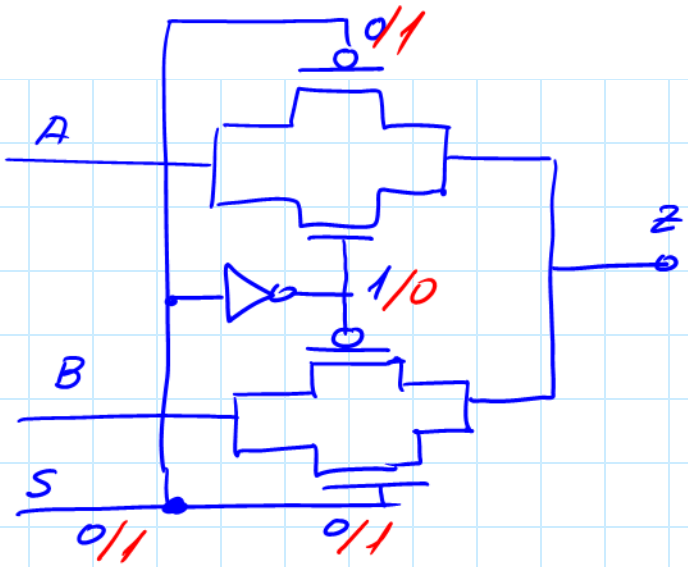
C) The logic function implemented is:

$$Z = S \cdot B + \overline{S} \cdot A$$

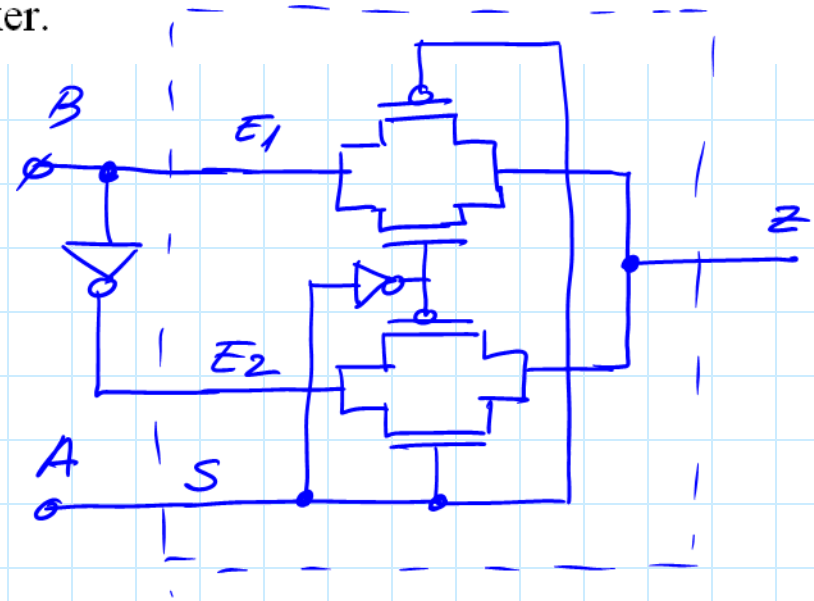
D) Transmission gates degrade circuit the logic levels. ✗



$S=\phi \Rightarrow Z=A$
$S=1 \Rightarrow Z=B$
$\Big\} Z=\overline{S}A+SB$



2.3. Make a design of two-input XOR gate based on CMOS transmission gates and additional logic gates if necessary. Tip: Use the basic structure of a 2-channel multiplexer.



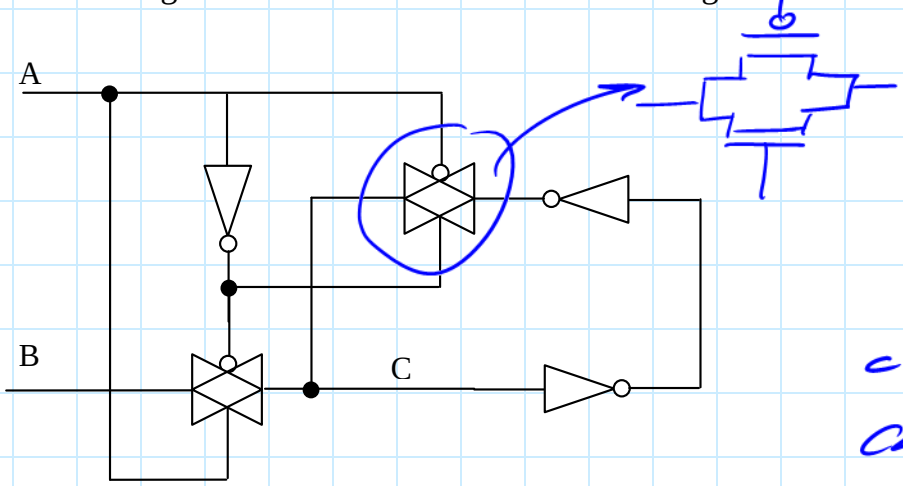
$Z = \bar{S} E_1 + S E_2$ (multiplexor)

$Z = \bar{A} B + A \bar{B}$ (XOR)

$\Rightarrow \begin{cases} S = A \\ E_1 = B \\ E_2 = \bar{B} \end{cases}$

UNIT 4. CMOS

2.4 Analyze the following circuit based on CMOS transmission gates. This is a:



A → CLK
B → D
C → Q
} latch

CLK: 0 ⇒ Memoria
CLK: 1 ⇒ C = B

A) XOR gate with inputs A and B ✗
B) Two-channel (A and B) multiplexer with a selection input C ✗
C) D latch , with data input B, enable input A and state variable Q=C ✓
D) RS latch, with R=A, S=B and state variable Q=C ✗