Diodes. Introduction. Static regime behaviour

1. Of the following statements about the PN junction diode in static regime, select which is the **FALSE**:
   [A] The load line is not dependent on the characteristic curve of the device.
   [B] In direct region, small increases in voltage V_{AK}cause large increases of I_D.
   [C] Is a nonlinear device.
   [D] The operating point does not depend on bias circuit.

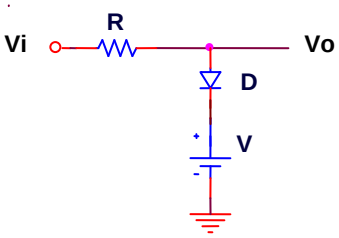
---

2. Analyzing the diode circuit of the figure and assuming an ideal diode approximation, we can **ASSERT** that:

[A] If the input voltage Vi is positive, the diode conducts and the output voltage is equal to V.

[B] If the input voltage Vi is negative, the diode does not conduct and the output voltage is 0V.

[C] When the input voltage Vi is lower than V, the output is Vi**.**



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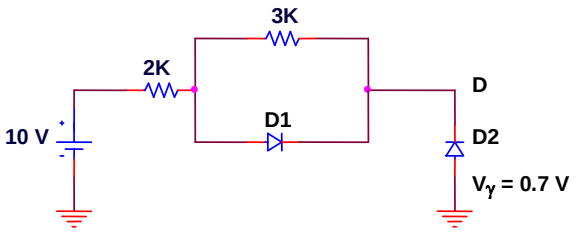
3. By solving the circuit of figure can be said that the voltage at point D is:

[A] 0V

[B] 10V

[C] 9.3V

[D] -0.7V



Diode circuits

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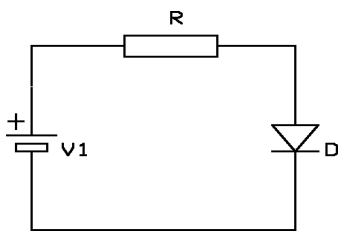
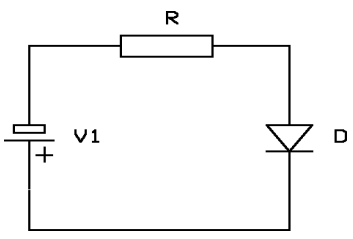
4. Calculate the operating point Q (V_{DQ}, I_{DQ}) of diodes in the following circuits:



A)



B)

DATA: V1 = 5V; R = 220Ω; Diode: Vγ = 0.6V

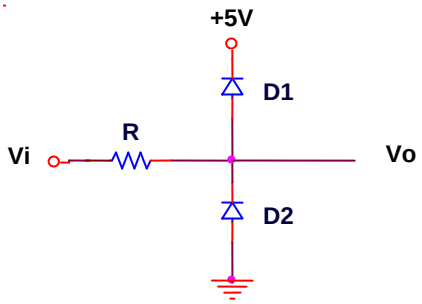
5. Given the following two-level clipping circuit, indicate the range of values that can be obtained at the output Vo. (V γ = 0.7V for both diodes).

[A] 0.7V <= Vo<= 5.7V

[B] -0.7V <= Vo<= 5.7V

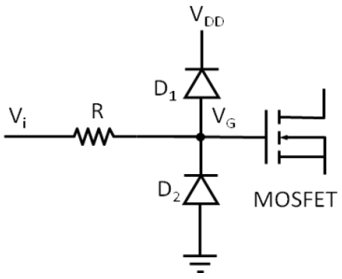
[C] -0.7V <= Vo<= 4.3V

[D] 0.7V <= Vo<= 4.3V



6. Given de following input-protection circuit for MOSFETs, calculate the voltages at all points and currents at all branches, and the status of both diodes, when the input is a static voltage of 4000V DC, produced when a person who has stepped on a carpet touches Vi terminal.

DATA: R = 200Ω; V_{DD} = 5V; Diodes: Vγ = 0.7V



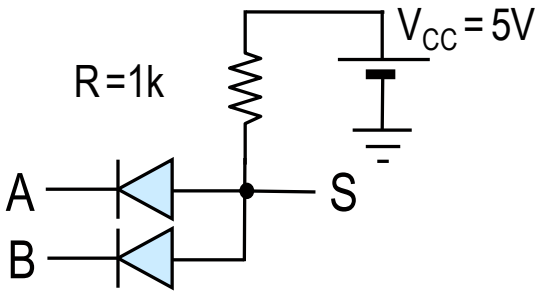
7. Given the circuit with diodes of figure and assuming A = “0” (0V) and B = “1” (5V) point out the CORRECT answer of the following, considering Vγ = 0.7V for both diodes:

[A] V_{AK} = - 4.3V for the diode of input B.

[B] This circuit implements a two-input OR logic gate.

[C] The voltage at S output is 4.3V.

[D] The current flowing through the resistor is divided equally in each diode.



8. a) Implement, using logic gates composed only by diodes and resistors, the logic equation F = AB + CD.

b) Calculate the output voltage of the designed circuit, for the following input combinations (assume all resistors value as R and ideal diodes):

b1. A = B = C = D = 0

b2. A = B =1; C = D = 0

b3. A=B=C=D= 1

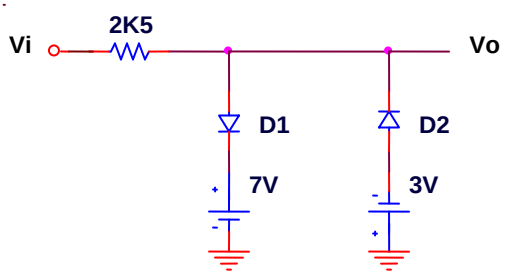
9. Calculate the value of Vo given Vi = 2V for the clipping circuit of the figure. Assume a Vγ=0.7 V for both diodes.

[A] -3.7V

[B] 0V

[C] 7.7V

[D] 2.0V



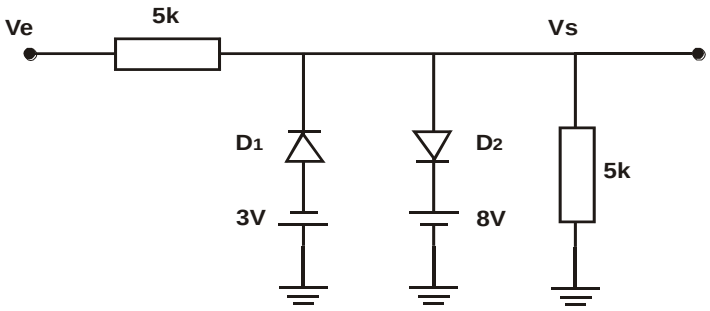
10. Given the following clipping circuit, and for Vγ=0.7V for all diodes, calculate Vs when Ve = 6V.

[A] 7.3V

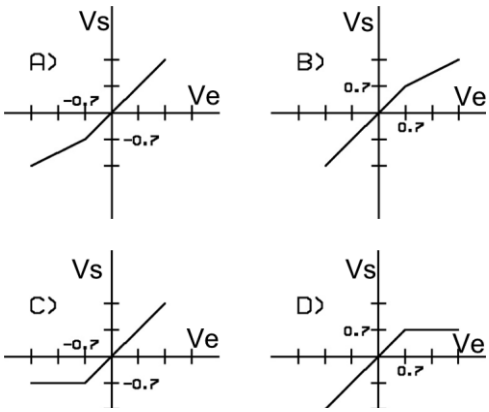
[B] 3V

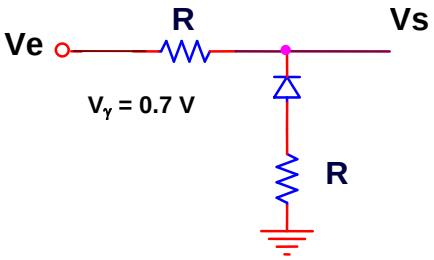
[C] 3.7V

[D] 6V



11. Given the circuit of the figure, determine which of the following curves (A,B,C,D) is its corresponding transference curve.





Special purpose diodes

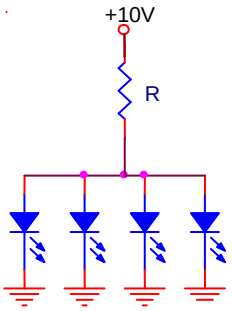
12. We aim to design the value of resistor R taking into account that LEDs must shine properly. Tick the **RIGHT** answer of the following:

DATA: V_{LED} = 1.5V; I_{LED} = 10mA

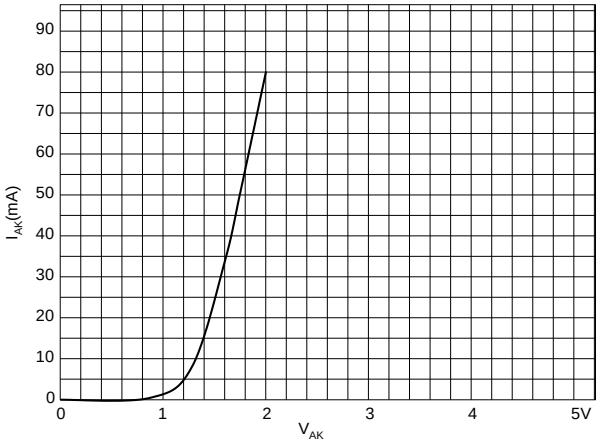
[A] R can have any value higher than R ≥ 0,21kΩ

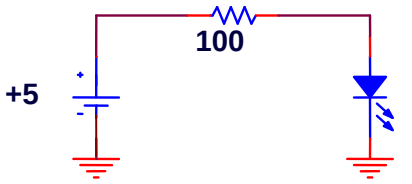
[B] R can be equal to R = 200Ω

[C] To make correctly the calculation of R, we should consider a voltage drop in R of 6V, since we have 4 LEDs in parallel.



13. Indicate the operating point of LED of the following circuit whose characteristic curve can be seen on the right.NOTE: We recommend using the load line.





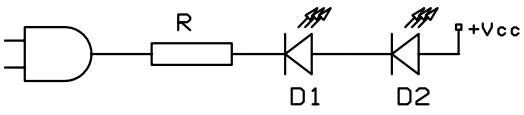
[A] The operating point can not be calculated because of missing data.
[B] 1.4V, 15mA
[C] 1.6V, 35mA
[D] 1.8V, 55mA

14. The circuit shown is intended to light the two LEDs when the logic gate output is low (V_{OL} = 0.2V). Indicate what would be the most appropriate value for the resistor R.

[A] 330 Ohm
[B] 220 Ohm
[C] 200 Ohm
[D] 180 Ohm

Data:
Vcc=5V

LED D1 and D2:
V_γ = 1.5V
I_{LED}= 10mA



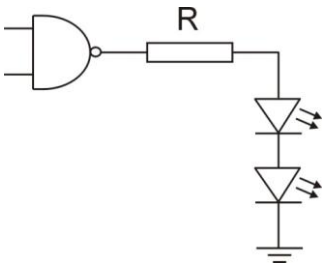
15. Given the following circuit with LEDs, signal the CORRECT answer between the following, taking into account the following parameters: For LEDs, V_{LED}=1.5V and I_{LED}= 10mA, and for NAND gate, V_{OL}=0.15V y V_{OH}=4.5V (V_{CC} = 5V).

[A] The LEDs will shine properly with a resistor higher than 150Ω.

[B] The LEDs will shine properly with a resistor lesser or equal than 150Ω.

[C] The LEDs will shine properly with a resistor of 150Ω.

[D] The LEDs will not shine for any of the logic level outputs of the NAND gate.



16. We have a TTL circuit (for example, an AND gate) that performs a generic function F. We want to light a LED when F = "0". Design a circuit for this purpose..

DATA: V_{LED} = 1.5V; I_{LED} = 10mA; $V_{OHmín}$ = 2.4V; $V_{OLmáx}$ = 0.5V

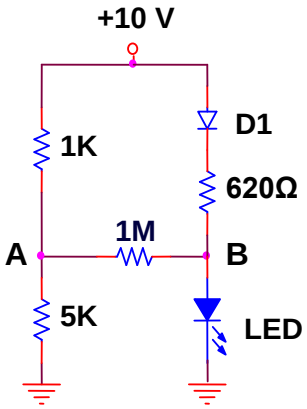
17. Given the circuit of the figure indicate the correct answer:

Data: D1: V_γ = 0.6V; LED: V_{LED} = 1.5V (to get a good bright is required I_{LED}among 10mA and 20mA). We recommend using the approximation of the resistive divider.

[A] The LED does not start conducting because the resistance between points A and B is too large.

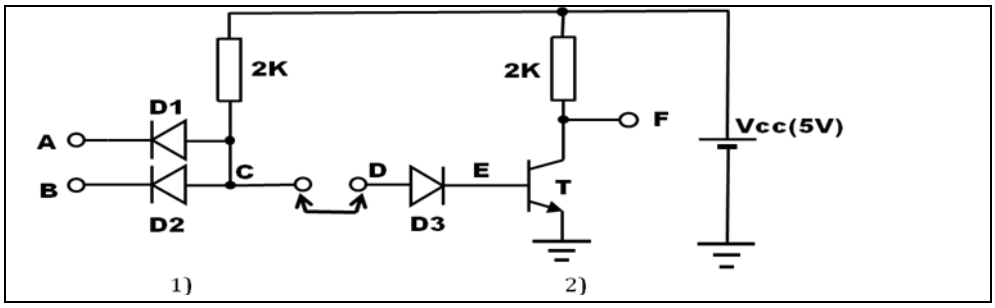
[B] The LED conductsand has a good brightness.

Enter the current through the LED: I_{LED} =



18. The circuit of figure shows two digital sub-circuits made with diodes, transistors and resistors: sub-circuit 1) has A and B as inputs and C as output; and2) has the input D and output F.

    Assuming that C and D are connected, point to the TRUE statement:
    DATA: Vγ= 0.7V (for all diodes); VBEON = 0,7V (for the transistor)



    [A] $F = \overline{A.B}$

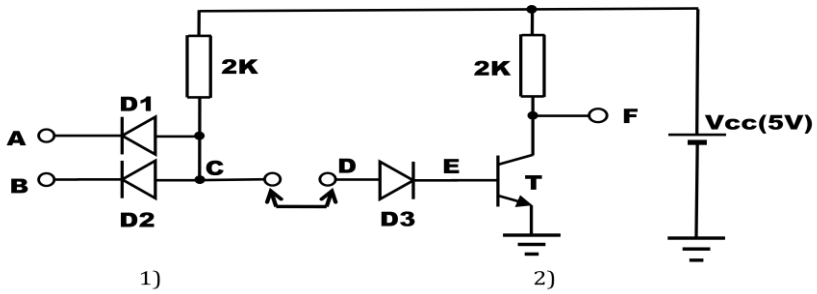
    [B] When the inputs are A=0 and B=1, then the output C is V_{CC}.

    [C] When D1 and/or D2 conducts, then so does diode D3.

    [D] In subcircuit 2), When the variable D=0 then the output F is 0 ($V_F = V_{CESAT}$ = 0.2V)

19. The circuit of figure shows two digital sub-circuits made with diodes, transistors and resistors: sub-circuit 1) has A and B as inputs and C as output; and2) has the input D and output F.

    Assuming that C and D are connected, point to the TRUE statement:
    DATA: Vγ= 0.7V (for all diodes); VBEON = 0,7V (for the transistor)



    [A] The first sub-circuit acts as a two-input OR gate and the second sub-circuit as an inverter.

    [B] When the inputs are A = 1 and B =1, D3 is ON, and output F is 0.

    [C] When D1 and/or D2 conduct, then so does D3 diode.

    [D] When D = 0, the transistor is conducting and the output F is 0.

Bipolar transistors. Basic concepts. Characteristic curves. Load line

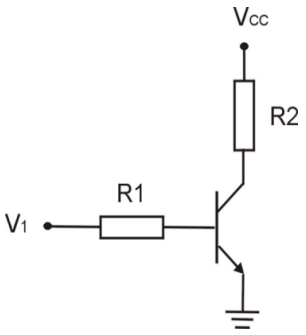
20. Choose the **TRUE** statement among the following statements related to bipolar transistors:

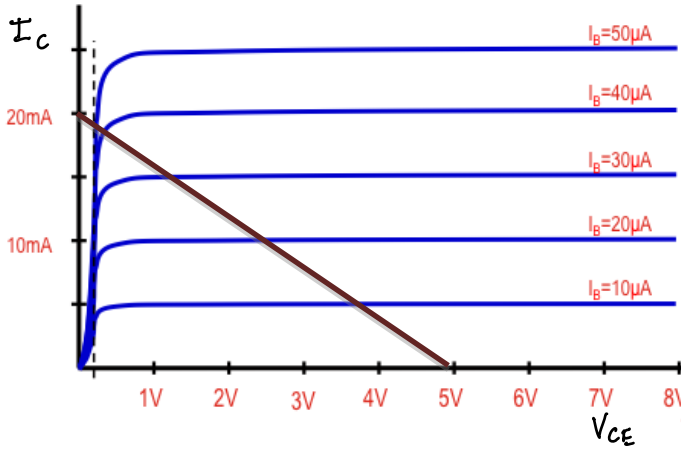
[A] The transistor is the union of two diodes in opposition.
[B] It is a symmetric three-terminal device, because you can swap the collector and emitter terminals.
[C] The base terminal is serving as the control terminal.

21. In the circuit with transistor of figure, and taking into account the following data, what will be the operating (quiescent) point of transistor?

DATA: V_{BEON}=0.7V, V1= 2.7V, R1=200k, β = 500

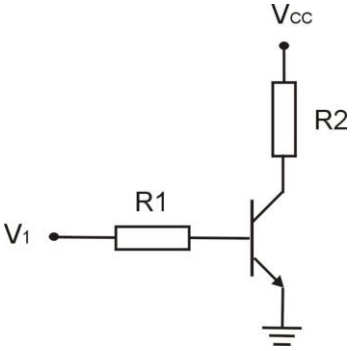
[A] (V_{CE}=1.25V, I_C=15mA)
[B] (V_{CE}=2.5V, I_C=10mA)
[C] (V_{CE}=3.75V, I_C=5mA)
[D] (V_{CE}=2.5V, I_C=10mA)

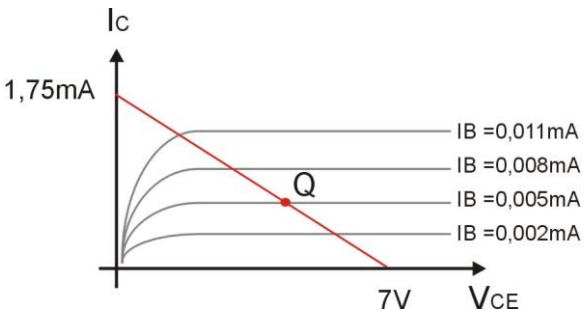




22. Given the following circuit, the corresponding load line, operating point Q and characteristic curves of the transistor, which of the following statements is correct?

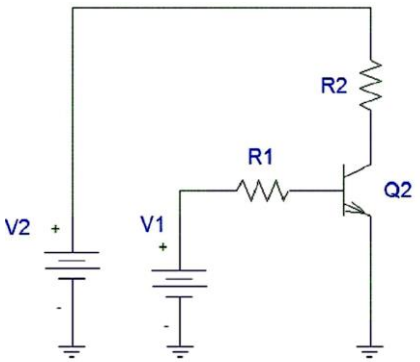
DATA: V_{CESAT} = 0,2V; V_{BEON} = 0,7V y β=100 ($I_B$is not negligible).

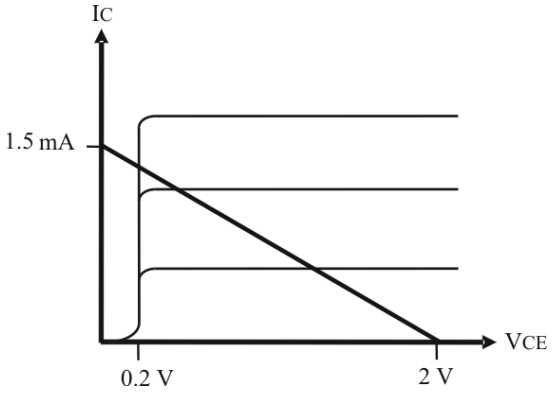




[A]. The transistor is saturated.
[B]. The I_C of transistor is 1,75mA.
[C]. The V_{CE} of transistor is 5V.
[D]. The value of R2 is 3K.

23. Indicate, using the attached figures, the value of resistance R2. (Data: β=100, $V_{CE(SAT)}$= 0.2V; $V_{BE\ (ON)}$ = 0.7V; V1= 6V; R1=100kΩ)





[A] 1,33 kΩ
[B] 1,2 kΩ
[C] 0,87 kΩ
[D] Some data are missing.

24. A bipolar NPN transistor is working on a circuit that has set the operating point Q in (V_{CE} = 5V, I_C = 2mA). If the supply voltage of circuit is 15V, what is the current $I_{C\ MAX}$ (which is obtained getting V_{CE} = 0 in the load line)?.

[A] 3mA
[B] 4mA
[C] 5mA
[D] 6mA

25. We have a NPN transistor that is biased in the point (V_{CE} = 5V I_B = 10 μA), with a power supply voltage of 10V. If we change the I_B to 15 μA, what is now the new value of V_{CE}? (NOTE: we recommend to use the load line).

[A] 7.5V
[B] 2.5V
[C] 0.2V (the transistor is saturated)
[D] None of the above values.

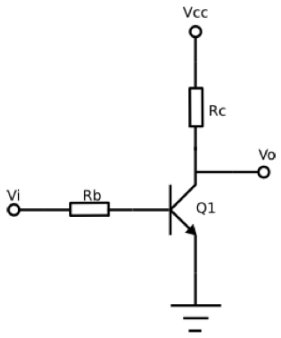
Operating regions

26. Signal the CORRECT answer from the following related to bipolar transistors:

[A] The transistor Works as an amplifier (I_C= βI_B) in saturation region.
[B] In cut-off region, voltage V_{CE} is minimum, and depends of voltage V_{BE}.
[C] The transistor switches from cut-off and forward active regions for digital applications.
[D] In forward active region, the power consumption P = V_{CE} x I_C, is higher than in the other 3 working regions.

27. Indicate the working región of transistor of figure for an input voltaje Vi of 3.7 V:
(DATA: Vcc = 5V; Rb = 100 kΩ; Rc = 2 kΩ, Q1: $V_{BE(ON)}$ = 0.7V, $V_{CE(SAT)}$ = 0.2V, β = 100)

[A] Cutt-off
[B] Active
[C] En el límite entre Active and Saturation regions.
[D] Saturation



28. In a NPN bipolar transistor connected into a given circuit, the following DC voltages and currents have been measured:

V_{CB} = -0.2V	I_B = 0.1mA
V_{BE} = 0.7V	I_E = 3.5mA

Taking into account the previous data, we can say that the transistor:

[A] Is in cut-off region..
[B] Is in the direct active region, with a β equal to 34.
[C] Is in the active region, but we cannot calculate β, as soon as we do not know I_C.
[D] Is saturated.

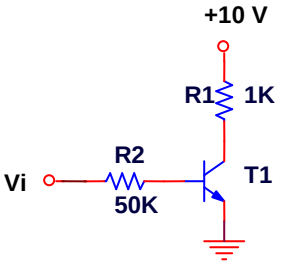
29. In a circuit based on a NPN bipolar transistor whose current gain β is 100, the following currents and DC voltages are measured:

V_{BE} = 0.7V	I_B = 0.1mA	I_E = 3.5mA

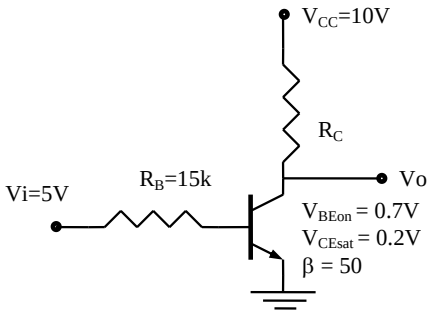
Taking into account these data, we can state that:
[A] The transistor is in cut-off mode.
[B] The transistor is in active region.
[C] The operating region cannot be known, because it is not know the value of V_{CE}.
[D] The transistor is saturated.

30. In the following circuit, and for V_{BEON} = 0.7V; V_{CESAT} = 0.2V and β = 100; indicate the working region of the transistor for the following values of Vi:

[A] Vi = 0.7V
[B] Vi = 4V
[C] Vi = 6.7V

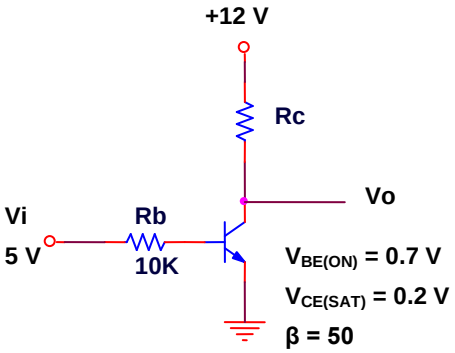


31. In the following circuit with transistor of the figure, which $R_C$value will get the transistor in the limit among active and saturation regions?



32. In the BJT transistor circuit of figure, what is the minimum resistance R_C which leads the transistor to saturation?

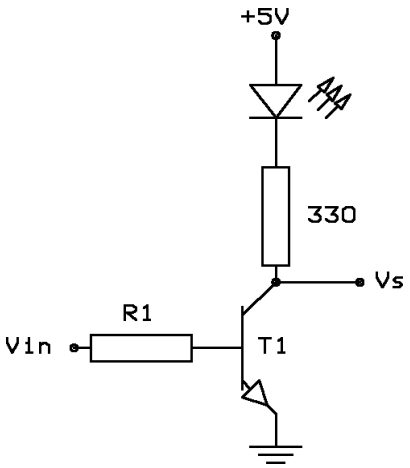
[A] $R_C = 549\Omega$
[B] $R_C = 558\Omega$
[C] $R_C = 472\Omega$
[D] None of the above.



33. What is the maximum value of R1 which leads T1 to saturation, if we connect the input of the circuit to a logic '1' output of a TTL logic gate? (Vin = 2.4V)?

DATA:V□(LED) = 1.5V; VCESAT = 0.2V; VBEON = 0.7V; β = 200.

86 KΩ
45.25 KΩ
34 KΩ
None of the above.



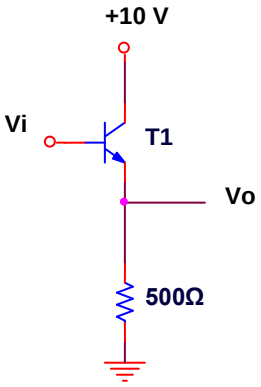
34. In the following transistor circuit, obtain:

•The operating point of the transistor(I_{CQ}, V_{CEQ}) when the input is Vi =5V.
•The base and emitter currents.
•The electrical power dissipated by the10V power supply and by the emitter resistance.

DATA:

$V_{BE(ON)}$ = 0.6V;$V_{CE(SAT)}$ = 0.2V; β = 30

The $I_B$current **is NOT** negligible.

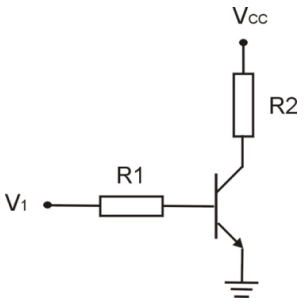


Switching. Elementary logic gates.

35. The circuit of figure is a logic inverter. ¿What will be the minimum voltage at the input for output saturation? (Ve $_{MIN(SAT)}$)

[A] $V_{eMIN(SAT)}$ = 2.5V
[B] $V_{eMIN(SAT)}$ = 2.7V
[C] $V_{eMIN(SAT)}$ = 3.1V
[D] $V_{eMIN(SAT)}$ = 5V

Data:
β: 100
R1= 100k
R2= 2k
Vcc= 5V
V_{BEON}= 0.7, V_{CESAT}=0.2V

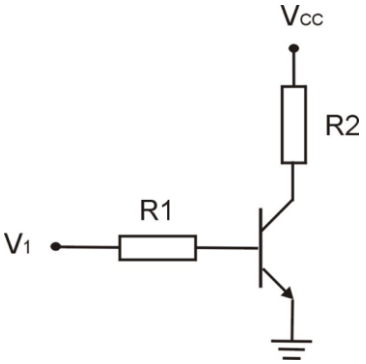


36. The circuit of the figure is a logic inverter. What is the minimum value of the input voltage so that transistor saturation is reached? ($V_{1MIN(SAT)}$)

[A] $V_{eMIN(SAT)}$ = 1.2V
[B] $V_{eMIN(SAT)}$ = 1.9V
[C] $V_{eMIN(SAT)}$ = 3.7V
[D] $V_{eMIN(SAT)}$ = 5V

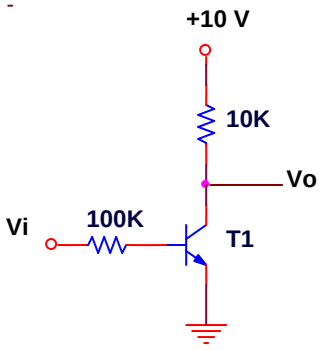
Datos:

β: 100
R1= 100k
R2= 4k
Vcc= 5V
V_{BEON}= 0.7, V_{CESAT}=0.2V



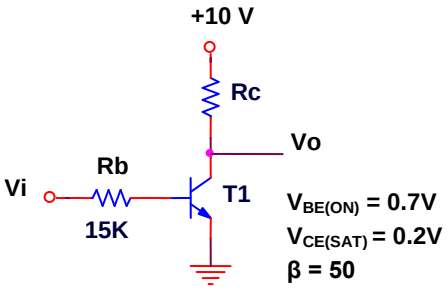
37. Given the circuit of the figure, calculate the value of the limits of the input voltage Vi that lead the transistor to switching mode (Vi_{OFF}, Vi_{SAT})

DATA:
$V_{CE(SAT)} = 0.2V$
$V_{BE(ON)} = 0.7V$
$\beta = 50$;



38. The input Vi of the following circuit varies between 0V and 5V (corresponding to an logic '0 'and '1 ' respectively). For which of the following values of R_C can ensure that the circuit works on switching mode (from cut-off and saturation regions)?

[A] 0.2K
[B] 0.5K
[C] 0.6K
[D] 5K



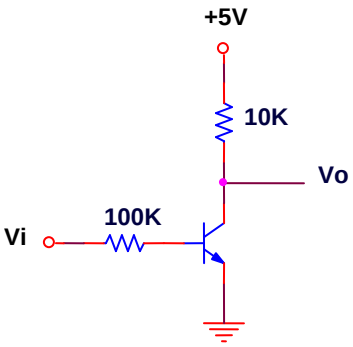
39. What will be the output of the following circuit if the input is a square wave with amplitude from 0V to 2V? (Data: $\beta = 100$; $V_{CE\ SAT} = 0.2V$; $V_{BE\ ON} = 0.7V$).

[A] A square wave with an amplitude from 0.7V to 5V.

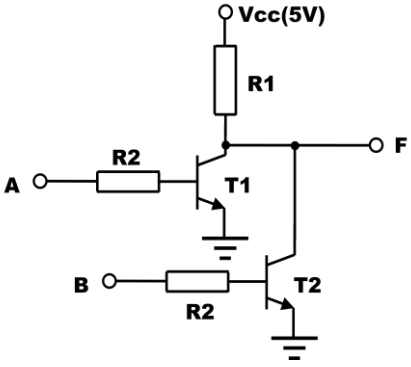
[B] A sine wave of same frequency and reverse phase.

[C] A square wave with an amplitude from 0.2V to 5V.

[D] A square wave with an amplitude from 2V to 5V.



40. Given the circuit of the figure:



DATA: $V_{BE(ON)}$ = 0.6V; $V_{CE(SAT)}$ = 0.2V; R1 = 1k; R2 = 200k; β = 500.
Inputs (“1”-> 5V; “0”-> 0V)

a) For each combination of inputs A and B, analyze the state of the transistors T1 and T2 and complete the truth table of the circuit.
b) Derive the logical function (F).
c) For each combination of inputs A and B, obtain the value of the output voltage.

A	B	T1	T2	F	V_F (Volts)
0	0				
0	1				
1	0				
1	1				

d) Determine the limit values of the input voltages if the transistors work in switching mode (from cut-off and saturation modes).

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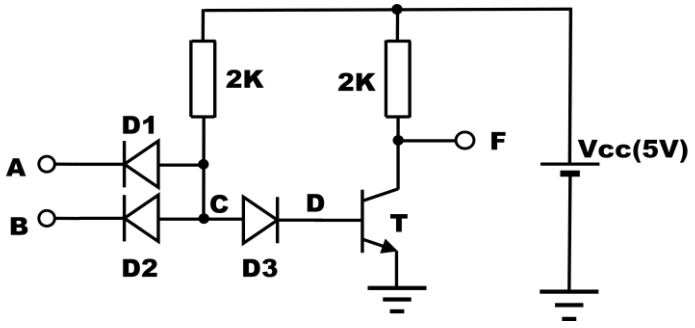
41. The following circuit implements a two-input logic gate: A and B are the inputs and F the output (F):

    a) Obtain the truth table of the circuit and infer which type of logic gate is. Inputs ("1" -> 5V; "0"-> 0V)
    b) Calculate approximately the voltage in the signaled points and the current of all branches, for each combination of inputs.
    DATA: $V_{BE(ON)}$ = 0.7V; $V_{CE(SAT)}$ = 0.2V, β=50. Diodes: Vγ=0.7V



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42. Given the circuit of the previous figure, which corresponds to a logic gate implemented in DTL technology, obtain the voltage in the signaled points and the current of all branches for each combination of inputs, with an output load in F equal to:
    a) 1 similar gate
    b) 5 gates
    c) 10 gates

DATA: Transistor: $V_{BE(ON)}$ = 0.7V; $V_{CE(SAT)}$ = 0.2V; β = 50
Diodes: Vγ=0.7V; I_S = 40μA