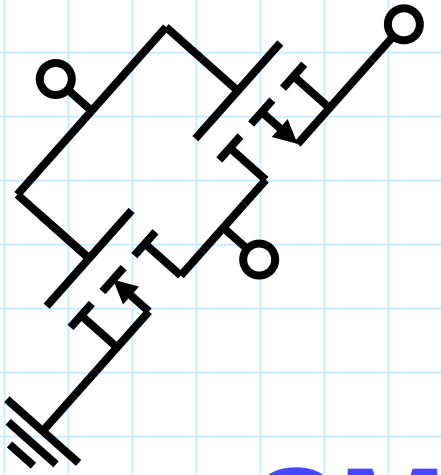


Unit 4:
CMOS technology foundations

Objectives

At the end of this Unit, the student should:

- Know and understand the design of CMOS integrated circuits
  - Complementary CMOS logic
  - Logic design based on transmission gates
- Know a wide range of CMOS logic circuits
  - Combinational, sequential, RAM memory cells
- Know how to characterize electrically the CMOS integrated circuits
  - Parameters of voltage, current, delay and power consumption
  - Special outputs: open drain, tri-state.
- Know the main CMOS subfamilies
  - Buffered outputs, high speed, low voltage, etc.
- Understand the foundations of design and manufacture of VLSI chips

Contents

Bibliography

- Theory
  - “Digital design”. Wakerly. Ed. Prentice-Hall. 2006. Chapter 3.
  - “Electronics”. Hambley. Ed. Prentice-Hall. 2002. Chapter 6.
  - “CMOS circuits”. R.M. Marston. Ed. Paraninfo. 1995.
  - “Digital integrated circuits”. Jan Rabaey et al. Ed. Prentice-Hall. 2004.
  - www.intel.com/technology
  - “International Technology Roadmap for Semiconductors – ITRS09”
- Problems
  - G.Benet; J.V.Benlloch; J.V.Busquets; D.Gil; P.Perez, *Ejercicios Resueltos de Tecnologia de Computadores, Cap.5,* SPUPV 2006.916

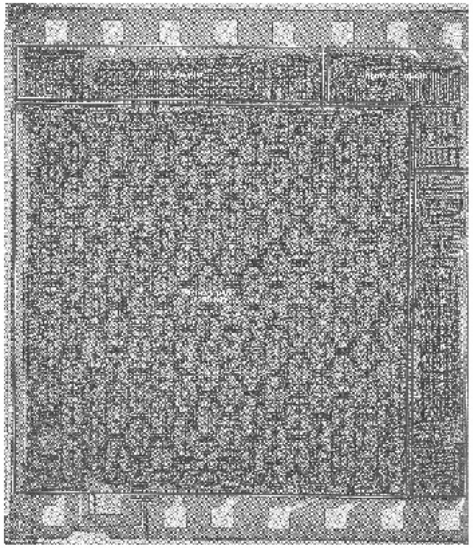
4.1. Introduction

- CMOS is the logic family with more looking forward to future.
- Application scope :
  - Most LSI and VLSI I.C.: Memories and Processors
  - SSI and MSI, together with TTL
- Relevant features
  - Low power consumption
  - Simple manufacturing process
  - Excellent noise immunity
  - Variable supply voltage
  - High Speed subfamilies.

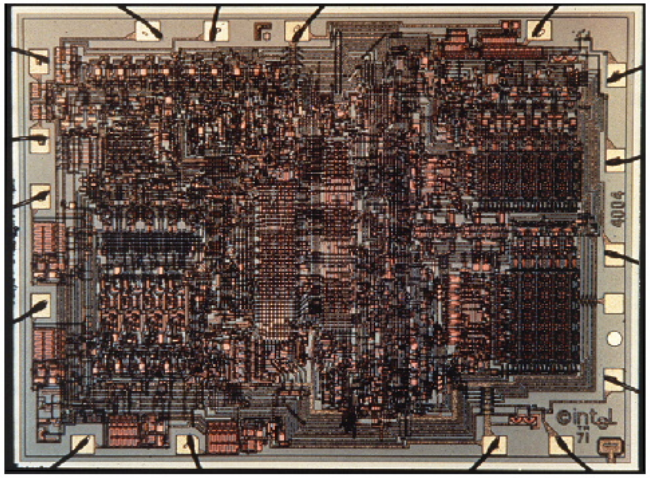
VLSI: Very Large Scale of Integration

4.1. Introduction. Historical evolution

- In 1970's the manufacturing processes for processors and memories was typically based on NMOS transistors
  - Cheap, but have static consumption (When Low level)



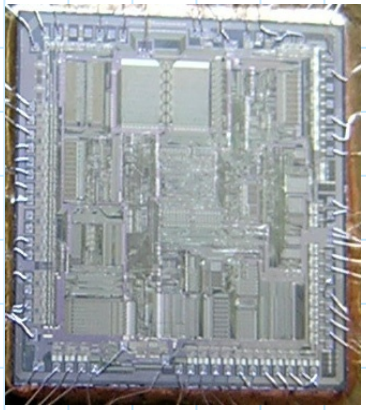
Intel 1101 256-bit SRAM



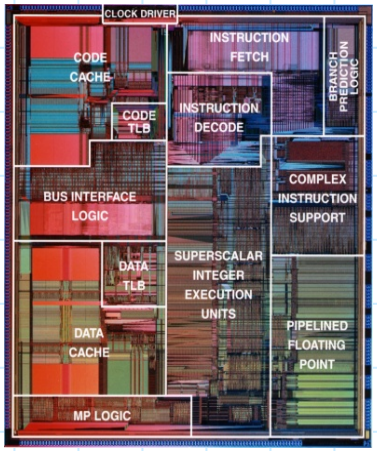
Intel 4004 4-bit μProc

4.1. Introduction. Historical evolution

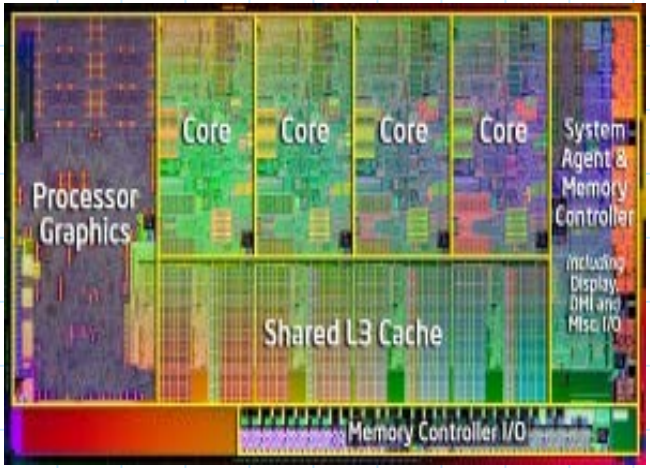
- From 1980's to present: CMOS technology: Low static power



Intel 286



Intel Pentium

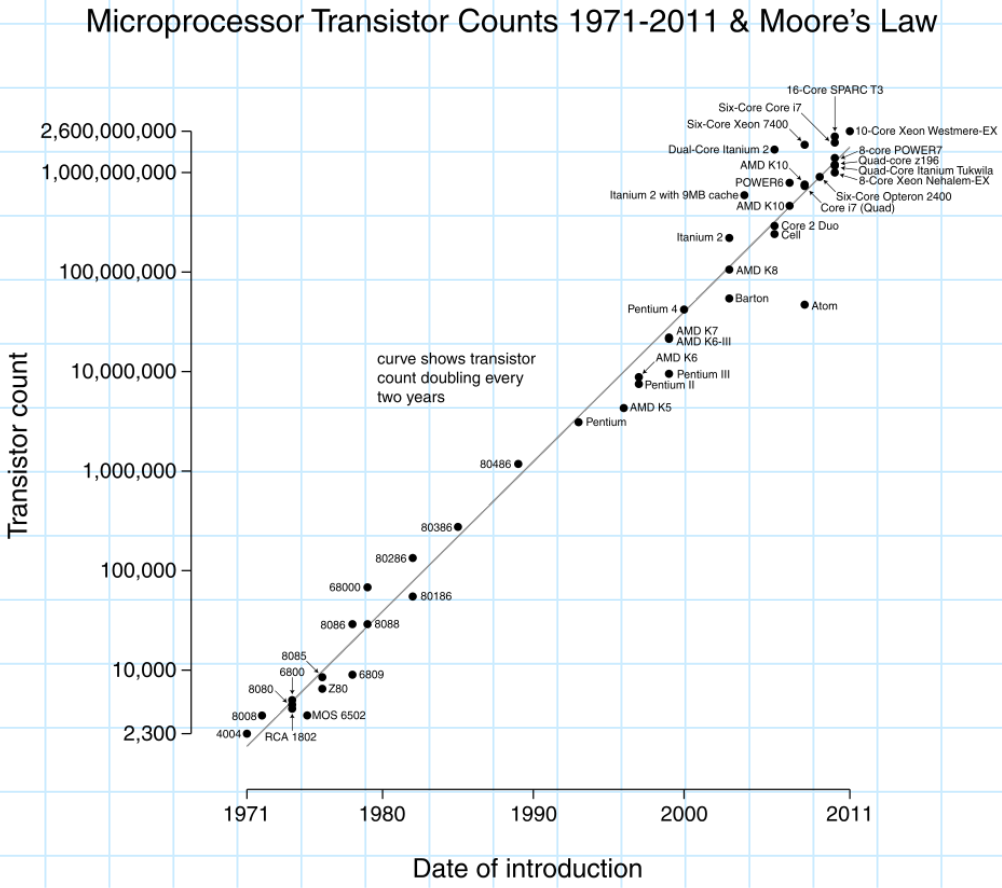


Intel-i7

From 16 bits of data bus: NON-FUNCTIONAL parts (e.g. fault detection)

4.1. Introduction. Moore's law

- 1965: Gordon Moore predicted the evolution of the number of transistors per chip
  - It fits a straight line in a semi-logarithmic scale
  - The number of transistors doubles every 18-24 months

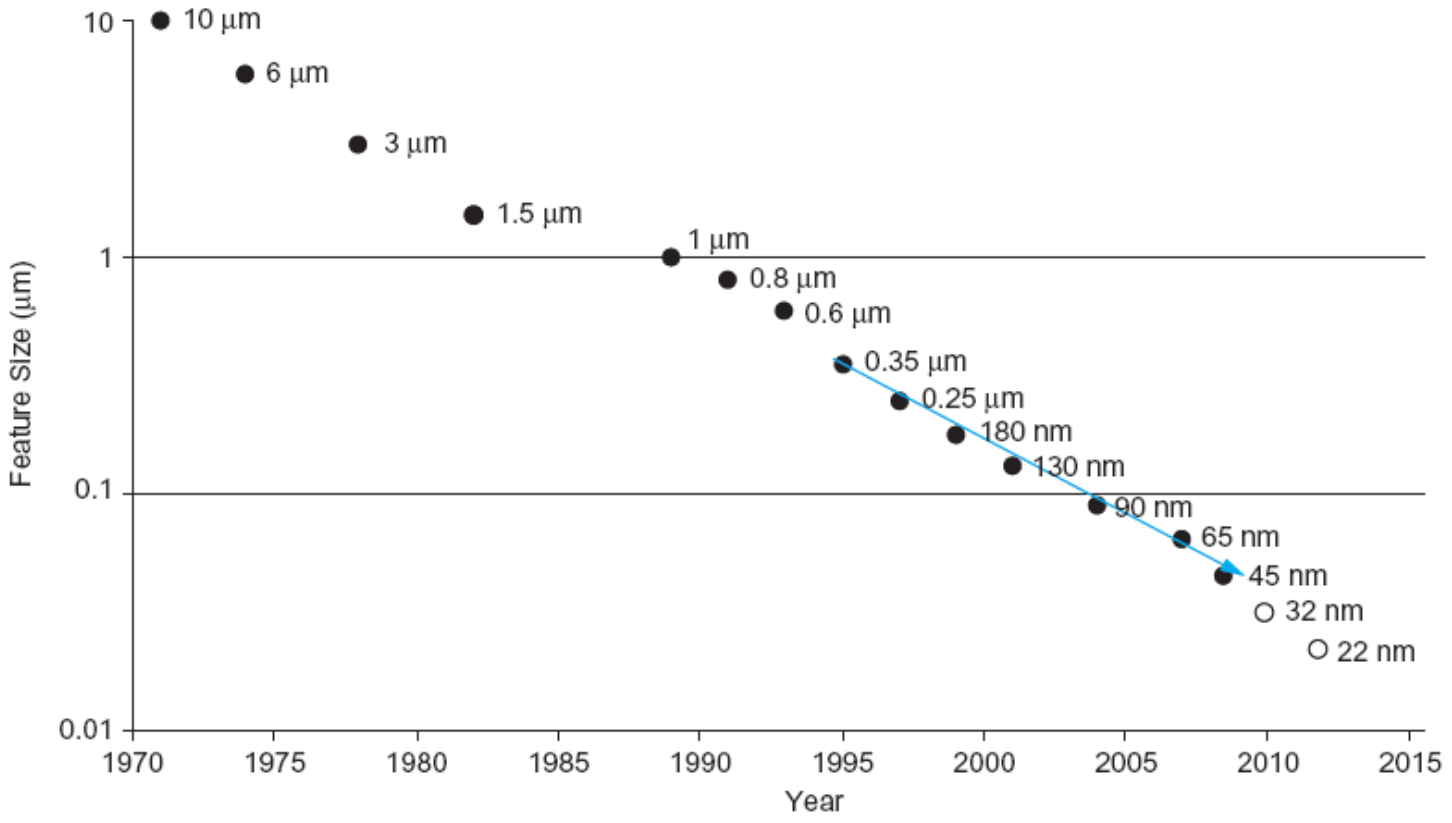


Integration Levels

SSI:	10 gates
MSI:	1000 gates
LSI:	10,000 gates
VLSI:	> 10k gates

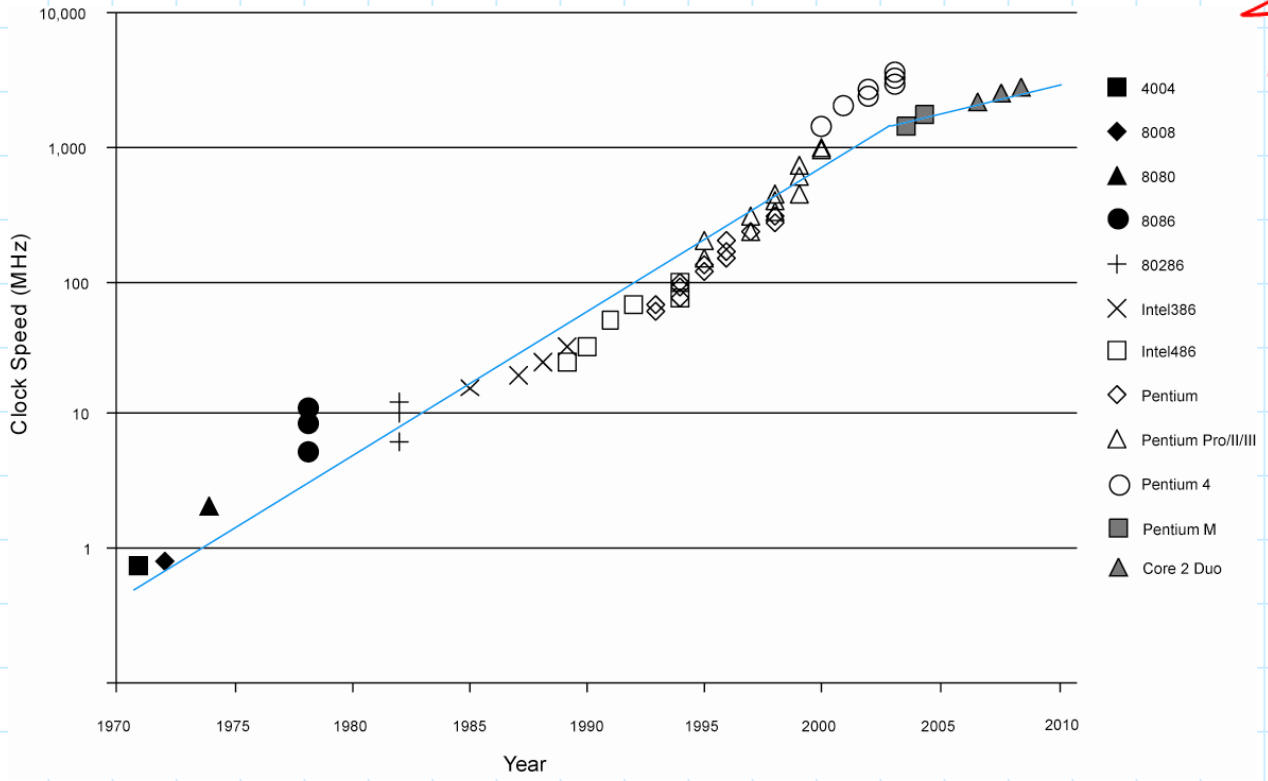
4.1. Introduction. Moore's law

- *Feature Size* brings down an 30% every 2-3 years



4.1. Introducción. Ley de Moore

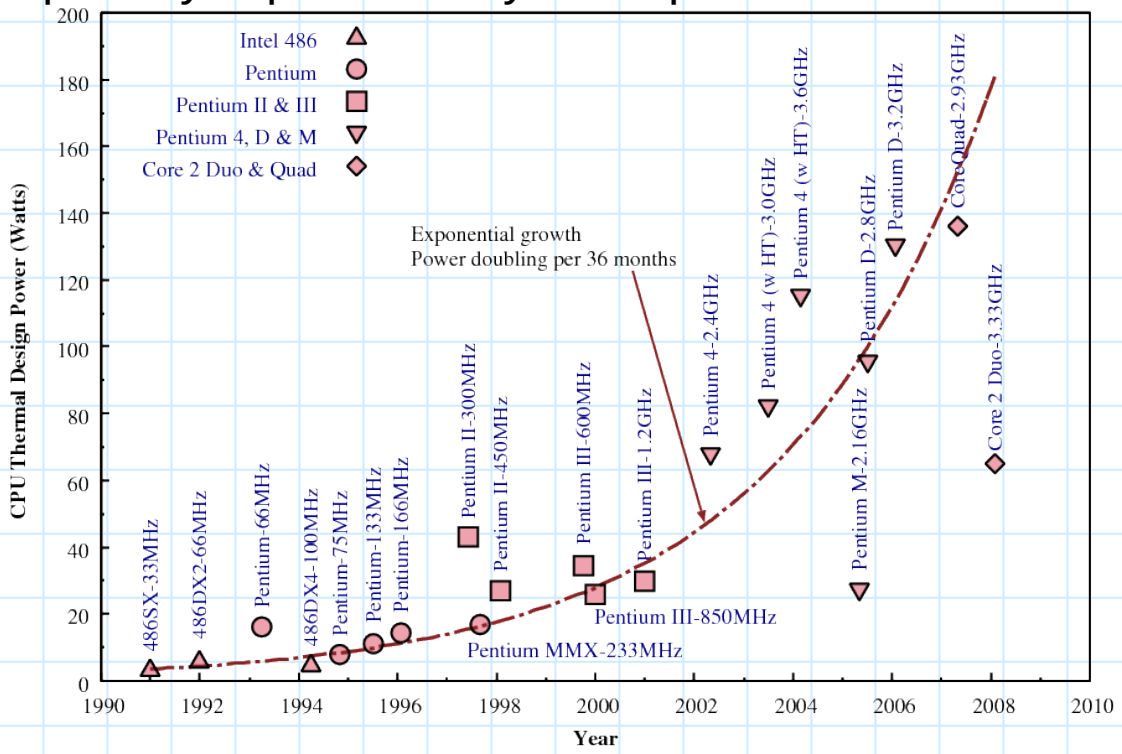
- Many other factors grow exponentially
  - Ex: clock frequency, processor performance



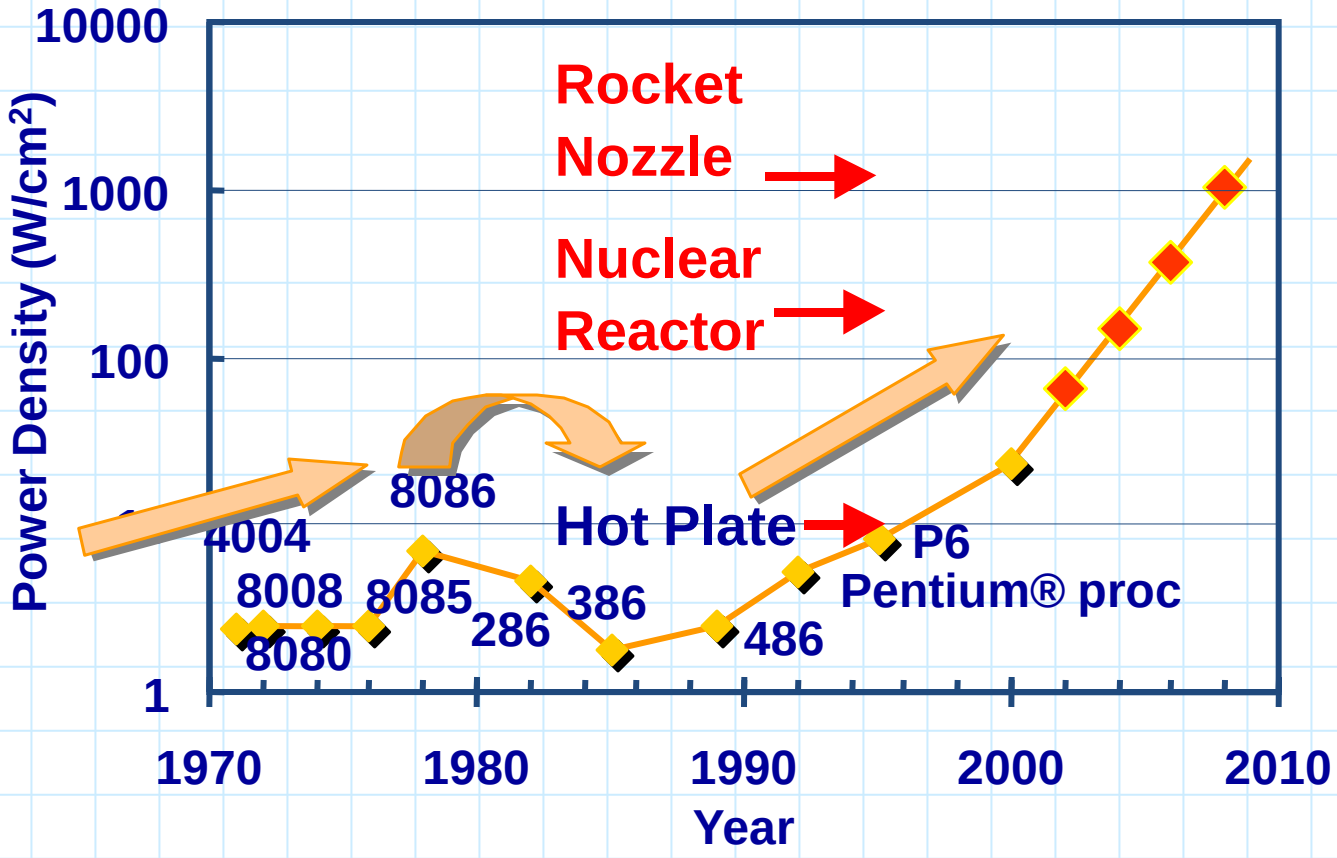
Limit → 2010
(Power disipation)

4.1 Introduction. Power

- The power consumed by chips has also grown exponentially, because:
  - Intensive integration, High frequency
- Power consumption is a key factor, as soon as:
  - Limits the integration density: Heat dissipation
  - It is specially important in systems powered with batteries



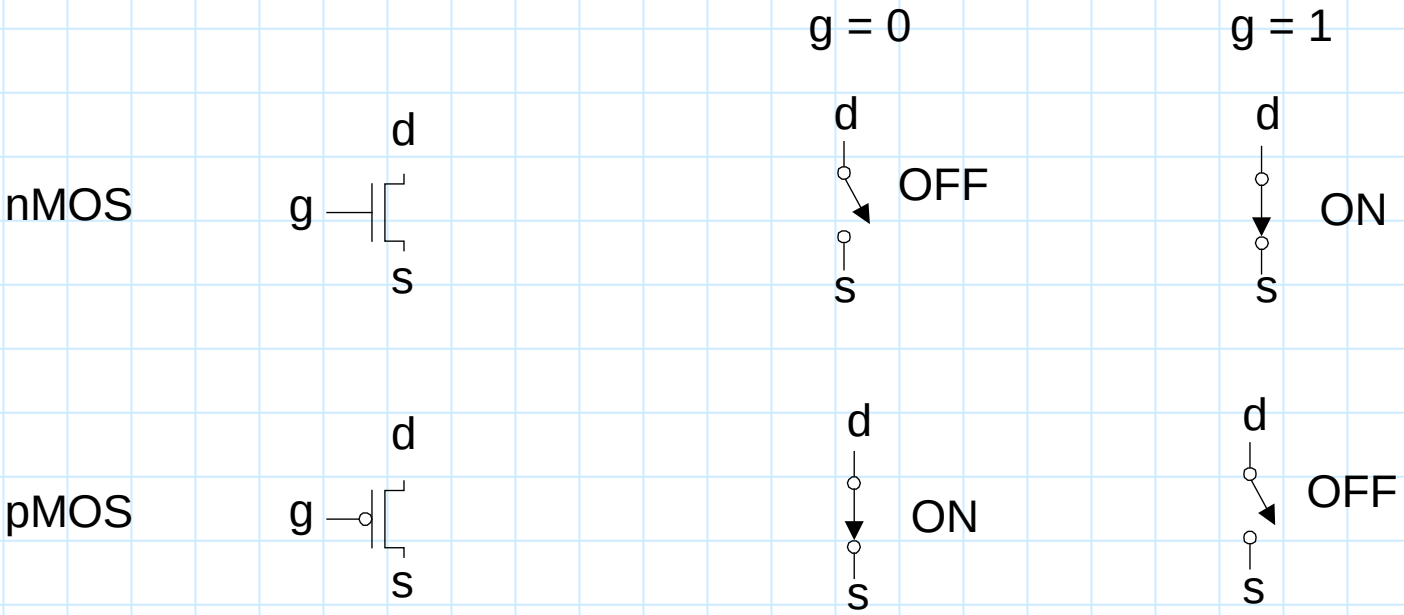
4.1 Introduction. Power density



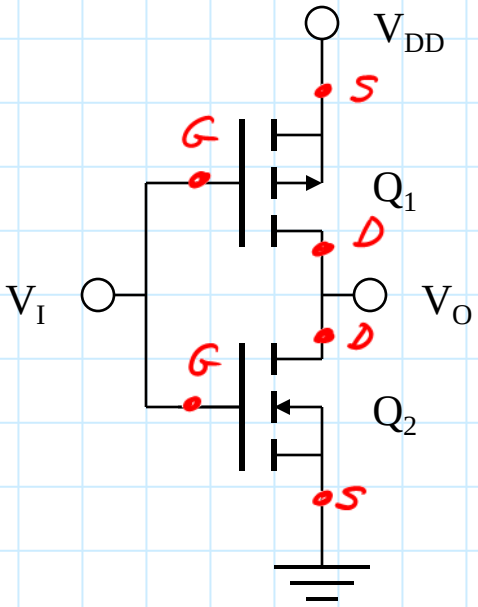
Courtesy, Intel

4.2. Combinational circuits

- MOS transistors as ideal switches: (SW)
  - MOS transistors can be seen as voltage-controlled switches (model); $R_{ON} \simeq 0$ (closed SW); $R_{OFF} \simeq \infty$ (open SW)
  - The gate voltage controls the connection between drain and source terminals

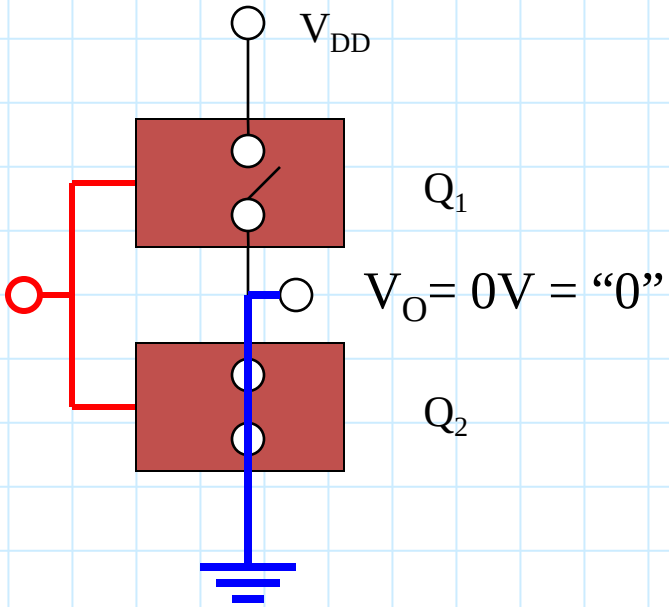


4.2.1 The CMOS inverter (review)



Digital input: $V_I = 0V = \text{“0”}$ $V_I = V_{DD} = \text{“1”}$

4.2.1 The CMOS inverter (review)



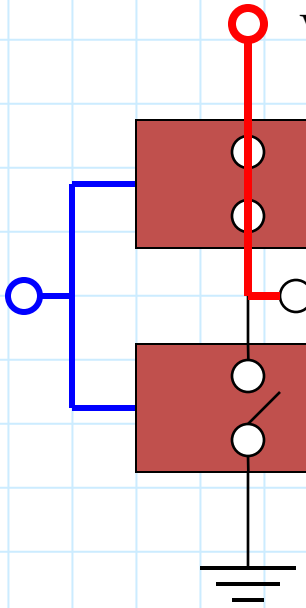
$V_{GS1} = V_{DD} - V_{DD} = 0V > -V_T$ ⇨ PMOS **OFF**

$V_{GS2} = V_{DD} - 0V = V_{DD} > V_T$ ⇨ NMOS **ON**

Static power consumption = 0 mW

(Except leakage)

4.2.1 The CMOS inverter (review)



$V_I = 0V = \text{“0”}$

$V_O = V_{DD} = \text{“1”}$

$V_{GS1} = 0V - V_{DD} = -V_{DD} < -V_T \Rightarrow$ PMOS **ON**

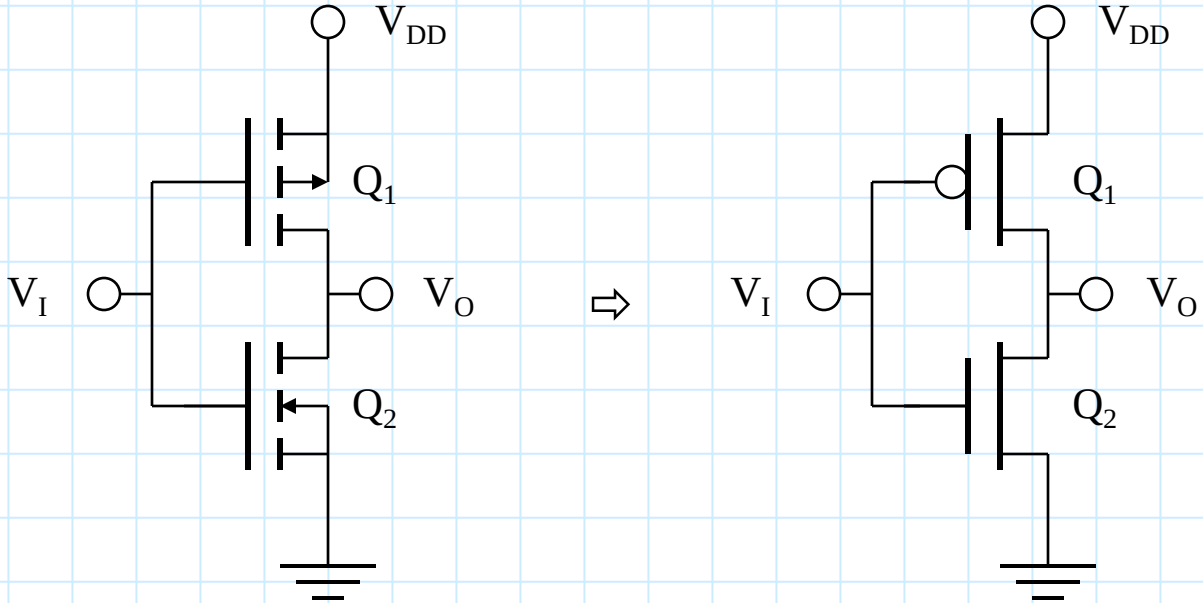
$V_{GS2} = 0V - 0V = 0V < V_T \Rightarrow$ NMOS **OFF**

Static power consumption = 0 mW

(Except leakage)

4.2.1 The CMOS inverter (review)

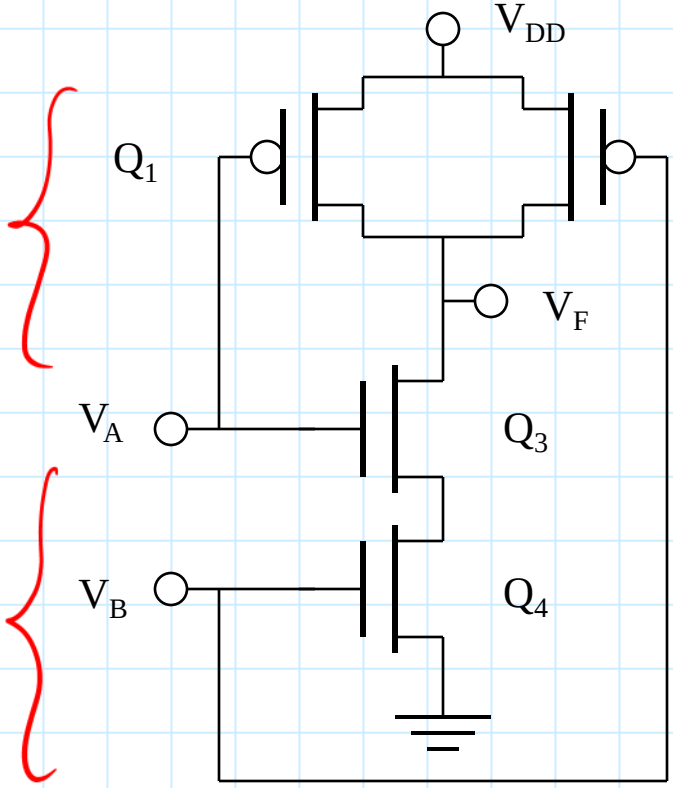
- An easier symbol for MOS transistors



Substrates { p-channel: connected to V_{SS}
n-channel: connected to GND.

4.2.2 Other logic gates. NAND CMOS

- Structure: PMOS transistors in parallel and NMOS in series



PMOS NET

NMOS NET

NMOS: V_F will be "0" if both V_A AND V_B are "1": $\bar{F} = A \cdot B$

$F = \overline{A \cdot B}$

PMOS: V_F will be "1" if V_A OR V_B are "0"

$F = \bar{A} + \bar{B} \Rightarrow F = \overline{A \cdot B}$

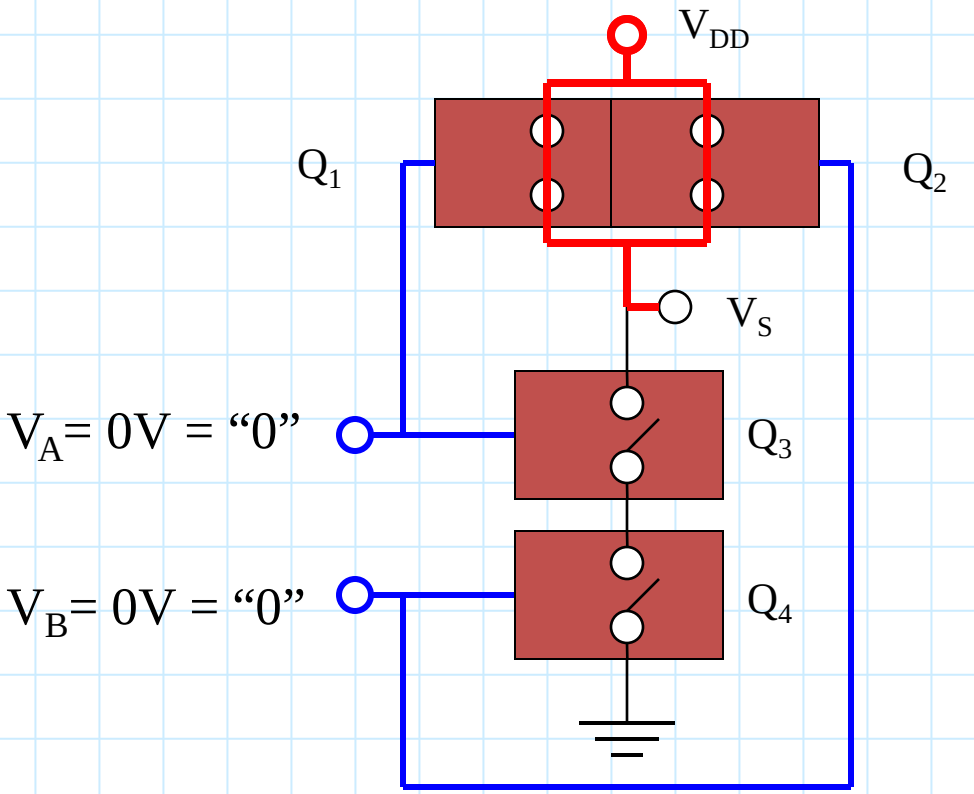
AND: SERIES transistors

OR: PARALLEL "

NMOS and PMOS nets are DUAL

NMOS series $\rightleftharpoons$ PMOS parallel

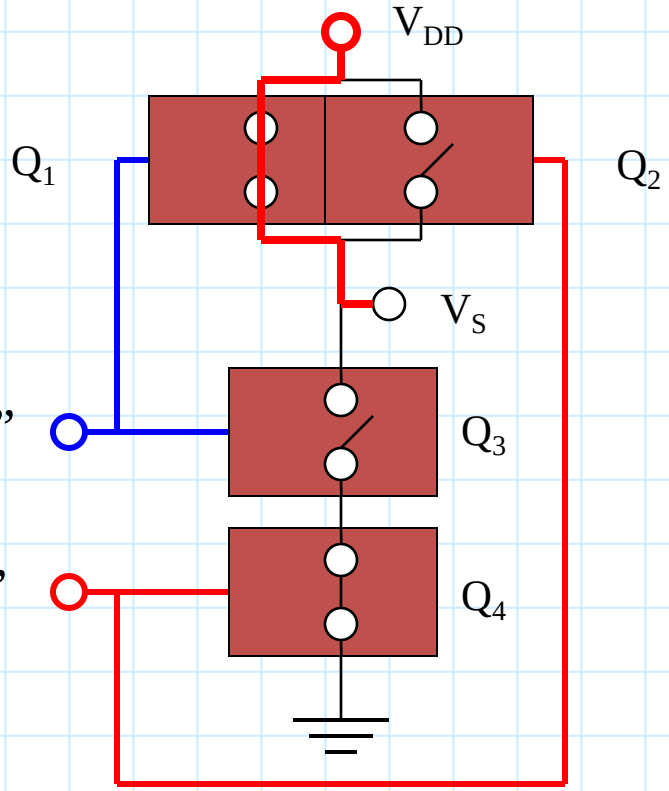
4.2.2 Other logic gates. NAND CMOS



V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	V_{DD}
V_{DD}	0V	V_{DD}
V_{DD}	V_{DD}	0V

Static power consumption = 0 mW

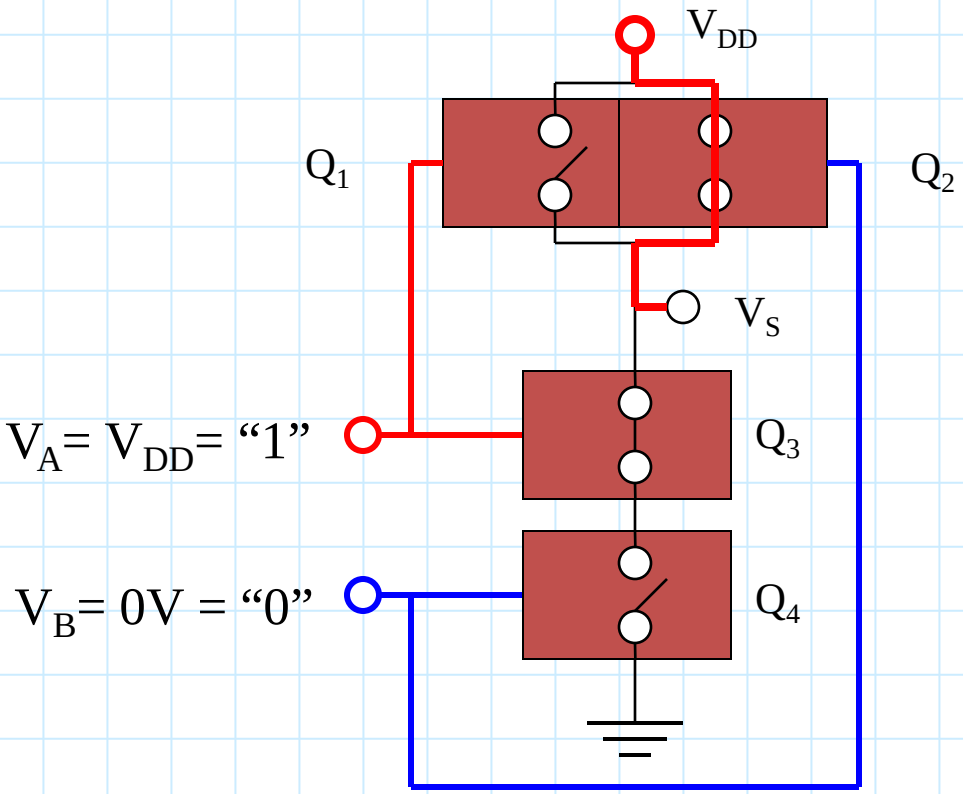
4.2.2 Other logic gates. NAND CMOS



V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	V_{DD}
V_{DD}	0V	V_{DD}
V_{DD}	V_{DD}	0V

Static power consumption = 0 mW

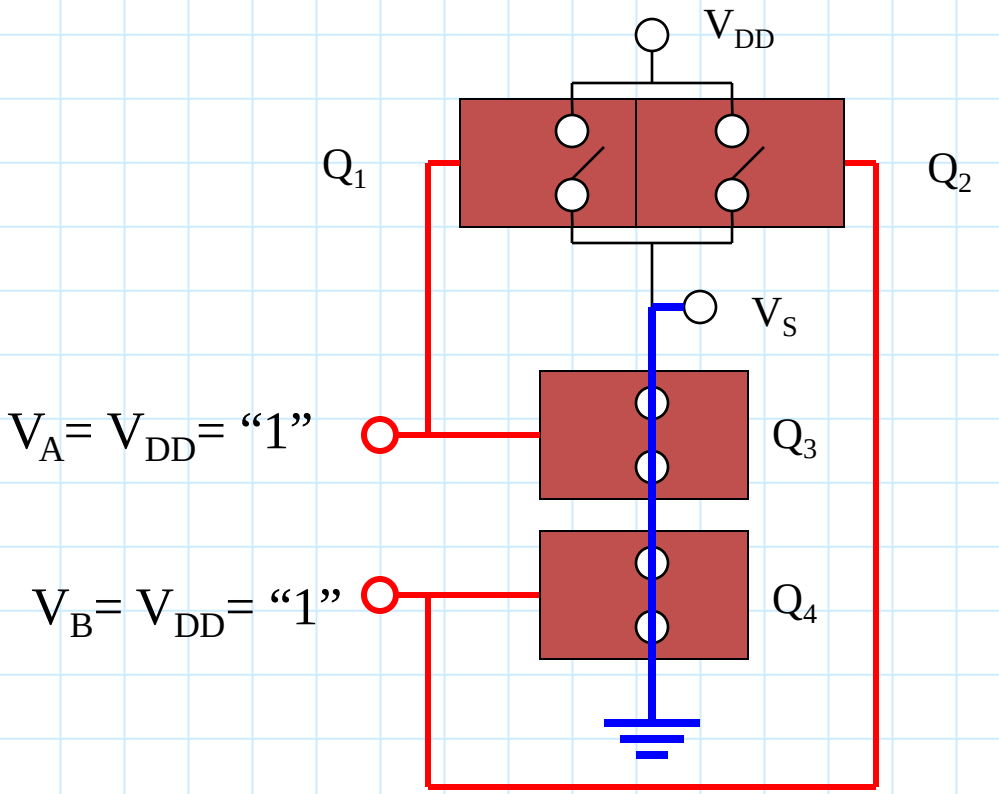
4.2.2 Other logic gates. NAND CMOS



V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	V_{DD}
V_{DD}	0V	V_{DD}
V_{DD}	V_{DD}	0V

Static power consumption = 0 mW

5.2.2 Other logic gates. NAND CMOS

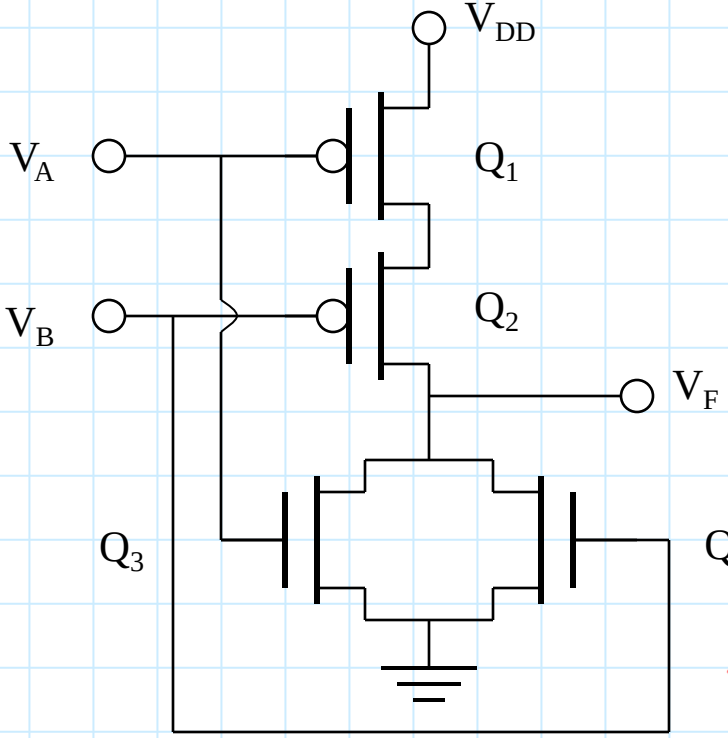


V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	V_{DD}
V_{DD}	0V	V_{DD}
V_{DD}	V_{DD}	0V

Static power consumption = 0 mW

4.2.2 Other logic gates. NOR CMOS

- Structure: NMOS transistors in parallel and PMOS in series



NMOS: V_F will be "0" if V_A OR V_B are "1": $\bar{F} = A + B$

$F = \overline{A+B}$

PMOS: V_F will be "1" if both V_A AND V_B are "0"

$F = \bar{A} \cdot \bar{B} \Rightarrow F = \overline{A+B}$

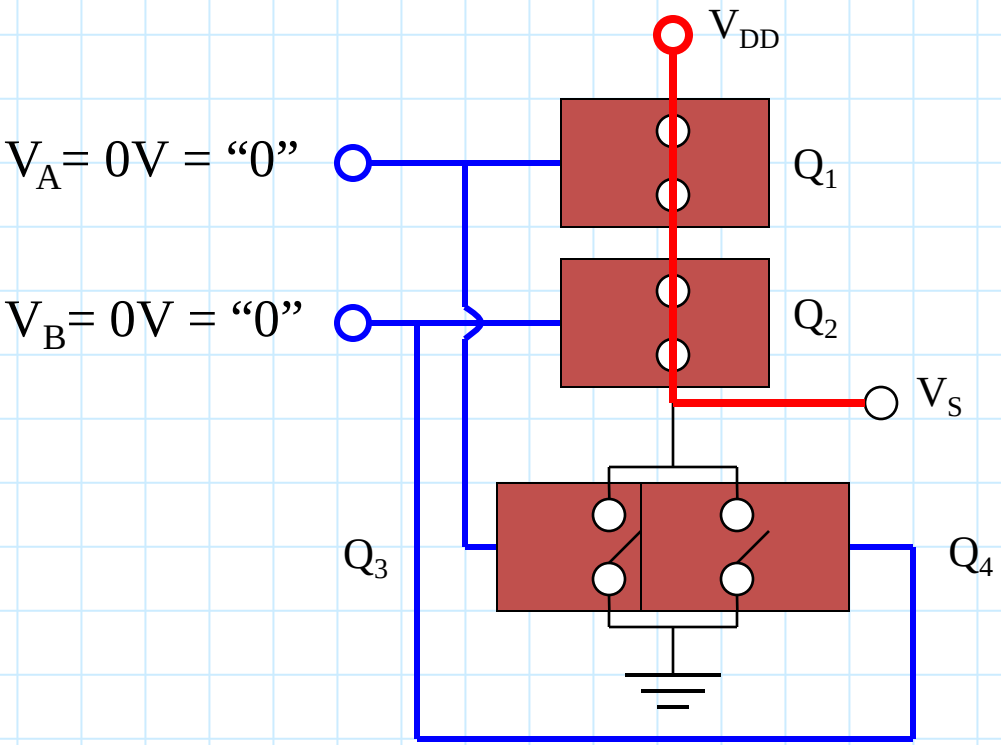
AND: SERIES transistors

OR: PARALLEL "

NMOS and PMOS nets are DUAL

NMOS series $\rightleftharpoons$ PMOS parallel

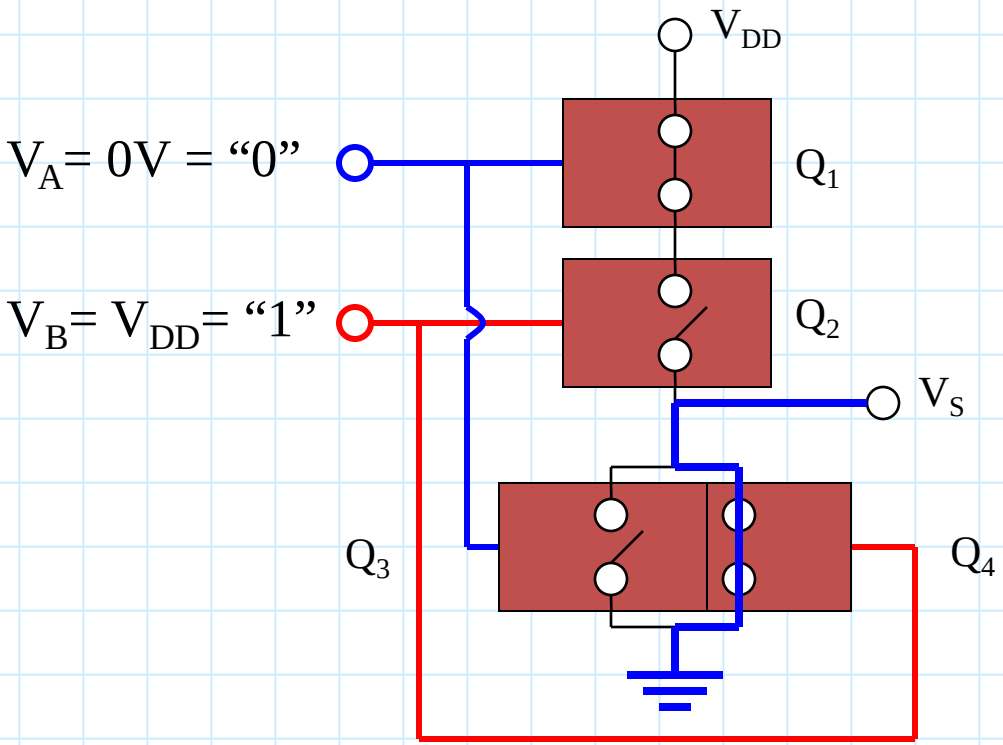
4.2.2 Other logic gates. NOR CMOS



V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	0V
V_{DD}	0V	0V
V_{DD}	V_{DD}	0V

Static power consumption = 0 mW

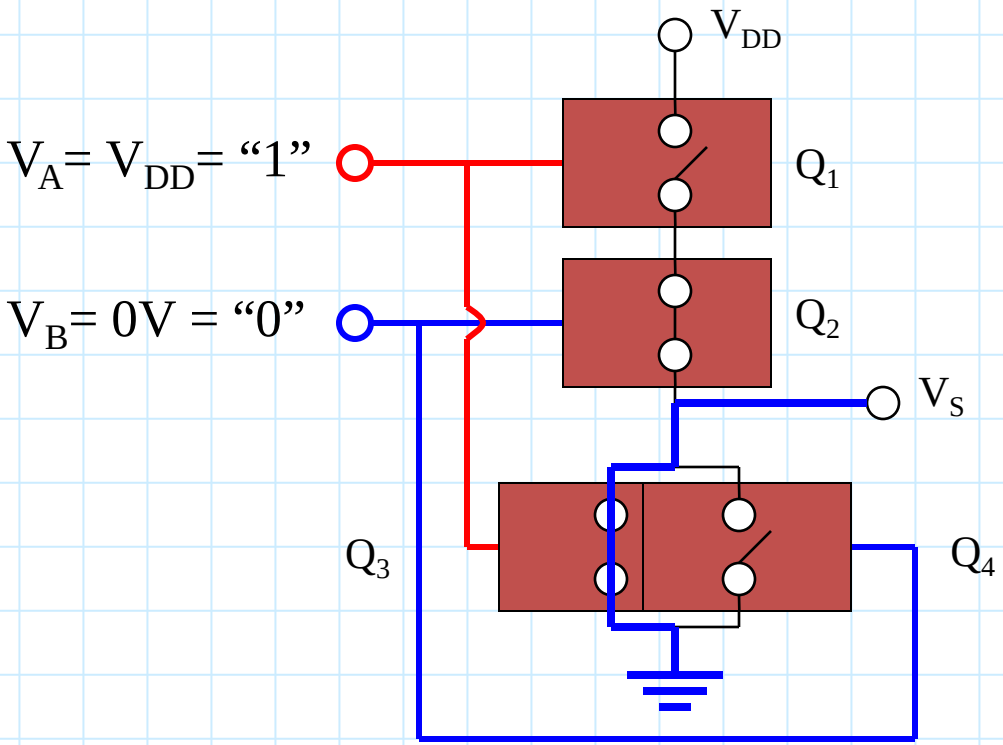
4.2.2 Other logic gates. NOR CMOS



V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	0V
V_{DD}	0V	0V
V_{DD}	V_{DD}	0V

Static power consumption = 0 mW

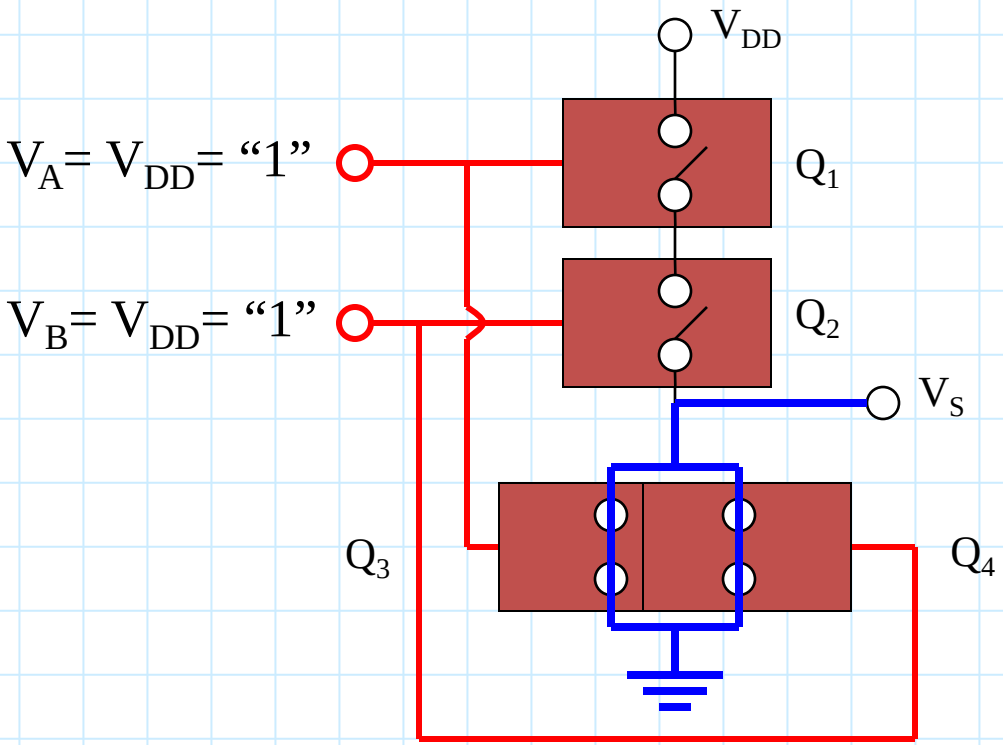
4.2.2 Other logic gates. NOR CMOS



V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	0V
V_{DD}	0V	0V
V_{DD}	V_{DD}	0V

Static power consumption = 0 mW

4.2.2 Other logic gates. NOR CMOS



V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	0V
V_{DD}	0V	0V
V_{DD}	V_{DD}	0V

Static power consumption = 0 mW

4.2.2 Other basic gates

- Buffer = NOT + NOT → Second NOT gives/ sinks more current than usual
- AND = NAND + NOT
- OR = NOR + NOT