Unit 5
Semiconductor memories Technology

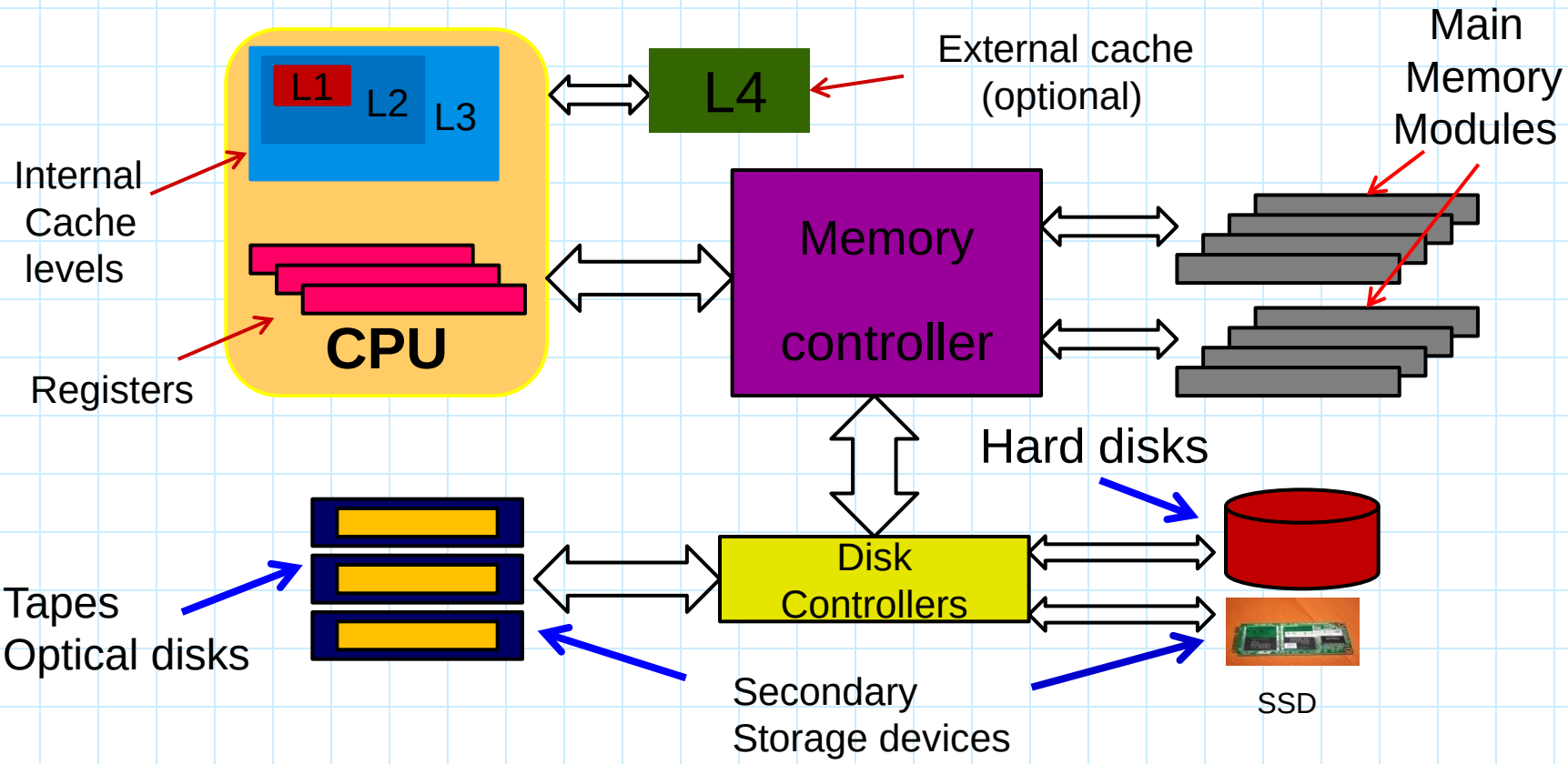
Contents (I)

Bibliography

- Bibliography
  - Floyd, T.L. Digital systems principles. Ed. Prentice Hall, 1997. Ch. 12 y 14.
  - J. F. Wakerly. Digital design. Ed. Prentice-Hall, 2006.
  - Prince, B. Semiconductor memories. A handbook of design manufacture and application. Ed. Wiley,1991
  - R. Tokheim: Digital electronics, Principles and applications. 2010. Ch. 11: Memorias.
  - Jan M. Rabaey. Digital integrated circuits. Ed. Pearson Prentice Hall, 2004.

Memory system of a computer

- The main system memory of a computer usually consists of a set of modules
- The system memory and bus structure are consistent with an organization determined by the processor



1. Basic organization.
1.1. Storage capacity

- Quantity of stored information: bits or bytes
  - Terminology: B = 1 byte, b = 1 bit
- ¿How is expressed the capacity?
  - Overall capacity: bytes or multiples of bytes
- Prefixes
  - Depending on the context, there are of 2^n **type** or 10^n **type**
    - Example: main memory capacity is always expressed in units of the type 2^n

Applicable prefixes :

Name	Value (2^n)	Value (10^n)
Kilo (K)	2^{10}	10^3
Mega (M)	2^{20}	10^6
Giga (G)	2^{30}	10^9
Tera (T)	2^{40}	10^{12}
Peta (P)	2^{50}	10^{15}

1.1. Storage capacity examples

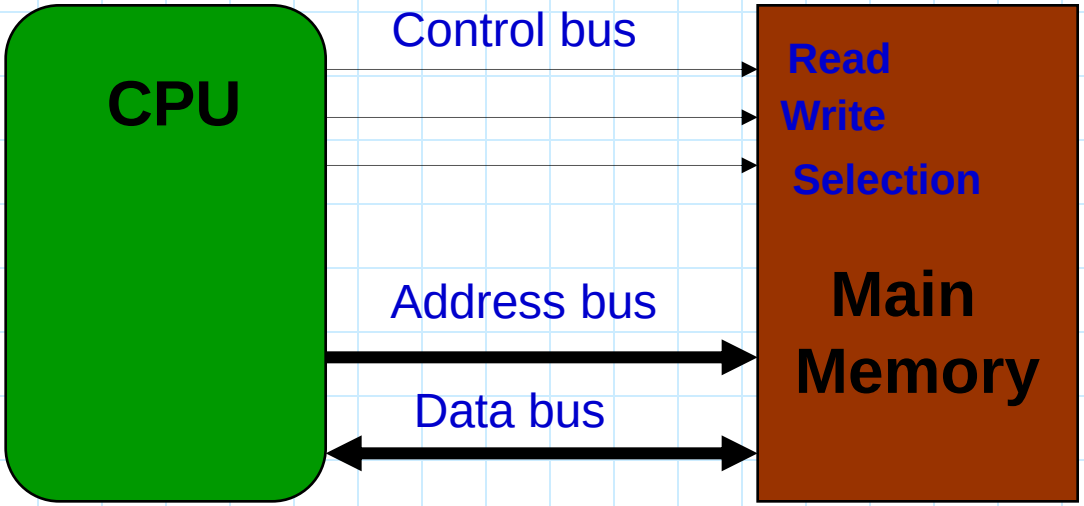
- Overall capacity expressed in bytes
  - 1024 bytes = 2^{10} bytes = 1 KB
- The memory has 128K words of 16 bits each
  - 128K×16 bits = 128K×2^4 bits = 128K×2^1 bytes = 256 KB
- The memory has 8 MB in words of 32 bits
  - 8 MB = 2^3×2^{20}×2^3 bits = 2^1×2^{20}×2^5 bits = 2M×32 bits
- Other examples:
  - 64 Kbits = 64K×1 bits = 2^{16} bits = 2^{13}×2^3 bits = 2^{13} bytes
  - 256 Mbits = 2^8×2^{20} bits = 2^5×2^{20}×2^3 bits = 32 MB

1.1. Information sizes

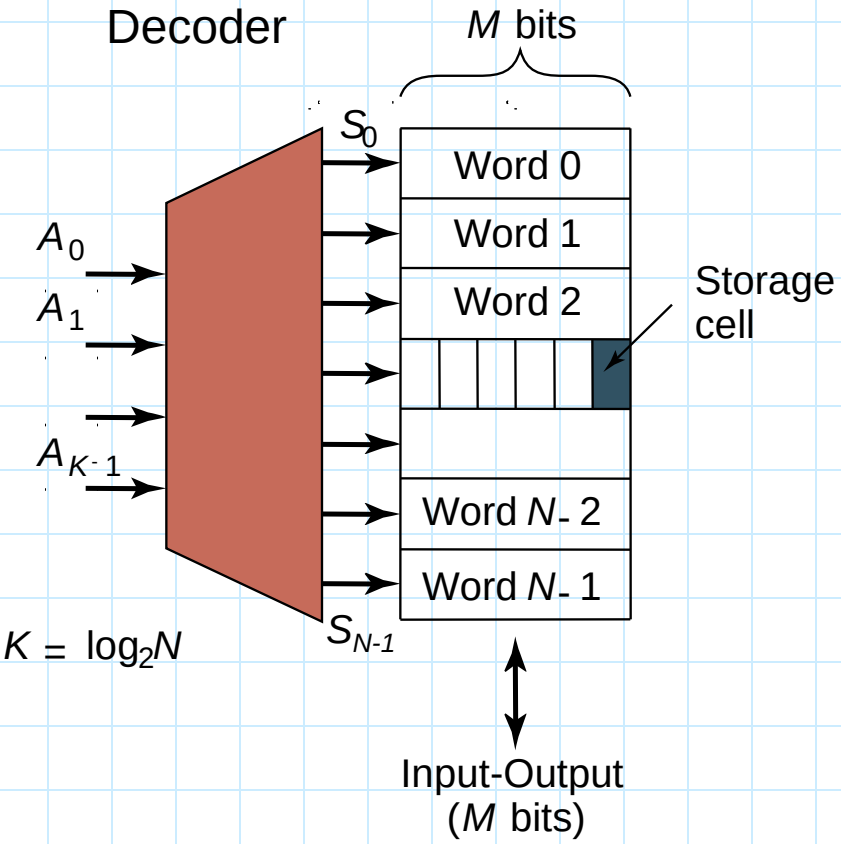
- Word
  - Maximum Transfer Unit in an access
  - The length in bits is usually an integer power of 2 (1, 2, 4, 8, 16, 32, 64)
  - Example
    - Transfers between main memory and processor without cache memory
- Block
  - Set of words to be accessed in a single request
  - Examples
    - Transfers between disk and main memory
    - Transfers between cache and main memory

1.2. CPU-memory interconnection

- Bus Lines
  - **Control:** The CPU selects memory and determines the operation to do (read or write)
  - **Address**: The CPU determines the address
  - **Data**: According to the operation, the data go:
    - In case of reading: from memory to the CPU
    - In case of writing: from the CPU to memory



1.3. Basic structure of semiconductor memories



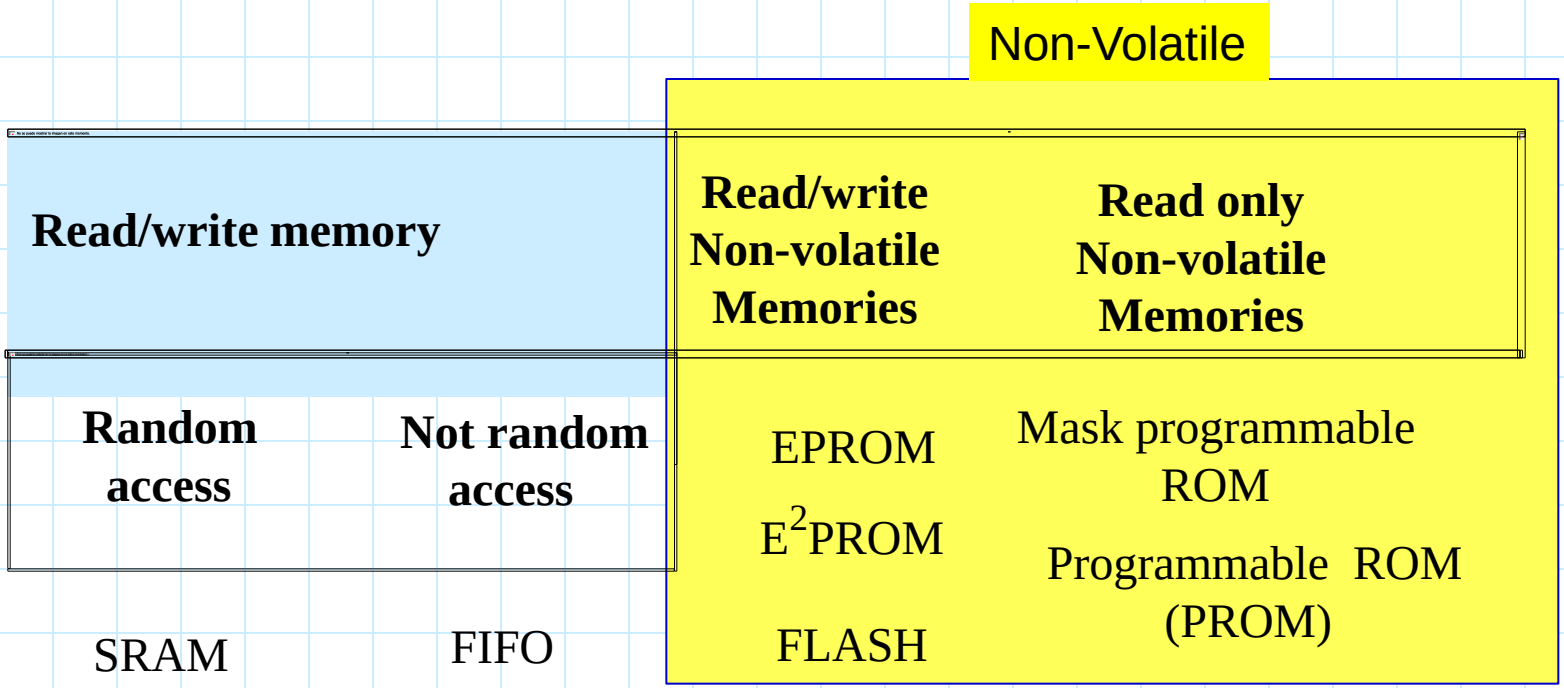
The decoder reduces the number of selection lines (S)

$$K = log_2 N$$

2. Types of semiconductor memories.

Read/write memory		Read/write Non-volatile Memories	Read only Non-volatile Memories
Random access	**Not random access**	EPROM	Mask programmable ROM
		E^2PROM	Programmable ROM (PROM)
SRAM	FIFO	FLASH	
DRAM	LIFO		
	Shift Register		
	CAM		

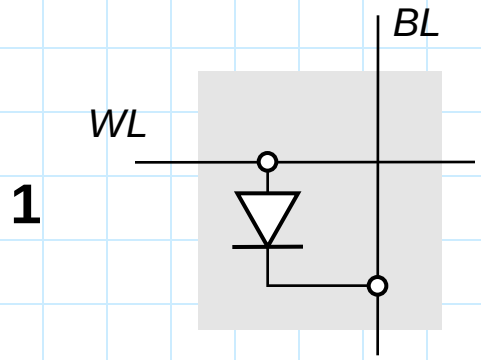
2. Types of semiconductor memories.

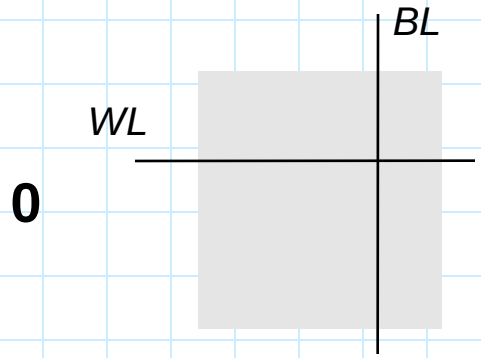


2.1.1. Read-Only Memories (ROM)

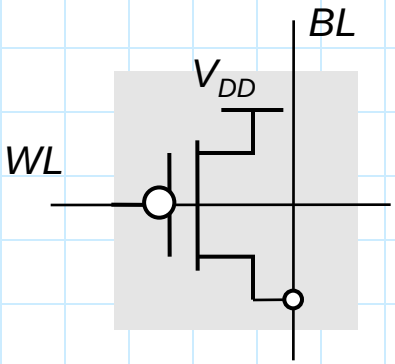
- The mask-programmed ROM have 1 transistor per bit
  - They are programmed during manufacturing.
  - The presence or absence of the transistor determines the '1 'or '0‘
- They are non-volatile
  - Hold their contents when power is removed

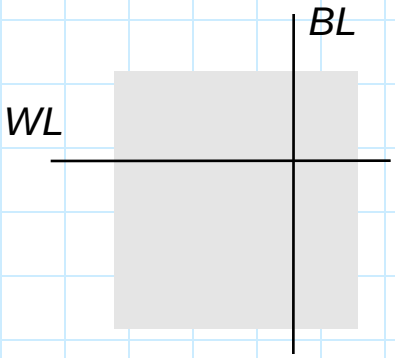
2.1.1. ROM cells



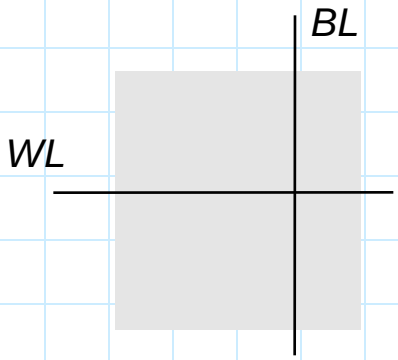


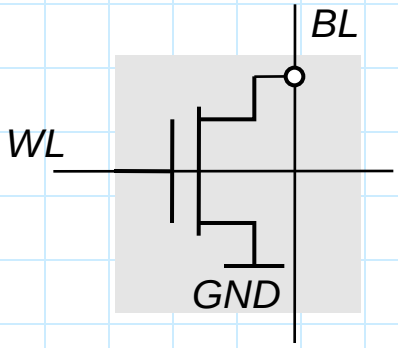
Diode ROM





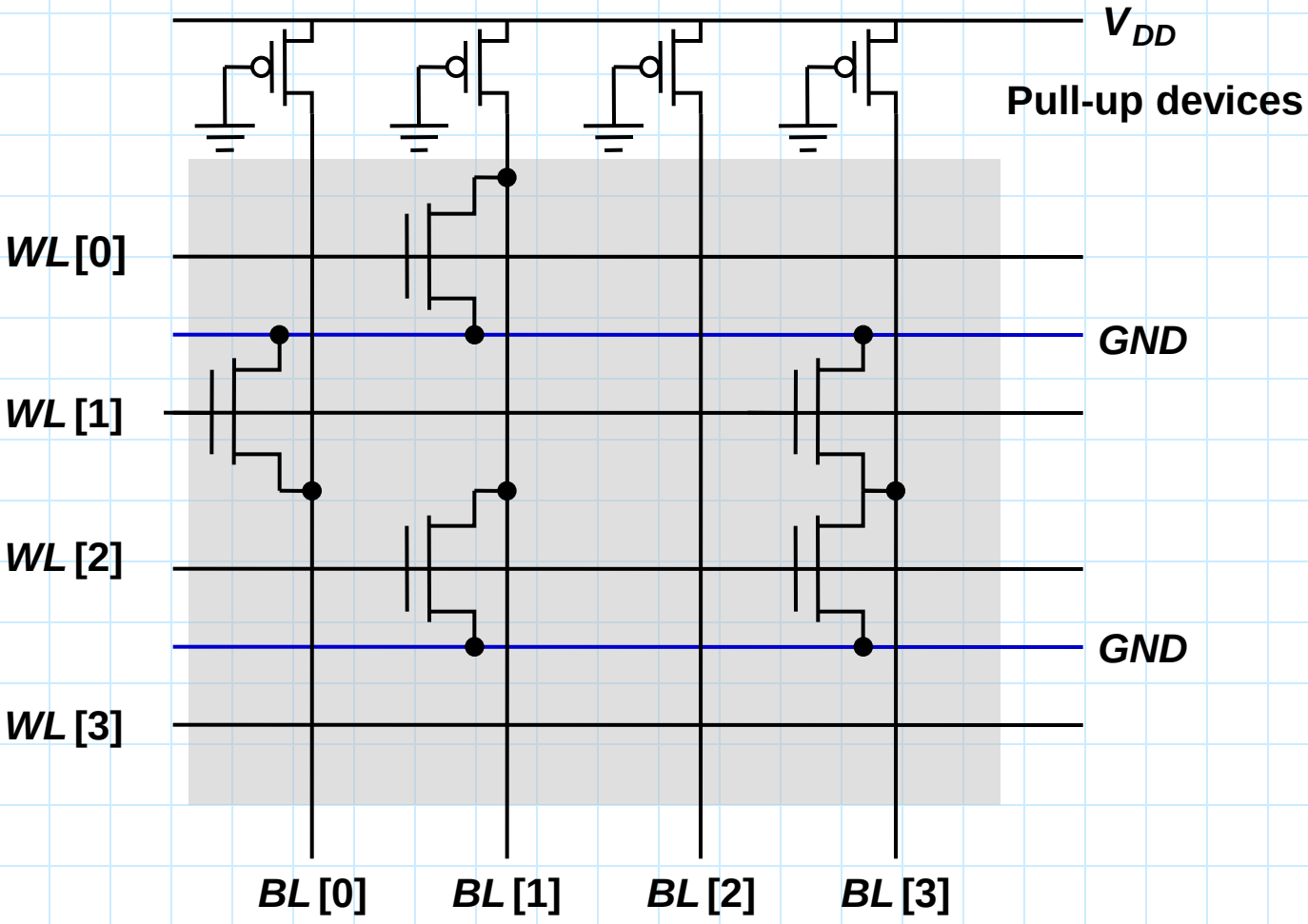
MOS ROM 1





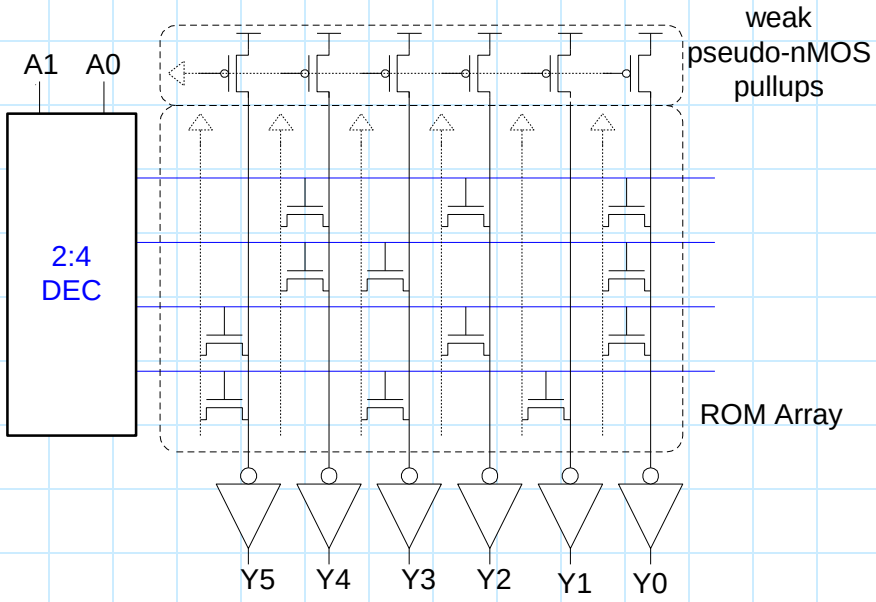
MOS ROM 2

2.1.1. MOS ROM with NOR structure



2.1.1. Example of ROM

- 4-word x 6-bit ROM
  - Dot diagram representation
  - Dots indicate the ROM´s 1's

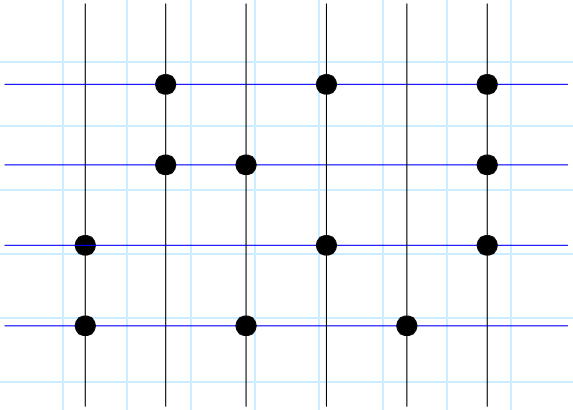


Word 0: **010101**

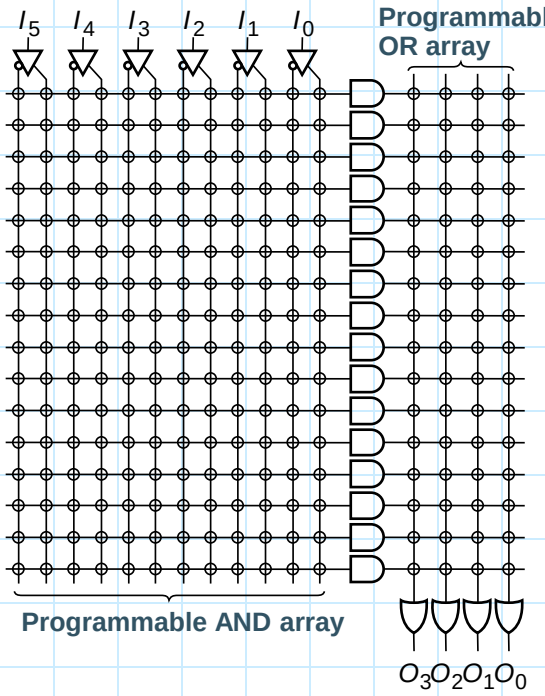
Word 1: **011001**

Word 2: **100101**

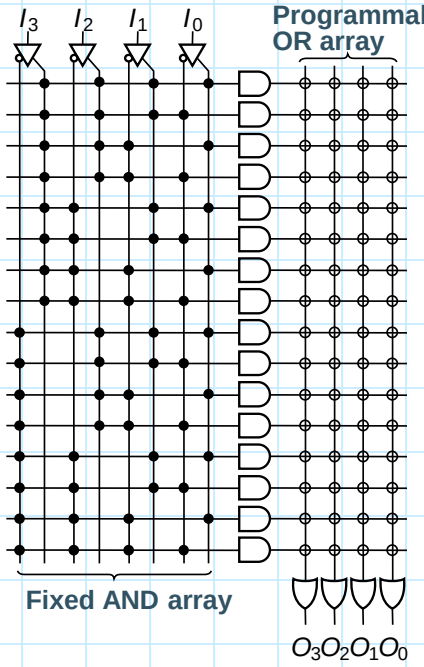
Word 3: **101010**



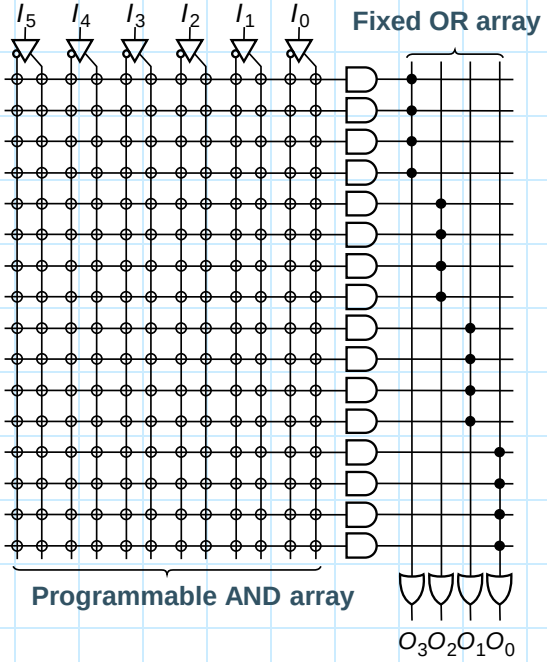
2.1.1 Programable ROM: PROM, PLA, PAL



PLA



PROM



PAL

Programmable connection: transistor with series fuse

Fixed connection: transistor

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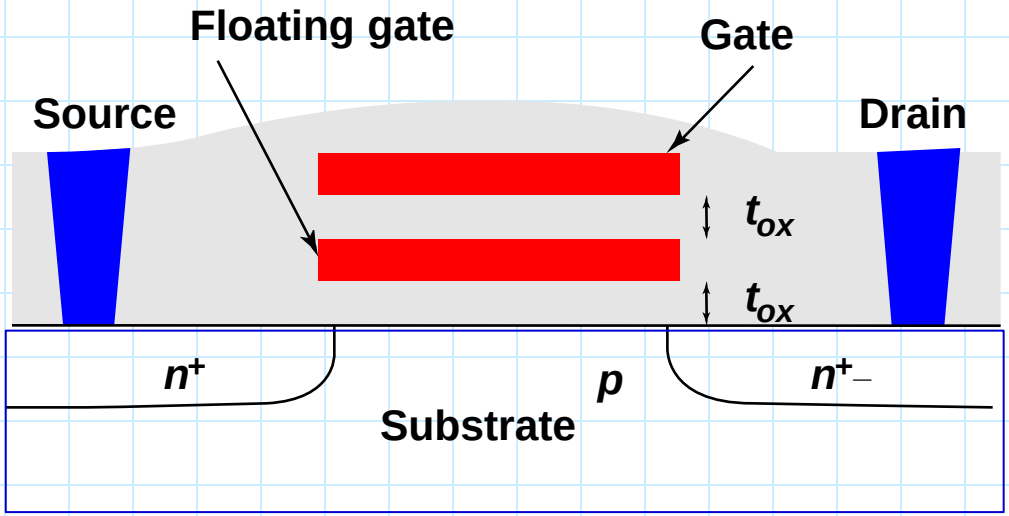
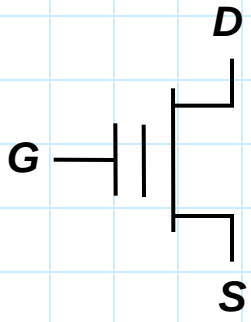
2.1.1. Re-programmable non volatile memories

- Electrically Programmable ROMs (EPROMs)
  - They use a floating gate MOSFET to cut unwanted transistors
  - EPROM, EEPROM, Flash



FAMOS Transistor

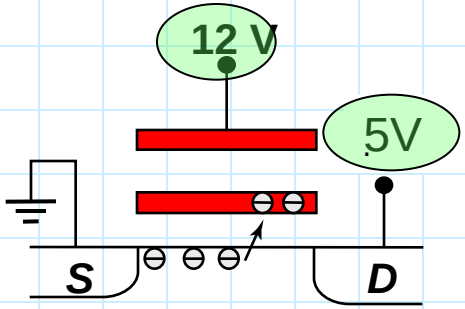


Symbol

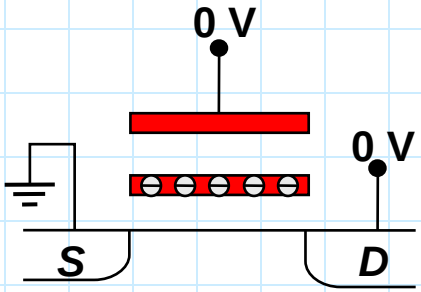
2.1.1. Flash memories

- **Non-volatile** read/write semiconductor memories:
- Applications
  - Pen drives
  - Memory cards in digital cameras
  - Portable Audio (MP3)
  - Mobile Phones
  - Solid state discs
  - ...
- Features
  - Small, cheap, low power consumption and flexible
  - Based on the EEPROM, but allows the erasure block by block
  - Limited number of write and delete cycles

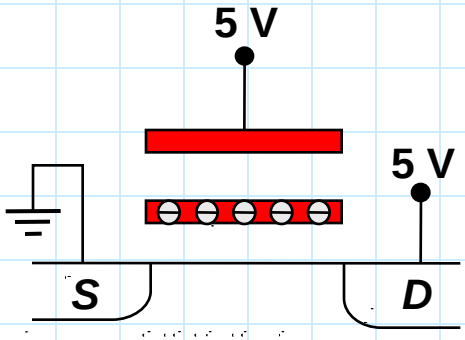
2.1.1. Flash cell: Programming and erasing mechanisms



Programming:
Avalanche injection

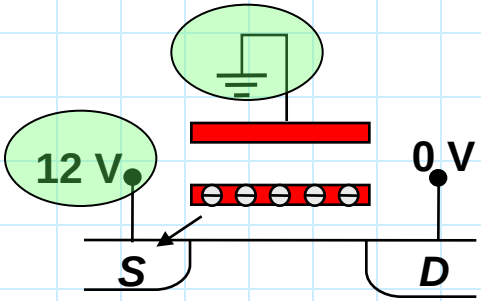


Removing the programming voltage, charge remains Stored in floating gate



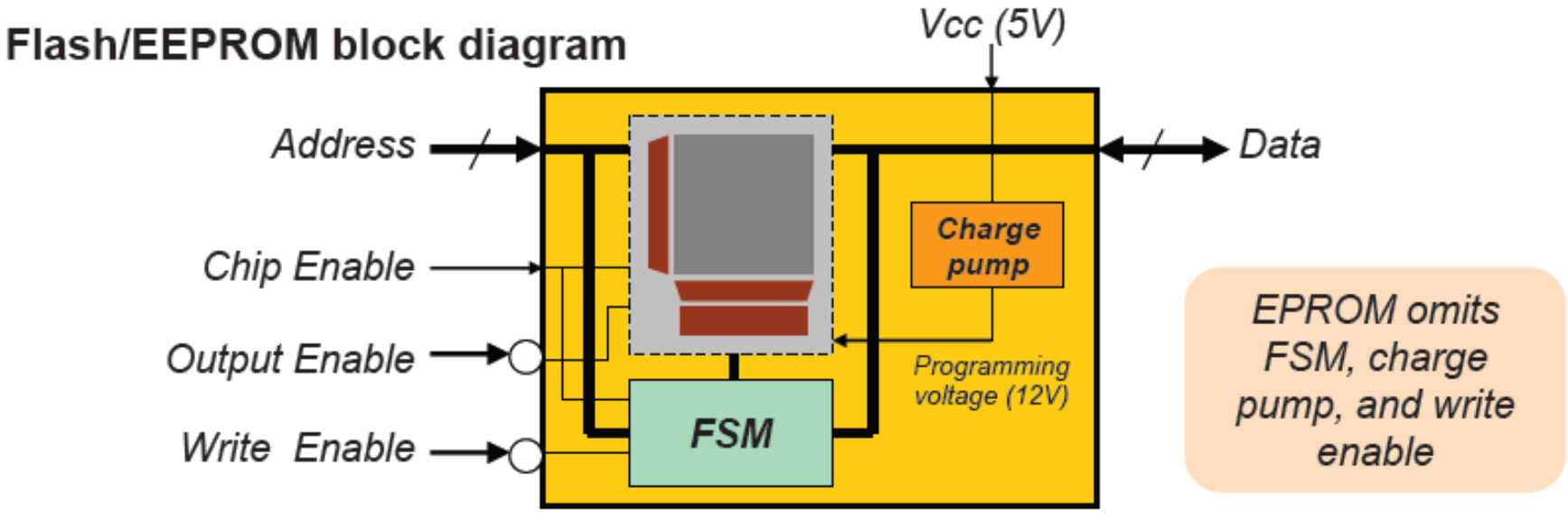
Programming provokes an Vt increment

Transistor always OFF: even when gate control has a "1" level

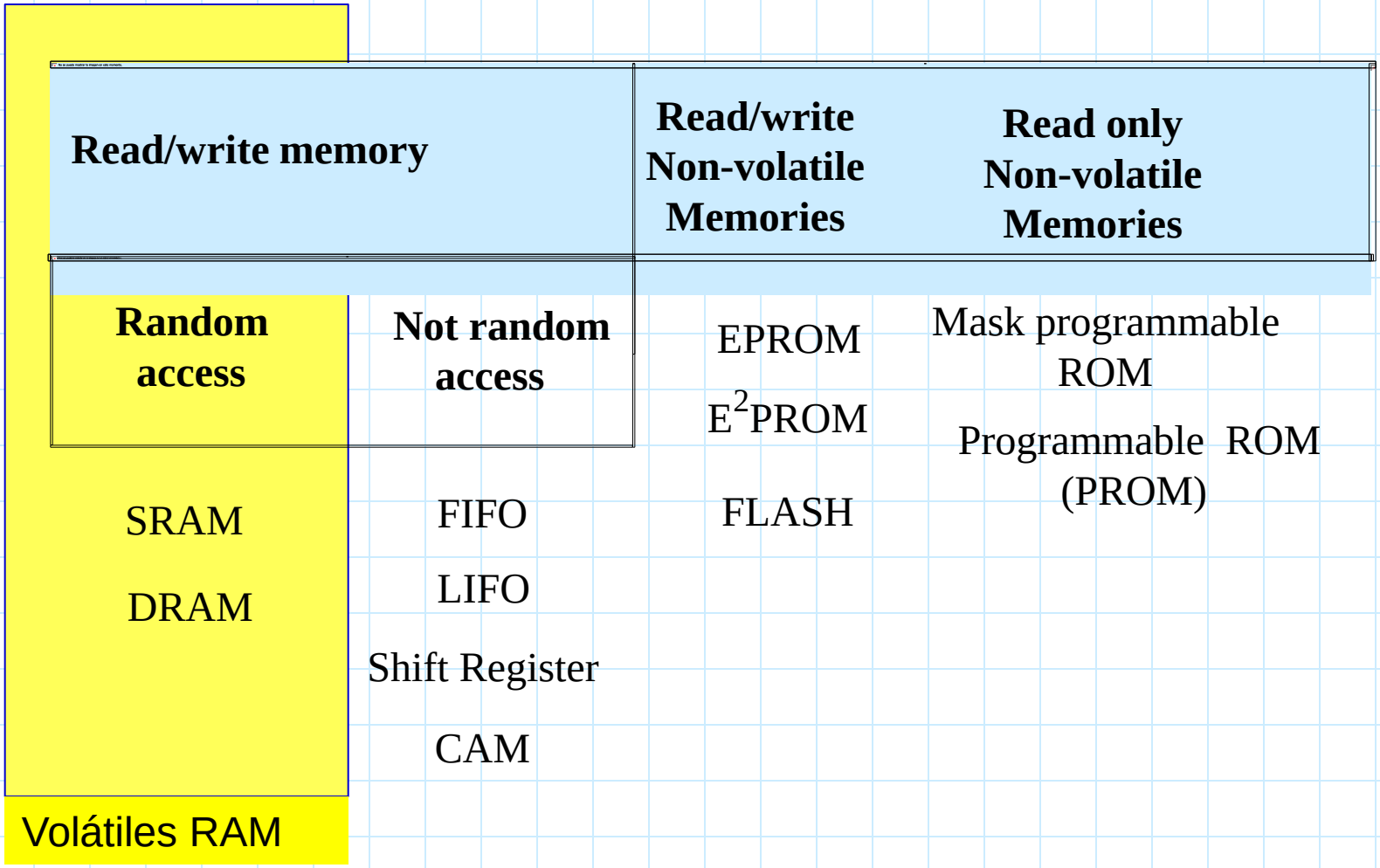


Erasing: tunnel effect

2.1.1. Internal structure of Flash memory chips



2. Types of semiconductor memories.



2.2. RAM features

RAM: *(Random Access Memory)*

- Volatile memories
- Read/write operations
- Random access

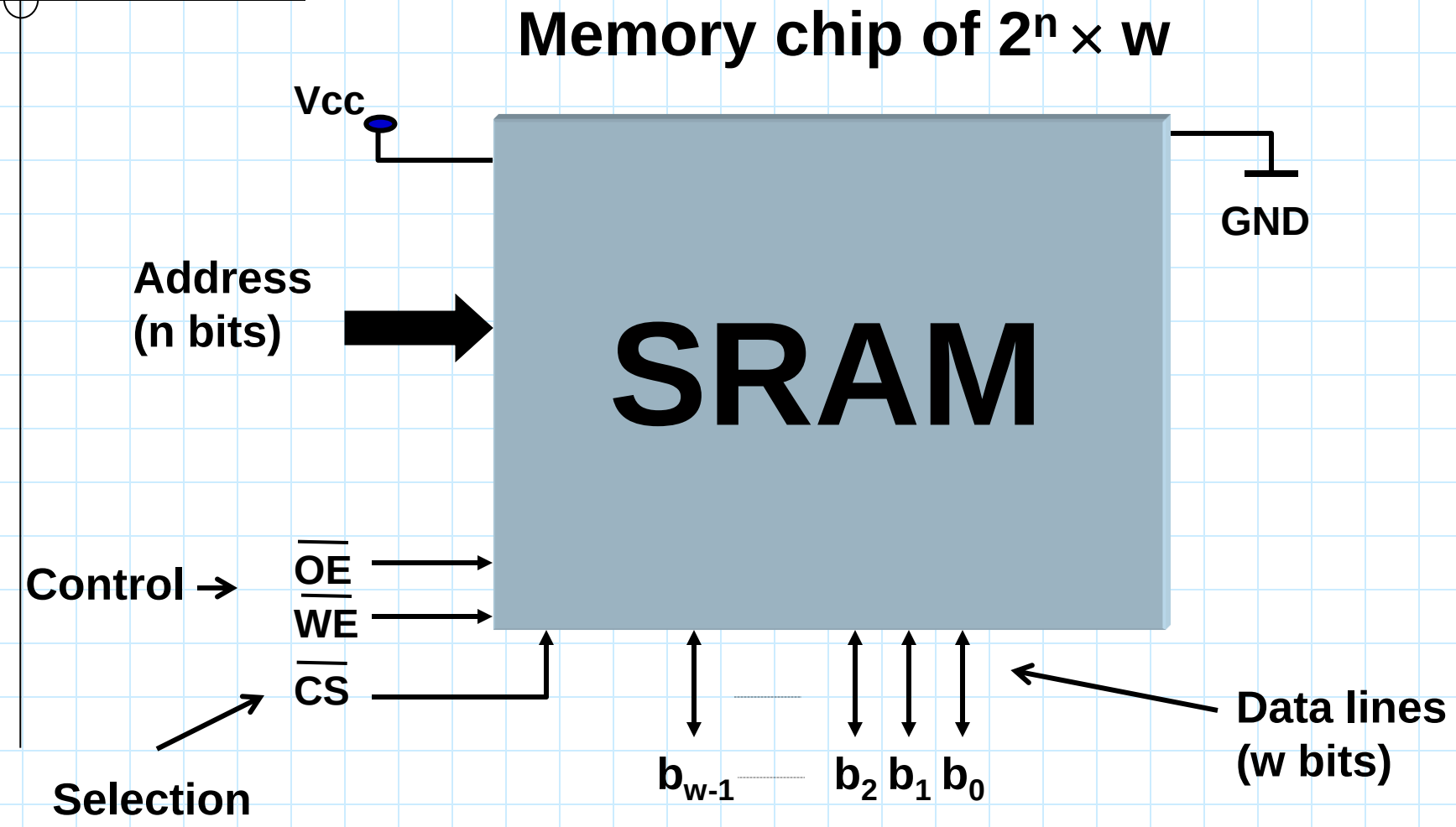
Depending on basic cells

- Static RAMs (**SRAM**)
- Dynamic RAMs (**DRAM**)

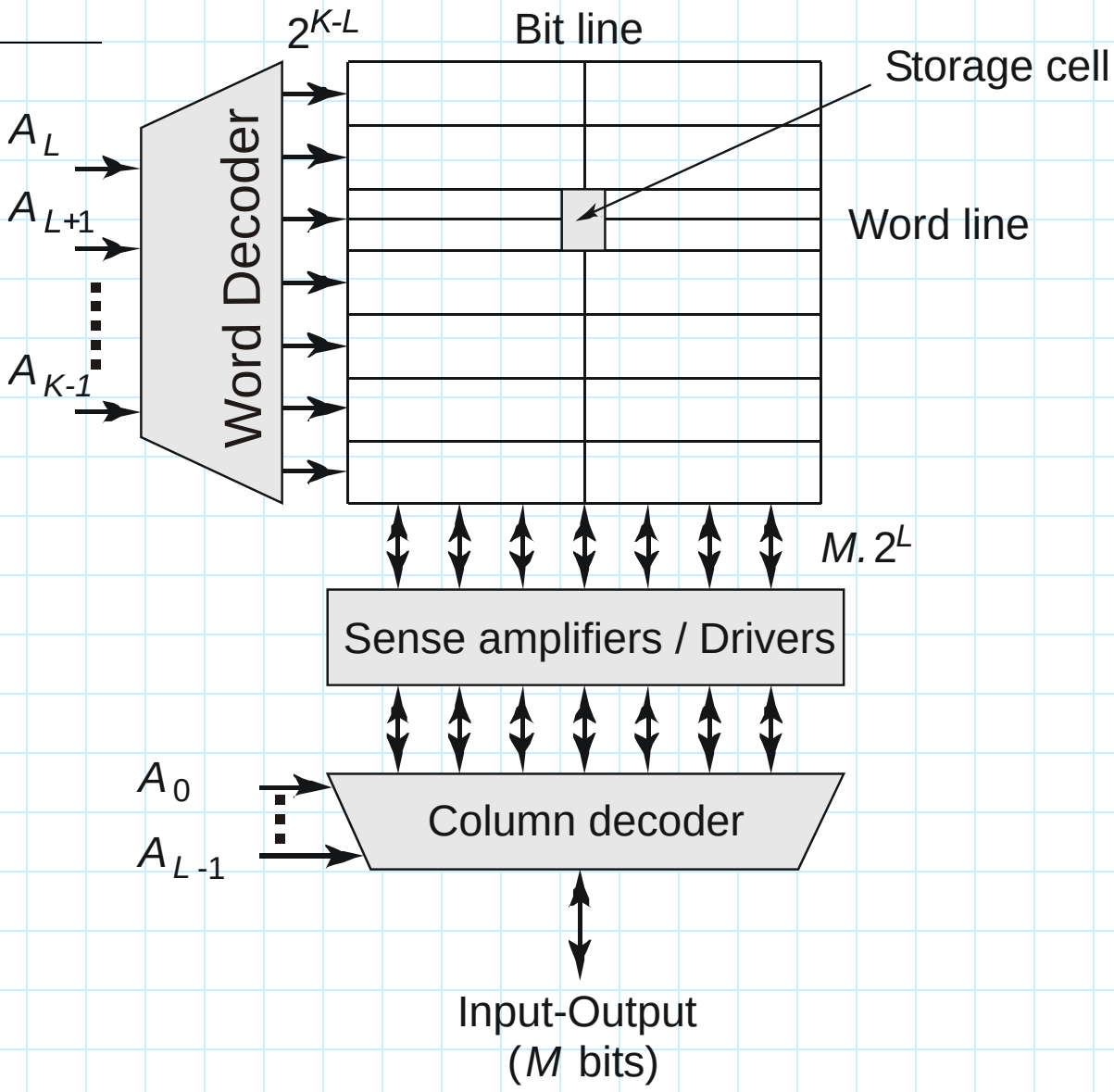
2.2. SRAM and DRAM classification

- Static (Static RAM = SRAM)
  - Flip-flop based
  - Data stored when power supply is ON
  - Large cell size (6 transistors / cell)
  - Fast (caches)
- Dynamic (Dynamic RAM = DRAM)
  - Based on the loading / unloading of a structural capacity
  - Require a periodic refresh
  - Small cell size (1 to 3 transistors / cell)
  - More bits / chip
  - Slower (memory)

2.2.1. Static RAM. External lines of a SRAM



2.2.1. Static RAM. Array structure

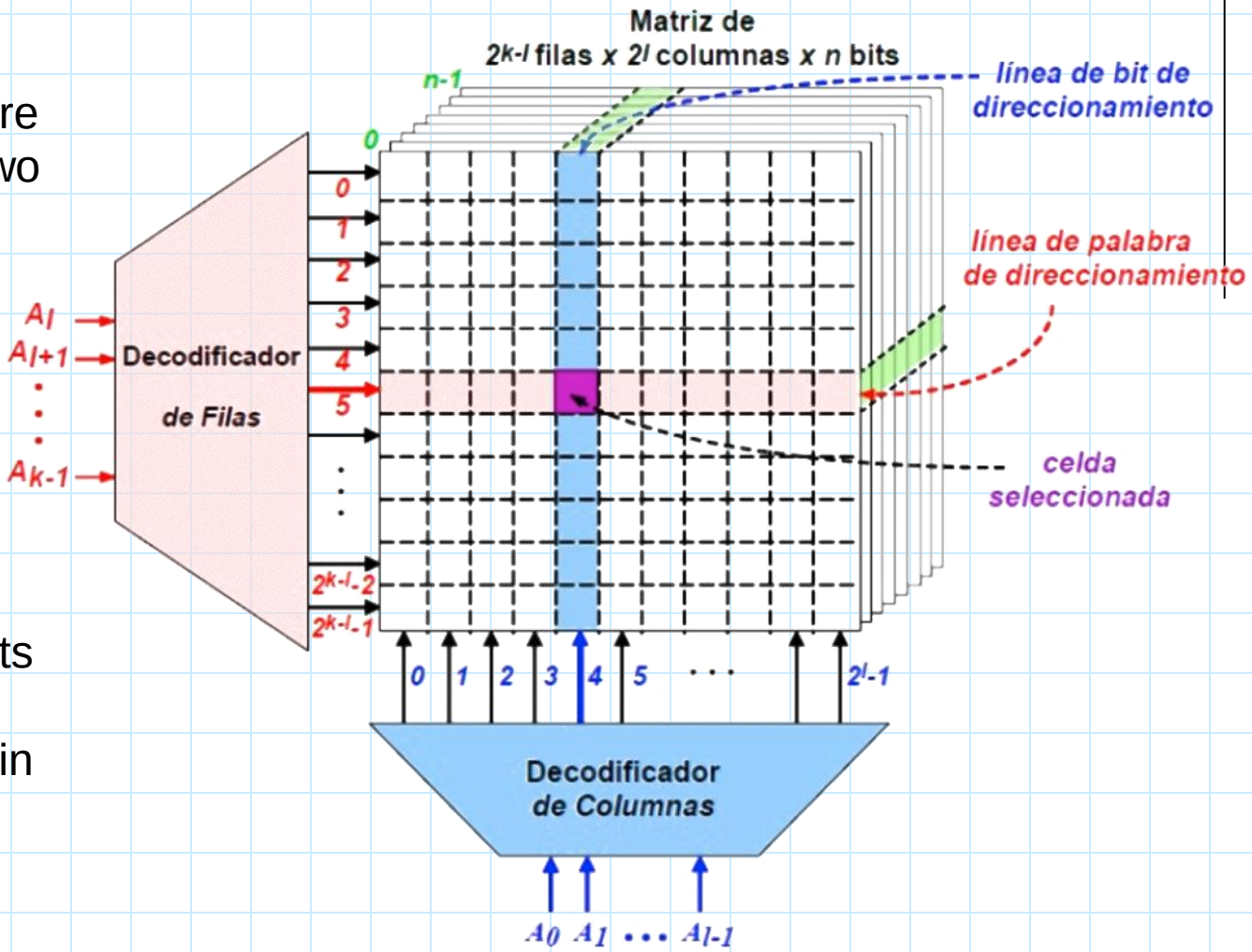


2.2.1. Static RAM. 2D ARRAY structure

- The address lines are divided approx. in two halves, so that the row and column decoders are of similar complexity (near square Matrix).

- Each address selects a complete word, which is distributed in n similar planes.

- The memory is an array of 2^{K-I} rows x 2^{I} colums x n bits (each bit in a different plane)



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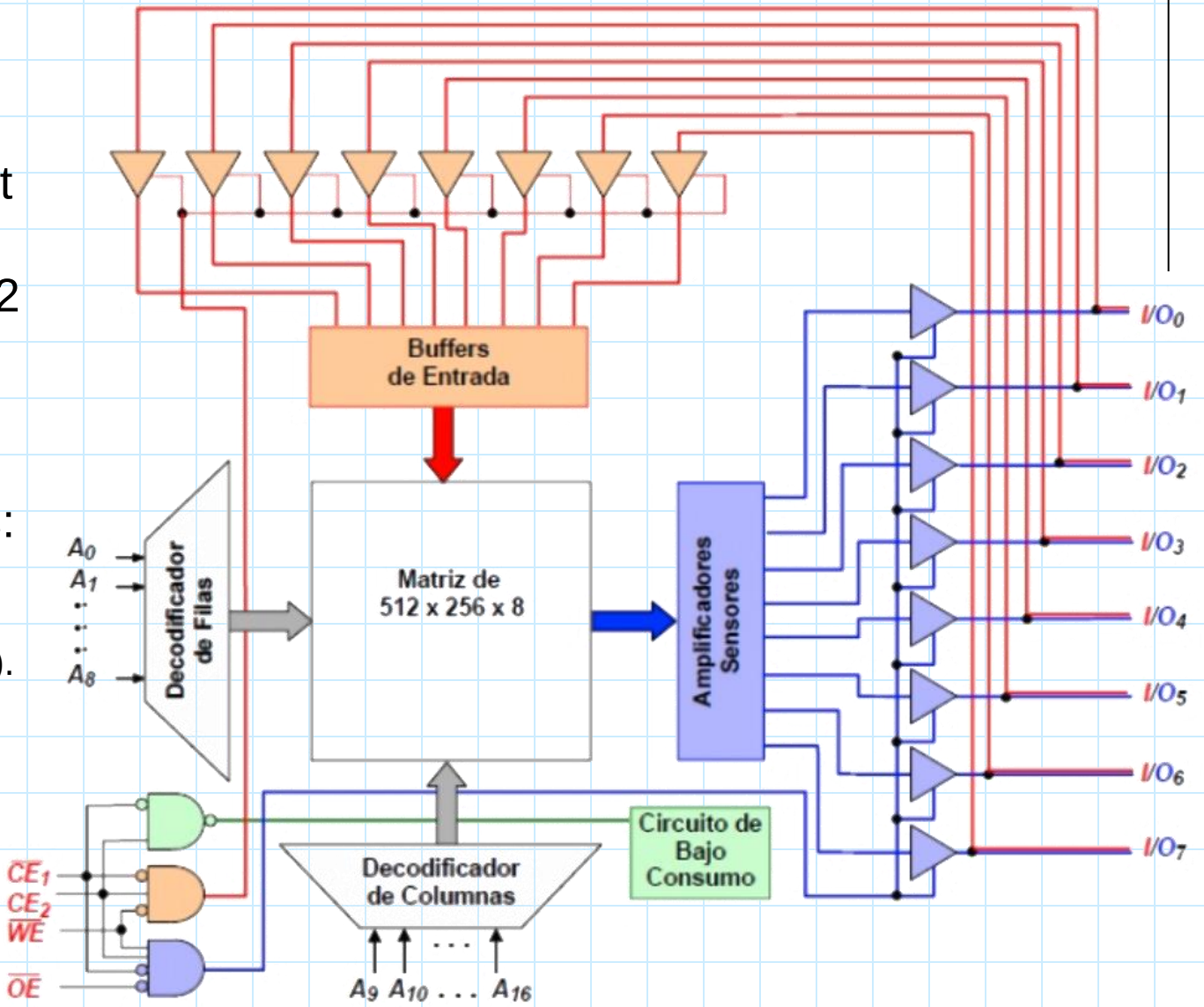
2.2.1. Static RAM. 2D ARRAY structure (II)

- Each input/output (data bus) have an amplifier and 2 tristate buffers.
- Control lines manage the input/output lines:
  - CS: Chip select
  - OE: Output enable (reading).
  - WE: Writing enable.



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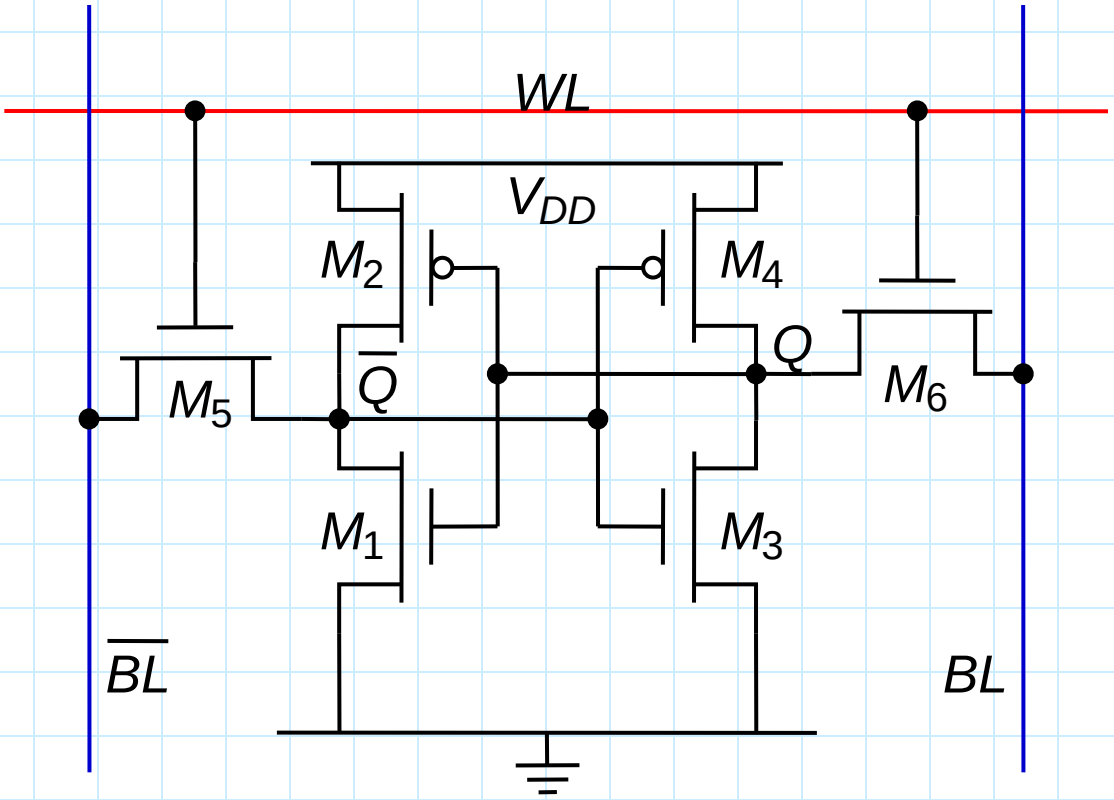
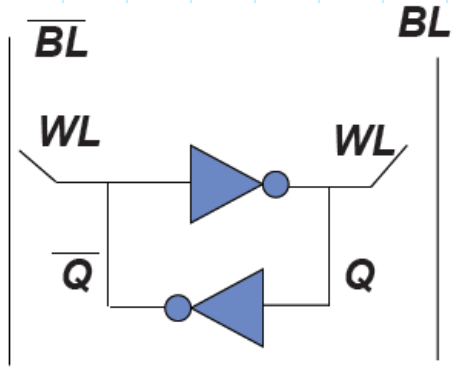
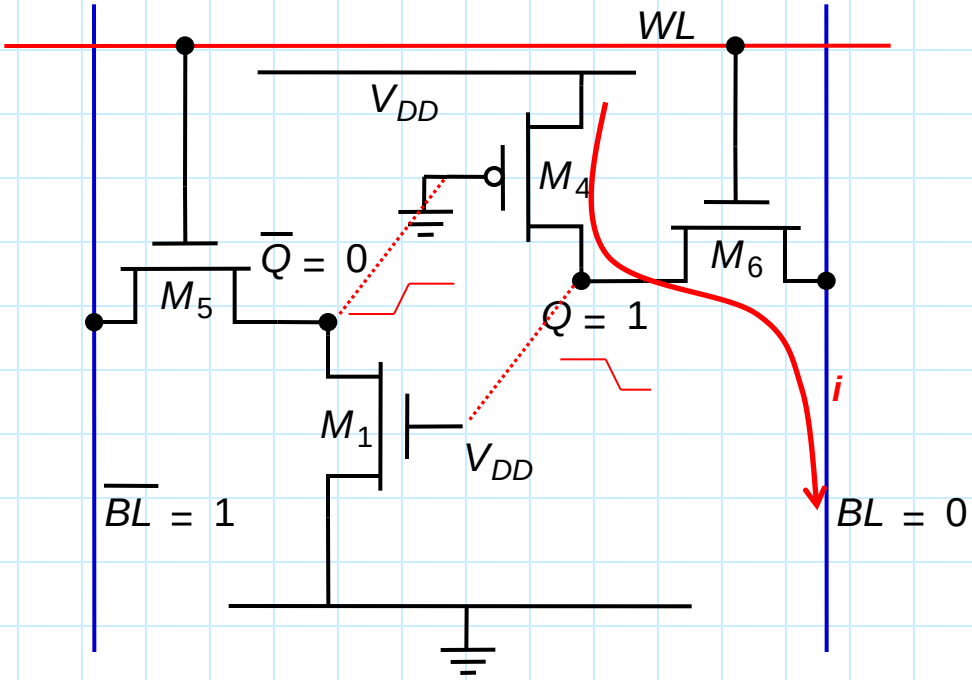
2.2.1. Static RAM. SRAM memory cell (6T)





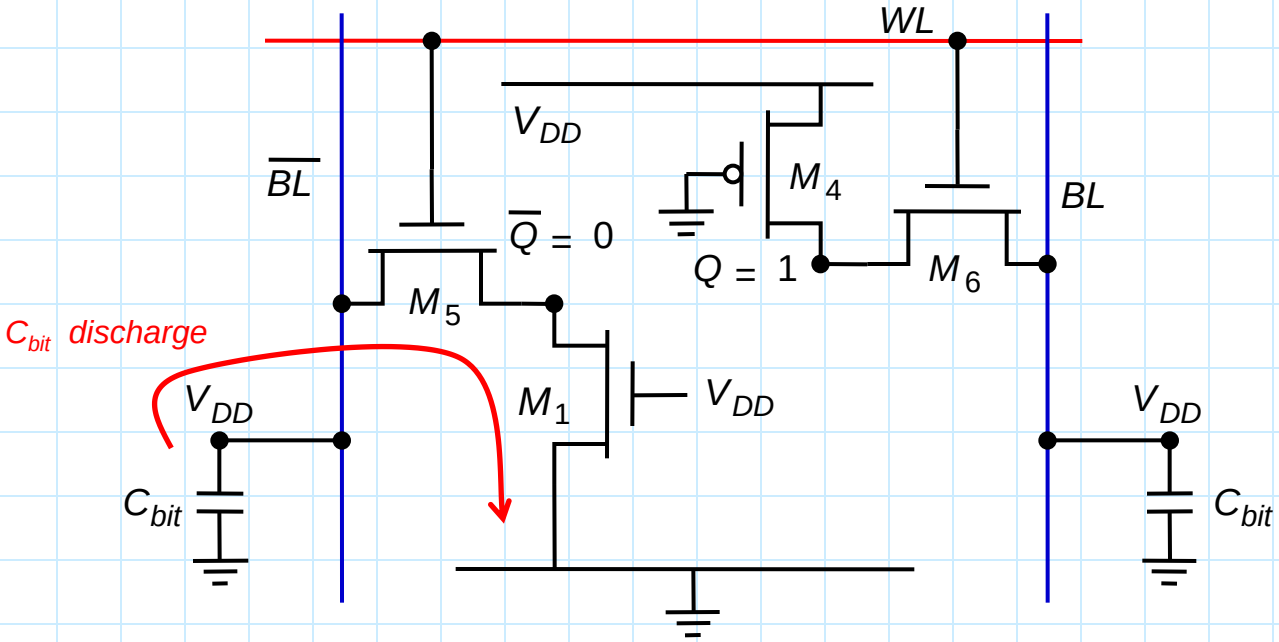
2.2.1. Static RAM. SRAM memory cell (6T). Writing operation



Assume Q = "1", /Q = "0“ and we want to write a "0"

1) The complementary data are set on BL and /BL
2) The cell is selected: WL = "1"
3) The flip-flop changes the state:
It is enough that Q is below VDD/2
The feedback makes /Q switch to "1" and Q to "0"

2.2.1. Static RAM. SRAM memory cell (6T). Reading operation



Assume Q = “1”, /Q = “0”

1) BL y /BL are pre-charged to VDD

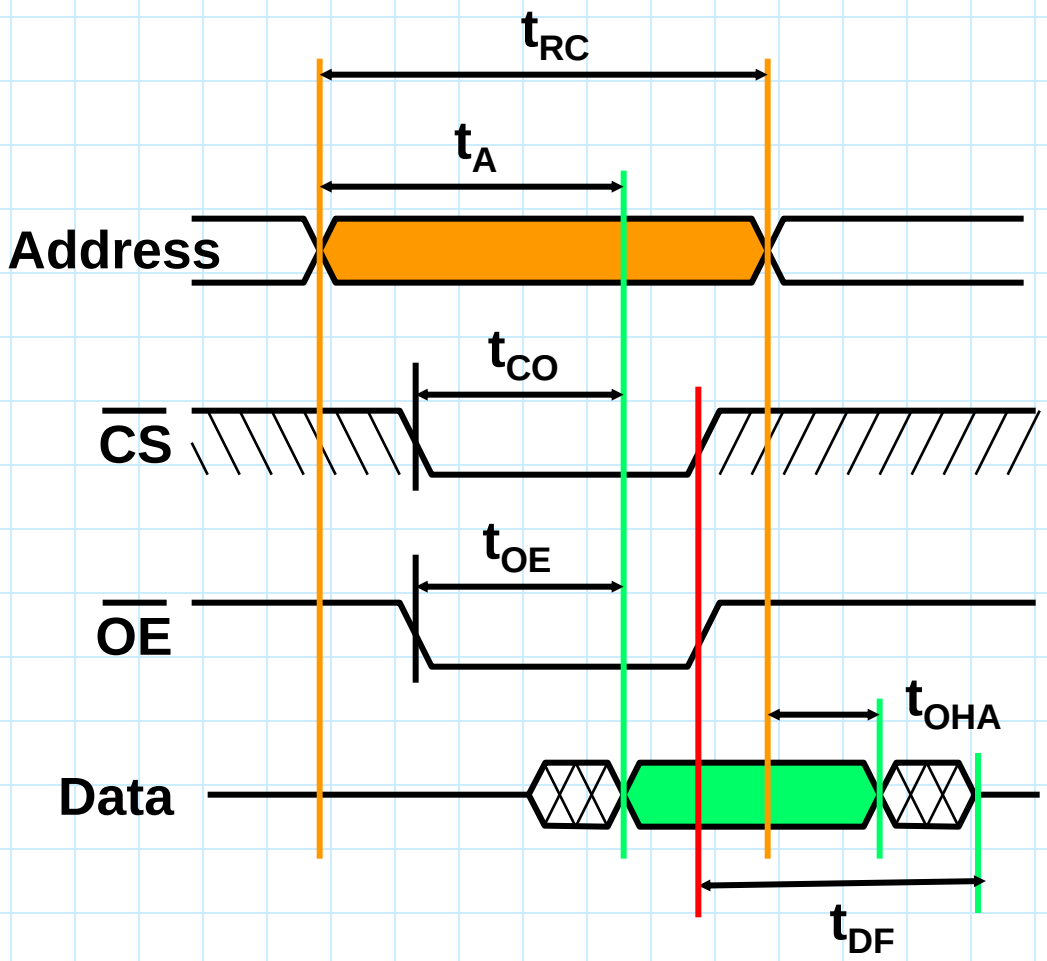
2) The cell is selected: WL = “1”

3) /BL is discharged through M5 and M1 and passes to “0”

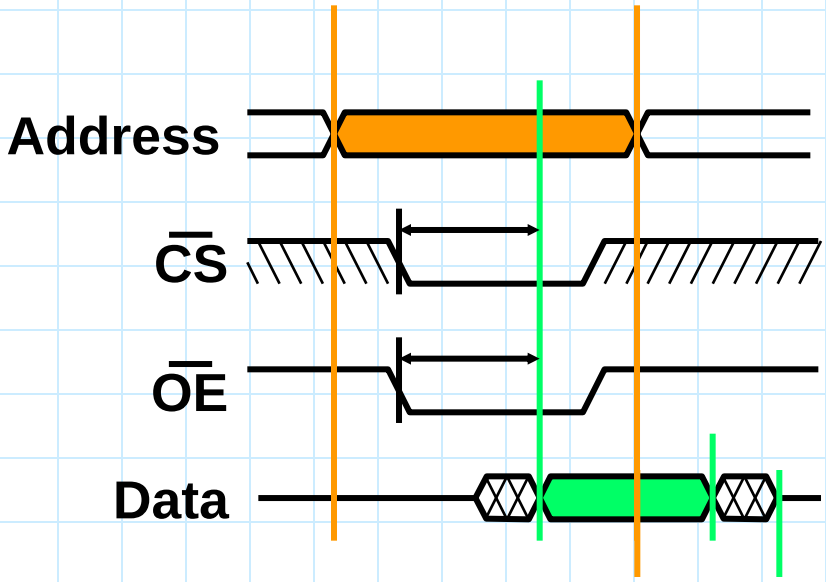
BL does not change, as BL and Q have a “1” and M3 is OFF

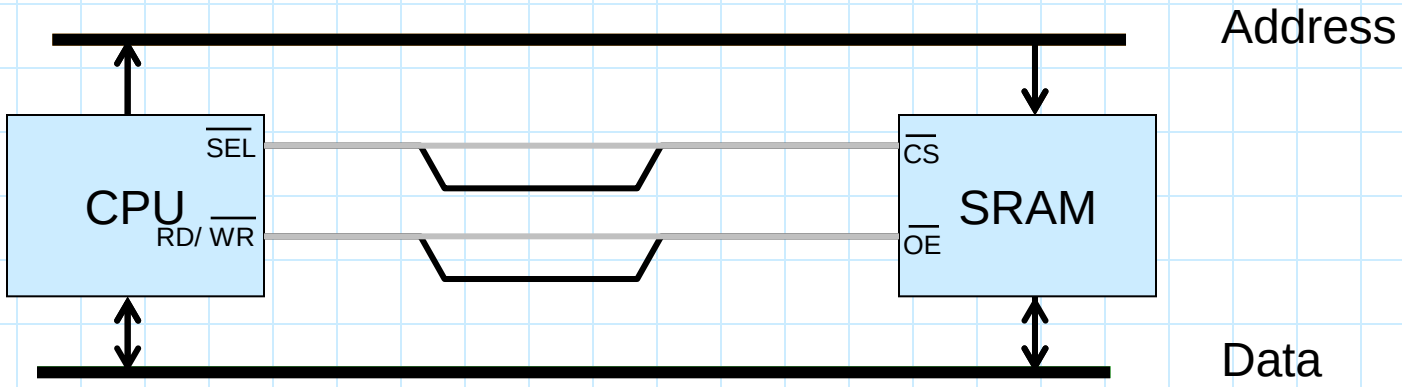
2.2.1. Static RAM. SRAM reading chronogram

t_{RC}	Read cycle time (mín.)
t_A	Access time from an address (max.)
t_{CO}	Access time from chip select (CS) (max.)
t_{OE}	Access time from output enable (OE) (max.)
t_{OHA}	Data hold time (min.)
t_{DF}	Time to high impedance (max.)



2.2.1. Static RAM. SRAM reading chronogram

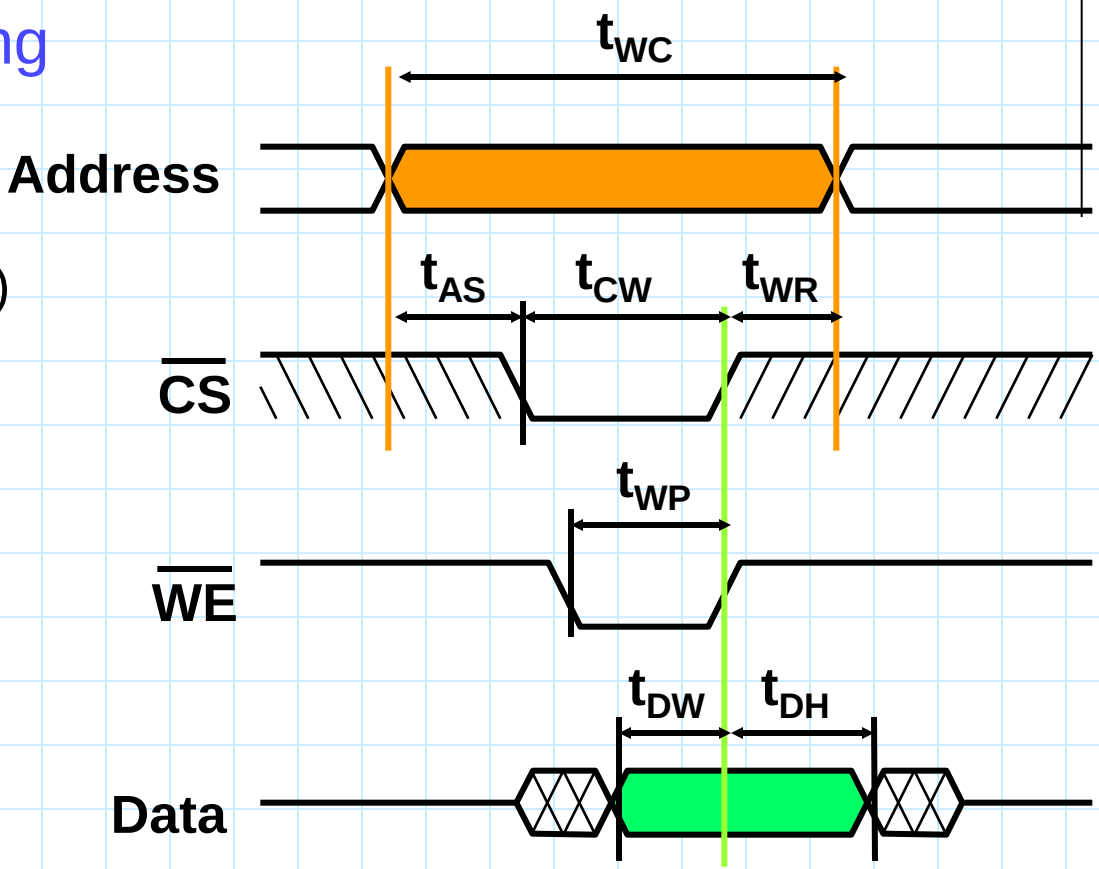




2.2.1. Static RAM. SRAM writing chronogram

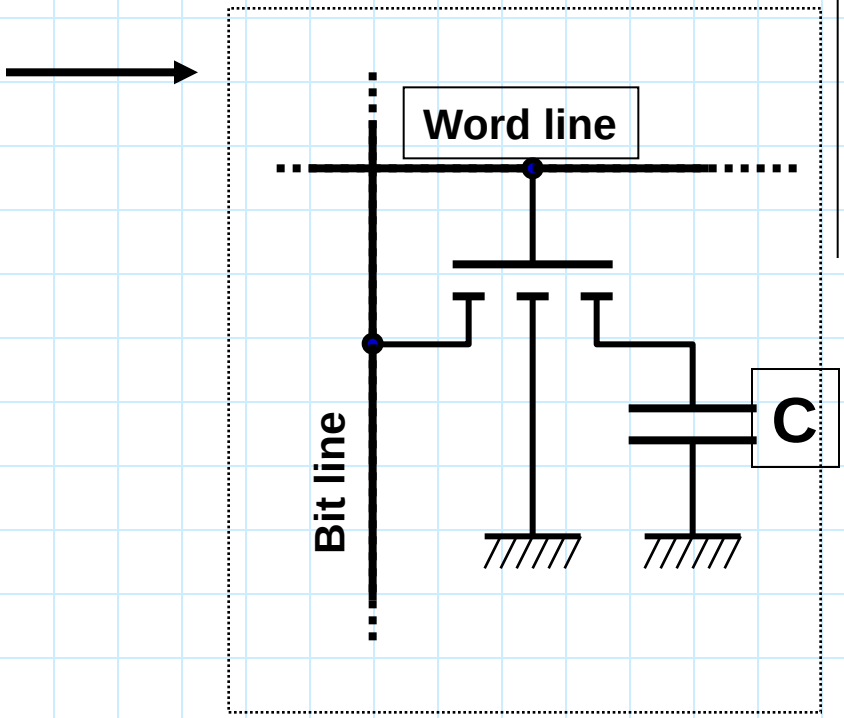
- WE controlled writing

t_{WC} Writing cycle time (mín.)
t_{WP} Writing pulse width (mín.)
t_{DW} Data set up time (mín.)
t_{DH} Data hold time (mín.)



2.2.2. DynamicRAM. Basic cell.

Basic cell: Capacitor



Tecnología:

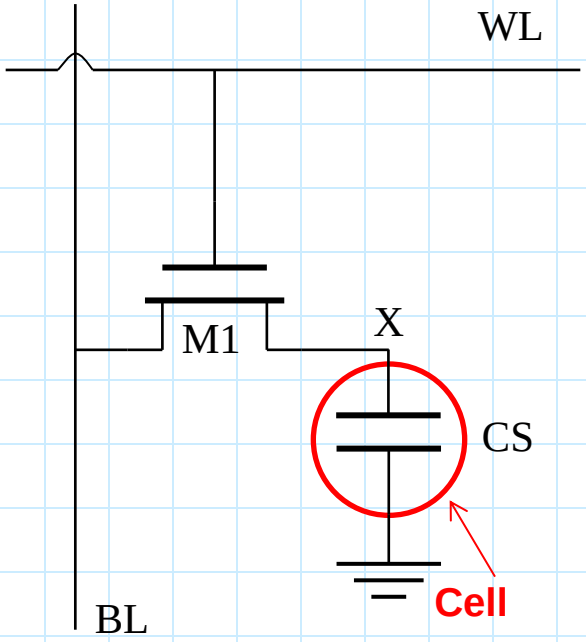
- Refreshing required (ms)
- Lower speed
- Very high integration density
- Cheap (cost/stored bit)
- Cycle time> Access time

Commercial chips capacity:

N= 1 … 128

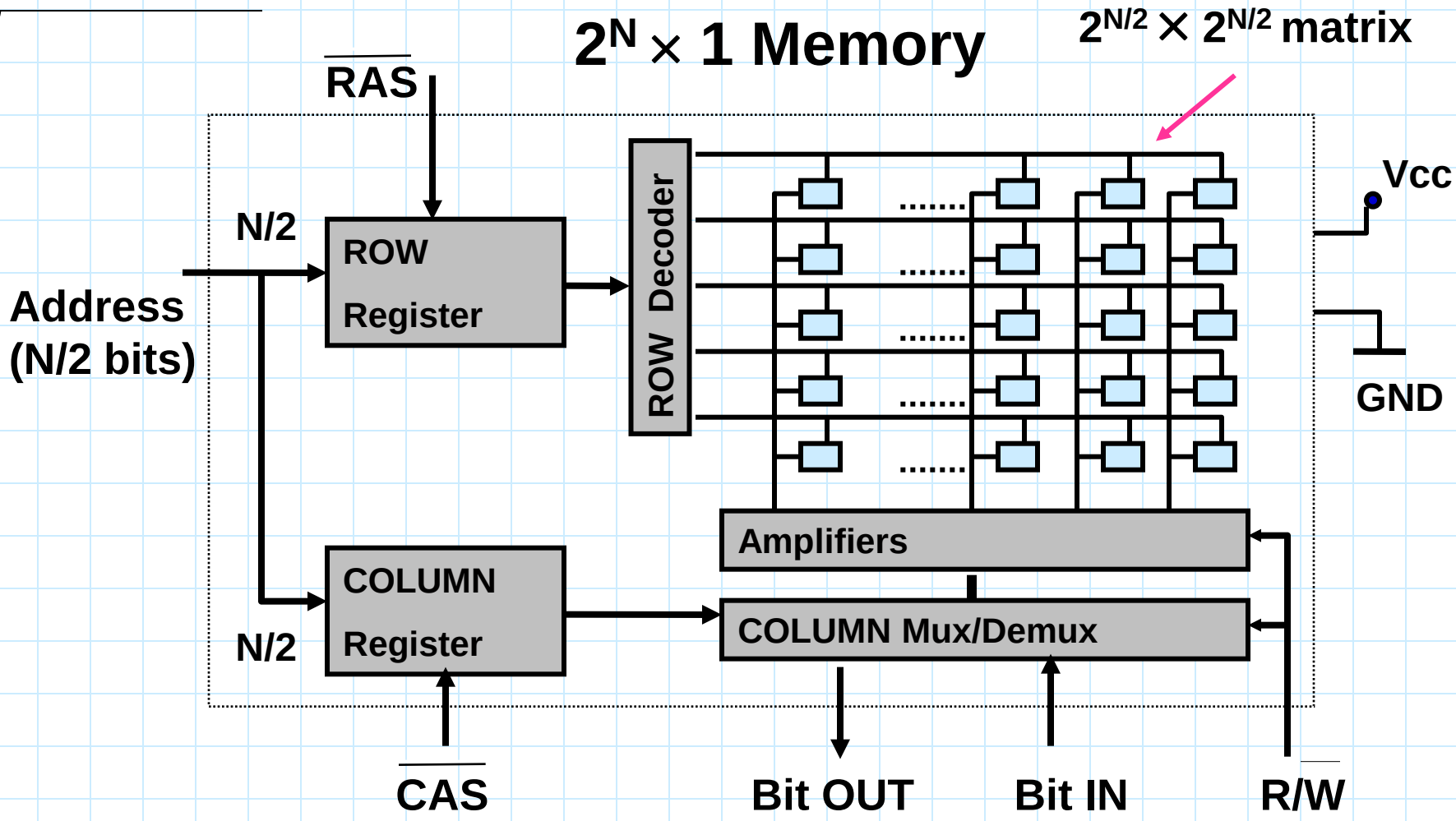
N M x 4 bit
N M x 8 bit
N M x 16 bit

2.2.2. DynamicRAM. Basic cell. DRAM-1T.



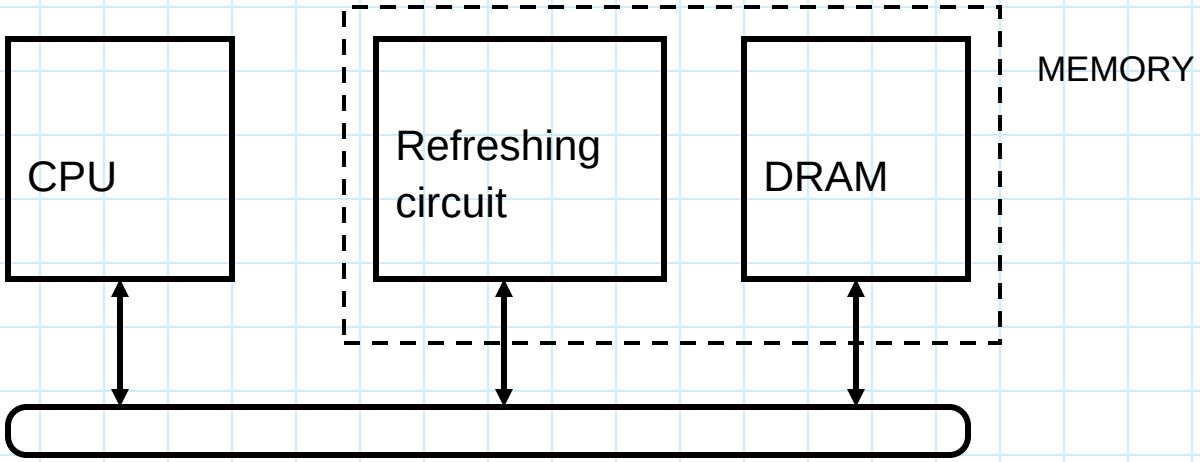
Datum stored as a charge of a CS capacitor
High integration density (1T)
Periodic refresh needed

2.2.2. Dynamic RAM. DRAM internal structure



2.2.2. Dynamic RAM. DRAM refreshing (I)

- Periodic writeback operation of the DRAM information
- It s performed by a refreshing circuit that can stand alone or be into the DRAM memory
- The refreshing can interfere with memory access cycles of the CPU



2.2.2. Dynamic RAM. DRAM refreshing (II)

In each DRAM access, either for reading or writing cycles, an entire row in the bit array is refreshed.

Refreshing period:

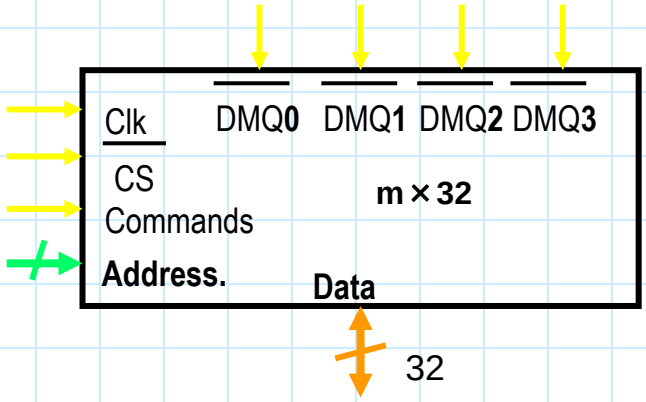
Maximum time that can be elapsed between two consecutive accesses to the same row of the DRAM

3. RAM memory modules- Introduction

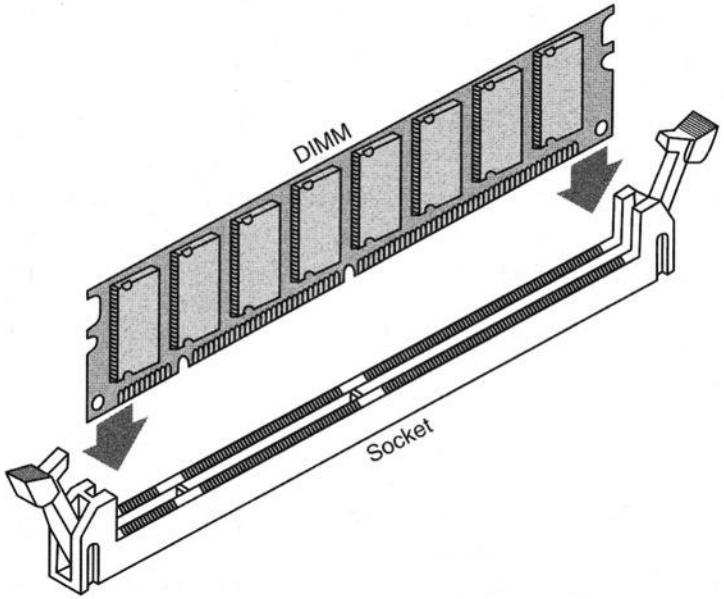
- The main memory system of a computer usually consists of a set of memory modules
- RAM modules are printed circuit boards having integrated DRAM chips soldered by one or both sides. The use of DRAM achieves high density memory
- Besides integrated circuits of DRAM, modules have an integrated circuit (SPD) enabling identification thereof to the PC through the serial communication protocol
- Over time various technologies of these modules have appeared:
  - SDR SDRAM (Single Data Rate Synchronous Dynamic Random Access Memory)
  - DDR SDRAM (Dual Data Rate SDRAM).
  - DDR2 SDRAM (DDR dual bandwidht)
  - DDR3 SDRAM (DDR quad bandwidht)
  - RDRAM (Rambus DRAM) (propietary technology and higher bandwidht)

3.2. Standard DRAM memory modules

- Terminals
  - The address lines are multiplexed
  - A CS * input line acts as module selection
  - DMQ inputs * (CAS) are byte-enable lines (for writing)

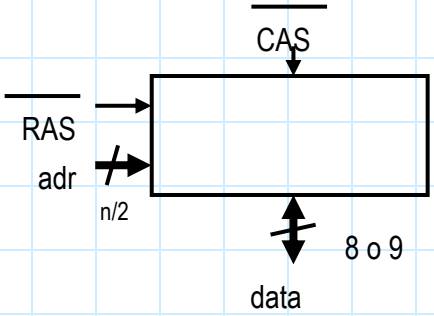


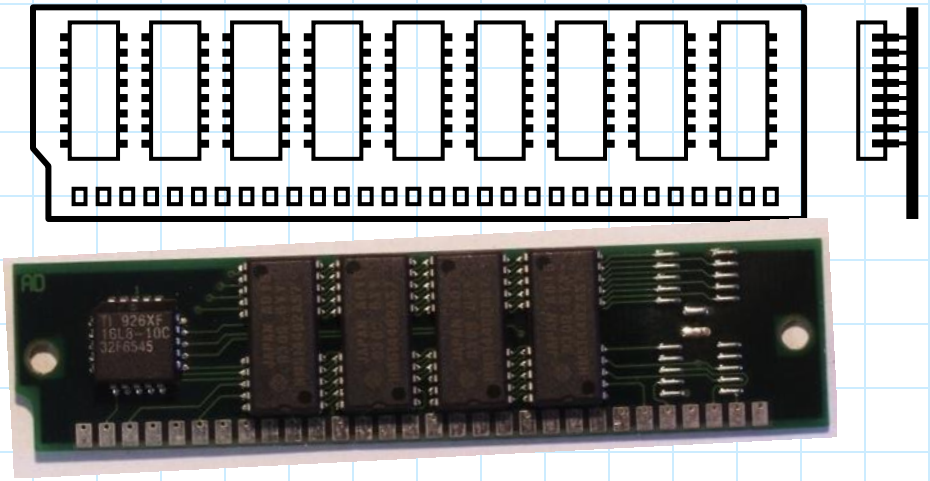
- Modules are inserted and removed easily from the main board *slots.*
  - Optional: Parity bits (for each 8-bits block, a redundant bit is added). Also Error Correcting Codes (ECC) (1 bit correction).



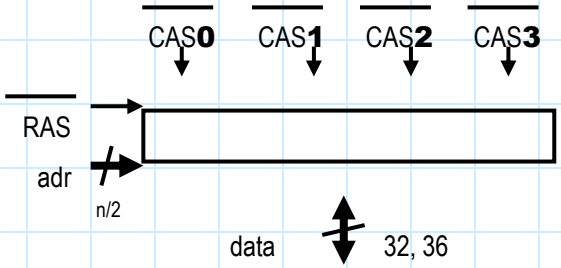
3.2.1. RAM memory modules: SIMM modules.

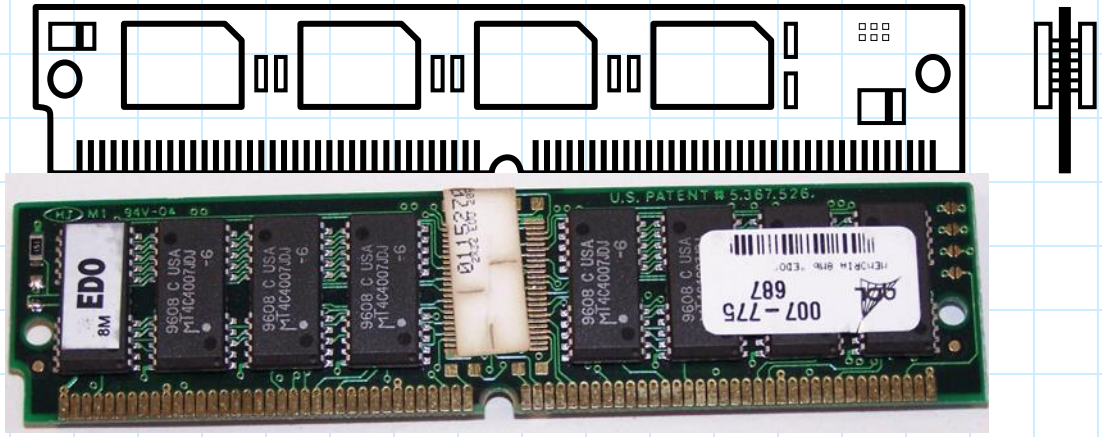
Example: SIMM (*Single Inline Memory Module*) of 30 contacts





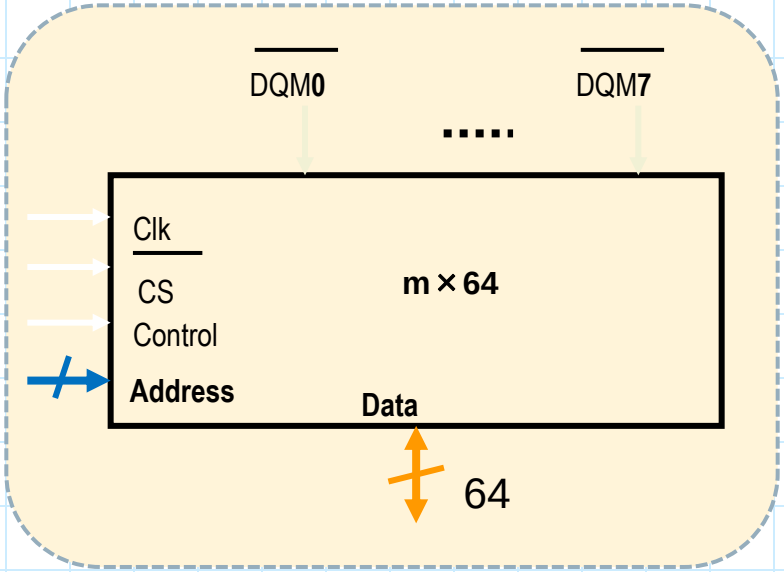
Example: SIMM of 72 contacts

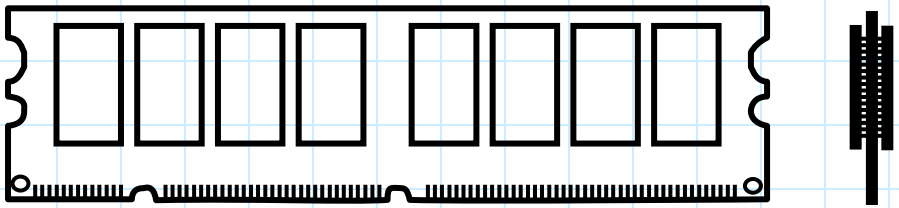




DIMM modules(*Dual Inline Memory Module*)

- 168/184/240 contacts, 64 data bits, 13 cm of lenght





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3.2.1. RAM memory modules: SO-DIMMmodules

- Módulos SO-DIMM (Small Outline Dual In Line Memory Module). For laptops. Miniaturized DIMM format.

- 144 contacts connector, used with SDRAM;
- 200 contacts, used with SDRAM DDR, DDR2 y DDR3, with different position of central mark (notch);

3.2.2. Double Data Rate Synchronous DRAM: 3.2.2.1. DDR standard modules

Name	Clock freq.	Delay	CLK fr. I/O	Transfer speed.	Name	Max. Trans. Rate
DDR-200	100 MHz	10 ns	100 MHz	200 million	PC1600	1.600 MB/s
DDR-266	133 MHz	7,5 ns	133 MHz	266 million	PC2100	2.133 MB/s
DDR-300	150 MHz	-ns	150 MHz	300 million	PC2400	2.400 MB/s
DDR-333	166 MHz	6 ns	166 MHz	333 million	PC2700	2.667 MB/s
DDR-366	183 MHz	5,5 ns	183 MHz	366 million	PC3000	2.933 MiB/s
DDR-400	200 MHz	5 ns	200 MHz	400 million	PC3200	3.200 MB/s
DDR-433	216 MHz	4,6 ns	216 MHz	433 million	PC3500	3.500 MB/s
DDR-466	233 MHz	4,2 ns	233 MHz	466 million	PC3700	3.700 MB/s
DDR-500	250 MHz	4 ns	250 MHz	500 million	PC4000	4.000 MB/s
DDR-533	266 MHz	3,7 ns	266 MHz	533 million	PC4300	4.264 MB/s

3.2.2. Double Data Rate Synchronous DRAM:
3.2.2.2. DDR2 standard modules.

Name	Clock freq.	Delay	CLK fr. I/O	Transfer speed.	Name	Max. Trans. Rate
DDR2-400	100 MHz	10 ns	200 MHz	400 million	PC2-3200	3.200 MB/s
DDR2-533	133 MHz	7,5 ns	266 MHz	533 million	PC2-4300	4.264 MB/s
DDR2-600	150 MHz	6,7 ns	300 MHz	600 million	PC2-4800	4.800 MB/s
DDR2-667	166 MHz	6 ns	333 MHz	667 million	PC2-5300	5.336 MB/s
DDR2-800	200 MHz	5 ns	400 MHz	800 million	PC2-6400	6.400 MB/s
DDR2-1000	250 MHz	3,75 ns	500 MHz	1.000 million	PC2-8000	8.000 MB/s
DDR2-1066	266 MHz	3,75 ns	533 MHz	1.066 million	PC2-8500	8.530 MB/s
DDR2-1150	286 MHz	3,5 ns	575 MHz	1.150 million	PC2-9200	9.200 MB/s
DDR2-1200	300 MHz	3,3 ns	600 MHz	1.200 million	PC2-9600	9.600 MB/s

3.2.2. Double Data Rate Synchronous DRAM: 3.2.2.3. DDR3 standard modules

Name	Clock freq.	Delay	CLK fr. I/O	Transfer speed.	Name	Max. Trans. Rate
DDR3-1.066	133 MHz	7,5 ns	533 MHz	1.066 million	PC3-8500	8.530 MB/s
DDR3-1.200	150 MHz	6,7 ns	600 MHz	1.200 million	PC3-9600	9.600 MB/s
DDR3-1.333	166 MHz	6 ns	667 MHz	1.333 million	PC3-10667	10.664 MB/s
DDR3-1.375	170 MHz	5,9 ns	688 MHz	1.375 million	PC3-11000	11.000 MB/s
DDR3-1.466	183 MHz	5,5 ns	733 MHz	1.466 million	PC3-11700	11.700 MB/s
DDR3-1.600	200 MHz	5 ns	800 MHz	1.600 million	PC3-12800	12.800 MB/s
DDR3-1.866	233 MHz	4,3 ns	933 MHz	1.866 million	PC3-14900	14.930 MB/s
DDR3-2.000	250 MHz	4 ns	1000 MHz	2.000 million	PC3-16000	16.000 MB/s

3.2.2. Double Data Rate Synchronous DRAM:
3.2.2.3. DDR4 standard modules

Name	Clock freq.	Delay	CLK fr. I/O	Transfer speed.	Name	Max. Trans. Rate
DDR4-1.600	200 MHz	5 ns	1600 MHz	3.200 million	PC3-12800	12.800 MB/s
DDR4-1.866	233 MHz	4,3 ns	1864 MHz	3.728 million	PC3-14900	14.930 MB/s
DDR4-2.133	266 MHz	3,76 ns	2128 MHz	4.256 million	PC4-17000	16.000 MB/s
DDR4-2400	300 MHz	3,34 ns	2400 MHz	4.800 million	PC3-12800	12.800 MB/s
DDR4-2666	333 MHz	3 ns	2664 MHz	5.328 million	PC3-14900	14.930 MB/s
DDR4-3200	400 MHz	2,5 ns	3200 MHz	6.400 million	PC3-16000	16.000 MB/s

3.2.2. Comparison of the shape of modules: DDR, DDR2 y DDR3

- The DDR3 DIMMs have 240 contacts or pins, the same number as DDR2, but the DIMMs are physically incompatible, due to a different location of the notch.
- The DDR4 have 288 pins, also incompatible with previous families of DDR.