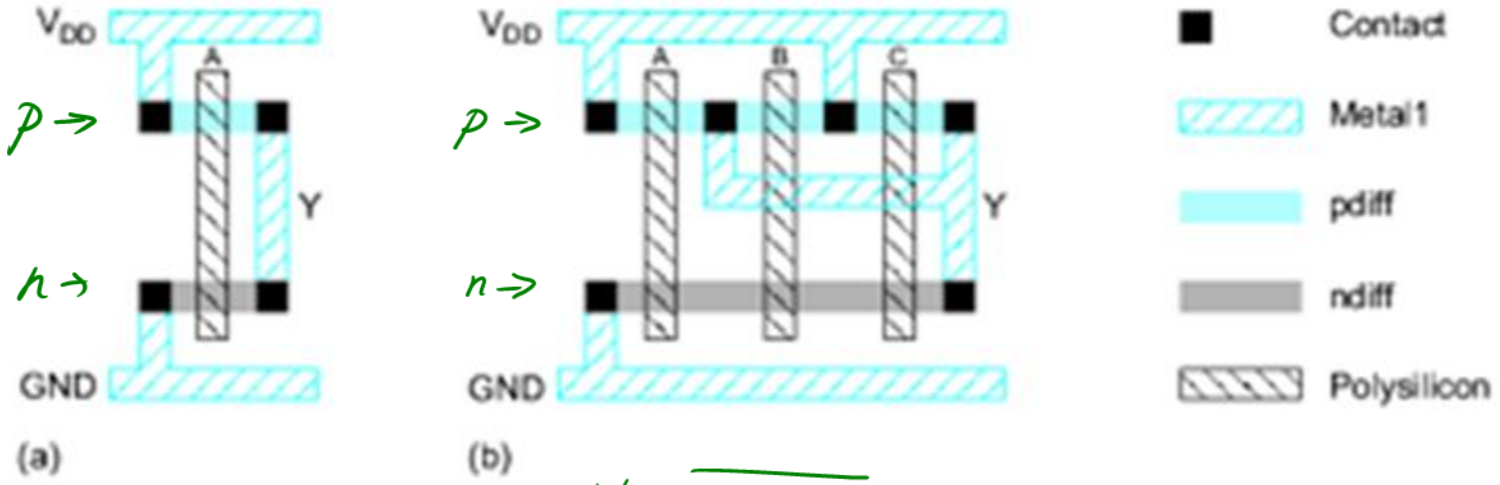
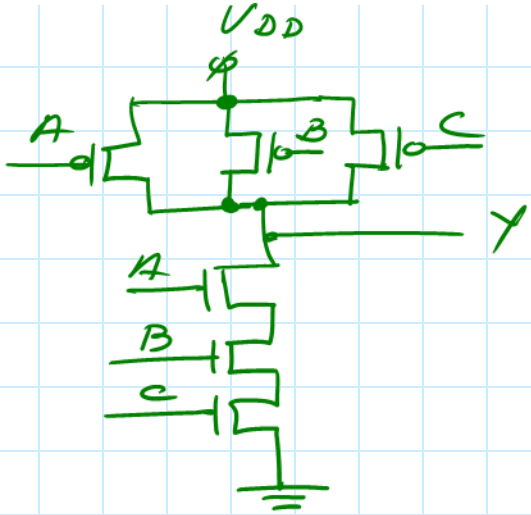
5.1. Indicate the logic function that implements the standard cell with the layouts of the figure:

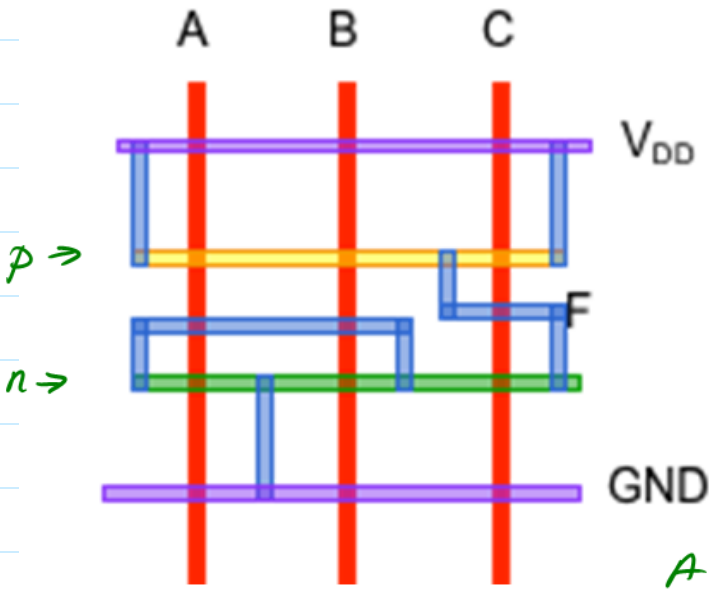


$Y = \overline{A}$

$Y = \overline{A \cdot B \cdot C}$

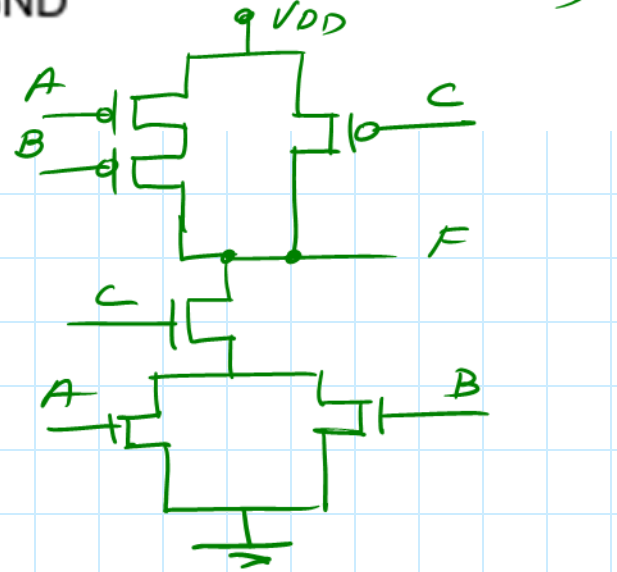


5.2. From layout diagram of the figure, indicate the logic function that implements the standard cell.



Violet → metal 2 (VDD y GND)
Blue→ metal 1 (internal connections)
Green → N-diffusion
Yellow → P-diffusion
Red → polisilicon (transistor gates)

$F = \overline{C \cdot (A+B)}$



UNIT 4. CMOS

5.3. Indicate whether they are true (V) or false (F) the following statements on the photolithographic manufacturing process of CMOS IC:

a) Usually, a circular silicon wafers are used as substrate ✓

b) Each wafer contains a single chip F

c) They are deposited layers (layers) of different materials in a bottom-up way ✓

d) The typical order in the deposition of layers is: 1) n + and p + areas of S and D, 2) metal interconnections, 3) thin insulating layer of gate, 4) polysilicon of the gate F → metal at the end

e) UV light is used to project the masks on the wafer ✓

f) Once you have the chips on the wafer substrate, they are cut, tested and encapsulated ✓

5.4. If we compare the standard cell based design with full-custom design, we can say that:

A) The semi-custom design based on cells optimizes the speed and silicon occupied area. ✗

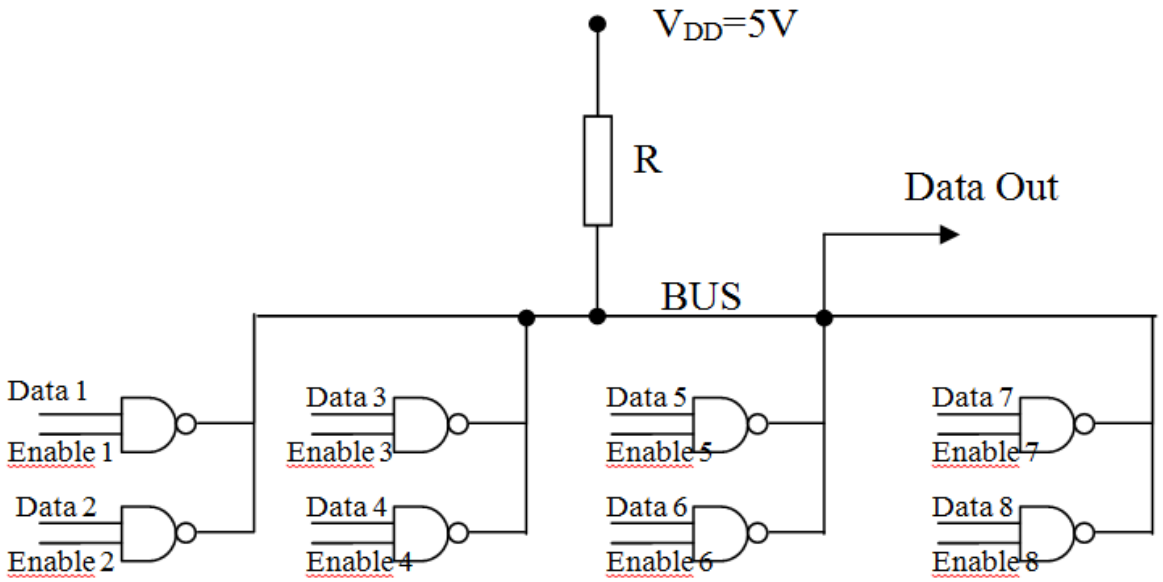
B) The full-custom design is getting more automated, minimizing the design time ✗

C) The full-custom design is done with layout editors, making the geometric description of the masks ✓

D) In the cell design, the smallest units of design are the transistors, which are stored in libraries ✗

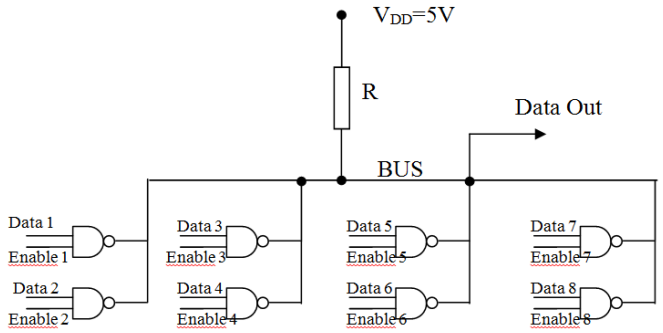
3.4. The figure shows 8 open-drain outputs connected to a bus. Only one gate is enabled at a time, remaining the other with a high level at the output. Indicate the maximum and minimum pull-up resistor R, according to the following specifications of the logic gates:

(74HC gates specifications):
I_{OLmax} = 4mA,
V_{OLmax} = 0.33V
V_{OHmin} = 3.84V
I_{OHmax} = 5µA (leakage current at the output when High)



A) 0.5K ≤ R ≤ 4K7
B) 0.5K ≤ R ≤ 10K
C) 1.5K ≤ R ≤ 3K3
D) 1.17K ≤ R ≤ 29K

UNIT 4. CMOS



$$\frac{V_{DD} - V_{OL\,max}}{I_{OL\,max} - n\,I_{IL\,max}} \leq R \leq \frac{V_{DD} - V_{OH\,min}}{m\,I_{OH\,max} - n\,I_{IH\,max}}$$

$m = 8;\ n = 0$

$$\frac{5 - 0.33}{4} \quad R \leq \frac{5 - 3.84}{8 \cdot 0.005}$$

$$1.168K \leq R \leq 29K$$