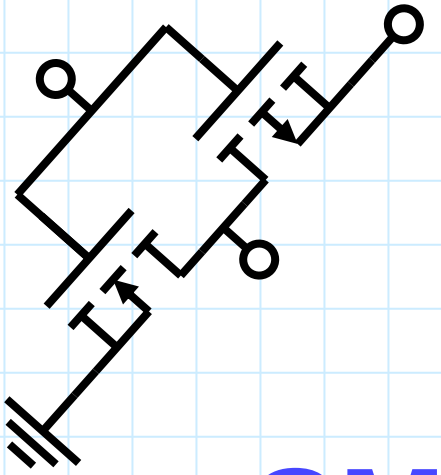


Unit 4:
CMOS technology foundations

Objectives

At the end of this Unit, the student should:

- Know and understand the design of CMOS integrated circuits
  - Complementary CMOS logic
  - Logic design based on transmission gates
- Know a wide range of CMOS logic circuits
  - Combinational, sequential, RAM memory cells
- Know how to characterize electrically the CMOS integrated circuits
  - Parameters of voltage, current, delay and power consumption
  - Special outputs: open drain, tri-state.
- Know the main CMOS subfamilies
  - Buffered outputs, high speed, low voltage, etc.
- Understand the foundations of design and manufacture of VLSI chips

Contents

Bibliography

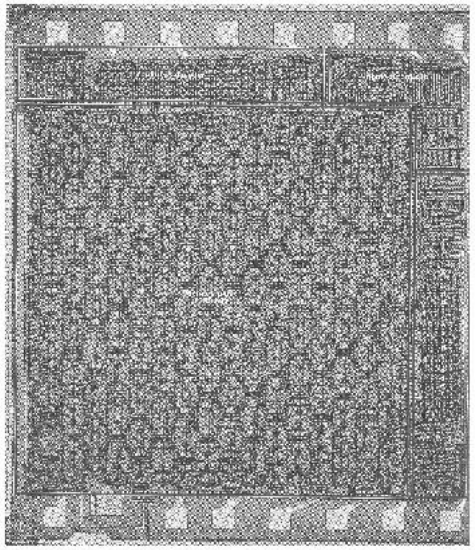
- Theory
  - “Digital design”. Wakerly. Ed. Prentice-Hall. 2006. Chapter 3.
  - “Electronics”. Hambley. Ed. Prentice-Hall. 2002. Chapter 6.
  - “CMOS circuits”. R.M. Marston. Ed. Paraninfo. 1995.
  - “Digital integrated circuits”. Jan Rabaey et al. Ed. Prentice-Hall. 2004.
  - www.intel.com/technology
  - “International Technology Roadmap for Semiconductors – ITRS09”
- Problems
  - G.Benet; J.V.Benlloch; J.V.Busquets; D.Gil; P.Perez, *Ejercicios Resueltos de Tecnologia de Computadores, Cap.5,* SPUPV 2006.916

4.1. Introduction

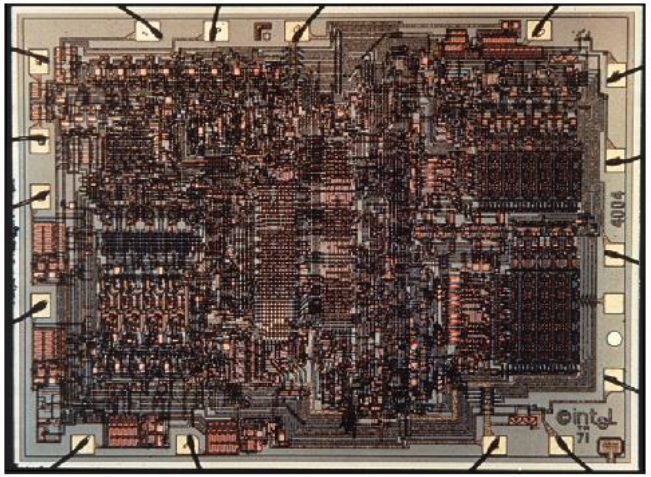
- CMOS is the logic family with more looking forward to future.
- Application scope :
  - Most LSI and VLSI I.C.: Memories and Processors
  - SSI and MSI, together with TTL
- Relevant features
  - Low power consumption
  - Simple manufacturing process
  - Excellent noise immunity
  - Variable supply voltage
  - High Speed subfamilies.

4.1. Introduction. Historical evolution

- In 1970's the manufacturing processes for processors and memories was typically based on NMOS transistors
  - Cheap, but have static consumption



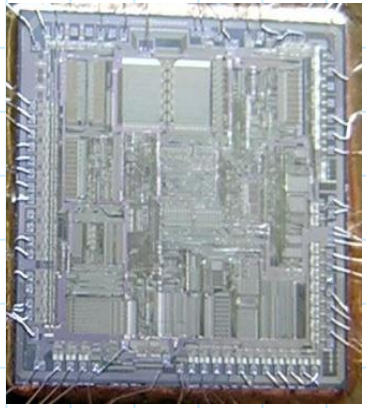
Intel 1101 256-bit SRAM



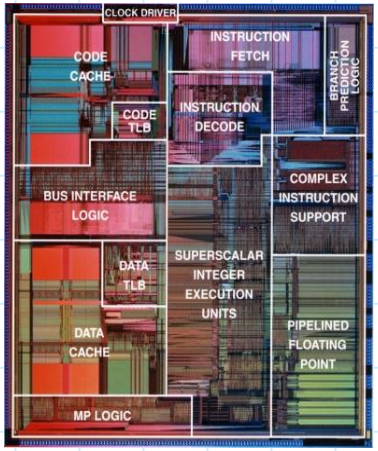
Intel 4004 4-bit μProc

4.1. Introduction. Historical evolution

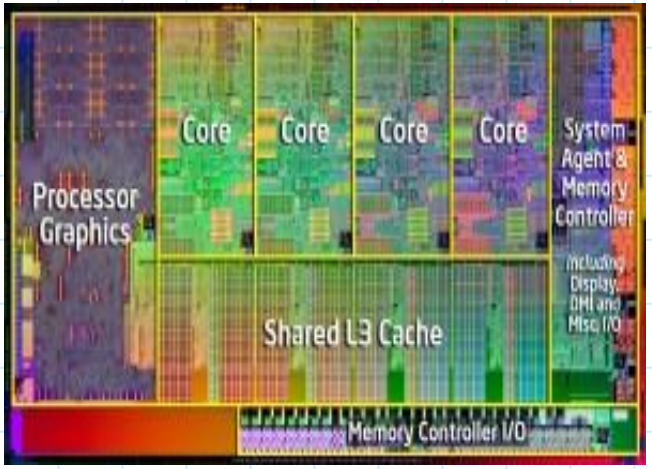
- From 1980's to present: CMOS technology: Low static power



Intel 286



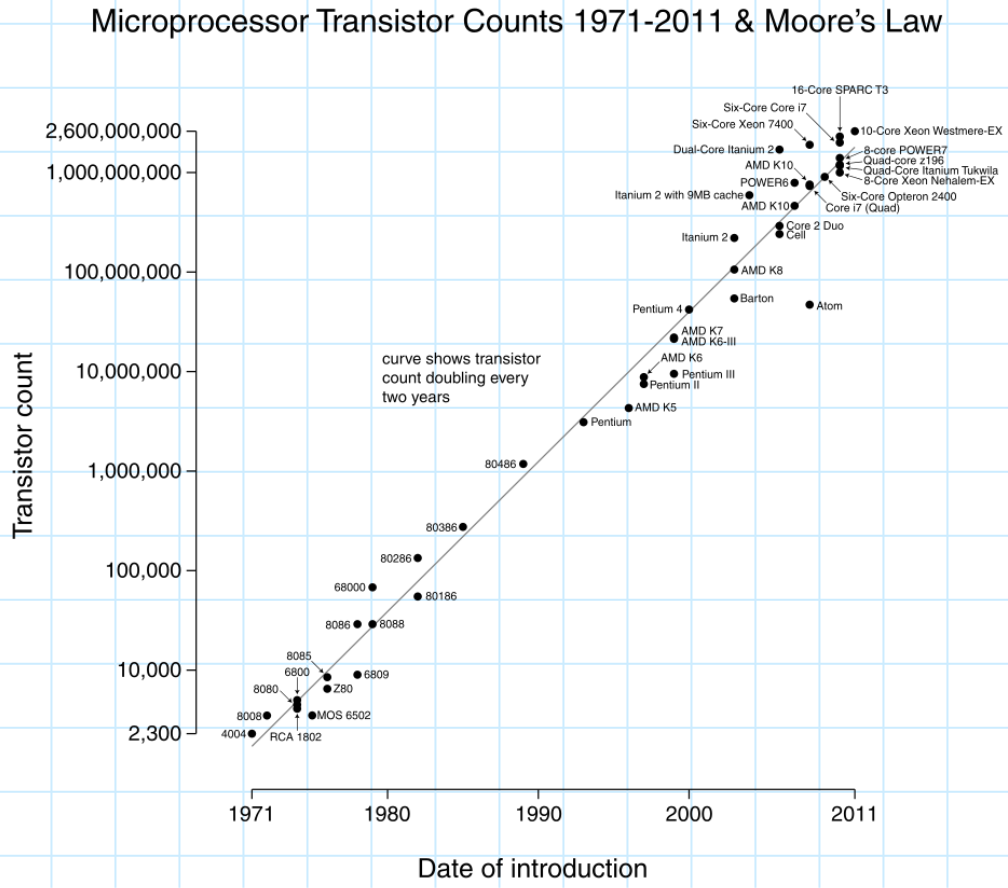
Intel Pentium



Intel-i7

4.1. Introduction. Moore's law

- 1965: Gordon Moore predicted the evolution of the number of transistors per chip
  - It fits a straight line in a semi-logarithmic scale
  - The number of transistors doubles every 18-24 months

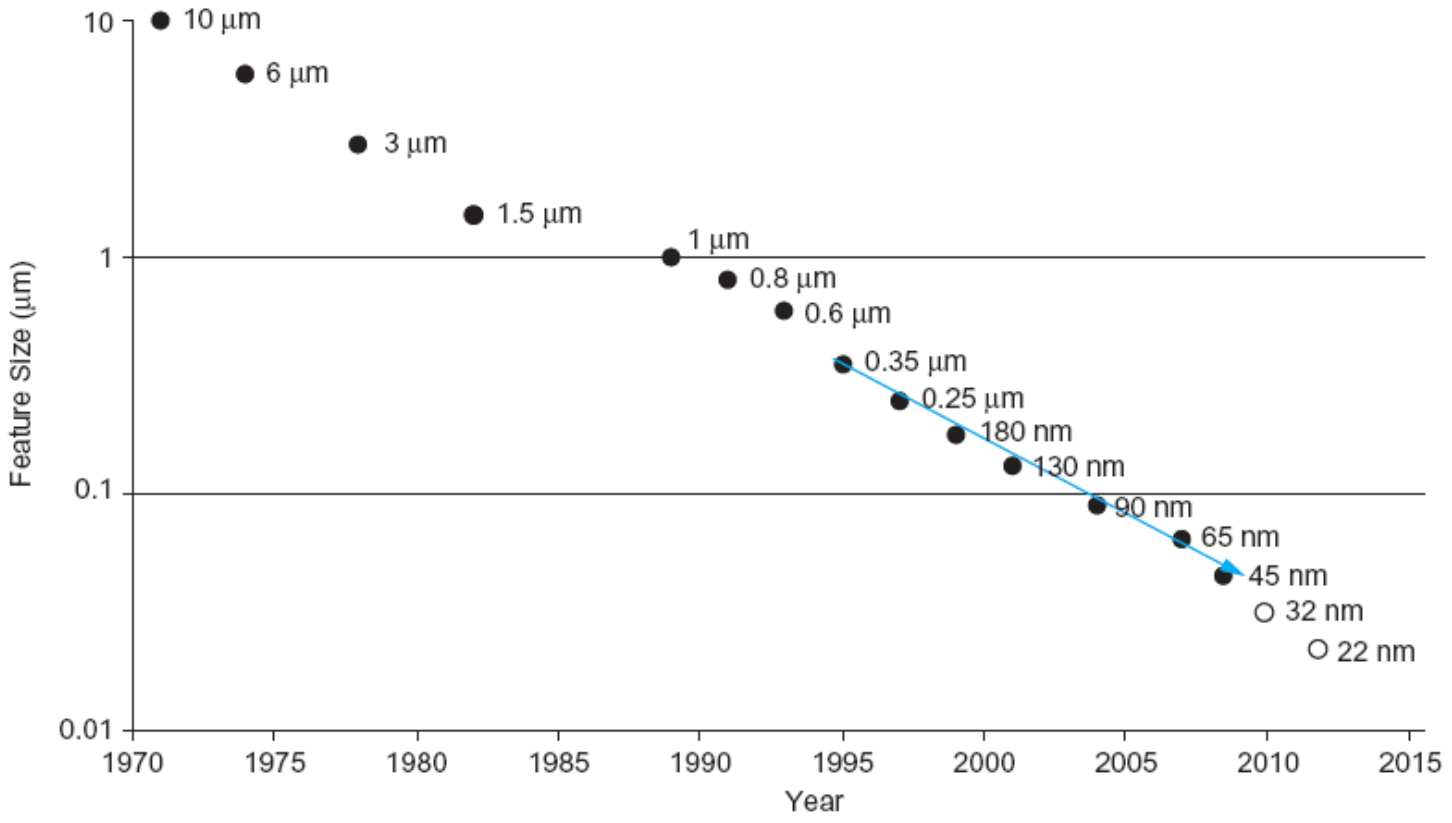


Integration Levels

SSI:	10 gates
MSI:	1000 gates
LSI:	10,000 gates
VLSI:	> 10k gates

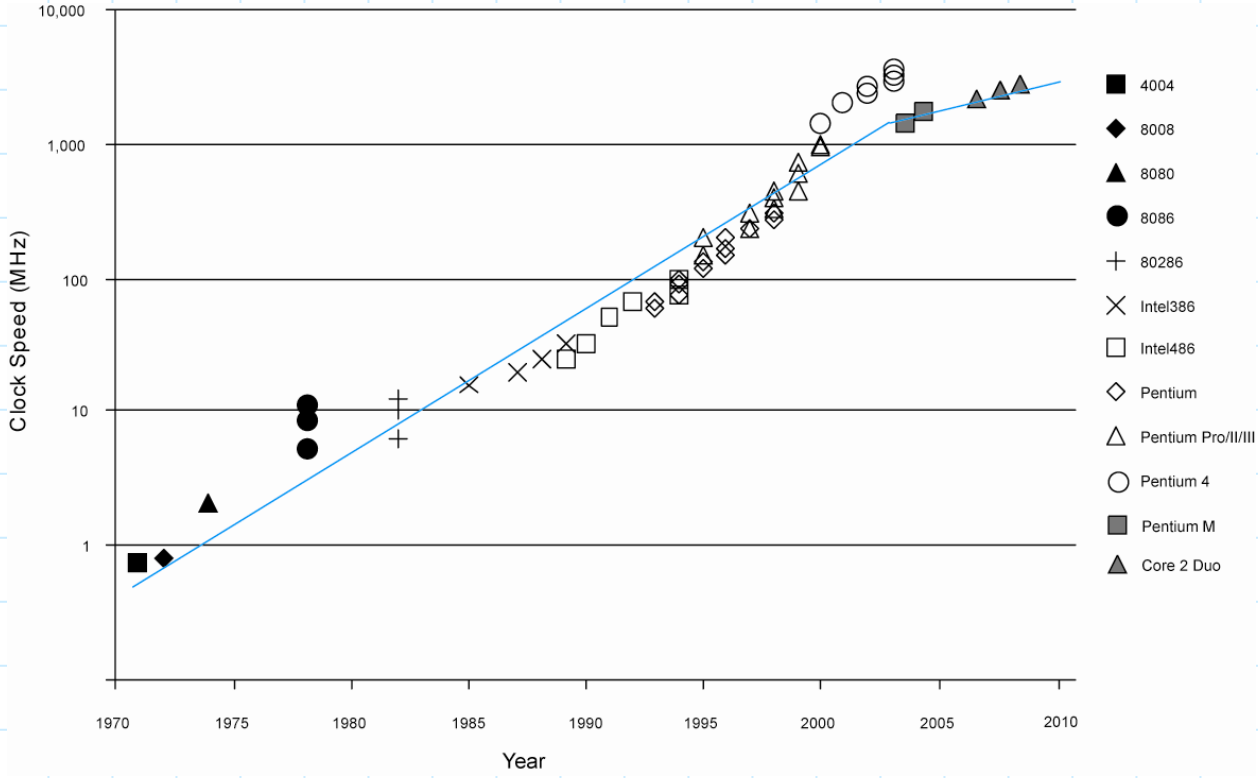
4.1. Introduction. Moore's law

- *Feature Size* brings down an 30% every 2-3 years



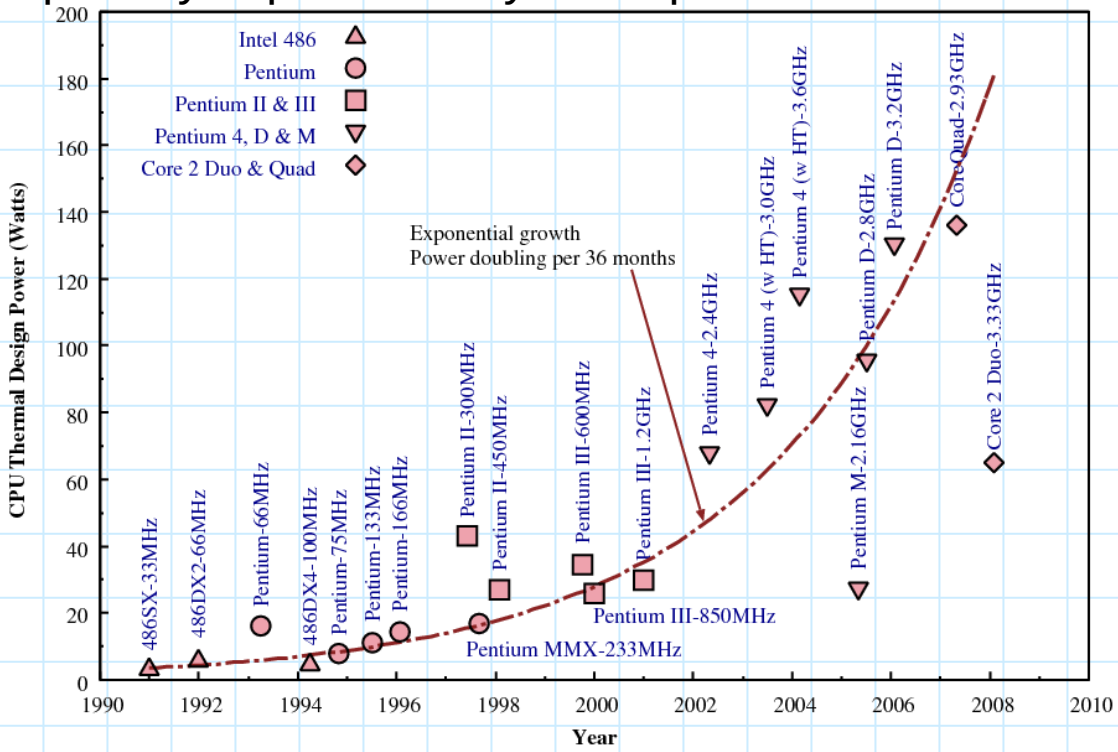
4.1. Introducción. Ley de Moore

- Many other factors grow exponentially
  - Ex: clock frequency, processor performance

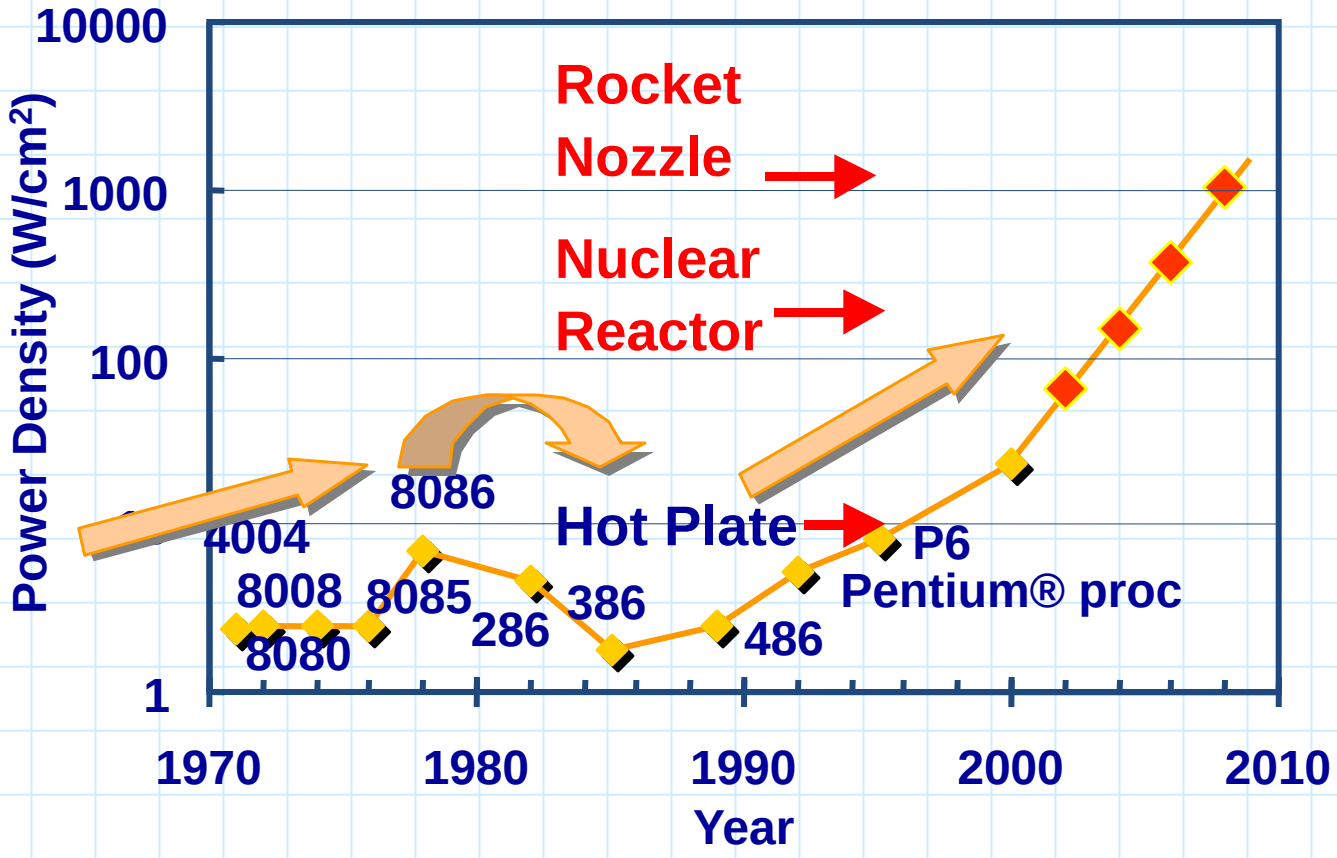


4.1 Introduction. Power

- The power consumed by chips has also grown exponentially, because:
  - Intensive integration, High frequency
- Power consumption is a key factor, as soon as:
  - Limits the integration density: Heat dissipation
  - It is specially important in systems powered with batteries



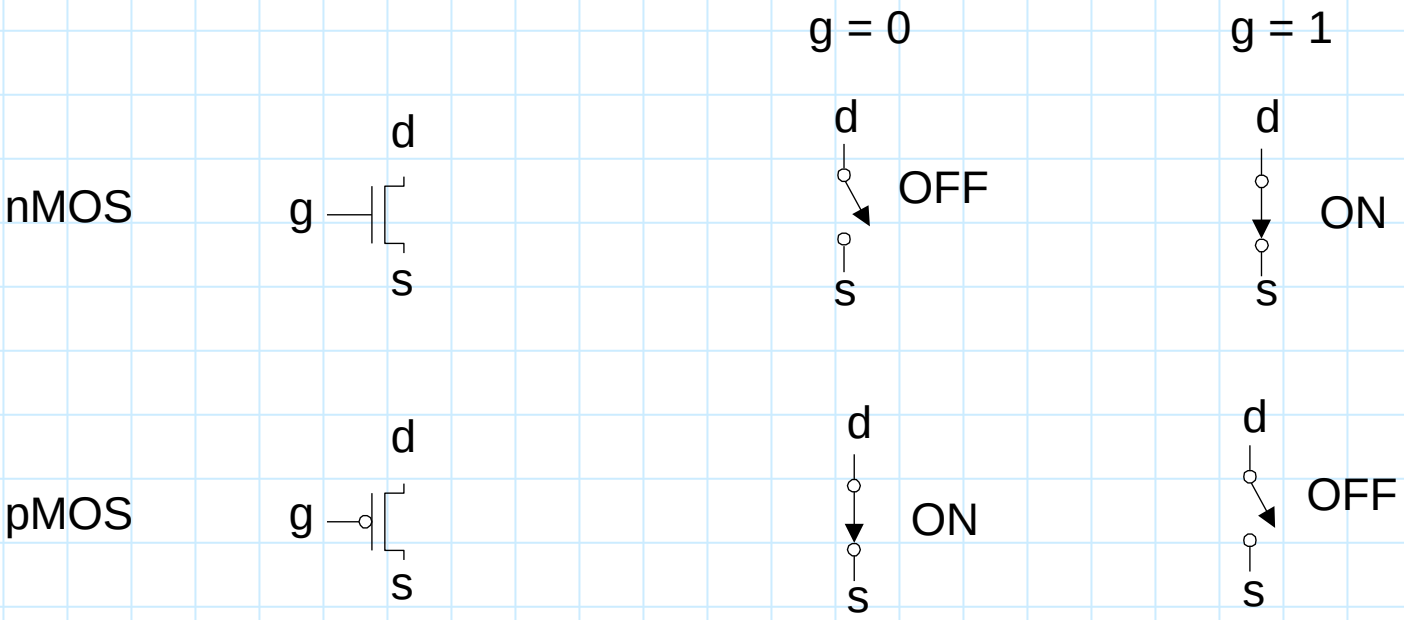
4.1 Introduction. Power density



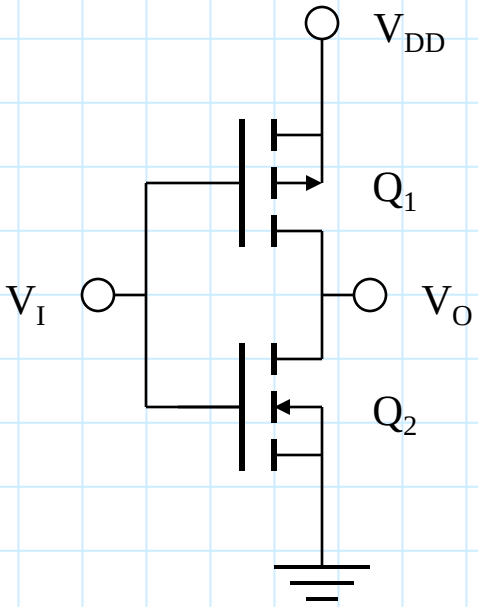
Courtesy, Intel

4.2. Combinational circuits

- MOS transistors as ideal switches:
  - MOS transistors can be seen as voltage-controlled switches (model)
  - The gate voltage controls the connection between drain and source terminals

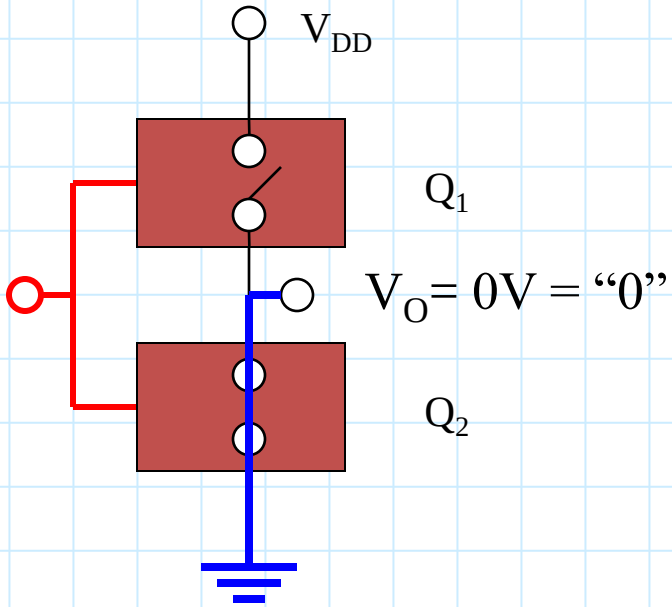


4.2.1 The CMOS inverter (review)



Digital input: $V_I = 0V$ = "0" $V_I = V_{DD}$ = "1"

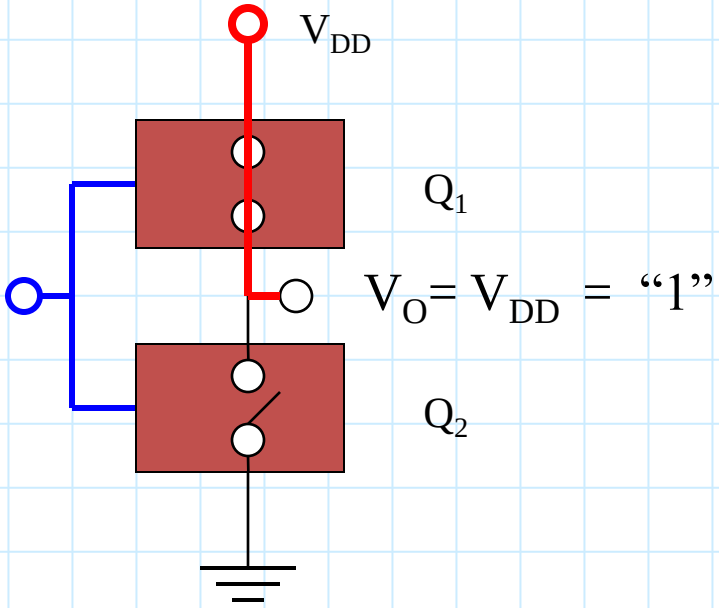
4.2.1 The CMOS inverter (review)



$V_{GS1} = V_{DD} - V_{DD} = 0V > -V_T$ ⇨ PMOS **OFF**
$V_{GS2} = V_{DD} - 0V = V_{DD} > V_T$ ⇨ NMOS **ON**

Static power consumption = 0 mW

4.2.1 The CMOS inverter (review)

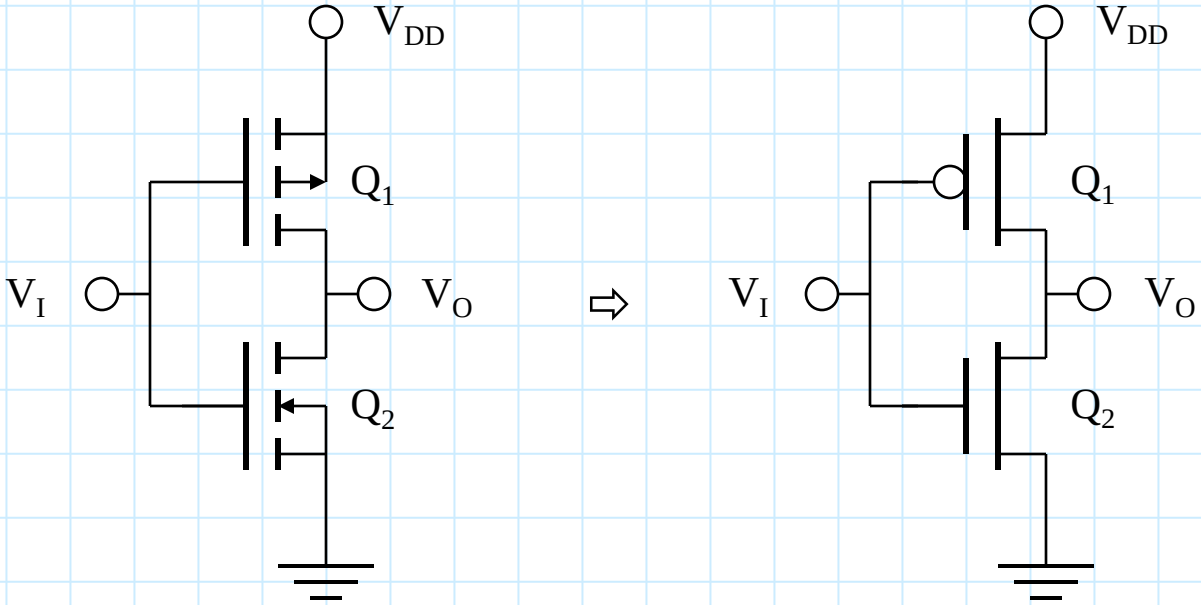


$V_{GS1} = 0V - V_{DD} = -V_{DD} < -V_T$ ⇨ PMOS **ON**
$V_{GS2} = 0V - 0V = 0V < V_T$ ⇨ NMOS **OFF**

Static power consumption = 0 mW

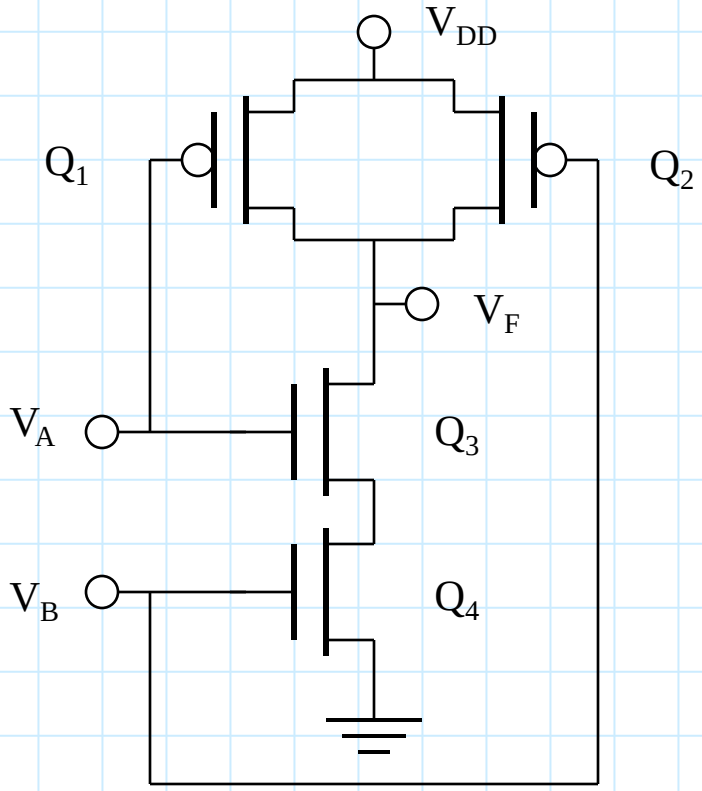
4.2.1 The CMOS inverter (review)

- An easier symbol for MOS transistors

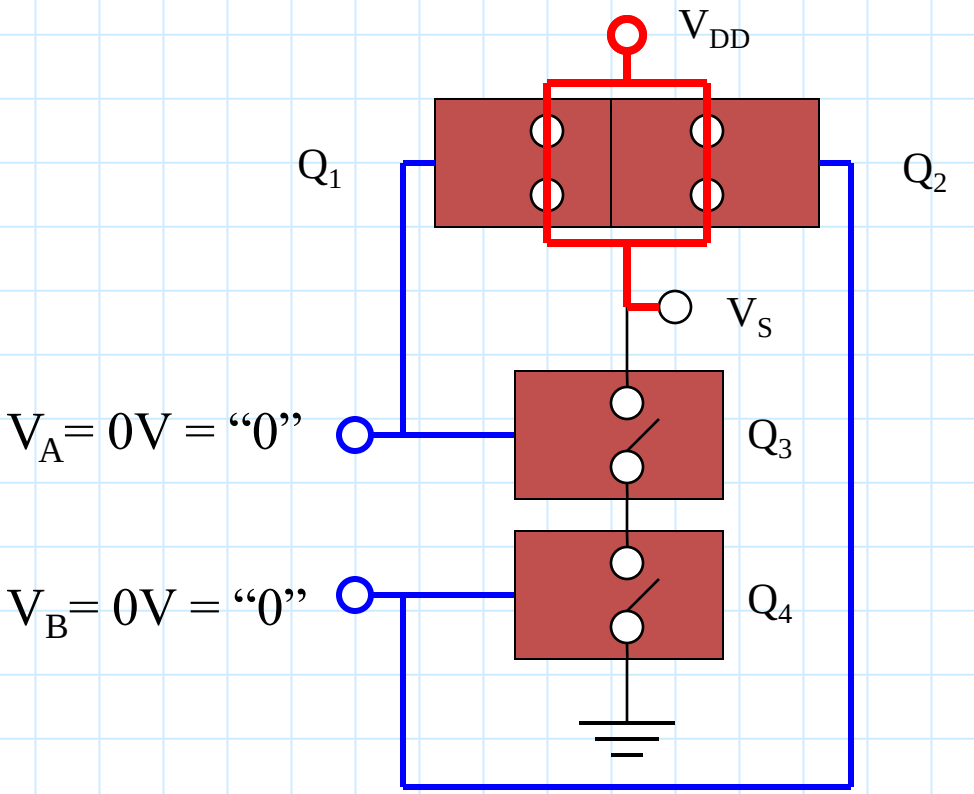


4.2.2 Other logic gates. NAND CMOS

- Structure: PMOS transistors in parallel and NMOS in series



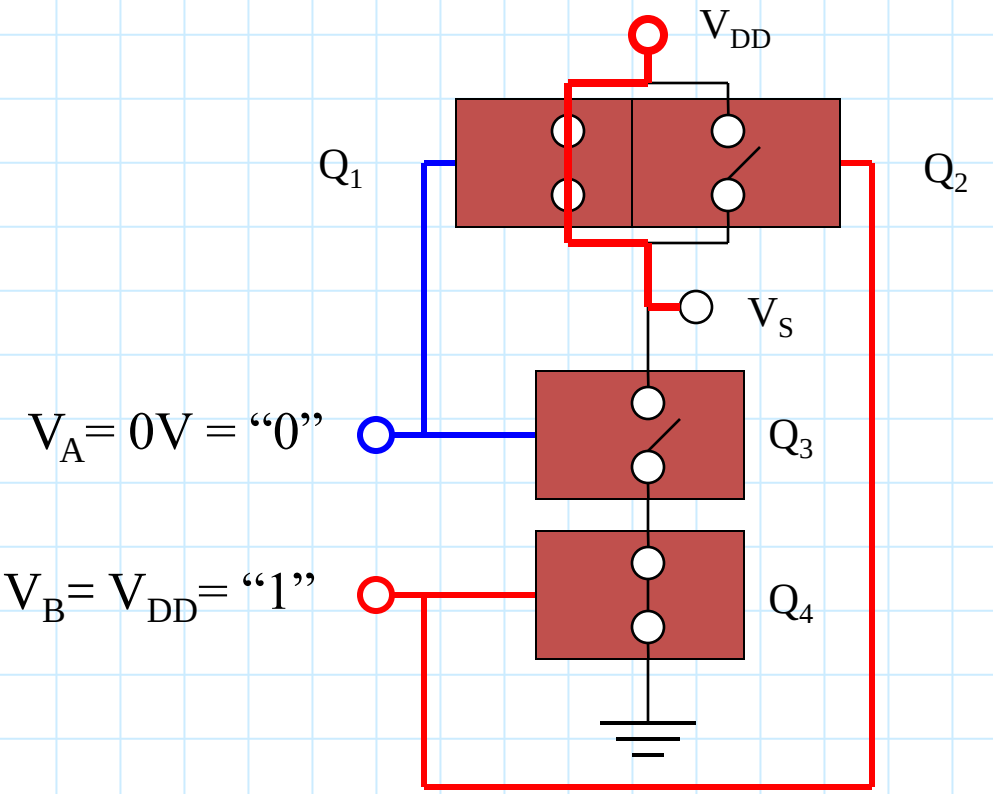
4.2.2 Other logic gates. NAND CMOS



V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	V_{DD}
V_{DD}	0V	V_{DD}
V_{DD}	V_{DD}	0V

Static power consumption = 0 mW

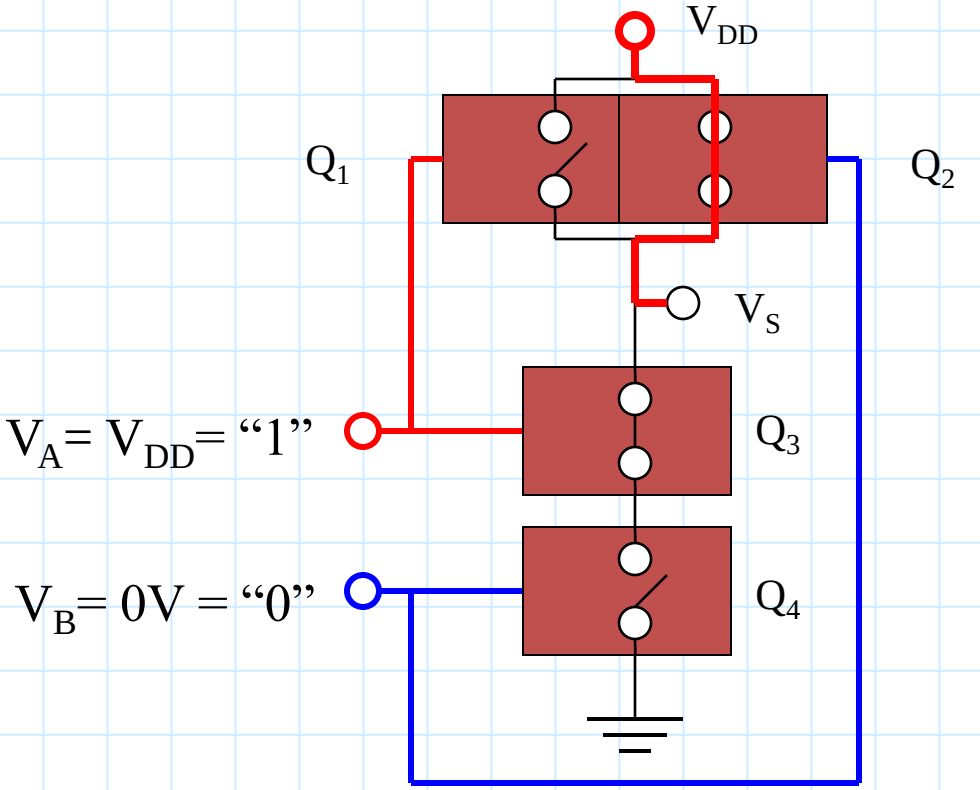
4.2.2 Other logic gates. NAND CMOS



V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	V_{DD}
V_{DD}	0V	V_{DD}
V_{DD}	V_{DD}	0V

Static power consumption = 0 mW

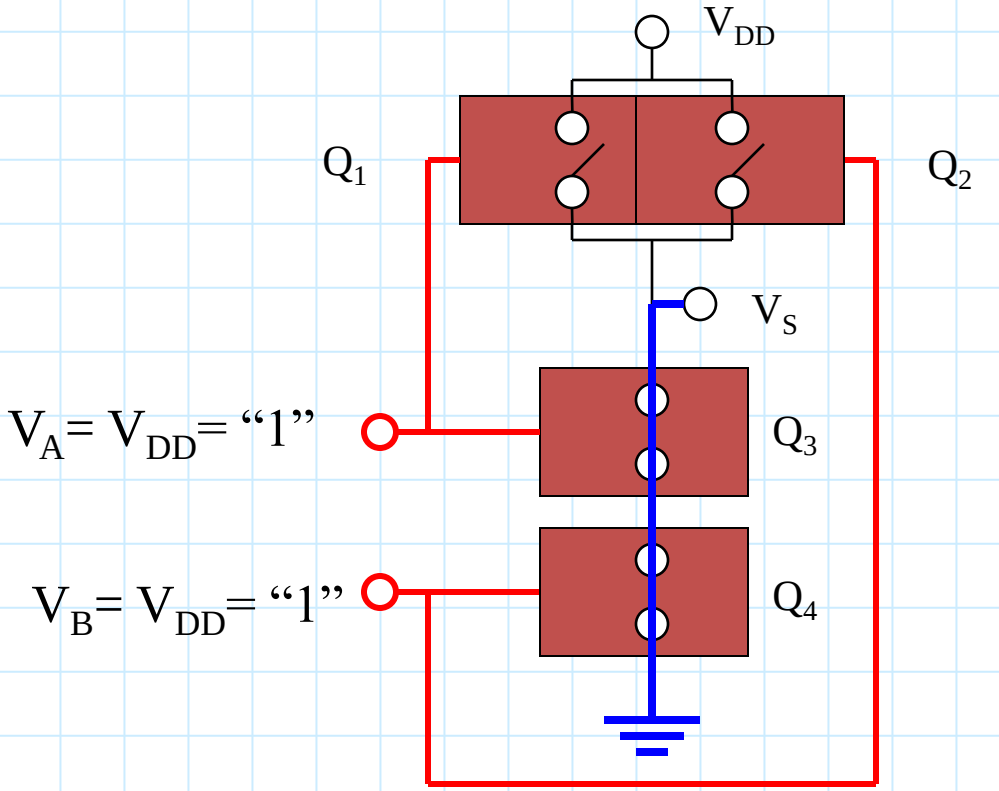
4.2.2 Other logic gates. NAND CMOS



V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	V_{DD}
V_{DD}	0V	V_{DD}
V_{DD}	V_{DD}	0V

Static power consumption = 0 mW

5.2.2 Other logic gates. NAND CMOS

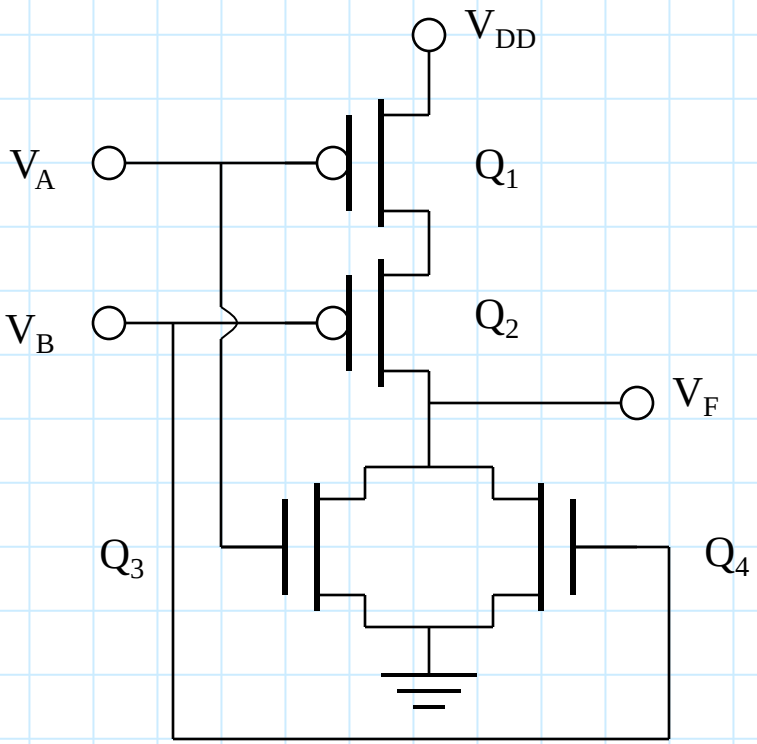


V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	V_{DD}
V_{DD}	0V	V_{DD}
V_{DD}	V_{DD}	0V

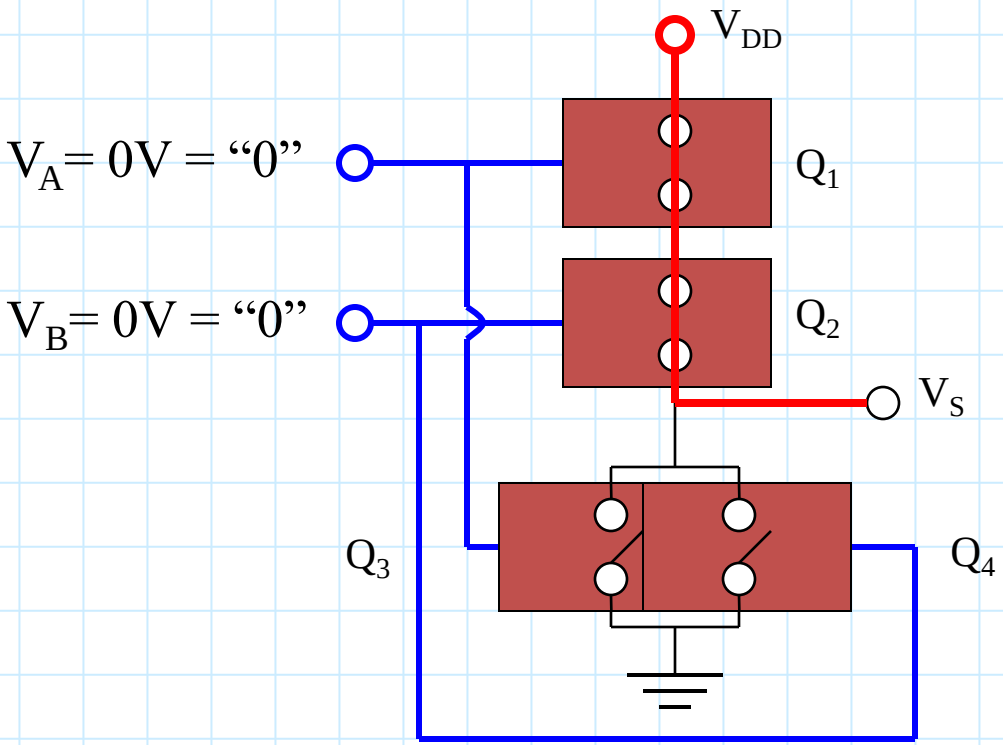
Static power consumption = 0 mW

4.2.2 Other logic gates. NOR CMOS

- Structure: NMOS transistors in parallel and PMOS in series



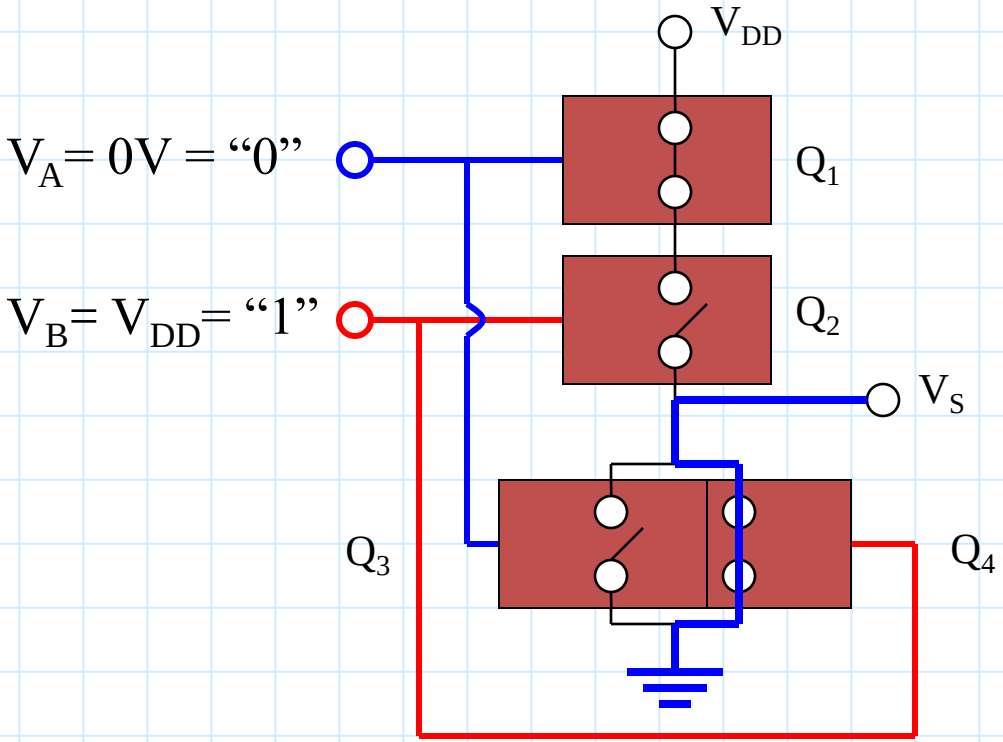
4.2.2 Other logic gates. NOR CMOS



V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	0V
V_{DD}	0V	0V
V_{DD}	V_{DD}	0V

Static power consumption = 0 mW

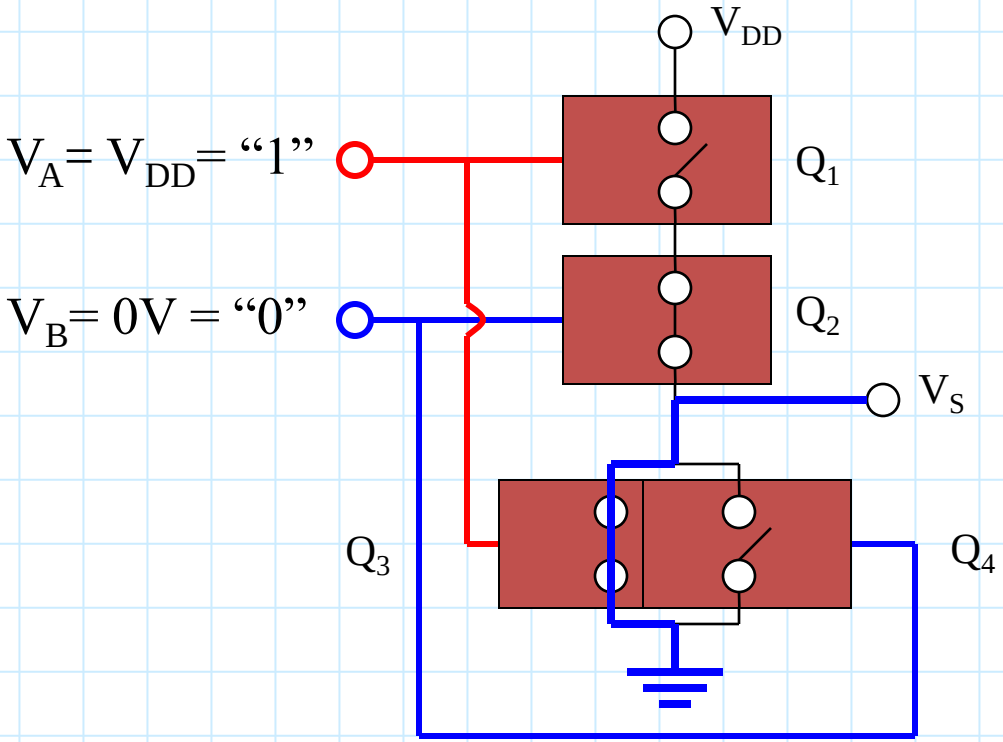
4.2.2 Other logic gates. NOR CMOS



V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	0V
V_{DD}	0V	0V
V_{DD}	V_{DD}	0V

Static power consumption = 0 mW

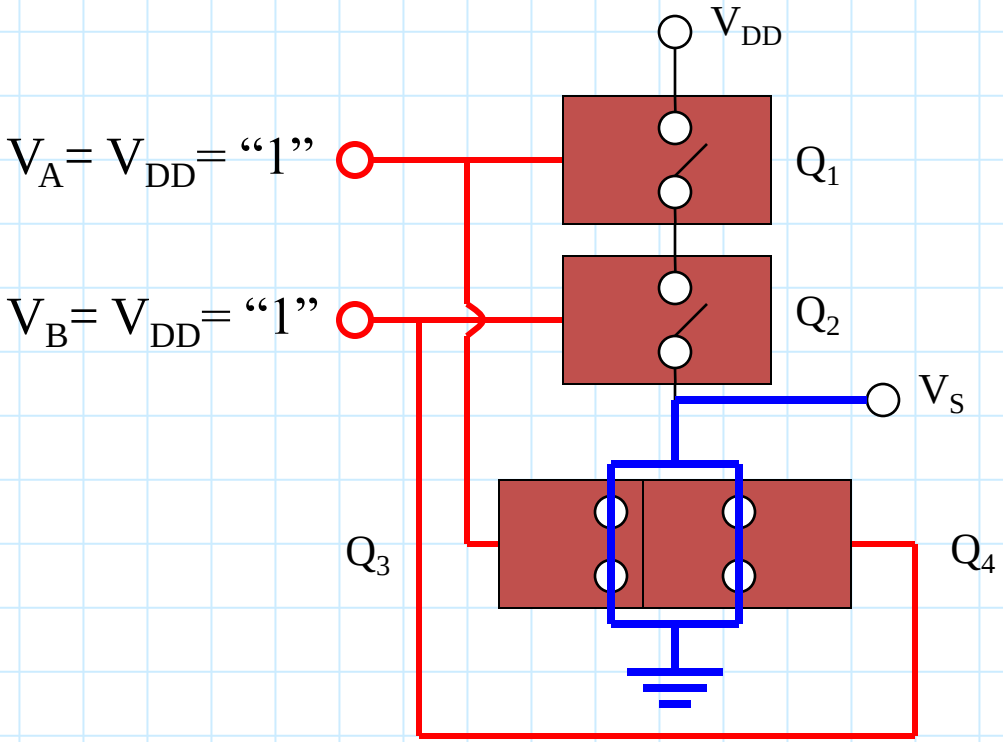
4.2.2 Other logic gates. NOR CMOS



V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	0V
V_{DD}	0V	0V
V_{DD}	V_{DD}	0V

Static power consumption = 0 mW

4.2.2 Other logic gates. NOR CMOS

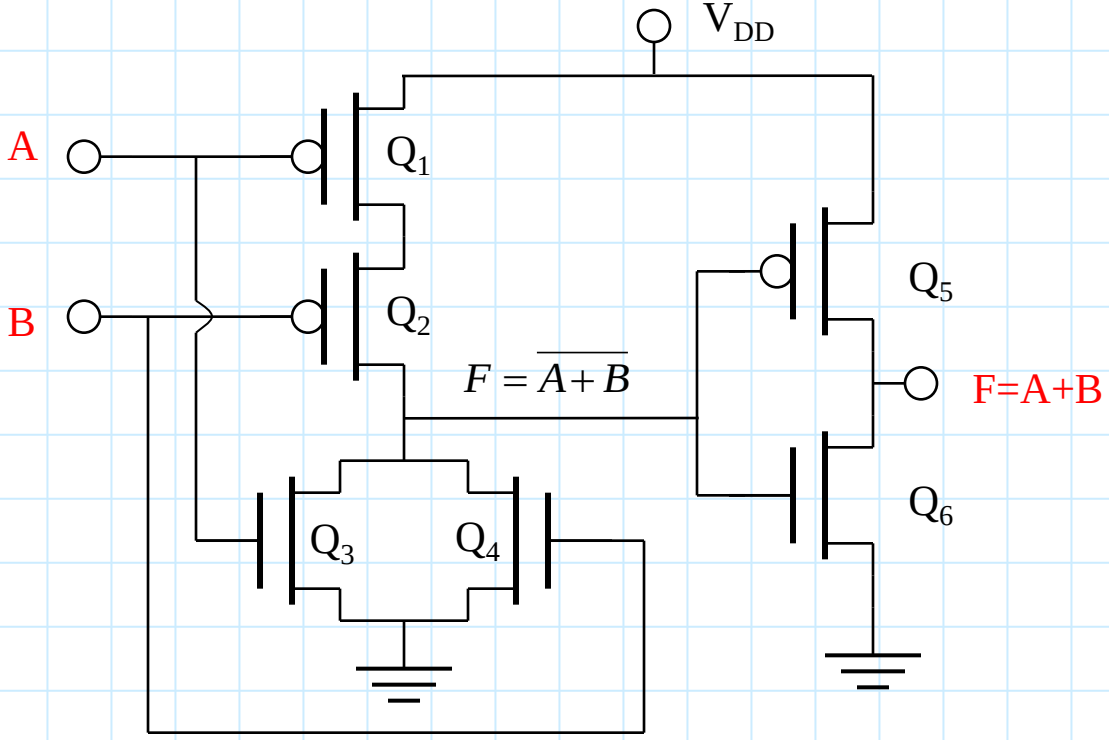


V_A	V_B	V_S
0V	0V	V_{DD}
0V	V_{DD}	0V
V_{DD}	0V	0V
V_{DD}	V_{DD}	0V

Static power consumption = 0 mW

4.2.2 Other basic gates

- Buffer = NOT + NOT
- AND = NAND + NOT
- OR = NOR + NOT



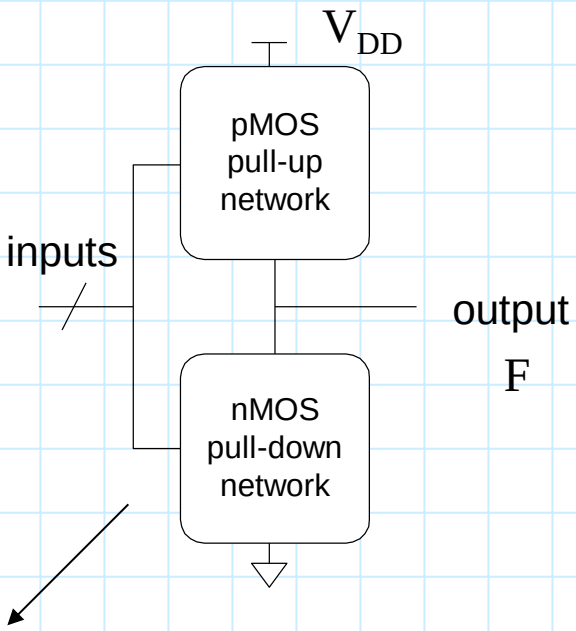
4.2.3 Design of general functions in CMOS Complementary Logic (1)

General case:

- NMOS and PMOS blocks are dual

  Series structures → · (AND)
  Parallel structures → + (OR)
  } → Intermediate function G

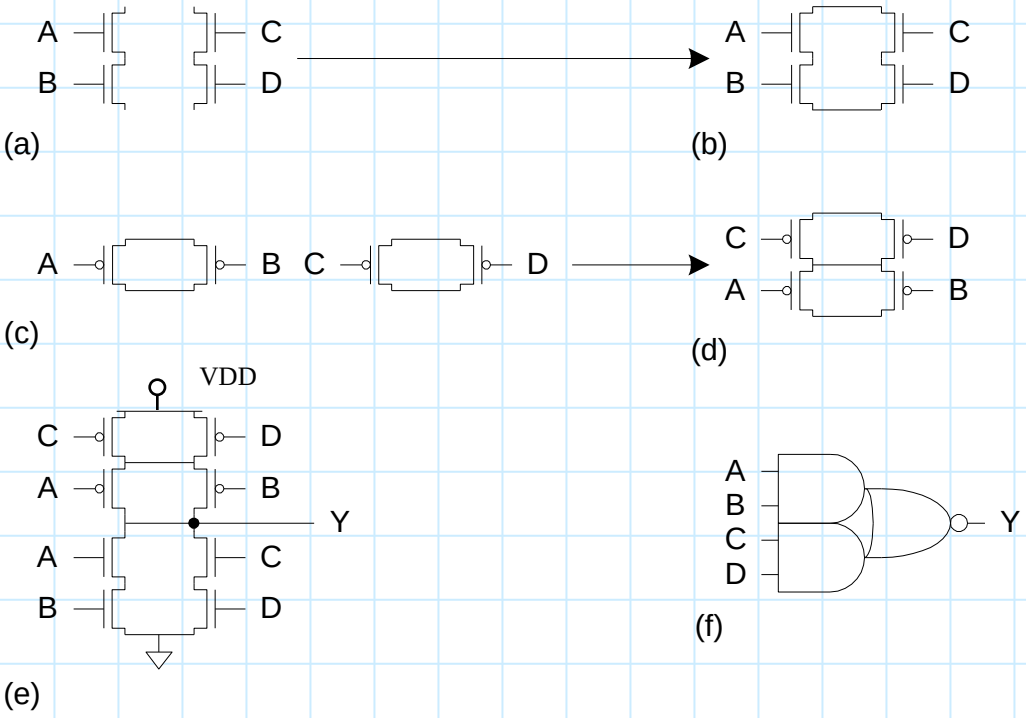
- NMOS block
  connected to ground
  F = $\overline{G}$
- PMOS block
  connected to VDD
  F = G, but inverted inputs



CMOS complementary logic

4.2.3 Design of general functions in CMOS Complementary Logic (2)

- Any inverted function can be implemented
- Ex: $Y = \overline{(A.B)+(C.D)}$ (AND-OR-INVERT-22)



NMOS block

Dual structure:
PMOS block

8 transistors

16 transistors

Chip area and power reduction

4.2.3 Design of general functions in CMOS Complementary Logic (3)

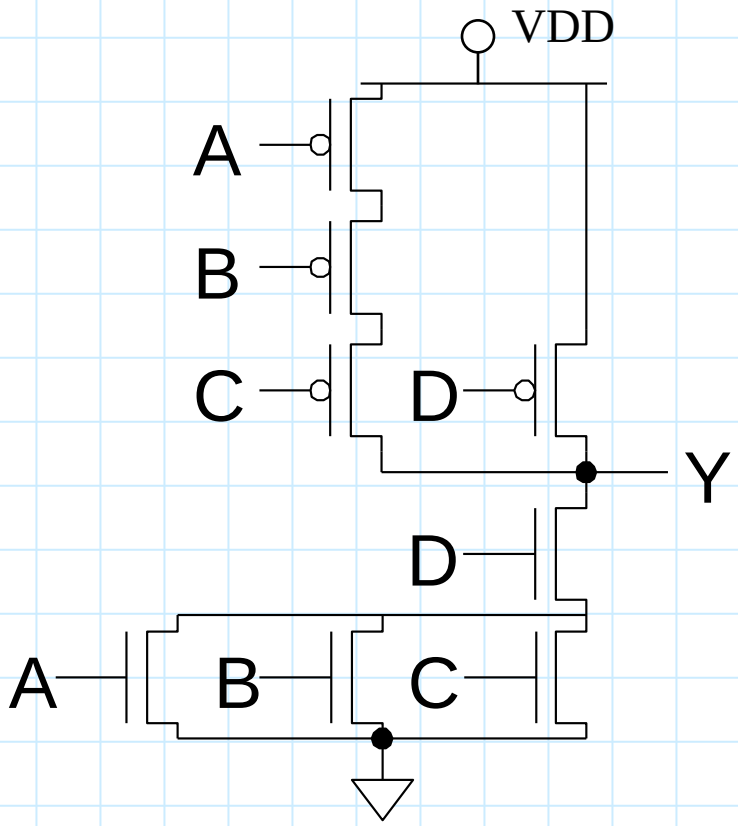
Example: OAI-31

$$Y = \overline{(A + B + C) \cdot D}$$

4.2.3 Design of general functions in CMOS Complementary Logic (4)

Example: OAI-31

$$Y = \overline{(A+B+C).D}$$



4.2.3 Design of general functions in CMOS Complementary Logic (5)

- If the function is not inverted:
- We have two solutions:
  1. Transform it to an equivalent inverted function, applying involution and De Morgan laws:
     - NMOS block design
     - PMOS block design with dual structure of NMOS block.
  2. Design from PMOS block, inverting the inputs. NMOS block is designed with the dual structure of the PMOS.
- Example: design the carry out function of a full-adder:

$$F = AB + AC + BC$$

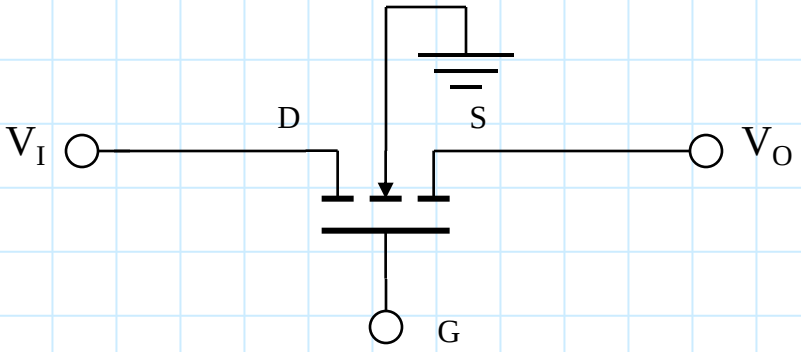
$$F = \overline{\overline{F}} = \overline{\overline{AB + AC + BC}} = \overline{(\overline{A} + \overline{B}).(\overline{A} + \overline{C}).(\overline{B} + \overline{C})}$$

$$G = (\overline{A} + \overline{B}).(\overline{A} + \overline{C}).(\overline{B} + \overline{C}) \rightarrow \text{Bloc NMOS}$$

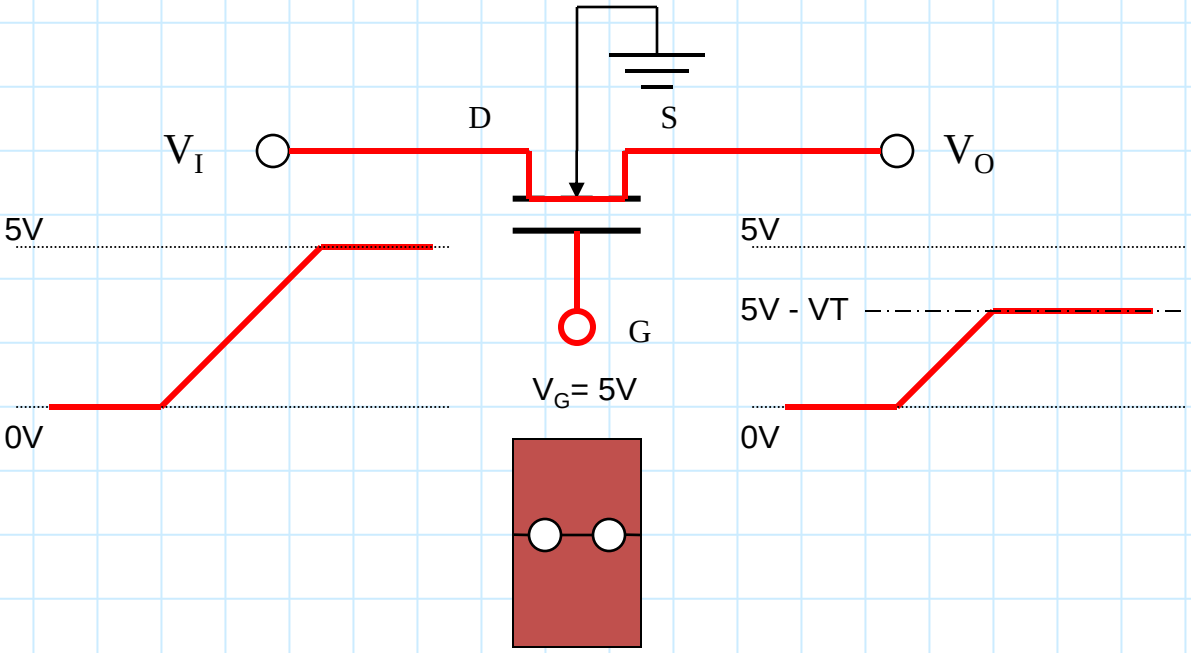
$$\text{Bloc PMOSdual}$$

4.2.4 Transmission gates (1): NMOS

- Bi-directional switch that opens or closes controlled by an external signal
  - NMOS transmission gate:
    - If $V_G = 0V \rightarrow$ Open Switch $\rightarrow V_O = 0V$
    - If $V_G = V_{DD} \rightarrow$ Closed Switch
      The transmission of "1" degrades V_T volts
      The transmission of "0" is not degraded

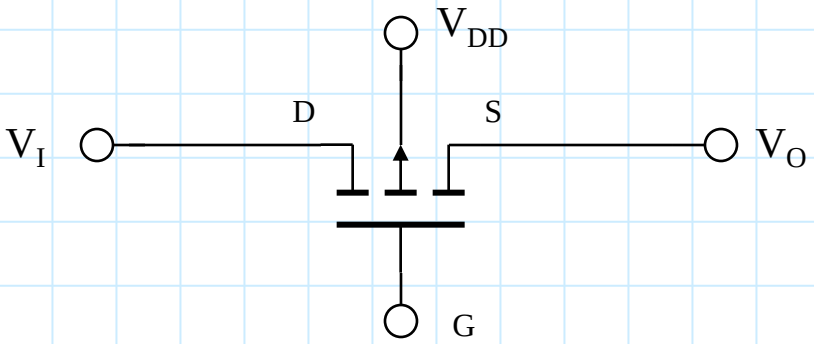


4.2.4 Transmission gates (2): NMOS

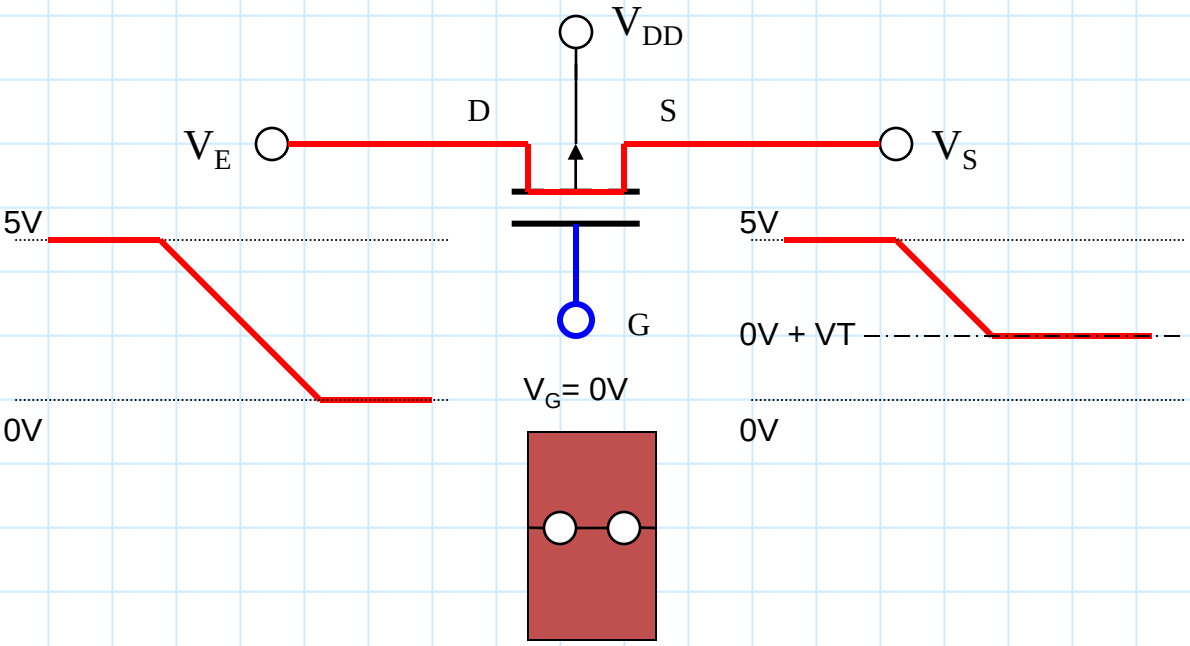


4.2.4 Transmission gates (3): PMOS

- PMOS transmission gate
  - If $V_G = V_{DD}$ → Open Switch → $V_O = 0V$
    If $V_G = 0V$ → Closed Switch
    The transmission of "1" is not degraded
    The transmission of "0" is degraded V_T

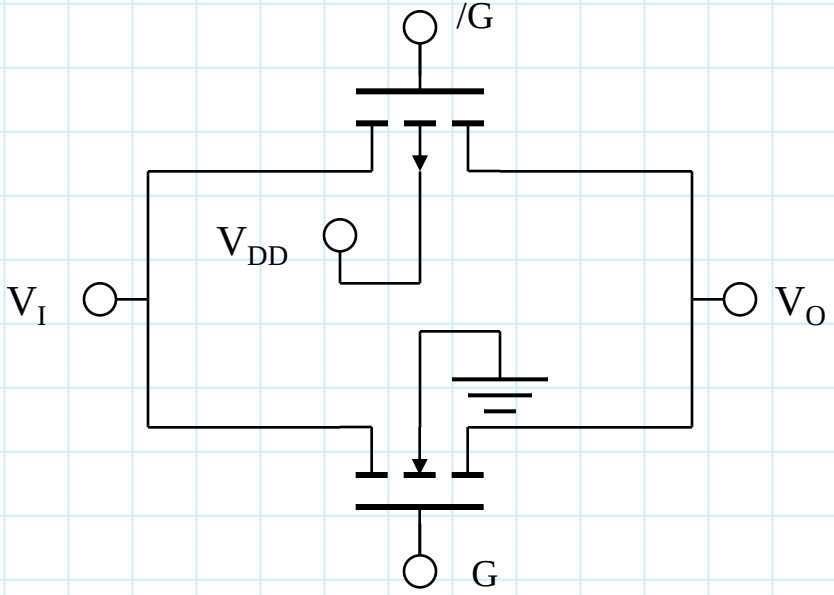


4.2.4 Transmission gates (4): PMOS



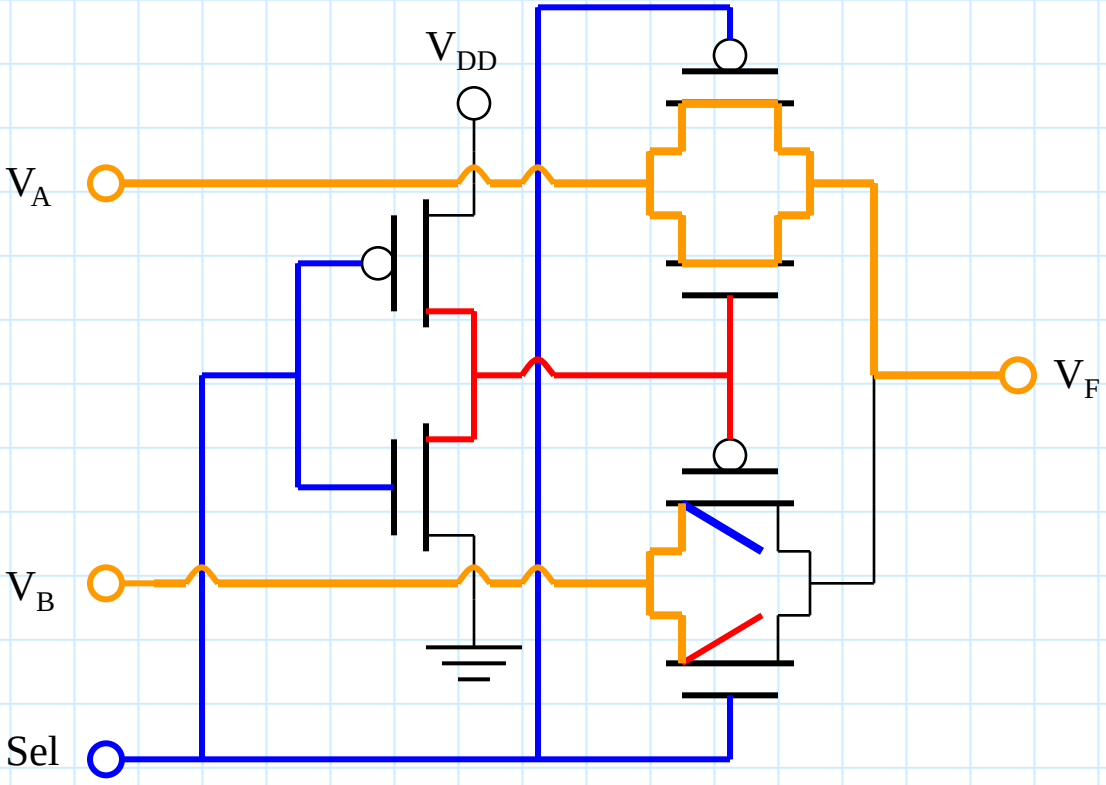
4.2.4 Puertas de transmisión (5): CMOS

- They join the characteristics of the two gates (NMOS and PMOS), not degrading the output
  - If V_G = 0V →NMOS and PMOS **OFF** →V_O = 0V
  - If $V_G = V_{DD}$ → NMOS and PMOS **ON**
    The NMOS transmits the "0" without degradation
    The PMOS transmits the "1 " without degradation



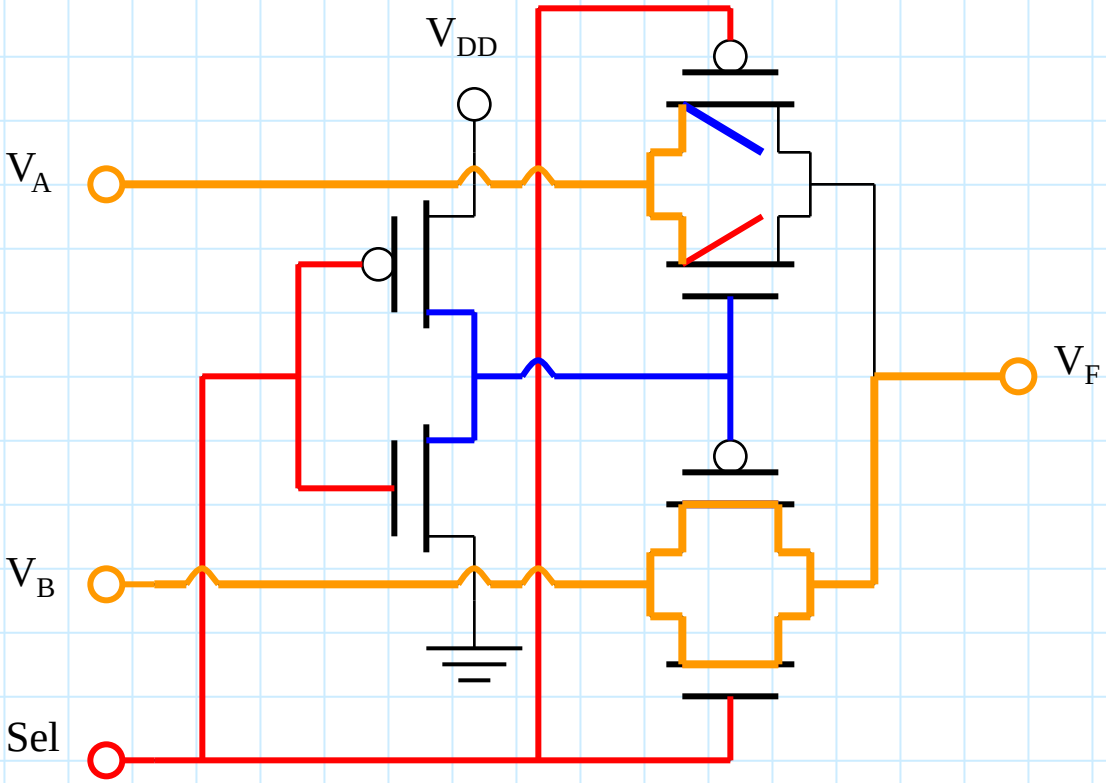
4.2.4 Transmission gates (6): Multiplexer

- Analog multiplexer
  - Inputs V_A, V_B, selection Sel, output V_F



Sel = “0”

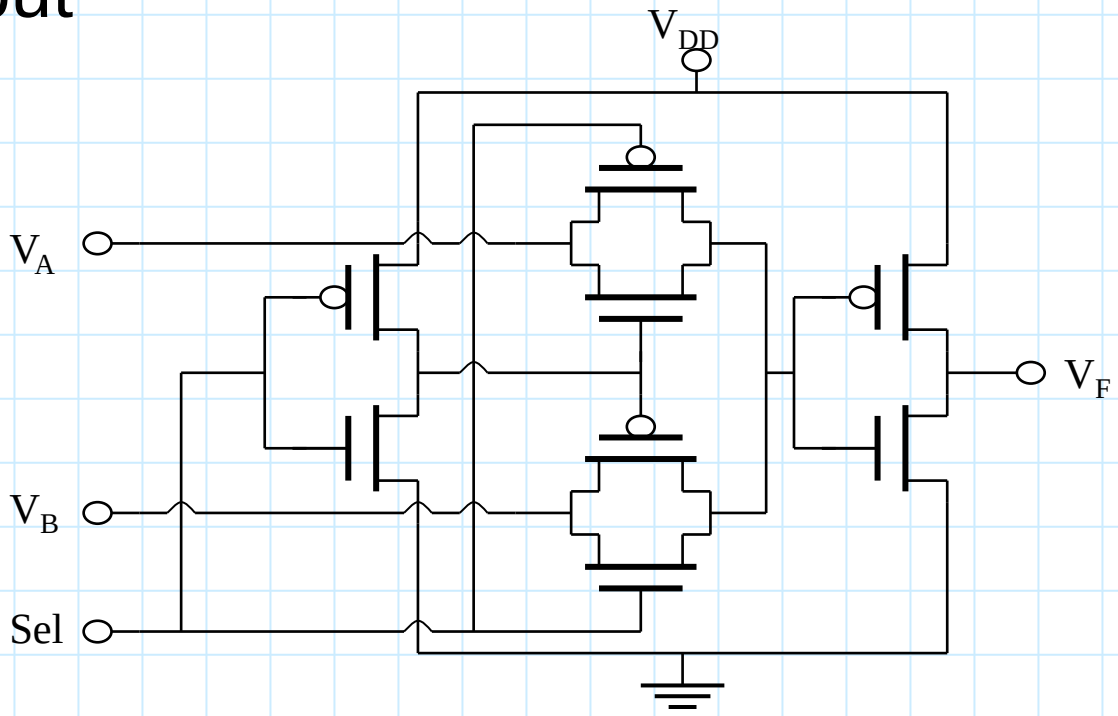
4.2.4 Transmission gates (7): Multiplexer



Sel = “1”

4.2.4 Transmission gates (8): Multiplexer

- Digital multiplexer: CMMOS inverter at the output



- 8 transistors →area and consumption saving, compared to a traditional design

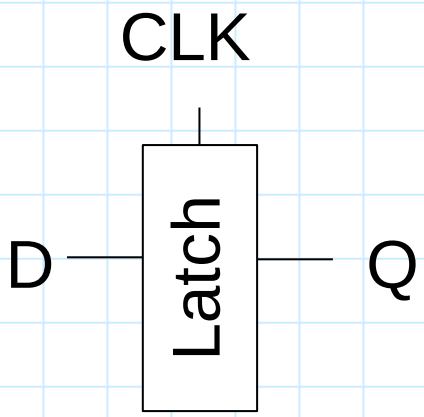
4.2.4 Transmission gates (9): Multiplexer

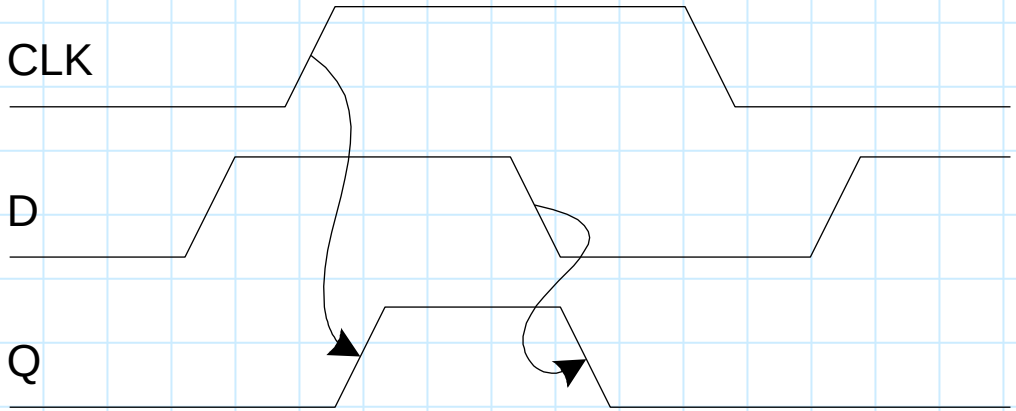
- Design of the multiplexer with basic gates:
- How many transistors do we need? (exercise)

$$F = B \cdot Sel + A \cdot \overline{Sel}$$

4.3 Latches and Flip-flops (1): The D Latch

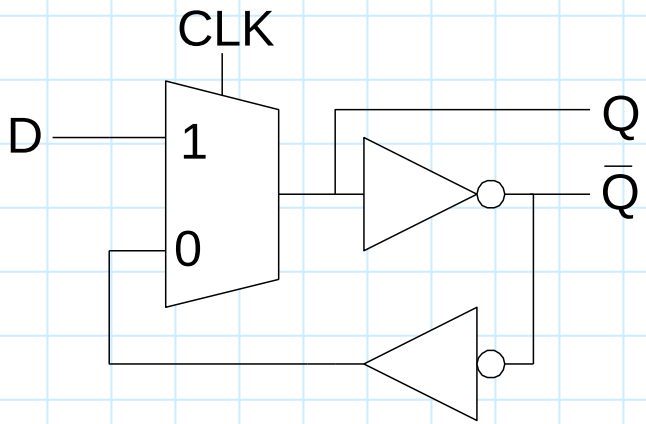
- If CLK = 1, the latch is transparent
  - (we can see D from Q)
  - D is transmitted to Q as in a buffer
- If CLK = 0, the latch is opaque
  - (we can see nothing from Q)
  - Q stores the old value independently of D
- Also called transparent or level-triggered latch

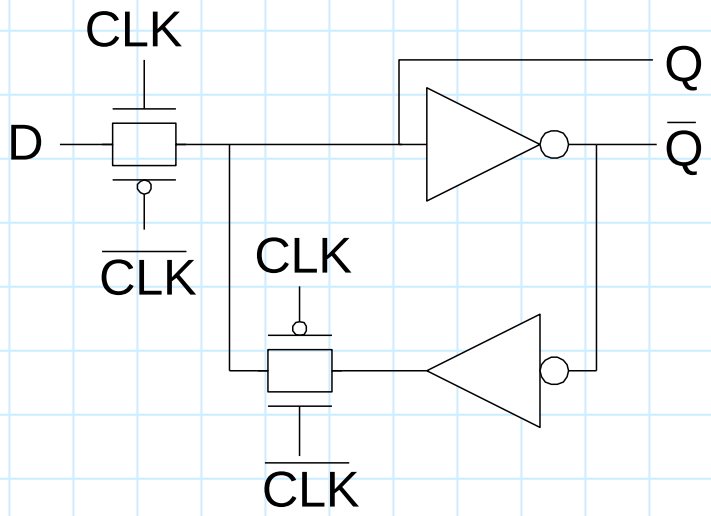




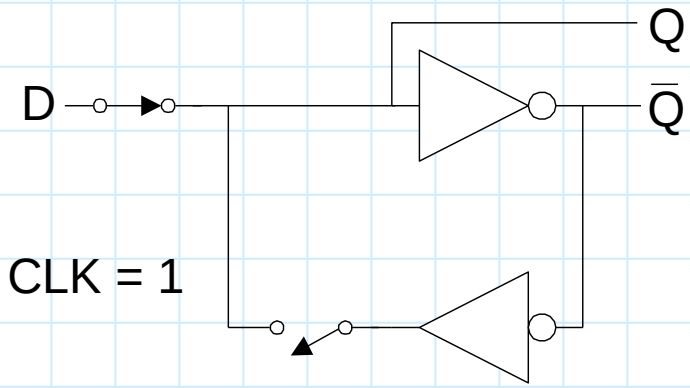
4.3 Latches and Flip-flops (2): Design of a D Latch from transmission gates

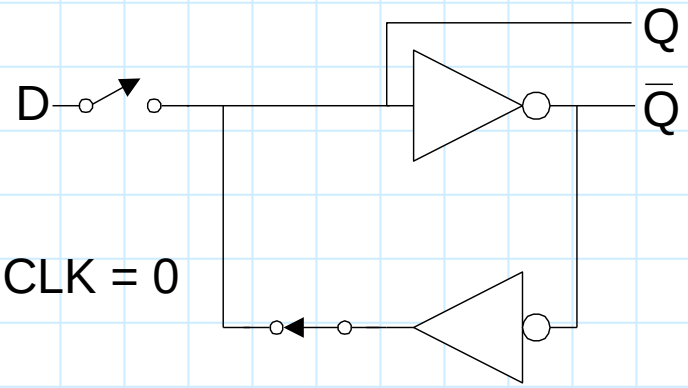
- Multiplexer selects D or holds Q

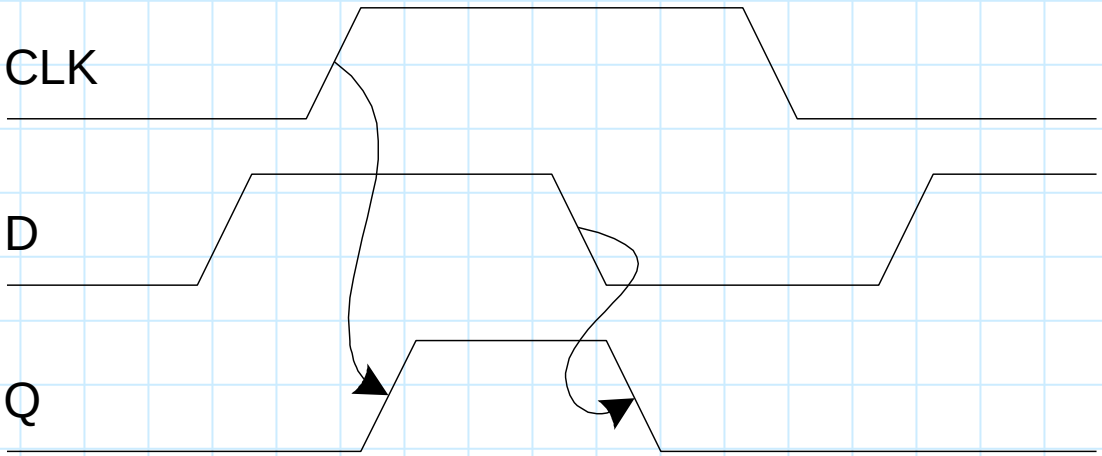




4.3 Latches and Flip-flops (3): Latch D operation

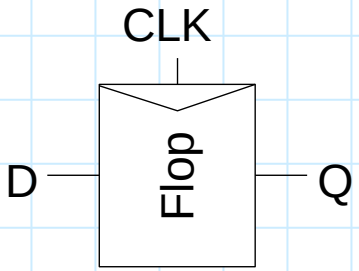


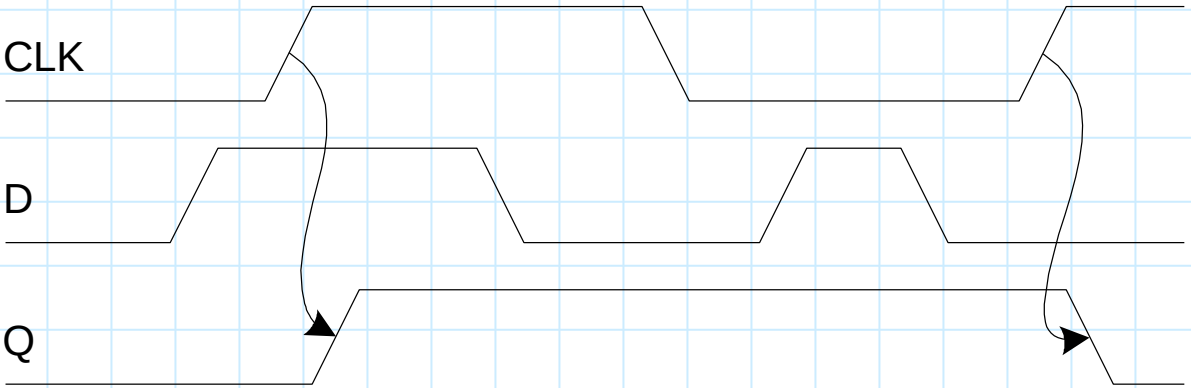




4.3 Latches and Flip-flops (4): The D Flip-flop

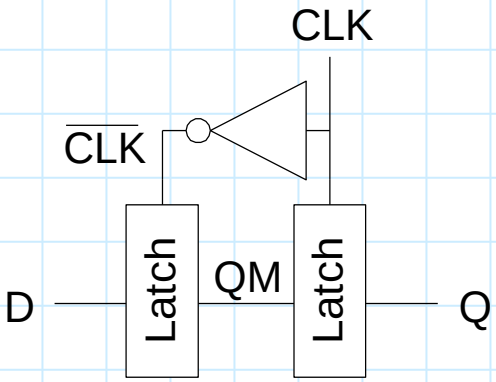
- When CLK has a rising edge, D passes to Q
- Otherwise, Q holds its old value
- Also called edge-triggered flip-flop, master-slave flip-flop

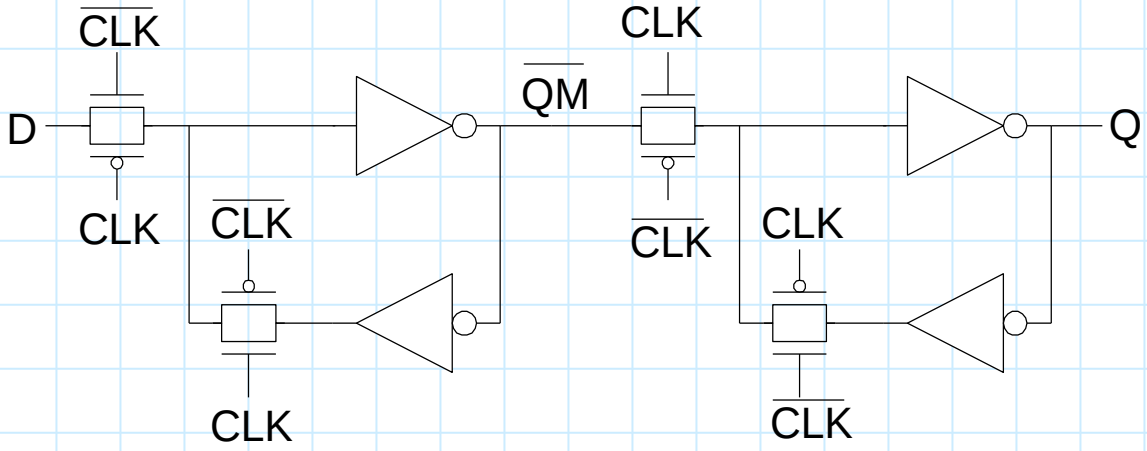




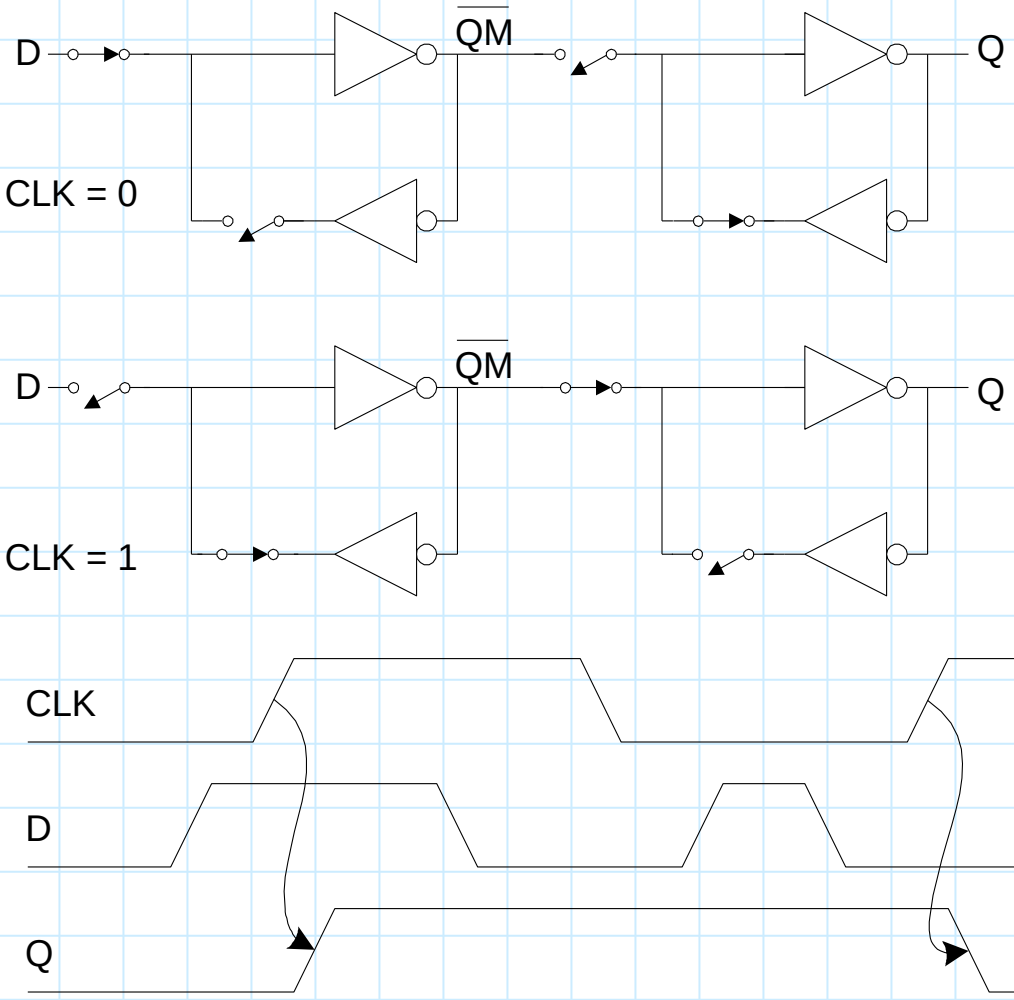
4.3 Latches and Flip-flops (6): Design of a D Flip-flop

- Master-slave design from latches:



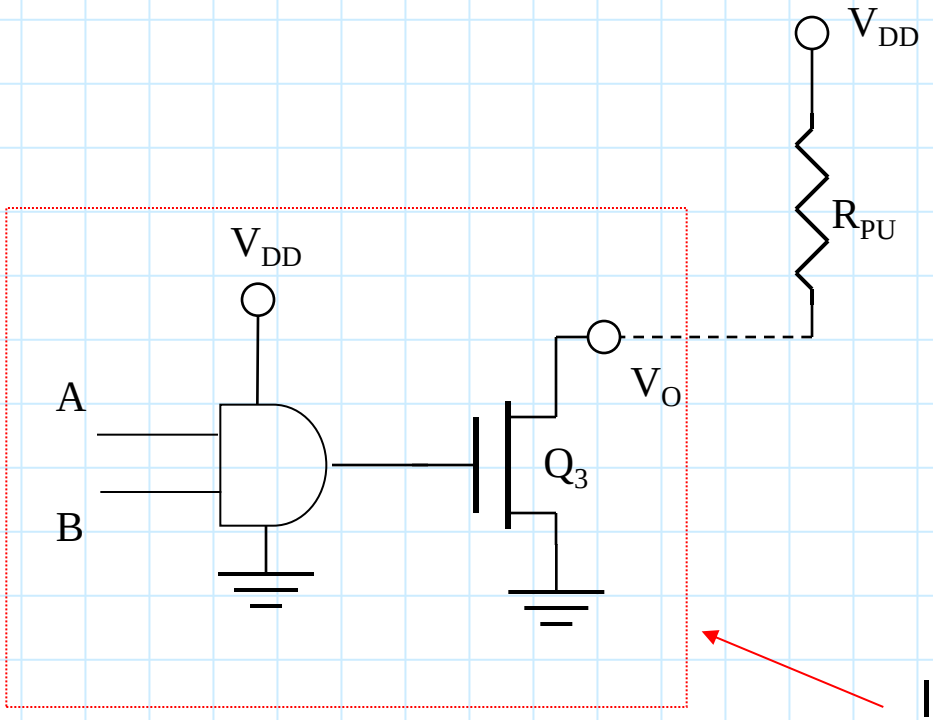


4.3 Latches and Flip-flops (6): D Flip-flop operation



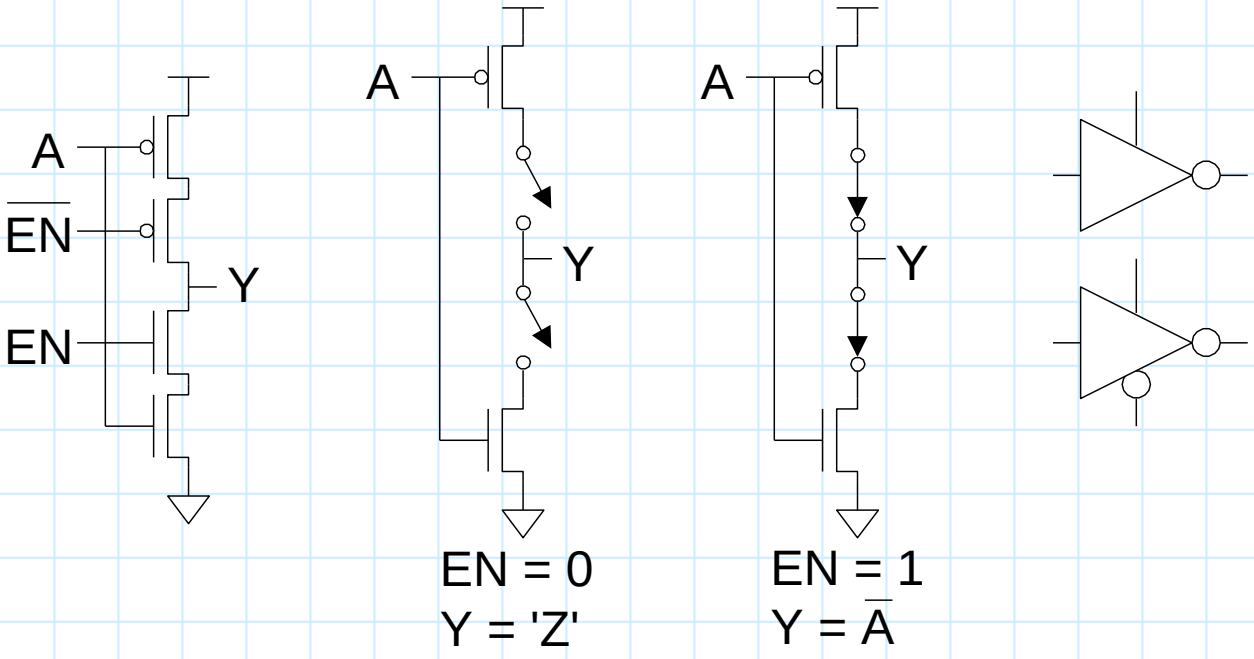
4.4 CMOS special outputs (1)

- Open-drain output
- Open-drain CMOS NAND
- R_{PU} is required



4.4 CMOS special outputs (2)

- Tri-state output:
  - Tri-state inverter



- Tri-state buffer (not inverting buffer):
  - Inverter+Tri-state inverter

4.5 Characteristic parameters (related to standard CMOS)

- Supply voltage:
  - V_{DD} typically between 3V and 15V in SSI and MSI chips
  - GND (V_{SS}) = 0 V
  - In 1980's, V_{DD} = 5V
  - V_{DD} has been reducing over the years in VLSI chips:
    - High V_{DD} may affect small current transistors of nowadays
    - A low V_{DD} decreases power consumption
    - V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, ...
    - VLSI chips have normally with 2 voltage supplies:
      - Logic "Core“: low V_{DD} (e.g. 1V)
        I/O cells: high V_{DD} (e.g. 2.5V)

4.5 CMOS characteristic parameters (2)

- Power Consumption:
  - Consequences:
    - Battery life (portable systems)
    - Wiring design (V_{DD}, V_{SS})
    - Refrigeration systems
    - Noise immunity
    - Reliability
  - Static consumption and Dynamic consumption:

$$P_{total} = P_{static} + P_{dynamic}$$

4.5 CMOS characteristic parameters (2)

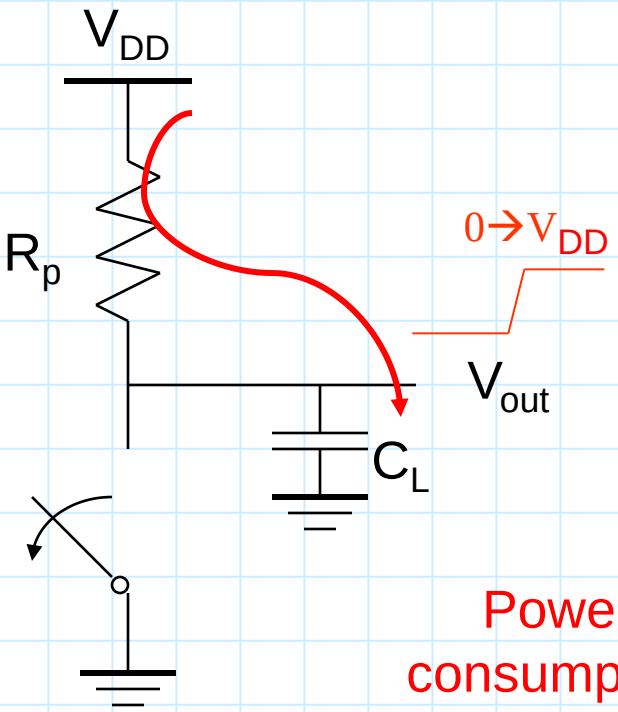
- Power Consumption:
  - Static regime: virtually null (≈ nA, pA), as there is always a transistor in cut-off mode (PMOS or NMOS)
  - Leakage currents:
    - Insulated Gate
    - Subthreshold (when $V_{GS} < V_T$ if V_T is very small)
    - Increasingly important in VLSI (a billion transistors nowadays)

$$P_{leakage} = V_{DD} \times I_{leakage}$$

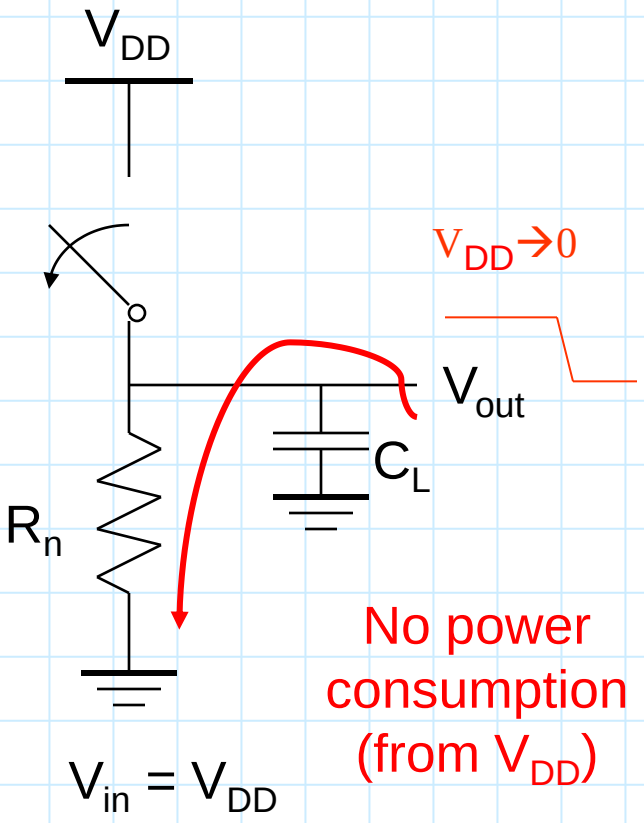
4.5 CMOS characteristic parameters (3)

- Dynamic regime: $P_d = (V_{DD})^2 C_L f_i$, where:
  - C_L → parasitic capacitance of the load
  - f_i → switching frequency of inputs
  - This dissipated power is due to:
    - loading / unloading of C_L
    - Current peaks during transitions: the two transistors (PMOS and NMOS) conduct simultaneously.
  - Dynamic power consumption is the most important in CMOS technology:
    - In fact, static power consumption can be neglected
  - Note: If we refer P_d to the clock frequency "f" of the system:
    - $P_d = \alpha (V_{DD})^2 C_L f$, where:
    - α → average activity factor of the inputs (average number of transitions in one clock cycle)
    - $\alpha < 1$

4.5 CMOS characteristic parameters (4): Dynamic power consumption



Power consumption (from V_{DD})

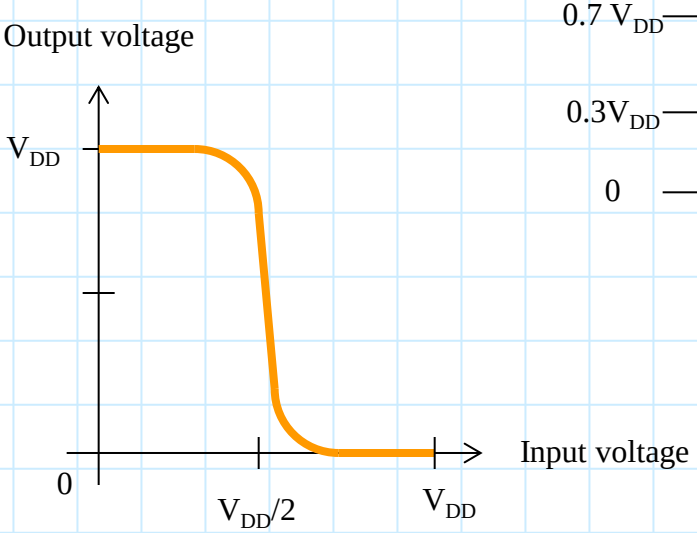


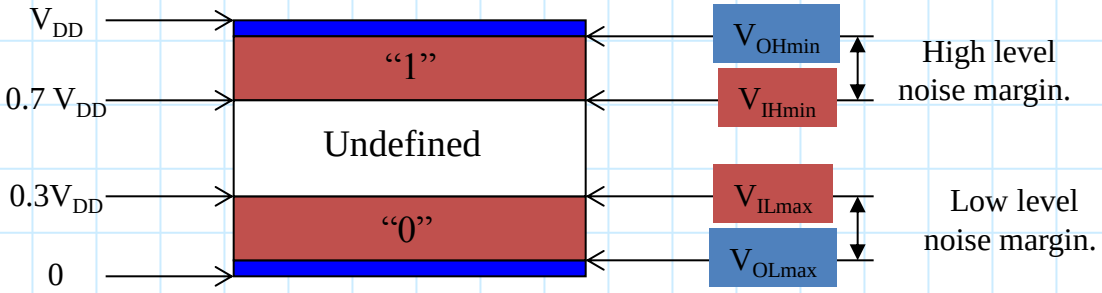
No power consumption (from V_{DD})

- The relevant dynamic consumption occurs in the transition L → H
- In the transition H → L there are only consumption due to simultaneous conduction of 2 transistors: short circuit.

4.5 CMOS characteristic parameters (5)

- Logic levels. Noise Immunity
  - Very ideal transfer curve





Standard CMOS values:

$V_{OHmin} = V_{DD} - 0.1V$

$V_{OLmax} = 0.1V$

$NM \approx 30\% V_{DD}$

Excellent noise inmunity (increases with V_{DD})

4.5 CMOS characteristic parameters (6)

- Current levels. FAN-OUT (Standard CMOS current values)

I_{OH}	-0.5 mA	High level output current	Exits
I_{OL}	0.5 mA	Low level output current	Enters
I_{IH}	10 pA	High level input current	Enters
I_{IL}	-10 pA	Low level input current	Exits

- Very small input currents → We can connect a lot of inputs to a single output

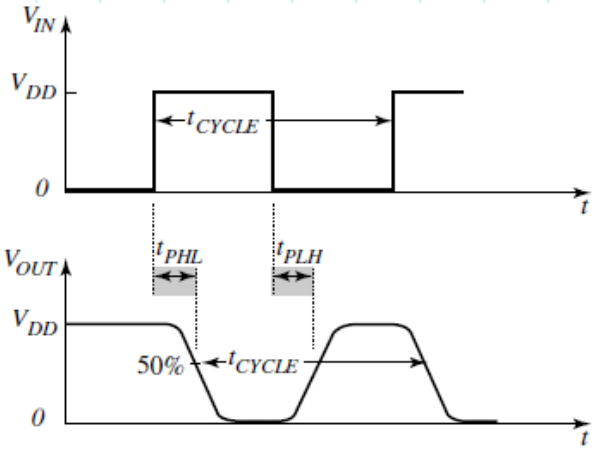
$$Fan-Out_L = \left|\frac{I_{OL}}{I_{IL}}\right| = 50.000.000 \qquad Fan-Out_H = \left|\frac{I_{OH}}{I_{IH}}\right| = 50.000.000$$

- Real constraint to not increase the delays and dynamic power consumption: the manufacturer recommends Fan-out = 50

4.5 CMOS characteristic parameters (7)

- Propagation delays

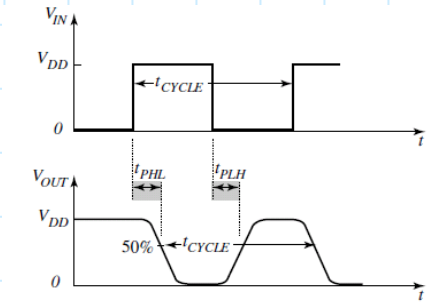
$$t_p = \frac{1}{2}\left(tp_{LH} + tp_{HL}\right) \approx \frac{C_L}{2V_{DD}}\left(\frac{1}{K_p} + \frac{1}{K_n}\right)$$

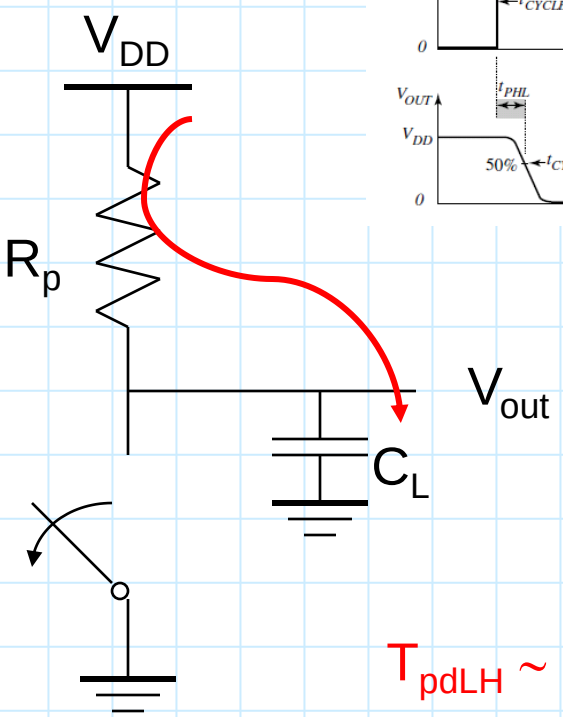


  - Depend on V_{DD}, C_L and K of transistors
    - Lower delay if high V_{DD}
    - Higher delay for high C_L
    - Lower delay if high K
  - t_{pLH} and t_{pHL} can be equal, adjusting the NMOS and PMOS transistors size
  - CMOS is now very fast, with similar delays to TTL
    - High Speed CMOS Subfamilies

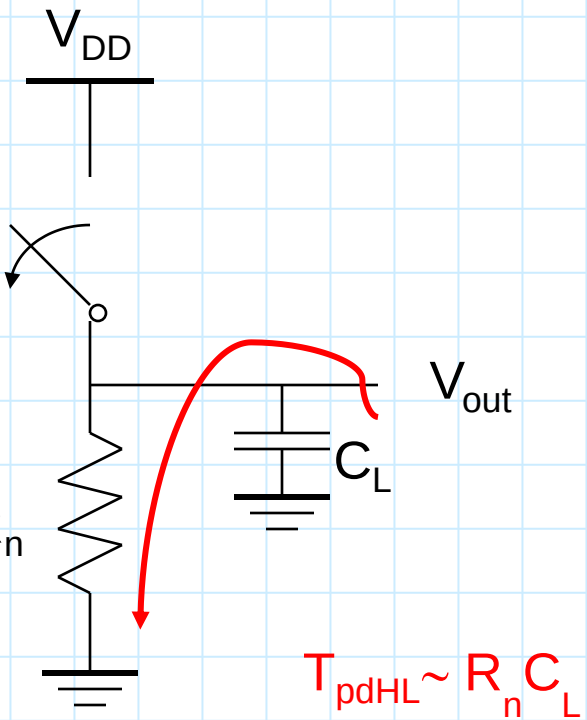
- Product Propagation Delay * Power consumption (PDP): t_p*P → pJ, rather low due to low consumption, although there is a small increase because propagation delays

RC model for propagation delay





$T_{pdLH} \sim R_p C_L$



$T_{pdHL} \sim R_n C_L$

- The delays are given by the charging time of C_L through R_p, and by the discharging time of C_L through R_n)

4.6 CMOS subfamilies

- CD 4XXX : original family
  - 4XXXA: conventional
  - 4XXXB: with output buffer
- 74CXXX: TTL functionally CMOS compatible (pins and functions), but not electrically
- 74HCXXX: high speed CMOS
- 74HCTXXX: high speed CMOS with TTL compatible inputs
- 74ACXXX: Advanced high speed CMOS
- 74ACTXXX: Advanced high speed CMOS with TTL compatible inputs
- 74FCTXXX: Fast CMOS, TTL compatible
- BCT: BiCMOS (Bipolar-CMOS)
- ABT: Advanced BiCMOS
- LVC, ALVC: Low Voltage CMOS

4.6 CMOS subfamilies (2)

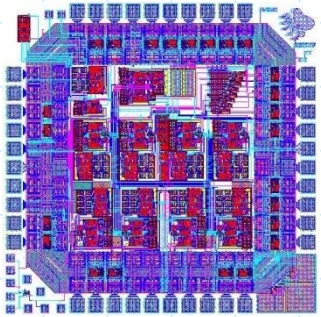
- The HC, AC and BCT subfamilies:
  - Have higher output current than standard CMOS
  - Are faster
  - The logic levels are not as extreme
  - More restricted supply voltage (between 2V and 6V)
- The HCT, ACT and FCT subfamilies:
  - Have TTL compatible inputs and CMOS outputs
  - Have a voltage supply of +5 V, as TTL
- LVC and ALVC subfamilies:
  - Work with V_{DD} less or equal to 3.3V (2.5, 1.8, 1.5,..)
  - Low-power applications

4.6 CMOS subfamilies (2)

- Example: 54/74HC00 (4 2-input NAND gates)
  - 54HC: military version (it works between -40 º C to +85 º C)
  - 74HC: commercial version (it works between -55 º C to +125 º C)
- VDD between 2V and 6V (typical = +5V)
  - V_{IHmin} = 3.15V, V_{ILmax} = 1.35V
  - V_{OHmin} = 3.84V, V_{OLmax} = 0.33V
  - I_{IHmax} = 1μA, I_{ILmax} = -1μA
  - I_{OHmax} = -4mA, I_{IHmax} = 4mA
  - $I_{CC(typ)}$ = 2 μA (average static current consumption)
  - $T_{pd(typ)}$ = 9 ns (average delay)
  - C_{pd} (gate capacity, without load) = 22pF
  - Comparing with standard CMOS:
    - Less extreme output voltage levels
    - Lower noise margin
    - Higher output currents
    - More speed

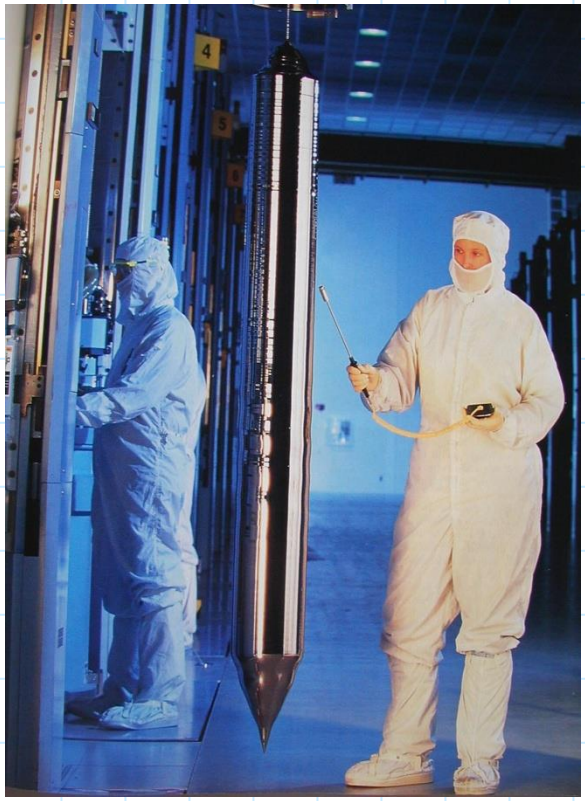
4.7 VLSI design foundations

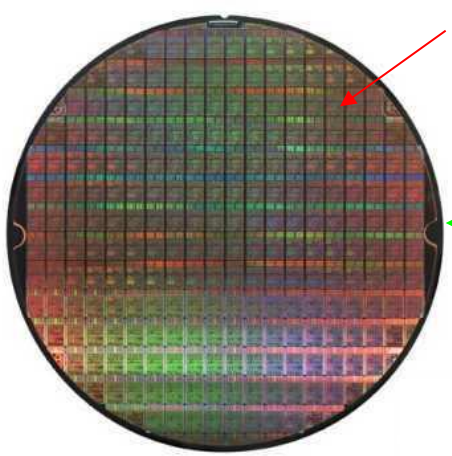
- Manufacturing Process:
  - CMOS transistors are manufactured in thin silicon wafers
  - Photo-lithographic process:
    - Sequence of photographic and chemical steps
    - At each step, different materials are deposited or printed
  - In each step, different materials are settled or engraved



4.7.1 Manufacturing Process

- Chip manufacturing in wafers:



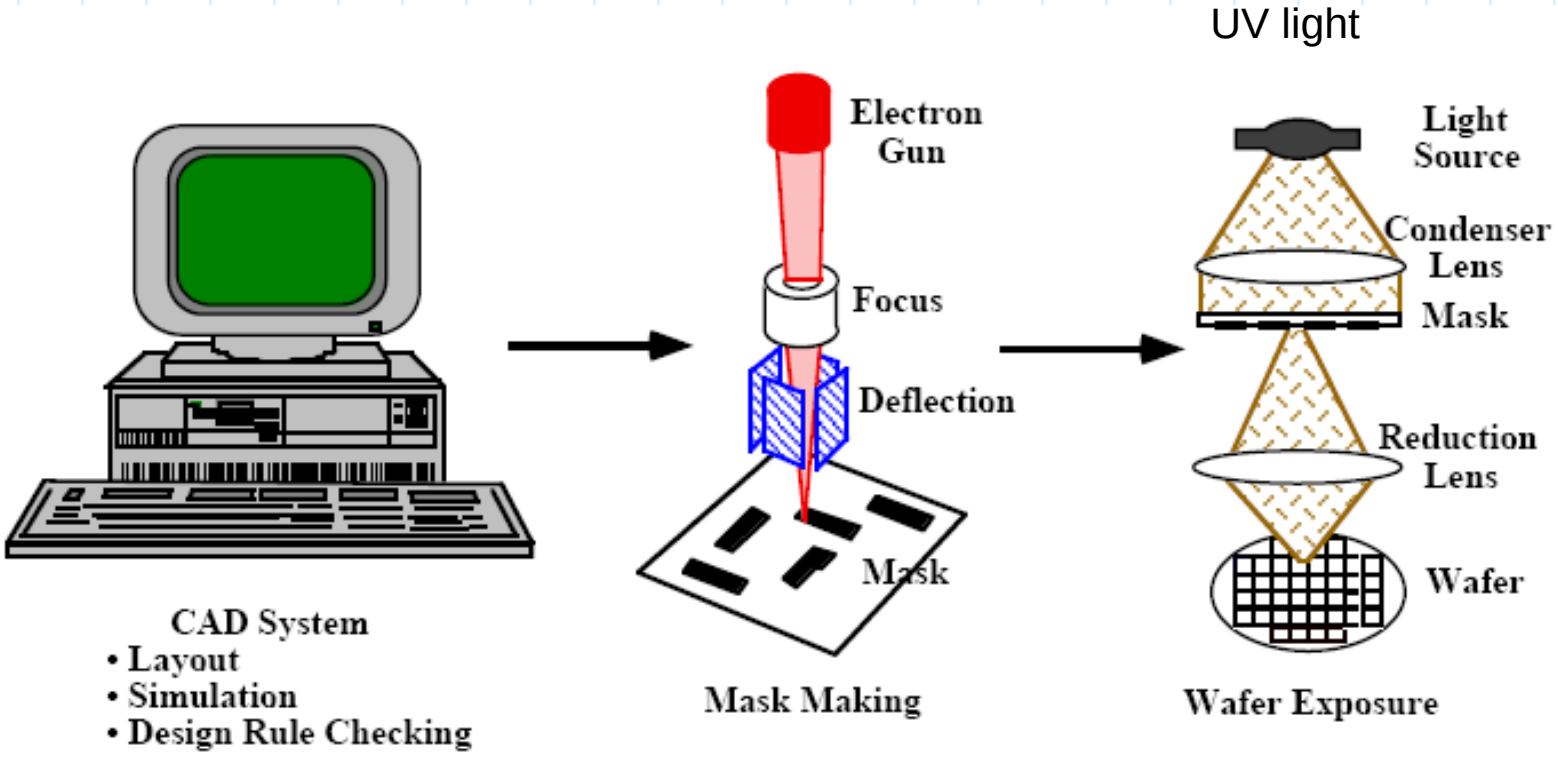


Diameter: 75-300 mm

Thickness: ~1mm

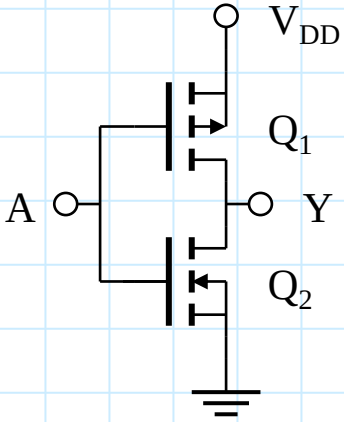
4.7.1 Manufacturing Process

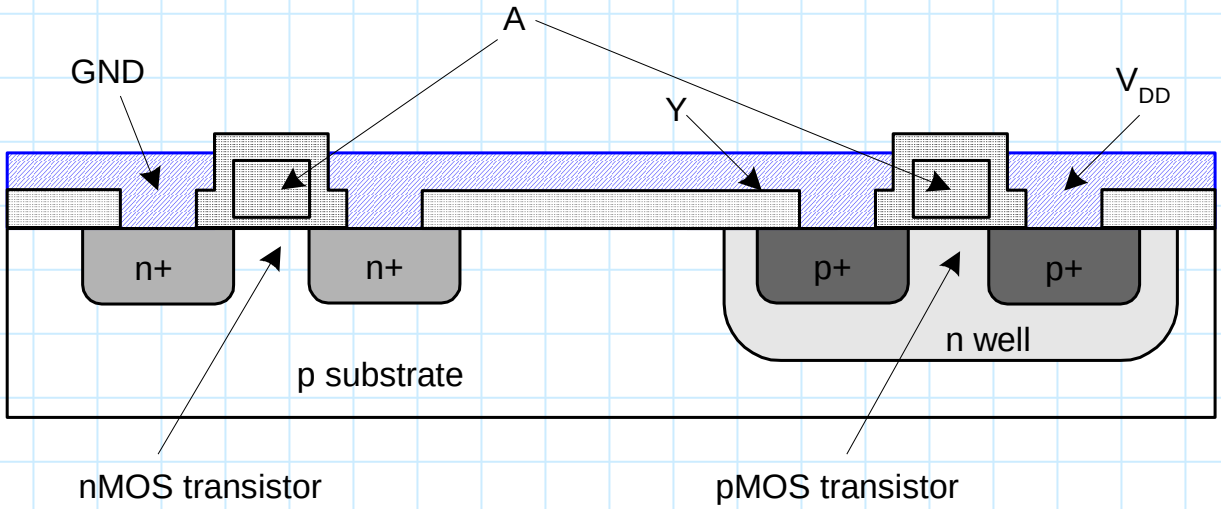
- CAD design→ masks→photolithography



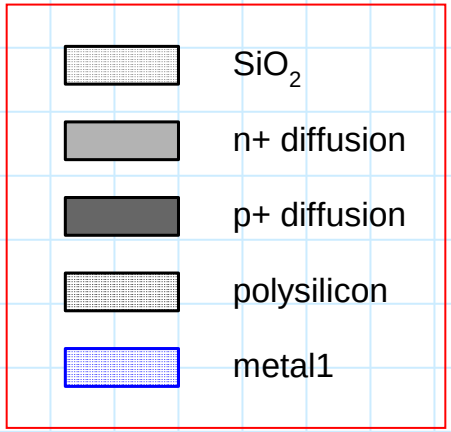
4.7.2 Cells layout: layers

- CMOS inverter on the wafer. Layers of materials (1):
  - Cross section of the inverter
  - P-substrate typically used for nMOS transistors
  - Requires n-well as a substrate of pMOS transistors



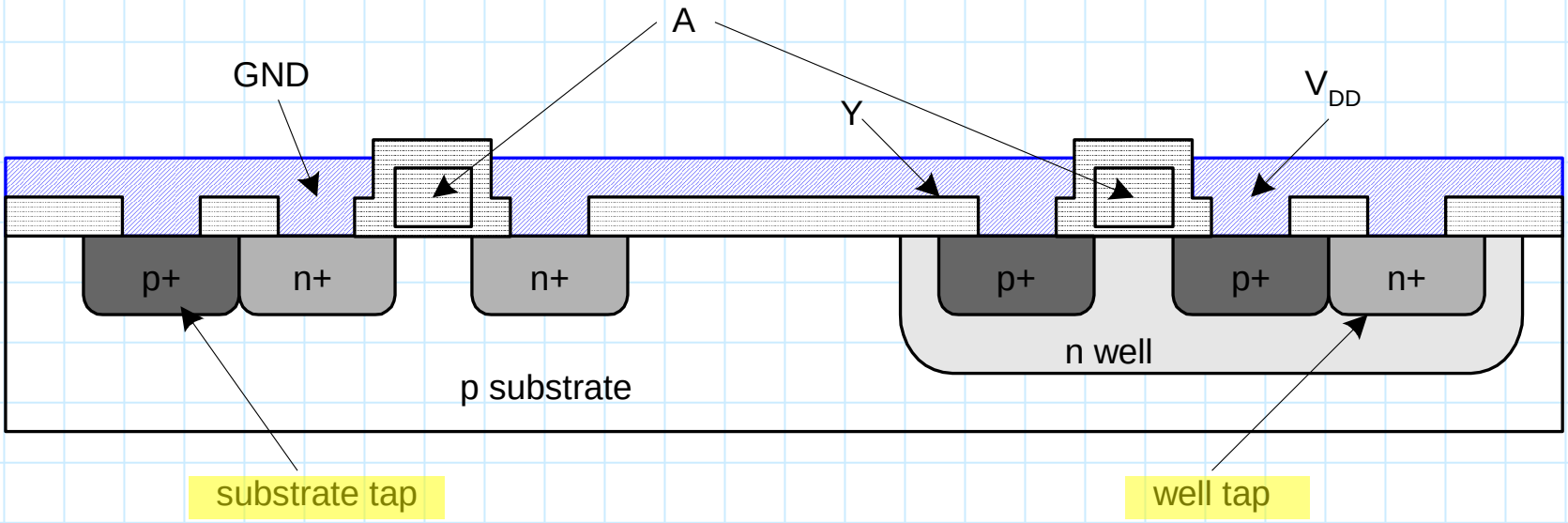


Layers



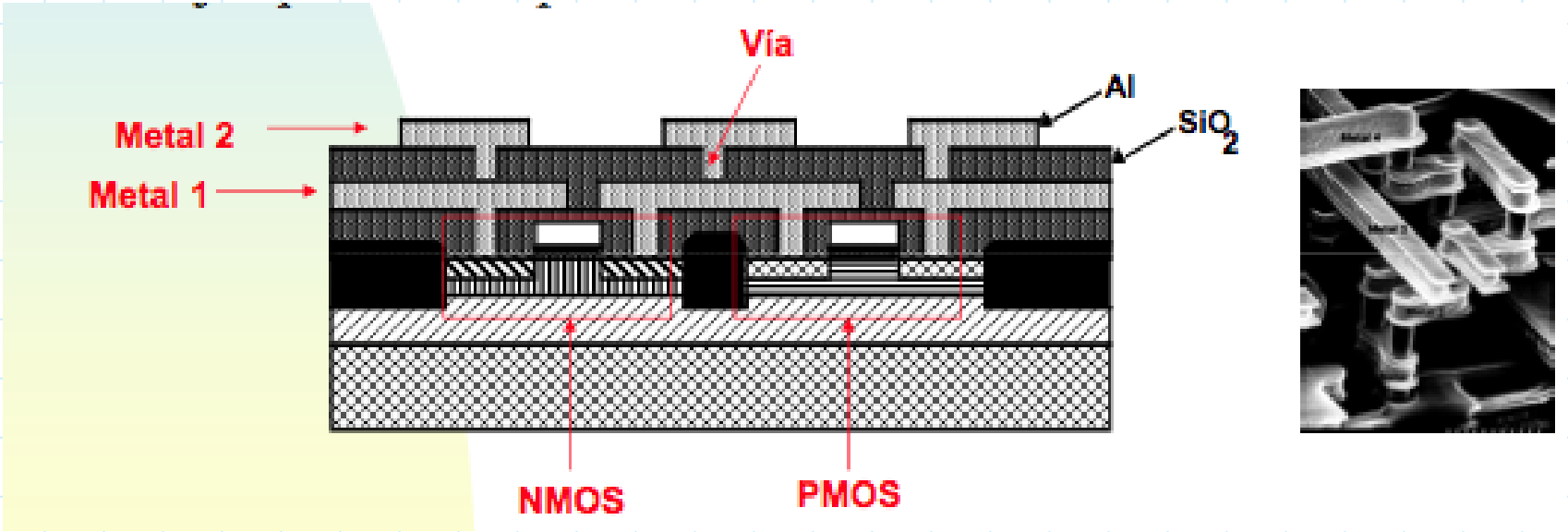
4.7.2 Cells layout: layers

- CMOS inverter on the wafer. Layers of materials (2):
  - Well and substrate contacts
    - The substrate must be connected to GND and the n-well to VDD
    - Contacts (taps) are made with heavily doped Si in substrate and the n-well



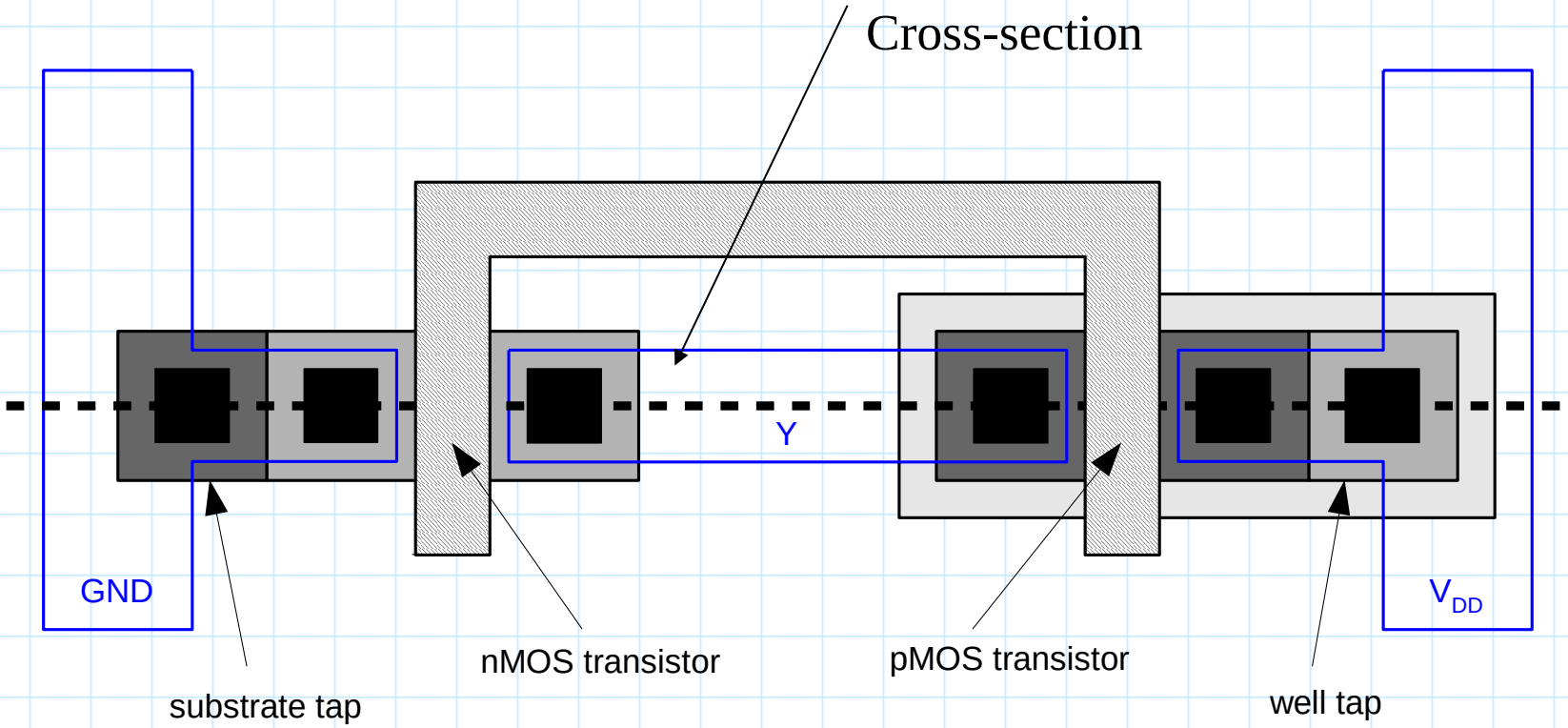
4.7.2 Cells layout: layers

- Normally, there are several metal layers:
  - Interconnections
  - V_{DD}, GND
  - Clock
- Example with 2 metal layers



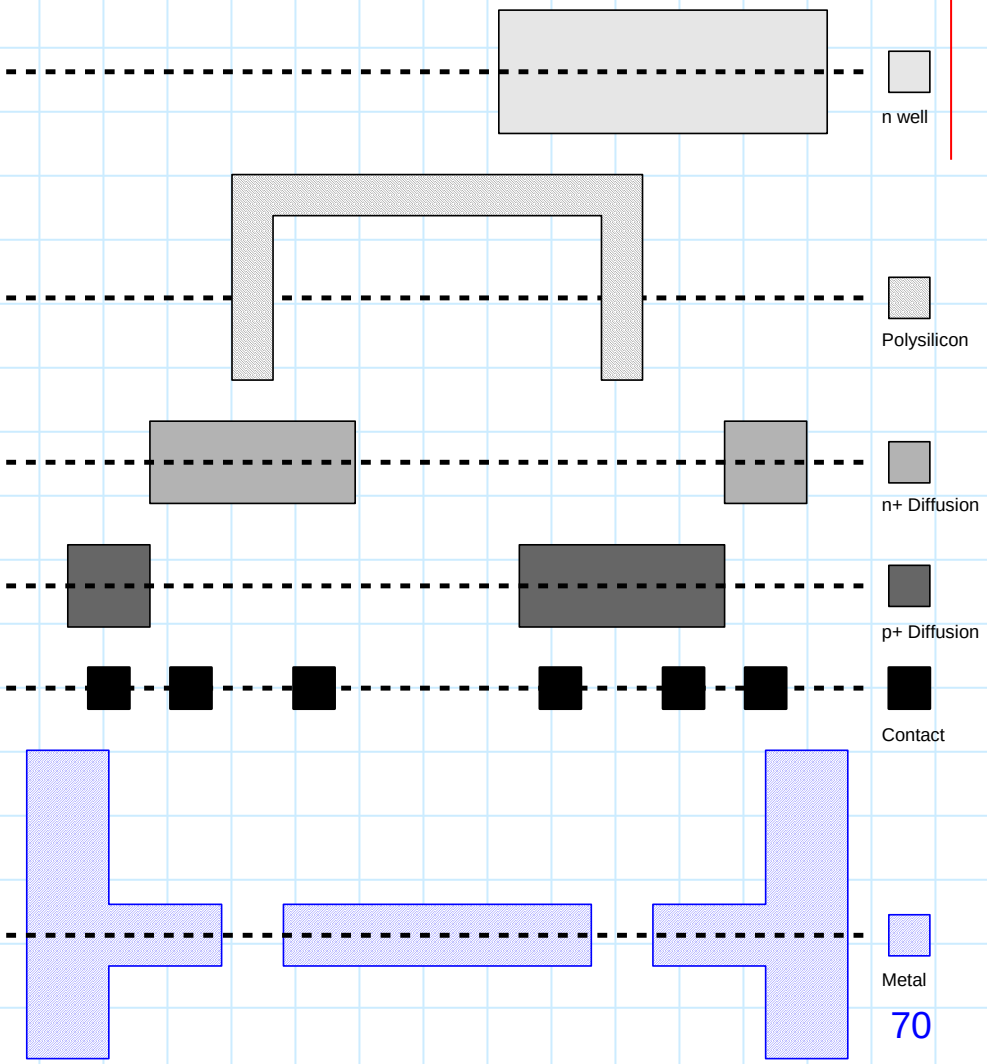
4.7.2 Cells layout: masks

- CMOS inverter. Masks
  - Transistors and connections are defined by masks
  - Top view:



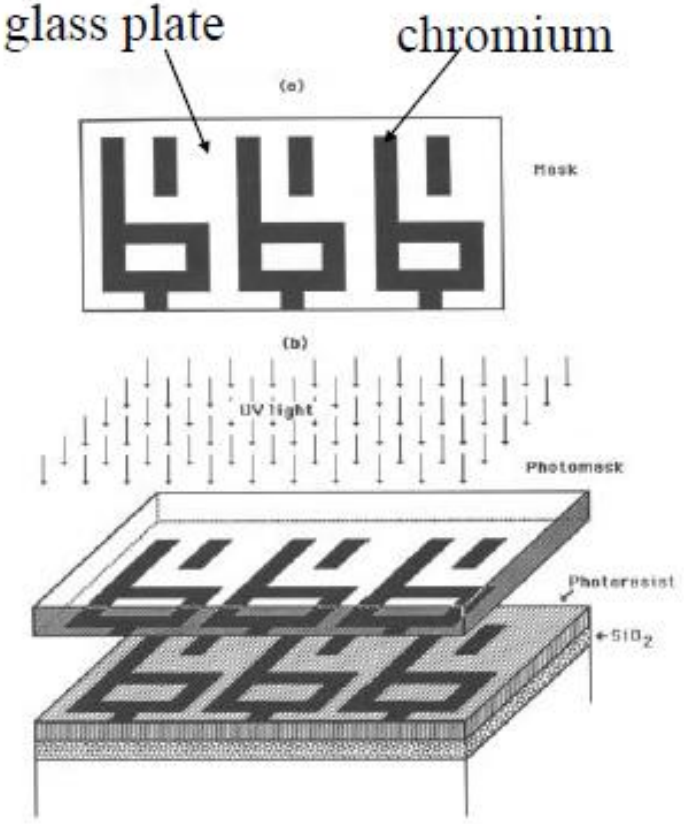
4.7.2 Cells layout: masks

- Example: 6 masks
- n-well
- Polysilicon
- n+ diffusion
- p+ diffusion
- Contact
- Metal



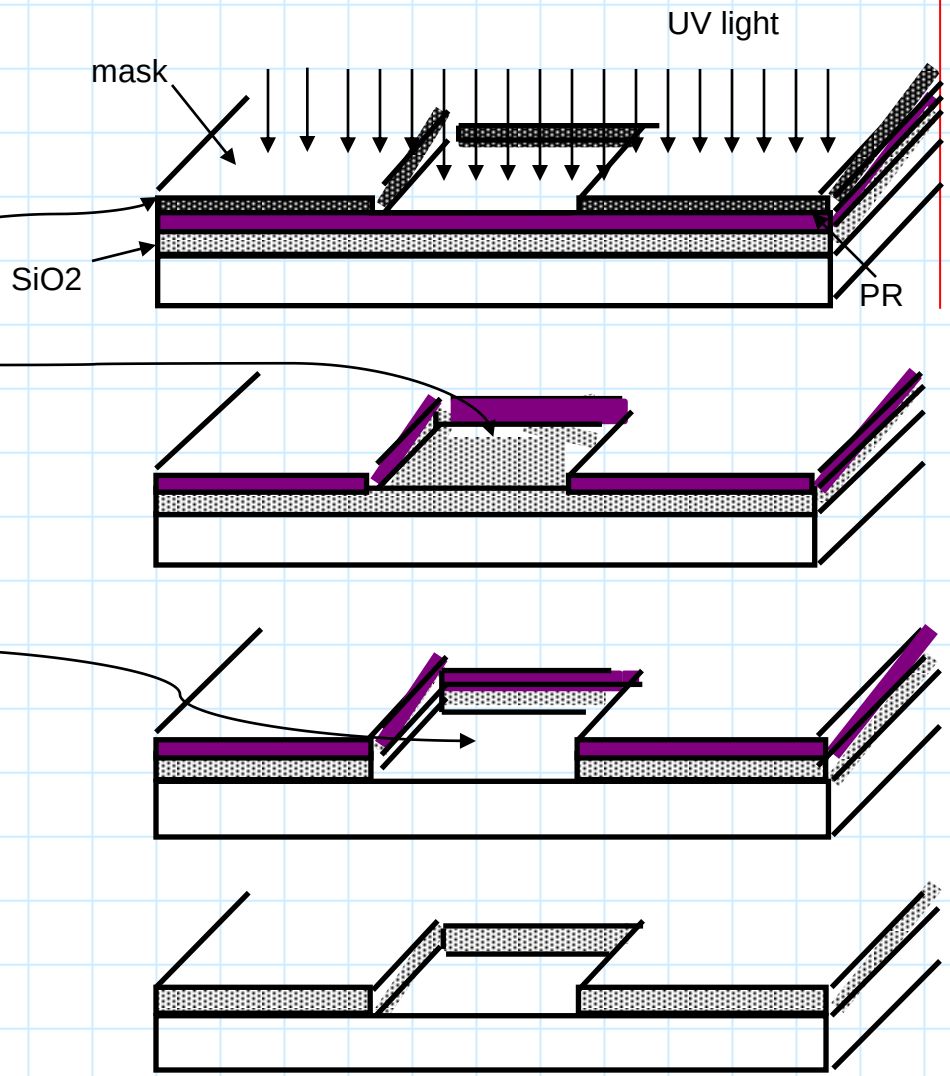
4.7.2 Photolitography

- Masks are projected over the wafer
- The parts on shadow are eliminated (Engrave)
- In the eliminated parts materials are settled (Place)

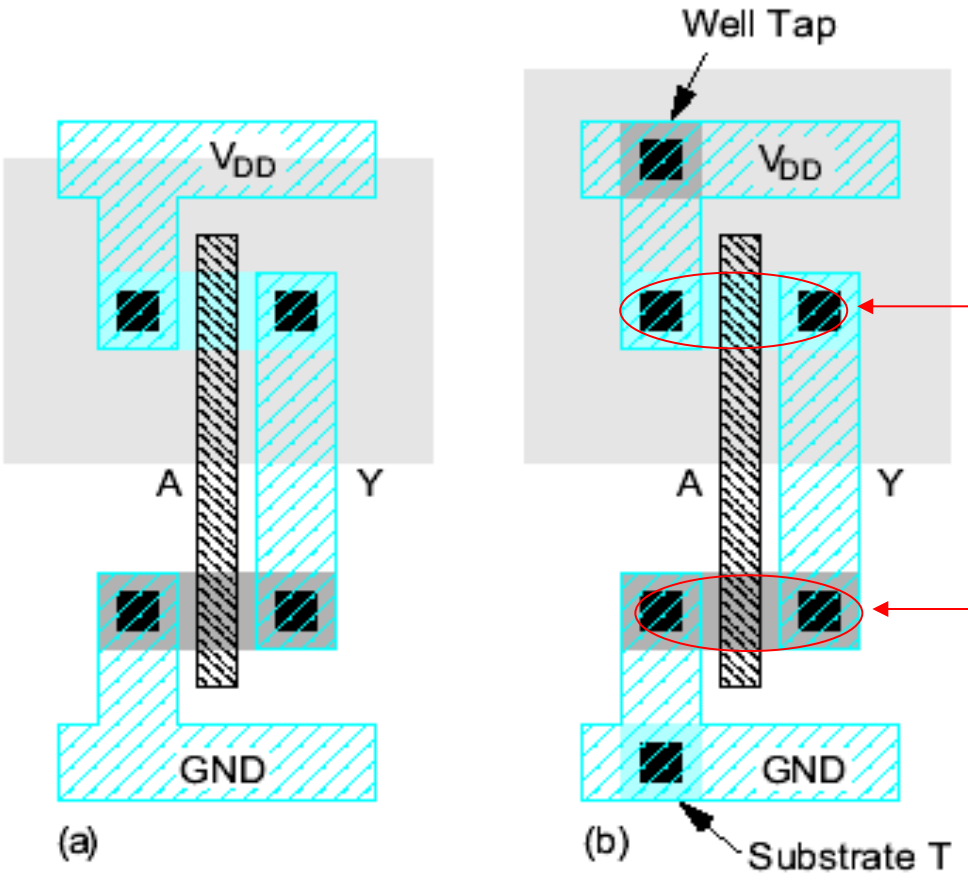


Patterning - Photolithography

1. Oxidation
2. Photoresist (PR) coating
3. Stepper exposure
4. Photoresist development and bake
5. Acid etching
   - Unexposed (negative PR)
   - Exposed (positive PR)
6. Spin, rinse, and dry
7. Processing step
   - Ion implantation
   - Plasma etching
   - Metal deposition
8. Photoresist removal (ashing)



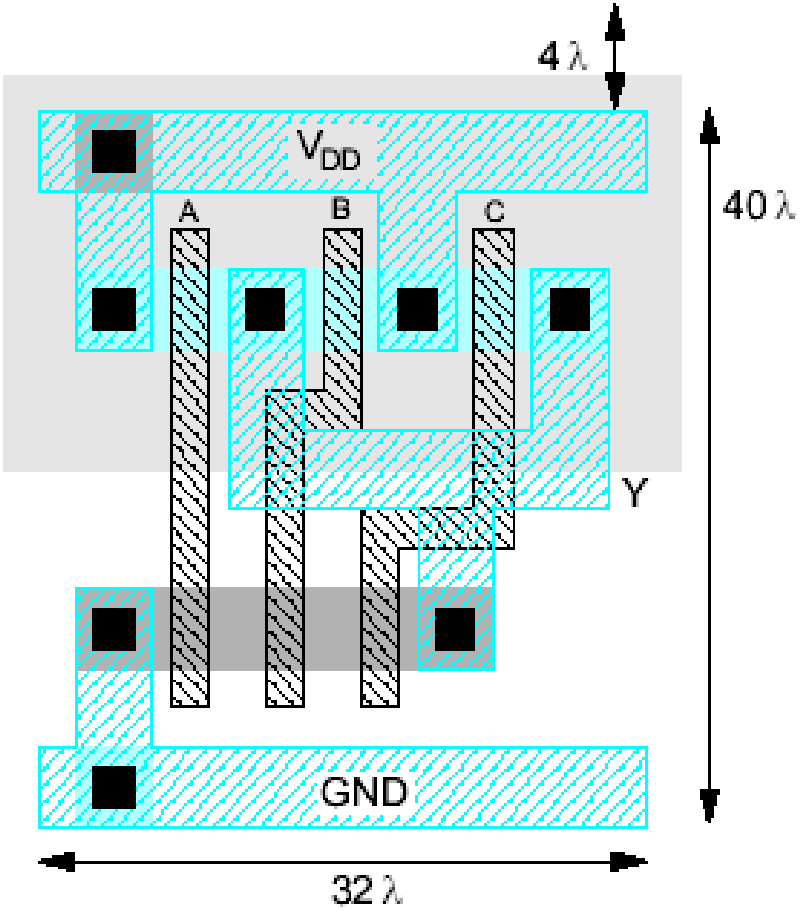
4.7.2 Cells layout: Inverter layout



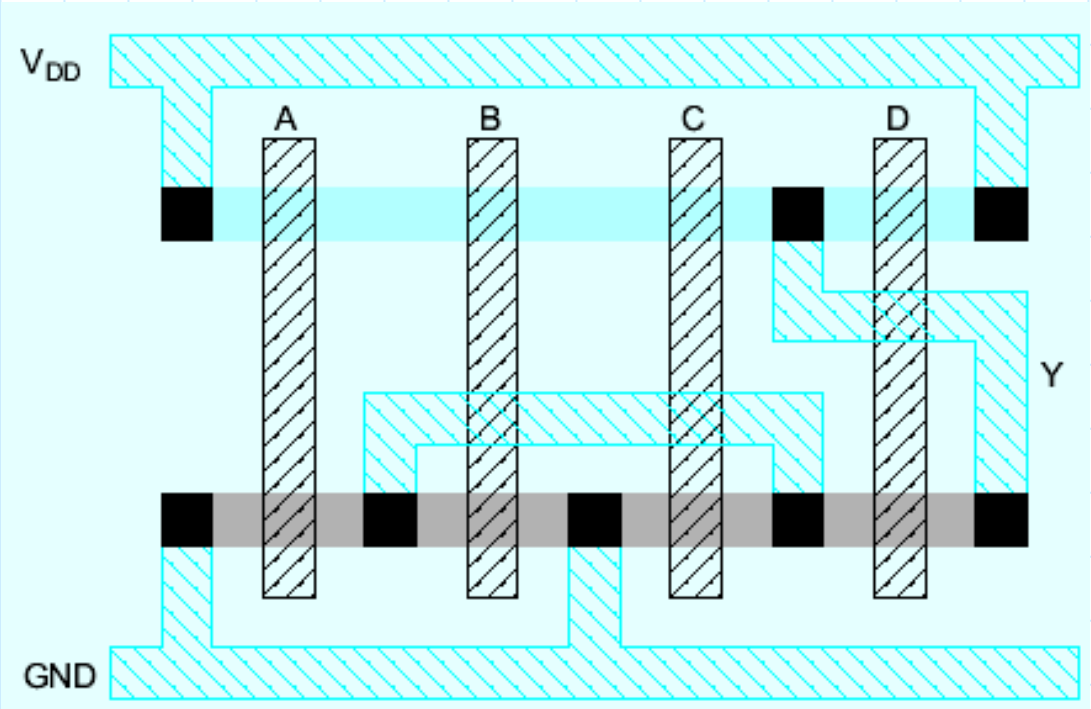
PMOS Transistor:
Poly-P^+diffusion cross

NMOS Transistor :
Poly-N^+diffusion cross

4.7.2 Cells layout: 3 input NAND

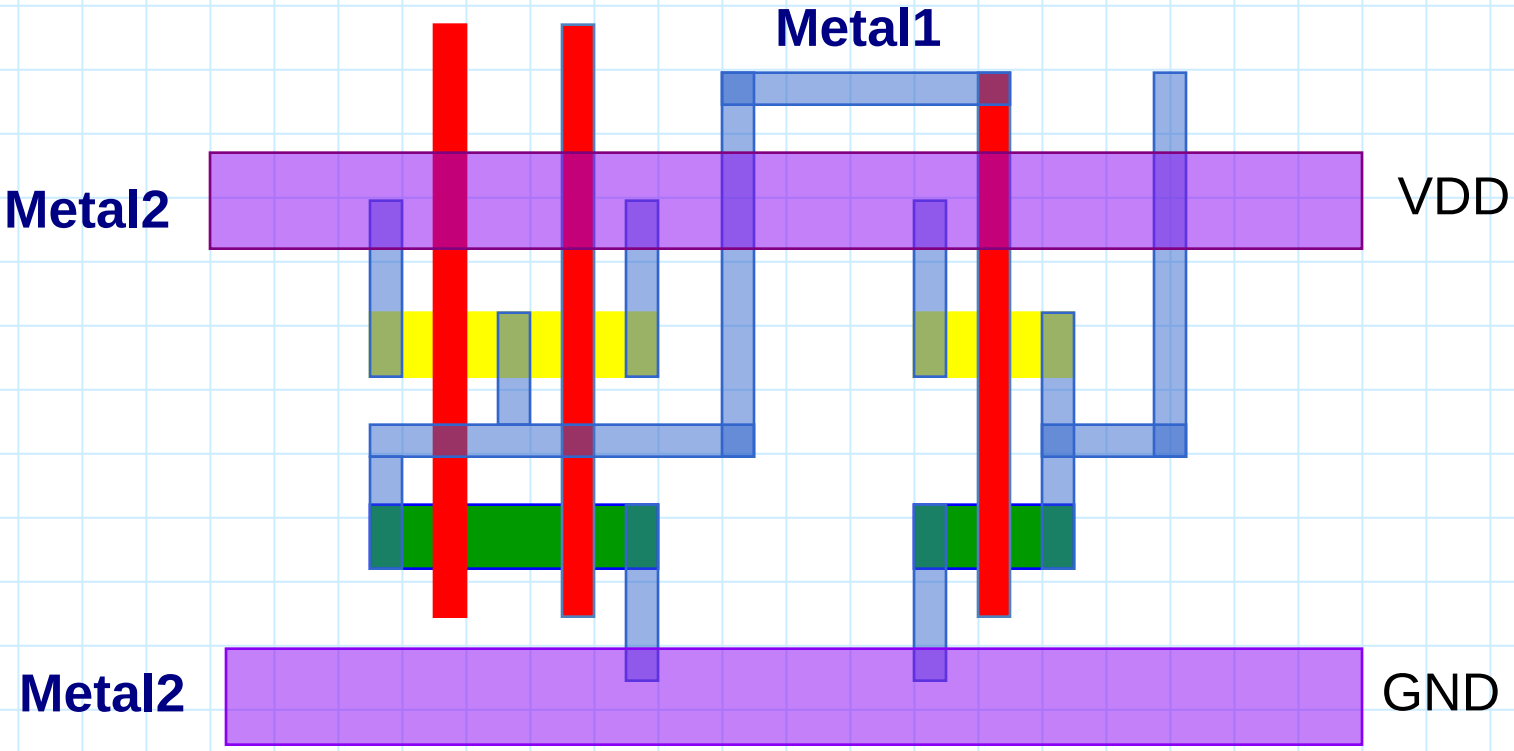


4.7.2 Cells layout



$$Y = \overline{(A + B + C).D}$$

5.7.2 Cells layout: Exercise

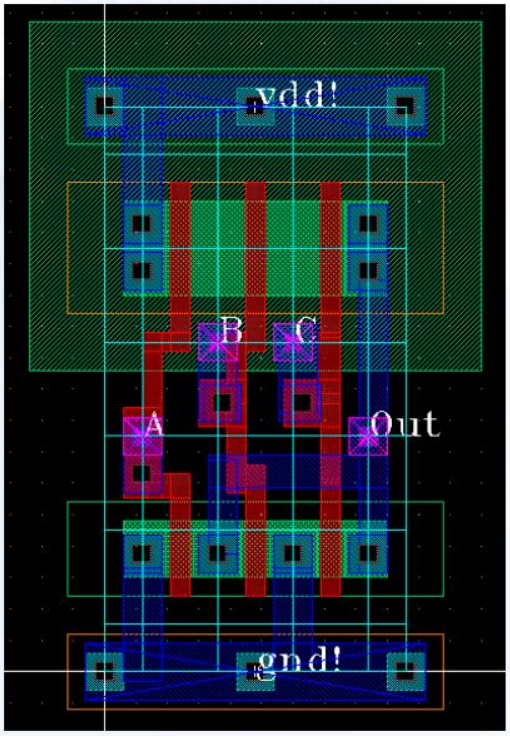


- Which function implements this layout?

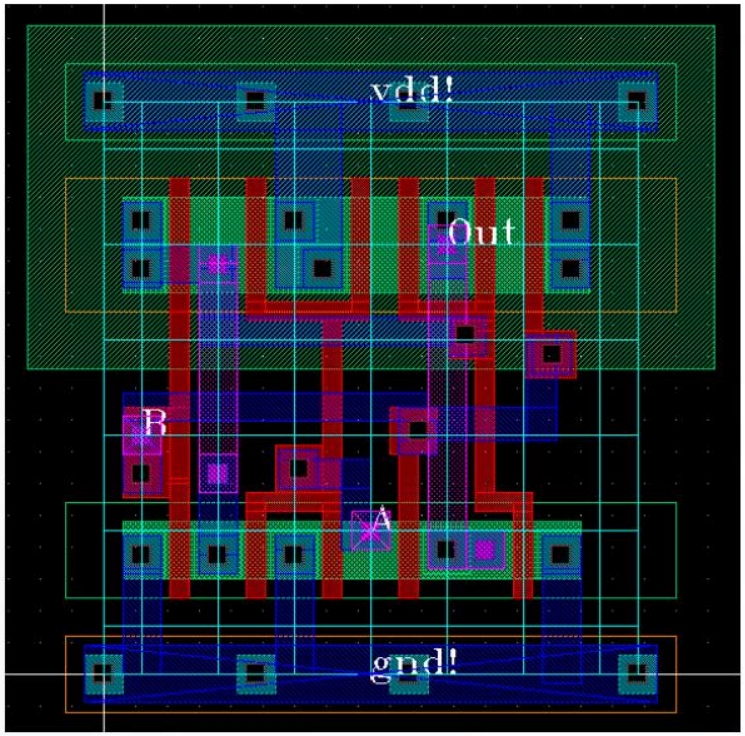
4.7.3 Design flow with standard cells

- Layouts of simple circuits
  - Logic gates, FF, full-adder, multiplexers, cell input / output,
- Cells stored in cell libraries
- Different sizes and output currents
- Predesigned and verified (area, delay, power consumption)
- Deposited on the chip to form more complex designs
  - Computer Aided Design (CAD): place and route
  - Reusability
  - Modularity
- Automatic design of macro-cells (macro-modules) memory modules, multipliers, ...

Standard Cells



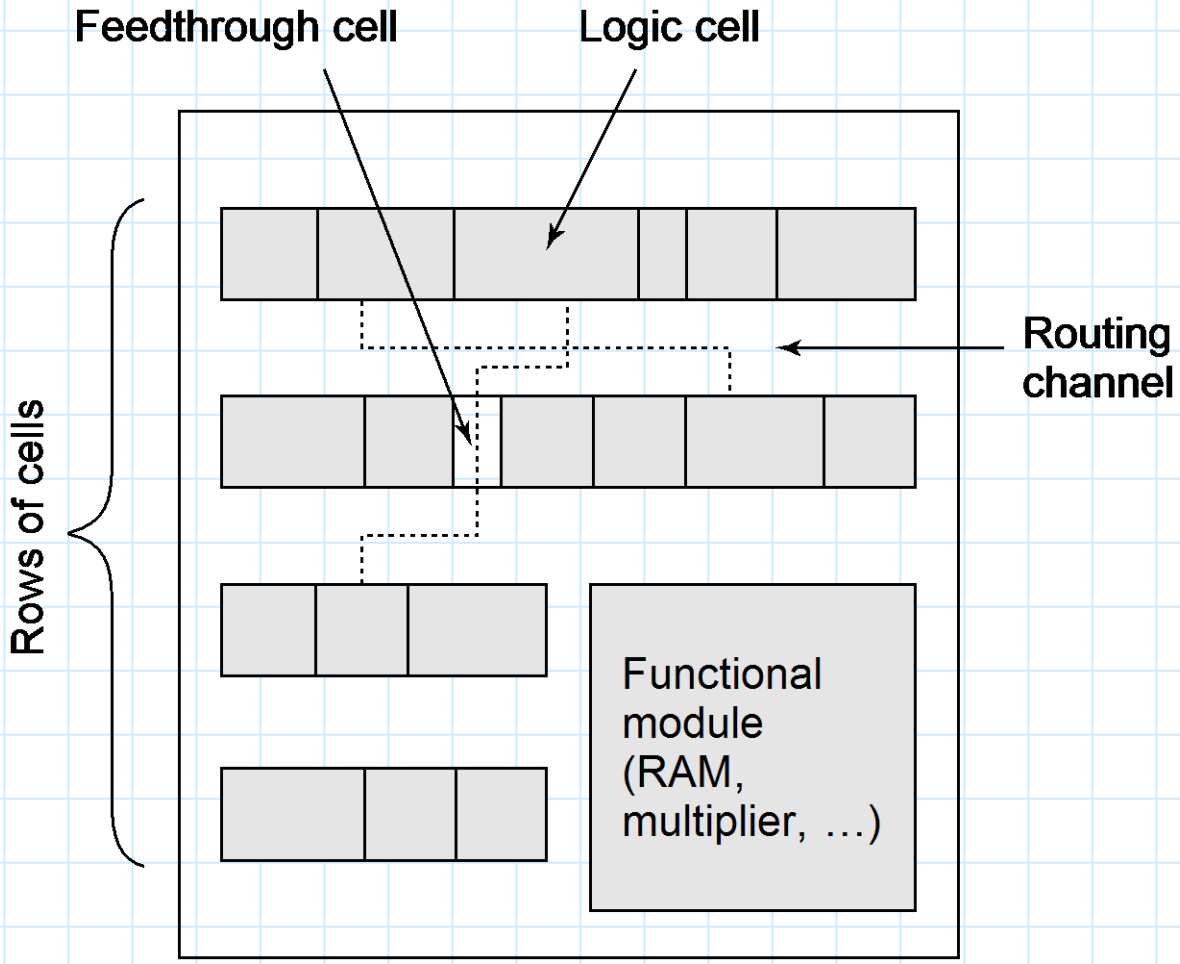
NOR-3



XOR-2

4.7.3 Design flow with estándar cells

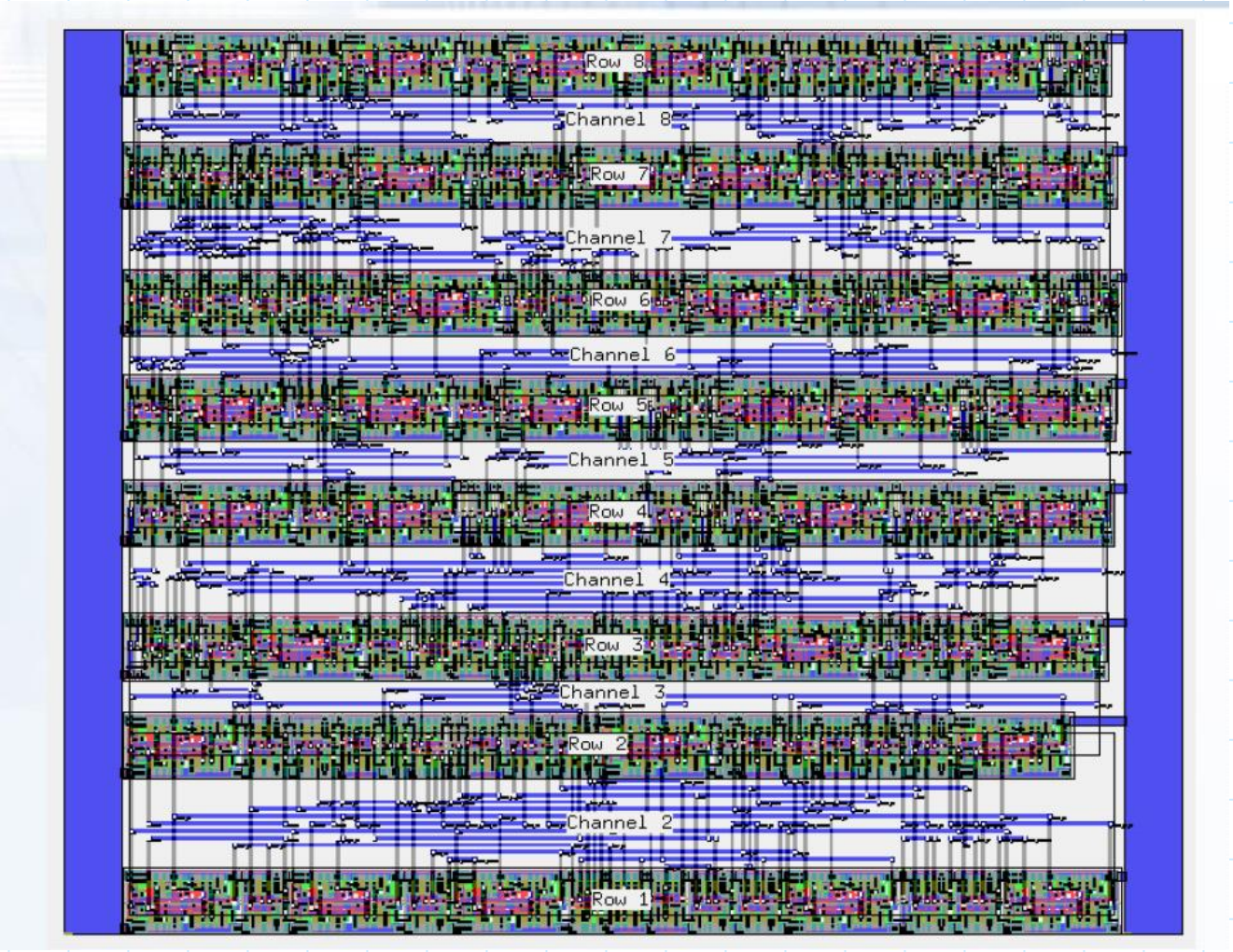
- Provision of standard cells on the chip:



Cells arranged in rows, with the same height and variable width
V_{DD} and GND shared

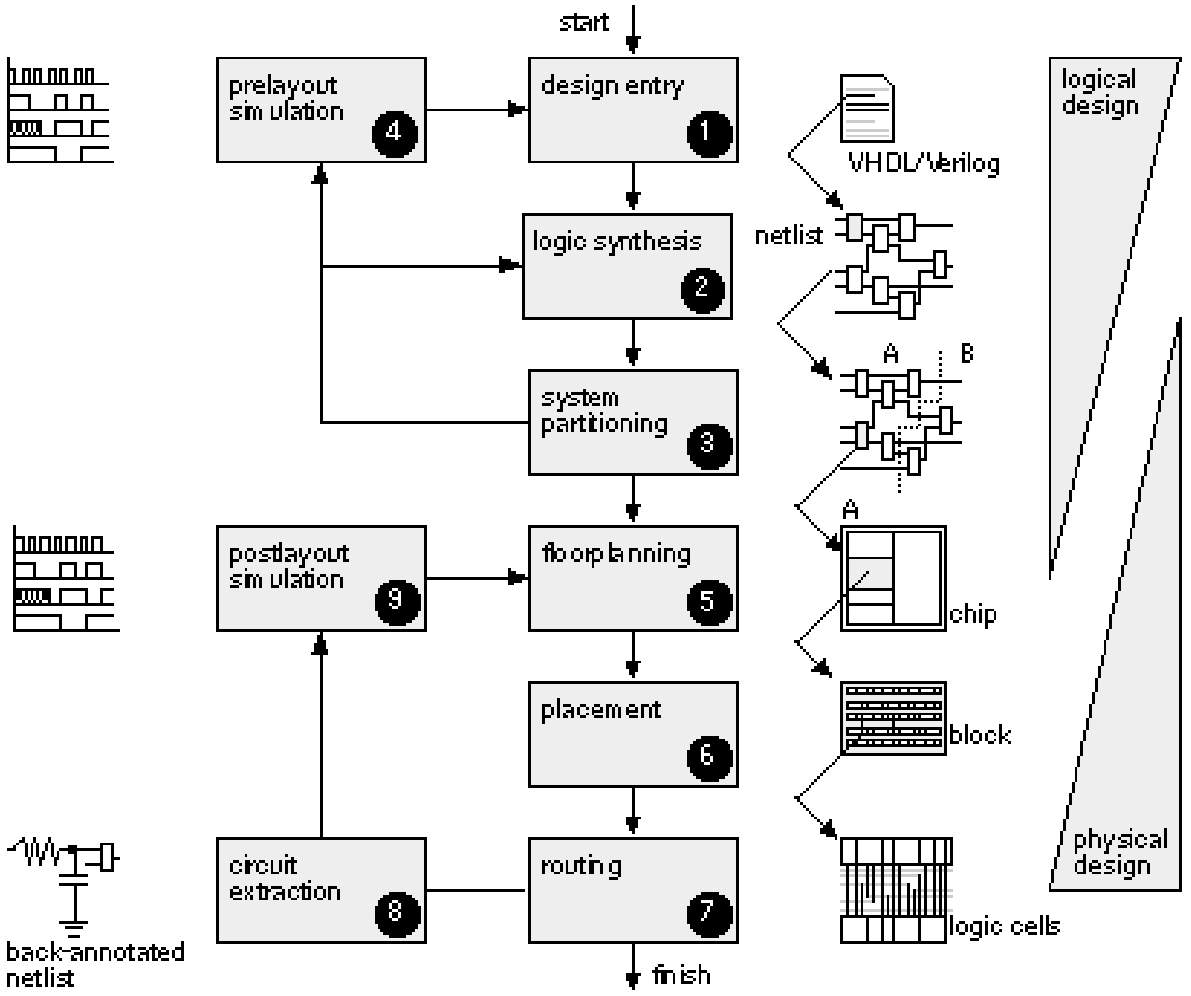
The interconnecting channels are reduced by increasing the presence of more metallization layers

Standard Cell Layout



4.7.3 Design flow with estándar cells

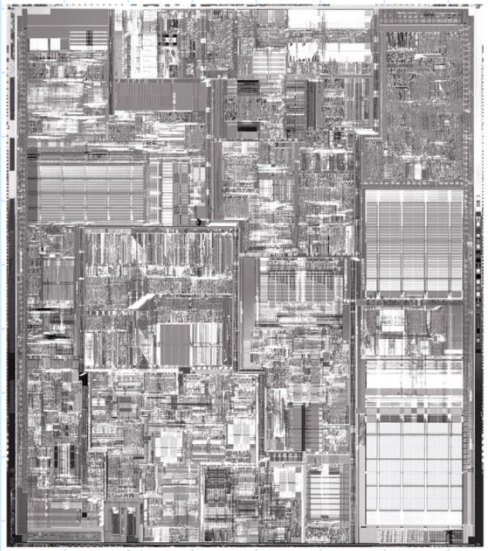
- Design flow based on standard cells



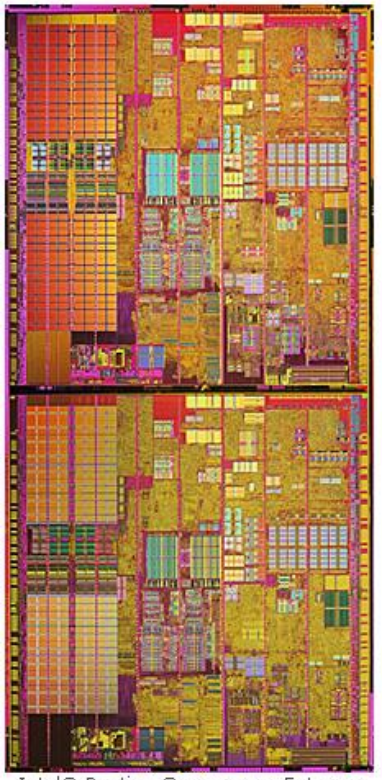
4.7.3 Design flow with estándar cells

- Steps in the flowchart
  - 0. System specification using a natural or formal language
  - 1. Initial description of the design. Behavioral description using HDL languages -Hardware Description Languages-(Verilog, VHDL).
  - 2. Logic synthesis. It automatically generates the netlist-description of the standard cells needed and the connections between them.
  - 3. System partition. Divides a large system into blocks.
  - 4. Pre-layout simulation. Verification of correct operation. Approximate temporal verification based on the cells delays.
  - 5 .Floor planning. Organize (place) blocks in the chip netlist.
  - 6. Placement. Deciding the location of cells within a block.
  - 7.Routing. Make connections between cells and block
  - 8.Extraction. Determine the resistance and capacitance of interconnecti ons.
  - 9. Post-layout simulation. Verification of timing requirements with the R and C values of the actual interconnections.

4.7.3 Design flow with estándar cells: examples



Pentium 4



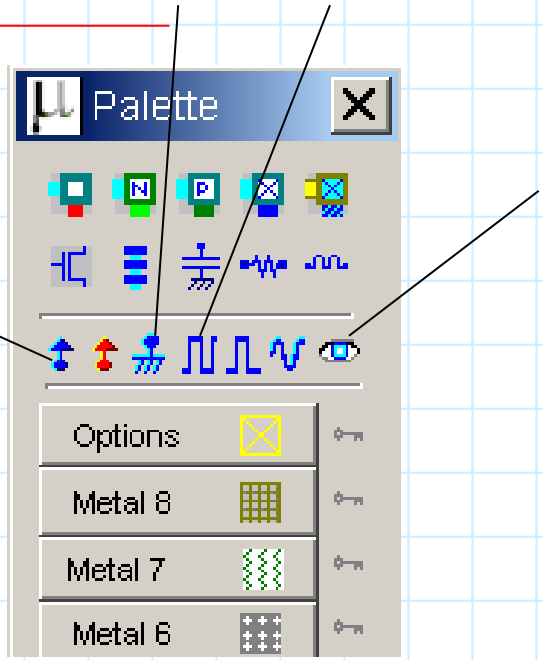
Intel® Pentium® processor Extreme Edition processor die

Dual-Core Processors

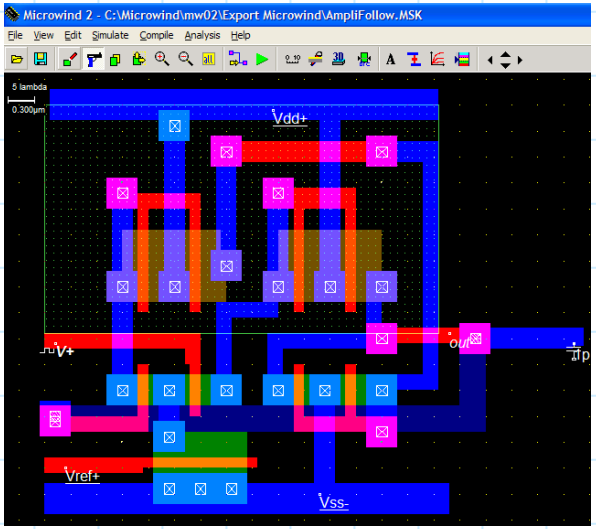
4.7.4 Full-custom design

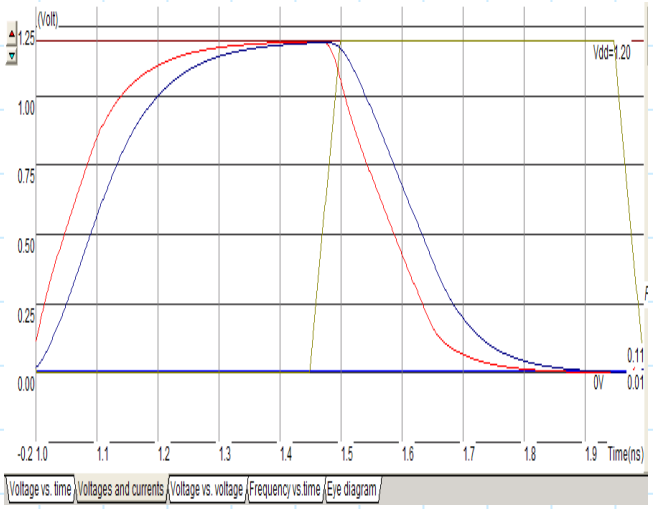
- Some cells or parts of the design require optimal features of the area, consumption or speed
  - Clock circuits (PLL, drivers, ...)
  - High-speed arithmetic circuits (floating point, ...)
  - Input / Output Drivers
  - ...
- For these cases, a full-custom design is used
  - Mask-level design (geometric)
  - More optimal design than based on Standard Cells (semi-custom)
  - For critical parts of small size
  - CAD Tools:
    - Graphical layout editor
    - Primitives: transistors, contacts, wires, ports
    - Automatic verification

4.7.4 Full-custom design



Layout editor

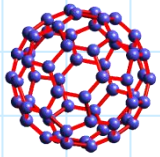


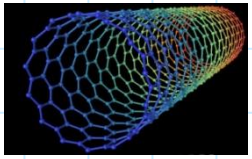


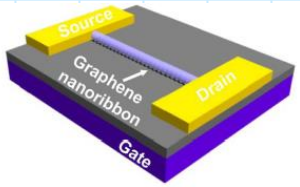
Post-Layout Simulation

4.7.5 VLSI design: current and future trends

- Historical evolution:
  - 4004: 10 μm technology
  - ....
  - Pentium 4: 0.13 μm technology, 90nm (submicron)
  - Dual-core, 4-cores, 8 cores, ... (thousands of millions of transistors)
- Current technologies: 90nm, 65nm, 45nm, 32nm, 22 n
- Current trends: technological and design **improvements in CMOS**
  - (www.intel.com /technology, ITRS 09)
  - New materials
  - New designs
- Future Trends: Research in **Nanotechnology** (ITRS 09)
  - Nanotubes, nanowires, graphene, spintronics, SET, molecular, quantum







4.7.4 VLSI design: New trends of today and future

Year	2009	2012	2015	2018	2021
Feature size (nm)	34	24	17	12	8.4
L_{gate} (nm)	20	14	10	7	5
V_{DD} (V)	1.0	0.9	0.8	0.7	0.65
Billions of transistors/die	1.5	3.1	6.2	12.4	24.7
Wiring levels	12	12	13	14	15
Maximum power (W)	198	198	198	198	198
DRAM capacity (Gb)	2	4	8	16	32
Flash capacity (Gb)	16	32	64	128	256

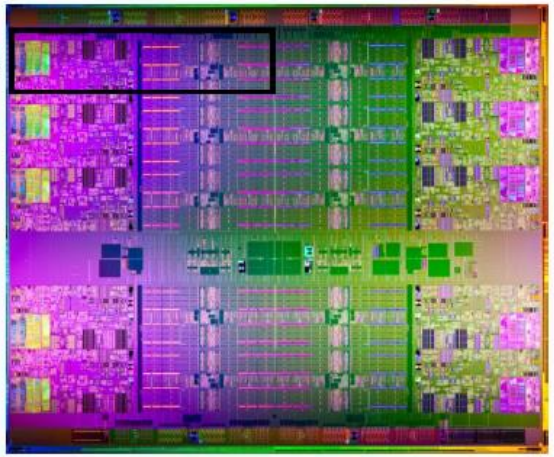
4.7.4 VLSI design: New trends of today and future

- *Multicore era*
  - Simpler Core microprocessors
  - Less voltage and frequency
  - More performance as there are more cores/chip

e.g. Intel 10 Core Xeon Westmere-EX

- 1.73-2.66 GHz (vs. previous Xeons at 4 Ghz)

1 core →



Summary

- In the first part of the unit we have introduced the structure and operation of CMOS basic gates (NOT, NAND, NOR, ...) .
- After that, we have addressed the design of generic combinational circuits using the complementary CMOS logic methodology.
- Then, the transmission gates have been introduced, studying their use in several logic circuits, such as multiplexers and flip-flops.
- We have also addressed the special CMOS outputs (open drain and tri-state), which allow for bus connections.
- We have also described the main characteristic parameters of the CMOS family and subfamilies, discussing the high-speed and low voltage CMOS subfamilies.
- Subsequently, we have seen a summary of the fundamentals of VLSI design and manufacturing.
- Finally, we have commented on the current and future trends in the design and manufacture of VLSI chips.