FUNDAMENTALS OF COMPUTER

Practice 3

Design and implementation of decoders and multiplexors

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Once known the concepts of the combinational logic-circuits design and having experimented with logic gates and elementary logical functions, as well as his utilization to generate functions and his later simplification, the student will put in practice the acquired knowledge relative to more complex circuits and of special importance inside the different functional units of the computer. Such circuits are the decoders and the multiplexers.

The ICs with decoders and multiplexors available in market are part of the known MSI (medium scale of integration) circuits. In this laboratory session decoders and multiplexors will be implemented. For that purpose we will use the logical trainer shown below.

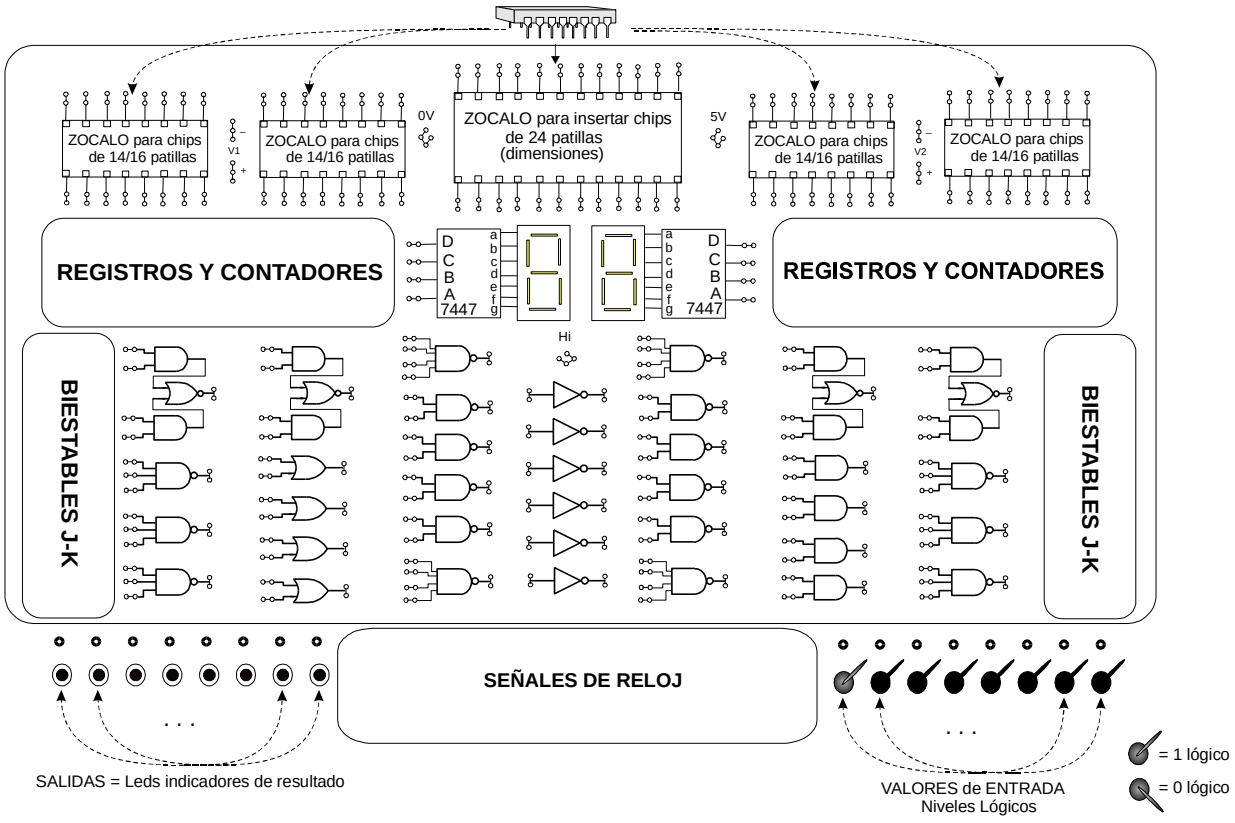

Figure 1: Functional diagram of the trainer.

1. BINARY DECODERS.

In the first part of the lab session the student will put into practice the theoretical knowledge acquired relative to binary decoders. The MSI circuit that will be used is the chip 74139 of 16 pins, The 74149 IC has two independent decoders with 2 inputs and four outputs (low-level activated). Besides it has an enable input (also low-level activated). The enable input is the same for the two decoders. In the datasheets of the manufacturer (at the end of the bulletin), the student will find all the necessary information for the utilization of the 74139 IC. The student must go familiarizing itself with these datasheets in order to be able to interpret any circuit from its specifications.

Warning: The manufacturer uses the same datasheets to describe two different decoders, the 74138 (3-8 decoder with several enable inputs) and the 74139 (two 2-4 Decoders with a <u>common</u> enable input).

Into one of the trainer's sockets a 74139 IC must be plugged.

a) Power the 74139 IC and make the proper wiring to test the first 2-4 decoder. Fulfill table 1 with the valuations and outputs obtained when verifying the functioning of the 2-4 decoder. The obtained values must be the same that the truth table of a 2 to 4 Decoder with enable input.

Inputs			Outputs			
Enable	Selection					
/G	**B**	**A**	**/Y0**	**/Y1**	**/Y2**	**/Y3**
1						
0						
0						
0						
0						

Table 1. Truth table of a 2 to 4 Decoder with enable input

b) **Draw the logic symbol corresponding to the truth table shown in figure 1.**

Warning: Do not forget that all inputs and outputs must have a name. The given name must follow the specifications used in theoretical classes.

Decoder's composition technique is used to obtain decoders with a bigger number of selection inputs. The technique consists of placing several decoders in parallel and by means of additional logic to determine what decoder must be active in every moment..

c) Using the decoder's composition technique a 3 to 8 decoder must be built. It is necessary to use the two 2 to 4 Decoders of the circuit 74139 plus a NOT gate for designing and implementing in the trainer. The logical symbol of the circuit to implement is shown in figure 2. (NOTE: The implemented circuit does not have enable input). Draw a possible implementation in figure 3.

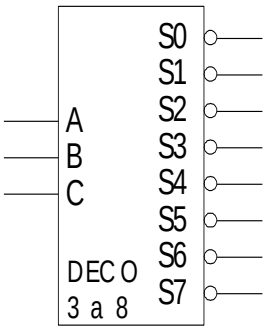

Figure 2. Logic Symbol of a 3 to 8 Decoder

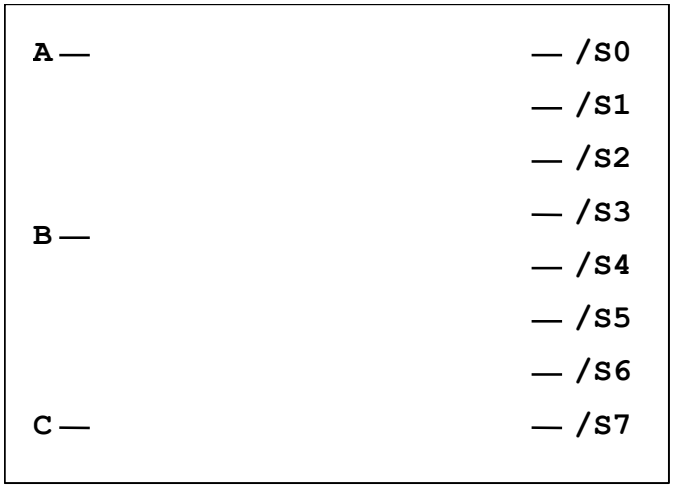

Figure 3. Circuit implementation

DO NOT UNMOUNT THE CIRCUIT (It is used in next section)

d) Verify the correct functioning of the implemented circuit writing its truth table in Table 2.

Inputs	Outputs							
CBA	**/S0**	**/S1**	**/S2**	**/S3**	**/S4**	**/S5**	**/S6**	**/S7**
000								
001								
010								
011								
100								
101								
110								
111								

Table 2. Truth table of a 3 to 8 decoder

e) Modify the 3 to 8 decoder yet implemented in section c in order to get a 3 to 8 decoder **with low-level active enable-input**. Additional gates will be necessary to design the final circuit.

Draw the designed circuit in Figure 5.

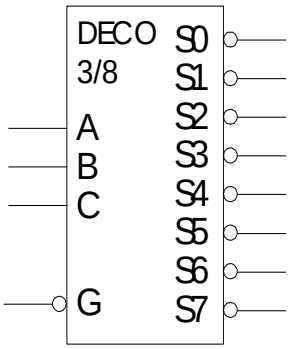

Figure 4. Logic symbol of a 3 to 8 decoder with low-level active enable input

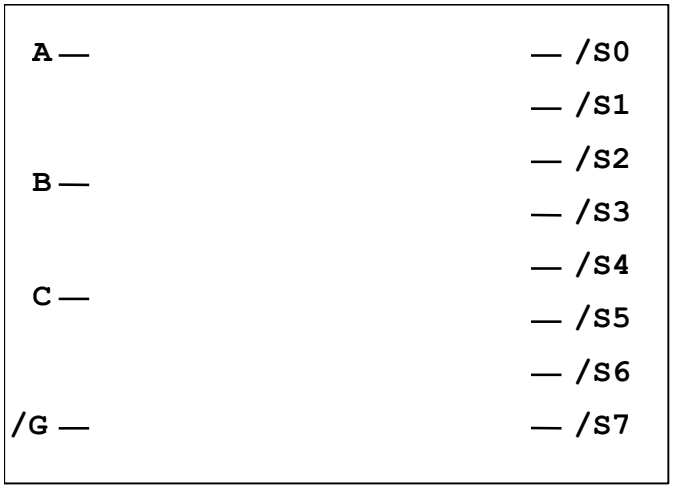

Figure 5. Implemented circuit

f) Verify the correct functioning of the implemented circuit writing its truth table in Table 2.

Inputs		Outputs							
/G	**CBA**	**/S0**	**/S1**	**/S2**	**/S3**	**/S4**	**/S5**	**/S6**	**/S7**
0	000								
0	001								
0	010								
0	011								
0	100								
0	101								
0	110								
0	111								
1	000								
1	001								
1	010								
1	011								
1	100								
1	101								
1	110								
1	111								

Table 3. Truth table of a 3 to 8 decoder with low-level active enable input.

2. MULTIPLEXORS.

A multiplexer is a combinational circuit with 2^n data inputs, n selection inputs and only one output. The selection inputs are used to indicate which data input is connected to the output. The MSI circuit that will be used is the 74153 IC (datasheet at the end of the bulletin). The 74153 IC has two complete multiplexers.
The composition technique also is applied when multiplexors of bigger size than commercial ones are needed.

a) Into one of the trainer's sockets a 74153 IC must be plugged. Using the 74153 IC plus the necessary logical gates a 8 to 1 multiplexor with low-level active enable input must be designed. Draw your design in Figure 7.
Warning: The trainer o**nly has one integrated circuit 74153, for what it will be necessary to implement with logical gates someone of the multiplexers used in the composition.**

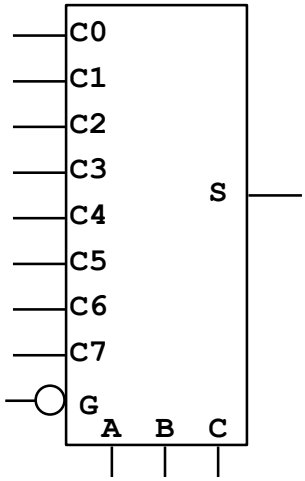

Figure 6. Logic Symbol of a 8 to 1 MUX with low-level active enable input

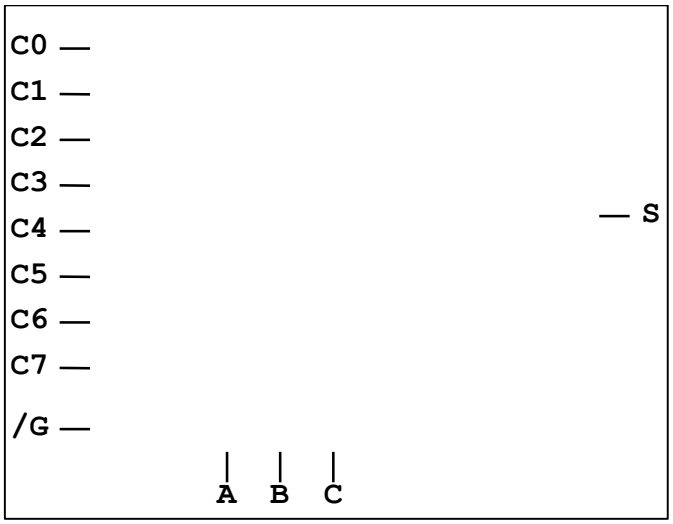

Figure 7. Implemented circuit

VERY IMPORTANT:
The trainer does not have enough switchboards for the 12 inputs (Selection inputs C, B and A, enable input /G and 8 data-inputs).
We will fix data-inputs (C7, C6, C5, C4, C3, C2, C1 y C0) to the fixed values 01110001 respectively. The switches will be used to wire selection-inputs C, B and A and the low-level active enable input)

Verify that the circuit's functioning is the right one. Fulfill the following table.

Inputs	Output
ABC	f
000	
001	
010	
011	
100	
101	
110	
111	