4.5 Characteristic parameters (related to standard CMOS)

- Supply voltage:
  - V_{DD} typically between 3V and 15V in SSI and MSI chips
  - GND (V_{SS}) = 0 V
  - In 1980's, V_{DD} = 5V
  - V_{DD} has been reducing over the years in VLSI chips:
    - High V_{DD} may affect small current transistors of nowadays
    - A low V_{DD} decreases power consumption
    - V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, ...
    - VLSI chips have normally with 2 voltage supplies:
      - Logic "Core": low V_{DD} (e.g. 1V) → Low power
        I/O cells: high V_{DD} (e.g. 2.5V) → High current

4.5 CMOS characteristic parameters (2)

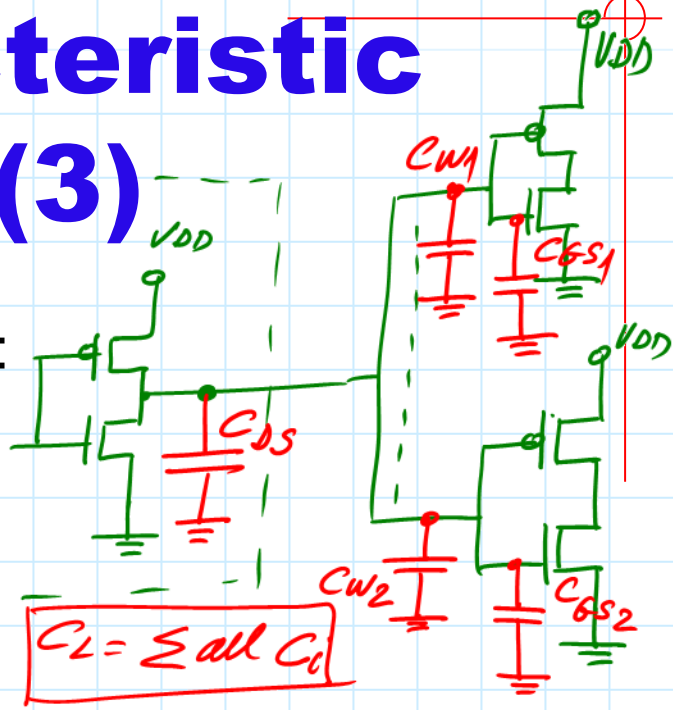
- Power Consumption:
  - Static regime: virtually null (≈ nA, pA), as there is always a transistor in cut-off mode (PMOS or NMOS)
  - Leakage currents:
    - Insulated Gate → Now high K dielectric instead of SiO_2
    - Subthreshold (when $V_{GS} < V_T$ if V_T is very small) → reverse currents
    - Increasingly important in VLSI (a billion transistors nowadays)

$$P_{leakage} = V_{DD} \times I_{leakage}$$

→ Provoques heating ⇒ Less integration density

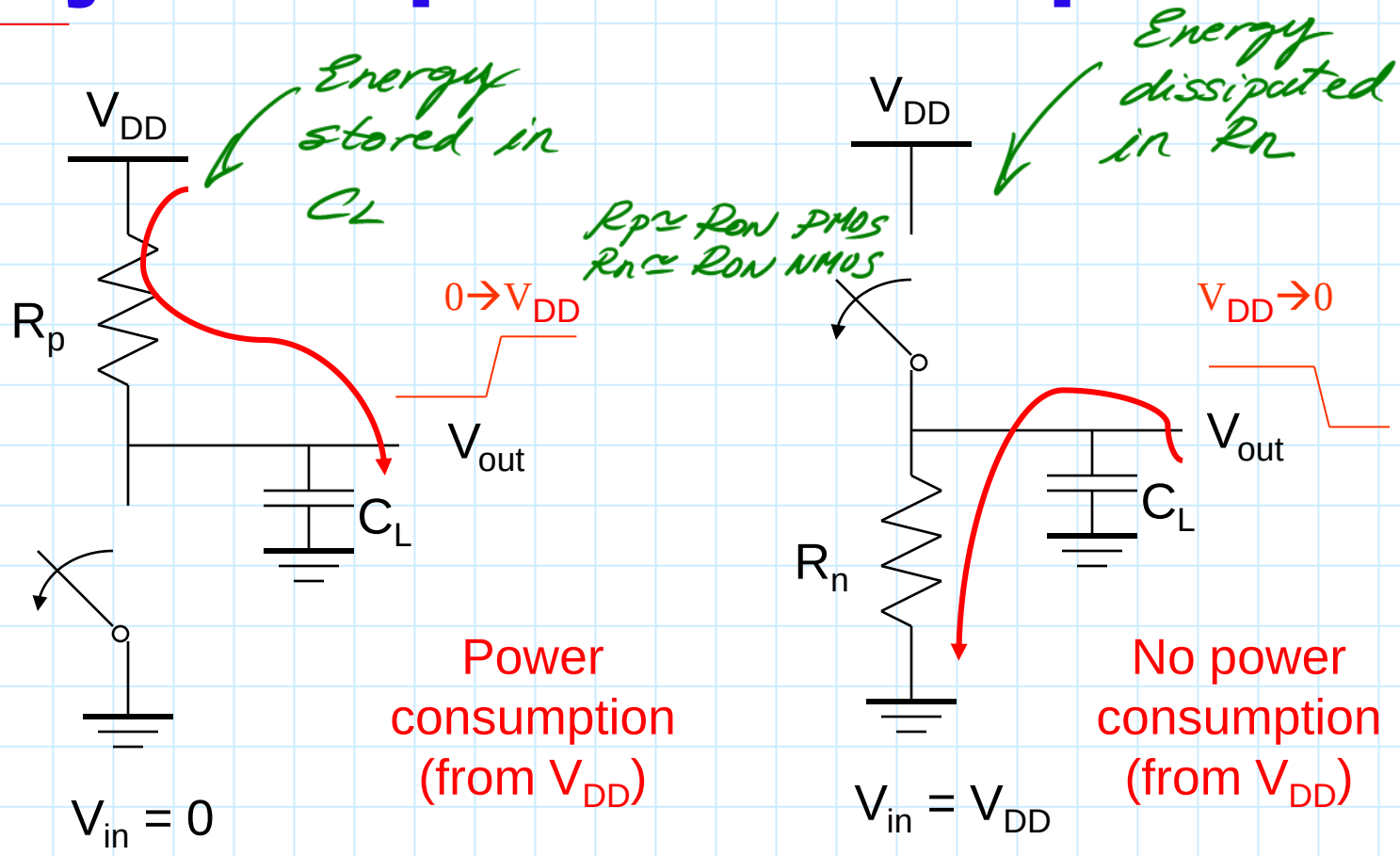
$1nA \times 1000 \cdot 10^6 = 1A!!$

4.5 CMOS characteristic parameters (3)



- Dynamic regime: $P_d = (V_{DD})^2 C_L f_i$, where:
  - C_L → parasitic capacitance of the load
  - f_i → switching frequency of inputs
  - This dissipated power is due to:
    - loading / unloading of C_L Great
    - Current peaks during transitions: the two transistors (PMOS and NMOS) conduct simultaneously. Small
  - Dynamic power consumption is the most important in CMOS technology:
    - In fact, static power consumption can be neglected
  - Note: If we refer P_d to the clock frequency "f" of the system:
    - $P_d = \alpha (V_{DD})^2 C_L f$ where:
    - α → average activity factor of the inputs (average number of transitions in one clock cycle)
    - $\alpha < 1$ → Normally, $\alpha < 0.5$; Input freq. is equal or less than $f/2$

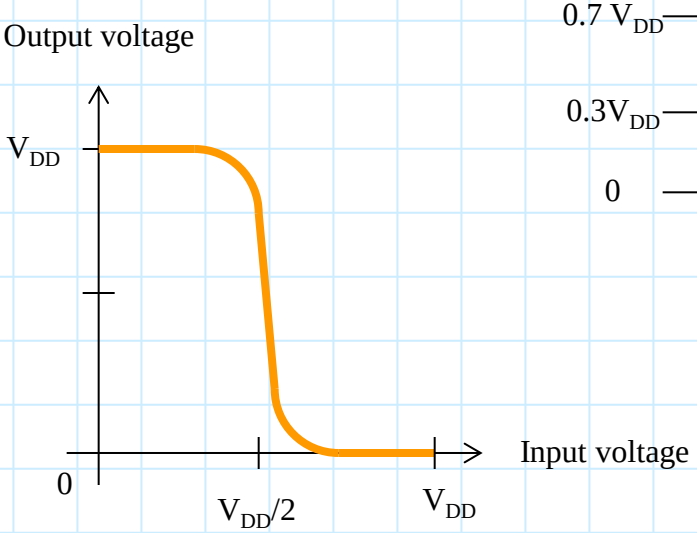
4.5 CMOS characteristic parameters (4): Dynamic power consumption

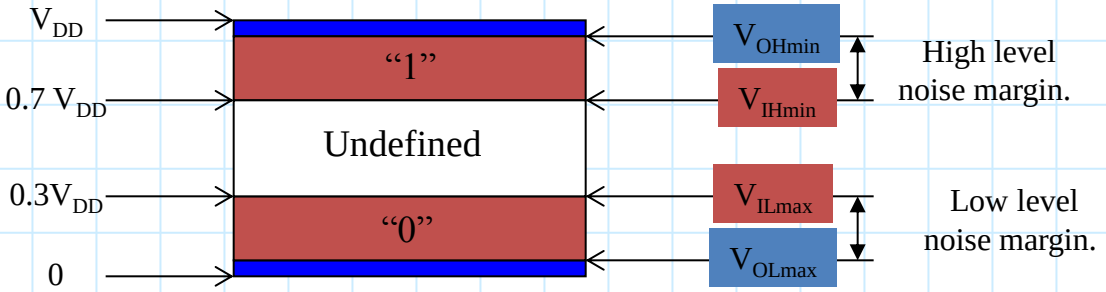


- The relevant dynamic consumption occurs in the transition L → H
- In the transition H → L there are only consumption due to simultaneous conduction of 2 transistors: short circuit.

4.5 CMOS characteristic parameters (5)

- Logic levels. Noise Immunity
  - Very ideal transfer curve





Standard CMOS values:

$V_{OHmin} = V_{DD} - 0.1V$ ≃ VDD

$V_{OLmax} = 0.1V$ ≃ 0V.

$NM \approx 30\% V_{DD}$ (1.5V for VDD=5V)*

Excellent noise inmunity (increases with V_{DD})

* TTL: 0.4V only!

4.5 CMOS characteristic parameters (6)

- Current levels. FAN-OUT (Standard CMOS current values)

I_{OH}	-0.5 mA	High level output current	Exits
I_{OL}	0.5 mA	Low level output current	Enters
I_{IH}	10 pA	High level input current	Enters
I_{IL}	-10 pA	Low level input current	Exits

- Very small input currents → We can connect a lot of inputs to a single output

static fan-out

$$Fan-Out_L = \left|\frac{I_{OL}}{I_{IL}}\right| = 50.000.000 \qquad Fan-Out_H = \left|\frac{I_{OH}}{I_{IH}}\right| = 50.000.000$$

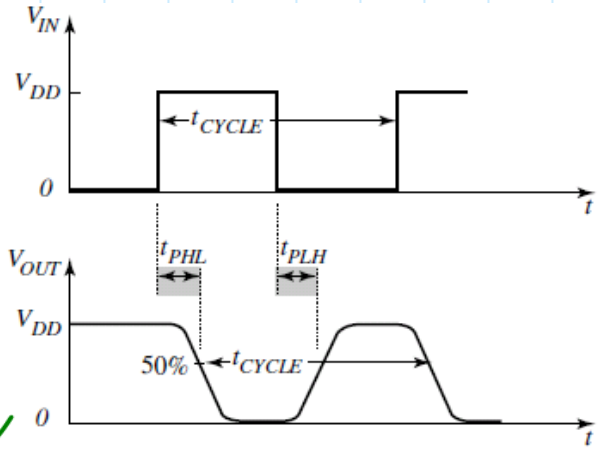
- Real constraint to not increase the delays and dynamic power consumption: the manufacturer recommends Fan-out = 50

dynamic fanout the most important!

4.5 CMOS characteristic parameters (7)

- Propagation delays

$$t_p = \frac{1}{2}\left(tp_{LH} + tp_{HL}\right) \approx \frac{C_L}{2V_{DD}}\left(\frac{1}{K_p} + \frac{1}{K_n}\right)$$



  - Depend on V_{DD}, C_L and K of transistors
    - Lower delay if high V_{DD}
    - Higher delay for high C_L
    - Lower delay if high K

$$K = \frac{1}{2}\mu C_{ox}\frac{W}{L}$$

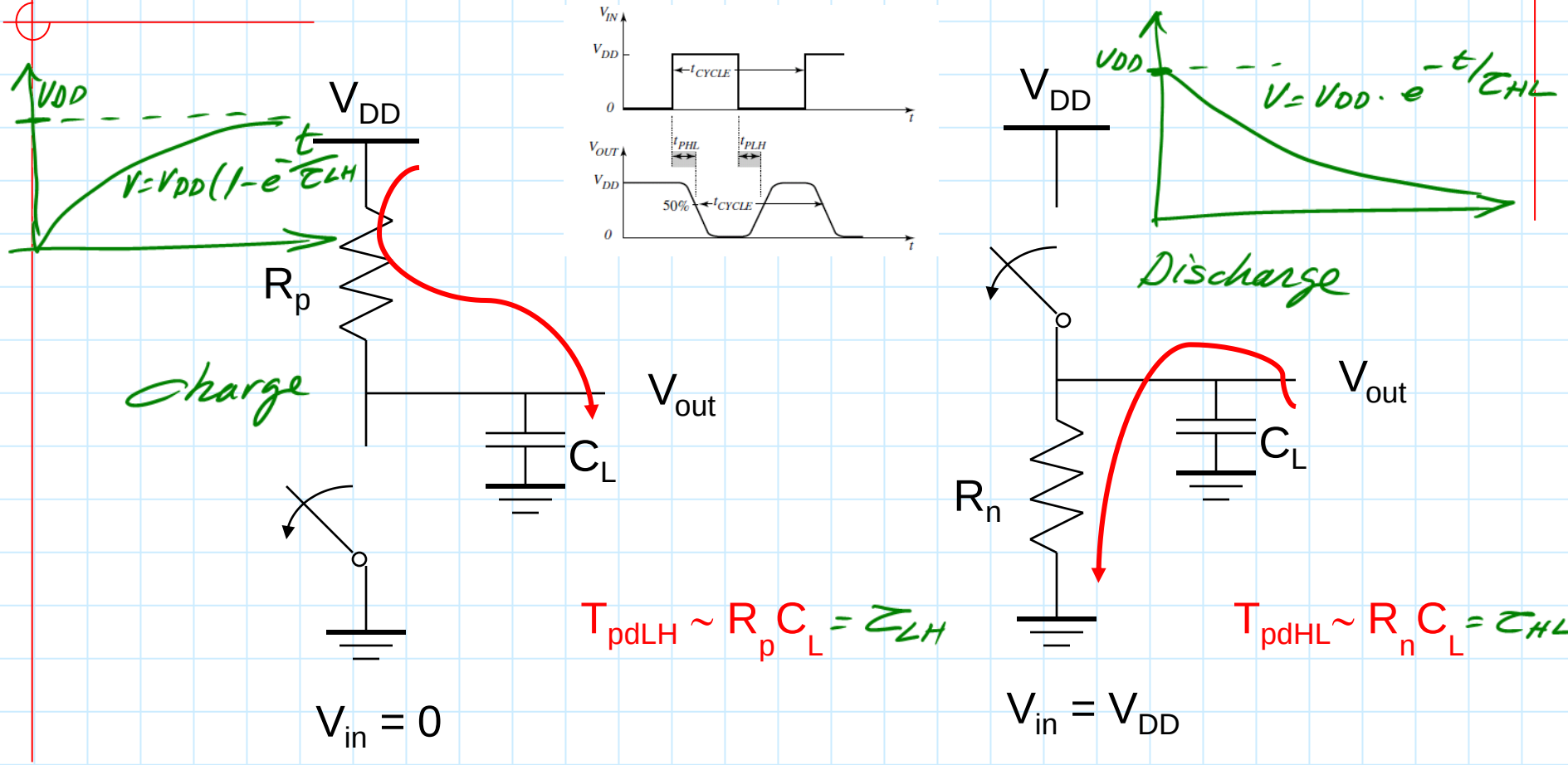
  - t_{pLH} and t_{pHL} can be equal, adjusting the NMOS and PMOS transistors size

$$\mu_n \approx 3\mu_p \qquad \left(\frac{W}{L}\right)_p \approx 2\left(\frac{W}{L}\right)_n$$

  - CMOS is now very fast, with similar delays to TTL
    - High Speed CMOS Subfamilies

- Product Propagation Delay * Power consumption (PDP): t_p*P → pJ, rather low due to low consumption, although there is a small increase because propagation delays

RC model for propagation delay



- The delays are given by the charging time of C_L through R_p, and by the discharging time of C_L through R_n)

4.6 CMOS subfamilies

- CD 4XXX : original family
  - 4XXXA: conventional
  - 4XXXB: with output buffer
- 74CXXX: TTL functionally CMOS compatible (pins and functions), but not electrically
- 74HCXXX: high speed CMOS
- 74HCTXXX: high speed CMOS with TTL compatible inputs
- 74ACXXX: Advanced high speed CMOS
- 74ACTXXX: Advanced high speed CMOS with TTL compatible inputs
- 74FCTXXX: Fast CMOS, TTL compatible
- BCT: BiCMOS (Bipolar-CMOS)
- ABT: Advanced BiCMOS
- LVC, ALVC: Low Voltage CMOS

4.6 CMOS subfamilies (2)

- The HC, AC and BCT subfamilies:
  - Have higher output current than standard CMOS
  - Are faster
  - The logic levels are not as extreme
  - More restricted supply voltage (between 2V and 6V)
- The HCT, ACT and FCT subfamilies:
  - Have TTL compatible inputs and CMOS outputs
  - Have a voltage supply of +5 V, as TTL
- LVC and ALVC subfamilies:
  - Work with V_{DD} less or equal to 3.3V (2.5, 1.8, 1.5,..)
  - Low-power applications

4.6 CMOS subfamilies (2)

- Example: 54/74HC00 (4 2-input NAND gates)
  - 54HC: military version (it works between -40 º C to +85 º C)
  - 74HC: commercial version (it works between -55 º C to +125 º C)
- VDD between 2V and 6V (typical = +5V)
  - V_{IHmin} = 3.15V, V_{ILmax} = 1.35V
  - V_{OHmin} = 3.84V, V_{OLmax} = 0.33V
  - I_{IHmax} = 1μA, I_{ILmax} = -1μA
  - I_{OHmax} = -4mA, I_{IHmax} = 4mA
  - $I_{CC(typ)}$ = 2 μA (average static current consumption)
  - $T_{pd(typ)}$ = 9 ns (average delay)
  - C_{pd} (gate capacity, without load) = 22pF
  - Comparing with standard CMOS:
    - Less extreme output voltage levels
    - Lower noise margin
    - Higher output currents
    - More speed

5V

	HC	CMOS
$V_{OH\,min}$	3.84	4.9
$V_{IH\,min}$	3.15	3.5
$V_{IL\,max}$	1.35	1.5
$V_{OL\,max}$	0.33	0.1
N_{MH}	0.69	1.4
N_{ML}	1.02	1.4