Session 8. Deliverable

PERFORMANCE AND CONFIGURATION OF MEMORY MODULES

Introduction

This practical exercise about memory modules is a deliverable task and therefore it has not a lab session assigned. For this task, the system information analysis program named CPU-Z is used to analyze the main memory configuration in a computer. The information provided by CPU-Z must be complemented with the analysis of the data sheet given by the memory manufacturer in order to know all the characteristics of the memory modules. Additionally, significant performance measurements, such as latencies and bandwidths, will be carried out. This exercise is oriented to the use of commercial SDRAM memory modules, so it is necessary to know how to interpret their data sheets and become familiar with them.

In addition, the complete realization of this practical exercise requires the previous installation of the CPU-Z program in some equipment to which the student has access, as well as the search in Internet of the data sheet of the memory modules contained in such equipment.

Objectives

- To obtain data about the capacity and structure of real memory modules
- To get and interpret information about the timing features of memory modules
- To calculate the most significant performance metrics of memory modules
- To reproduce the temporal sequence of commands and data transfer (chronogram) to access a certain number of memory blocks

In order to accomplish these objectives and to answer the proposed questions, in addition to this manual, in PoliformaT you can obtain the following:

- Version of the CPU-Z program to install on Windows. This can also be obtained through the following link: http://www.cpuid.com/softwares/cpu-z.html
- The data sheet provided by the manufacturer of the memory modules that are used as an example in the first part of this exercise.
- Illustrative videos on the main characteristics of SDRAM memories.
- The answer template to complete with the solutions and deliver through the corresponding task opened in PoliformaT

Basic timing parameters of SDRAM memories

As known, the memory access is usually carried out by the memory controller in a block-basis scheme (multi-word burst). This is the case when accessing blocks for filling the cache memory.

SDRAM memories are capable of transferring one word per clock cycle, or two words in the case of DDR SDRAM (one word on the rising and other on the falling edge of the clock). In any case, the first word of the block is transferred after a certain number of clock cycles (latency) since the beginning of the read operation. In this practical exercise only block read operations will be considered.

The different accesses to memory involve the generation of a series of commands subject to strict timing requirements, as established by the corresponding read chronogram of the memory chips. In this sense, accessing to a certain memory block requires, first, the activation of the corresponding row within the bank in which the block is located, sending the ACTIVATION command jointly with the row address and the bank number. Next, the reading operation must be ordered, sending the READ command together with the column address of the first word of the block and the bank number.

Once a row has been activated within certain bank, it is possible to issue successive READ commands on blocks belonging to the same row. However, to access blocks belonging to a different row within the same bank, it is necessary to perform a PRECHARGE operation of the current row before activating the new row. This operation is intended to restore the initial voltage values of the bit lines and leave the row amplifiers ready to accept a new row. On the other hand, it is possible to activate rows in different banks and keep them simultaneously open (as many rows as banks exist in the SDRAM), issuing READ commands on them in an interleaving or random way.

The SDRAM read chronogram forces a set of timing conditions on sending the different commands and transferring the data, having to fulfil minimum temporal distances (clock cycles) between them. The main timing parameters that govern the read of a memory block can be seen in Figure 1. In the case of DDR SDRAM memories, the data is transferred on each of the rising and falling edges of the clock (two words per cycle), whereas SDRAMs transmit only one word per cycle.

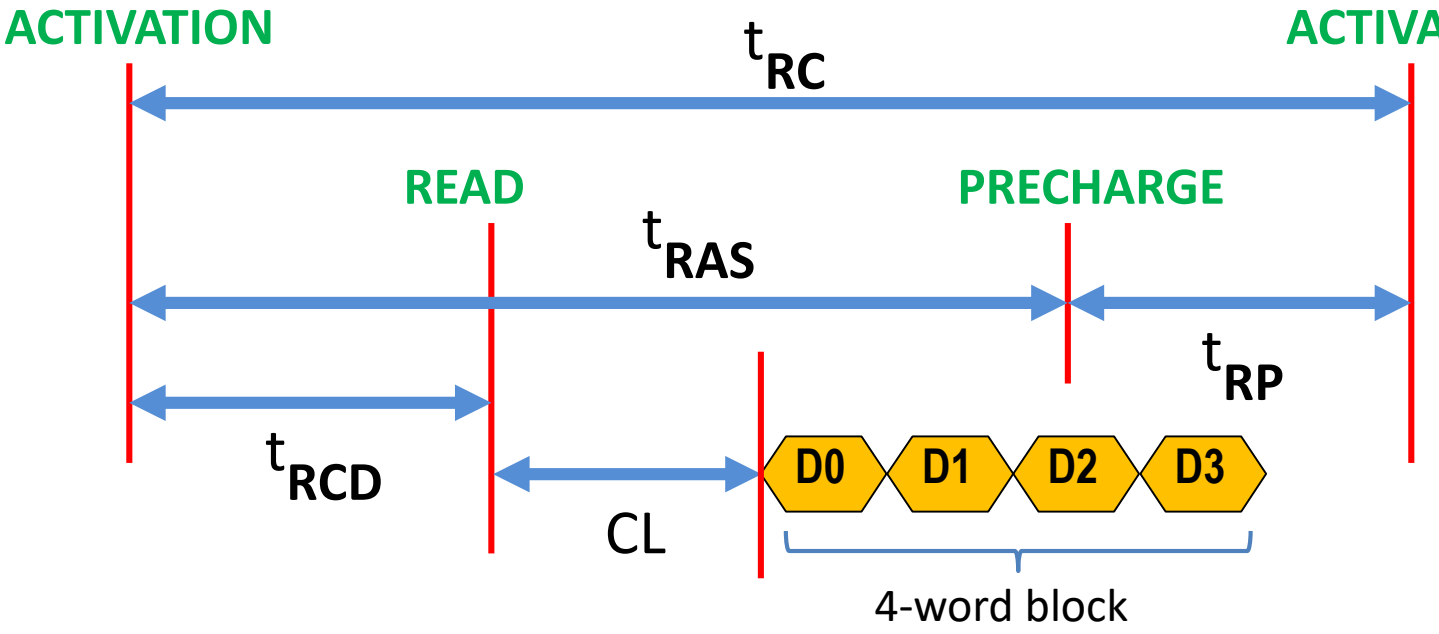

Figure 1. Basic timing parameters of a memory block READ operation

CL	CAS Latency: Number of clock cycles that the memory takes to provide the first word of the block since the sending of the READ command. The remaining words of the block are provided to the rate set either by the clock cycle or by its rising and falling edges
T_{RCD}	**Minimum** time between ACTIVATION and READ/WRITE commands on the same bank
T_{RP}	**Minimum** time between PRECHARGE and ACTIVATION commands on the same bank
T_{RAS}	**Minimum** time between ACTIVATION and PRECHARGE commands on the same bank
T_{RC}	**Minimum** time between ACTIVATION commands within the same bank

The corresponding data sheet of the SDRAM chips provides the values of the different timing parameters in nanoseconds (ns). Most of these parameters, as T_{RCD}, T_{RP}, T_{RAS} and T_{RC} parameters listed above, establish minimum timing requirements that must be guaranteed. For example, the elapsed time between two consecutive ACTIVATION commands on the same bank must be, at least, T_{RC}, but nothing prevents that there may be a greater temporal distance between them. For its practical application in a synchronous environment (timing requirements that the memory controller must satisfy), it is common to give these parameters in clock cycles. For this, the real value of the parameter (expressed in ns) is divided by the clock cycle and rounded to the upper integer. The timing of the SDRAM chips, in clock cycles, is usually expressed in the standard format established by JEDEC (Joint Electron Device Engineering Council): CL- TRCD - TRP- TRAS. This timing depends on the working frequency of the SDRAM chips, giving rise to different timings that, in the standard denomination, are referred to as JEDEC # 1, JEDEC # 2, JEDEC # 3, ... (see Figure 3).

It is important to know how to interpret the previous timing parameters correctly. For example, the T_{RC} parameter imposes the minimum elapsed time between two consecutive ACTIVATION commands on the same bank. However, the issue of the second ACTIVATION command depends not only on T_{RC}, but also on the time the PRECHARGE command has been issued, because from the latter must elapse, at least, T_{RP} before issuing the next ACTIVATION command. The issue of the PRECHARGE command must not take place until elapsed, at least, T_{RAS} since the issue of the previous ACTIVATION command. This means that the moment in which a certain command is issued must satisfy, at the same time, all the timing parameters. The parameter imposing the most restrictive constraints will eventually determine the minimum time to issue the referred command. Thus, the temporal distance between two consecutive ACTIVATION commands will correspond to:

$$máx\ (T_{RC},\ T_{RAS}+T_{RP},\ t_{PRECHARGE}+T_{RP})$$

where $t_{PRECHARGE}$ represents the real temporal distance ($\geq T_{RAS}$) between the PRECHARGE command and the issue of the previous ACTIVATION command. Note that this time could be delayed as a consequence of the block size, since a premature generation of the PRECHARG command (even satisfying T_{RAS}) would truncate the access to the block.

The SDRAM has two modes to perform the precharge: (1) explicitly, through the issue of a PRECHARGE command, and (2) implicitly or automatically, through the AUTO-PRECHARGE command. The latter is ordered alongside the READ command through an address line not used in the column address (line A10 in the example of Figure 2), which avoids wasting a clock cycle for the subsequent sending of the PRECHARGE command. However, it has the same effect as the latter and is subject to the same timing constrains (T_{RAS} since sending the ACTIVATION command).

It takes advantage of the fact that the precharge is performed automatically and at the optimum time[1].

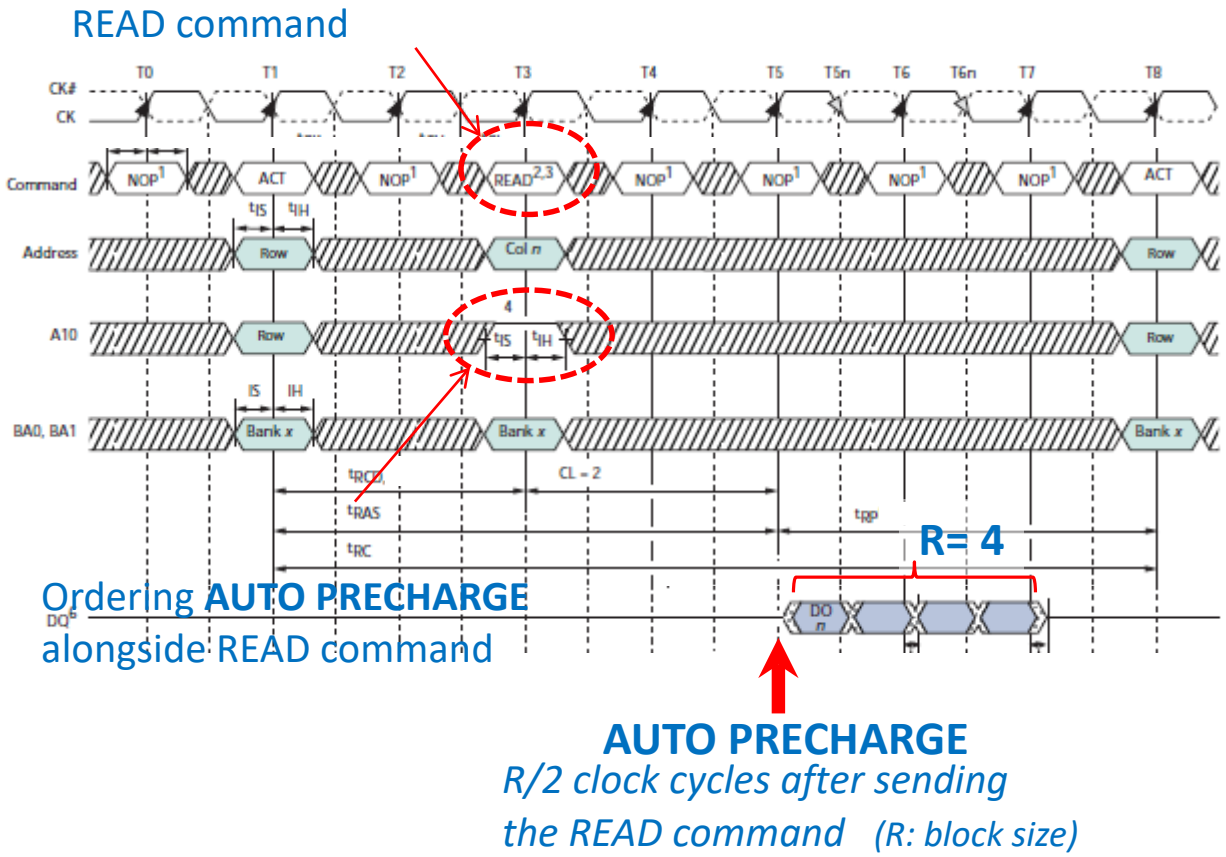

Figure 2. AUTO-PRECHARGE command ordering. DDR SDRAM

Finally, remember that SDRAM memories require a periodic refresh of their rows in order to guarantee the information integrity. There are different modes of refreshment, but the most common is the distributed refreshment of the different rows throughout the refresh period. To do this, SDRAMs provide the AUTO-REFRESH command, which refreshes the same row in all banks at the same time. The row address to be refreshed is contained in an internal memory register and is increased automatically. The refresh operation cannot be performed simultaneously with a memory access. In particular, the T_{RFC} parameter indicates the minimum time between the AUTO-REFRESH command and the sending of an ACTIVATION command. During this time read and write operations are not possible.

[1] *Given a block size of R words, the optimal instant to perform the precharge usually occurs R clock cycles after sending the READ command, in case of simple SDRAM, or R / 2 clock cycles after in the case of DDR SDRAM, as shown in Figure 2. In this case, being a four-word block (R = 4) and being a DDR SDRAM, the precharge will be effective 2 clock cycles after sending the READ command, coinciding with the outcoming of the first block word. Note that in this case the time T_{RAS} is accomplished. Otherwise, the precharge could not be carried out at the optimum moment. In any case, T_{RP} time must elapse since the precharge is effective until a new ACTIVATION command can be sent*

Proposed exercises: Obtaining the characteristics of SDRAM memory modules

To carry out the first part of this practice, two documents should be consulted: (1) the data sheet of a certain memory module provided by the manufacturer (file kvr1333d3n9_4g.pdf in PoliformaT); and (2) the data obtained regarding the memory subsystem configuration of an example computer after executing the CPU-Z analysis program in it, which is shown in Figures 3 and 4.

The data sheet of the memory module provides concise information about it. In particular, you can find information on the size and structure of the module, the type and maximum working frequency of its memory chips and some of the most relevant timing parameters of these chips. Also, parametric values with which the SPD (Serial Presence Detect)[2] of the memory module has been configured are provided.

The CPU-Z program provides additional information about the size, type, working frequency and timing characteristics of the memory modules just as they are configured in the computer in which CPU-Z is executed. This information is collected under the SPD and Memory tabs. CPU-Z provides a part of this information by accessing the SPD of the memory modules. That information is accessed during the boot by the BIOS[3] in order to configure the memory controller according to the timing requirements of the memory modules.

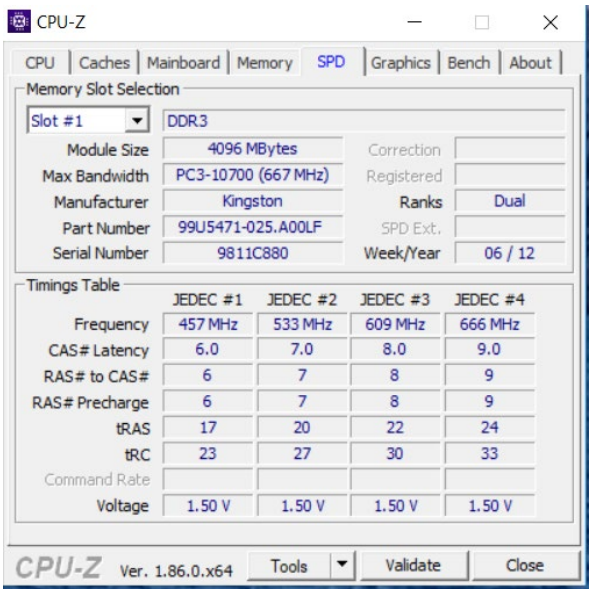

Figure 3. Memory module characteristics provided by the manufacturer

Figure 3 shows the information available in the SPD label corresponding to one of the memory slots (Slot # 1), an identical configuration in each available Slot can be found. Keep this information in mind to correctly answer the questions proposed. In particular, the different programmable settings in the SPD, which depend on the working frequency of the memory modules, can be observed (JEDEC # 1, …, JEDEC # 4).

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[2] *A small EEPROM memory recorded at the time of the module's manufacture.*

[3] *The BIOS (Basic Input Output System) is the firmware (software stored in a non-volatile memory) that is responsible, among other functions, for checking and setting the hardware before starting the operating system.*

Additionally, under the Memory tab you can find the values of the basic timing parameters of the memory modules, particularized to the frequency at which they are working in the computer in which they are installed, as shown in Figure 4.

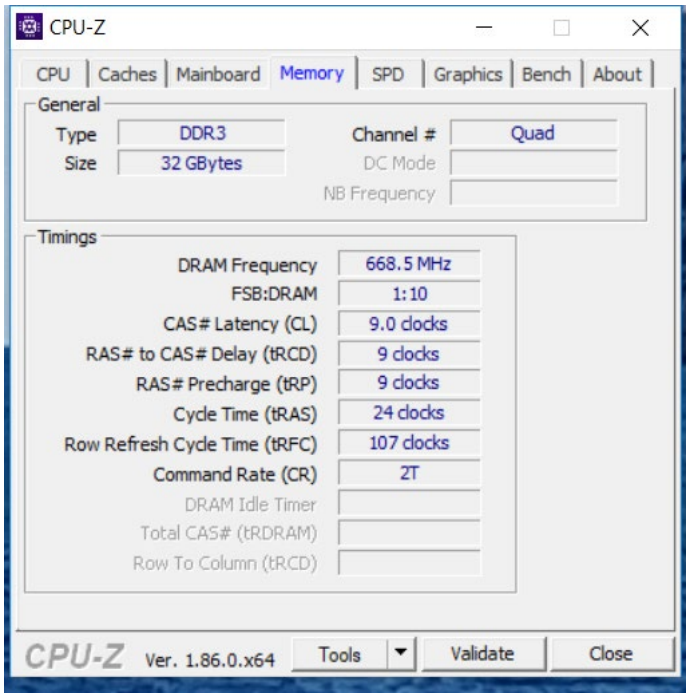

Figure 4. Basic timing parameters of the memory module according to its working frequency

PART I. Analysis of the memory configuration of the example equipment

1. From the data provided by the data sheet of the modules (file kvr1333d3n9_4g.pdf) and the CPU-Z program (Figures 3 and 4), complete in the following table. Recall that Figure 3 shows information only of one slot, but there is a second one with identical characteristics.

Information about the capacity and organization of memory modules

Total number of DIMMs	
Size of the DIMMs that compose the main memory *Expressed in MB*	
Total size of available main memory *Expressed in GB*	
Number of memory channels	
Capacity in words x word_size of the DIMMs	

Number of chip rows in each module	
Module memory chip size *(Expressed in words × word_size)*	
Total number of memory chips contained in a module	
Type of module memory chips *(DDR, DDR2, DDR3, DDR4)*	
Information about work frequency and bandwidth of the modules	
Clock frequency of the external buses of the modules used **in the computer on which CPU-Z was executed**	
Peak bandwidth of the modules used **in the computer on which CPU-Z was executed** *Expressed in MB/s*	
Standard nomenclature of the modules used **in the computer in which CPU-Z was executed** *(PC-xx00, PC2-xx00, PC3-xxx00, PC4-xxx00)*	
Maximum clock frequency to which the external buses of the module memory chips could work	
Maximum transfer rate that the memory modules could reach (words that are transferred per second) *Expressed in millions of transfers per second (MT/s)*	
Peak bandwidth that the memory modules could reach *Expressed in MB/s*	

2. The data sheet indicates that the module memory chips are of the DDR3-1333 type. What does the value 1333 mean?

3. From the data provided by the modules data sheet (kvr1333d3n9_4g.pdf) and by the CPU-Z program, complete the following table with the values of the main timing parameters:

	ns	Clock cycles
t_{CK} (clock cycles)		
T_{RAS}		
T_{RC}		
T_{RFC}		

***Note**: The number of clock cycles must always be an integer, so, if needed, it must be rounded to the upper integer. In the case that the clock cycle (t_{CK}) is not explicitly indicated in the data sheet, it should be calculated from the frequency at which the memory module has been programmed through its SPD*

4. Give the timing of the SDRAM chip in the standard format established by JEDEC (*Joint Electron Device Engineering Council*): JEDEC #X: CL- T_{RCD} - T_{RP}- T_{RAS}

JEDEC	#					

5. What would be the value of CL if the working frequency of the external buses of the memory modules is 500 MHz?

6. What would be the access time of the memory modules accounted from the start of the read operation (sending the ACTIVATION command) until the first data of the block is obtained?

	Clock cycles	ns
Access time		

PART II. Read chronogram for 3 four-word blocks. ► Using the data shown in Figure 2 and the timing parameters obtained in Part I, represent on the chronogram the timing of: i) the successive command issue, ii) the corresponding row and column addresses and, iii) the data transfer corresponding to the access to 3 blocks belonging to different rows of the same bank. The commands are: ACTIVATION (A) and READ (R). The address can be rows (Fi) or columns (Ci), where the subscript indicates the order number of the block (0 ... 2) to which they refer. Finally, the data will be expressed as D_i, where the subscript i refers to the word (0 ... 3) within each of the blocks. In addition, **the clock cycles in which precharges are performed must be marked with a (P) on the command line.** Remember that since it is a DDR SDRAM, two words are transferred in each clock cycle. ***Note**: It is not necessary to represent the issue of the NOP commands*

	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17	T18	T19	T20	T21	T22	T23	T24	T25	T26	T27	T28	T29	T30	T31	T32	T33	T34	T35	T36
Command																																				
Address																																				
Data																																				

	T37	T38	T39	T40	T41	T42	T43	T44	T45	T46	T47	T48	T49	T50	T51	T52	T53	T54	T55	T56	T57	T58	T59	T60	T61	T62	T63	T64	T65	T66	T67	T68	T69	T70	T71	T72
Command																																				
Address																																				
Data																																				

	T73	T74	T75	T76	T77	T78	T79	T80	T81	T82	T83	T84	T85	T86	T87	T88	T89	T90	T91	T92	T93	T94	T95	T96	T97	T98	T99	T100	T101	T102	T103	T104	T105	T106	T107	T108
Command																																				
Address																																				
Data																																				

PART III. Analysis of the student's computer memory configuration

To carry out this part of the practice, the student must install the CPU-Z program on his/her personal computer, either from the file provided in PoliformaT or through the link: http://www.cpuid.com/softwares/cpu -z.html

The file must be executed on the student's computer to know the most important characteristics of the system. The obtained memory information must be completed with the data extracted from the data sheet provided by the chip manufacturer. Commonly, this data sheet is easy to obtain through a query in any search engine. For example, for a memory manufactured by Kingston whose identification is KHX1600C10D3B1/8G (Part Number), you can type in any search engine "Kingston KHX1600C10D3B1/8G" to obtain the corresponding data sheet.

1. Copy and paste the screenshots corresponding to the SPD and Memory labels obtained from the execution of CPU-Z on your computer, equivalent to those shown in Figures 3 and 4.

2. From the data provided by the CPU-Z program about the memory configuration of the computer in which it was installed, complete the table below:

Identification of the memory module provided by the manufacturer	
Total number of DIMMs	
Total size of available main memory *Expressed in GB*	
Clock frequency of the external buses of the SDRAM modules *Expressed in MHz*	
Clock cycle to which the external buses of the SDRAM modules work *Expressed in ns*	
Peak bandwidth of the SDRAM modules *Expressed in MB/s*	
Standard nomenclature of the modules used in the computer analyzed *(PC-xx00, PC2-xx00, PC3-xxx00, PC4-xxx00)*	

3. Represent the timing of the SDRAM chip in the standard format established by JEDEC (*Joint Electron Device Engineering Council*): JEDEC #X: CL- T_{RCD} - T_{RP}- T_{RAS}

JEDEC	#		:		--		--		--	

4. What would be the access time of the memory modules counted from the start of the read operation (sending the ACTIVATION command) until the first data of the block is obtained?

	Clock cycles	**ns**
Access time		

5. Search for the data sheet of the memory modules installed in the analyzed equipment according to CPU-Z. Attach a copy of such data sheet as an annex to the end of this deliverable.
   ***Note**: Occasionally, the memory identifier offered by CPU-Z does not correspond to the real one, which can be observed by opening the device and examining the legend contained on the installed DIMMs. If this operation can be easily carried out, please indicate below the authentic identification of the modules*

6. Based on the data sheet of the memory modules you have located (according to the identifier offered by CPU-Z), fill in the table below:

Capacity in words x word_size of the DIMMs	
Number of chip rows in each module	
Total number of memory chips contained in a module	
Module memory chip capacity *(Expressed in words × word_size)*	
Type of module memory chips *(DDR, DDR2, DDR3, DDR4)*	
Maximum clock frequency to which the external buses of the module memory chips could work	
Maximum transfer rate that the memory modules could reach (words that are transferred per second) *Expressed in millions of transfers per second (MT/s)*	
Peak bandwidth that the memory modules could reach *Expressed in MB/s*	