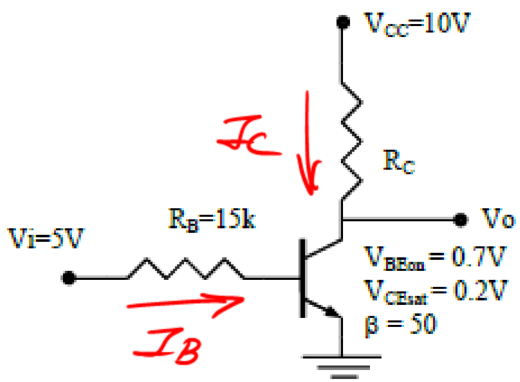
31. In the following circuit with transistor of the figure, which R_C value will get the transistor in the limit among active and saturation regions?



Conditions in the limit:

a) $V_{CE} = V_{CE(SAT)} = 0.2V$

b) $I_C \leq \beta I_B$

$\hookrightarrow$ (=) in the limit

$$I_B = \frac{V_i - V_{BE(ON)}}{R_B} = 0.29mA \;;\quad \overset{a)}{I_C = I_{C\,SAT}} = \frac{V_{CC} - V_{CE(SAT)}}{R_C} = \frac{9.8}{R_C}$$

b) $$I_C \leq \beta I_B = 14.33mA \;;\quad 14.33 \geq I_{C\,SAT} = \frac{9.8}{R_C}$$

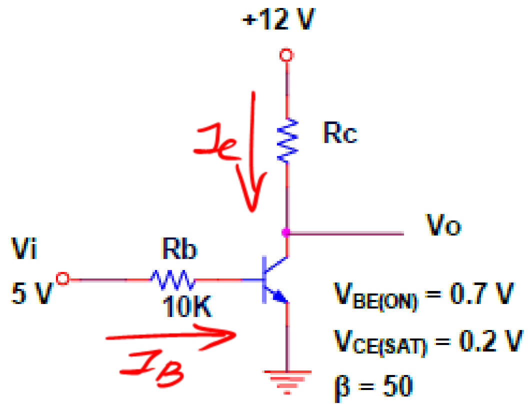
$$\boxed{R_C \geq \frac{9.8}{14.33} = 0.68K}$$

$R_C = 0.68K \Rightarrow$ limit $\begin{cases} \text{active} \\ \text{sat.} \end{cases}$

$R_C > 0.68K \Rightarrow$ saturation

32 In the BJT transistor circuit of figure, what is the minimum resistance R_C which leads the transistor to saturation?

[A] $R_C = 549\Omega$
[B] $R_C = 558\Omega$
[C] $R_C = 472\Omega$
[D] None of the above.



Sat $\Rightarrow$ $V_{CE} = V_{CE(SAT)} = 0.2\,V$; $I_C = I_{C(SAT)} = \dfrac{12 - V_{CE(SAT)}}{R_C} = \dfrac{11.8}{R_C}$

$I_B = \dfrac{5-0.7}{10K} = 0.43\,mA$

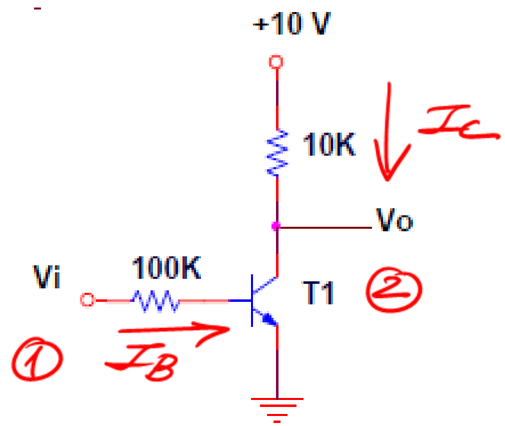
Sat: $I_C < \beta I_B \Rightarrow \dfrac{11.8}{R_C} < 50 \cdot 0.43 = 21.5\,mA$

$$\boxed{R_C > \dfrac{11.8}{21.5} = 0.549K}$$

37. Given the circuit of the figure, calculate the value of the limits of the input voltage Vi that lead the transistor to switching mode (Vi_{OFF}, Vi_{SAT})

DATA:

$V_{CE(SAT)} = 0.2V$
$V_{BE(ON)} = 0.7V$
$\beta = 50;$



a) Vi_{OFF} (T_1 OFF)

$Vi \leq V_{BE(ON)} = 0.7V \Rightarrow T_1 OFF;$

$$\boxed{Vi \leq 0.7 \Rightarrow T_1 OFF}$$

b) Vi_{SAT} (T_1 ON)

Input loop $\Rightarrow$ $I_B = \dfrac{Vi - V_{BE(ON)}}{100K} = \dfrac{Vi - 0.7}{100K}$

Output loop $\Rightarrow$ $I_C = \dfrac{10 - V_{CE(SAT)}}{10K} = \dfrac{10 - 0.2}{10K} = 0.98\,mA$

SAT $\Rightarrow$ $I_C < \beta I_B \Rightarrow 0.98 < \dfrac{50(Vi - 0.7)}{100} = \dfrac{Vi - 0.7}{2}$

$Vi > 0.7 + 2 \cdot 0.98 = 1.26\,V$

$$\boxed{Vi > 2.66V \Rightarrow T_1 SAT}$$

(35) The circuit of figure is a logic inverter. ¿What will be the minimum voltage at the input for output saturation? ($Ve_{MIN(SAT)}$)

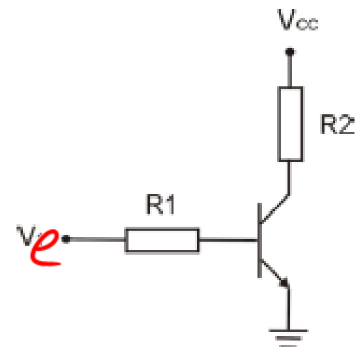
[A] $V_{eMIN(SAT)} = 2.5V$

[B] $V_{eMIN(SAT)} = 2.7V$

[C] $V_{eMIN(SAT)} = 3.1V$

[D] $V_{eMIN(SAT)} = 5V$

Data:
β: 100
R1= 100k
R2= 2k
Vcc= 5V
V_{BEON}= 0.7, V_{CESAT}=0.2V



$$SAT: V_{CE} = V_{CE(SAT)} = 0.2V;\ I_C = I_{C(SAT)} = \frac{V_{CC} - V_{CE(SAT)}}{R2} = \frac{5-0.2}{2} = 2.4mA$$

$$I_B = \frac{Ve - V_{BE(ON)}}{R1} = \frac{Ve - 0.7}{100}$$

$$SAT: I_C < \beta I_B \Rightarrow 2.4mA < 100\,\frac{Ve - 0.7}{100K}$$

$$\Rightarrow \boxed{Ve > 2.4 + 0.7 = 3.1V}$$

CH1. BASIC SEMICONDUCTOR DEVICES

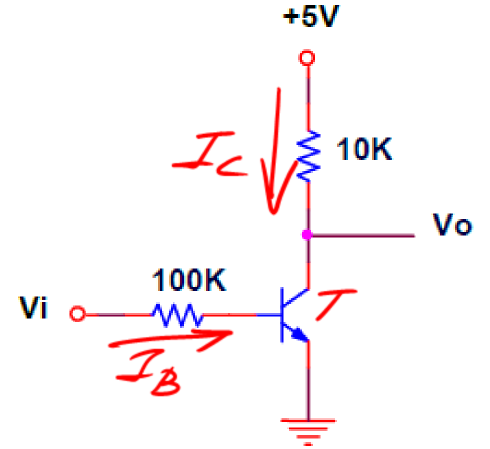
39. What will be the output of the following circuit if the input is a square wave with amplitude from 0V to 2V? (Data: $\beta = 100$; $V_{CE\,SAT} = 0.2V$; $V_{BE\,ON} = 0.7V$).

[A] A square wave with an amplitude from 0.7V to 5V. ✗

[B] A sine wave of same frequency and reverse phase. ✗

[C] A square wave with an amplitude from 0.2V to 5V. ✓

[D] A square wave with an amplitude from 2V to 5V. ✗



a) $V_i = 0V < V_{BE(ON)} \Rightarrow T$ OFF $\Rightarrow I_B = I_C = 0mA \Rightarrow \boxed{V_o = V_{CE} = V_{CC} = 5V.}$

b) $V_i = 2V > V_{BE(ON)} \Rightarrow T_{ON}$; $I_B = \dfrac{V_i - V_{BE(ON)}}{100K} = \dfrac{5-0.7}{100K} = 0.043mA$

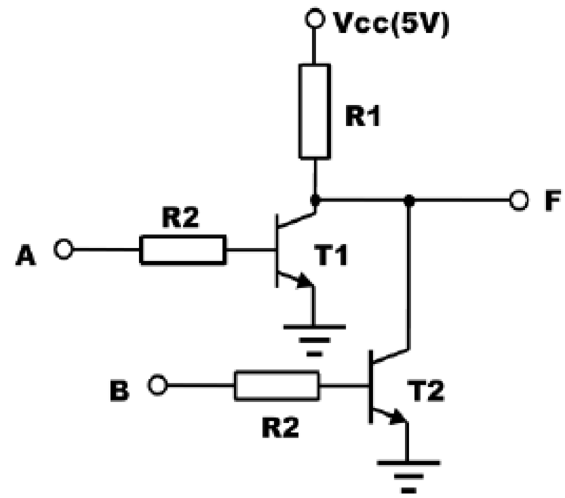
Assume saturated

$$I_C = I_{C(SAT)} = \frac{V_{CC} - V_{CE(SAT)}}{10K} = \frac{5-0.2}{10K} = 0.48mA$$

as $0.48mA = I_C < \beta I_B = 4.3mA \Rightarrow T$ saturated

an $\boxed{V_o = V_{CE(SAT)} = 0.2V}$

40. Given the circuit of the figure:



DATA: $V_{BE(ON)} = 0.6V$; $V_{CE(SAT)} = 0.2V$; R1 = 1k; R2 = 200k; $\beta = 500$.
Inputs ("1"-> 5V; "0"-> 0V)

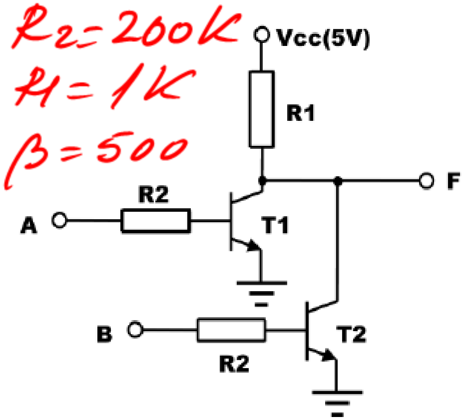
A) Truth table and state of T_1 and T_2 for all input combinations:

A	B	T_1	T_2	F	V_F (Volts)
0	0	OFF	OFF	1	Vcc (5V)
0	1	OFF	ON	0	0.2 V
1	0	ON	OFF	0	0.2 V
1	1	ON	ON	0	0.2 V

$\rightarrow$ V_{CESAT}, but we have to check (See C)

B) Logic function $F = \overline{A+B}$ (NOR)

$R_2 = 200K$
$R_1 = 1K$
$\beta = 500$

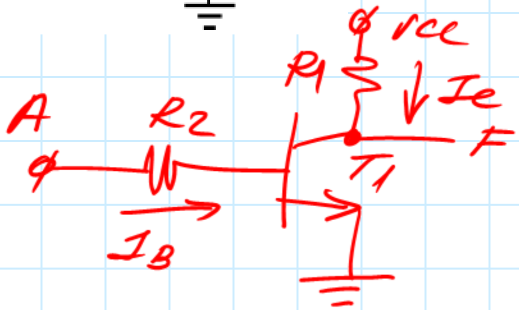


c) Voltage in F for all combinations

Case c1) $A = B = \emptyset \Rightarrow$ T1 OFF, T2 OFF $\Rightarrow$ $\boxed{V_F = V_{CC} = 5V}$

Case c2) $\left.\begin{array}{l} A = 1; B = 0 \\ A = 0; B = 1 \end{array}\right\}$ One trans. ON and another OFF

$\Rightarrow$



Minimum voltage of V_A for saturation:

$$I_{C(SAT)} = \frac{V_{CC} - V_{CE(SAT)}}{R_1} = \frac{5 - 0.2}{1K} = 4.8mA$$

$$\left.\begin{array}{l} I_B = \dfrac{V_A - V_{BE(ON)}}{R_2} \\ \beta I_B > I_{C(SAT)} \end{array}\right\} \quad \frac{500\,(V_A - 0.7)}{200} > 4.8mA \Rightarrow$$

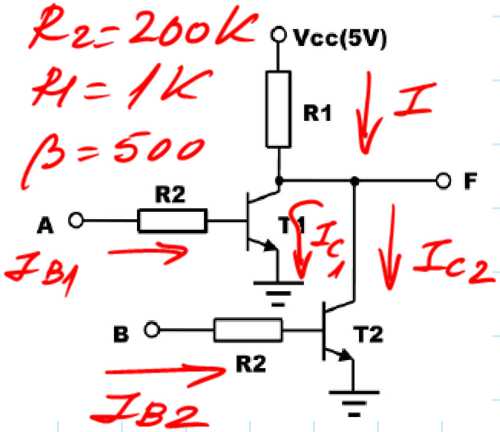
$$V_A > 0.7 + 4.8 \cdot \frac{2}{5} = 2.62V$$

$V_A > 2.62V \Rightarrow T_1$ saturated

as $V_A = 5V$ (High level) $\Rightarrow T_1$ saturated $\Rightarrow$

$$\boxed{V_F = V_{CE(SAT)} = 0.2V}$$

$R_2 = 200K$
$R_1 = 1K$
$\beta = 500$



Case a) $A = B = 1 \Rightarrow$ T_1 ON, T_2 ON

$I = I_{C1} + I_{C2}$ (Current through R_1 is split in two) Assuming both transistors equal: $I_{C1} = I_{C2} = \frac{I}{2} = I_C$ (also $I_{B1} = I_{B2} = I_B$)

Minimum V_A (or V_B) for saturation $\Rightarrow$ assume saturated both transistors $\Rightarrow$ $I = \frac{V_{CC} - V_{CE(SAT)}}{R_1} = 4.8\,mA$

$$\left.\begin{aligned} &I_C = \frac{I}{2} = 2.4\,mA = I_{C(SAT)} \\ &I_B = \frac{V_A - V_{BE(ON)}}{R_B} \\ &\beta I_B > I_{C(SAT)} \end{aligned}\right\} 500\,\frac{V_A - 0.7}{200} > 2.4\,mA \Rightarrow$$

$V_A > 0.7 + 2.4\,\frac{2}{5} = 1.66\,V$ for sat. (The same for V_B)

as $\left.\begin{aligned} V_A = 5V \\ V_B = 5V \end{aligned}\right\}$ $\left.\begin{aligned} T_1 \\ T_2 \end{aligned}\right\}$ saturated $\Rightarrow$ $\boxed{V_F = 0.2\,V}$