Practice 8. Deliverable

PERFORMANCE AND CONFIGURATION OF MEMORY MODULES

Name and surname:

GROUP:

Proposed exercises: Obtaining the characteristics of SDRAM memory modules

Information provided by the CPU-Z program for the example computer under the SPD tab.

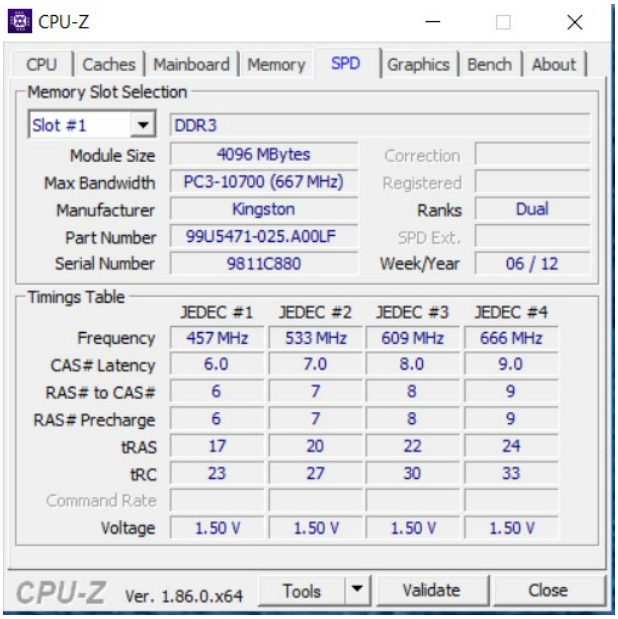

Figure 3. Memory module characteristics provided by the manufacturer

Timing parameters of the computer memory example:

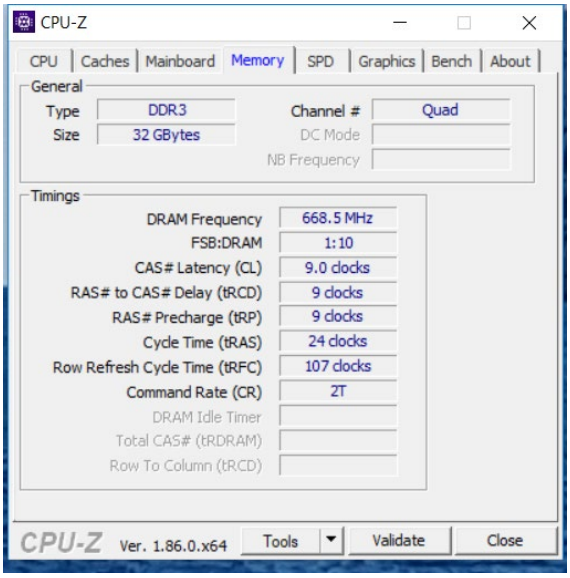

Figure 4. Main timing parameters of the memory module according to its working frequency

PART I. Analysis of the memory configuration of the example equipment

1. From the data provided by the data sheet of the modules (file kvr1333d3n9_4g.pdf) and the CPU-Z program (Figures 3 and 4), fill in the following table. Recall that Figure 3 shows information only of one slot, but there is a second one with identical characteristics.

(2.5 puntos)

Information about the capacity and organization of memory modules	
Total number of DIMMs	
Size of the DIMMs that constitute the memory *Expressed in MB*	
Total size of available main memory *Expressed in GB*	
Capacity in words x word_size of the DIMMs	
Number of memory channels	
Number of chip rows in each module	
Memory chips capacity of the modules *(expressed in words × word_size)*	
Total number of memory chips contained in a module	
Type of module memory chips *(DDR, DDR2, DDR3, DDR4)*	
Information about work frequency and bandwidth of the modules	
Clock frequency of the the external buses of the modules used **in the equipment on which CPU-Z was executed**	
Peak bandwidth of the modules used **in the equipment on which CPU-Z was executed** *Expressed in MB/s*	
Standard nomenclature of the modules used **in the equipment in which CPU-Z was executed** *(PC-xx00, PC2-xx00, PC3-xxx00, PC4-xxx00)*	
Maximum clock frequency to which the external buses of the module memory chips could work	
Maximum transfer rate that the memory modules could reach (words that are transferred per second) *Expressed in millions of transfers per second (MT/s)*	

Peak bandwidth that the memory modules could reach *Expressed in MB/s*	

2. The data sheet indicates that the module memory chips are of the DDR3-1600 type. What does the value 1600 mean?

(0.5 puntos)

3. A partir de los datos proporcionados por la hoja de especificaciones de los módulos (file kvr1333d3n9_4g.pdf) y el programa CPU-Z, rellénese la siguiente tabla con los valores de los principales parámetros temporales: **(0.5 puntos)**

	ns	**Ciclos de Reloj**
t_{CK} (ciclo de reloj)		
T_{RAS}		
T_{RC}		
T_{RFC}		

***Note**: The number of clock cycles must always be an integer, so, if needed, it must be rounded to the upper integer. In the case that the clock cycle (t_{CK}) is not explicitly indicated in the data sheet, it should be calculated from the frequency at which the memory module has been programmed through its SPD.*

4. Express the timing of the SDRAM chip in the standard format established by JEDEC (*Joint Electron Device Engineering Council*): JEDEC #X: CL- T_{RCD} - T_{RP}- T_{RAS} **(0.5 puntos)**

JEDEC # [ ] : [ ] -- [ ] -- [ ] -- [ ]

5. What would be the value of CL if the working frequency of the external buses of the memory modules was 500 MHz? **(0.5 puntos)**

6. What would be the access time of the memory modules counted from the start of the read operation (sending the ACTIVATION command) until the first data of the block is obtained?

(0.5 puntos)

	Clock cycles	**ns**
Access time		

PART II. Read chronogram for 3 four-word blocks. ► Using the data shown in Figure 2 and the timing parameters obtained in Part I, represent on the chronogram the timing of: i) the successive command issue, ii) the corresponding row and column addresses and, iii) the data transfer corresponding to the access to 3 blocks belonging to different rows of the same bank. The commands are: ACTIVATION (A) and READ (R). The address can be rows (Fi) or columns (Ci), where the subscript indicates the order number of the block (0 ... 2) to which they refer. Finally, the data will be expressed as D_i, where the subscript i refers to the word (0 ... 3) within each of the blocks. In addition, **the clock cycles in which precharges are performed must be marked with a (P) on the command line.** Remember that since it is a DDR SDRAM, two words are transferred in each clock cycle. ***Note****: It is not necessary to represent the issue of the NOP commands*

	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17	T18	T19	T20	T21	T22	T23	T24	T25	T26	T27	T28	T29	T30	T31	T32	T33	T34	T35	T36
Command																																				
Address																																				
Data																																				

	T37	T38	T39	T40	T41	T42	T43	T44	T45	T46	T47	T48	T49	T50	T51	T52	T53	T54	T55	T56	T57	T58	T59	T60	T61	T62	T63	T64	T65	T66	T67	T68	T69	T70	T71	T72
Command																																				
Address																																				
Data																																				

	T73	T74	T75	T76	T77	T78	T79	T80	T81	T82	T83	T84	T85	T86	T87	T88	T89	T90	T91	T92	T93	T94	T95	T96	T97	T98	T99	T100	T101	T102	T103	T104	T105	T106	T107	T108
Command																																				
Address																																				
Data																																				

PART III. Analysis of the student's computer memory configuration

To carry out this part of the practice, the student must install the CPU-Z program on his personal computer, either from the file provided in PoliformaT or through the link: http://www.cpuid.com/softwares/cpu -z.html

The file must be executed on the student's computer to know the most important characteristics of the system. The obtained memory information must be completed with the data extracted from the data sheet provided by the chip manufacturer. Commonly, this data sheet is easy to obtain through a query in any search engine.

For example, for a memory manufactured by Kingston whose identification was KHX1600C10D3B1/8G (Part Number), it would suffice to type in any search engine "Kingston KHX1600C10D3B1/8G" to obtain the corresponding data sheet.

1. Copy and paste the screenshots corresponding to the SPD and Memory labels obtained from the execution of CPU-Z on your computer, equivalent to those shown in Figures 3 and 4.

   (0.5 puntos)

2. From the data provided by the CPU-Z program about the memory configuration of the equipment in which it was installed, fill in the table below:

   (0.5 puntos)

Identification of the memory provided by the manufacturer	
Total number of DIMMs	
Total size of available main memory *Expressed in GB*	
Clock frequency of the external buses of the SDRAM modules *Expressed in MHz*	
Clock cycle to which the external buses of the SDRAM modules work *Expressed in ns*	
Peak bandwidth of the SDRAM modules *Expressed in MB/s*	
Standard nomenclature of the modules used in the analyzed equipment *(PC-xx00, PC2-xx00, PC3-xxx00, PC4-xxx00)*	

3. Represent the timing of the SDRAM chip in the standard format established by JEDEC (*Joint Electron Device Engineering Council*): JEDEC #X: CL- T_{RCD} - T_{RP}- T_{RAS} **(0.25 puntos)**

JEDEC	#		:		--		--		--	

4. What would be the access time of the memory modules accounted from the start of the read operation (sending the ACTIVATION command) until the first data of the block is obtained? **(0.25 puntos)**

	Clock cycles	**ns**
Access time		

5. Search for the data sheet of the memory modules installed in the analyzed equipment according to CPU-Z. Attach a copy of such data sheet as an annex to the end of this deliverable. **(0.25 puntos)**

***Note**: Occasionally, the memory identifier offered by CPU-Z does not correspond to the real one, which can be observed by opening the device and examining the legend contained on the installed DIMMs. If this operation can be easily carried out, please indicate below the authentic identification of the modules*

6. Based on the data sheet of the memory modules you have located (according to the identifier offered by CPU-Z), fill in the table below: **(0.5 puntos)**

Capacity in words x word_size of the DIMMs	
Number of chip rows in each module	
Total number of memory chips contained in a module	
Module memory chips capacity *(Expressed in words × word_size)*	
Type of module memory chips *(DDR, DDR2, DDR3, DDR4)*	
Maximum clock frequency to which the external buses of the module memory chips could work	
Maximum transfer rate that the memory modules could reach (words that are transferred per second) *Expressed in millions of transfers per second (MT/s)*	
Peak bandwidth that the memory modules could reach *Expressed in MB/s*	

Insert here the screenshots obtained after executing the CPU-Z program

Insert here manufacturer's data sheet