Computer Architecture and Engineering - 3rd Course. **Examen 1st partial** **24/1/2017**

Answer each question in a different answer sheet. Available time: 2h 30'

1. **(3 points)**

   A program is sequentially executed in 100 seconds on a computer. It devotes 20 % of this time to carry out arithmetic operations and 50 % loading data from, and storing results to, memory. During the remaining 30 % of the time, the programa carries out other tasks. It is worth mentioning that half of the time devoted to these other tasks concentrates in tasks whose execution cannot be parallelized. Answer the following questions:

   a) How long would the execution of the program take if the program runs on a computer providing SIMD (*Single Instruction, Multiple-Data*) instructions suitable for processing 4 elements in each ALU, load and store operation? Asume all concerned operations can be replaced by SIMD instructions.

   b) How long would the execution of the program take if using a 10-core, without SIMD instructions support, computer?

   c) If each of the 10 cores available provides support to the considered SIMD instructions, which will be the resulting speed-up with respect to the original computer? and, which will be the new execution time of the considered program?

   d) Which will be the best possible performance (speed-up and execution time for the considered program) if one could integrate in the computer as many cores as desired?

2. **(2.5 points)**

   The execution of a program shows that 10 % ($CPI = 1{,}5$) of instructions are branches, 30 % ($CPI = 2$) are loads and stores, 10 % ($CPI = 1$) are ALU, 20 % ($CPI = 4$) are single precision floating point instructions and finally, the remaining 30 % ($CPI = 6$) are double precision floating point instructions.

   Answer the following questions:

   a) Average execution CPI.

   b) The use of vector instructions (SIMD) is introduced in order to improve the execution of floating point instructions. These instructions enable:

   - The combination of 4 single-precision floating point instructions into a single SIMD instruction.
   - The combitnation of 2 double-precision floating point instructions into a single SIMD instruction.

   On the other hand, it is known that SIMD instructions have the same CPI that the corresponding floating point ones.

   Assuming that all floating point instructions in the considered application can be replaced by SIMD instructions, which will be the new distribution of instructions?

   c) Which will be the execution speed up resulting from the use of SIMD instructions?

3. **(2.5 points)** A MIPS processor is available. It integrates the following operators:

   - Pipelined Adder/Substracter. Lat= 2, IR= 1.
   - Pipelined Multiplier. Lat= 4, IR= 1.
   - Conventional Divider. Lat= 5, IR= $\frac{1}{5}$.

   Structural and data hazards are detected in stage ID, thus inserting as many stalls are necessary and using shortcircuits whenever possible. Control hazards are solved through delayed branching, taking into account that conditions and branch destination addresses are computed during ID and the PC is updated with the destination address at the end of EX.

   The code executed in the considered processor is:

```
dadd r1, r0, x
dadd r2, r0, z
dadd r4, r1, 32
```

```
        l.d f0, a(r0)           ; Load a
loop:
        l.d f1, 0(r1)
        div.d f2, f1, f0
        mult.d f3, f1, f0
        add.d f4, f2, f3
        s.d f4, 0(r1)
        dadd r1, r1, 8
        dsub r5, r4, r1
        bnez r5, loop
        nop
        nop
        nop
        trap 0.
```

Answer the following questions using the notation: `IF` instruction fetch, `ID` instruction decoding, `EX` monocycle execution, `A1,A2` adder/substracter execution stages, `M1,M2,M3,M4` multiplier execution stages, `D1,D2,D3,D4,D5` divider execution stages, `ME` memory access stage and `WB` write back to registers. Multicycle instructions do not carry out the `ME` stage.

a) Complete the instructions-time diagram for the first loop iteration including until the first instruction of the second loop iteration.

b) Complete the instructions-time diagram of the last loop iteration, from the *dsub* instruction to the *trap* instruction (both included).

c) Compute the average CPI of a loop iteration.

d) Compute the TOTAL execution time of the provided code in cycles for n iterations (from the fetch of the first instruction dadd r1,r0,x until the WB stage of instruction trap 0).

4. **(2 points)** A processor with an MIPS-like instruction set is available. It integrates an execution unit pipelined in the following stages:

   - **IF** Instruction Fetch.
   - **ID** Instruction decoding and register reading.
   - **EX** ALU execution. Computation of conditions and destination addresses for branches. Computation of the address for a memory (load/store) access.
   - **ME** Memory access.
   - **WB** Writing back of results to the register file.

   The following table shows the behavior of a *Branch Target Buffer* predictor when it predicts that a conditional branch instruction is **taken** and it is finally **not taken**.

I. Salto	IF	ID	EX	ME	WB			
DEST		IF	ID	X				
DEST+1			IF	X				
PC+1				IF	ID	EX	ME	WB

   Answer the following questions:

   a) In which stage is updated the PC?

   b) In which stage is the prediction carried out?

   c) Complete the same tables considering the following cases: i) Prediction is **not taken** and it is **not taken** , ii) Prediction is **not taken** and it is **taken** and iii) Prediction is **taken** and it is **taken**

Name and Surname:	

Exercise 3

1. Complete the instructions-time diagram for the first loop iteration including until the first instruction of the second loop iteration.

	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
dadd r1, r0, x																														

2. Complete the instructions-time diagram of the last loop iteration, from the *dsub* instruction to the *trap* instruction (both included).

	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16
dsub r5, r4, r1																