## UNIT 5. SEMICONDUCTOR MEMORY TECHNOLOGY. PROPOSED QUESTIONS AND EXERCISES

1) A memory has 2048 words of 32 bits. What is its storage capacity in KBytes?
   [A] 2KB
   [B] 4KB
   [C] 8KB
   [D] 16KB

2) Given a $2^{14}$-word semiconductor memory and provided that each word has 32 bits, we can conclude that:
   [A] It requires 14 address lines
   [B] It requires 6 address lines
   [C] Its storage capacity is 16KBytes
   [D] Its storage capacity is 64Kbits

3) Concerning the mask-programmed ROMs, we can state that:
   [A] They are volatile memories which lose their content when power is switched off.
   [B] They are no random access memories.
   [C] They are programmed during the manufacturing process.
   [D] We can re-write its content by using the appropriate programming device.

4) The data stored in a given address of SRAM memory are lost when:
   [A] Power is switched off.
   [B] We read the data in this address.
   [C] It passes longer time than the memory refresh time.
   [D] None of the above.

5) A ROM is:
   [A] A non-volatile memory
   [B] A volatile memory
   [C] A read/write memory
   [D] A memory based on FAMOS cells

6) The storage cell in a SRAM is:
   [A] A fuse
   [B] A capacitor
   [C] A flip-flop
   [D] An NMOS transistor

7) The storage cell in a DRAM is:
   [A] A fuse
   [B] A capacitor
   [C] A flip-flop
   [D] An NMOS transistor

8) The storage cell in a FLASH is:
   [A] A fuse
   [B] A capacitor
   [C] A flip-flop
   [D] A FAMOS transistor

9) A DRAM should be:
   [A] Regularly replaced
   [B] Regularly refreshed
   [C] Always enabled
   [D] Programmed before each use

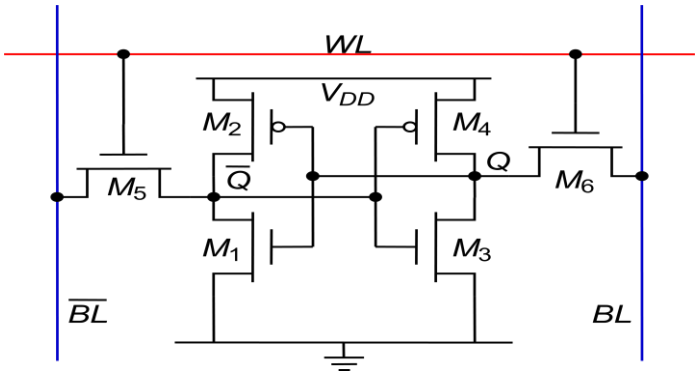
10) A FLASH memory is:
[A] Volatile
[B] Read-only memory
[C] A read/write memory
[D] Non-volatile
[E] The answers [A] & [C]
[F] The answers [C] & [D]

11) Signal the FALSE statement among the following related to semiconductor-based memories:
[A] PROMs are non-volatile, random access memories.
[B] The cells inside ROMs are implemented in the manufacturing process, then they are not programmable by the end user.
[C] SRAMs are non-volatile random access memories, as soon as they do not need a refreshing process.
[D] The cells of EPROMs and FLASHs are based on FAMOS transistors that have floating gates for cutting the selected transistors.

12) Indicate the pros and cons of flash memory in relation to SRAM and DRAM memories.

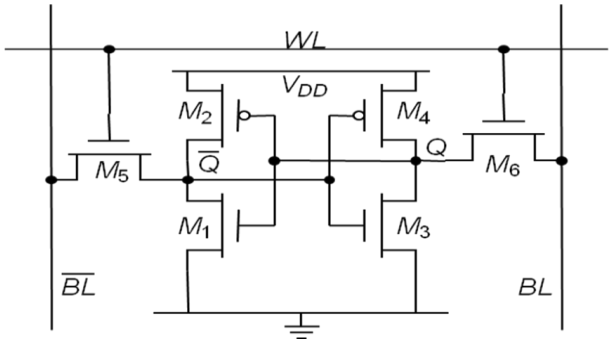
13) Given a DRAM chip of a capacity of 2Mx1, we can state that:
[A] Its internal structure can be an array of $2^{11}$ rows and $2^{10}$ columns.
[B] It has a capacity of 2MBytes.
[C] It has 20 address lines and 1 data line
[D] We can build a 16Mbytes memory grouping 8 of the same type.

14) Given the memory cell of the figure, indicate the CORRECT answer:




[A] It is a 6T dynamic memory cell
[B] The input data are in /BL, and output data in BL
[C] The storage core is the flip-flop formed by transistors M1-M2-M3-M4.
[D] The pass transistors M5 and M6 provide access to the cell in read/write, when WL="0"

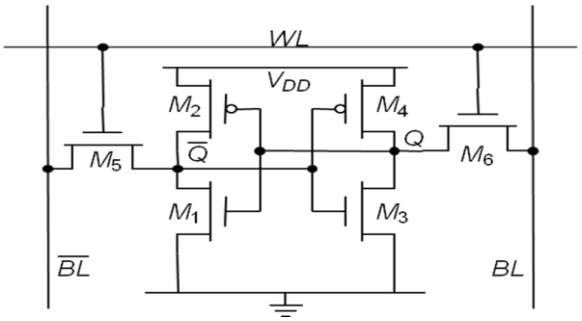
15) Given the memory cell of the figure, indicate the CORRECT answer:




[A] It is a 6T dynamic memory cell
[B] The reading process is: Precharge of BL and /BL; activate WL to '1', and read the bit lines.
[C] The input data are placed in /BL and the output data in BL.
[D] The pass transistors M5 and M6 provide access to the cell in read/write, when WL="0"

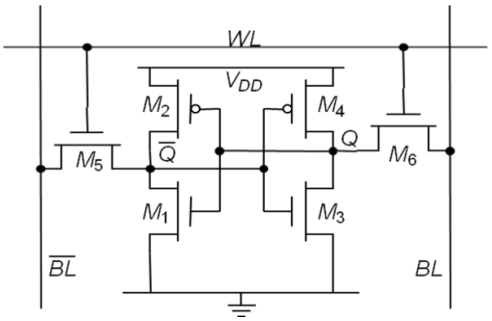
16. Given the memory cell of the figure, indicate the CORRECT answer:

[A] It is a 6T dynamic memory cell
[B] For writing a '1' in the cell (Q='1' y /Q='0'), we have to set /BL to '0' and BL to '1', enabling afterwards the cell setting WL='1'.
[C] The resistors $R_{ON}$ of all transistors of the cell should be approximately the same value, to properly writing and reading in the cell.
[D] The connections shown in the figure are wrong. BL and /BL are interchanged.



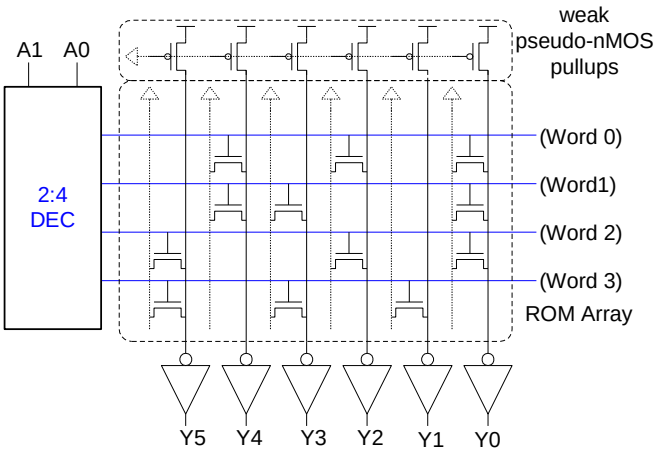

17. Given the memory cell of the figure, indicate the CORRECT answer:

[A] This is a DRAM cell including the refresh circuit.
[B] Writing process is the following: precharge BL with the data to be written and /BL with the opposite, activate WL to 0 and wait the data to be written into the cell.
[C] BL bit line is for data reading, and /BL for data writing.
[D] Transistors M1, M2, M3 and M4 implement a flip-flop that stores the logic value of the cell.



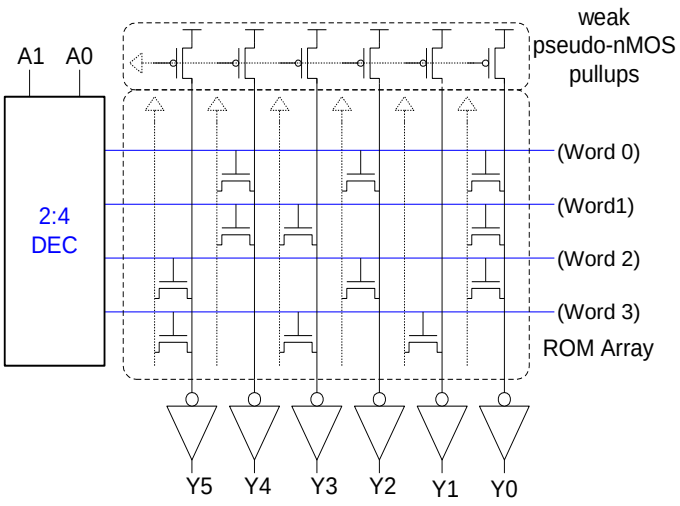
18. Given the memory of figure, point out the FALSE statement:

[A] This is a ROM memory of 4 words of 6 bits.
[B] When A1=1 and A0=1, the word “100101” is obtained in the data bus.
[C] The presence of transistor sets to “0” the cell, but a “1” is read at the output Yx.
[D] The transistors are placed in the manufacturing process, not allowing subsequently any modification, and giving non-volatility at these memories.




19. Given the memory of figure, point out the FALSE statement:

[A] This is a ROM memory of 4 words of 6 bits.
[B] When A1=1 and A0=1, the word “100101” is obtained in the data bus.
[C] The presence of transistor sets to “0” the cell, but a “1” is read at the output Yx.
[D] Pull up transistors behave as a pull up resistors connected to power supply..

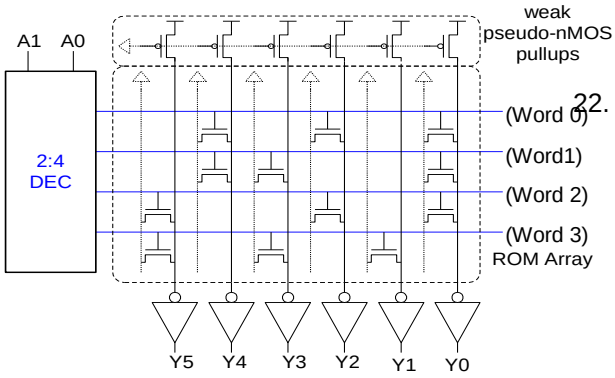



20. Indicate the relative size of transistors of a 6T SRAM cell: (NMOS, PMOS pass transistors). Justify your answer.

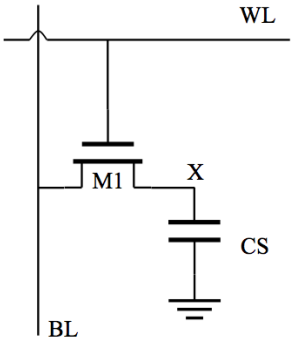
21. Signal the **CORRECT** statement among the following related to the memory of figure:

**Note:** A1 is the most significant bit and A0 the least significant.

[A] This is an example of a NAND ROM structure.
[B] It corresponds to a non-volatile programmable memory, since it is easy to add or remove transistors, at any time by the user.
[C] When A1=0 and A0=1, the word "011001" is read in the Y5, Y4,…, Y0 data lines.
[D] The presence of an NMOS transistor puts a '1' in the cell, which is read as '0' in the corresponding output Yx.

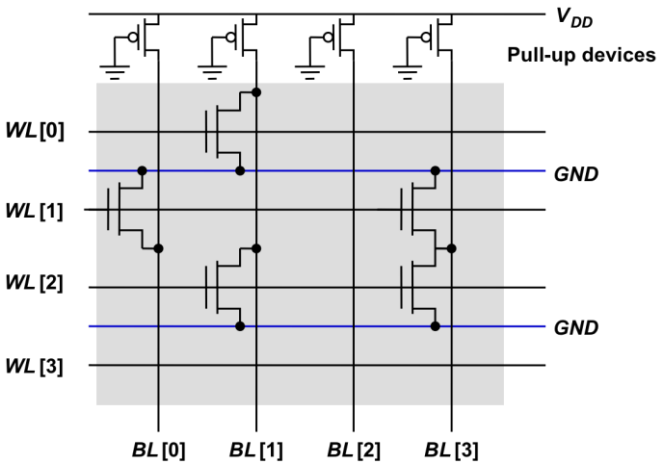



22. Given the memory cell of the figure, indicate the CORRECT answer:




[A] This is a DRAM cell with 3 transistors.
[B] Data are stored in the gate capacitance of M1 transistor.
[C] If we want to write a "1", we set BL="1", WL="1", and the capacitor CS is charged through M1pass transistor.
[D] Reading the cell do not require the precharge of BL line.

23. Determine the values ("0" or "1") of the data stored at addresses 0,1, 2 and 3 of the ROM in the following figure.



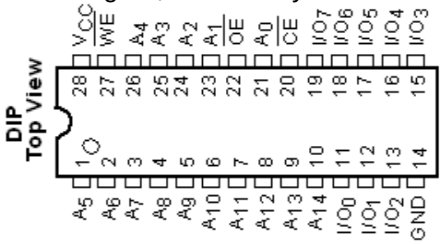

| Address | BL 0 | BL 1 | BL 2 | BL 3 |
|---|---|---|---|---|
| 0 | | | | |
| 1 | | | | |
| 2 | | | | |
| 3 | | | | |

24. Draw the basic cell of the FLASH memory and explain its non-volatility.

25. With respect to Flash type semiconductor memories, it can be stated that:

[A] The storage cell is based on FAMOS transistors, with an intermediate floating gate that is discharged when turning off the power.
[B] The number of erasing and rewriting operations is unlimited.
[C] When the floating gate of the FAMOS transistor is charged with electrons, channel formation is prevented, so that the transistor will always be in cut-off region, regardless of the voltage applied in normal gate.
[D] They are faster than static RAM memories, but slower than dynamic RAMs.

26. The integrated circuit CY62256, whose pinout is shown in the figure, is a SRAM with a typical access time of about 70ns. Analyzing the pin out of the figure, we can say that:

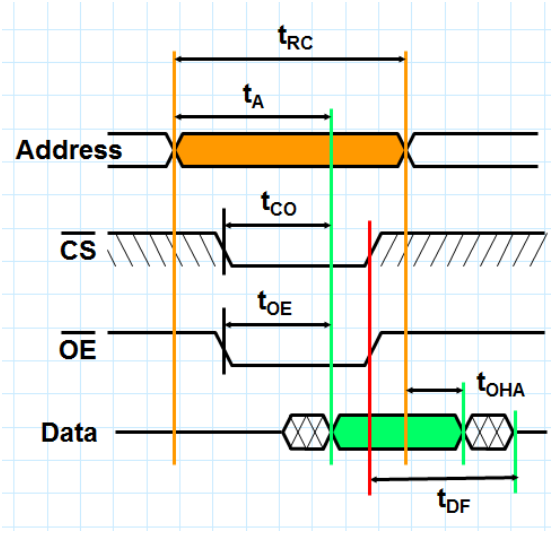



[A] The storage capacity is of 16Kbytes ($2^{14}$ words of 8 bits).
[B] 70 ns is the maximum time it takes for data to be written in the storage cells from which the address is stabilized.
[C] /CE (pin 20) corresponds to the selection of chip, so it should be maintained to '0' during any read or write operation affecting the chip.
[D] /WE allows to control the timing of the reading process, while /OE allows to control the timing of the writing process.

27. Design a Full Adder using a ROM NOR. Draw the internal structure and indicate the memory size.

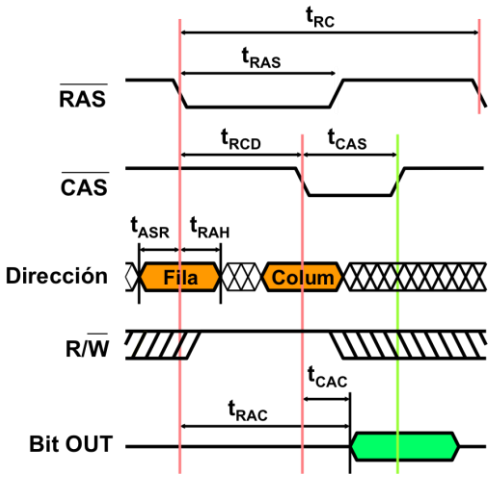
28. Taking into account the following timing diagram, indicate what is the correct statement:

[A] $t_{RC}$ is the minimum read cycle time.
[B] $t_{DF}$ is the maximum access time from the valid address.
[C] The timing diagram does not correspond to a read timing diagram, is actually a write timing diagram.
[D] The timing diagram is not complete, as Read / Write (RW) line is missing.




29. Taking into account the following timing diagram, indicate what is the correct statement:

[A] ($t_{RCD}$+$t_{CAS}$) is the minimum read cycle time.
[B] It corresponds to a read timing diagram in a DRAM memory.
[C] It corresponds to a write timing diagram in a DRAM memory.
[D] The timing diagram is not complete, as Chip Select (CS) line is missing.




30. Concerning dynamic memory refresh, indicate which is the FALSE:

[A] It is the periodic re-write operation of the DRAM information.
[B] It is done by a refresh circuit that can be independent or be inside the DRAM memory.
[C] Refresh can interfere with the memory access cycles by the CPU.
[D] In each access to the DRAM, for Read or Write, a whole column of the bit array is refreshed.