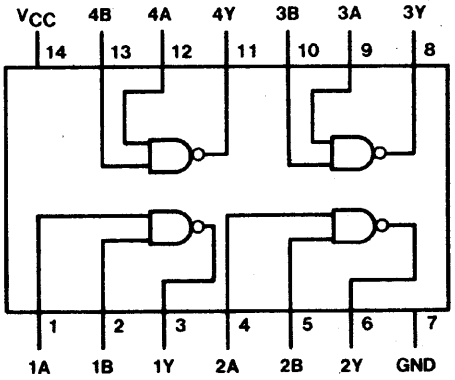
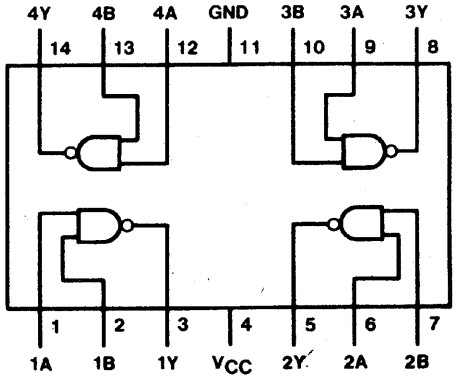
00 Quad 2-Input NAND Gates

$Y = \overline{AB}$



5400 (J)
54H00 (J)
54L00 (J,W)
54LS00 (J,W)
54S00 (J,W)

7400 (N)
74H00 (N)
74L00 (N)
74LS00 (N)
74S00 (N)

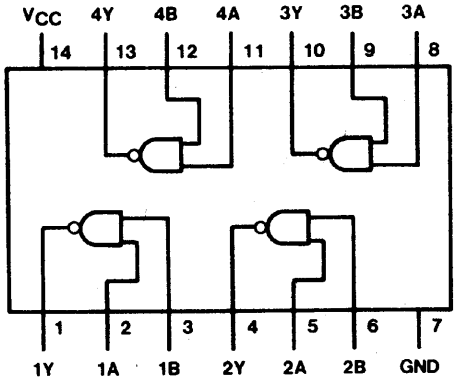


5400 (W)
54L00 (W)

See page 5-4

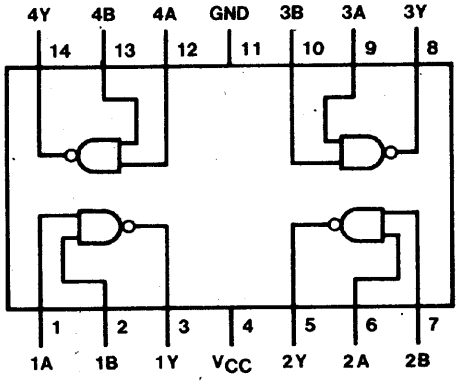
01 Quad 2-Input NAND Gates with Open-Collector Outputs

$Y = \overline{AB}$

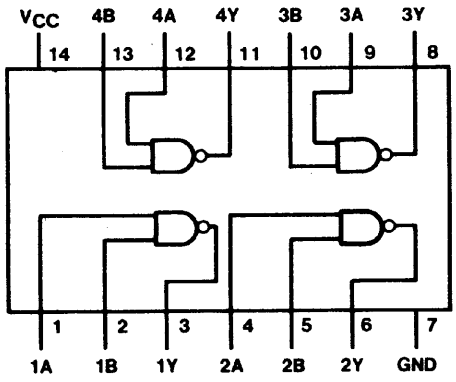


5401 (J)
54LS01 (J,W)

7401 (N)
74LS01 (N)



5401 (W)
54L01 (W)

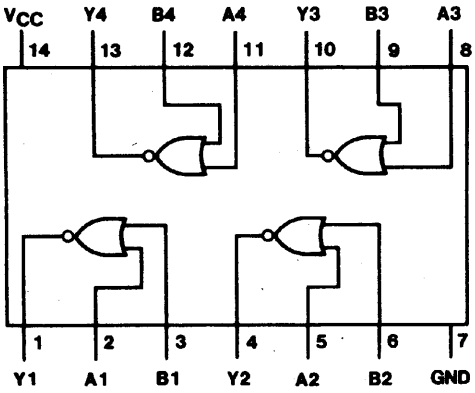


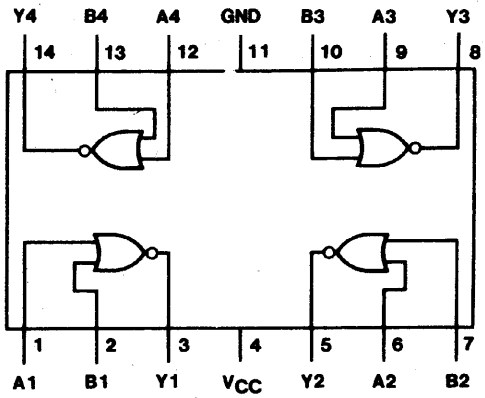
54H01 (J); 74H01 (N)

See page 5-6

02 Quad 2-Input NOR Gates

$Y = \overline{A + B}$





5402 (J)
54L02 (J)
54LS02 (J,W)
54S02 (J,W)

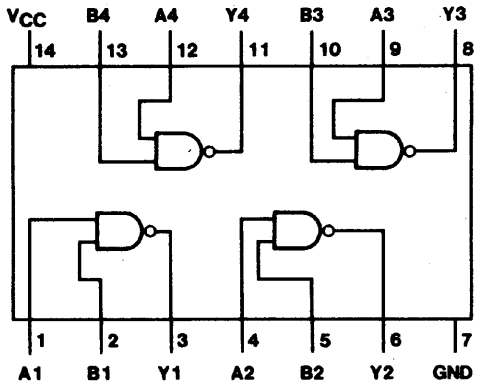
7402 (N)
74L02 (N)
74LS02 (N)
74S02 (N)

5402 (W)
54L02 (W)

See page 5-8

03 Quad 2-Input NAND Gates with Open-Collector Outputs

$Y = \overline{AB}$



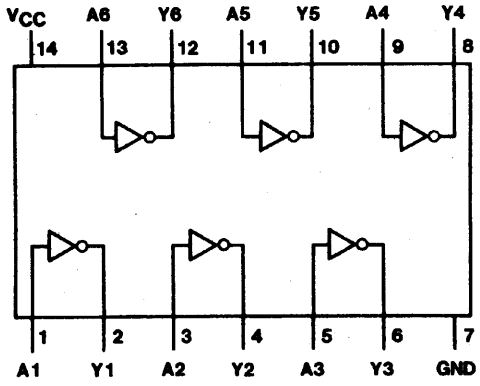
5403 (J)
54L03 (J)
54LS03 (J,W)
54S03 (J,W)

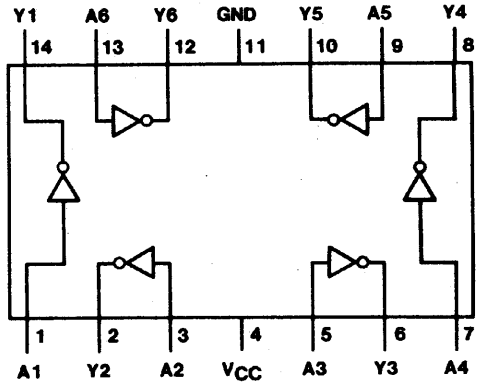
7403 (N)
74L03 (N)
74LS03 (N)
74S03 (N)

See page 5-6

04 Hex Inverters

$Y = \overline{A}$





5404 (J)
54H04 (J)
54L04 (J)
54LS04 (J,W)
54S04 (J,W)

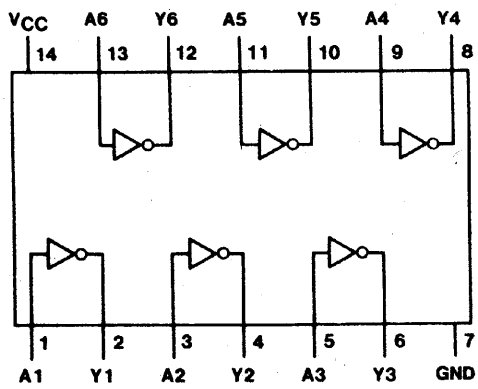
7404 (N)
74H04 (N)
74L04 (N)
74LS04 (N)
74S04 (N)

5404 (W)
54L04 (W)

See page 5-4

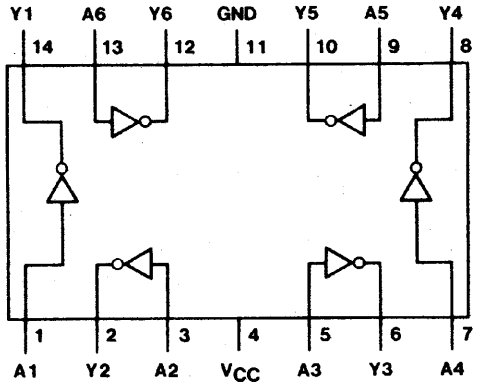
05 Hex Inverters with Open-Collector Outputs

$Y = \overline{A}$



5405 (J)
54L05 (J)
54LS05 (J,W)
54S05 (J,W)

7405 (N)
74L05 (N)
74LS05 (N)
74S05 (N)

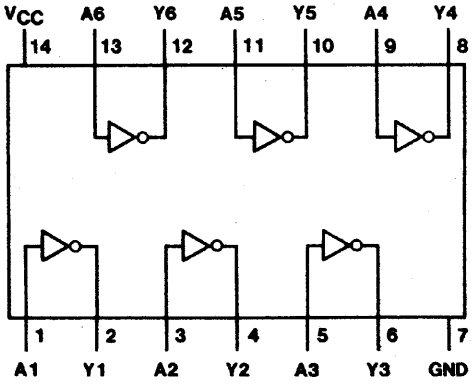


5405 (W)
54L05 (W)

See page 5-6

06 Hex Inverter Buffers with Open-Collector High Voltage Outputs

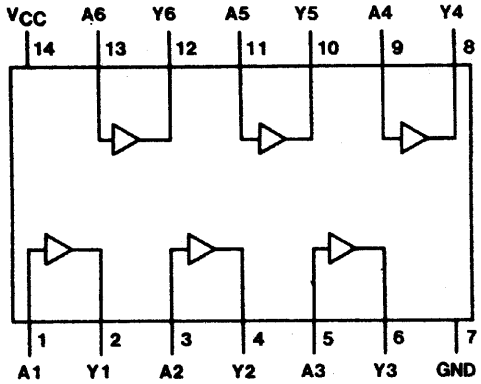
$Y = \overline{A}$



5406 (J,W); 7406 (N)

See page 5-10

07 Hex Buffers with Open-Collector High Voltage Outputs

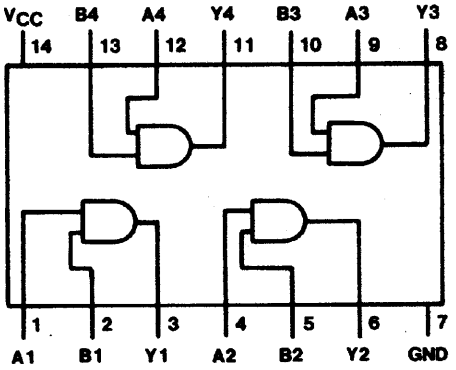


5407 (J,W); 7407 (N)

See page 5-10

08 Quad 2-Input AND Gates

$Y = AB$

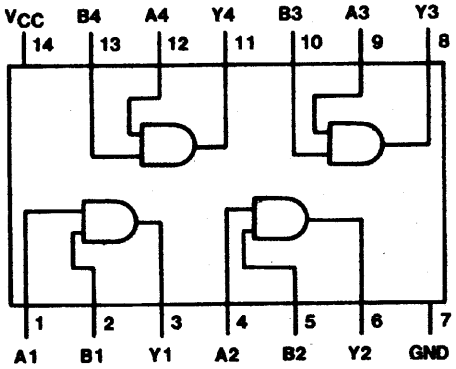


5408 (J,W)	7408 (N)
54H08 (J)	74H08 (N)
54L08 (J,W)	74L08 (N)
54LS08 (J,W)	74LS08 (N)
54S08 (J,W)	74S08 (N)

See page 5-12

09 Quad 2-Input AND Gates with Open-Collector Outputs

$Y = AB$

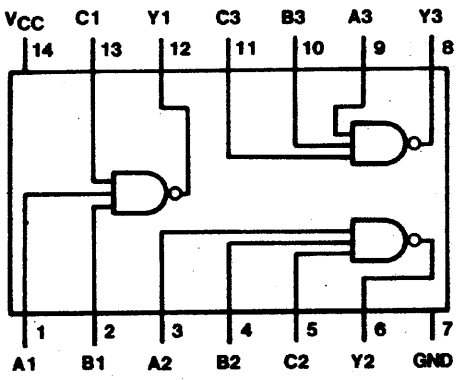


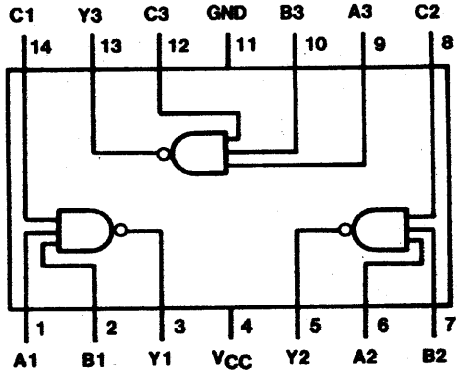
5409 (J,W)	7409 (N)
54L09 (J,W)	74L09 (N)
54LS09 (J,W)	74LS09 (N)
54S09 (J,W)	74S09 (N)

See page 5-14

10 Triple 3-Input NAND Gates

$Y = \overline{ABC}$



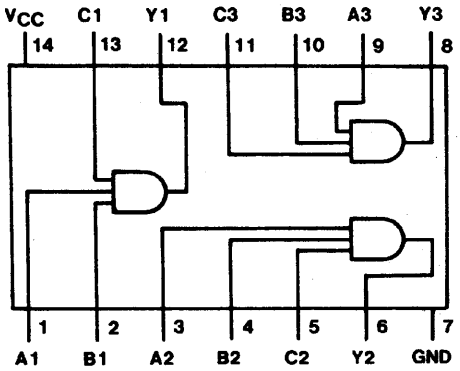


5410 (J)	7410 (N)	5410 (W)
54H10 (J)	74H10 (N)	54L10 (W)
54L10 (J)	74L10 (N)	
54LS10 (J,W)	74LS10 (N)	
54S10 (J,W)	74S10 (N)	

See page 5-4

11 Triple 3-Input AND Gates

$Y = ABC$

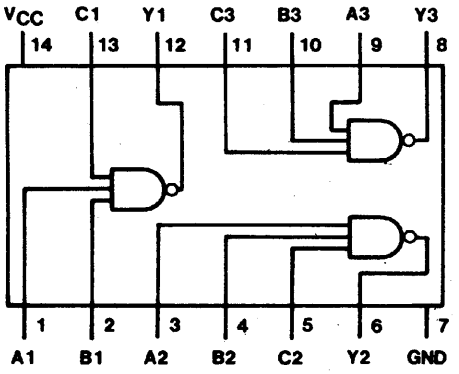


5411 (J)	7411 (N)
54H11 (J)	74H11 (N)
54L11 (J)	74L11 (N)
54LS11 (J,W)	74LS11 (N)
54S11 (J,W)	74S11 (N)

See page 5-12

12 Triple 3-Input NAND Gates with Open-Collector Outputs

$Y = \overline{ABC}$

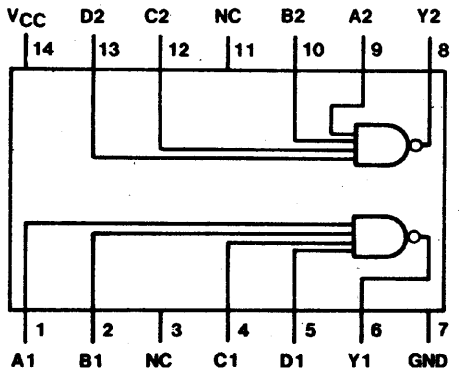


54LS12 (J,W); 74LS12 (N)

See page 5-6

13 Dual 4-Input NAND Schmitt Triggers

$Y = \overline{ABCD}$

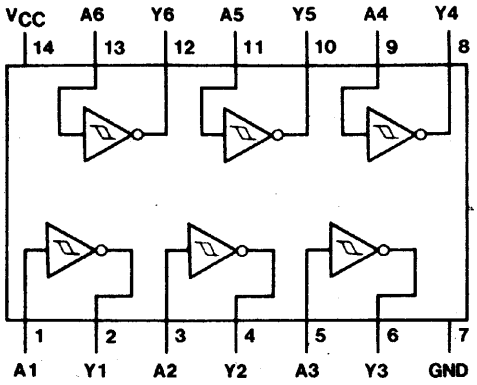


5413 (J,W)	7413 (N)
54LS13 (J,W)	74LS13 (N)

See page 5-16

14 Hex Schmitt Triggers

$Y = \overline{A}$

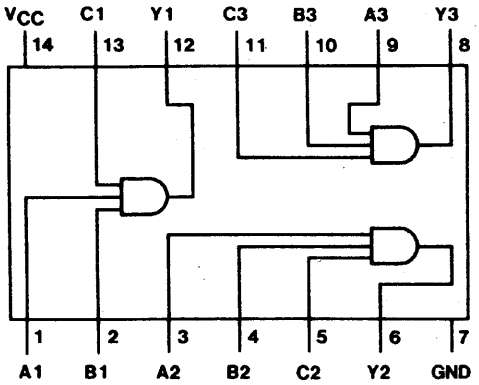


5414 (J,W) **7414 (N)**
54LS14 (J,W) **74LS14 (N)**

See page 5-16

15 Triple 3-Input AND Gates with Open-Collector Outputs

$Y = ABC$

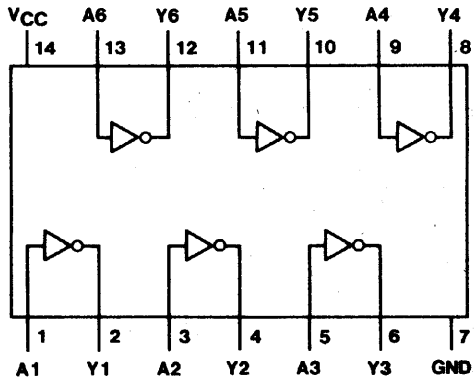


54LS15 (J,W) **74LS15 (N)**
54S15 (J,W) **74S15 (N)**

See page 5-14

16 Hex Inverter Buffers with Open-Collector High-Voltage Outputs

$Y = \overline{A}$

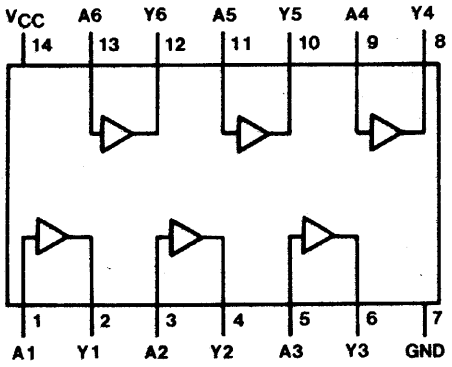


5416 (J,W); 7416 (N)

See page 5-10

17 Hex Buffers with Open-Collector High-Voltage Outputs

Y = A

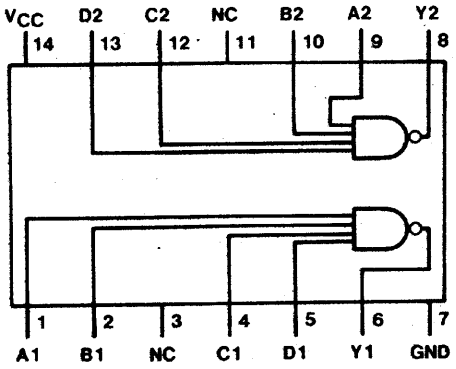


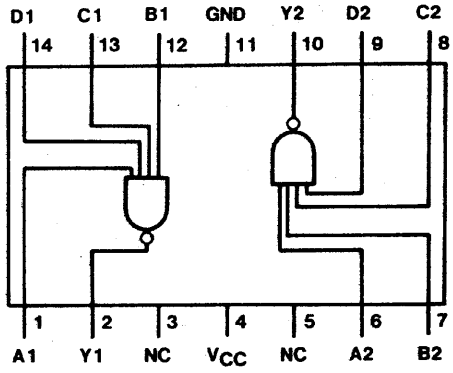
5417 (J,W); 7417 (N)

See page 5-10

20 Dual 4-Input NAND Gates

$Y = \overline{ABCD}$





5420 (J)
54H20 (J)
54L20 (J)
54LS20 (J,W)
54S20 (J,W)

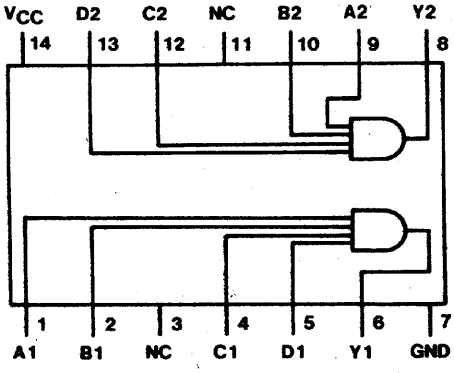
7420 (N)
74H20 (N)
74L20 (N)
74LS20 (N)
74S20 (N)

5420 (W)
54L20 (W)

See page 5-4

21 Dual 4-Input AND Gates

Y = ABCD



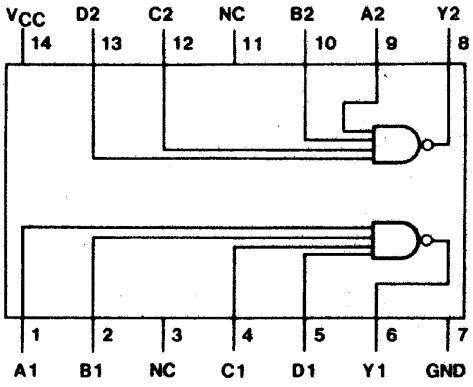
54H21 (J)
54LS21 (J,W)

74H21 (N)
74LS21 (N)

See page 5-12

22 Dual 4-Input NAND Gates with Open Collector Outputs

$Y = \overline{ABCD}$

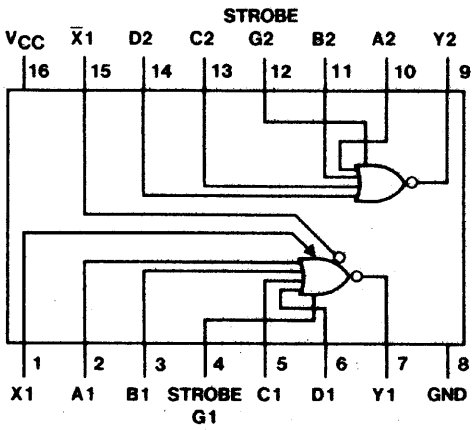


54LS22 (J,W) **74LS22 (N)**
54S22 (J,W) **74S22 (N)**

See page 5-6

23 Expandable Dual 4-Input NOR Gates with Strobe

$Y1 = \overline{G1\,(A1+B1+C1+D1)+X}$
$Y2 = \overline{G2\,(A2+B2+C2+D2)}$
X = output of 5460/7460

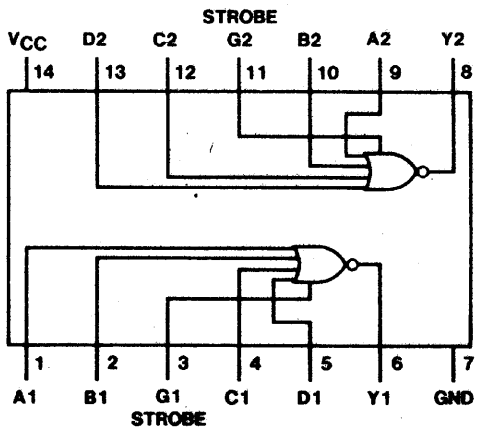


5423 (J,W); 7423 (N)

See page 5-18

25 Dual 4-Input NOR Gates with Strobe

$Y = \overline{G(A+B+C+D)}$

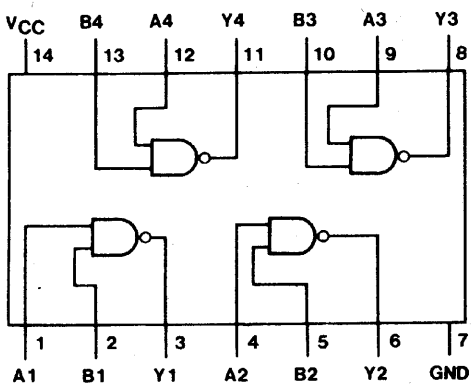


5425 (J,W); 7425 (N)

See page 5-8

26 Quad 2-Input High-Voltage NAND Gates

$Y = \overline{AB}$



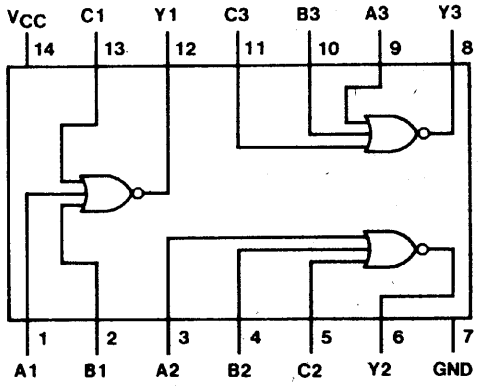
5426 (J)
54L26 (J)
54LS26 (J,W)

7426 (N)
74L26 (N)
74LS26 (N)

See page 5-10

27 Triple 3-Input NOR Gates

$Y = \overline{A+B+C}$



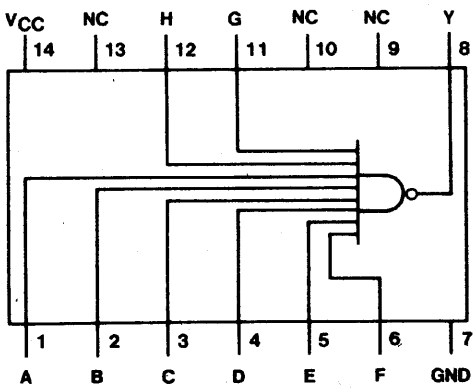
5427 (J,W)
54LS27 (J,W)

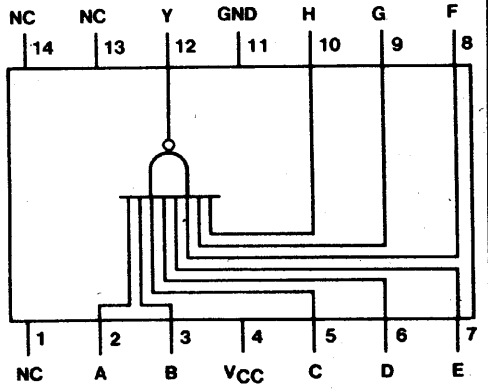
7427 (N)
74LS27 (N)

See page 5-8

30 8-Input NAND Gates

$Y = \overline{ABCDEFGH}$





5430 (J)
54H30 (J)
54L30 (J)
54LS30 (J,W)
54S30 (J,W)

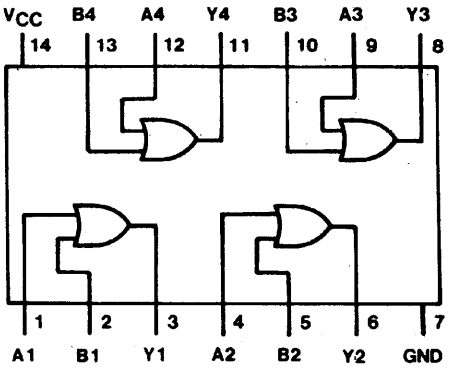
7430 (N)
74H30 (N)
74L30 (N)
74LS30 (N)
74S30 (N)

5430 (W)
54L30 (W)

See page 5-4

32 Quad 2-Input OR Gates

$Y = A + B$

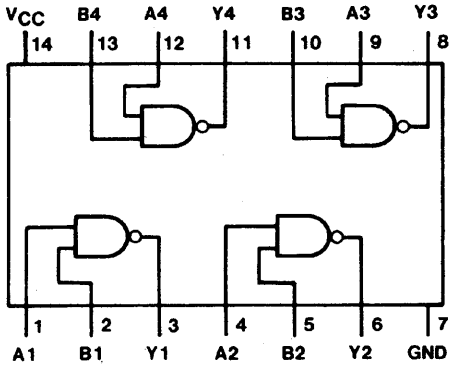


5432 (J,W) **7432 (N)**
54L32 (J,W) **74L32 (N)**
54LS32 (J,W) **74LS32 (N)**
54S32 (J,W) **74S32 (N)**

See page 5-20

37 Quad 2-Input NAND Buffers

$Y = \overline{AB}$

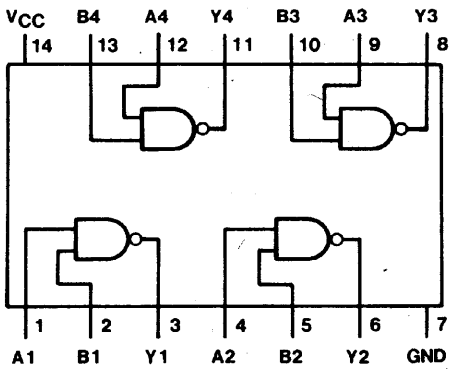


5437 (J,W) **7437 (N)**
54LS37 (J,W) **74LS37 (N)**

See page 5-22

38 Quad 2-Input NAND Buffers with Open-Collector Outputs

$Y = \overline{AB}$

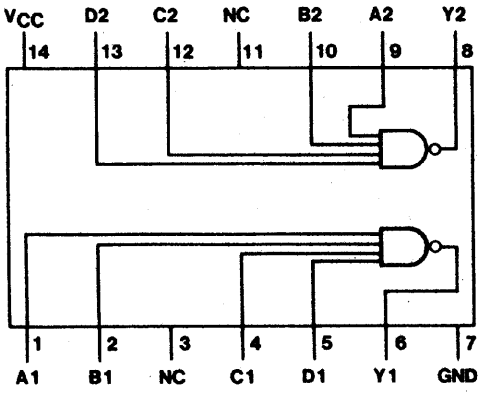


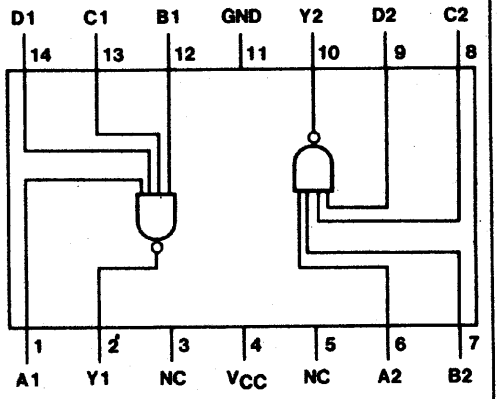
5438 (J,W) **7438 (N)**
54LS38 (J,W) **74LS38 (N)**

See page 5-10

40 Dual 4-Input NAND Buffers

$Y = \overline{ABCD}$





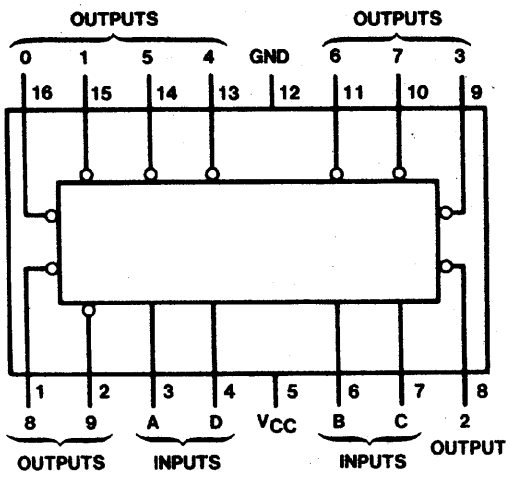
5440 (J)
54H40 (J)
54LS40 (J,W)
54S40 (J,W)

7440 (N)
74H40 (N)
74LS40 (N)
74S40 (N)

5440 (W)

See page 5-22

41 Nixie Driver

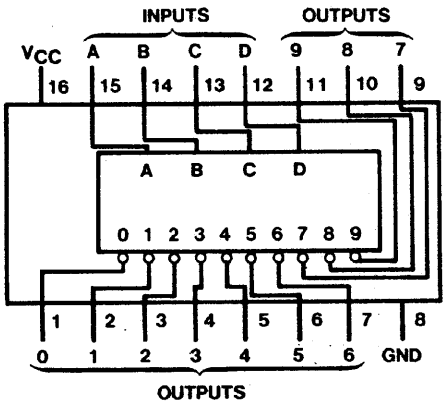


5441A (J,W); 7441A (N)

See page 6-4

4 Line-to-10-Line Decoder

42 BCD-to-Decimal



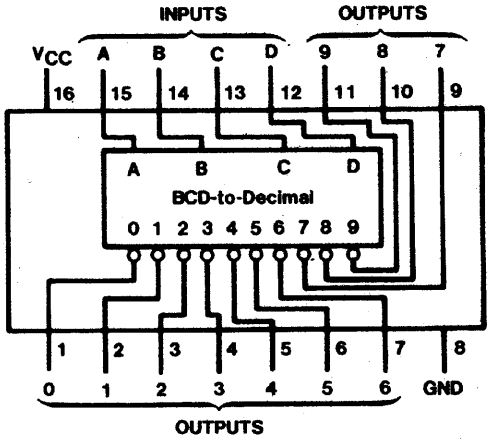
5442A (J,W)
54L42A (J,W)
54LS42 (J,W)

7442A (N)
74L42A (N)
74LS42 (N)

See page 6-7

BCD-to-Decimal Decoder/Driver

45 Lamp, Relay, or MOS Driver
80-mA Current Sink
Outputs Off for Invalid Codes



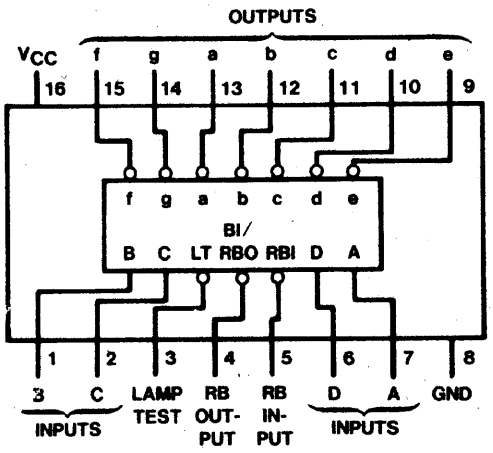
5445 (J,W); 7445 (N)

See page 6-10

BCD-to-Seven-Segment Decoders/Drivers

46 Active-Low, Open-Collector, 30-V Outputs

47 Active-Low, Open-Collector, 15-V Outputs

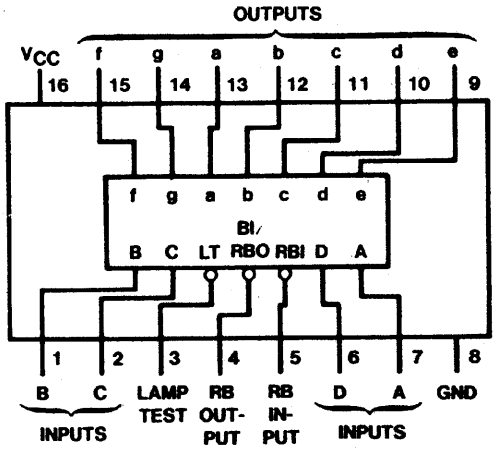


5446A (J,W)	7446A (N)
5447 (J,W)	7447A (N)
54LS47 (J,W)	74LS47 (N)

See page 6-12

BCD-to-Seven-Segment Decoders/Drivers

48 Internal Pull-Up Outputs

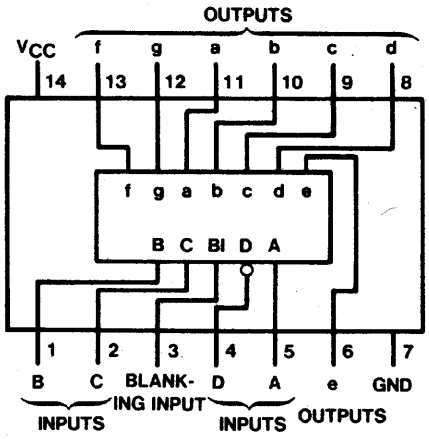


5448 (J,W)	7448 (N)
54LS48 (J,W)	74LS48 (N)

See page 6-12

BCD-to-Seven-Segment Decoders/Drivers

49 Open-Collector Outputs



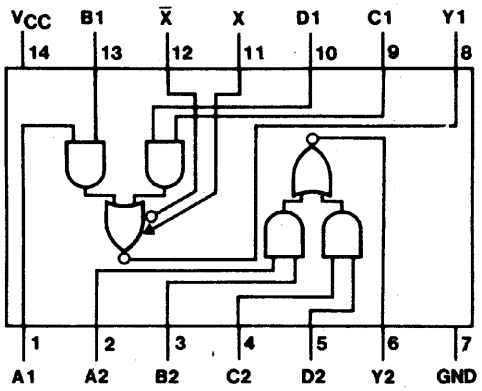
54LS49 (J,W); 74LS49 (N)

See page 6-12

50 Dual 2-Wide, 2-Input, AND-OR-INVERT Gates

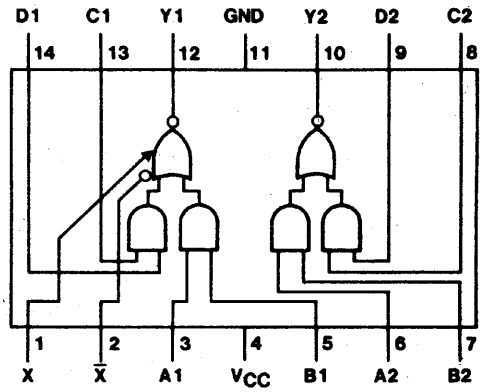
$Y = \overline{AB+CD+X}$

50: X = output of 5460/7460



5450 (J)
54H50 (J)

7450 (N)
74H50 (N)

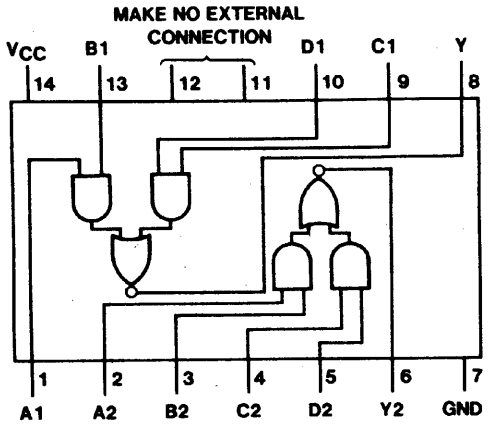


5450 (W)

See page 5-18

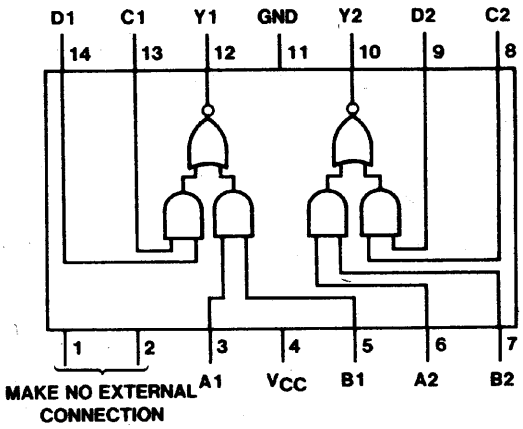
51 Dual 2-Wide, 2-Input AND-OR-INVERT Gates

51, S51
$Y = \overline{AB+CD}$



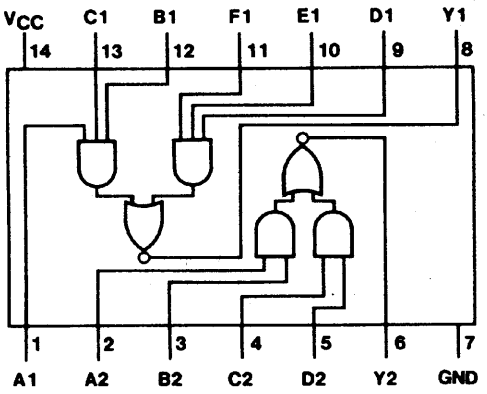
5451 (J)
54S51 (J,W)

7451 (N)
74S51 (N)



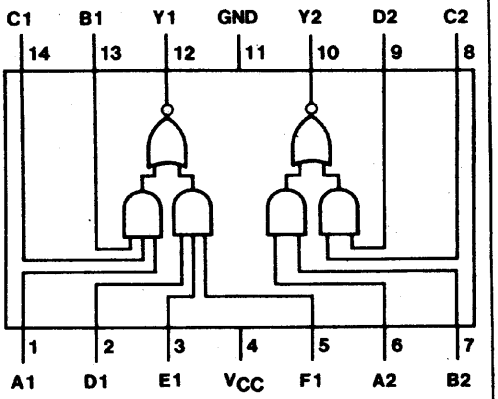
5451 (W)

L51, LS51
$Y1 = \overline{(A1xB1xC1) + (D1xE1xF1)}$
$Y2 = \overline{(A2xB2) + (C2xD2)}$



54L51 (J)
54LS51 (J,W)

74L51 (N)
74LS51 (N)



54L51 (W)

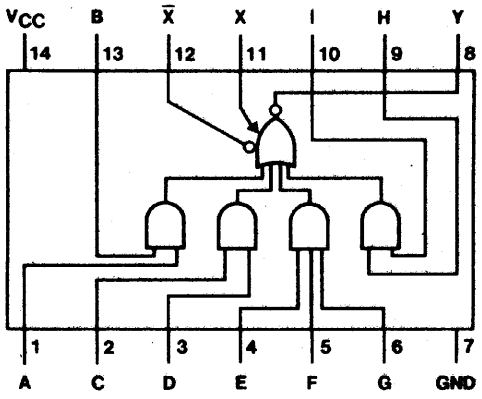
See page 5-24

53 Expandable 4-Wide AND-OR-INVERT Gates

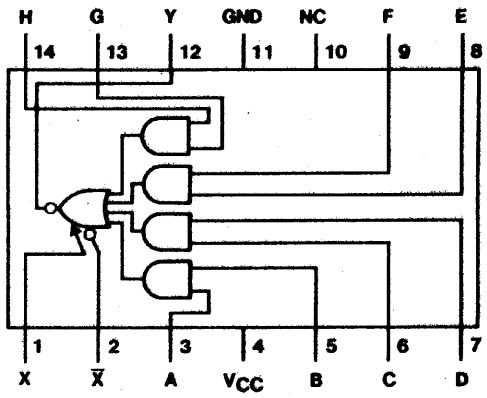
53

$Y = \overline{AB+CD+EF+GH+X}$

X = output of 5460/7460



5453 (J); 7453 (N)

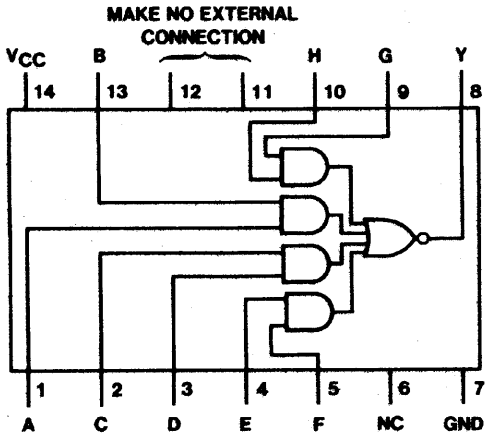


5453 (W)

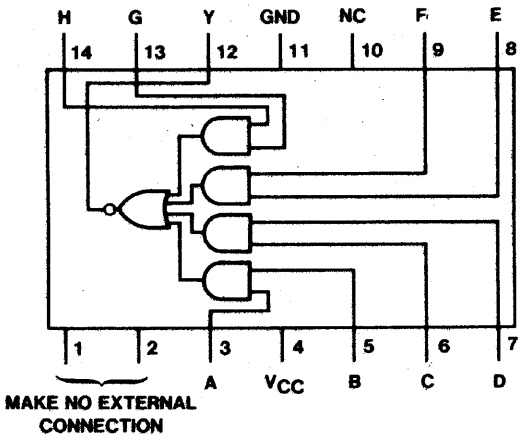
See page 5-18

54 4-Wide AND-OR-INVERT Gates

54
$Y = \overline{AB+CD+EF+GH}$

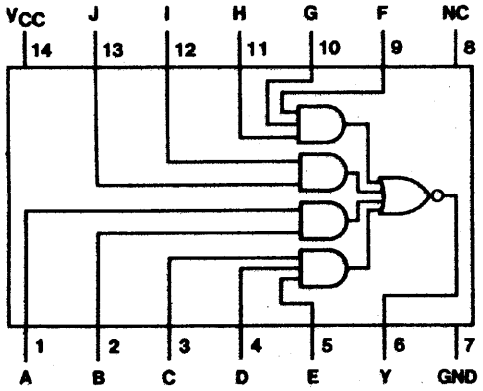


5454 (J); 7454 (N)



5454 (W)

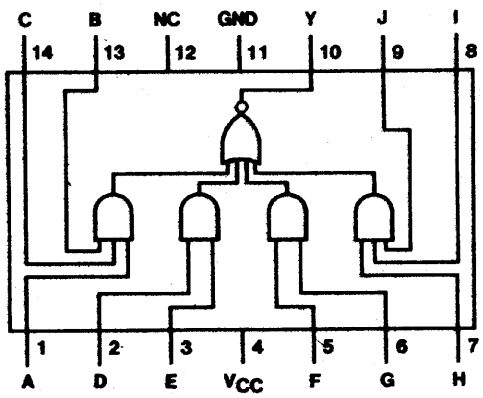
L54, LS54
$Y = \overline{AB+CDE+FGH+IJ}$



54L54 (J)
54LS54 (J,W)

74L54 (N)
74LS54 (N)

L54
$Y = \overline{ABC+DE+FG+HIJ}$

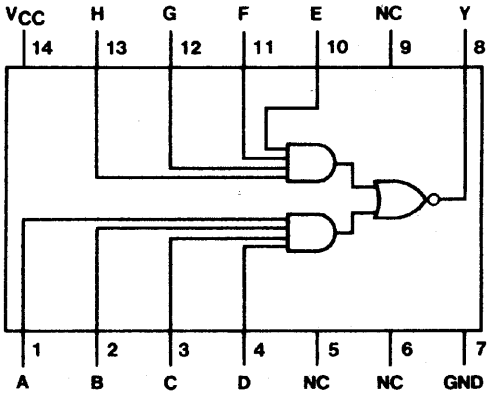


54L54 (W)

See page 5-24

55 2-Wide, 4-Input AND-OR-INVERT Gates

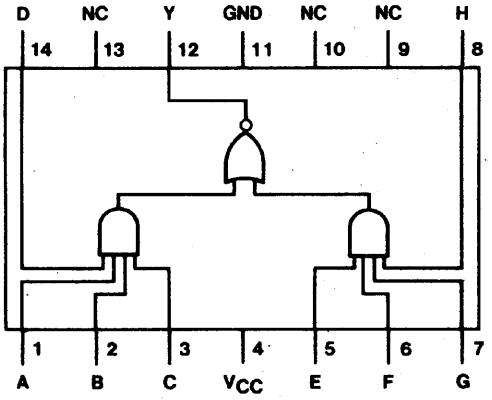
L55, LS55
$Y = \overline{ABCD+EFGH}$



54L55 (J)
54LS55 (J,W)

74L55 (N)
74LS55 (N)

L55
$Y = \overline{ABCD+EFGH}$

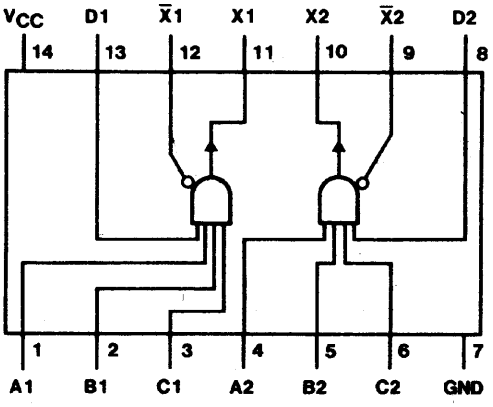


54L55 (W)

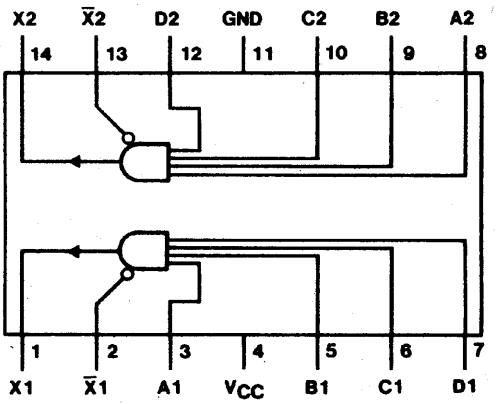
See page 5-24

60 Dual 4-Input Expanders

X = ABCD when connected to X and $\overline{X}$ inputs of 5423/7423, 5450/7450 or 5453/7453



5460 (J); 7460 (N)

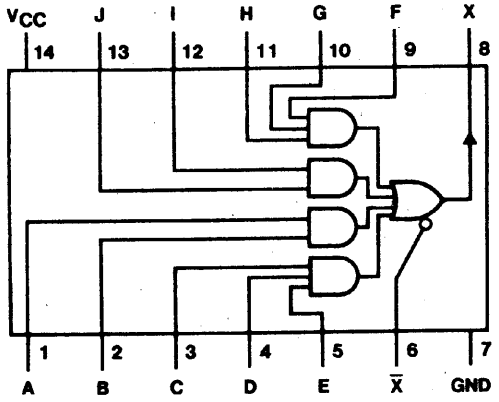


5460 (W)

See page 5-26

62 4-Wide AND-OR Expander

$X = AB+CDE+FGH+IJ$ when connected to X and $\overline{X}$ inputs of 54H50/74H50

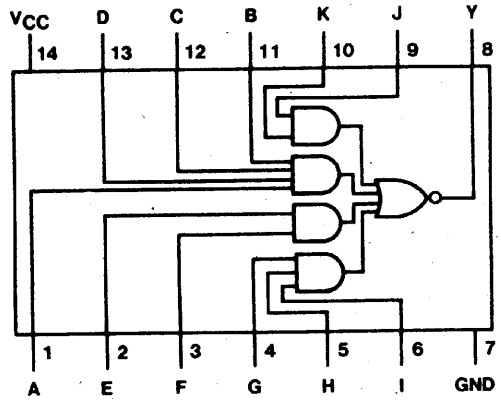


54H62 (J); 74H62 (N)

See page 5-27

64 4-Wide AND-OR-INVERT Gates

$Y = \overline{ABCD+EF+GHI+JK}$

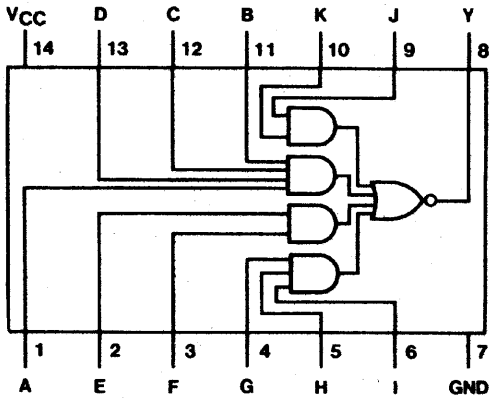


54S64 (J,W); 74S64 (N)

See page 5-24

65 4-Wide AND-OR-INVERT Gates with Open-Collector Outputs

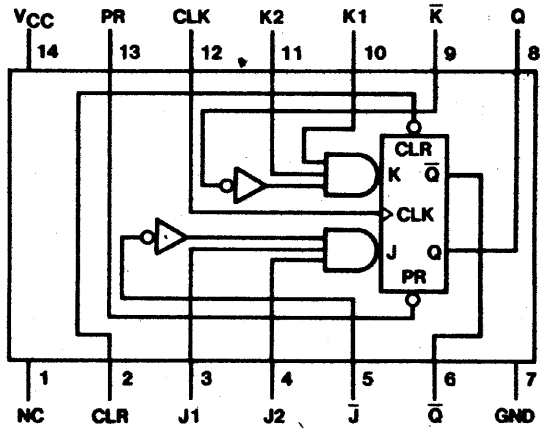
$Y = \overline{ABCD+EF+GHI+JK}$



54S65 (J,W); 74S65 (N)

See page 5-28

70 AND-Gated J-K Positive-Edge-Triggered Flip-Flops with Preset and Clear



5470 (J); 7470 (N)

Truth Table

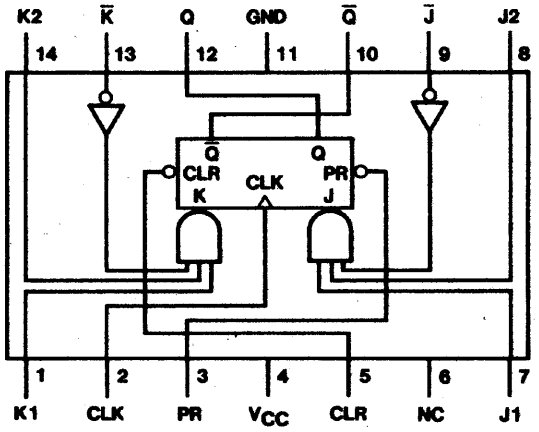
Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	L	X	X	H	L
H	L	L	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	Q0	$\overline{Q}$0
H	H	↑	H	L	H	L
H	H	↑	L	H	L	H
H	H	↑	H	H	TOGGLE	
H	H	L	X	X	Q0	$\overline{Q}$0

$J = J1 \cdot J2 \cdot \overline{J}$
$K = K1 \cdot K2 \cdot \overline{K}$

If inputs J and $\overline{K}$ are not used, they must be grounded.

Preset or Clear Function can occur only when clock input is low.

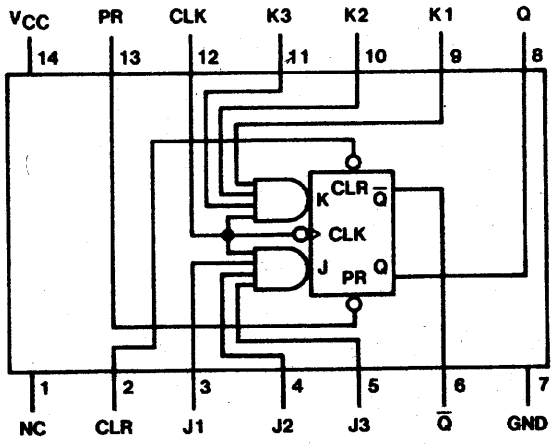
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level



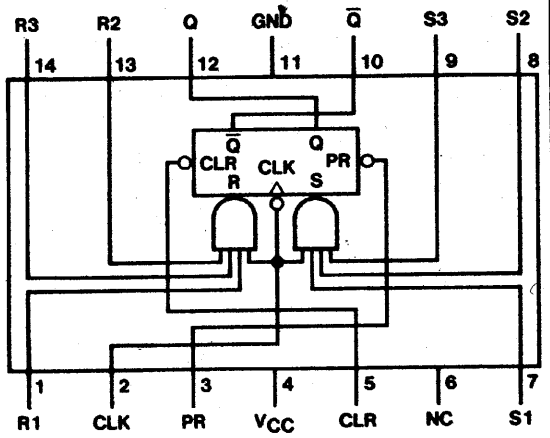
5470 (W)

See page 5-29

71 AND-OR-Gated J-K Master-Slave Flip-Flops with Preset



54L71 (J); 74L71 (N)



54L71 (W)

Truth Table

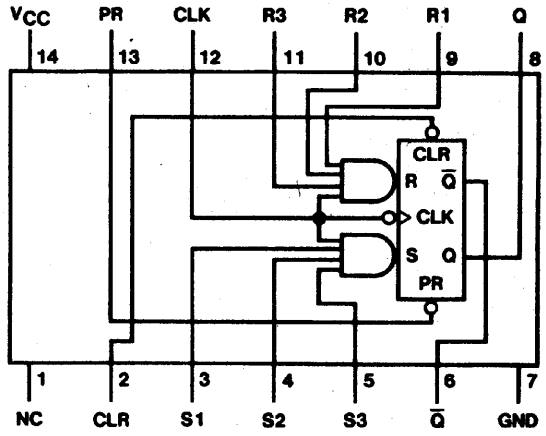
Inputs					Outputs	
PR	CLR	CLK	S	R	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍⎍	L	L	Q0	$\overline{Q}$0
H	H	⎍⎍	H	L	H	L
H	H	⎍⎍	L	H	L	H
H	H	⎍⎍	H	H	INDETER-MINATE	

R = R1 · R2 · R3
S = S1 · S2 · S3

See page 5-31

⎍⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

72 AND-Gated J-K Master-Slave Flip-Flops with Preset and Clear



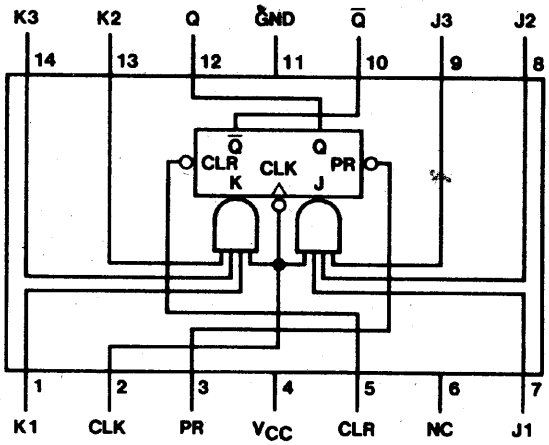
5472 (J)
54L72 (J)

7472 (N)
74L72 (N)

Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓	L	L	Q0	$\overline{Q}$0
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	

J = J1 · J2 · J3
K = K1 · K2 · K3



5472 (W); 54L72 (W)

See page 5-29 (72), 5-31 (L72)

73 Dual J-K Flip-Flops with Clear

Truth Table

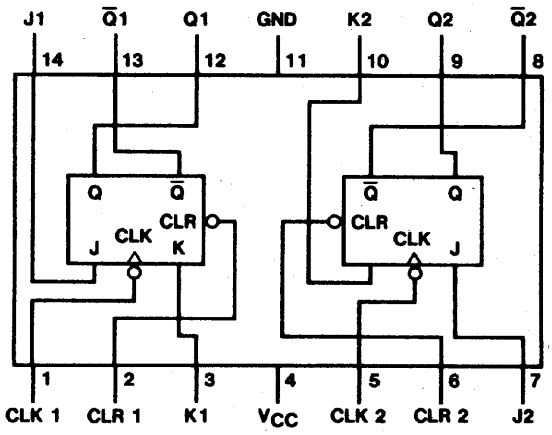
73, L73

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⊓	L	L	Q0	$\overline{Q}$0
H	⊓	H	L	H	L
H	⊓	L	H	L	H
H	⊓	H	H	TOGGLE	

Truth Table

LS73A

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0



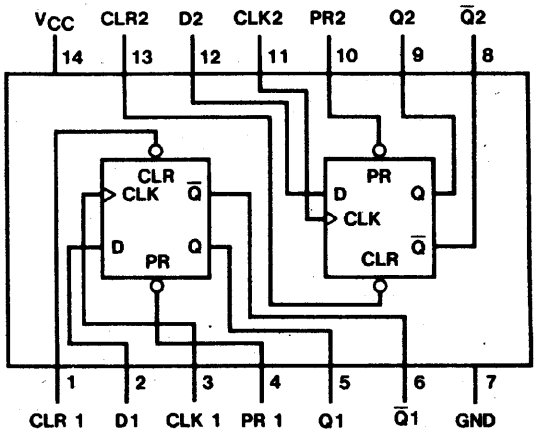
5473 (J,W)
54L73 (J,W)
54LS73 (J,W)

7473 (N)
74L73 (N)
74LS73 (N)

See page 5-29 (73), 5-31 (L73), 5-33 (LS73)

Notes: ⊓ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to ouput on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

74 Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear

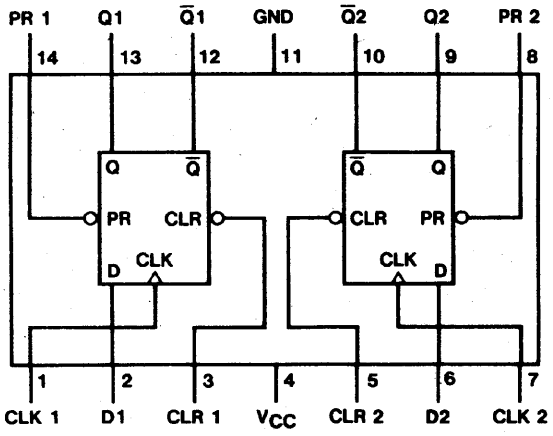


5474 (J) **7474 (N)**
54H74 (J) **74H74 (N)**
54L74 (J) **74L74 (N)**
54LS74A (J,W) **74LS74A (N)**
54S74 (J,W) **74S74 (N)**

Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

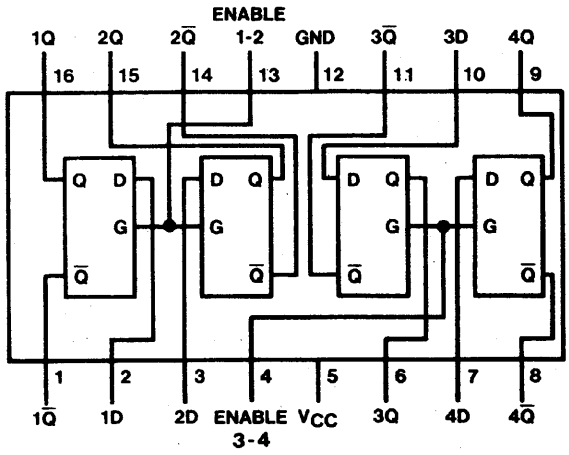
Notes: Q0 = the level of Q before the indicated input conditions were established.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



5474 (W); 54L74 (W)

See page 5-29 (74), 5-38 (H74), 5-31 (L74), 5-33 (LS74A), 5-35 (S74)

75 4-Bit Bistable Latches



5475 (J,W) **7475 (N)**
54L75A (J,W) **74L75A (N)**
54LS75 (J,W) **74LS75 (N)**

Truth Table
(Each Latch)

Inputs		Outputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G

See page 6-18

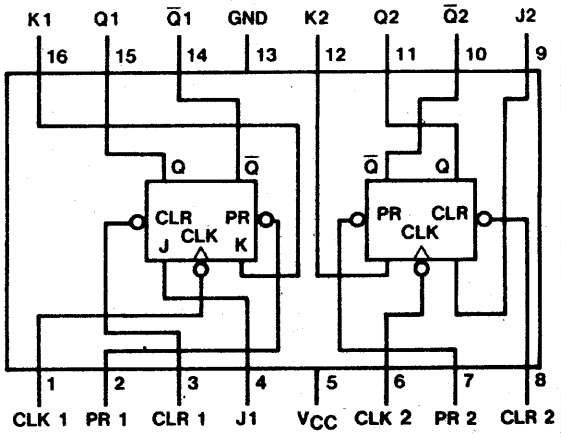
76 Dual J-K Flip-Flops with Preset and Clear

Truth Table
76, H76

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓	L	L	Q0	$\overline{Q}$0
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	

Truth Table
LS76

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0



5476 (J,W)
54LS76A (J,W)

7476 (N)
74LS76A (N)

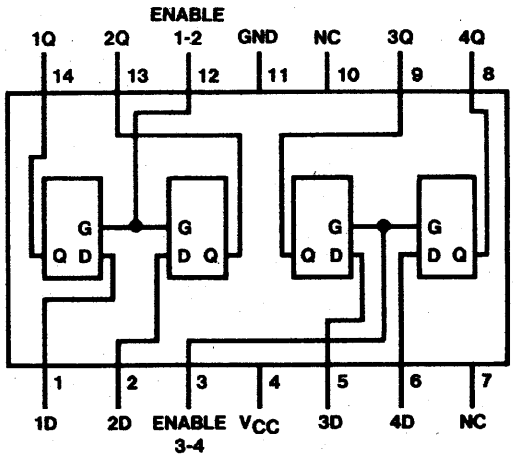
See page 5-29 (76), 5-33 (LS76A)

77 4-Bit Bistable Latches

Truth Table
(Each Latch)

Inputs		Outputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}$0

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transistion of G



54LS77 (W); 74LS77 (W)

See page 6-18

Notes: ⊓ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

78 Dual J-K Flip-Flops with Preset, Common Clear, and Common Clock

Truth Table

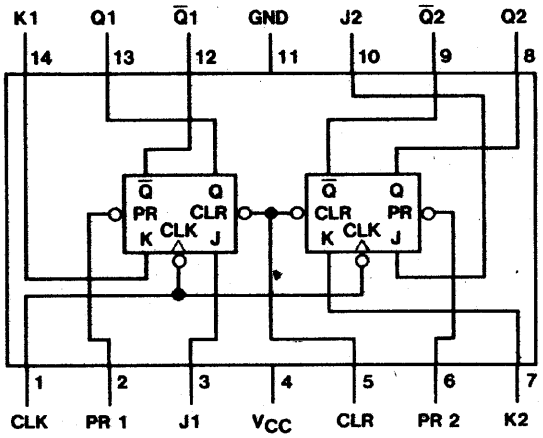
L78

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q0	$\overline{Q}$0
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

Truth Table

LS78

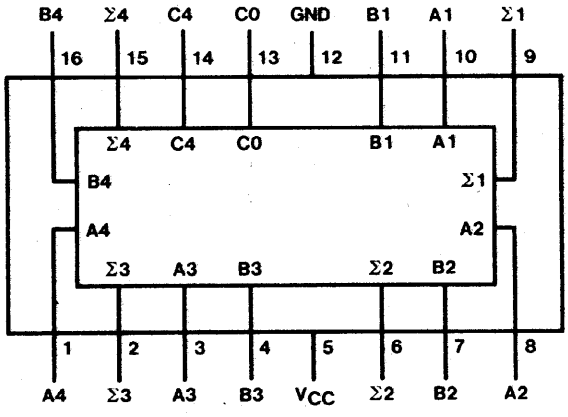
Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0



54L78 (J,W) 74L78 (N)
54LS78A (J,W) 74LS78A (N)

See page 5-31 (L78), 5-33 (LS78A)

83 4-Bit Binary Full Adders With Fast Carry

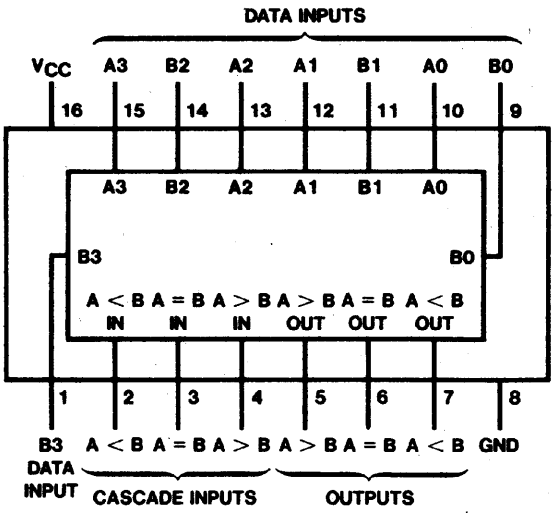


5483 (J,W) 7483 (N)
54LS83A (J,W) 74LS83A (N)

See page 6-21

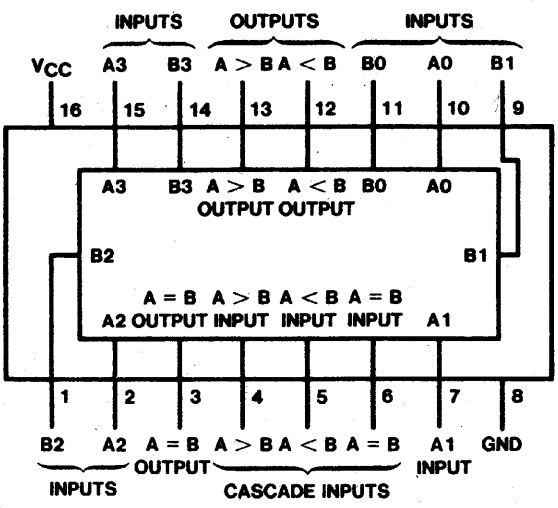
Notes: ⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

85 4-Bit Magnitude Comparators



5485 (J,W)
54LS85 (J,W)

7485 (N)
74LS85 (N)



54L85 (J,W); 74L85 (N)

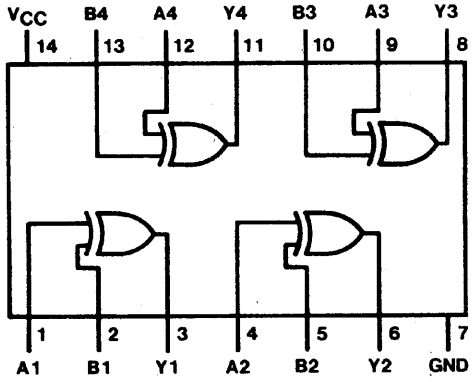
See page 6-27

86 Quad 2-Input EXCLUSIVE-OR Gates

Truth Table
(86,L86, LS86, S86)

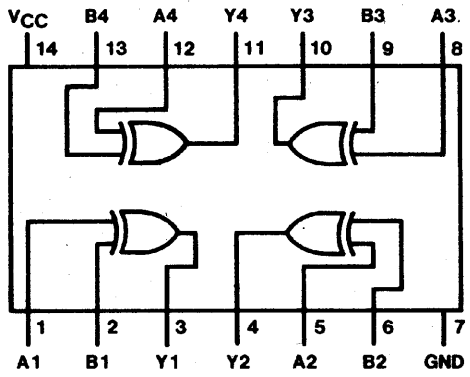
Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

$Y = A \oplus B = \overline{A}B + A\overline{B}$

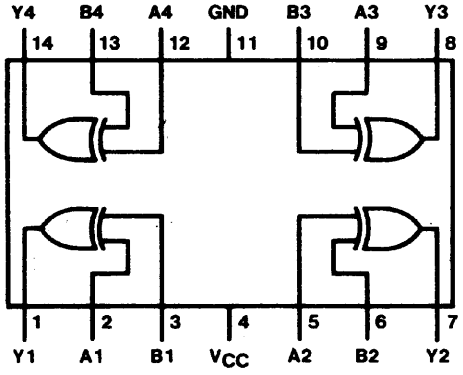


5486 (J,W)
54LS86 (J,W)
54S86 (J,W)

7486 (N)
74LS86 (N)
74S86 (N)



54L86 (J); 74L86 (N)

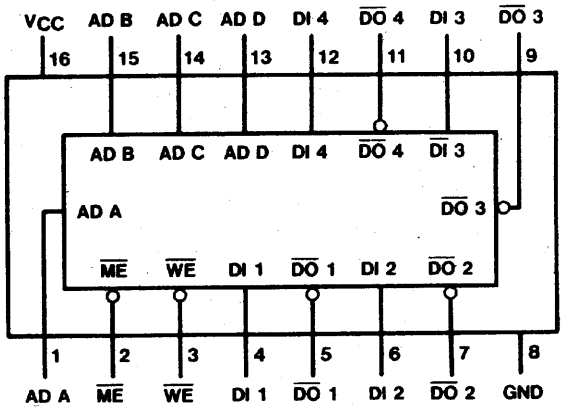


54L86 (W)

See page 5-40

64-Bit Read/Write Memories

89 16 4-Bit Words



5489B (J) 7489B (N)
54L89A (J) 74L89A (N)

See page 6-33

Decade Counters

90 Divide-By-Two and Divide-By-Five

'90A, 'L90, 'LS90
BCD Count Sequence
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

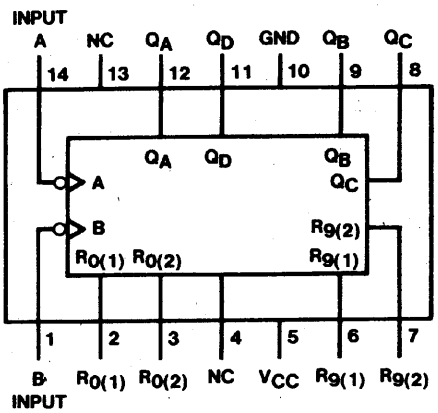
'90A, 'L90, 'LS90
Bi-Quinary (5-2)
(See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Note A: Output Q_A is connected to input B for BCD count.
Note B: Output Q_D is connected to input A for bi-quinary count.

'90A, 'L90, 'LS90
Reset/Count Function Table

Reset Inputs				Output			
$R_{O(1)}$	$R_{O(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			



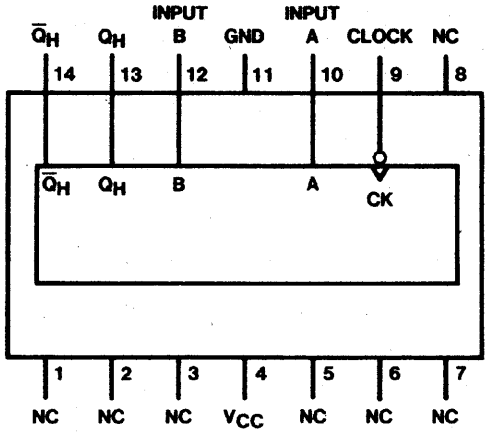
5490A (J,W) 7490A (N)
54L90 (J,W) 74L90 (N)
54LS90 (J,W) 74LS90 (N)

NC—No internal connection (54LS90/74LS90)
NC—make no external connection (5490A/7490A) (54L90/74L90)

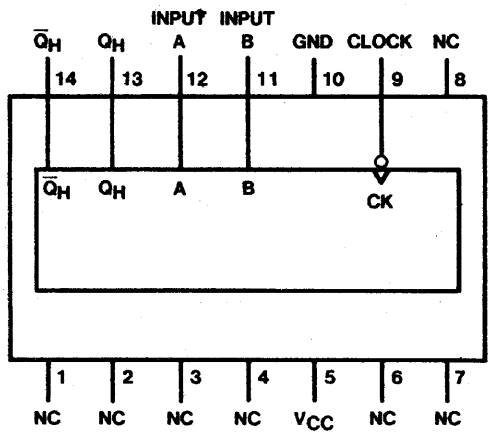
See page 6-36

8-Bit Shift Registers

91 Serial-In, Serial-Out Gated Input



54L91 (W)



54L91 (J); 74L91 (N)

NC—make no external connection

Truth Table

Inputs AT t_n		Outputs AT t_{n+8}	
A	B	Q_H	$\overline{Q}_H$
H	H	H	L
L	X	L	H
X	L	L	H

H = high, L = low
X = irrelevant
t_n = Reference bit time, clock low
t_{+8} = Bit time after 8 low-to-high clock transitions

See page 6-42

Divide-By-Twelve Counters

92 Divide-By-Two and Divide-By-Six

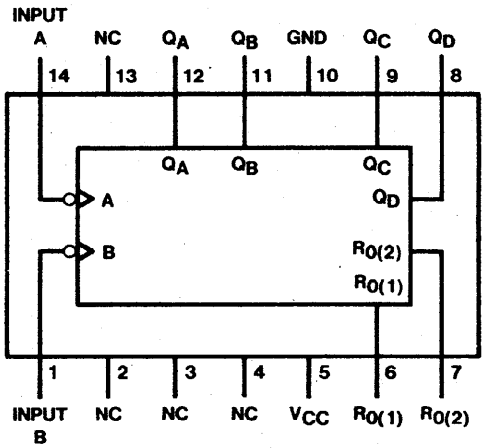
'92A, 'LS92
Count Sequence
(See Note C)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

C. Output Q_A is connected to input B.

'92A, 'LS92,
Reset/Count Function Table

Reset Inputs		Output			
$R_{O(1)}$	$R_{O(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			



5492A (J,W) 7492A (N)
54LS92 (J,W) 74LS92 (N)

NC—No internal connection (54LS92/74LS92)
NC—Make no external connection (5492A/7492A)

See page 6-36

4-Bit Binary Counters

93 Divide-By-Two and Divide-By-Eight

'93A, 'L93, 'LS93
Count Sequence
(See Note C)

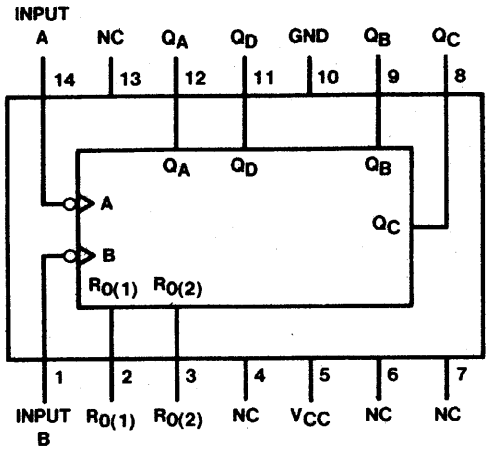
Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

'93A, 'L93, 'LS93
Reset/Count Function Table

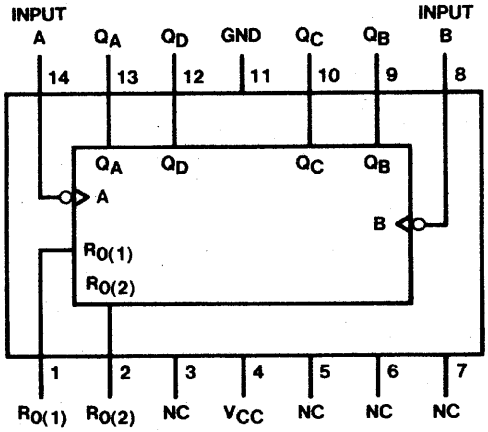
Reset Inputs		Output			
$R_{O(1)}$	$R_{O(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

C. Output Q_A is connected to input B.

See page 6-36



5493A (J,W) **7493A (N)**
54LS93 (J,W) **74LS93 (N)**



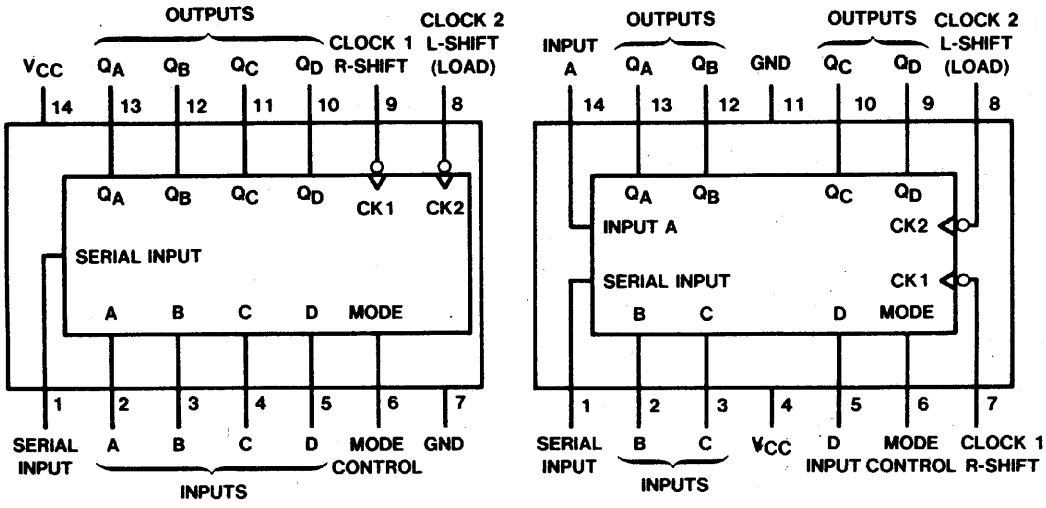
54L93 (J,W); 74L93 (N)

NC—No internal connection (54LS93/74LS93)
NC—Make no external connection (5493A/7493A) (54L93/74L93)

3

4-Bit Shift Registers

95 Parallel In/Parallel Out Shift Right, Shift Left Serial Input



5495 (J,W); 7495 (N)

54L95 (J,W); 74L95 (N)

See page 6-44

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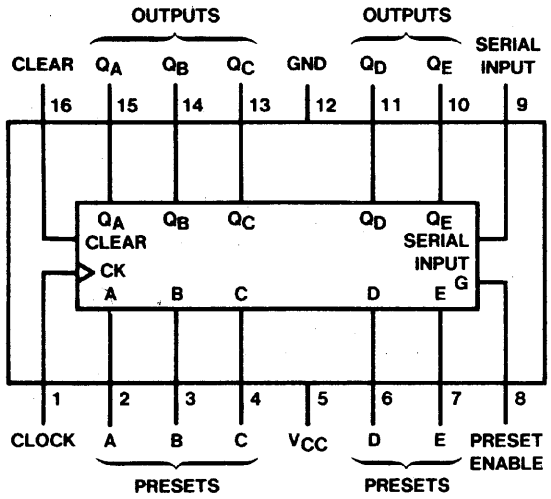
96 5-Bit Shift Register Asynchronous Preset

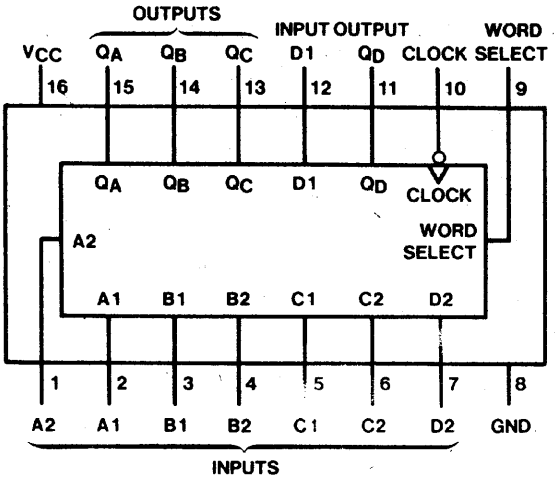


5496 (J,W); 7496 (N)

See page 6-47

4-Bit Data Selector/Storage Registers

98 Selects 1 of 2 4-Bit Words Parallel In/Out



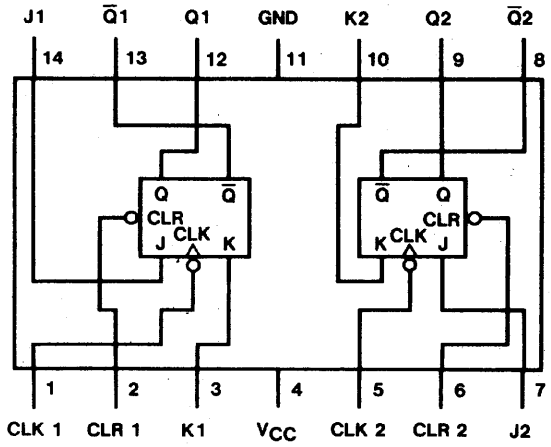
54L98 (J); 74L98 (N)

See page 6-51

103 Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

Truth Table

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0



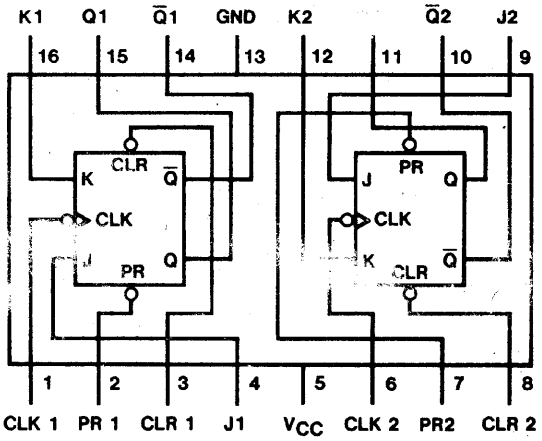
54H103 (J); 74H103 (N)

See page 5-42

106 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

Truth Table

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0



54H106 (J); 74H106 (N)

See page 5-42

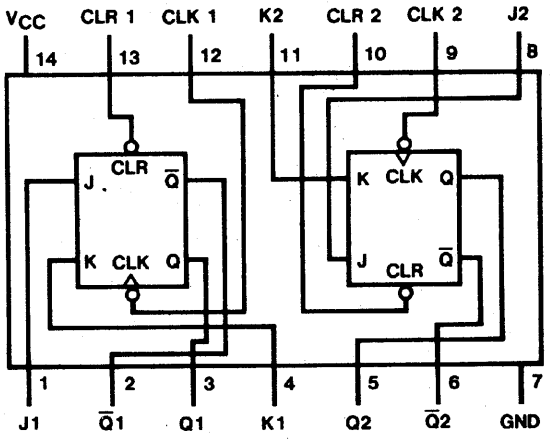
107 Dual J-K Master-Slave Flip-Flops with Clear

Truth Table
107

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q0	$\overline{Q}$0
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

Truth Table
LS107A

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0



54107 (J)
54LS107A (J,W)

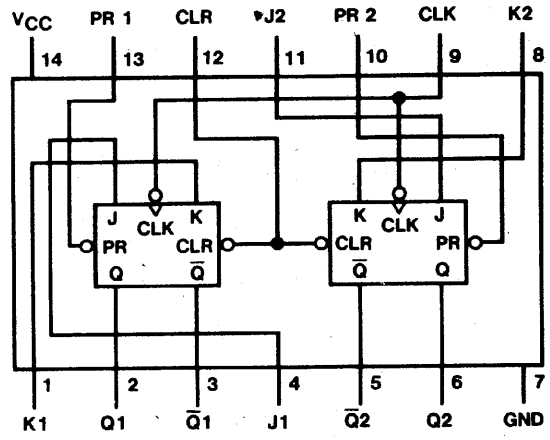
74107 (N)
74LS107A (N)

See page 5-29 (107), 5-33 (LS107A)

108 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset, Common Clear, and Common Clock

Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0



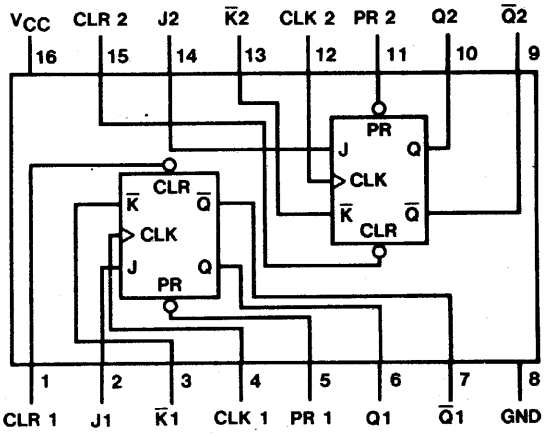
54H108 (J); 74H108 (N)

See page 5-42

109 Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flops with Preset and Clear

Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q0	$\overline{Q}$0
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q}$0



54109 (J,W)
54LS109 (J,W)

74109 (N)
74LS109 (N)

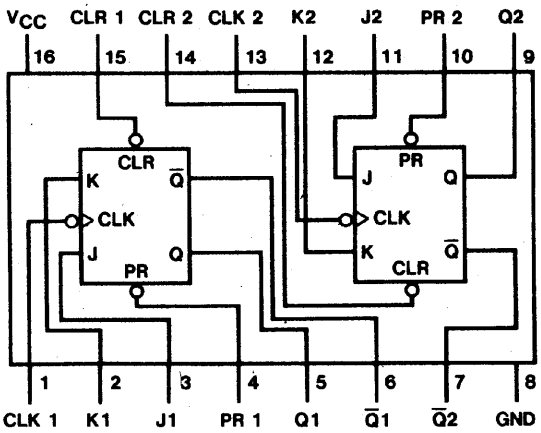
See page 5-29 (109), 5-33 (LS109A)

Notes: ⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

112 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0



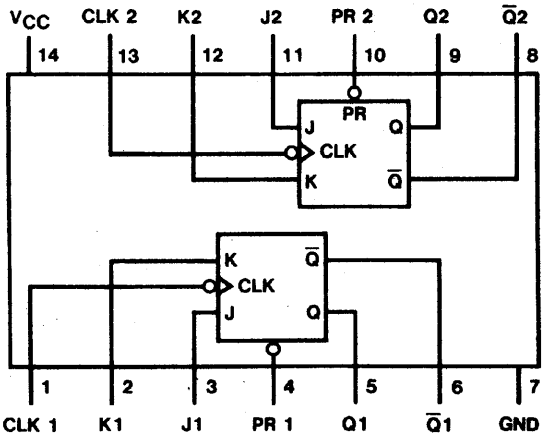
54LS112A (J,W) **74LS112A (N)**
54S112 (J,W) **74S112 (N)**

See page 5-33 (LS112A), 5-35 (S112)

113 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset

Truth Table

Inputs				Outputs	
PR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0



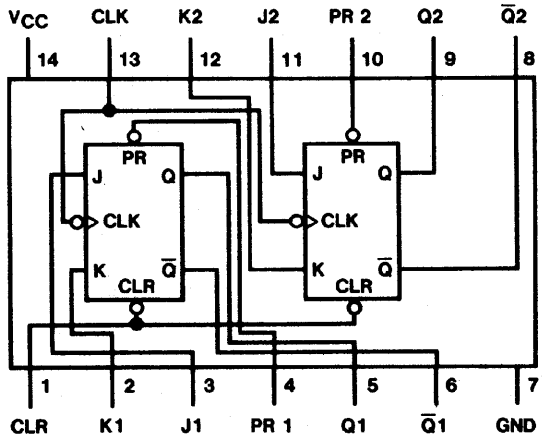
54LS113A (J,W) **74LS113A (N)**
54S113 (J,W) **74S113 (N)**

See page 5-33 (LS113A), 5-35 (S113)

114 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset, Common Clear, and Common Clock

Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0



54LS114A (J,W) **74LS114A (N)**
54S114 (J,W) **74S114 (N)**

See page 5-33 (LS114A), 5-35 (S114)

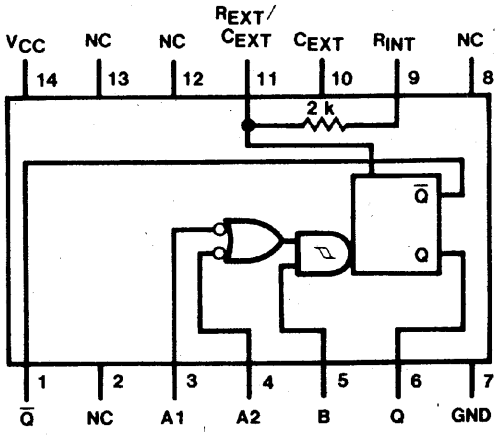
Notes: Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

121 One Shots

Truth Table

Inputs			Outputs	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎌
↓	H	H	⎍	⎌
↓	↓	H	⎍	⎌
L	X	↑	⎍	⎌
X	L	↑	⎍	⎌

See page 5-44



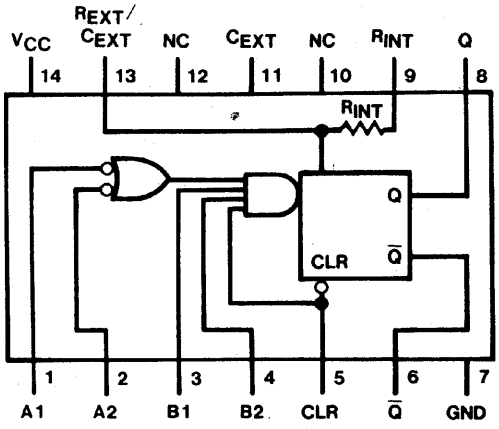
54121 (J,W); 74121 (N)

122 Retriggerable One Shots with Clear

Truth Table

Inputs					Outputs	
Clear	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	↑	H	⎍	⎌
H	L	X	H	↑	⎍	⎌
H	X	L	H	H	L	H
H	X	L	↑	H	⎍	⎌
H	X	L	H	↑	⎍	⎌
H	H	↓	H	H	⎍	⎌
H	↓	↓	H	H	⎍	⎌
H	↓	H	H	H	⎍	⎌
↑	L	X	H	H	⎍	⎌
↑	X	L	H	H	⎍	⎌

See page 5-46



54LS122 (J,W); 74LS122 (N)

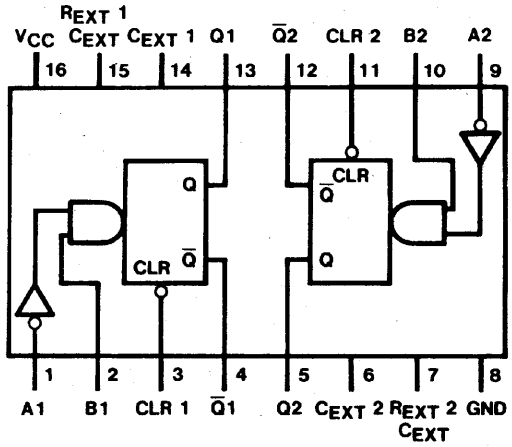
Notes: ⎍ = one high-level pulse, ⎌ = one low-level pulse.
To use the internal timing resistor of 54121/74121, connect R_{INT} to V_{CC}.
An external timing capacitor may be connected between C_{EXT} and R_{EXT}/C_{EXT} (positive).
For accurate repeatable pulse widths, connect an external resistor between R_{EXT}/C_{EXT} and V_{CC} with R_{INT} open-circuited.
To obtain variable pulse widths, connect external variable resistance between R_{INT} or R_{EXT}/C_{EXT} and V_{CC}.

123 Dual Retriggerable One Shots with Clear

Truth Table

123, L123A

Inputs			Outputs	
A	B	CLR	Q	$\overline{Q}$
H	X	H	L	H
X	L	H	L	H
L	↑	H	⎍	⎎
↓	H	H	⎍	⎎
X	X	L	L	H

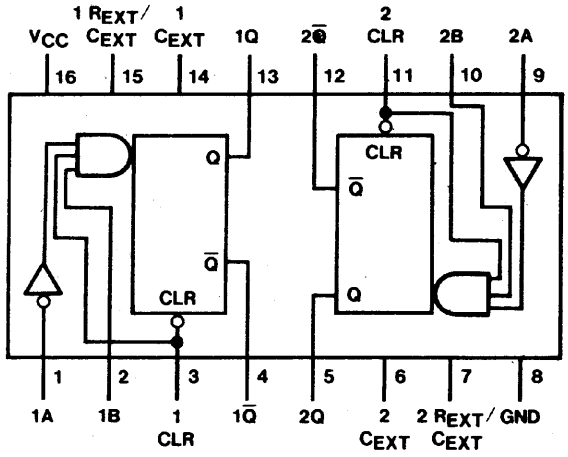


54123 (J,W) **74123 (N)**
54L123A (J,W) **74L123A (N)**

Truth Table

LS123

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎



54LS123 (J,W); 74LS123 (N)

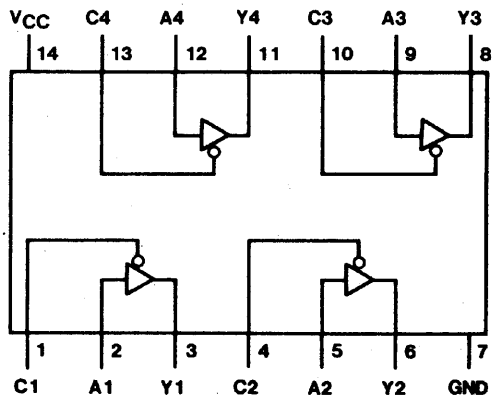
See page 5-46

125 TRI-STATE® Quad Buffers

Truth Table

Inputs		Output
A	C	Y
H	L	H
L	L	L
X	H	Hi-Z

Y = A



54125 (J,W) **74125 (N)**
54LS125A (J,W) **74LS125A (N)**

See page 5-48

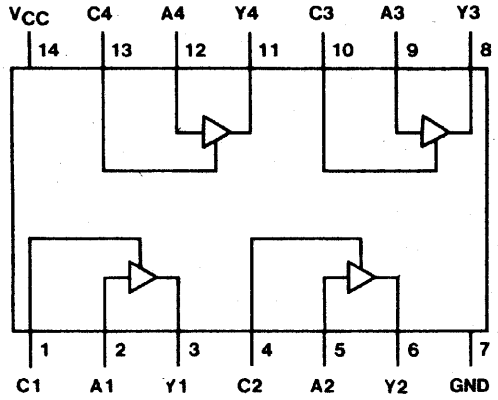
Notes: ⎍ = one high-level pulse, ⎎ = one low-level pulse.
An external timing capacitor may be connected between C_{EXT} and R_{EXT}/C_{EXT} (positive).
For accurate repeatable pulse widths, connect an external resistor between R_{EXT}/C_{EXT} and V_{CC}.
To obtain variable pulse widths, connect external variable resistance between R_{EXT}/C_{EXT} and V_{CC}.

126 TRI-STATE® Quad Buffers

Truth Table

Inputs		Output
A	C	Y
H	H	H
L	H	L
X	L	Hi-Z

Y = A

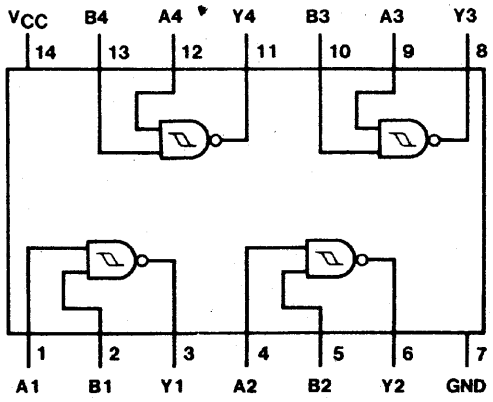


54126 (J,W) 74126 (N)
54LS126A (J,W) 74LS126A (N)

See page 5-48

132 Quad 2-Input NAND Schmitt Triggers

$Y = \overline{AB}$

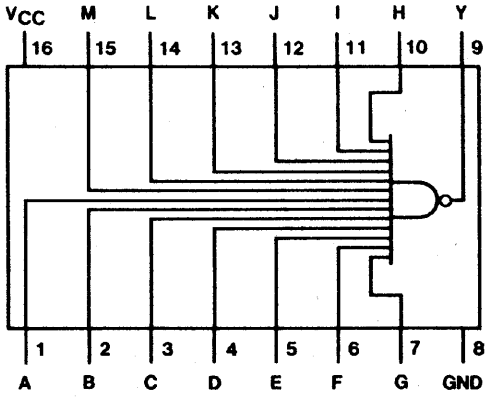


54132 (J,W) 74132 (N)
54LS132 (J,W) 74LS132 (N)

See page 5-16

133 13-Input NAND Gates

$Y = \overline{ABCDEFGHIJKLM}$



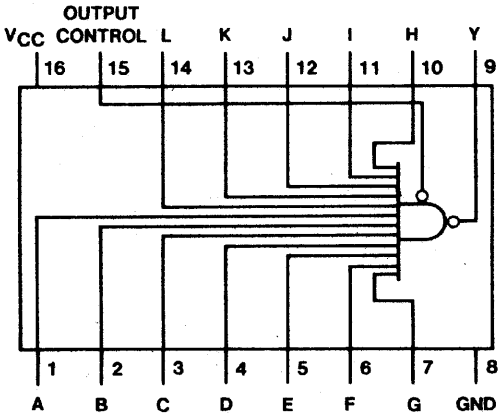
54S133 (J,W); 74S133 (N)

See page 5-4

134 TRI-STATE® 12-Input NAND Gates

$Y = \overline{ABCDEFGHIJKL}$

Output is off (disabled) when output control is high.



54S134 (J,W); 74S134 (N)

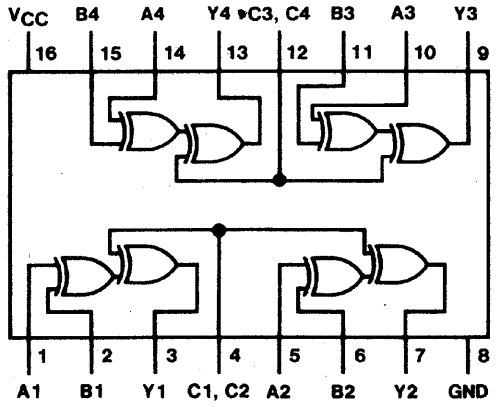
See page 5-48

135 Quad EXCLUSIVE-OR/NOR Gates

Truth Table

Inputs			Output
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

$Y = (A \oplus B) \oplus C =$
$A\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{B}C + ABC$



54S135 (J,W); 74S135 (N)

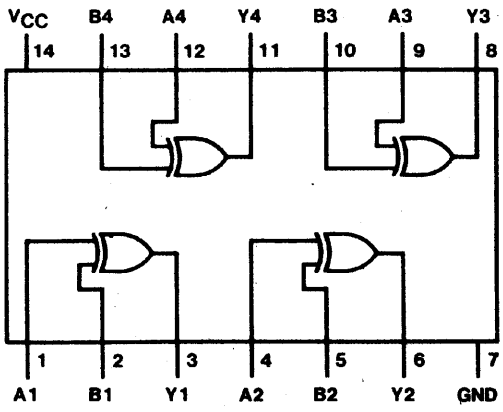
See page 5-50

136 Quad EXCLUSIVE-OR Gates with Open-Collector Outputs

Truth Table

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

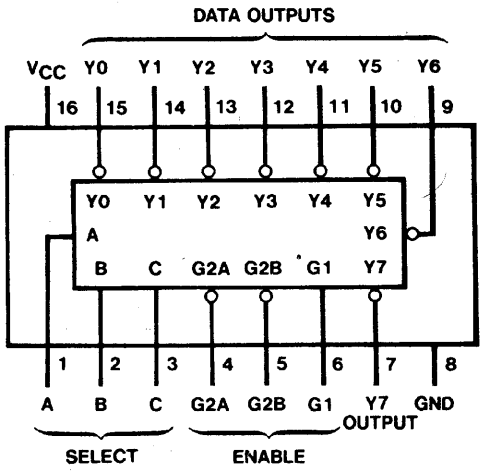
$Y = A \oplus B = \overline{A}B + A\overline{B}$



54LS136 (J,W) **74LS136 (N)**
54S136 (J,W) **74S136 (N)**

See page 5-52

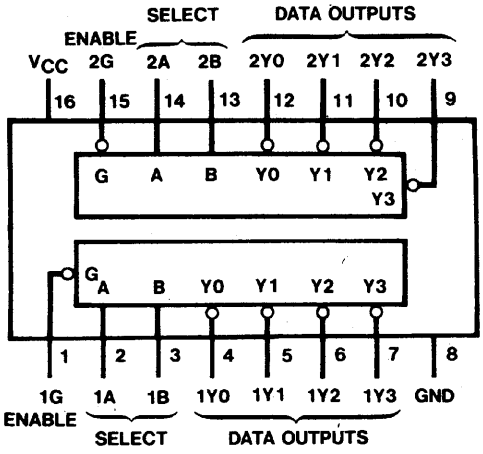
138 3-to-8 Line Decoders/Multiplexers



54LS138 (J,W) **74LS138 (N)**
54S138 (J,W) **74S138 (N)**

See page 6-53

139 Dual 2-to-4 Line Decoders/Multiplexers

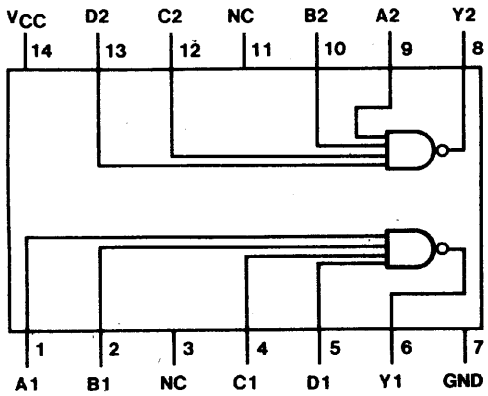


54LS139 (J,W) **74LS139 (N)**
54S139 (J,W) **74S139 (N)**

See page 6-53

140 Dual 50-Ohm Line Drivers

$Y = \overline{ABCD}$

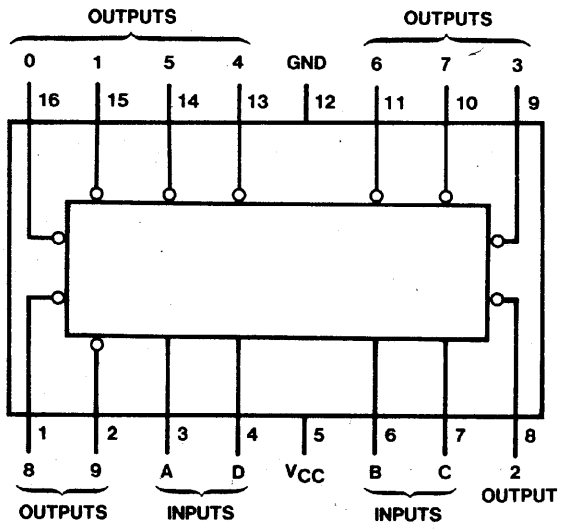


54S140 (J,W); 74S140 (N)

See page 5-22

141 NIXIE® Driver

Input				Output
D	C	B	A	ON*
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
(Over Range)				
H	L	H	L	None
H	L	H	H	None
H	H	L	L	None
H	H	L	H	None
H	H	H	L	None
H	H	H	H	None

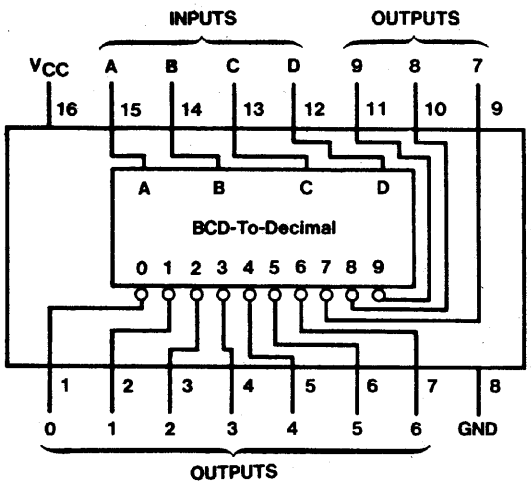


54141 (J,W); 74141 (N)

See page 6-4

BCD-To-Decimal Decoders/Drivers For Lamps, Relays, MOS

145 BCD-to decimal

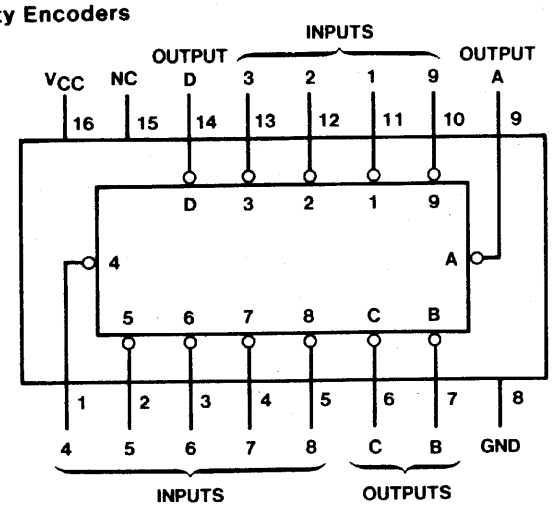


54145 (J,W); 74145 (N)

See page 6-10

10-Line Decimal to 4-Line BCD Priority Encoders

147



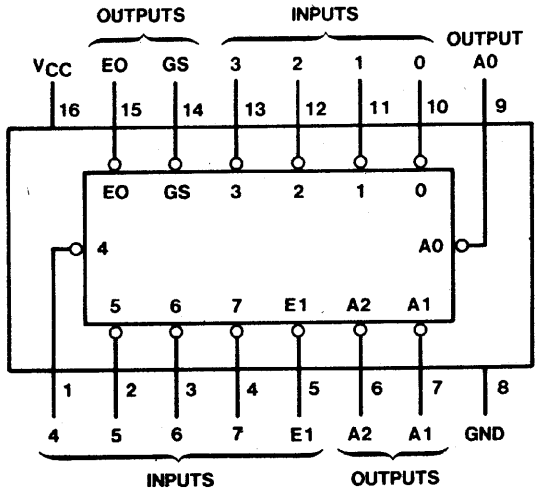
54147 (J,W); 74147 (N)

NC—No internal connection

See page 6-58

8-Line-To-3-Line Octal Priority Encoders

148

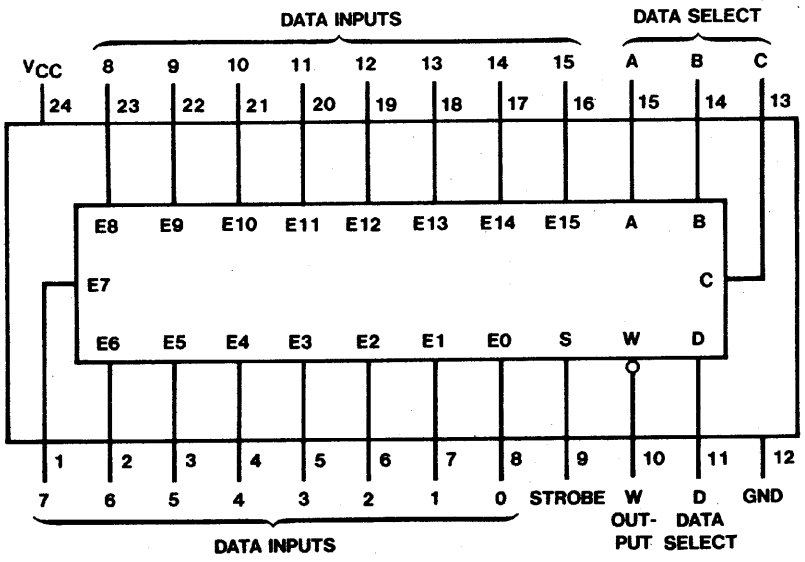


54148 (J,W); 74148 (N)

See page 6-58

1-Of-16-Data Selectors/Multiplexers

150

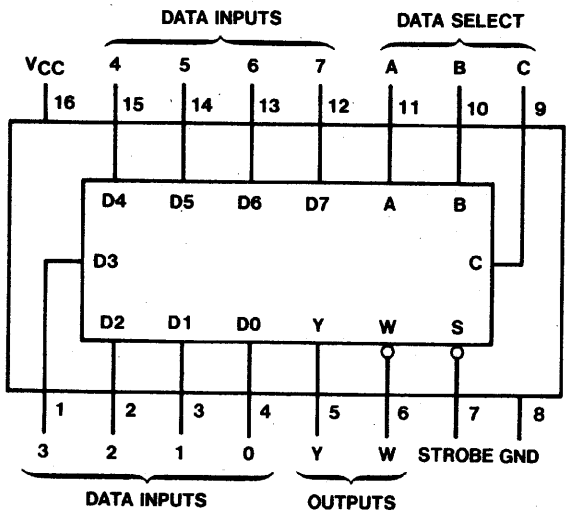


54150 (J,F); 74150 (N)

See page 6-62

1-Of-8 Data Selectors/Multiplexers

151



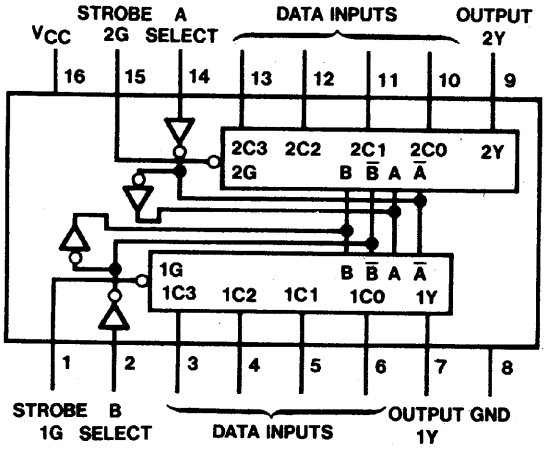
54151A (J,W)
54LS151 (J,W)
54S151 (J,W)

74151A (N)
74LS151 (N)
74S151 (N)

See page 6-62

Dual 4-Line To 1-Line Data Selectors/Multiplexers

153



54153 (J,W)
54LS153 (J,W)
54S153 (J,W)

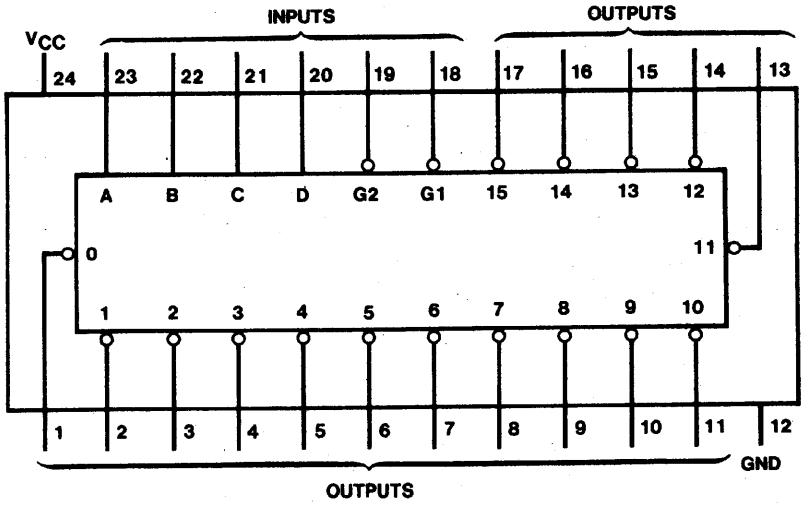
74153 (N)
74LS153 (N)
74S153 (N)

See page 6-68

3

4-Line to 16-Line Decoders/Demultiplexers

154



54154 (J,F)
54L154A (J,F)
54LS154 (J,W)

74154 (N)
74L154A (N)
74LS154 (N)

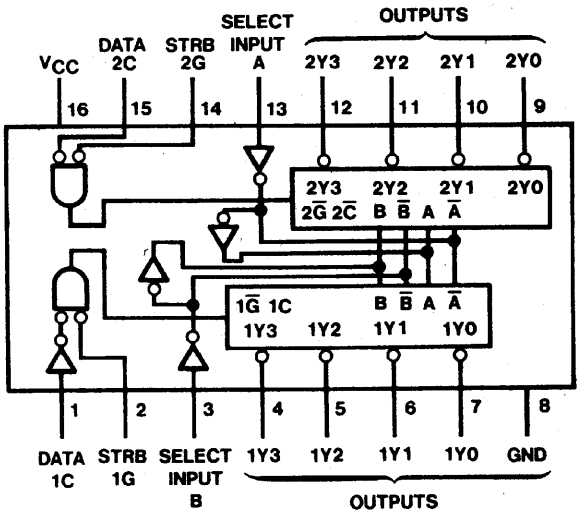
See page 6-71

Decoders/Demultiplexers

Dual 2- to 4-line decoder
Dual 1- to 4-line demultiplexer
3- to 8-line decoder
1- to 8-line demultiplexer

155 Totem-pole outputs

156 Open-collector outputs



54155 (J,W)
54LS155 (J,W)
54156 (J,W)
54LS156 (J,W)

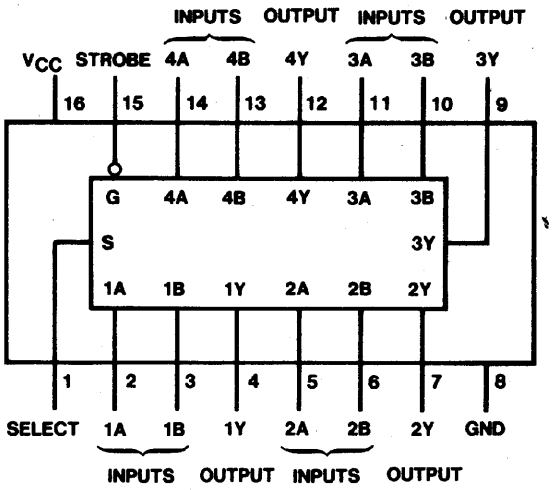
74155 (N)
74LS155 (N)
74156 (N)
74LS156 (N)

See page 6-75

Quad 2- To 1-Line Data Selectors/Multiplexers

157 Noninverted data outputs

158 Inverted data outputs



54157 (J,W)
54L157A (J,W)
54LS157 (J,W)
54S157 (J,W)
54LS158 (J,W)
54S158 (J,W)

74157 (N)
74L157A (N)
74LS157 (N)
74S157 (N)
74LS158 (N)
74S158 (N)

See page 6-78

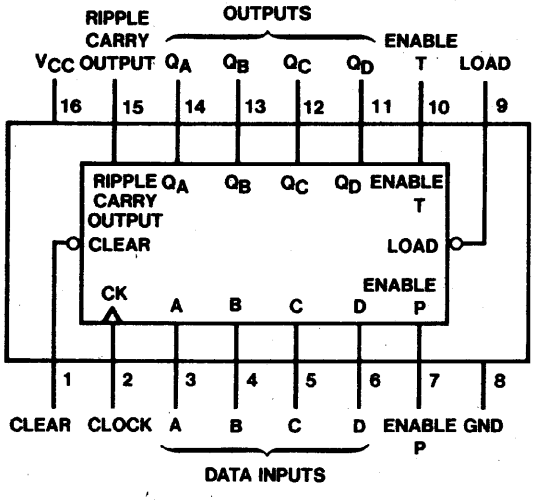
Synchronous 4-Bit Counters

160 Decade, direct clear

161 Binary, direct clear

162 Decade, synchronous clear

163 Binary, synchronous clear



54160A (J,W)
54LS160A (J,W)
54S160 (J,W)
54161A (J,W)
54LS161A (J,W)
54S161 (J,W)
54162A (J,W)
54LS162A (J,W)
54S162 (J,W)
54163A (J,W)
54LS163A (J,W)
54S163 (J,W)

74160A (N)
74LS160A (N)
74S160 (N)
74161A (N)
74LS161A (N)
74S161 (N)
74162A (N)
74LS162A (N)
74S162 (N)
74163A (N)
74LS163A (N)
74S163 (N)

See page 6-82

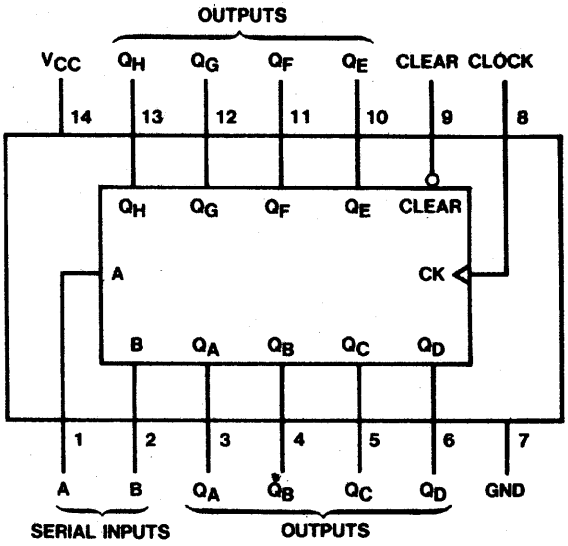
8-Bit Parallel Output Serial Shift Registers

164 Asynchronous clear

Truth Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.



54164 (J,W) **74164 (N)**
54L164A (J,W) **74L164A (N)**
54LS164 (J,W) **74LS164 (N)**

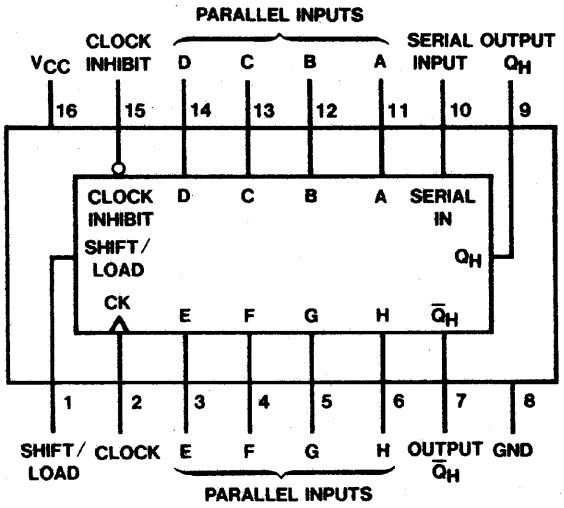
See page 6-95

Parallel-Load 8-Bit Shift Registers With Complementary Outputs

165

Truth Table

Inputs					Internal Outputs		Output Q_H
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

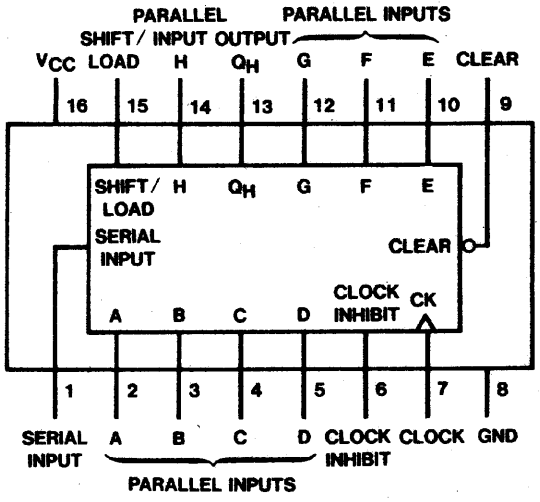


54165 (J,W) **74165 (N)**
54L165A (J,W) **74L165A (N)**
54LS165 (J,W) **74LS165 (N)**

See page 6-98

8-Bit Shift Registers

166 Parallel/serial input Serial output



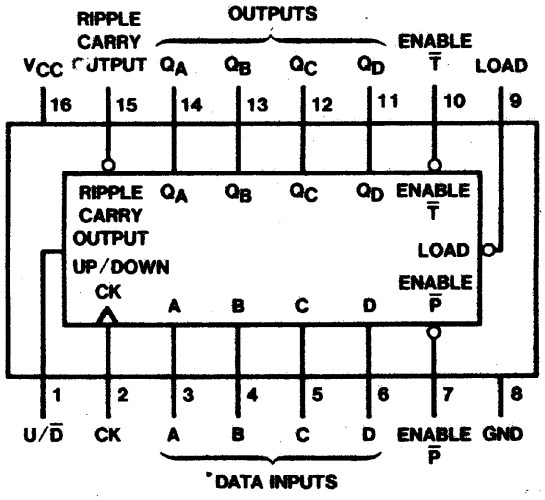
54166 (J) **74166 (N)**
54LS166 (J,W) **74LS166 (N)**

See page 6-102

4-Bit Up/Down Synchronous Counters

168 Decade

169 Binary



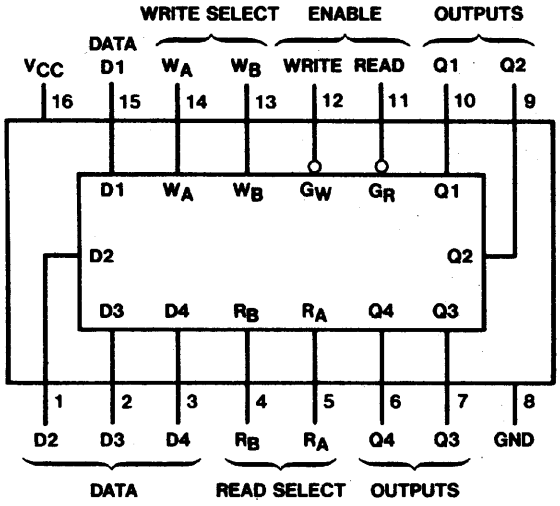
54LS168A (J,W) **74LS168A (N)**
54LS169A (J,W) **74LS169A (N)**

See page 6-106

4-By-4 Register Files

170

Separate read/write addressing
Simultaneous read and write
Open-collector outputs
Expandable to 1024 words



54LS170 (J,W)

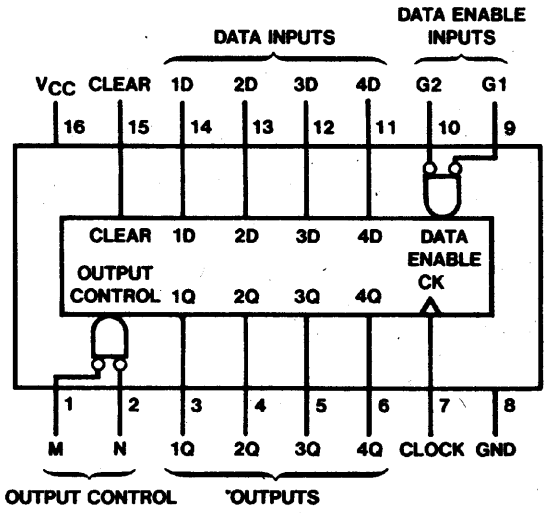
74170 (N)
74LS170 (N)

See page 6-113

4-Bit D-Type Registers

173

TRI-STATE® outputs



54173 (J,W)
54LS173 (J,W)

74173 (N)
74LS173 (N)

See page 6-118

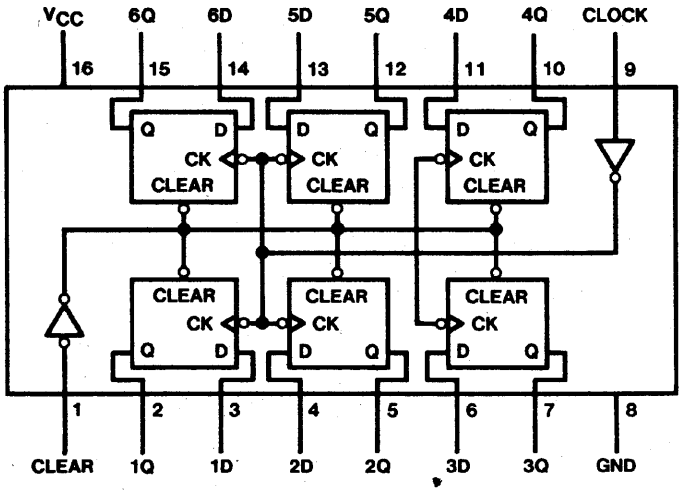
Hex D-Type Flip-Flops

174 Single rail outputs Common direct clear

Truth Table
(Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.



54174 (J,W) **74174 (N)**
54LS174 (J,W) **74LS174 (N)**
54S174 (J,W) **74S174 (N)**

See page 6-122

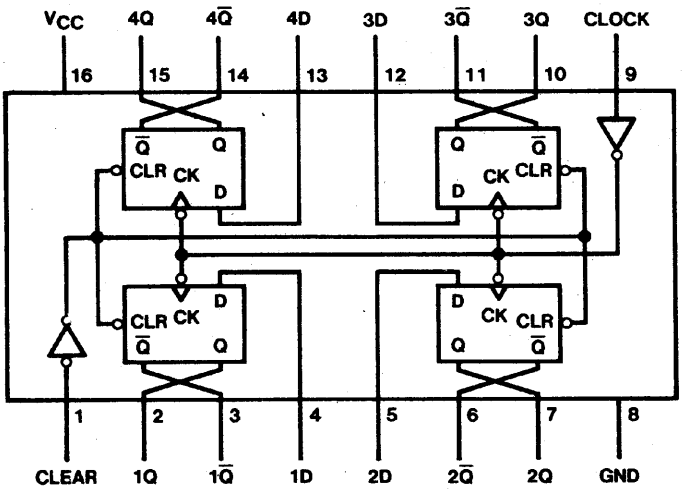
Quad D-Type Flip-Flops

175 Complementary outputs Common direct clear

Truth Table
(Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.



54175 (J,W) **74175 (N)**
54LS175 (J,W) **74LS175 (N)**
54S175 (J,W) **74S175 (N)**

See page 6-122

3

Presettable Counters/Latches

176 Decade (Bi-quinary)

177 Binary

Truth Tables

Decade (BCD)
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Bi-Quinary (5-2)
(See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

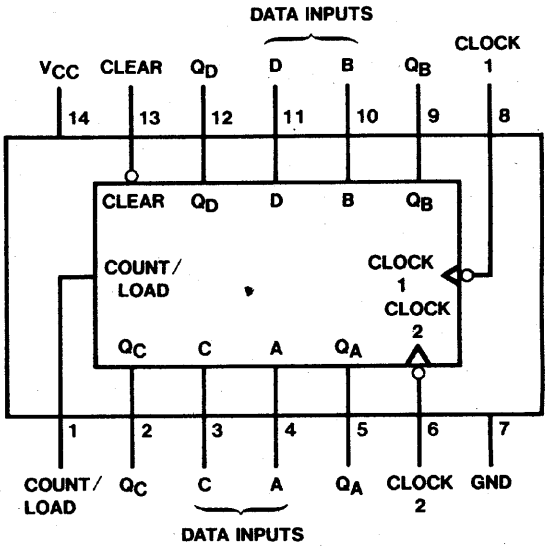
H = high level, L = low level
Note A: Output Q_A connected to clock-2 input.
Note B: Output Q_D connected to clock-1 input.

Truth Table

(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = high level, L = low level
Note A: Output Q_A connected to clock-2 input.



54176 (J) **74176 (N)**
54177 (J) **74176 (N)**

See page 6-126

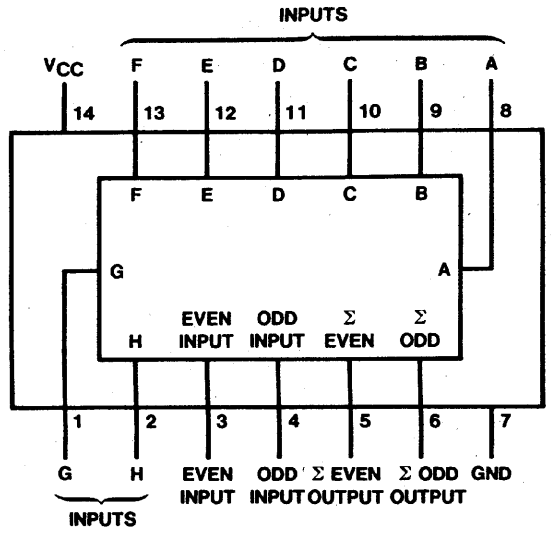
9-Bit Odd/Even Parity Generators/Checkers

180

Truth Table

Inputs			Outputs	
Σ of H's at A thru H	Even	Odd	Σ Even	Σ Odd
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = high level, L = low level, X = irrelevant

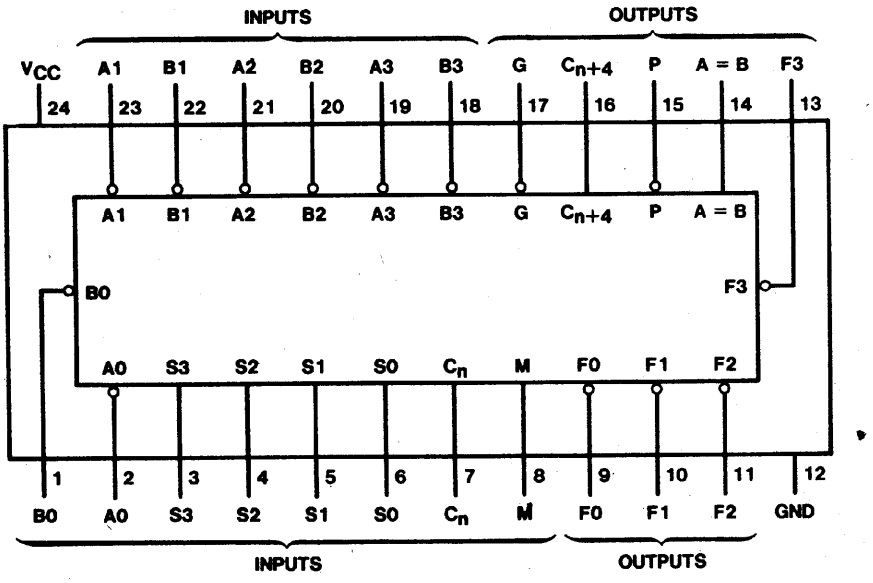


54180 (J,W); 74180 (N)

See page 6-132

Arithmetic Logic Units/Function Generators

181 16 Arithmetic operations 16 Logic functions



54181 (J) 74181 (N)
54S181 (J) 74S181 (N)

See page 6-135

3

Look-Ahead Carry Generators

182

Truth Table

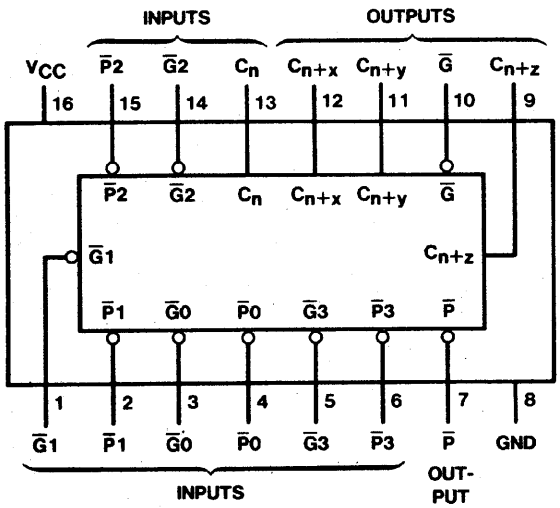
For $\overline{G}$ Output

Inputs							Output
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

H = high level, L = low level, X = irrelevant
Any inputs not shown in a given table are irrelevant with respect to that output.

For $\overline{P}$ Output

Inputs				Output
$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{P}$
L	L	L	L	L
All other combinations				H



54S182 (J,W); 74S182 (N)

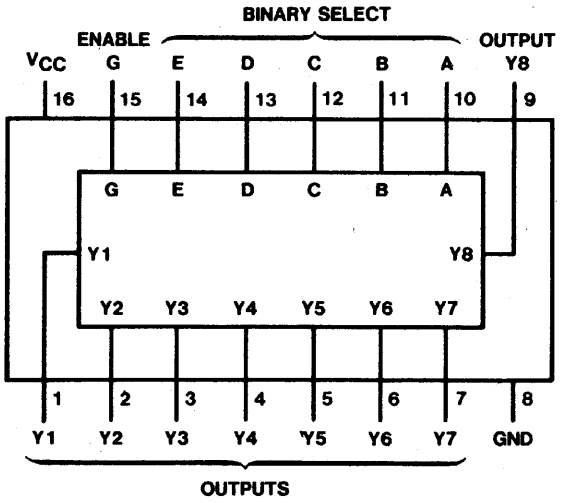
See page 6-144

Code Converters

Cascadeable to N-Bits

184 BCD-to-Binary

185 Binary-to-BCD



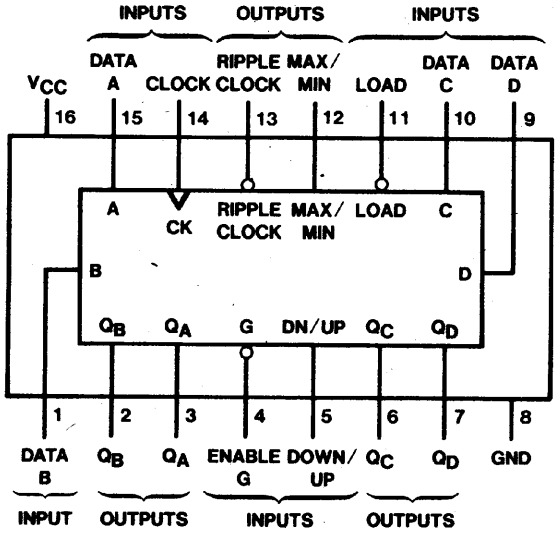
54184 (J,W) **74184 (N)**
54185A (J,W) **74185A (N)**

See page 6-148

Synchronous Up/Down Counters

190 BCD

191 Binary



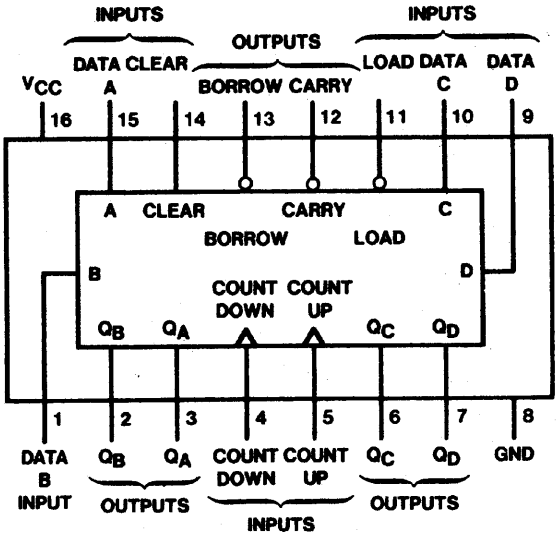
54190 (J,W) **74190 (N)**
54LS190 (J,W) **74LS190 (N)**
54191 (J,W) **74191 (N)**
54LS191 (J,W) **74LS191 (N)**

See page 6-154

Synchronous Up/Down Dual Clock Counters

192 BCD with clear

193 Binary with clear



54192 (J,W)
54L192 (J,W)
54LS192 (J,W)
54193 (J,W)
54L193 (J,W)
54LS193 (J,W)

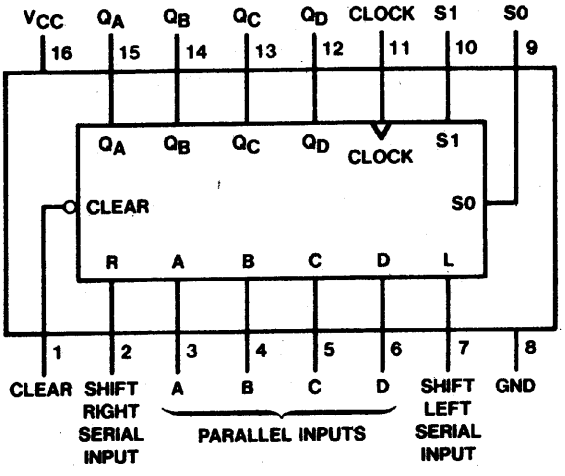
74192 (N)
74L192 (N)
74LS192 (N)
74193 (N)
74L193 (N)
74LS193 (N)

See page 6-161

3

4-Bit Bidirectional Universal Shift Registers

194



Truth Table

Inputs									Outputs			
Clear	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S2		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

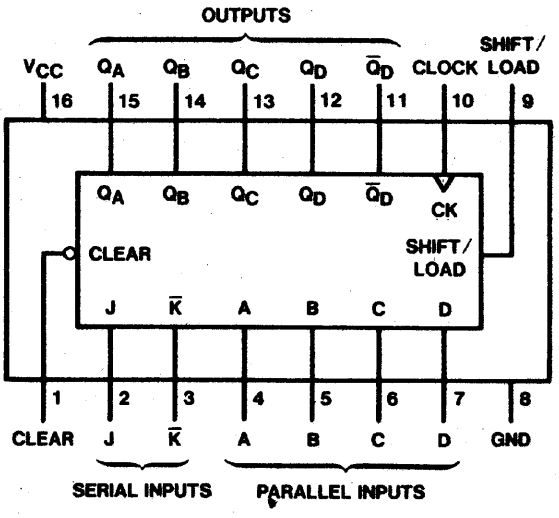
54194 (J,W)
54LS194A (J,W)
54S194 (J,W)

74194 (N)
74LS194A (N)
74S194 (N)

See page 6-169

4-Bit Parallel-Access Shift Registers

195



Truth Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}, = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent transition of the clock.

See page 6-174

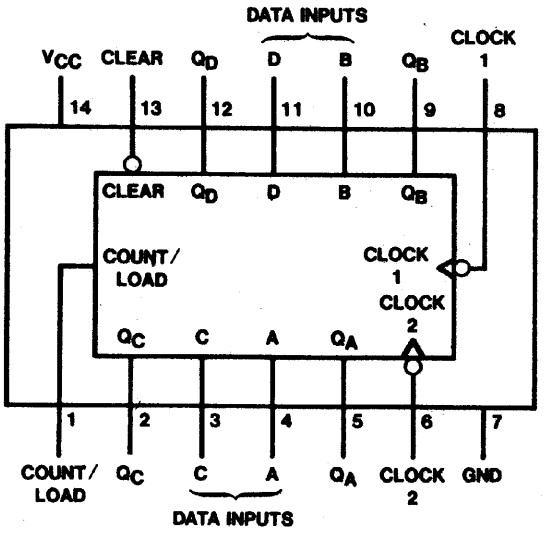
54195 (J,W)
54LS195A (J,W)
54S195 (J,W)

74195 (N)
74LS195A (N)
74S195 (N)

Presettable Counters/Latches

196 Decade/Bi-quinary

197 Binary



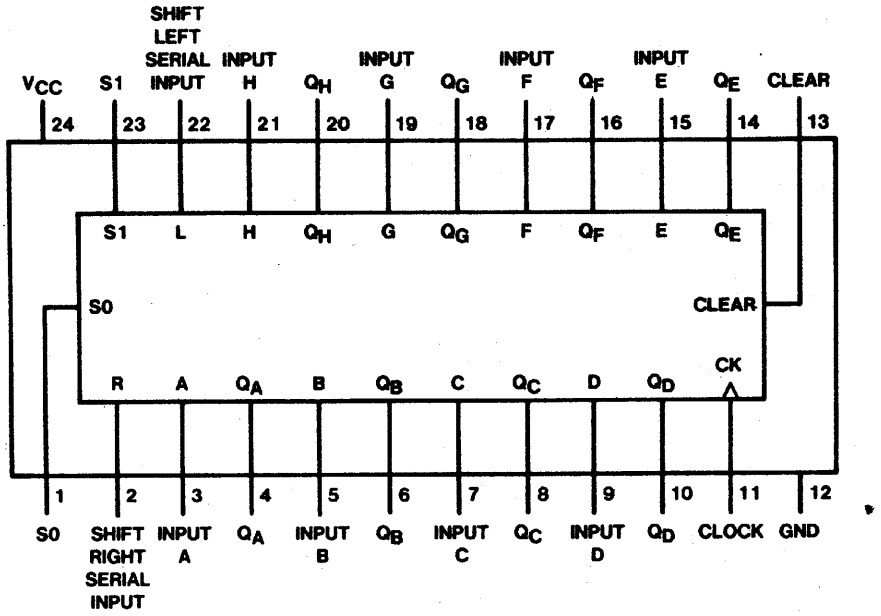
54196 (J,N)
54LS196 (J,W)
54S196 (J,W)
54197 (J)
54LS197 (J,W)
54S197 (J,W)

74196 (N)
74LS196 (N)
74S196 (N)
74197 (N)
74LS197 (N)
74S197 (N)

See page 6-126

8-Bit Bidirectional Universal Shift Registers

198

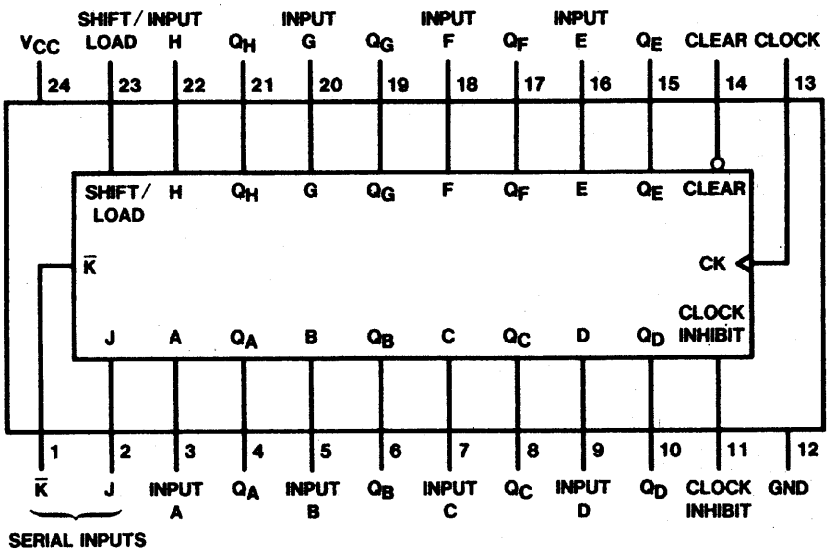


54198 (J); 74198 (N)

See page 6-178

8-Bit Bidirectional Universal Shift Registers

199 J-$\overline{K}$ serial inputs



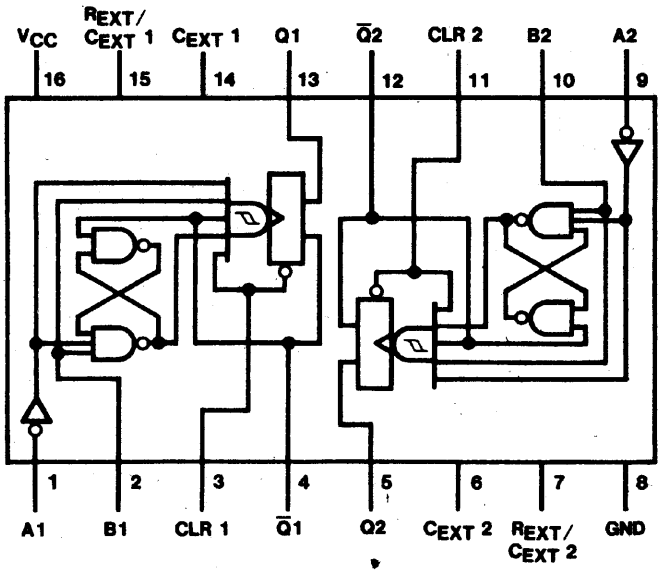
54199 (J); 74199 (N)

See page 6-178

221 Dual One Shots with Schmitt-Trigger Inputs

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

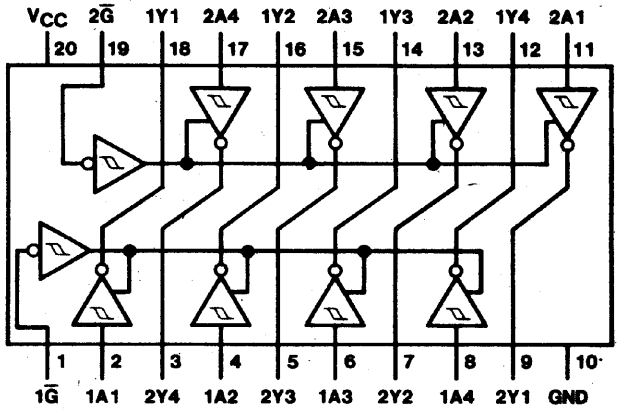


54LS221 (J,W); 74LS221 (N)

See page 5-44

Octal Buffers/Line Drivers/Line Receivers

240 Inverted TRI-STATE® Outputs



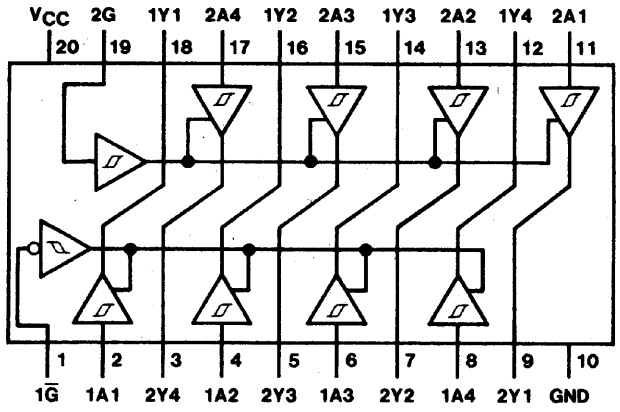
54LS240 (J)
54S240 (J)

74LS240 (N)
74S240 (N)

See page 5-53

Octal Buffers/Line Drivers/Line Receivers

241 Noninverted TRI-STATE Outputs



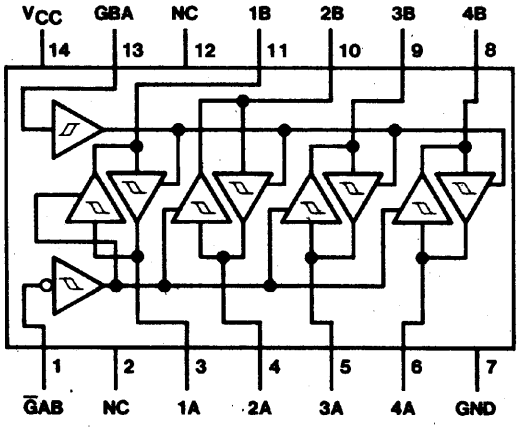
54LS241 (J)
54S241 (J)

74LS241 (N)
74S241 (N)

See page 5-53

Quadruple BUS Transceivers

242 Inverted TRI-STATE® Outputs



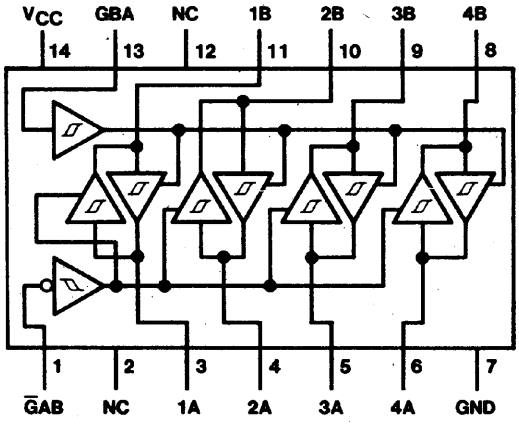
54LS242 (J) **74LS242 (N)**
54S242 (J) **74S242 (N)**

NC—No internal connection

See page 5-57

Quadruple Bus Transceivers

243 Noninverted TRI-STATE Outputs



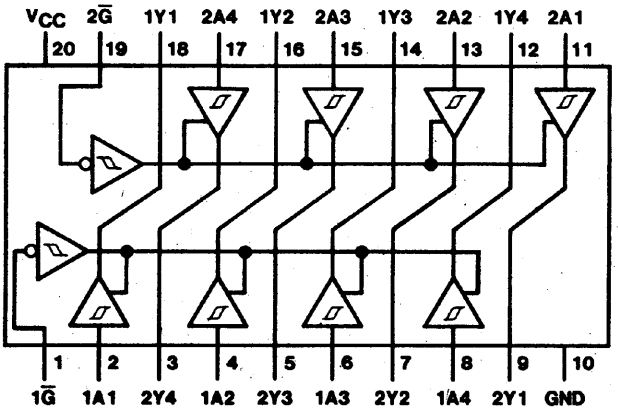
54LS243 (J) **74LS243 (N)**
54S243 (J) **74S243 (N)**

NC—No internal connection

See page 5-57

Octal Buffers/Line Drivers/Line Receivers

244 Noninverted TRI-STATE Outputs

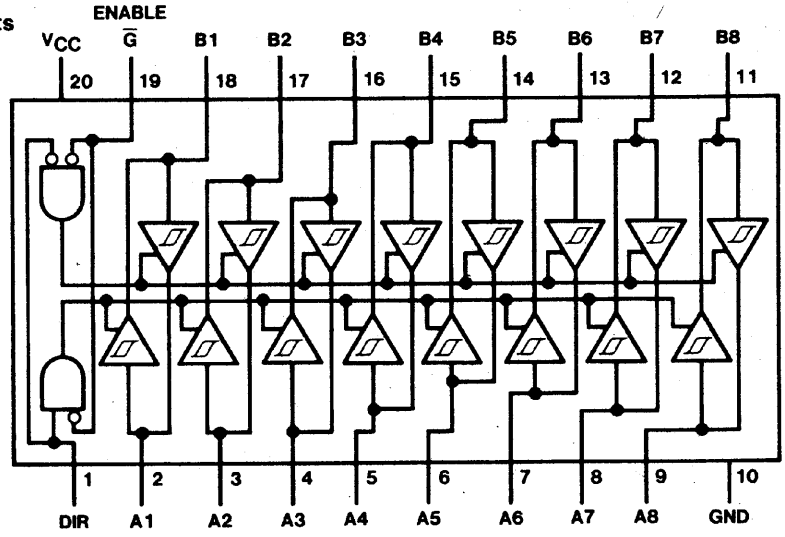


54LS244 (J) **74LS244 (N)**
54S244 (J) **74S244 (N)**

See page 5-53

Octal Bus Tranceivers

245 Noninverted TRI-STATE® Outputs

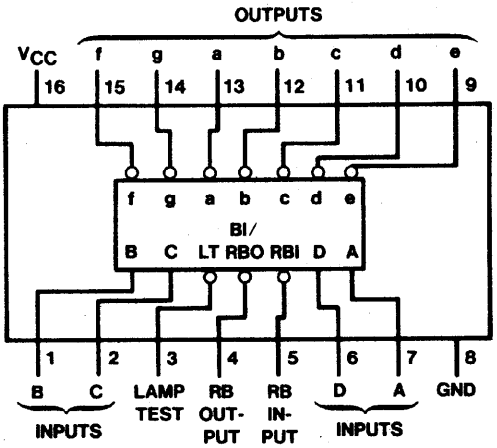


54LS245 (J); 74LS245 (N)

See page 5-60

BCD-to-Seven-Segment Decoders/Drivers

247 Active-Low, Open-Collector, 15-V Outputs



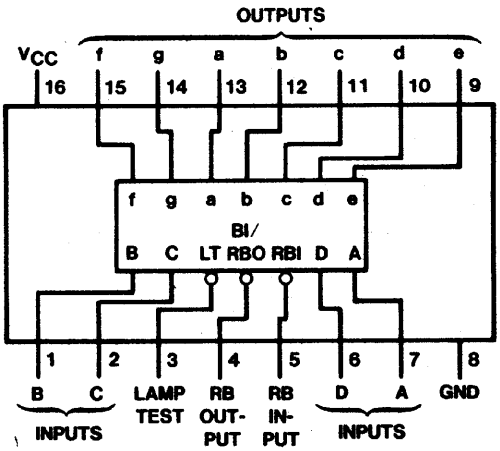
54LS247 (J,W); 74LS247 (N)

See page 6-184

BCD-to-Seven-Segment Decoders/Drivers

248 Internal Pull-Up Outputs

249 Open-Collector Outputs



54LS248 (J,W) 74LS248 (N)
54LS249 (J,W) 74LS249 (N)

See page 6-184

Data Selectors/Multiplexers

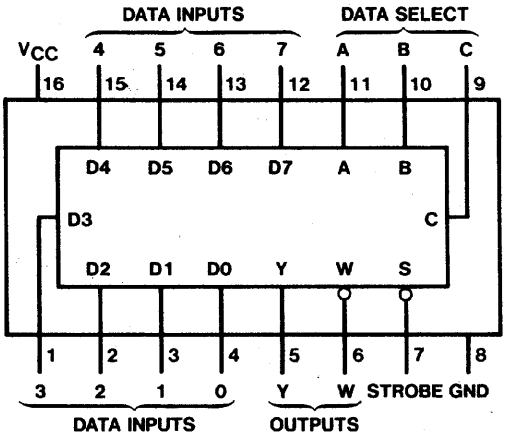
251 True and Inverted TRI-STATE® Outputs

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1...D7 = the level of the respective D input

See page 6-190



54251 (J,W) 74251 (N)
54LS251 (J,W) 74LS251 (N)
54S251 (J,W) 74S251 (N)

Dual Data Selectors/Multiplexers

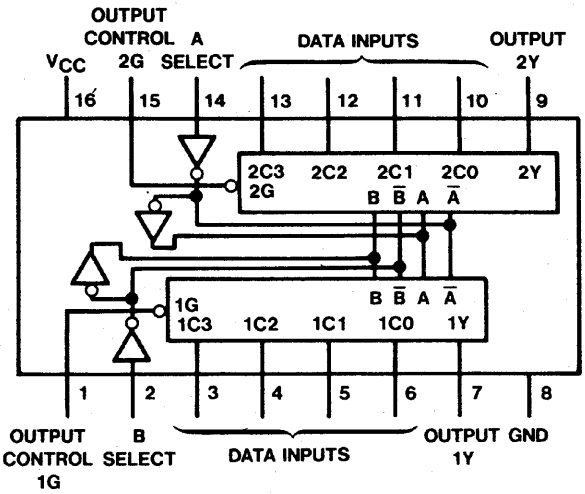
253 TRI-STATE Outputs

Truth Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

See page 6-194



54LS253 (J,W) 74LS253 (N)
54S253 (J,W) 74S253 (N)

Quad Data Selectors/Multiplexers

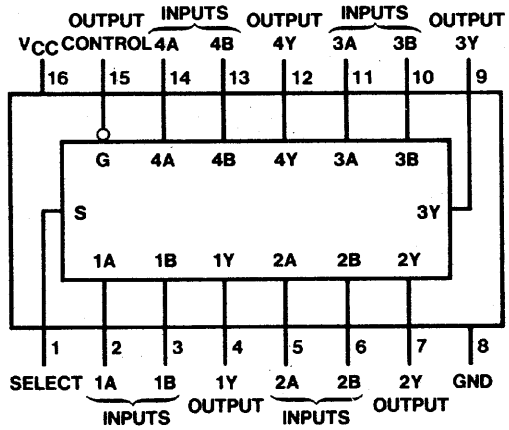
257 Noninverted TRI-STATE Outputs

Truth Table

Inputs				Output Y
Output Control	Select	A	B	'LS257A 'S257
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant, Z = high impedance, (off)

See page 6-197



54LS257B (J,W) 74LS257B (N)
54S257 (J,W) 74S257 (N)

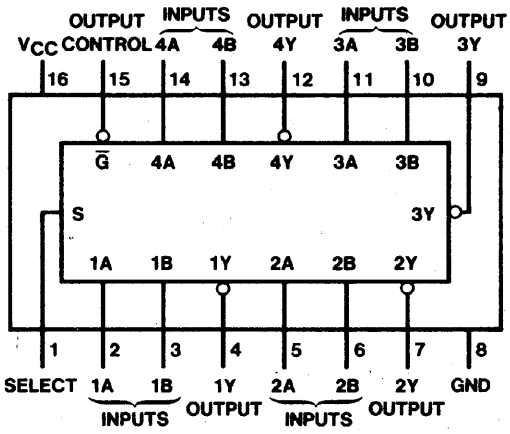
Quad Data Selectors/Multiplexers

258 Inverted TRI-STATE® Outputs

Truth Table

Inputs				Output Y
Output Control	Select	A	B	'LS258A 'S258
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = high level, L = low level, X = irrelevant, Z = high impedance, (off)



54LS258B (J,W) 74LS258B (N)
54S258 (J,W) 74S258 (N)

See page 6-197

Eight-Bit Addressable Latches

259

Truth Table

Inputs		Output of Addressed Latch	Each Other Output	Function
Clear	$\overline{G}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

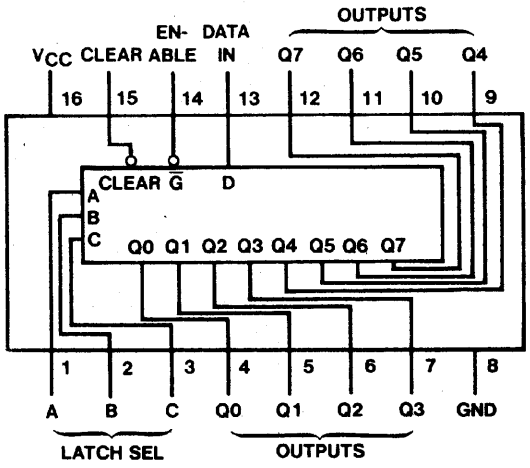
Latch Selection Table

Select Inputs			Latch Addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = high level, L = low level

D = the level at the data input

Q_{i0} = the level of Q_i (i = 0, 1...7, as appropriate) before the indicated steady-state input conditions were established.



54LS259 (J,W) 74LS259 (N)
54259 (J,W) 74259 (N)

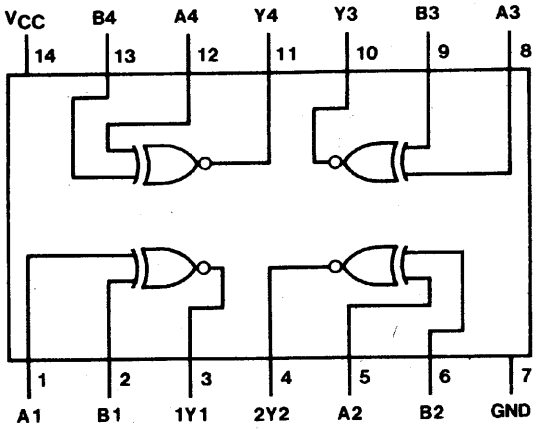
See page 6-201

266 Quad EXCLUSIVE-NOR Gates with Open-Collector Outputs

Truth Table

Inputs A	Inputs B	Output Y
L	L	H
L	H	L
H	L	L
H	H	H

$Y = \overline{A \oplus B} = AB + \overline{A}\overline{B}$



54LS266 (J,W); 74LS266 (N)

See page 5-52

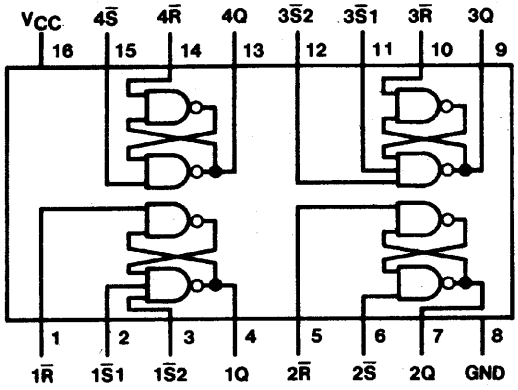
Quad $\overline{S}$-$\overline{R}$ Latches

279

Truth Table

Inputs $\overline{S}$†	Inputs $\overline{R}$	Output Q
H	H	Q_0
L	H	H
H	L	L
L	L	H*

H = high level
L = low level
Q_0 = the level of Q before the indicated input conditions were established.
*This output level is pseudo stable; that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.
†For latches with double $\overline{S}$ inputs:
H = both $\overline{S}$ inputs high
L = one or both $\overline{S}$ inputs low



54LS279 (J,W); 74LS279 (N)

See page 5-63

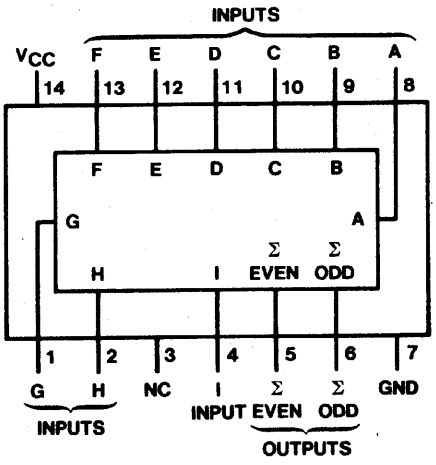
9-Bit Odd/Even Parity Generators/Checkers

280 N-Bit Cascadeable

Truth Table

Number of Inputs A Thru I That Are High	Outputs Σ Even	Outputs Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level



54S280 (J,W); 74S280 (N)

See page 6-204

4-Bit Binary Full Adders

283

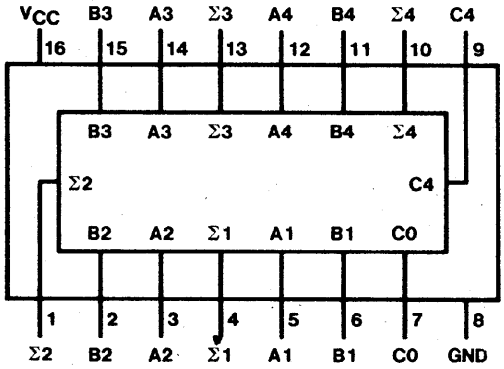
Truth Table

Input				Output					
				When C0 = L			When C0 = H		
				When C2 = L			When C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

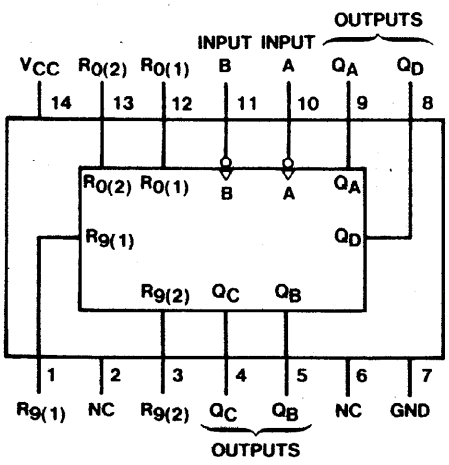
See page 6-21



54LS283 (J,W) **74LS283 (N)**
54S283 (J,W) **74S283 (N)**

4-Bit Decade Counters

290 Divide-by-Two and Divide-by-5



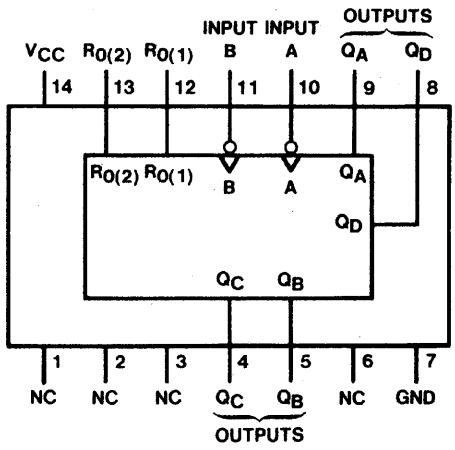
54LS290 (J,W); 74LS290 (N)

NC—no internal connection

See page 6-207

4-Bit Binary Counters

293 Divide-by-Two and Divide-by-Eight



54LS293 (J,W); 74LS293 (N)

NC—no internal connection

See page 6-207

Quad 2-Input Multiplexers With Storage

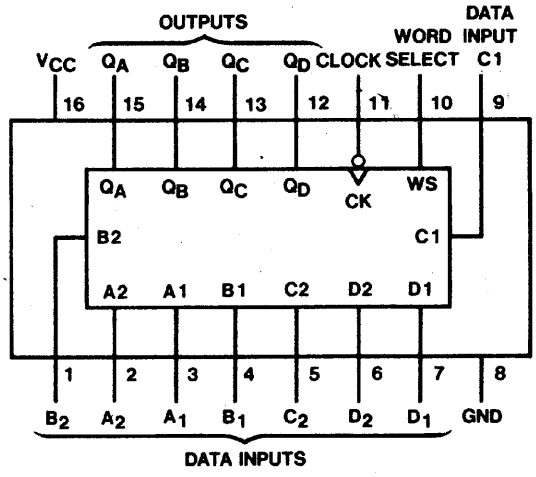
298

Truth Table

Inputs		Outputs			
Word Select	Clock	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most-recent ↓ transition of the clock input.

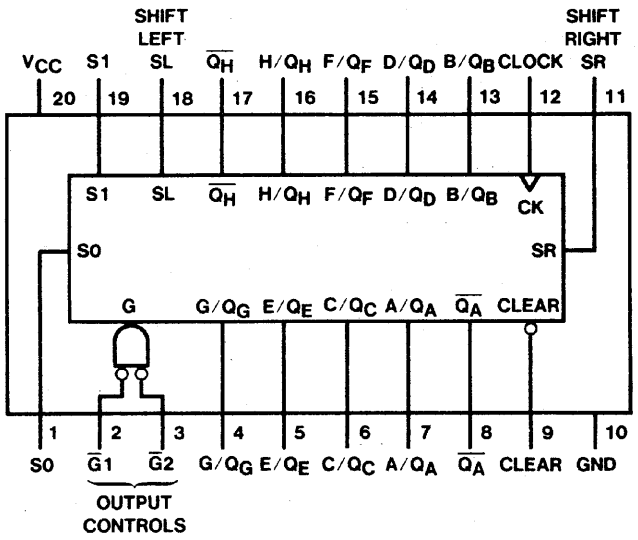
See page 6-211



54LS298 (J,W); 74LS298 (N)

8-Bit Bidirectional Universal Shift/Storage Registers

299 TRI-STATE® Outputs

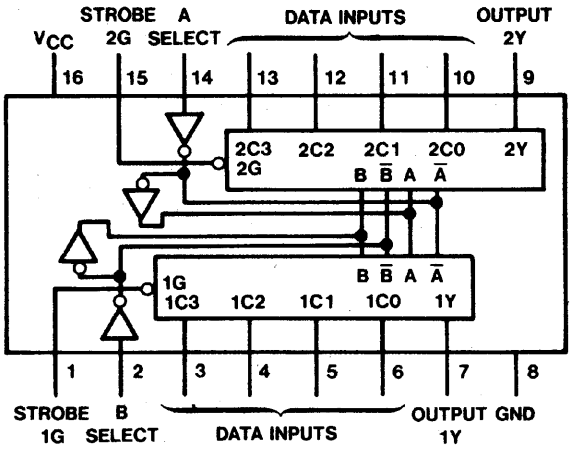


54S299 (J); 74S299 (N)

See page 6-214

Dual 4-Line-to-1-Line Data Selectors/Multiplexers

352 Inverting Version of 'LS153

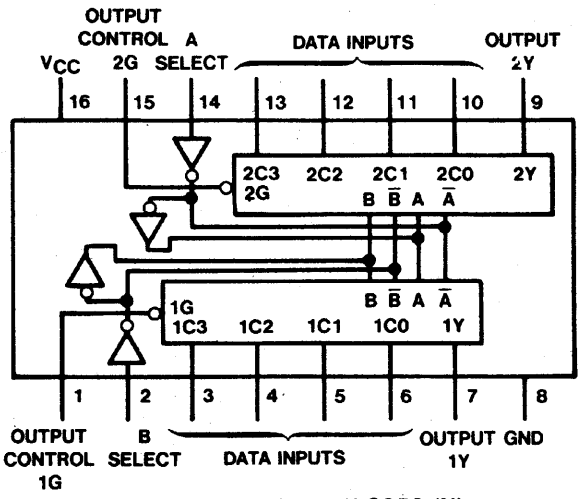


54LS352 (J,W); 74LS352 (N)

See page 6-220

Dual 4-Line-to-1-Line Data Selectors/Multiplexers

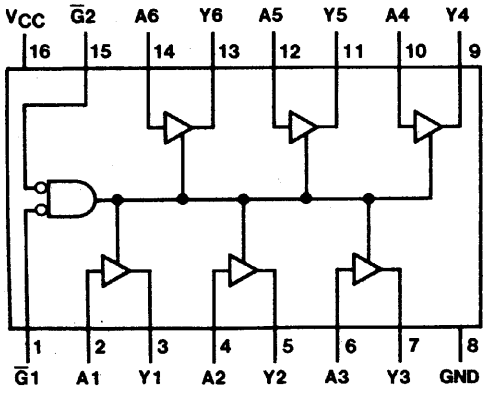
353 TRI-STATE® Outputs Inverting Version of 'LS253



54LS353 (J,W); 74LS353 (N)

See page 6-222

365 TRI-STATE Hex Buffers



Truth Table

Inputs			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

54365 (J,W) 74365 (N)
54LS365A (J,W) 74LS365A (N)

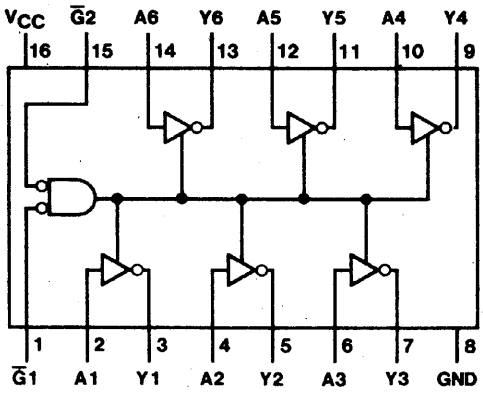
See page 5-64

366 TRI-STATE® Hex Inverting Buffers

Truth Table

Inputs			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

See page 5-64



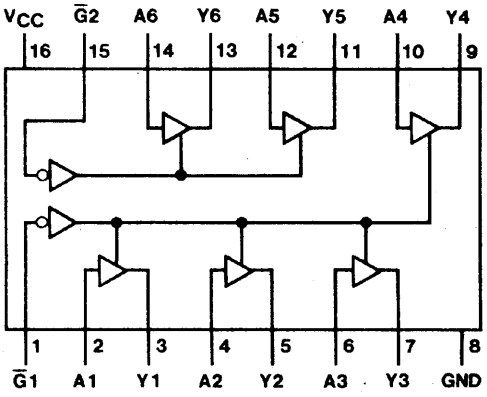
54366 (J,W) 74366 (N)
54LS366A (J,W) 74LS366A (N)

367 TRI-STATE Hex Buffers

Truth Table

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

See page 5-64



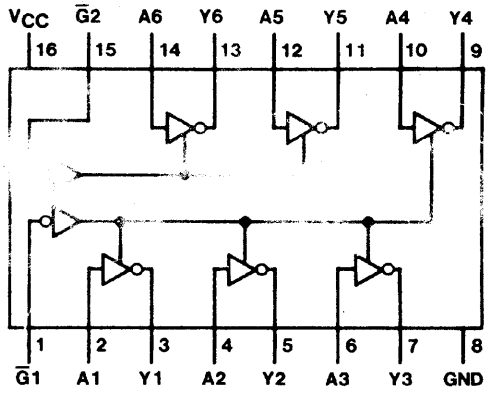
54367 (J,W) 74367 (N)
54LS367A (J,W) 74LS367A (N)

368 TRI-STATE Hex Inverting Buffers

Truth Table

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

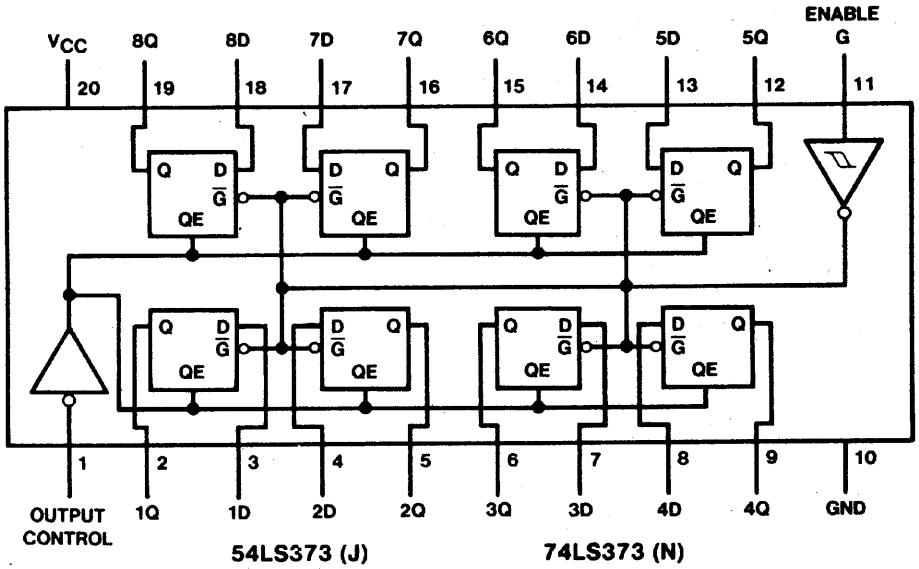
See page 5-64



54368 (J,W) 74368 (N)
54LS368A (J,W) 74LS368A (N)

Octal D-Type Latches

373 TRI-STATE® Outputs



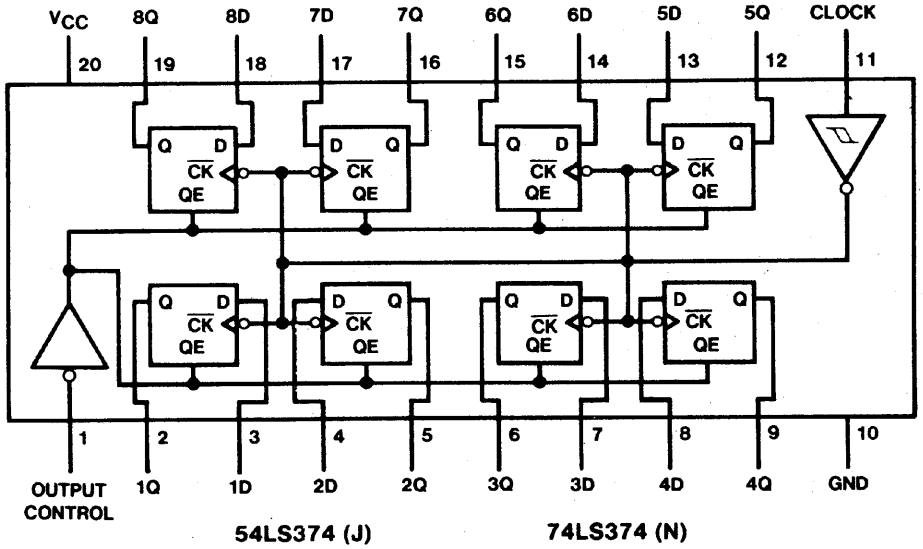
54LS373 (J)
54S373 (J)

74LS373 (N)
74S373 (N)

See page 6-225

Octal D-Type Flip-Flops

374 TRI-STATE Outputs



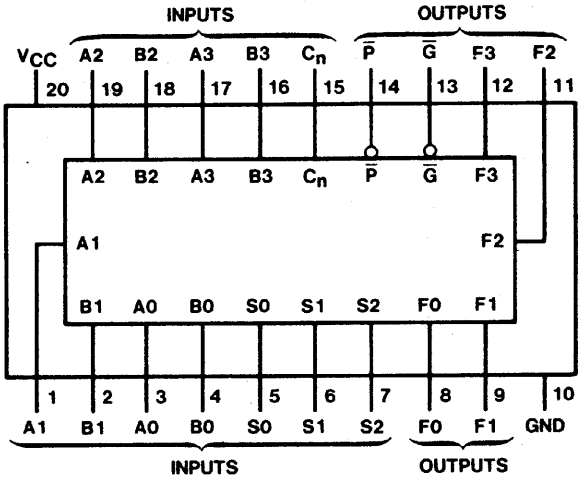
54LS374 (J)
54S374 (J)

74LS374 (N)
74S374 (N)

See page 6-225

Arithmetic Logic Units/Function Generators

381



54S381 (J); 74S381 (N)

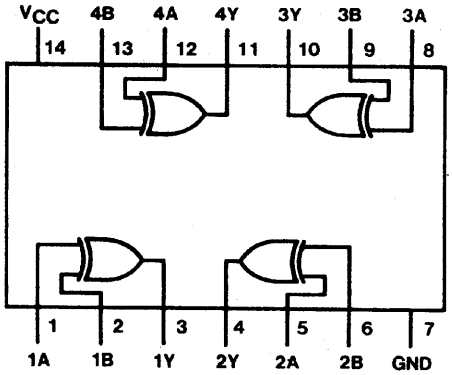
See page 6-230

Quad 2-Input Exclusive-OR Gates

386

Positive Logic:

$Y = A \oplus B = \overline{A}B + A\overline{B}$

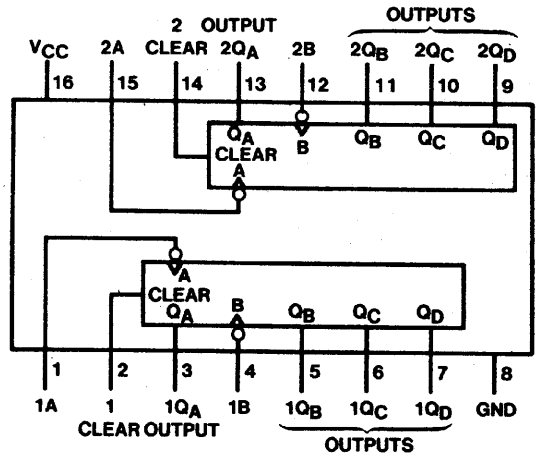


54LS386 (J,W); 74LS386 (N)

See page 5-40

Dual Decade Counters

390 Bi-Quinary or BCD Sequences

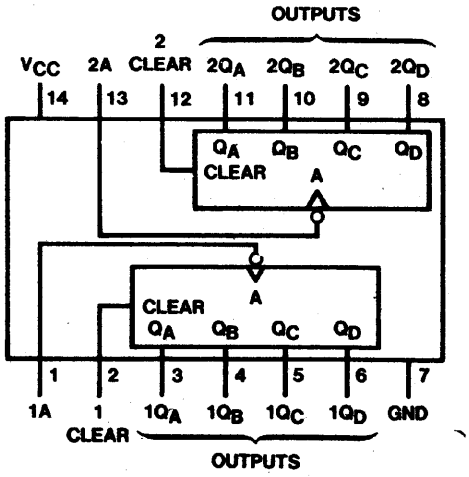


See page 6-234

54LS390 (J,W); 74LS390 (N)

Dual 4-Bit Binary Counters

393

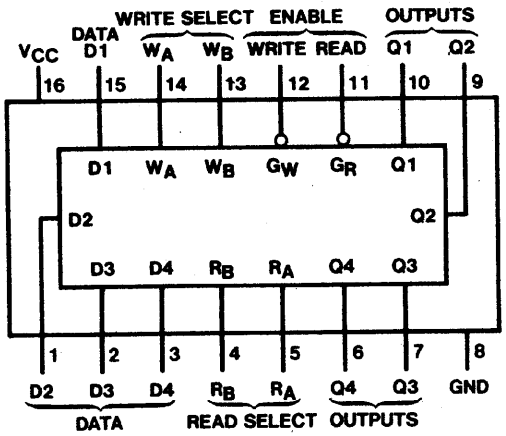


See page 6-234

54LS393 (J,W); 74LS393 (N)

4-by-4 Register Files

670 TRI-STATE® Outputs

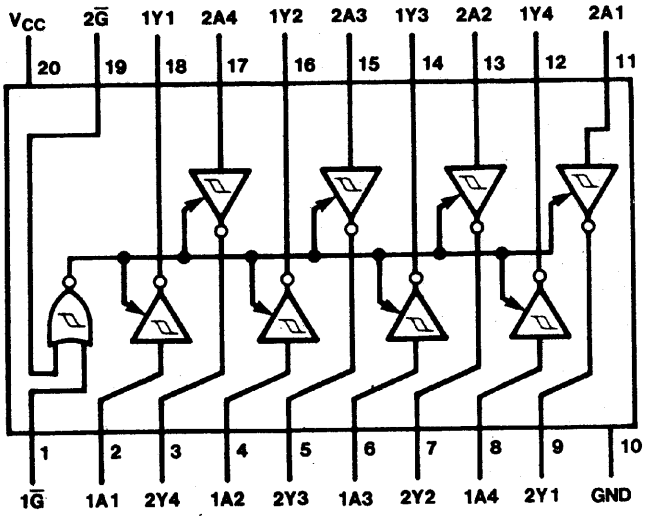


54LS670 (J,W); 74LS670 (N)

See page 6-239

Buffers/Line Drivers/Line Receivers

940 Octal TRI-STATE®

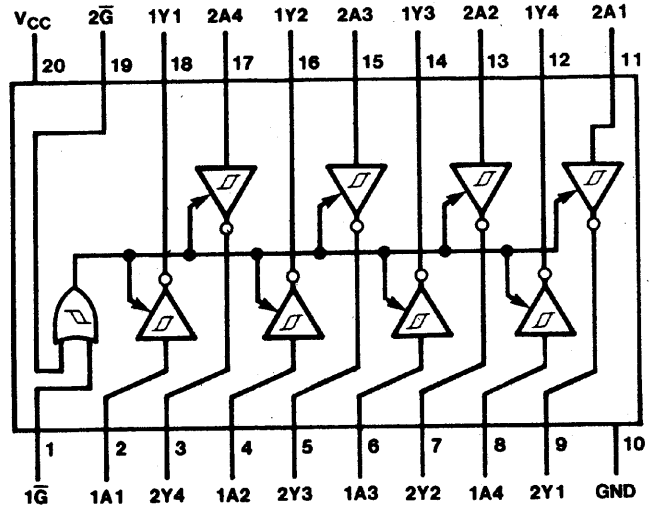


54S940 (J); 74S940 (N)

See page 5-53

Buffers/Line Drivers/Line Receivers

941 Octal TRI-STATE®

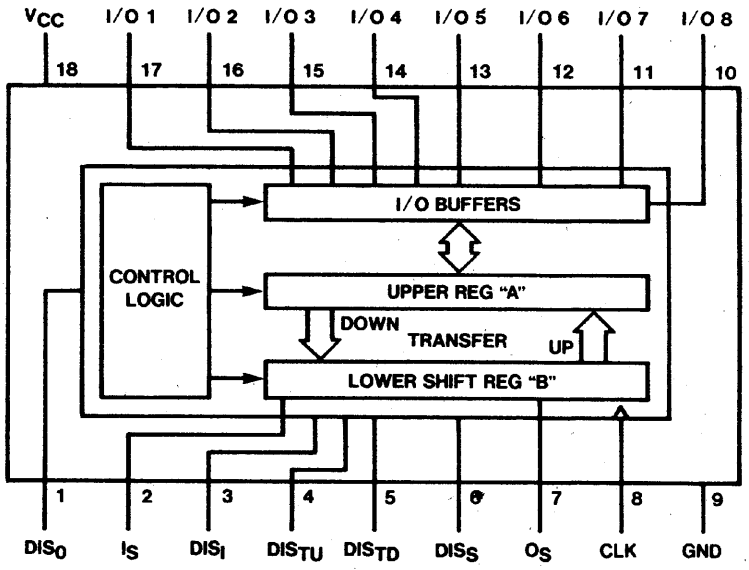


54S941 (J); 74S941 (N)

See page 5-53

Dual Rank 8-Bit TRI-STATE Shift Register

952 Synchronous Clear
962 Exchange Data Between Registers A & B



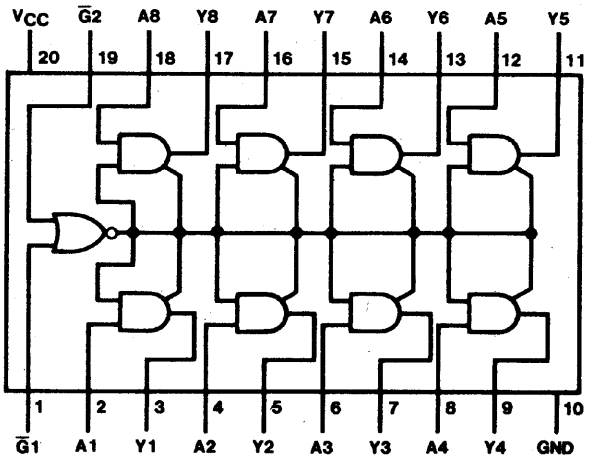
54LS952 (J) 74LS952 (N)
54LS962 (J) 74LS962 (N)

See page 6-243

Octal Buffers/Line Drivers/Line Receivers

71LS95A Noninverted TRI-STATE® Outputs

Inputs			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L



71LS95A (J); 81LS95A (N)

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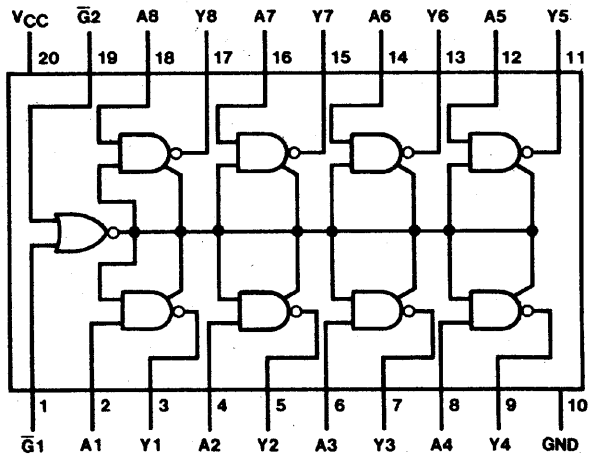
Octal Buffers/Line Drivers/Line Receivers

71LS96A Inverted TRI-STATE Outputs

Inputs			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H



71LS96A (J); 81LS96A (N)

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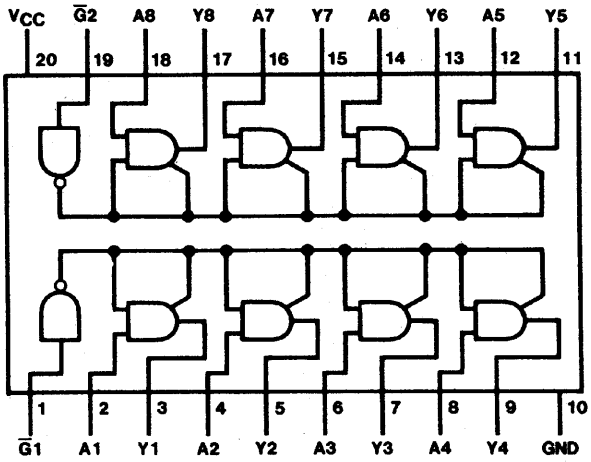
Octal Buffers/Line Drivers/Line Receivers

71LS97A Noninverted TRI-STATE Outputs

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L



71LS97A (J); 81LS97A (N)

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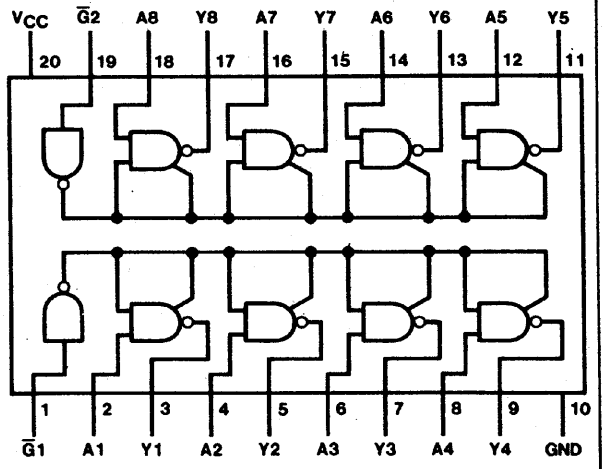
71LS98A Inverted TRI-STATE® Outputs

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H



71LS98A (J); 81LS98A (N)

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