

3D Silicon Nanowire FET

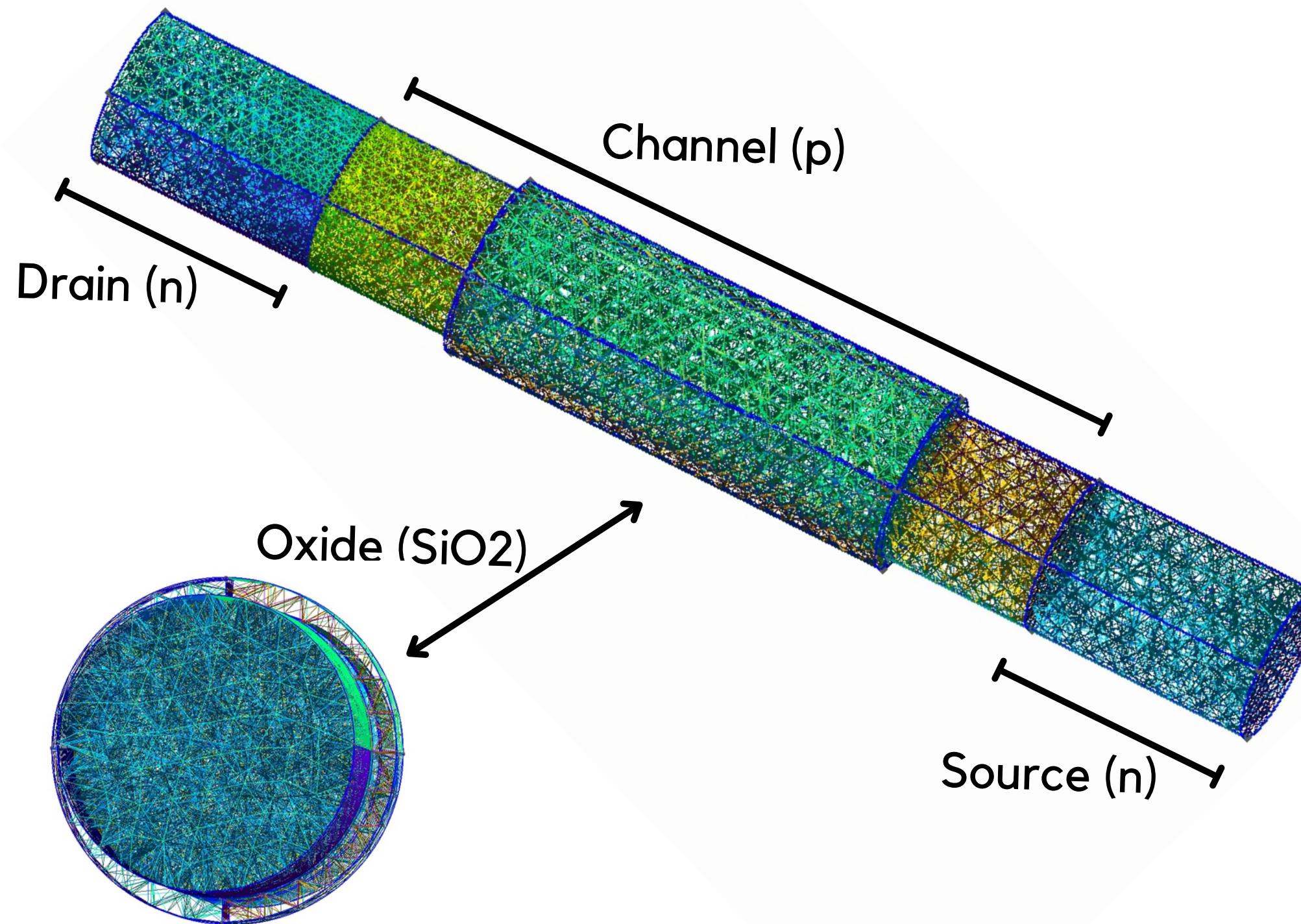
Nanoelectronics
Simulation Laboratory 3

Department of Electrical
and Computer
Engineering

Tutor: Manuel Gößwein

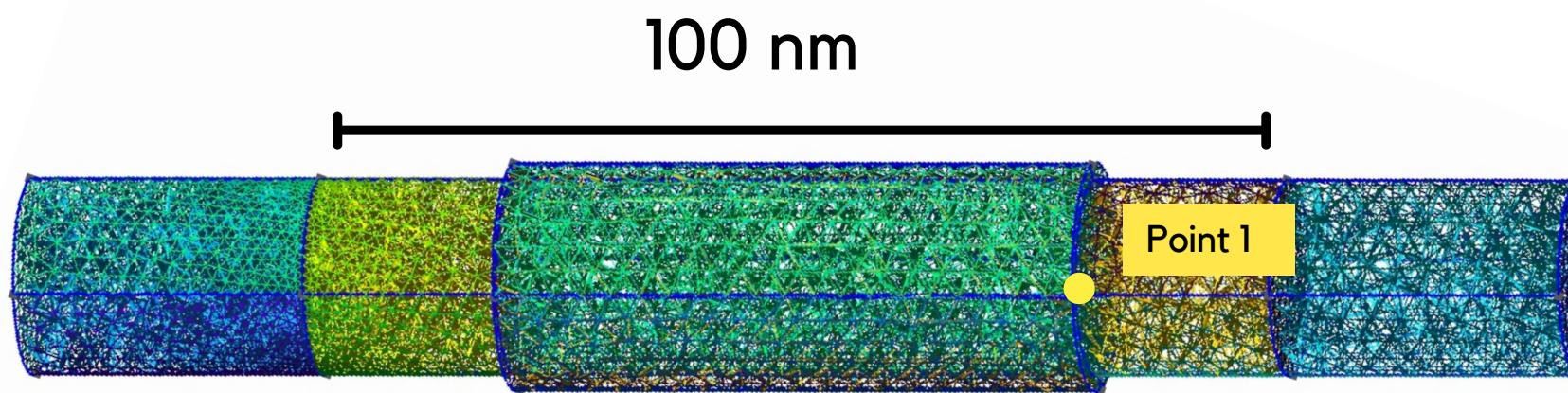
Team:
Sarahí José Aguilar
Luis Antonio Durán Soto
Francesco Conoscenti
Luca Rommeis

.geo geometry file

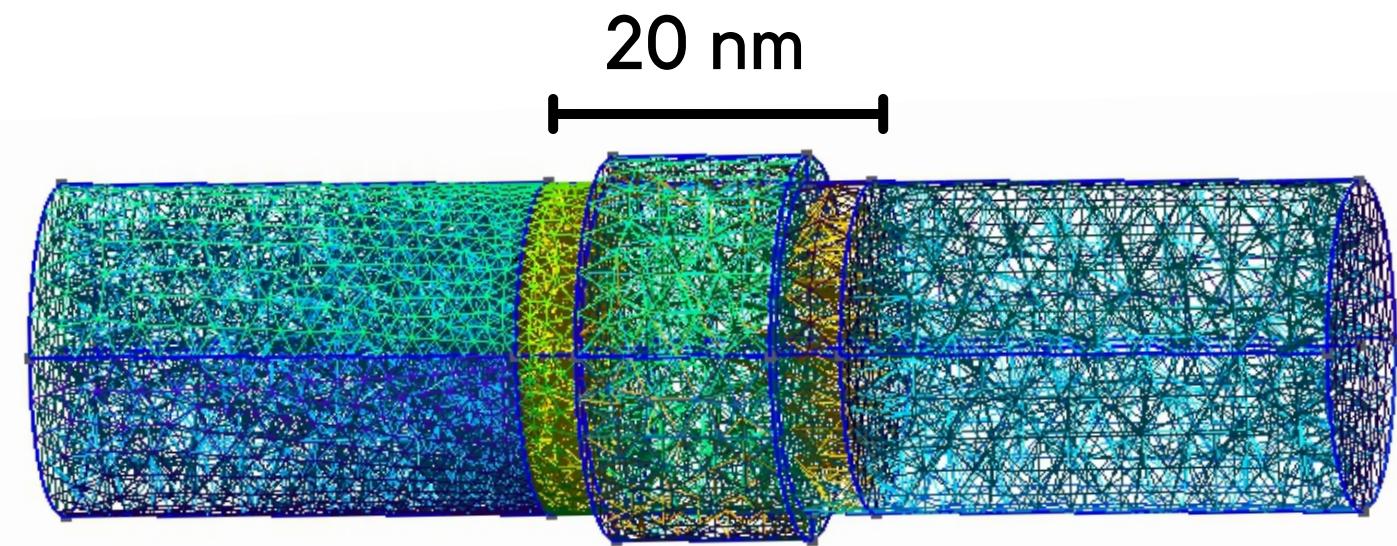


```
// Definition physical entities  
Physical Surface("drain") = {323};  
Physical Surface("gate") = {49, 21, 33, 37};  
Physical Surface("source") = {237};  
  
Physical Volume("oxide") = {3, 2};  
Physical Volume("channel") = {1, 4, 6};  
Physical Volume("drain_region") = {7};  
Physical Volume("source_region") = {5};
```

Channel Length



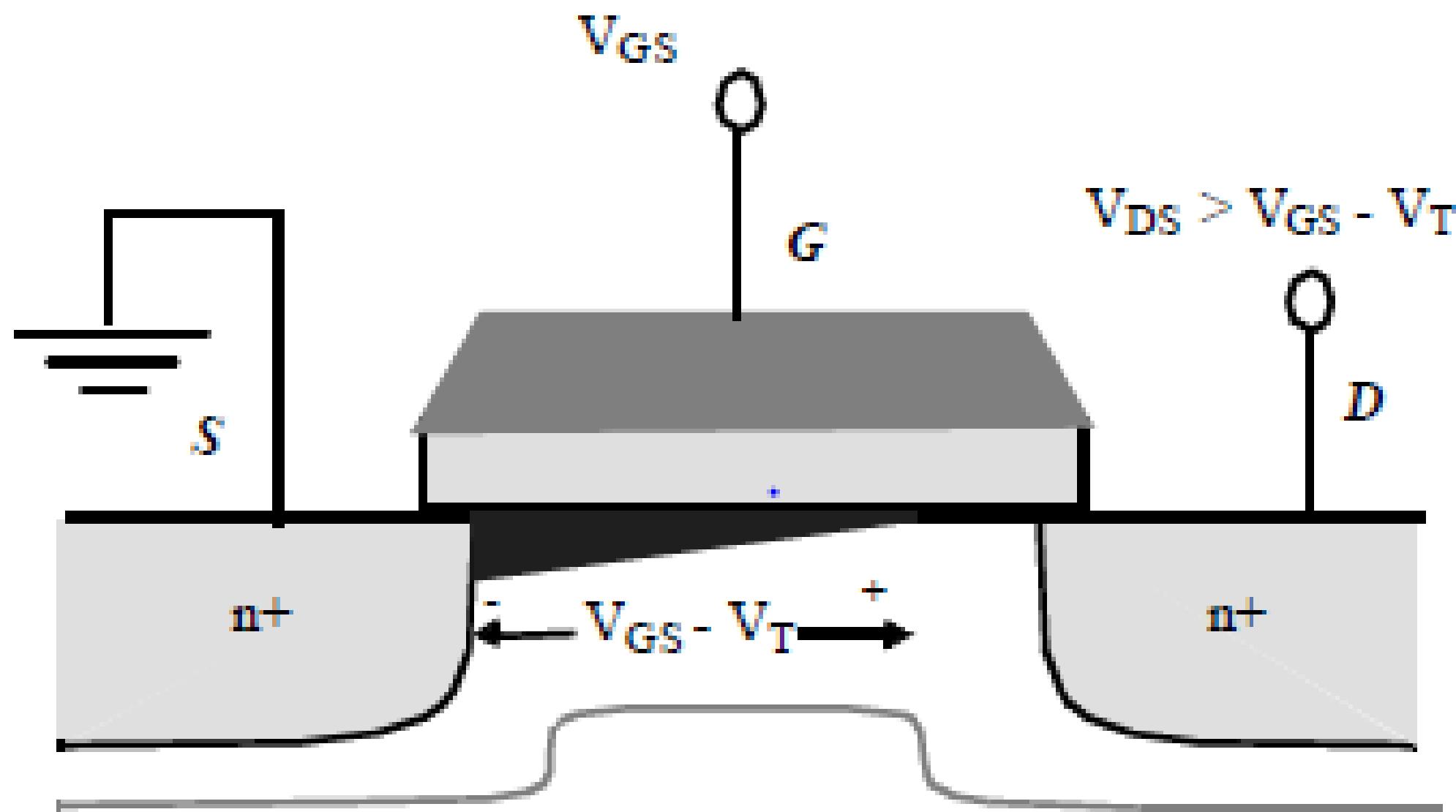
```
Point(1) = {10, 10, 0, lc1};  
....  
Extrude {0, 0, 60} {  
    Line{2, 6, 7, 3, 4, 8, 5, 1};  
}  
...  
Extrude {0, 0, -20} {  
    Point{1, 3, 4, 2};  
}  
...  
Extrude {0, 0, 20} {  
    Point{16, 18, 10, 13, 12};  
}
```



```
Point(1) = {10, 10, 0, lc1};  
....  
Extrude {0, 0, 12} {  
    Line{2, 6, 7, 3, 4, 8, 5, 1};  
}  
...  
Extrude {0, 0, -4} {  
    Point{1, 3, 4, 2};  
}  
...  
Extrude {0, 0, 4} {  
    Point{16, 18, 10, 13, 12};  
}
```

Mesh and its refinement in different regions

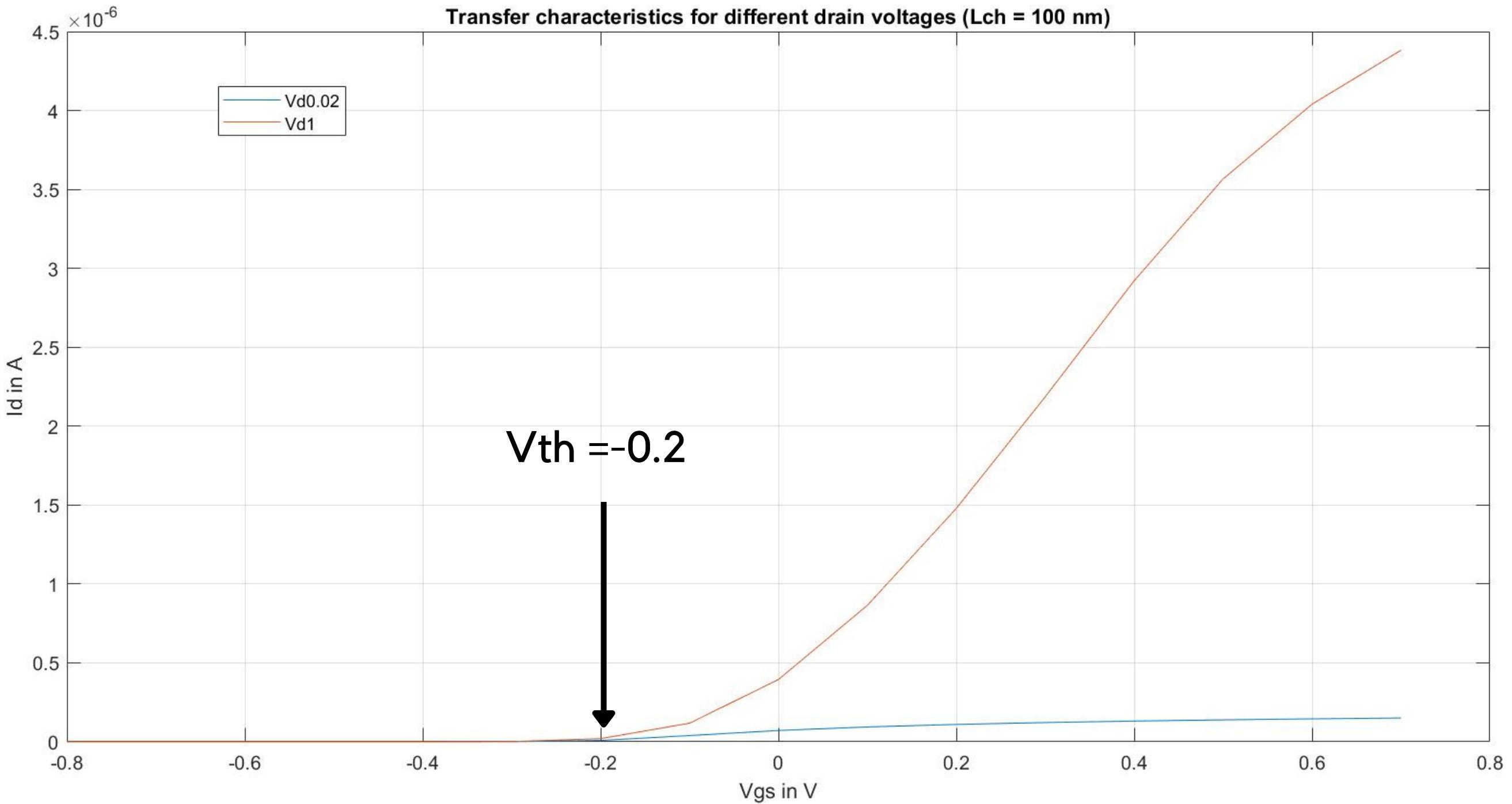
MOSFET



Mesh is finer near the drain for simulating precisely the part of the pinch off in the channel

Threshold voltage

Transfer Characteristics in linear scale
100 nm



Voltage applied to the gate that is enough to turn on the transistor.

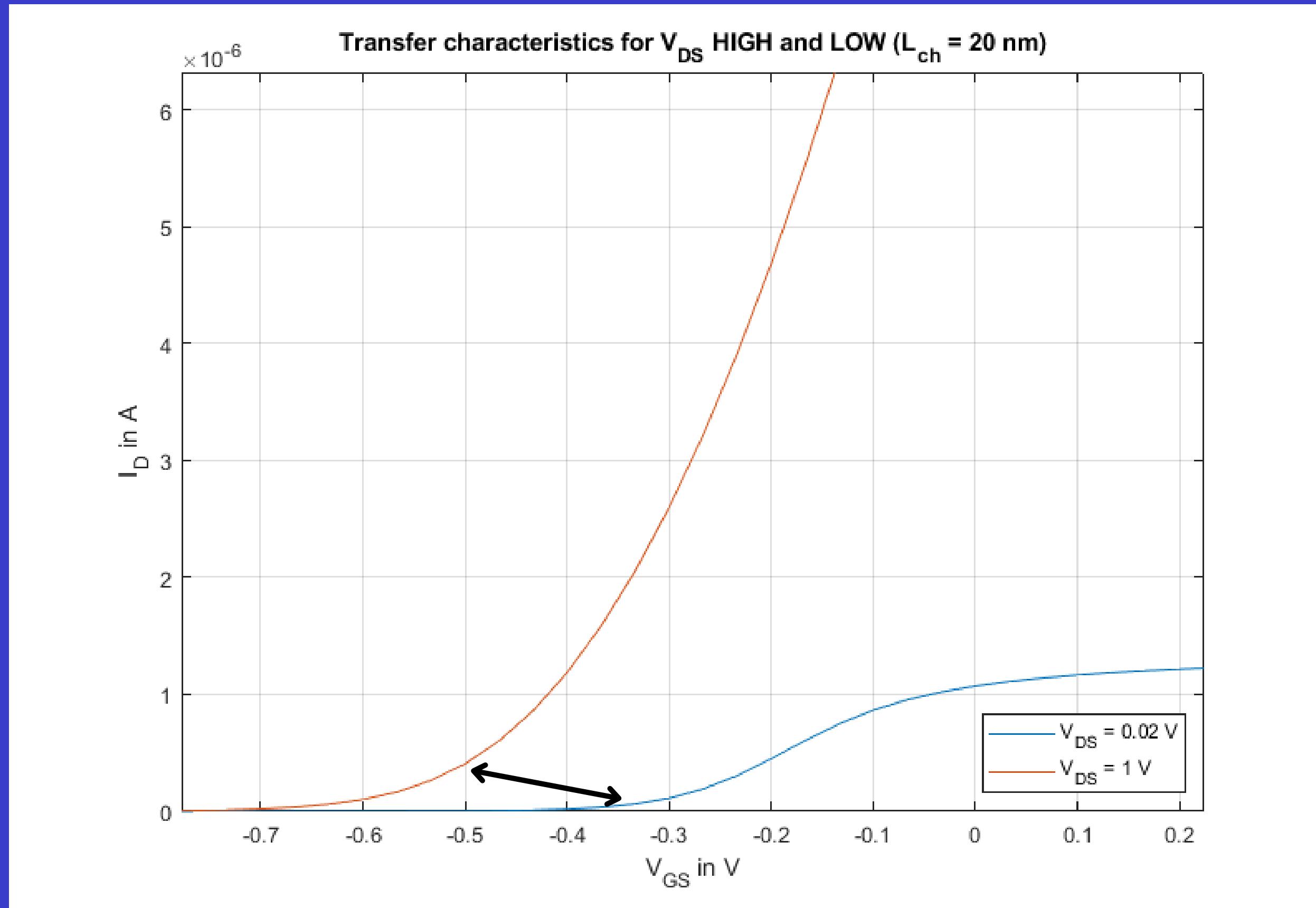
It starts conducting current between the source and drain terminals.

Inversion

Negative $V_{th} = -0.2 \text{ V}$
(unusual)

Depletion mode
FET

Transfer Vd HIGH and LOW



The threshold voltages differ for Vd HIGH and LOW

100nm VS 20nm Vth

$$V_{th} \text{ 100nm} = -0.2 \text{ V}$$

$$V_{th} \text{ 20nm} = -0.35 \text{ V}$$

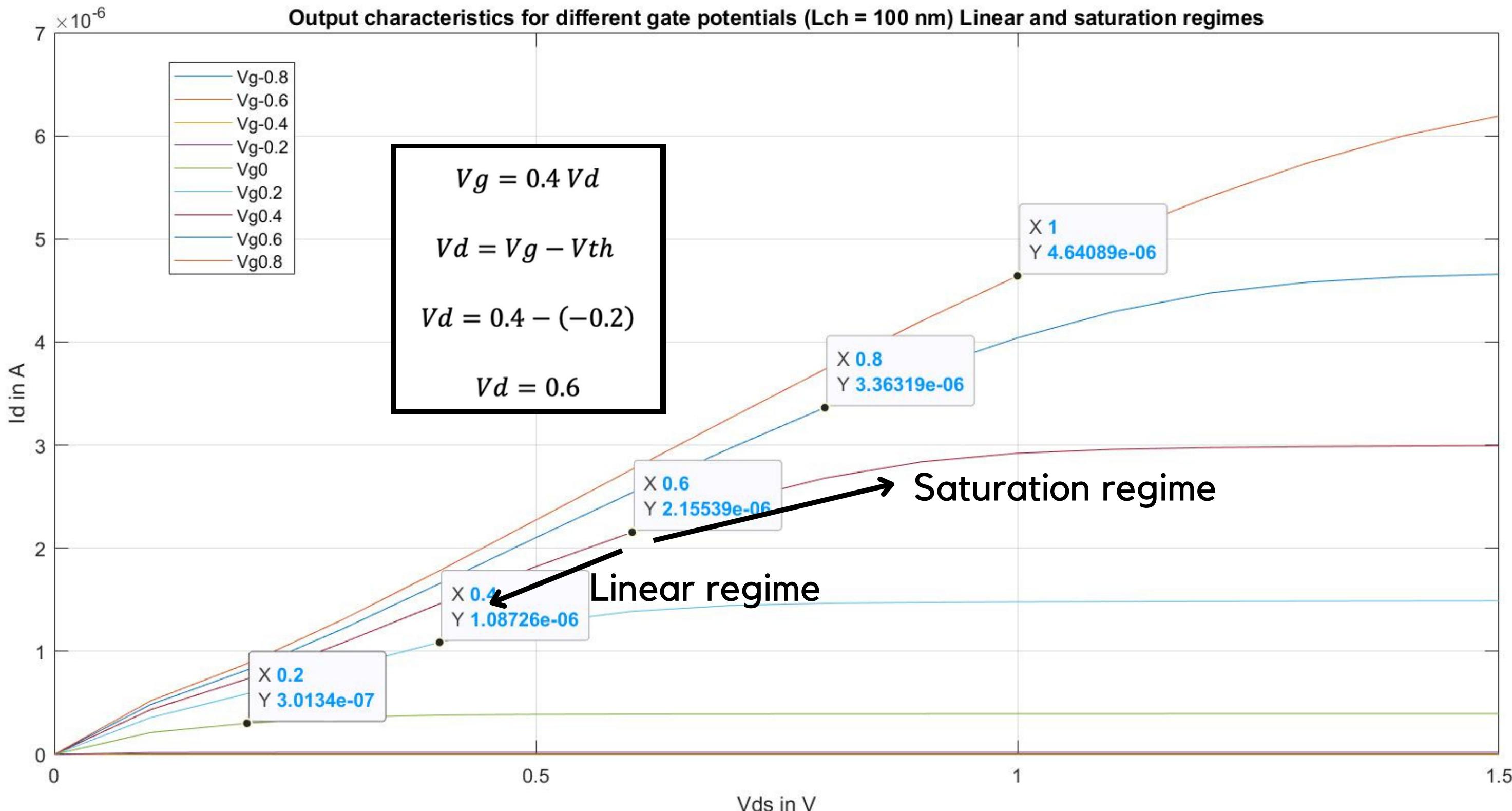
Due to the smaller
channel length the gate
capacitance decreases

$$\longrightarrow C = 2\pi\epsilon_0\epsilon_r \frac{l}{\ln \frac{R_2}{R_1}} \longrightarrow C \text{ is proportionally to } L$$

$$Q = \int_V \rho_q(\mathbf{r}) dV$$

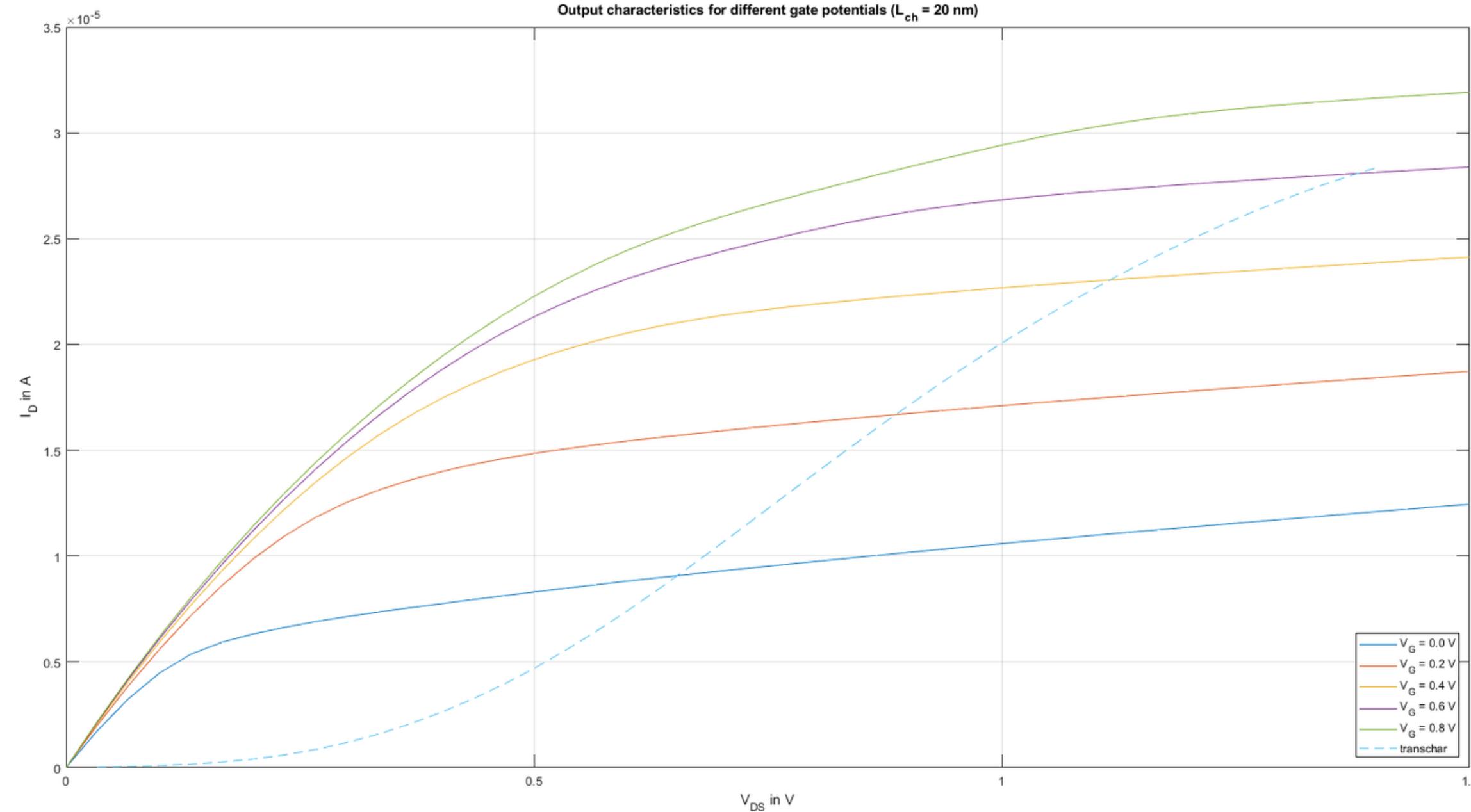
$$V_T = V_{FB} + 2\psi_B + \sqrt{4q\epsilon_{Si}N_A\psi_B}/C_{ox}$$

Linear and saturation regime

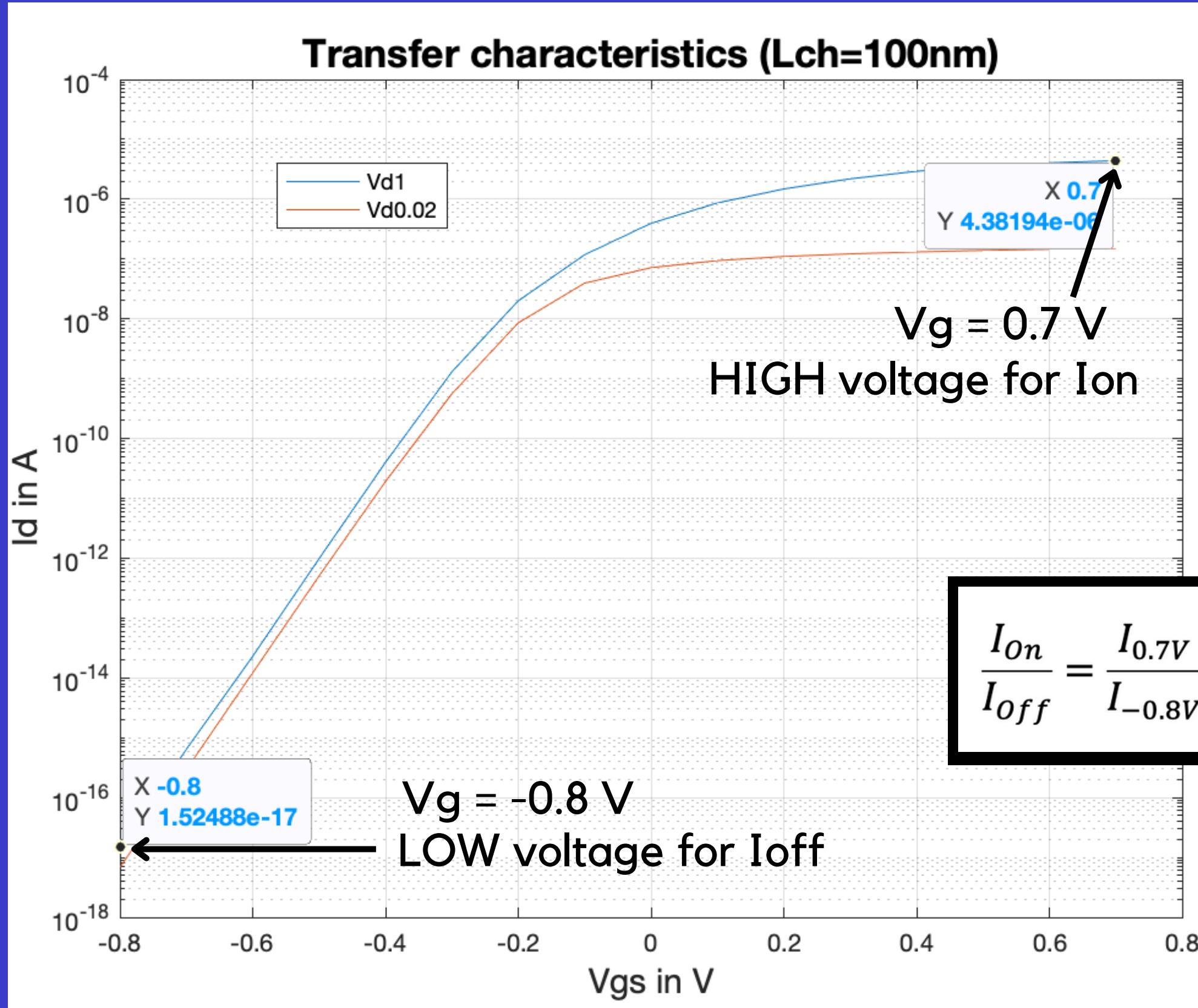


In order to increase the current you should change the gate voltage.

Output Characteristics for different Gate Potentials



The on and off currents for a drain voltage

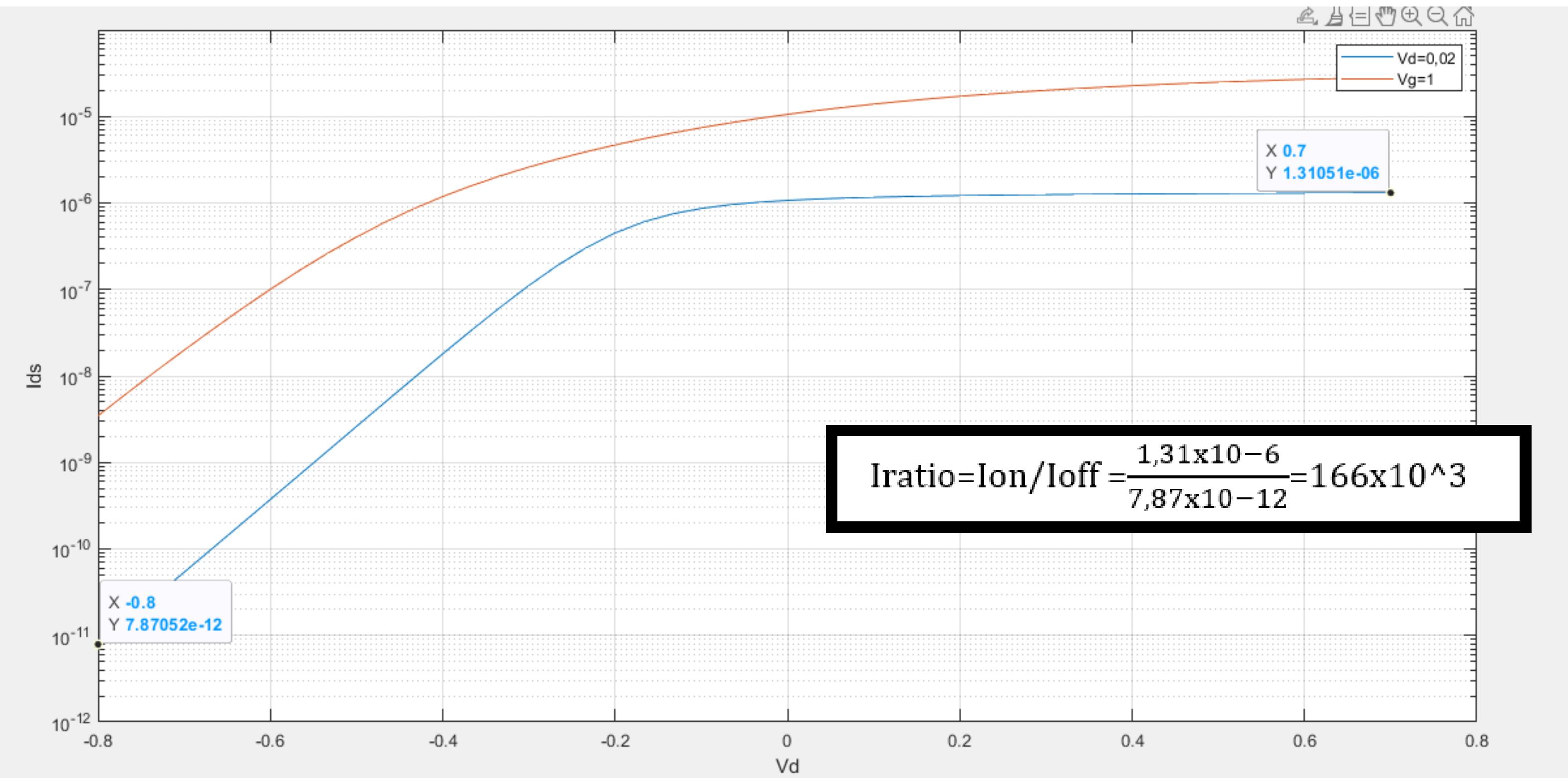


100 nm

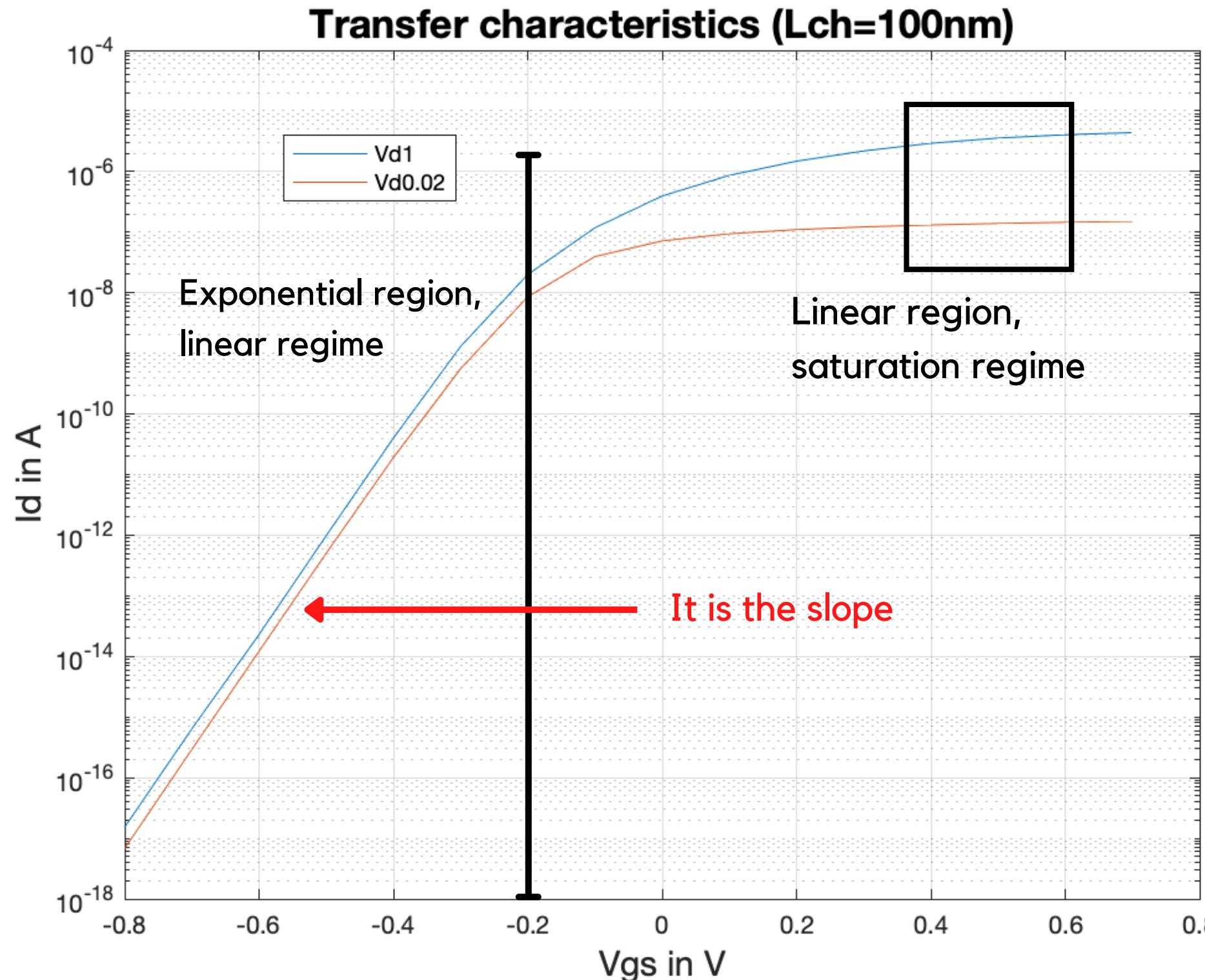
A high on-off ratio means a low leakage current

$$\frac{I_{On}}{I_{Off}} = \frac{I_{0.7V}}{I_{-0.8V}} = \frac{4.38194 \times 10^{-6} A}{1.51474 \times 10^{-17} A} = 2.89287 \times 10^{11} A$$

20 nm



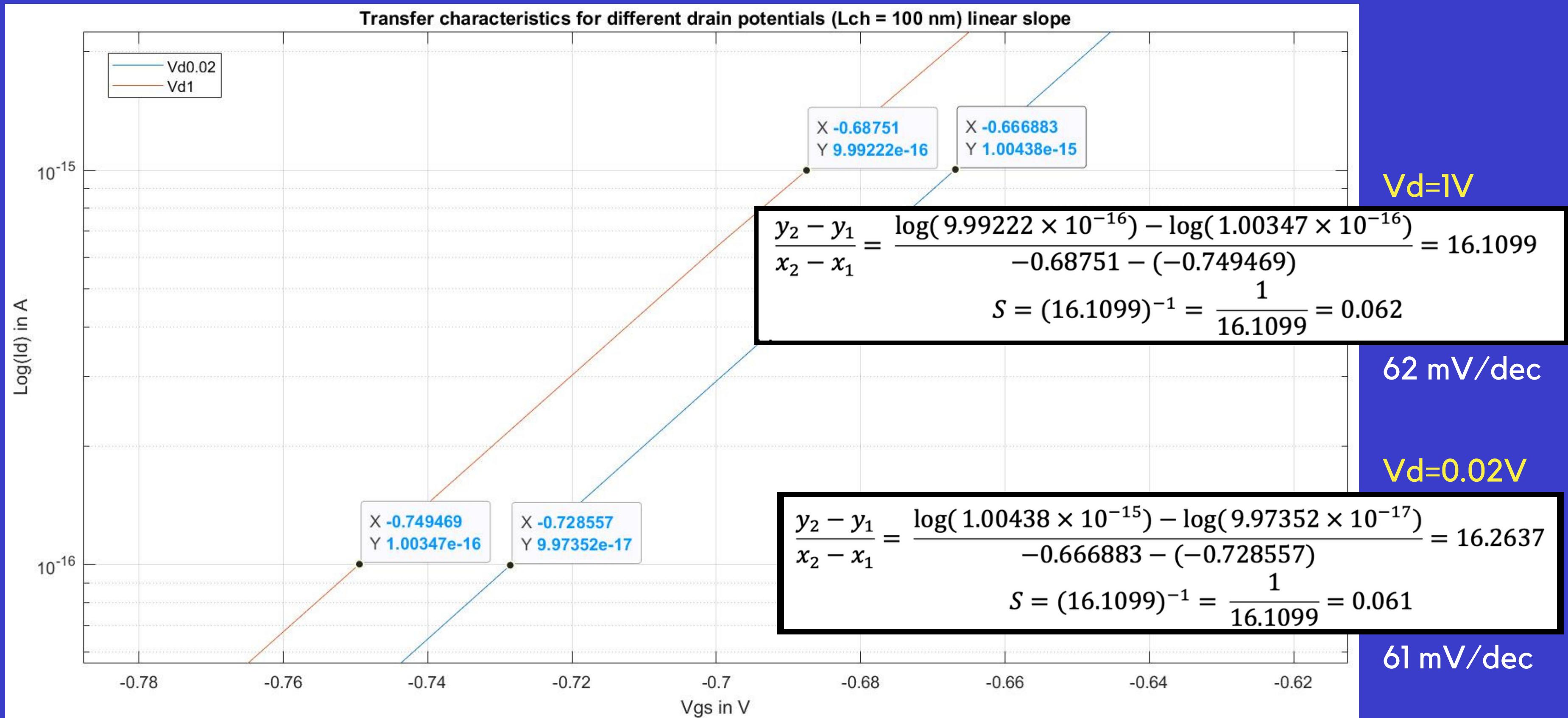
Sub-threshold slopes in linear and saturation regime 100 nm



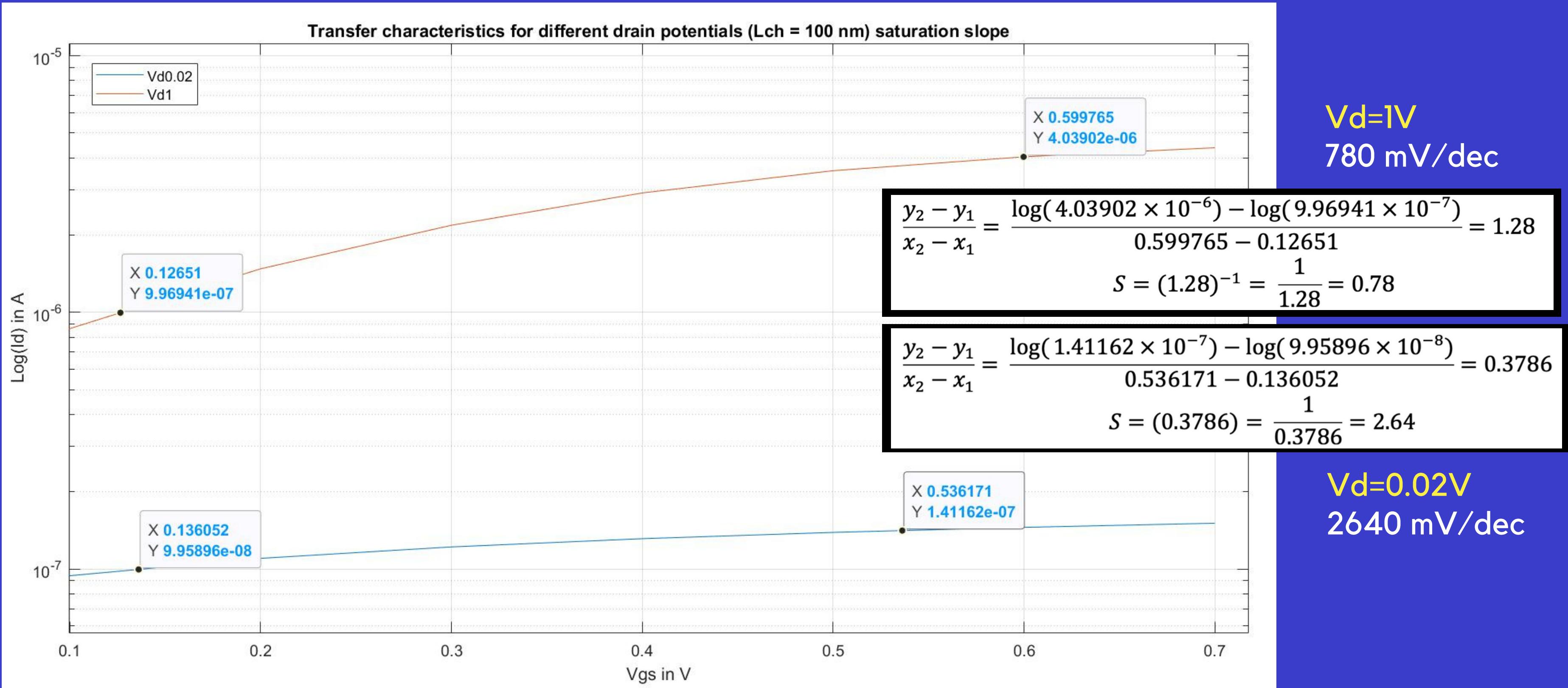
$$\text{Slope} = \frac{1}{S}$$

$$S = \left(\frac{\partial \log I_D}{\partial V_{GS}} \right)^{-1}$$

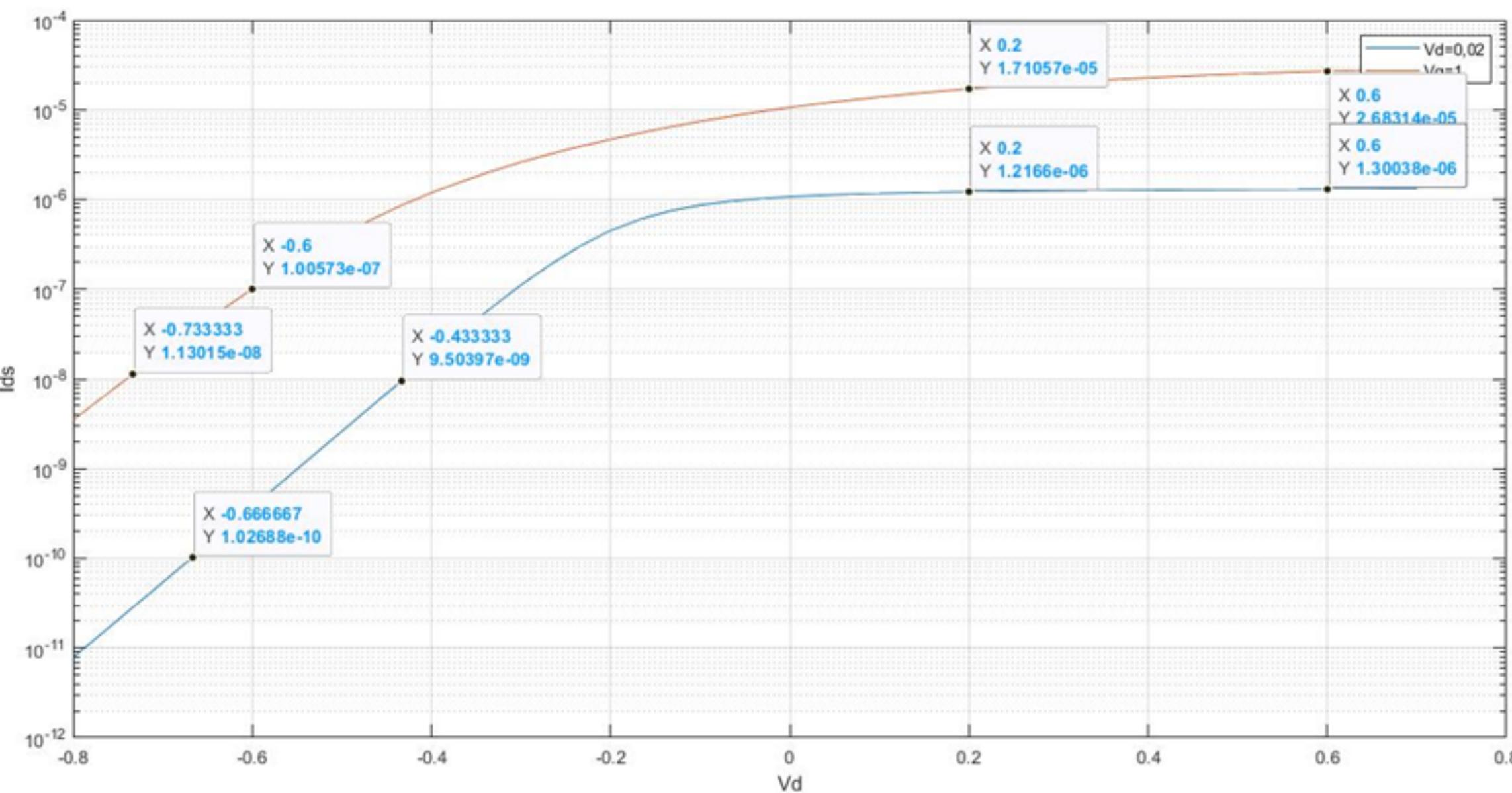
Linear regime 100 nm



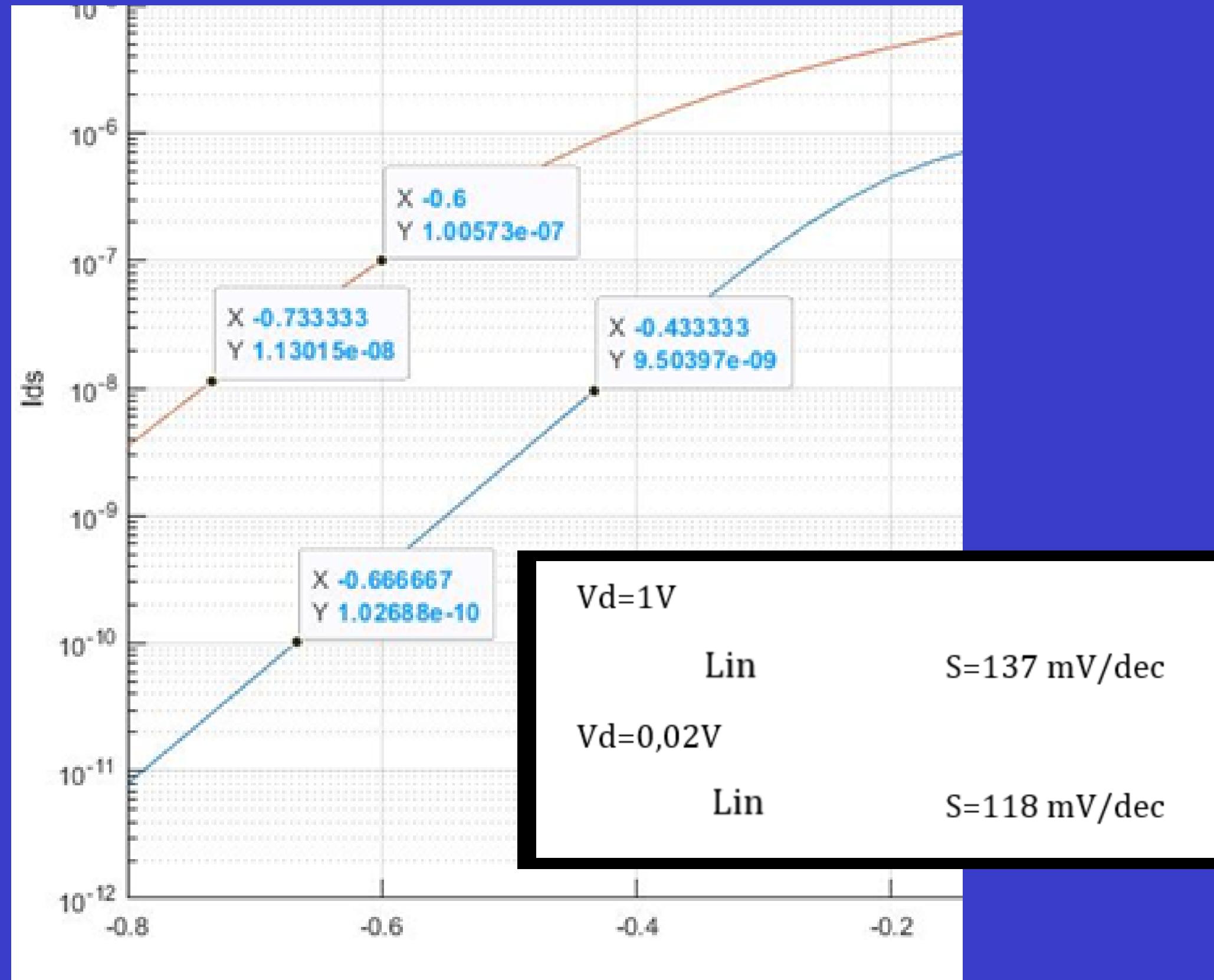
Saturation regime 100 nm



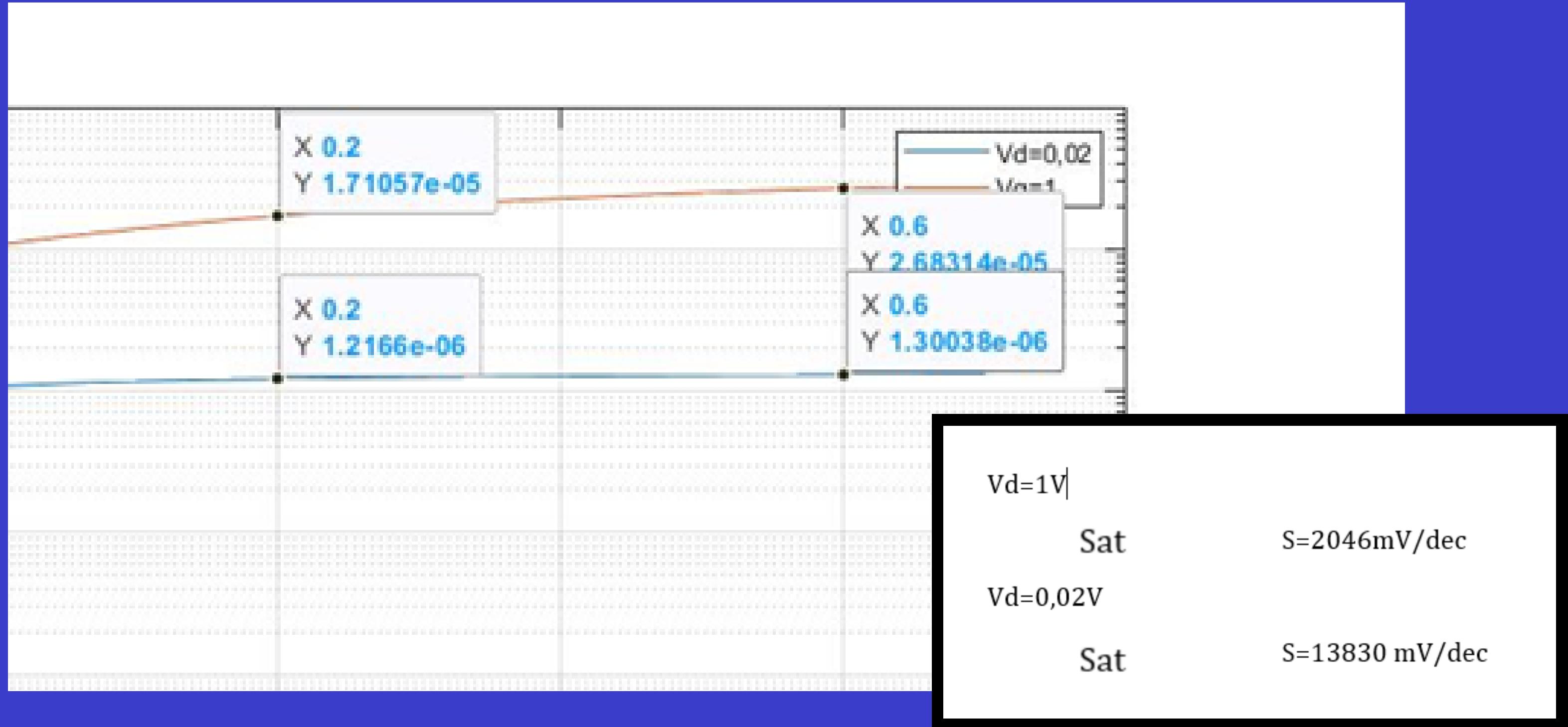
Sub-threshold slopes in linear and saturation regime 20 nm



Linear regime 20 nm



Saturation regime 20 nm



100nm VS 20nm Sub-threshold

Meaning of Subthreshold Swing

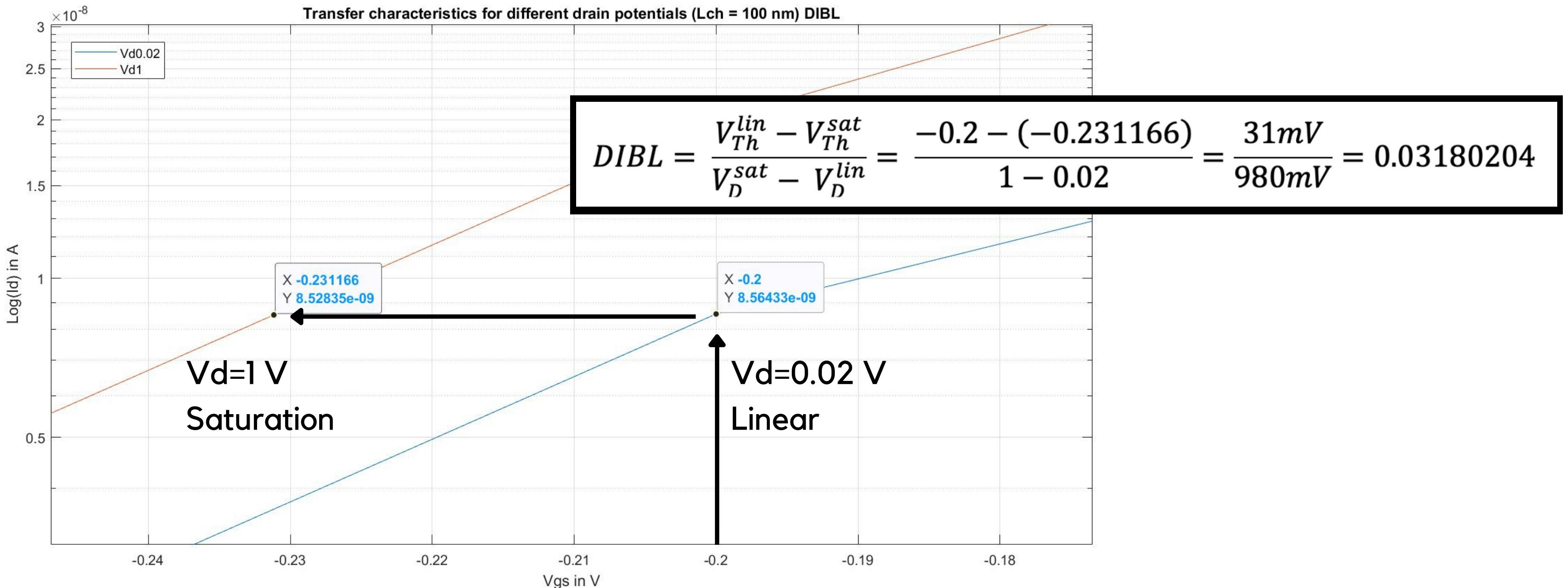
$$\begin{aligned} S &= \left(\frac{\partial \log(I_D)}{\partial V_{GS}} \right)^{-1} = \ln(10) \left(\frac{\partial I_D}{\partial V_{GS}} \frac{1}{I_D} \right)^{-1} \\ &= \ln(10) \left(\frac{\partial I_D}{\partial \Phi_f^0} \frac{\partial \Phi_f^0}{\partial V_{GS}} \frac{1}{I_D} \right)^{-1} = \ln(10) \left(\frac{\partial I_D}{\partial \Phi_f^0} \frac{\partial \Phi_f^0(-q)}{\partial \Phi_G} \frac{1}{I_D} \right)^{-1} \\ &\quad \nearrow \\ \Phi_G &= -qV_{GS} \end{aligned}$$

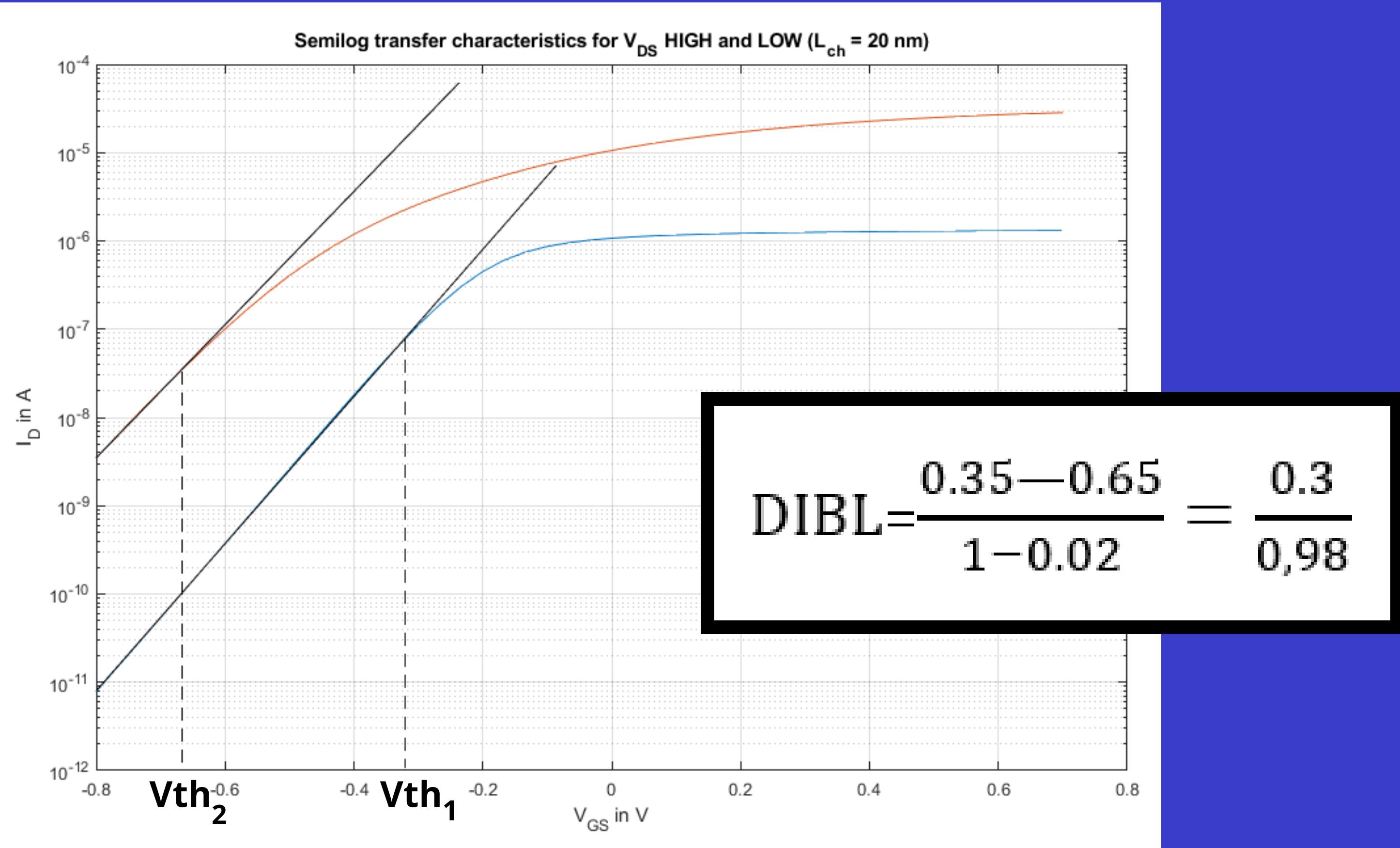
The subthreshold swing is a parameter that tells you how fast or how efficiently a transistor can switch from off to on. With higher slopes the current grows faster.

$$S = \frac{k_B T}{|q|} \ln(10) \left(\frac{\partial \Phi_f^0}{\partial \Phi_G} \right)^{-1}$$

$$S_{s-th} = \ln(10) \frac{kT}{q} \left(1 + \frac{C_d}{C_{ox}} \right)$$

Drain-induced barrier lowering (DIBL)

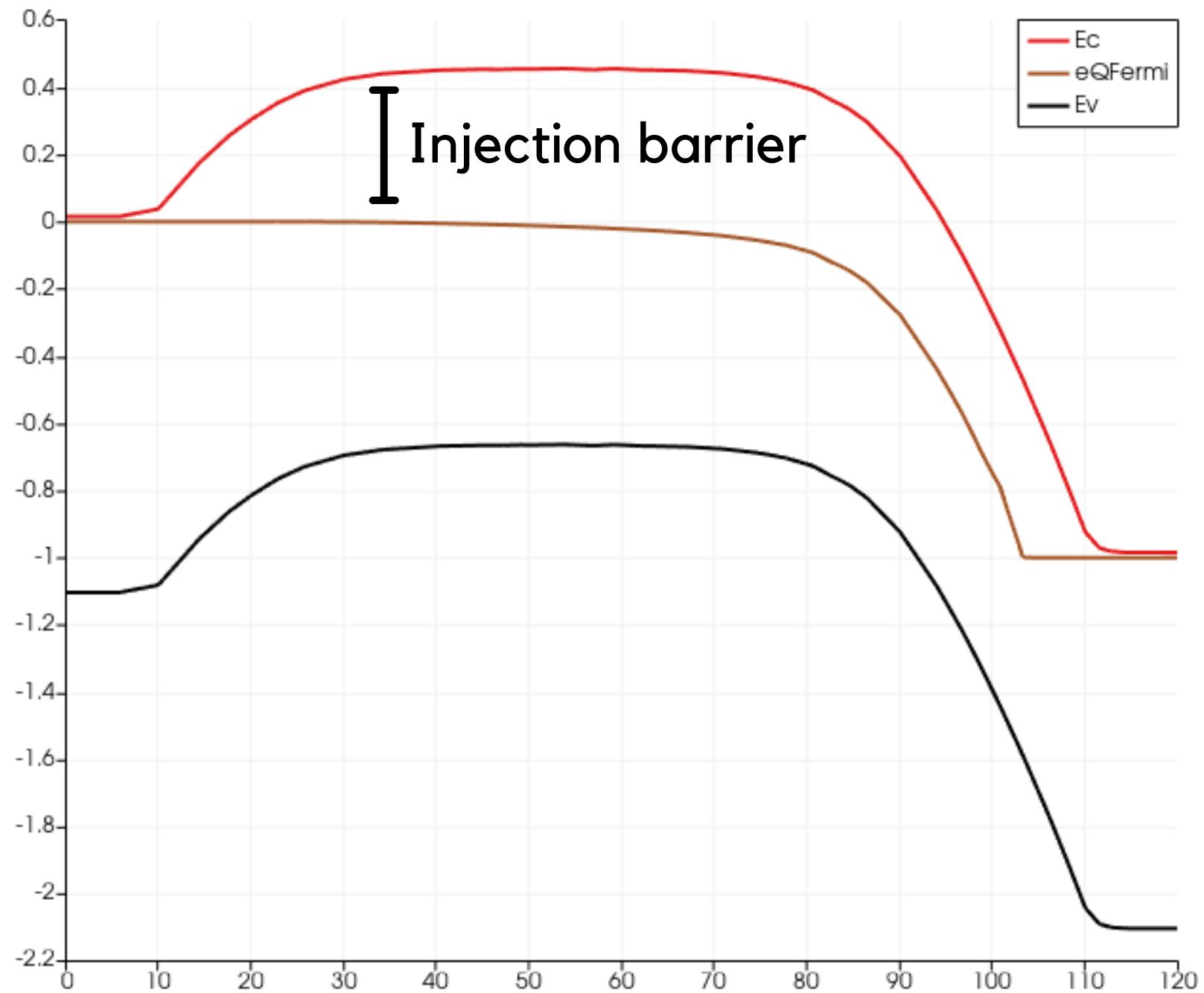




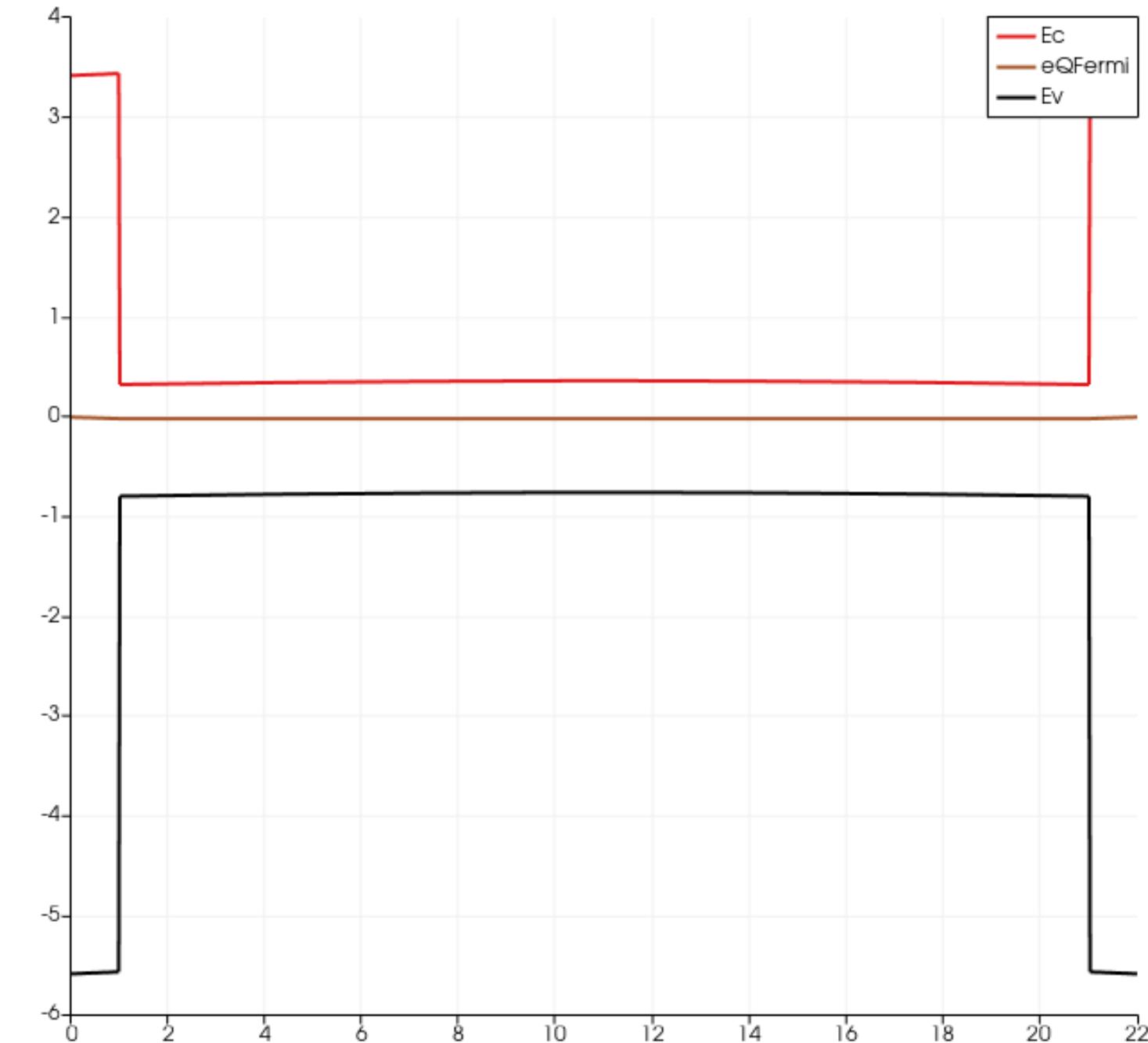
Along and across the channel $V_G < V_{th}$

100 nm

Off state



Along the channel $V_g = -0.5V$, with $V_d = 1V$

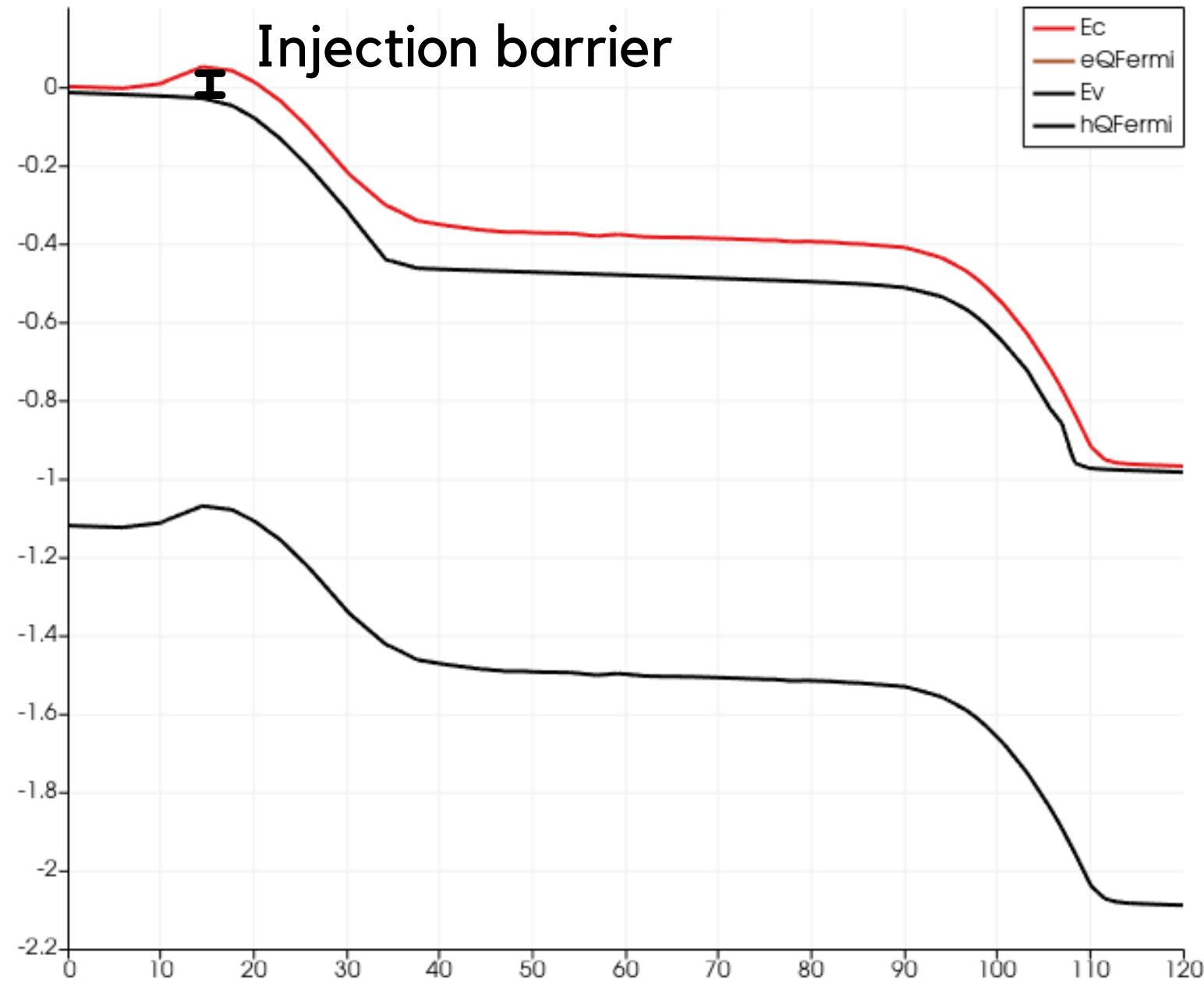


Across the channel $V_g = -0.5V$, with $V_d = 1V$

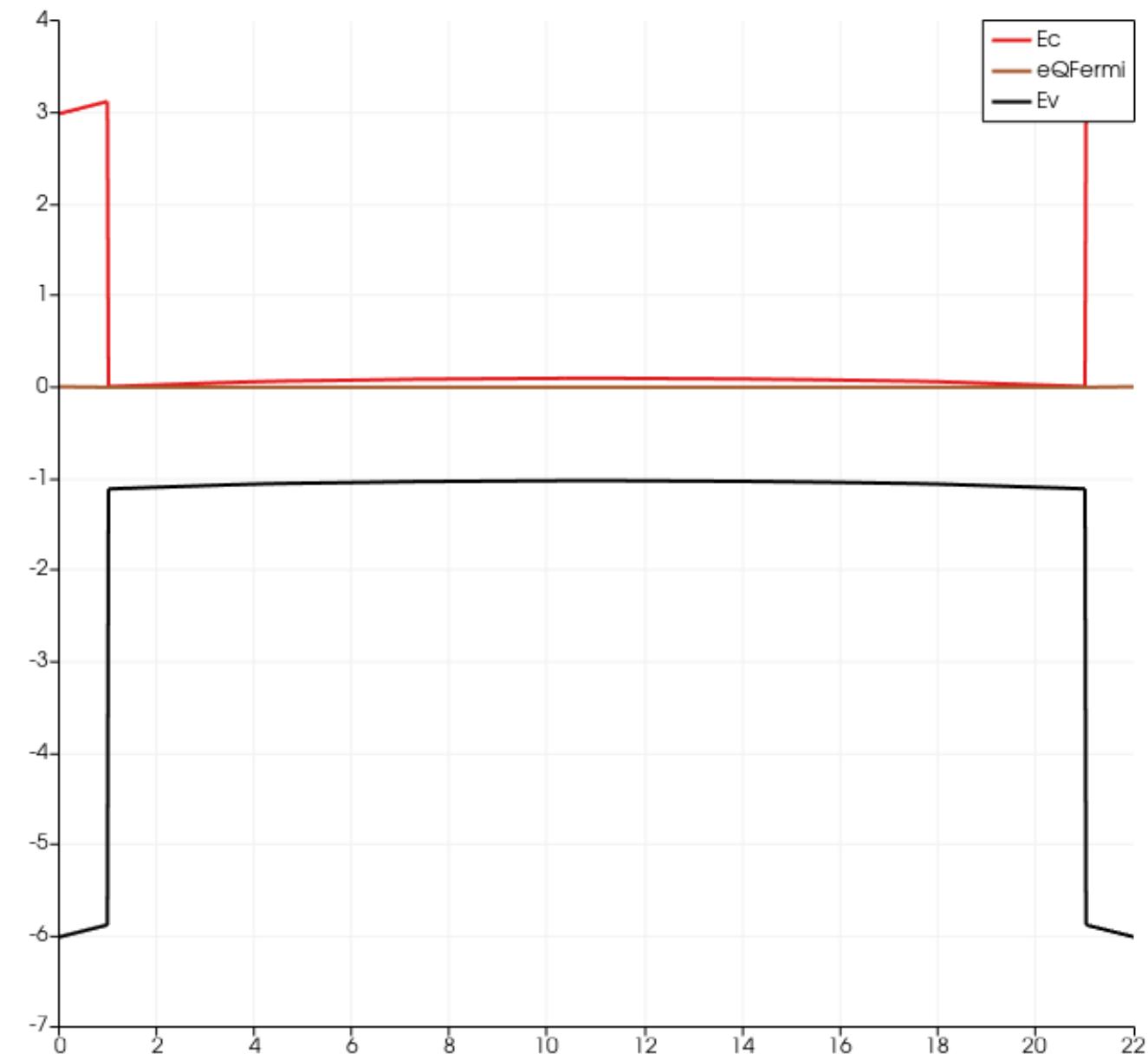
Along and across the channel $V_G > V_{th}$

100 nm

On state



Along the channel $V_g=0.5V$, with $V_d=1V$

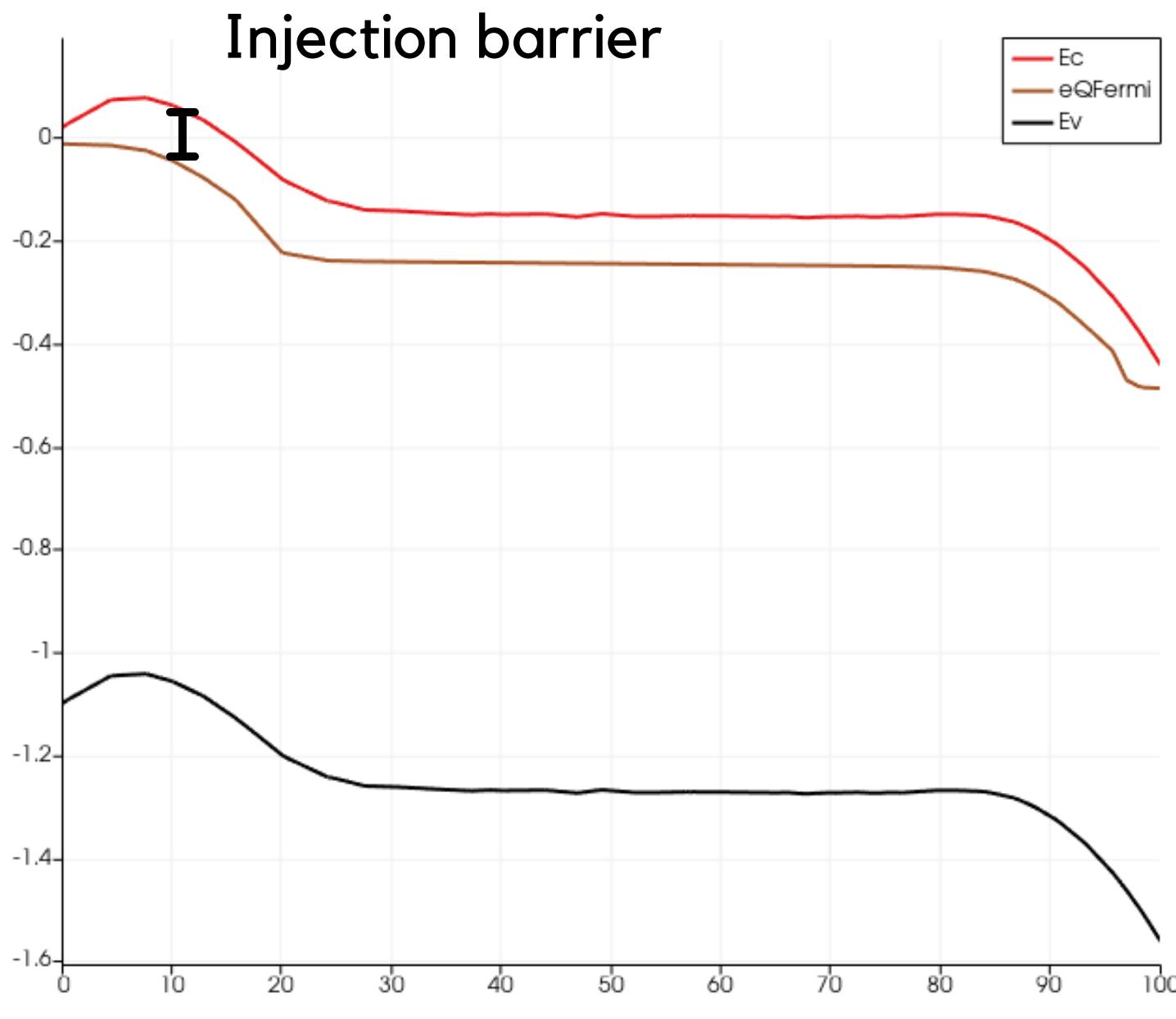


Across the channel $V_g=0.5V$, with $V_d=1V$

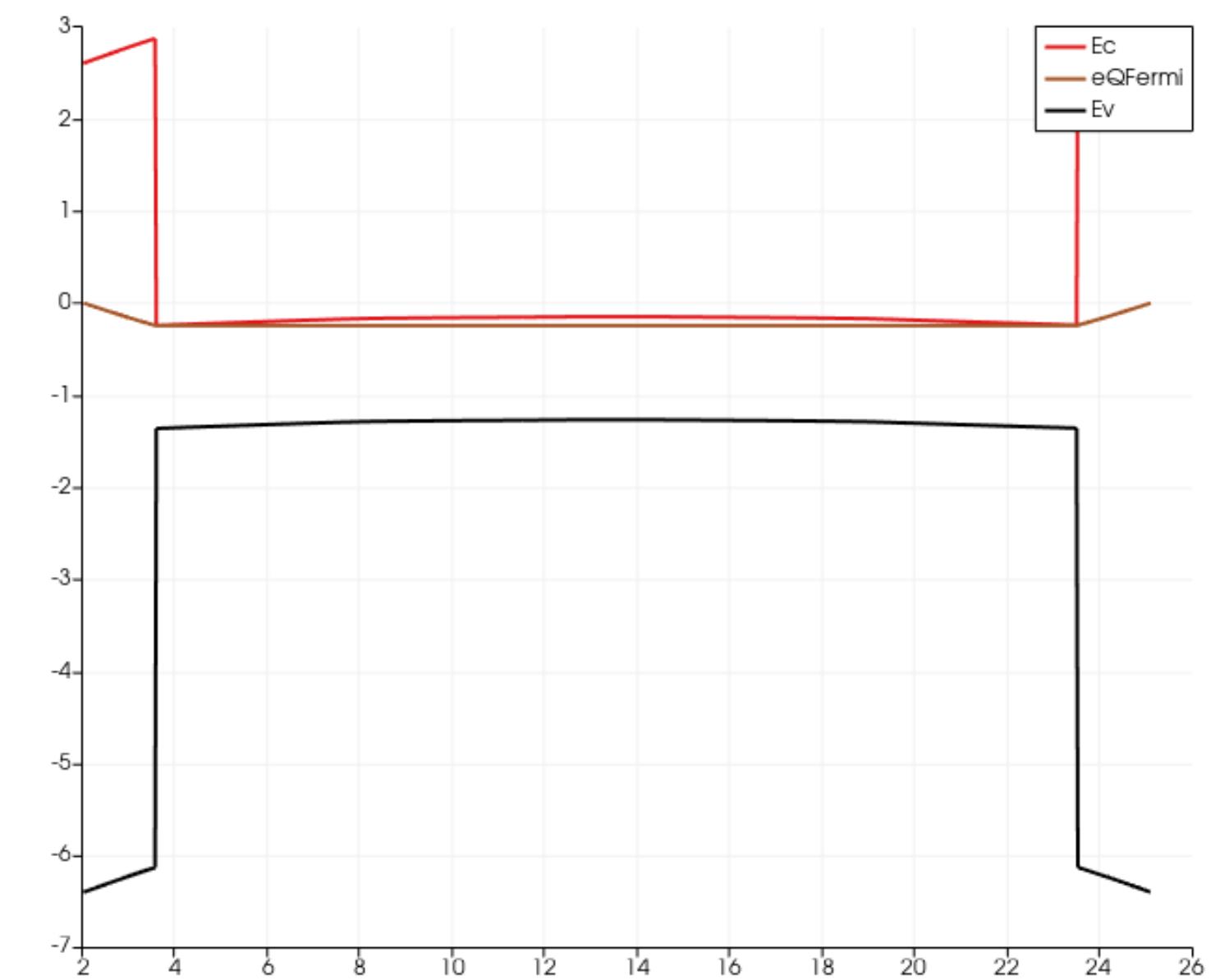
Along and across the channel - Linear

100 nm

On state



Along the channel $V_d=0.5V$, with $V_g= 4V$

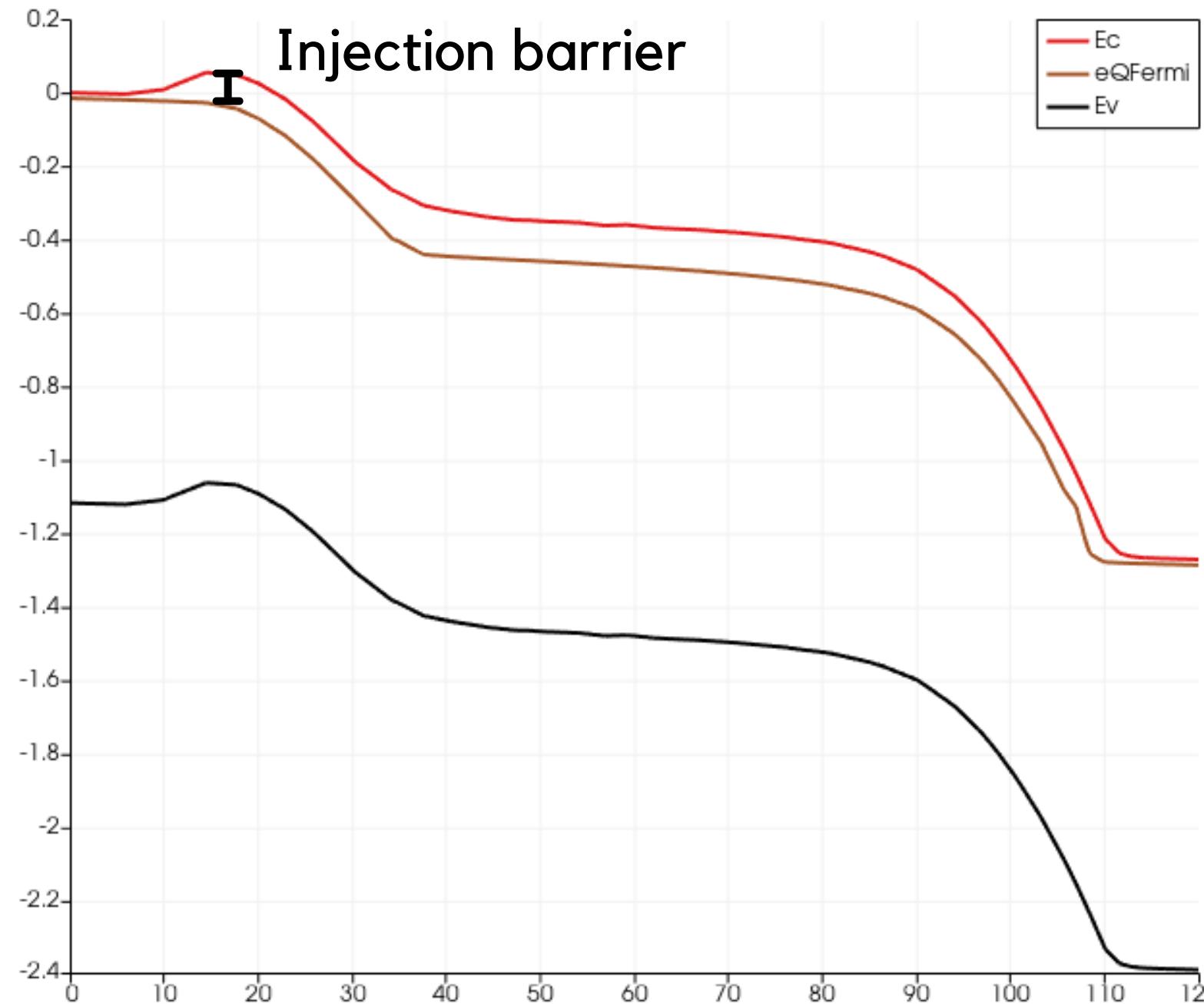


Across the channel $V_g=0.5V$, with $V_d= 4V$

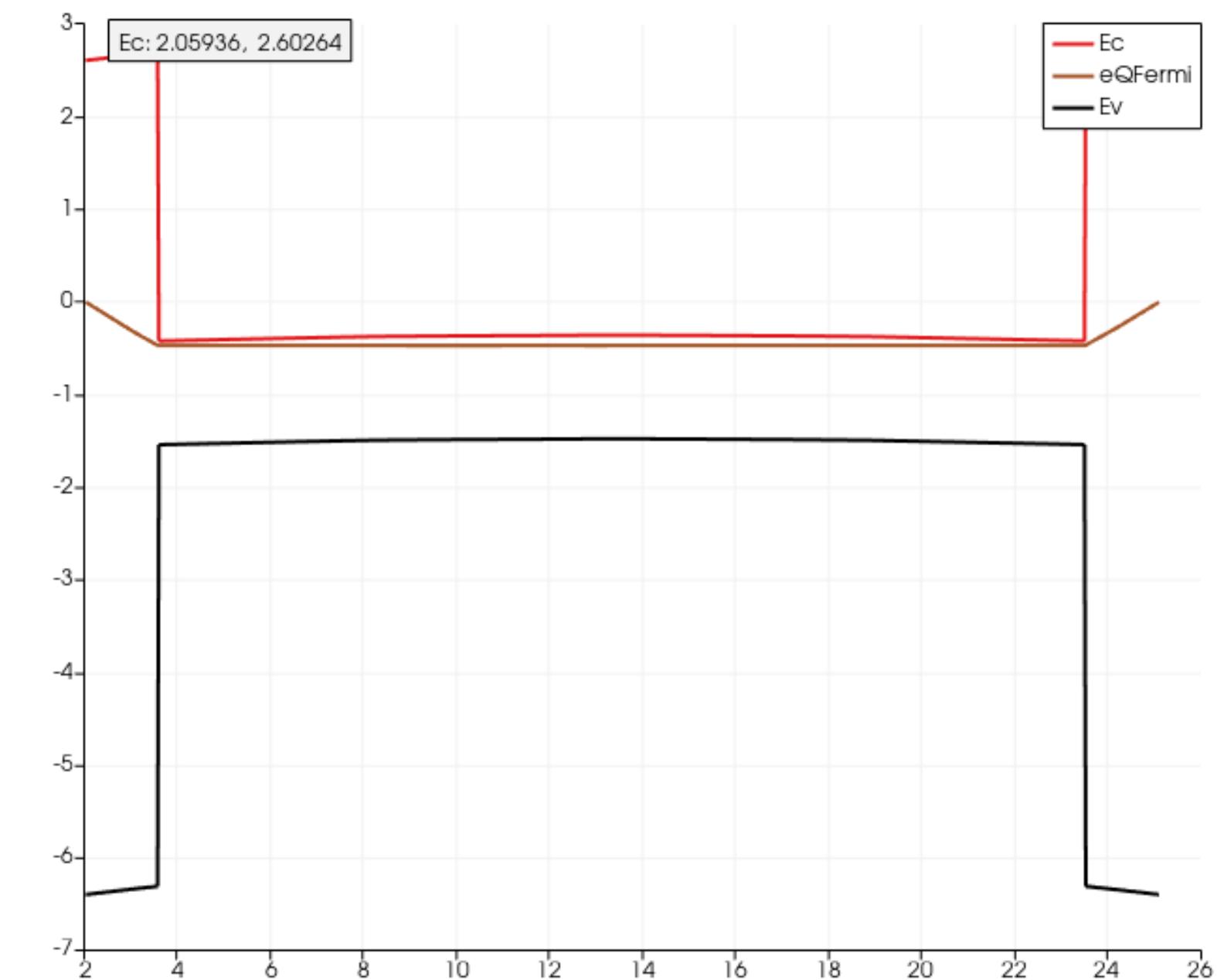
Along and across the channel - Saturation

100 nm

On state



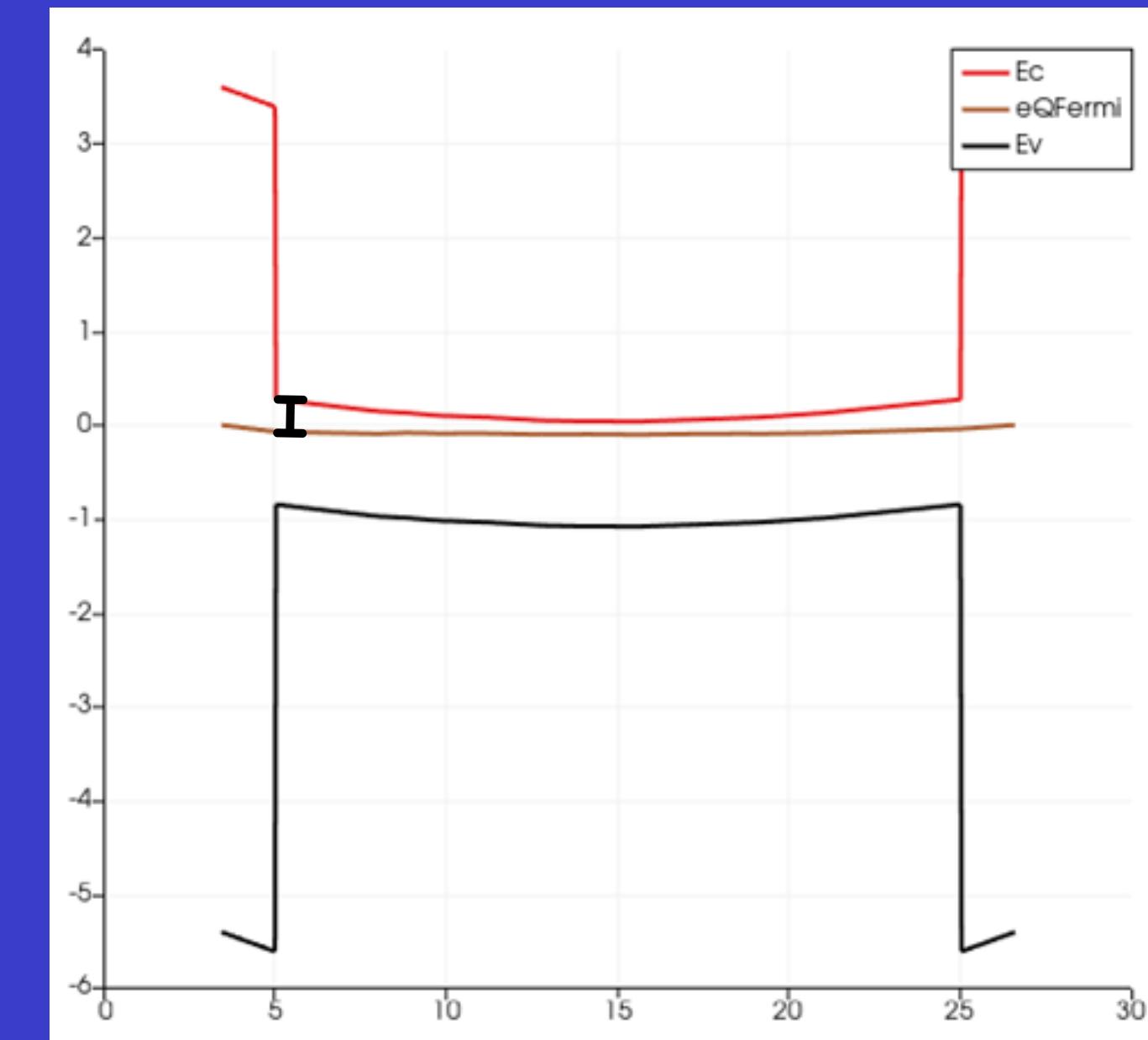
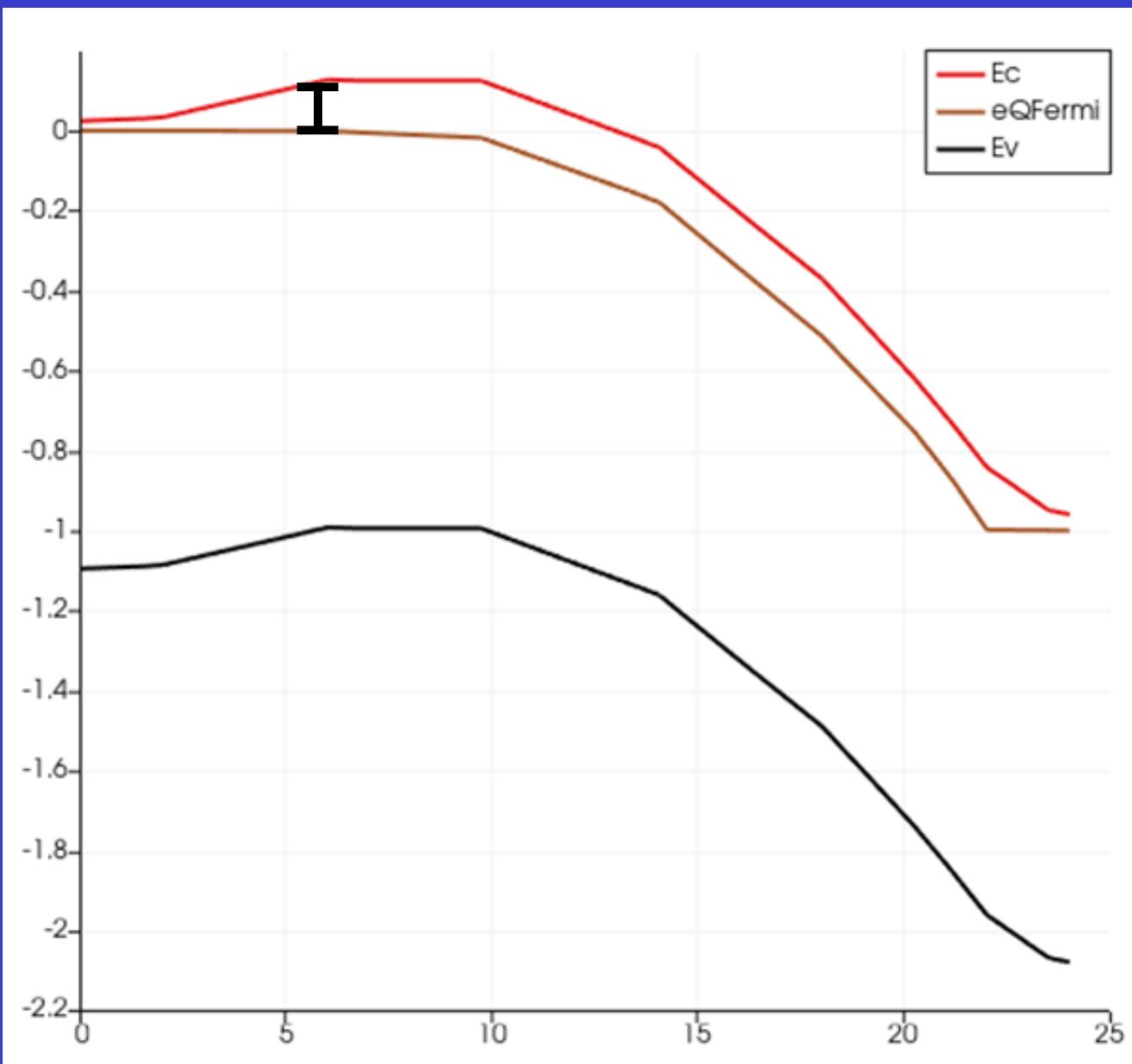
Along the channel $V_d=1.3V$, with $V_g= 0.4V$



Across the channel $V_g=1.3V$, with $V_d= 4V$

20nm

Along and across the channel: OFF

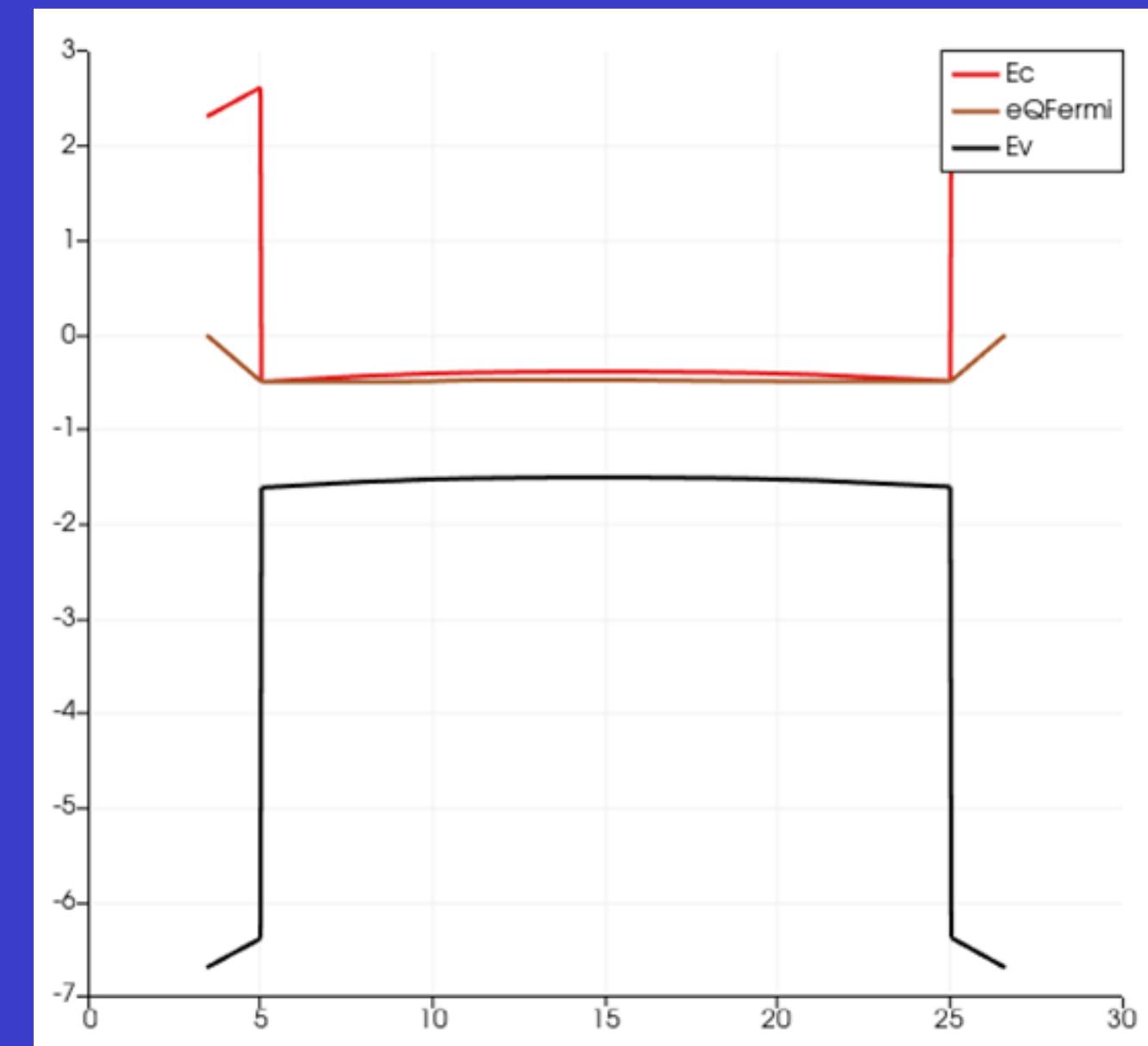
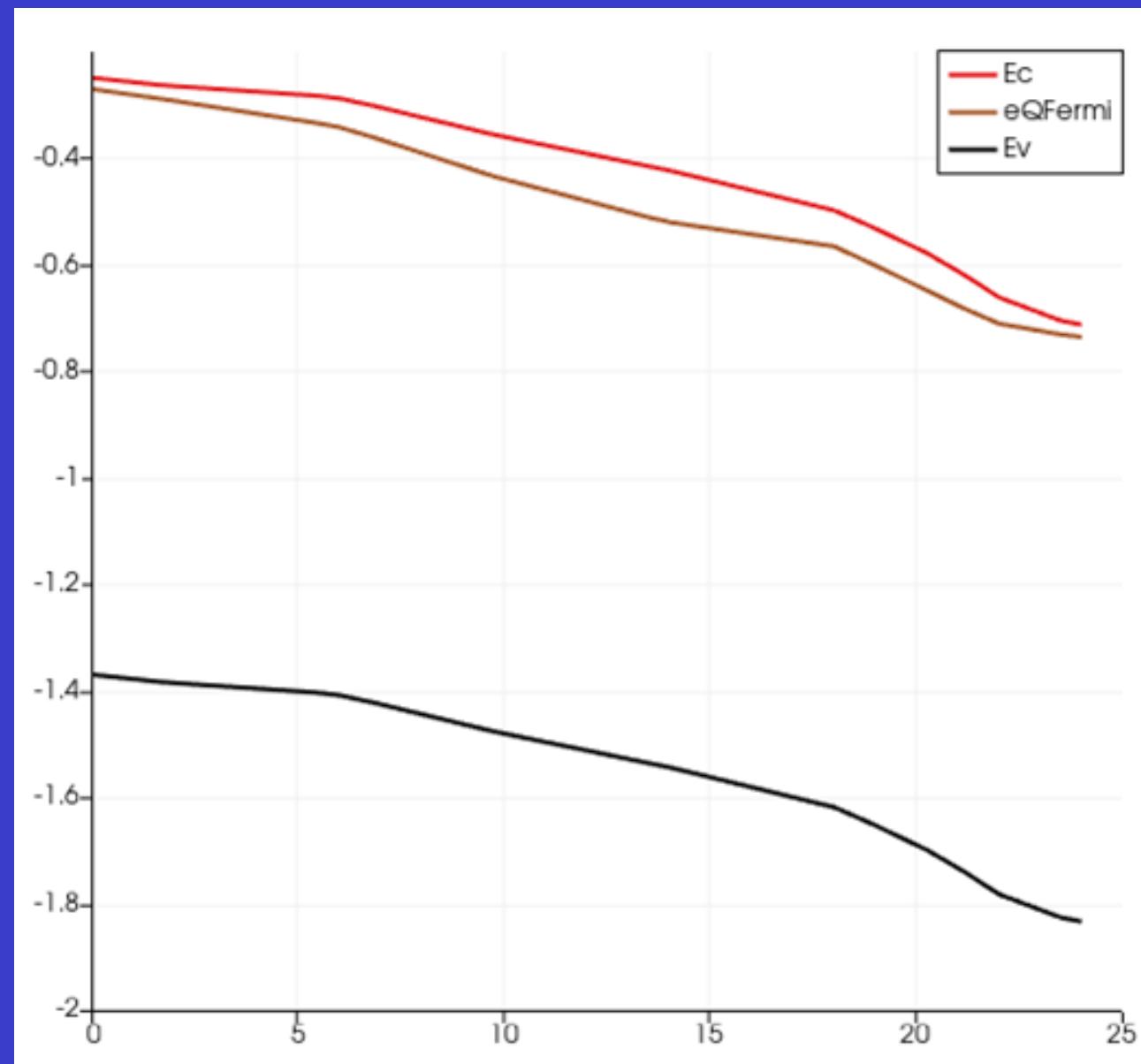


$V_{gs} < V_{th}$ OFF
 $V_{gs} = -0.6$
 $V_{ds} = 1$

1. Overlapping of Drain and Source SCL, so the bands sum up in the channel
2. Fermi further conduction (means that less e- are able to reach conduction)
3. Bending of conduction band show we are accumulating major type carrier in channel (Accumulation)

20nm

Along_and across the channel: ON

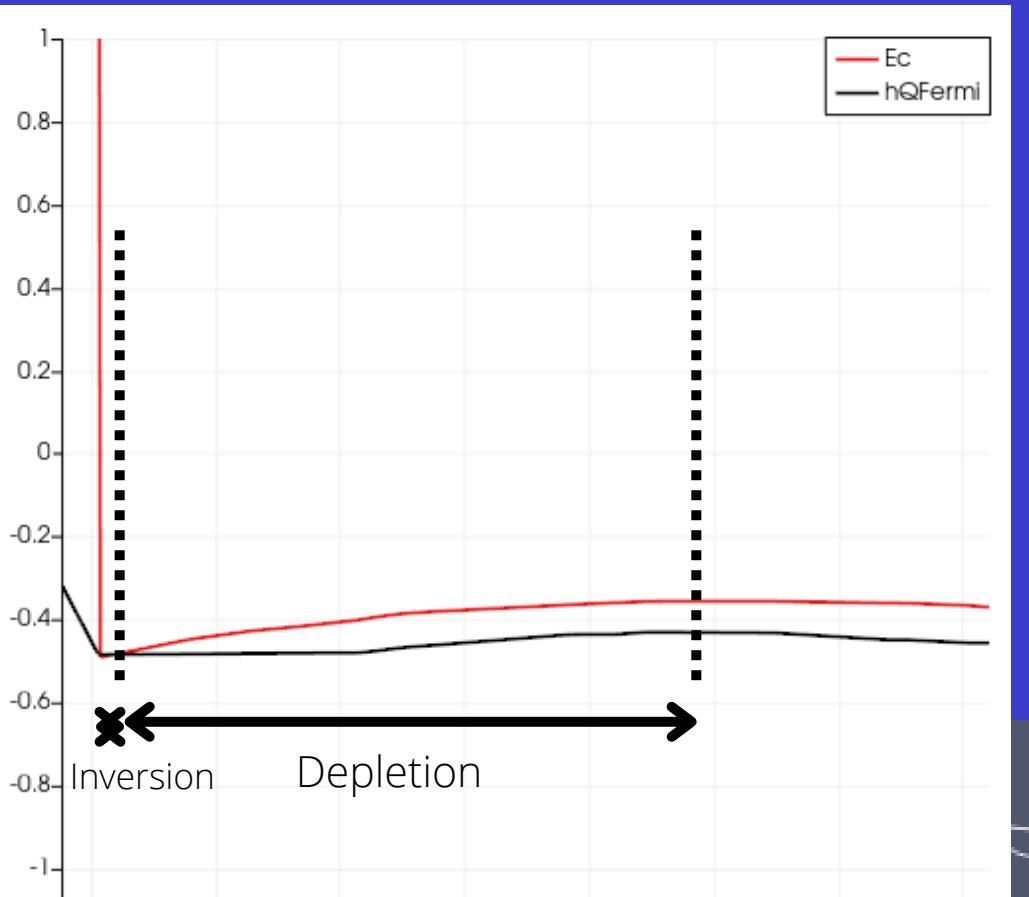
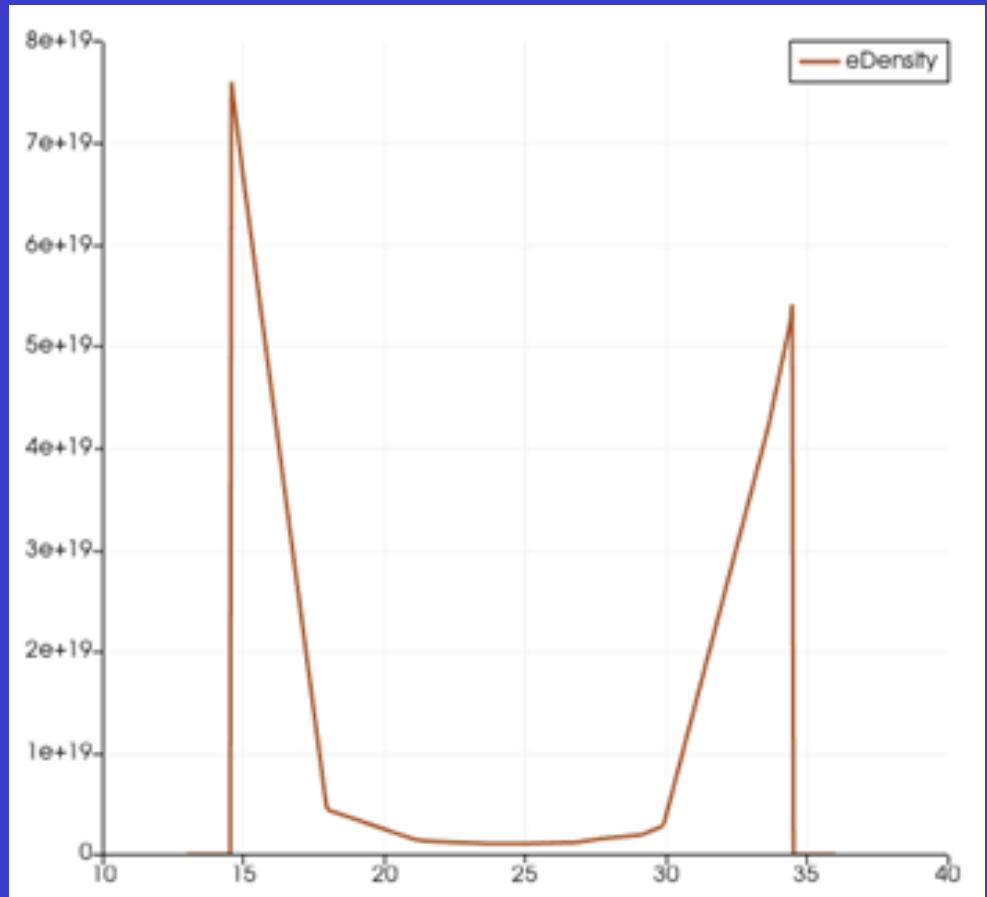


$V_{gs} > V_{th}$ ON
 $V_{gs} = 0.7$
 $V_{ds} = 1$

1. Overlapping of band in the channel
2. Fermi closer conduction

20nm

Across the channel: Fermi & e- density.

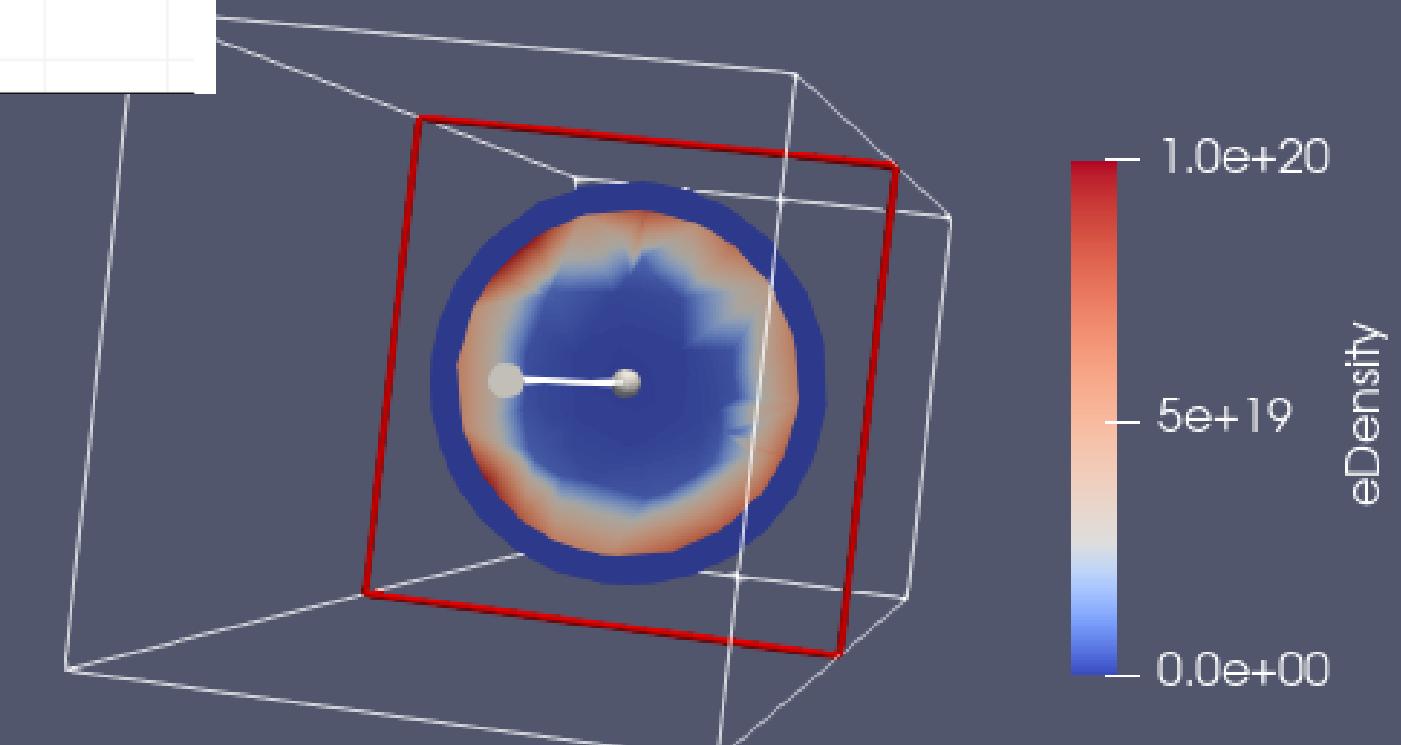


$V_{gs} > V_{th}$ ON

$V_{gs} = 0,7$

$V_{ds} = 1$

Comments on electron density
Location across the channel

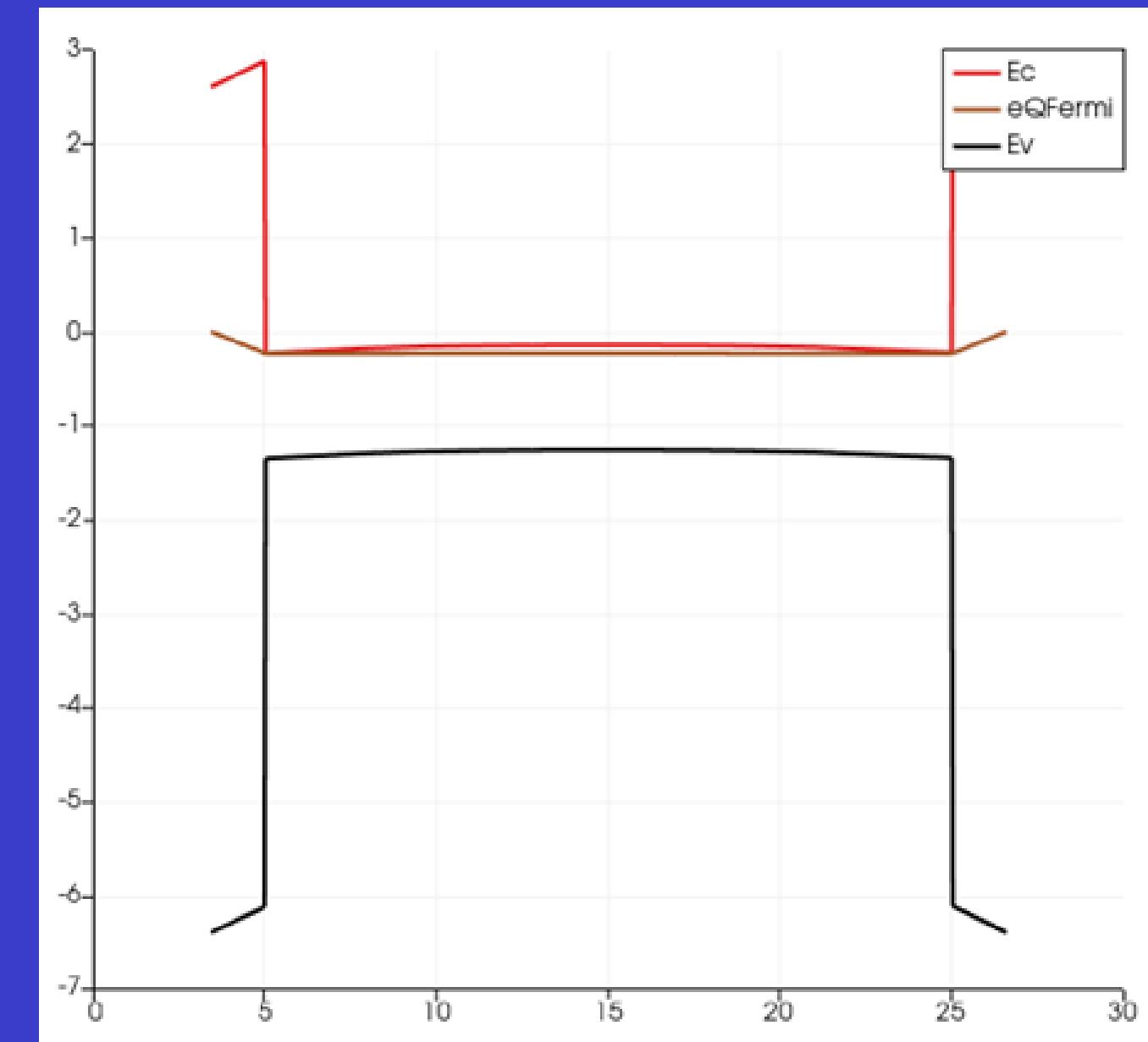
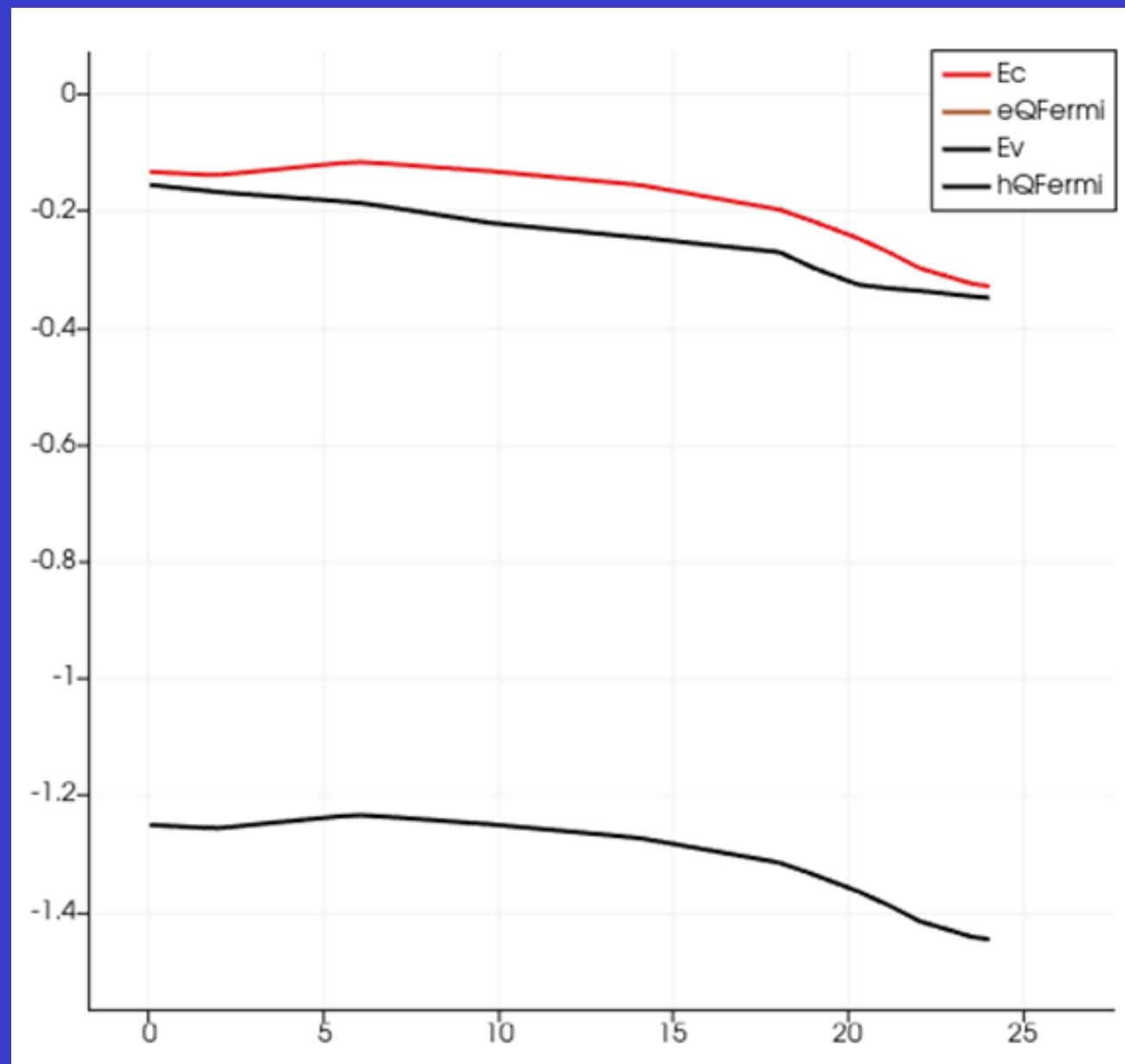


1.0e+20
5e+19
0.0e+00

eDensity

20nm

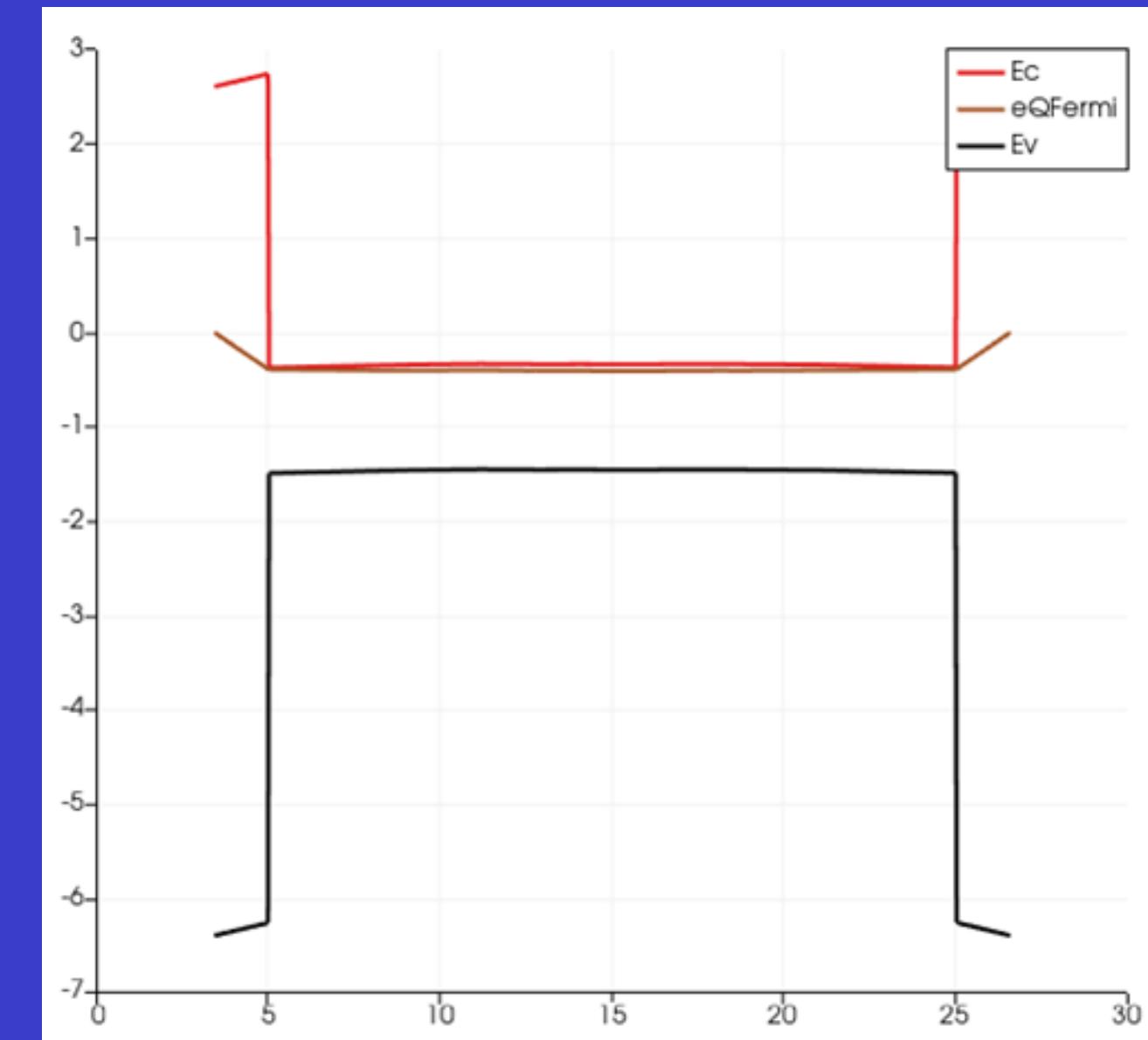
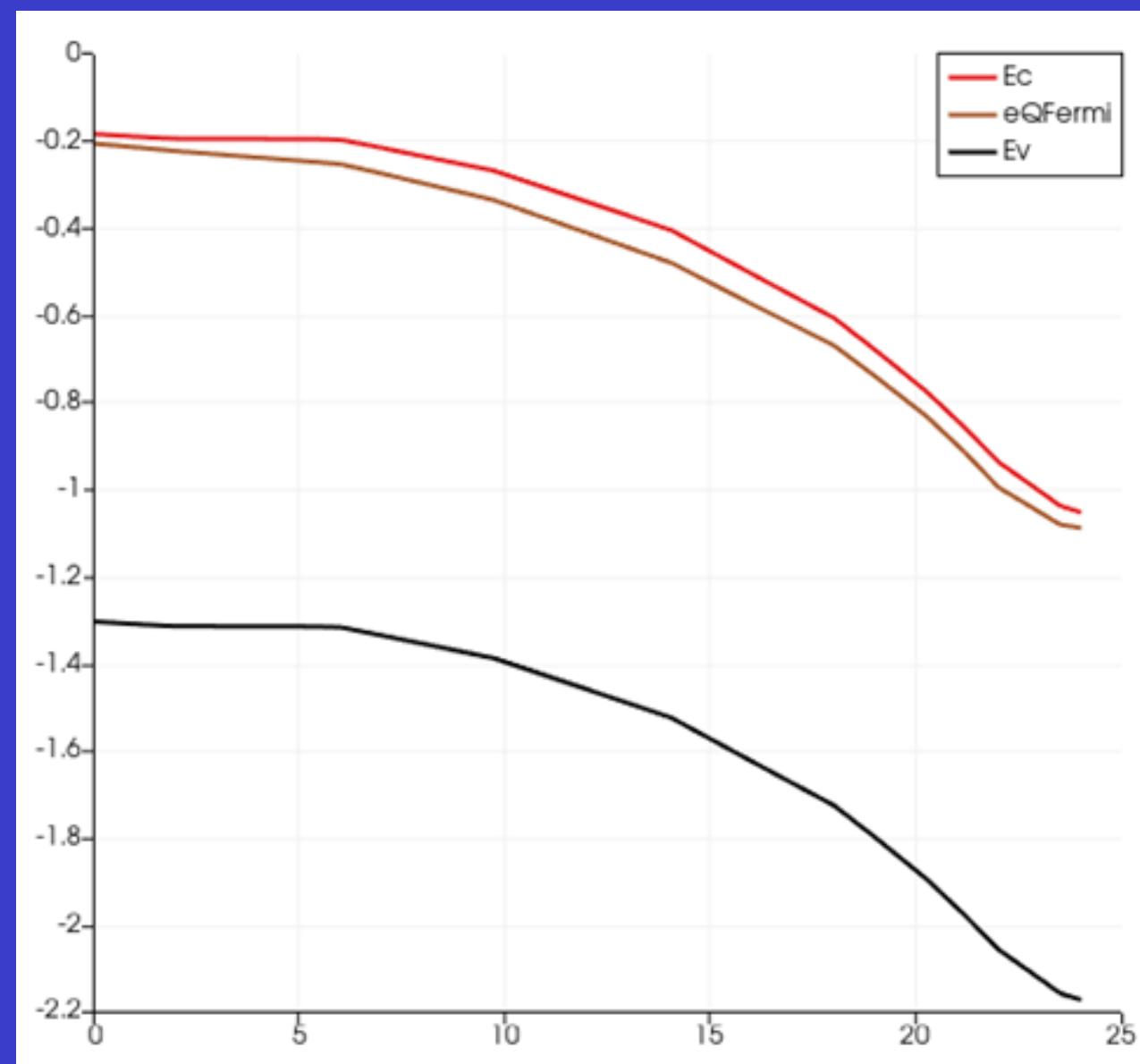
Along and across the channel: LIN



$V_{ds} < V_{gs} - V_{th}$ LIN
 $V_{gs} = 0,4$
 $V_{ds} = 0,5$

20nm

Along_and across the channel: SAT



$V_{ds} > V_{gs} - V_{th}$ SAT
 $V_{gs} = 0,4$
 $V_{ds} = 1,3$