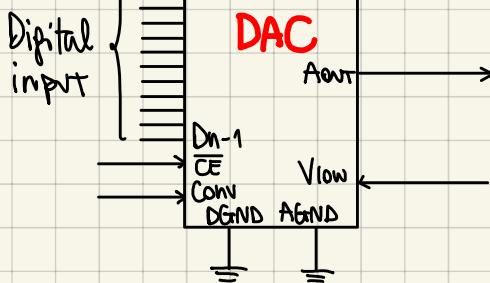


$$n = \# \text{ of bits}$$

$$2^n = \# \text{ of levels}$$



RESOLUTION

$$\text{LSB} = \frac{\text{FSR}}{2^n}$$

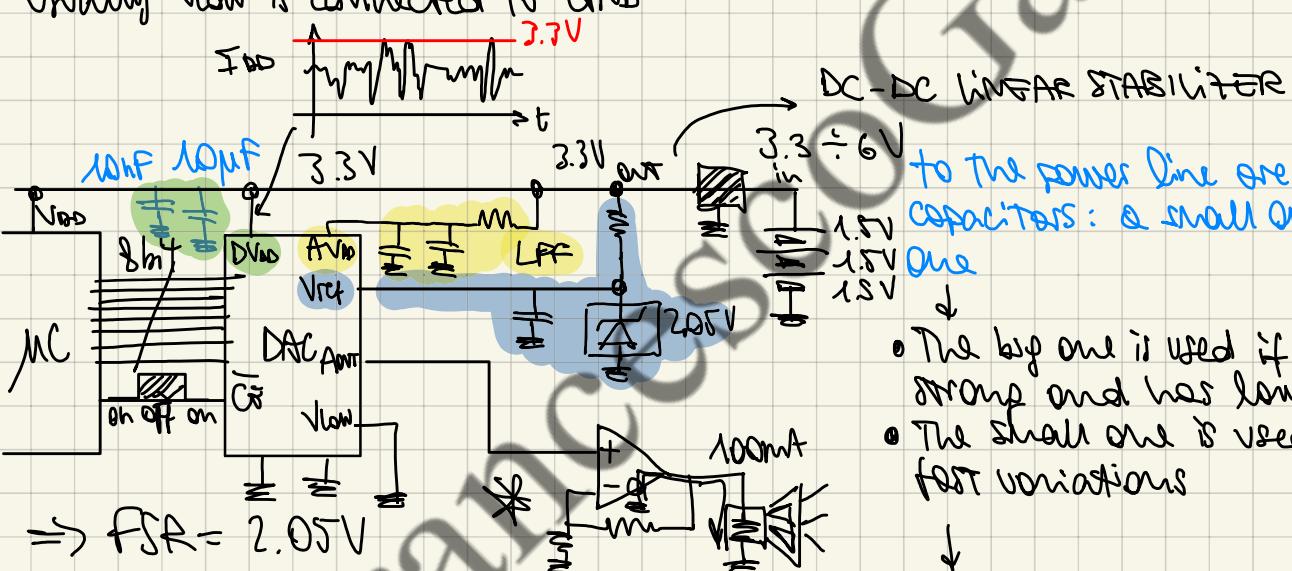
 $\overline{\text{CE}}$  = CHIP ENABLE (digital input)

$\overline{\text{CE}}$  is a logic input which allows us to completely turn on the full chip or keep it in the low power consumption mode.

$\overline{\text{CE}}$  → it means that the pin is active low so it is active when connected to a low value (GND).

when instead  $\overline{\text{CE}}$  is connected to Vdd the chip is in LPCM and Aout is zero or floating.

Usually Vref is connected to GND



to the power line are connected two capacitors: a small one and a big one

- The big one is used if the current is strong and has low variations
- The small one is used to kill the fast variations

They are used in order to keep the voltage on the power line almost constant

In case that batteries change and so the power supply has some fluctuations we use some filters:

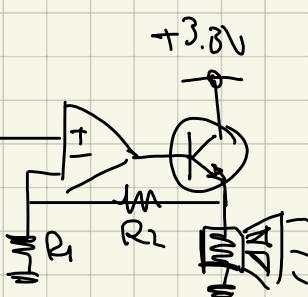
→ used to keep as constant as possible DVdd

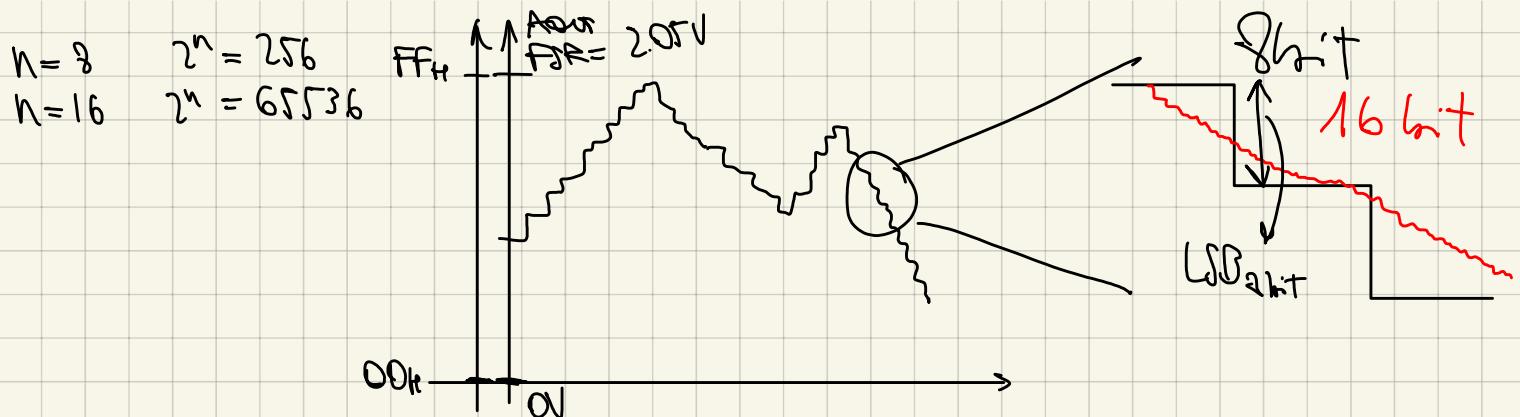
→ used to keep as constant as possible AVdd

→ The Vref network allows us to keep Vref independent from the PS

or \*

Aout





$$\Rightarrow LSB_{8\text{bit}} = 256 \text{ LSB}_{16\text{bit}}$$

$$\text{if } FSR = 5V \Rightarrow LSB_{8\text{bit}} = FSR/2^8 = 19.5 \text{ mV}$$

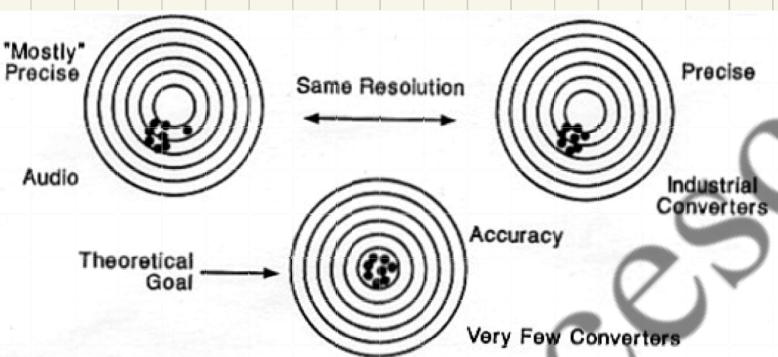
$$LSB_{16\text{bit}} = FSR/2^{16} = 76 \mu\text{V}$$

$$\left. \begin{array}{l} LSB_{16\text{bit}} = LSB_{8\text{bit}} / 256 \\ \end{array} \right\}$$

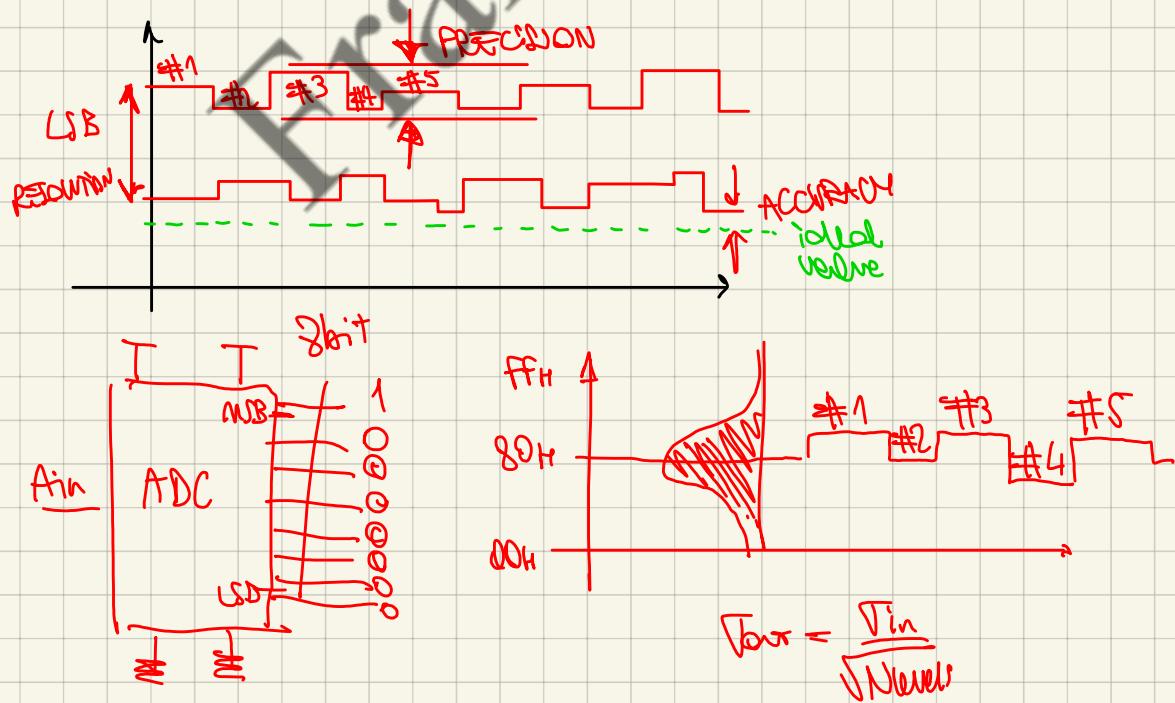
• **RESOLUTION** = # of levels the DAC is able to provide =  $2^n$

• **Precision** = is the spread of the output value, when the input is the same

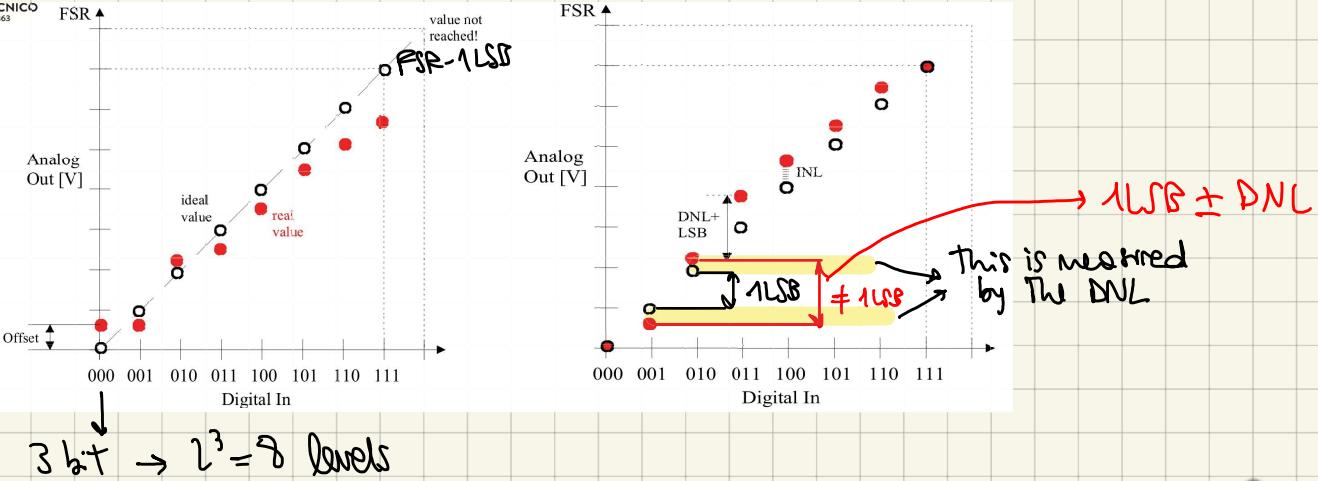
• **ACCURACY** = is the maximum error b/w Aout and the theoretical expected value



How can we improve precision? We can do many measurements and then average the results



# ERRORS AND NON-LINEARITIES



If the DAC is ideal  $000 \equiv 0V$  and  $111 = FSR$

## NOTICE:

since the 1st code (000) corresponds to the 0 level (0V), so the 8th code must correspond to the 7th value ( $FSR - 1LSB$ )

↓  
The ideal flow should lie on the 45° line

when we apply 000 in input the output is not 0V → OFFSET ERROR

when we apply 111 in input the output is not  $FSR - 1LSB$  → GAIN ERROR

Some DACs force the 000 code to be 0V and so to compensate the OFFSET error and also force the 111 to be ( $FSR - 1LSB$ ) so to compensate the GAIN error

**INL = INTEGRAL NON-LINEARITY = REAL - IDEAL DISTANCE**

↳ it's the distance b/w the measured Aout and the ideal

from one code to the next one : horizontally we increase of 1 bit and vertically we should increase of 1 LSB

↓  
This is true for ideal values, but not for real actual values

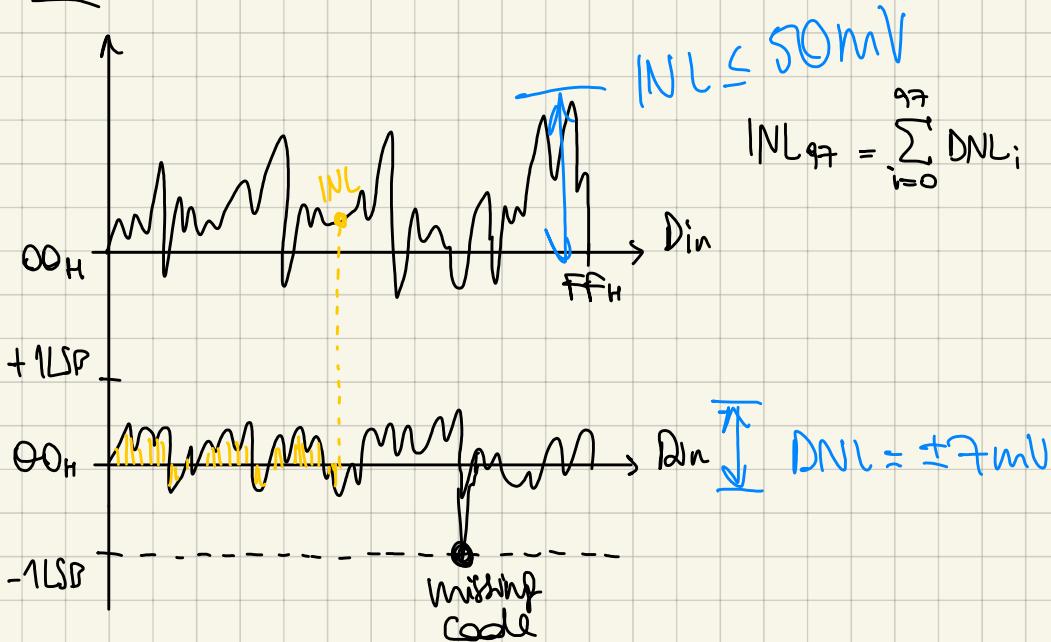
**DNL = DIFFERENTIAL NON-LINEARITY = REAL - IDEAL STEP HEIGHT**

↳ it is "how much the step from two consecutive real values differ from 1LSB"

Example: if  $DNL = -1LSB$  → means that the DAC has a missing code in that specific position

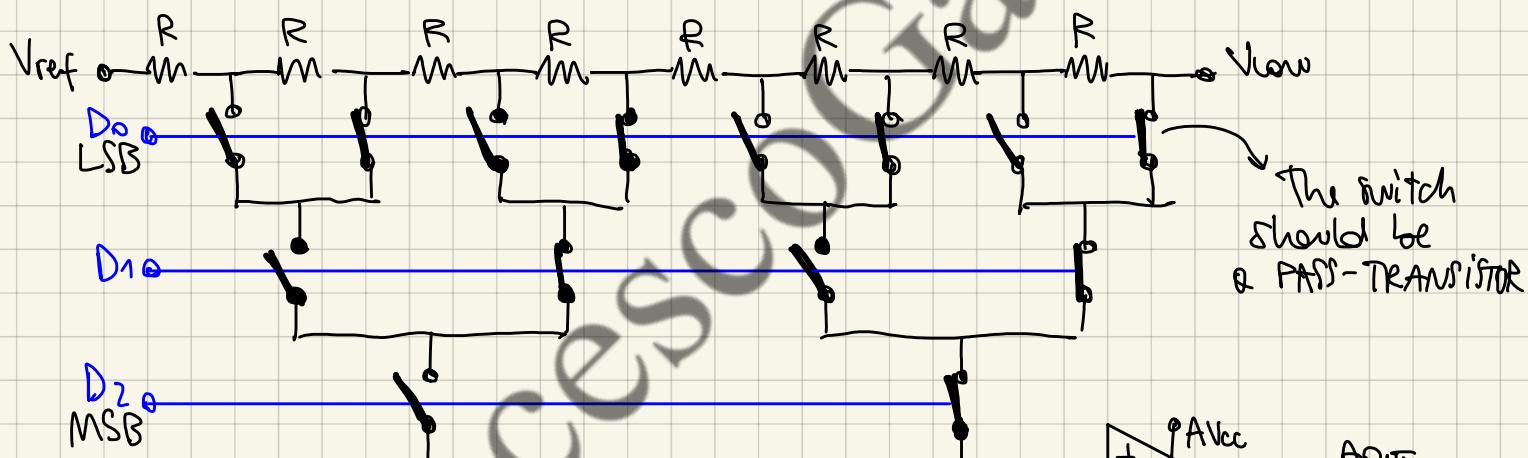
NOTICE: each code has its specific INL and DNL

Notice:

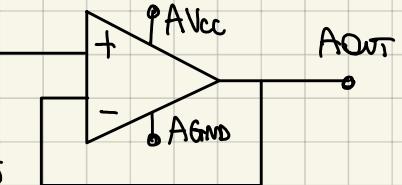


A good designed DAC should have:  $-1LSB \leq DNL \leq +1LSB$

### VOLTAGE-SCALING DAC



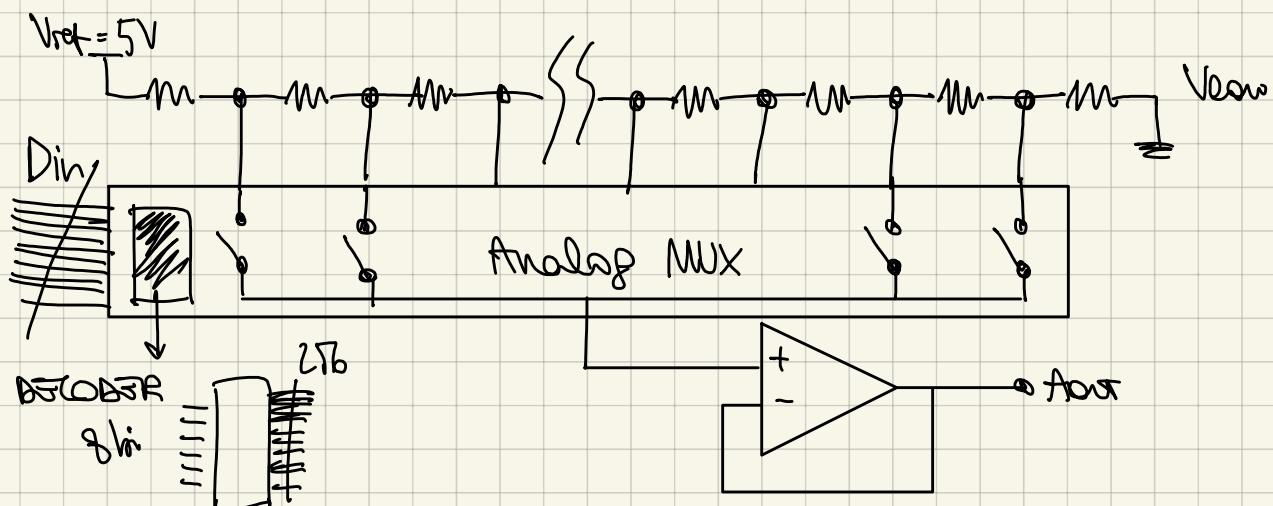
Components:  $\left\{ \begin{array}{l} n = \text{bit} \Rightarrow 2^n = \text{levels} \rightarrow 2^n \text{ resistors} \\ 2^n \text{ PASS-TRANSISTORS} \rightarrow 2 \cdot 2^n \text{ MOSFETS} \\ 1 \text{ OpAmp} \end{array} \right.$



ADVANTAGE: easy scalability of resistors (all identical)

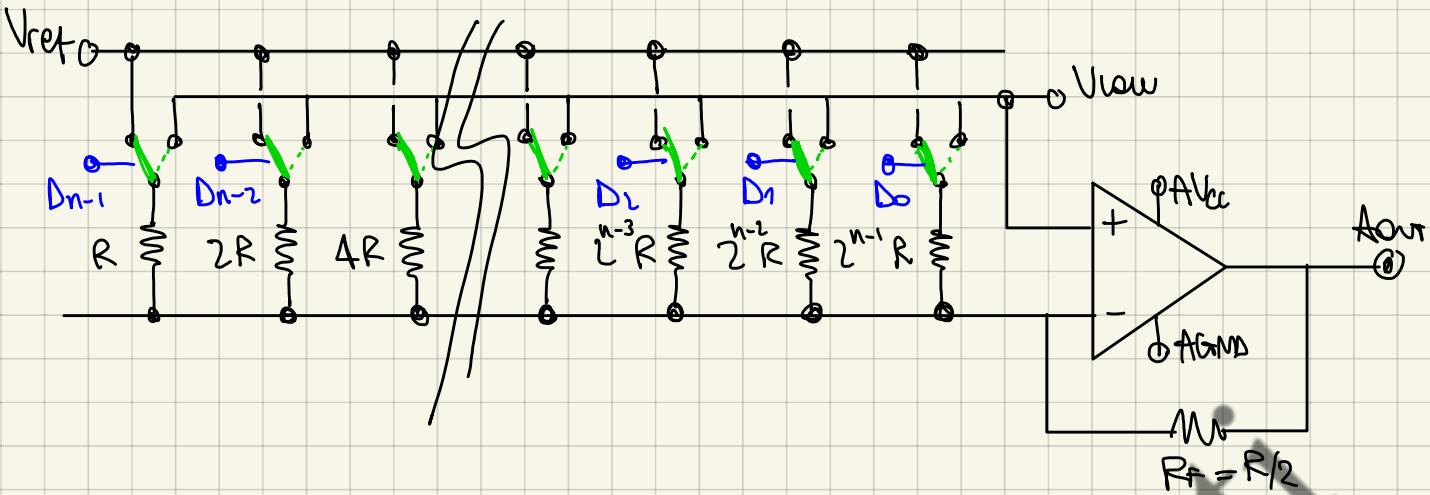
PROBLEM: OpAmp bias current causes non-linearity

$\left\{ \begin{array}{l} 2^n \text{ pMOS} \\ 2^n \text{ nMOS} \end{array} \right.$



## WEIGHTED-R DAC

↳ we let each bit to drive the corresponding resistor



The less significant is the bit, the higher the resistance connected to it

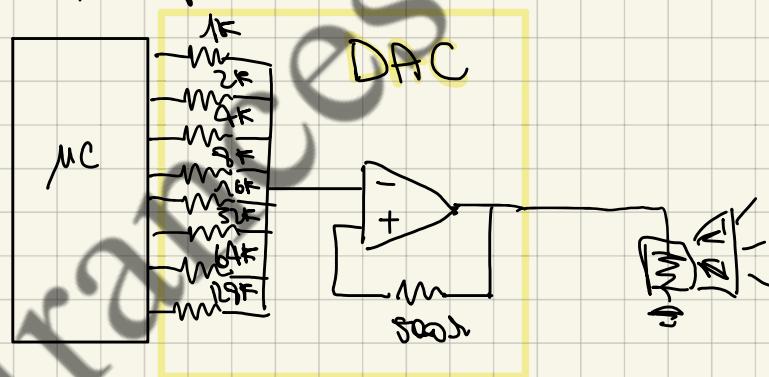
$$V_{out} = V_{ref} \frac{R_f}{R} \left\{ \frac{D_{n-1}}{1} + \frac{D_{n-2}}{2} + \dots + \frac{D_0}{2^{n-1}} \right\} = V_{ref} \left\{ \frac{D_{n-1}}{2} + \frac{D_{n-2}}{2^2} + \dots + \frac{D_0}{2^n} \right\}$$

Components:

$n$ resistors	$n$ P-MOSFETS
$n$ PASS-TRANSISTORS $\rightarrow 2 \cdot n$ MOSFETS	$n$ n-MOSFETS
1 OpAmp	

ADVANTAGES:

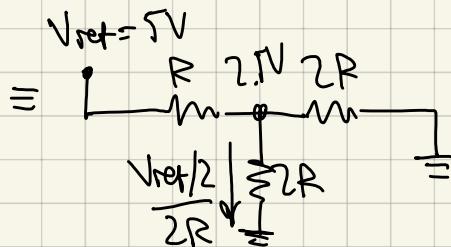
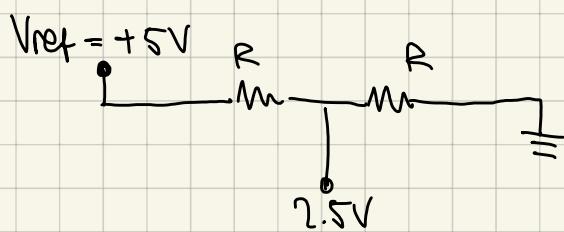
1. If we manufacture the DAC w/ discrete components, in case of a 8 bit DAC, w/ this configuration we use 8 resistors, while w/ the former one we used  $2^8 = 256$  resistors



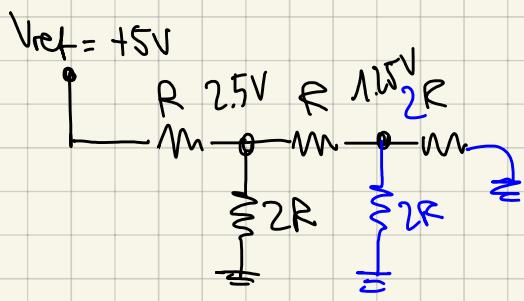
2. We use even less transistors

$\Rightarrow$  we are saving volume!!

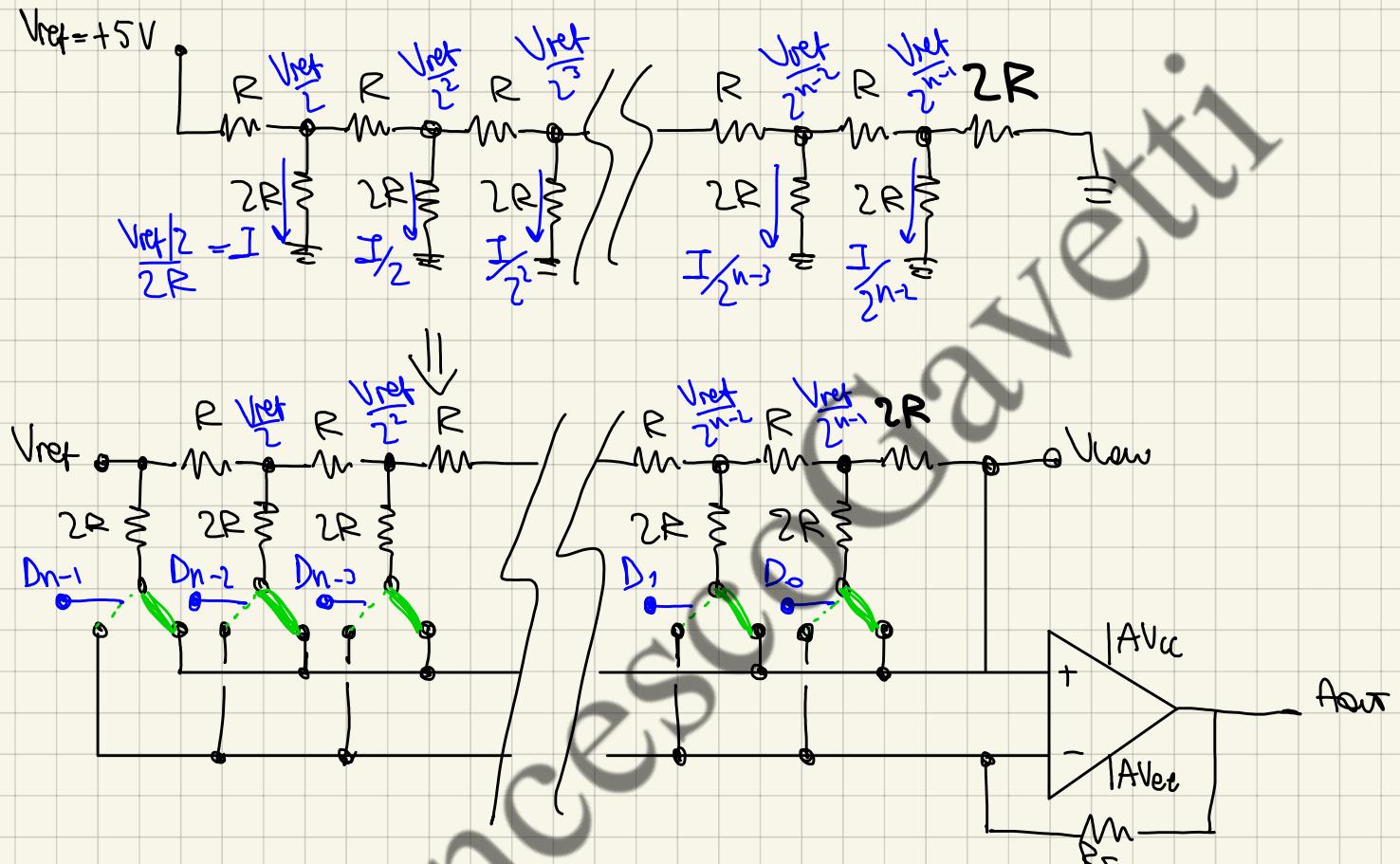
## CURRENT-SCALING DAC



let's iterate the process:



We can choose whatever # we wish of resistors:

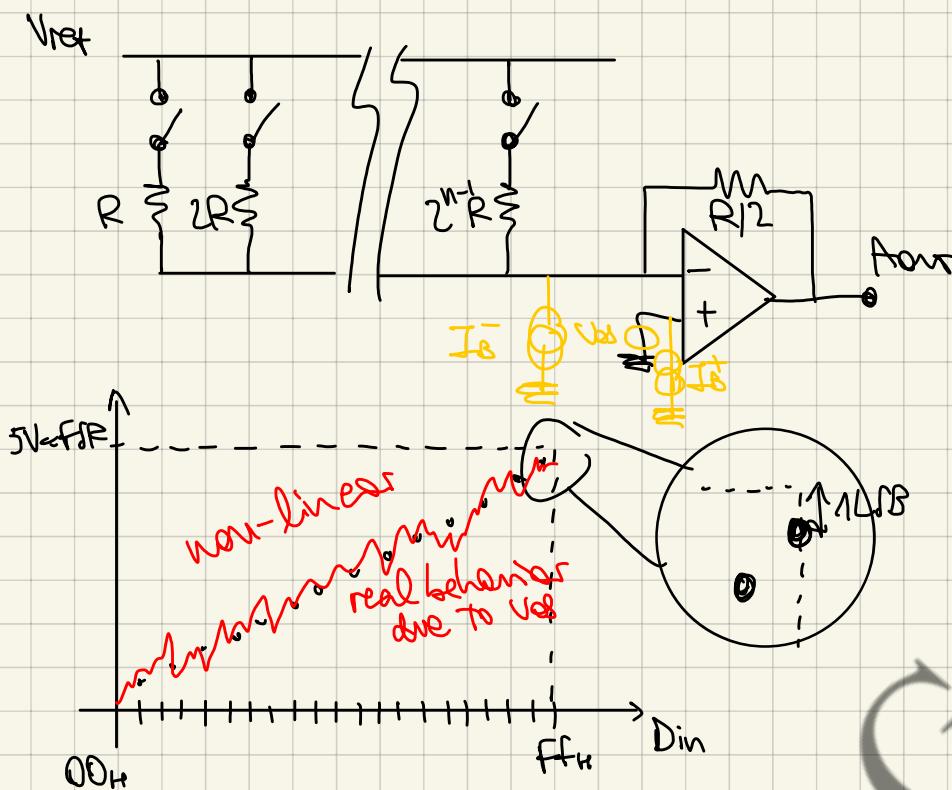


Components:  $\left\{ \begin{array}{l} 2n \text{ resistors} (\text{n } 2R \text{ resistors and } \text{n } R \text{ resistors}) \\ \text{n PNP-TRANSISTORS} \rightarrow \text{2n MOSFETS} \rightarrow \left\{ \begin{array}{l} \text{n nMOS} \\ \text{n pMOS} \end{array} \right. \\ \text{1 OpAmp} \end{array} \right.$

↓  
smallest area occupation

let's go back to the WEIGHTED-R DAC  
we told that we needed 2 switches in order to connect both to Vref and to Vout

Why do we need to connect to Vout?



$I_S^\pm$  has no effects

$$A_{out}(V_{os}) = V_{os} \left( 1 + \frac{R/2}{?} = \frac{R}{2} \right)$$

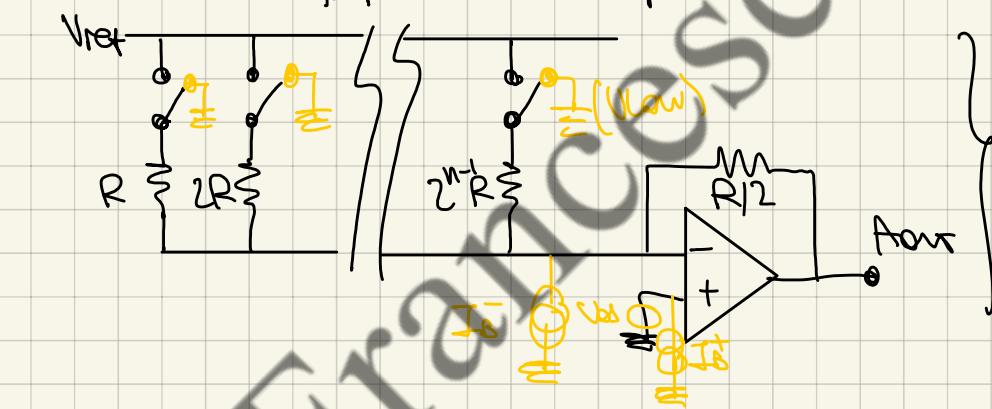
$$G_{min} = 1$$

$$G_{max} = 2$$

The parallel  
of the resistors  
whose switch  
is closed

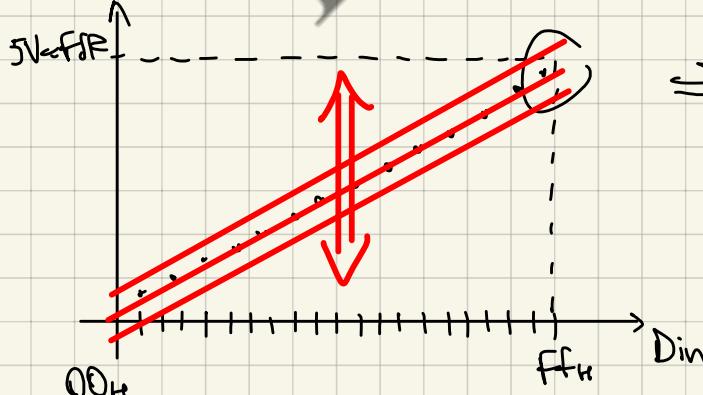
$$V_{os} \leq E(V_{os}) \leq 2V_{os}$$

for this reason it's much better to add a deviator but in this way the resistor is always present so the gain will be  $G=2$  which is constant



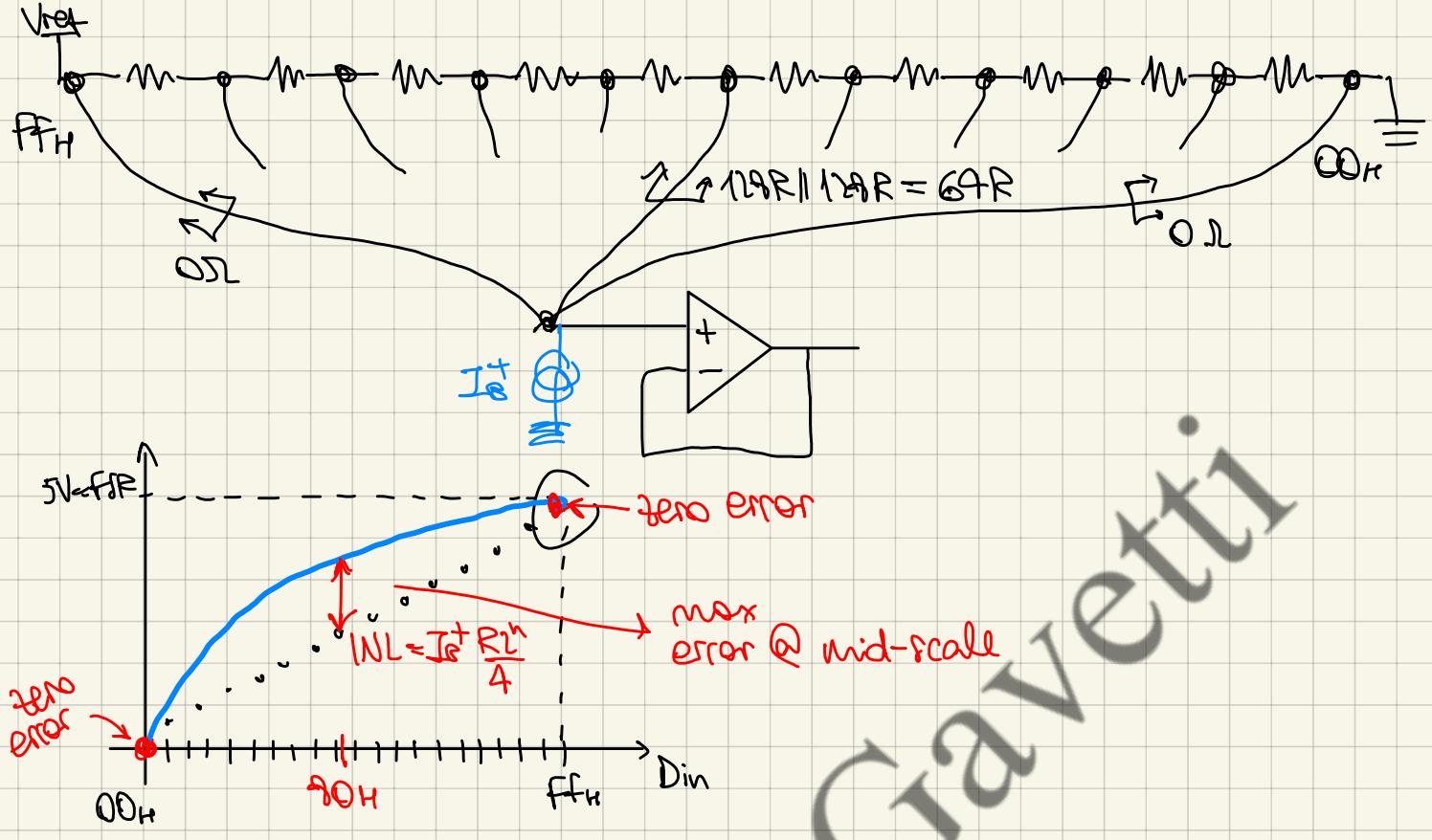
In this way we have an higher but CONSTANT error

$$A_{out}(I_S^\pm) = I_S^\pm R/2$$



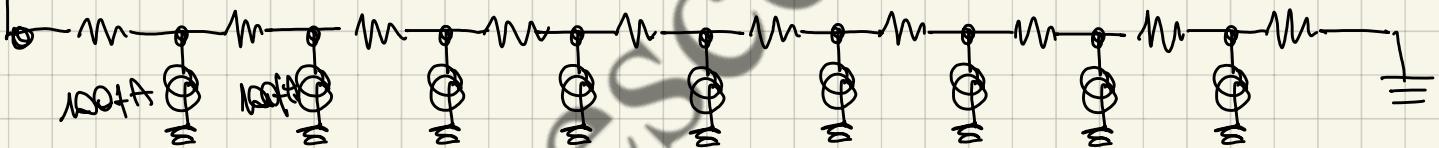
⇒ LINEAR!!! (thanks to the deviator)

If we consider the voltage-scaling DAC, the situation is even more dramatic:

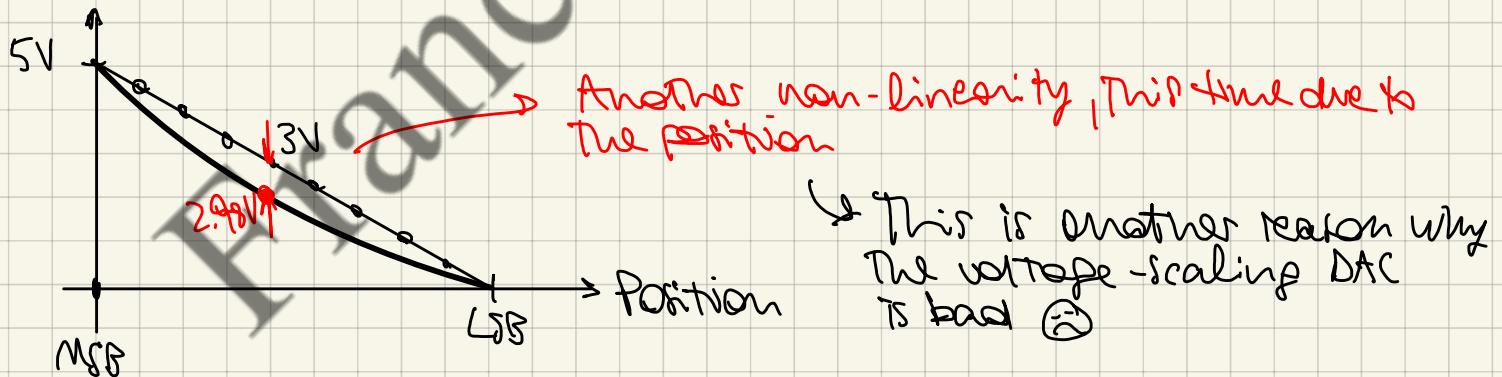


furthermore each PT can have a leakage current

Vier-fse



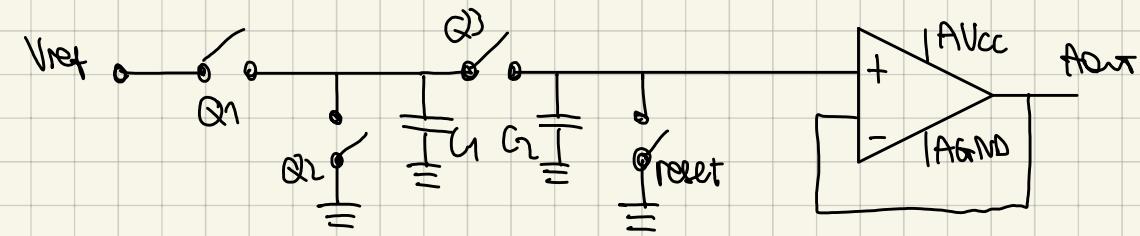
If the leakage currents are constant:



Instead in The weighted-F DAC The leakage has no effect

In The current-scaling DAC The leakage pumps into The V.O., but The output error is constant and doesn't depend on The digital input code.

## SERIAL INPUT DAC



① At the beginning  $Q_2, Q_3$  and reset switches are closed

Then we open the reset switch and we leave it opened permanently.

Then we open  $Q_3$

Now depending on the input bit we close  $Q_1$  or  $Q_2$

After the closure of one of the two switches, the "share" switch  $Q_3$  is opened and closed for a short period before applying the same procedure on the next bit

- if the input bit is 1  $\rightarrow Q_1$  is closed so we charge  $C_1$  @  $V_{ref}$ . Then when we close  $Q_3$  we perform charge sharing to  $C_2$  reaching  $V_{ref}/2$  on both the capacitors
- if the input bit is 0  $\rightarrow Q_2$  is closed so we store 0V on  $C_1$ . Then  $Q_3$  closes, we perform charge sharing

So if we apply  $\underbrace{10000000}_{n \text{ terms}} \rightarrow$  eventually at the output we'll have  $\frac{5V}{n}$

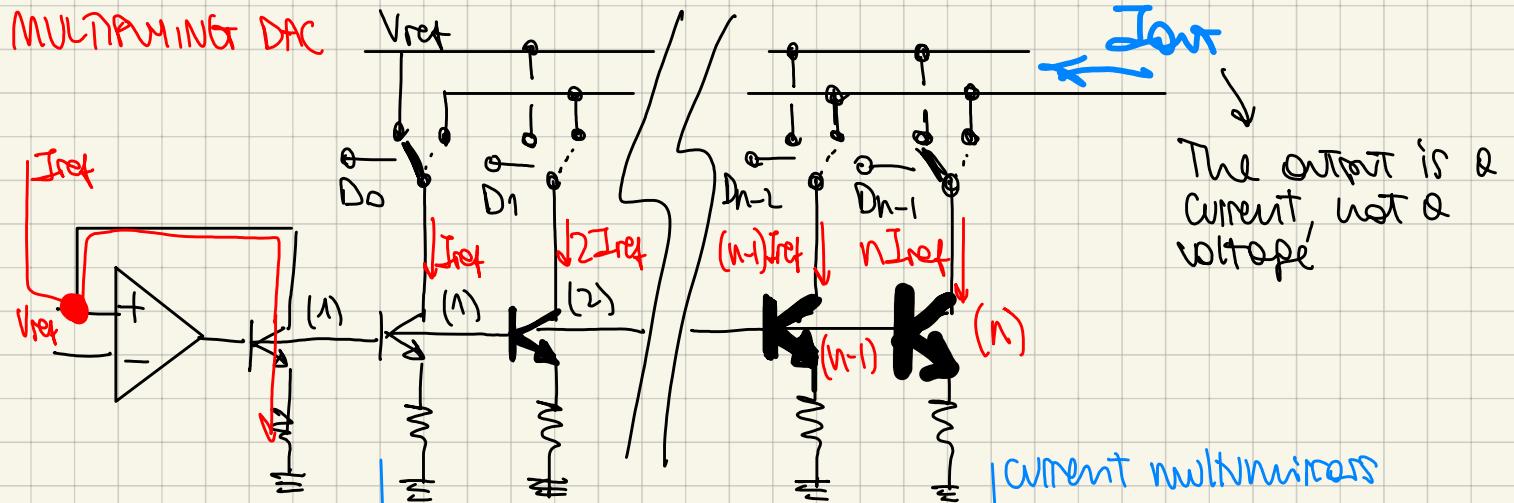
but everytime we have 0 at input we force the voltage value stored on  $C_1$  to be halved

if we apply  $00000001 \rightarrow$  at the output we'll have  $5V/2 = 2.5V$

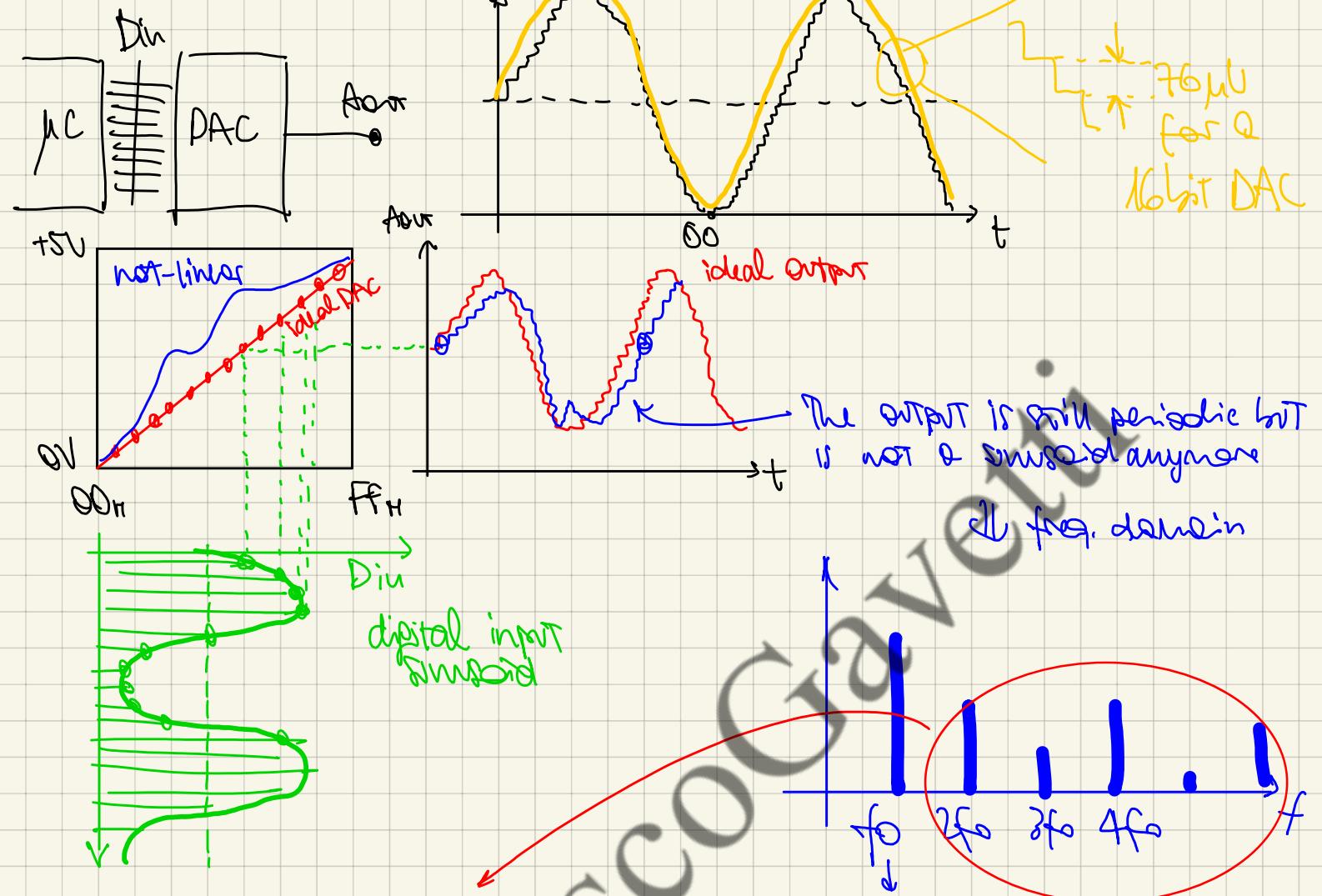
$\Rightarrow$  The last applied bit is the MSB

Components  
 { 2 capacitors  
 { 4 MOSFETs  
 { 1 OpAmp (buffer)

## MULTIPLEXING DAC



We have seen that a DAC can reconstruct the waveform but reconstructs it as a staircase



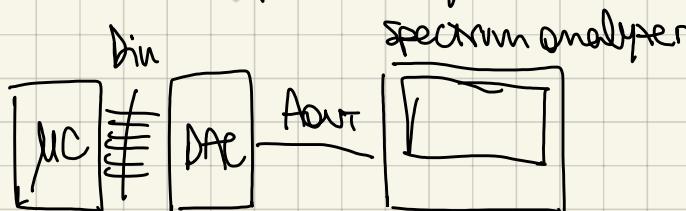
These harmonics comes from the NON-LINEARITY of the DAC

NOT from other disturbances (i.e. noise in power supply)

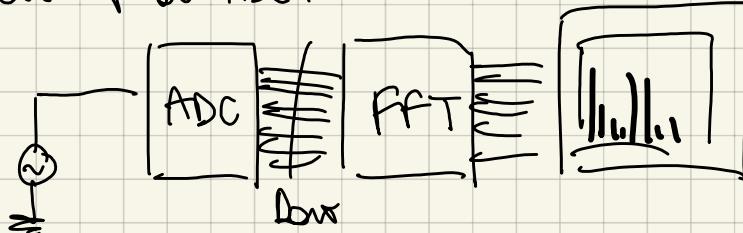
These harmonics depend on the input freq.

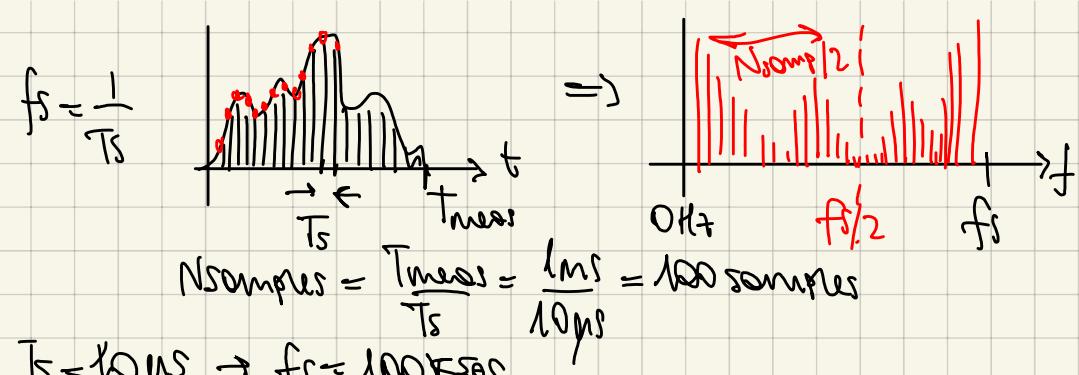
To understand if our DAC is good or not it's better to perform the FFT and move to the freq domain

if a lot of harmonics pop up it means that the DAC is not that good in terms of linearity



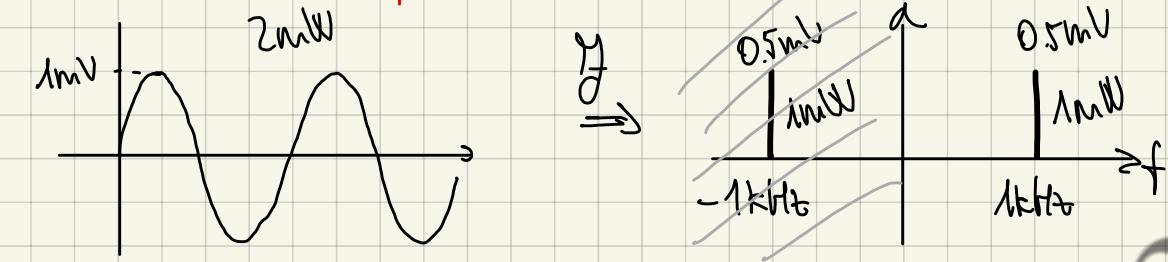
In case of an ADC:



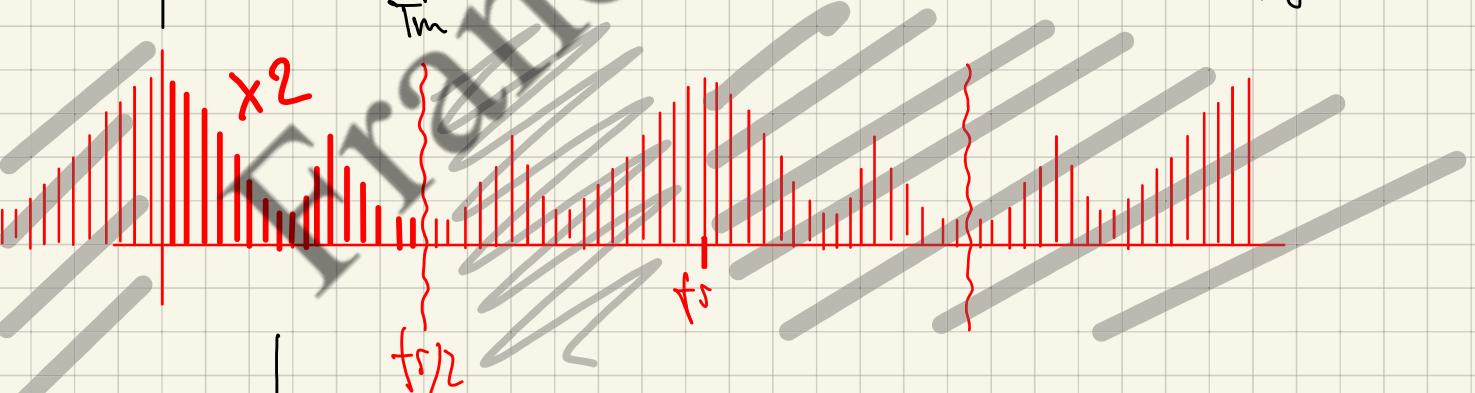
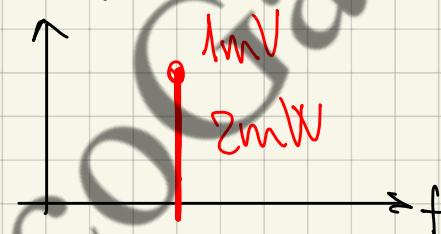


$$T_s < 10 \mu\text{s} \rightarrow f_s = 100 \text{ KHz}$$

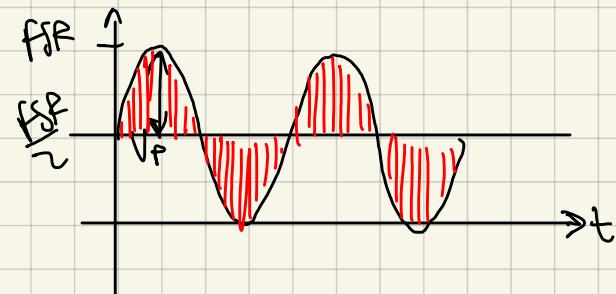
real values  $\rightarrow$  symmetric spectrum around  $f_s/2$



We can consider just one side of the spectrum, but in this case:



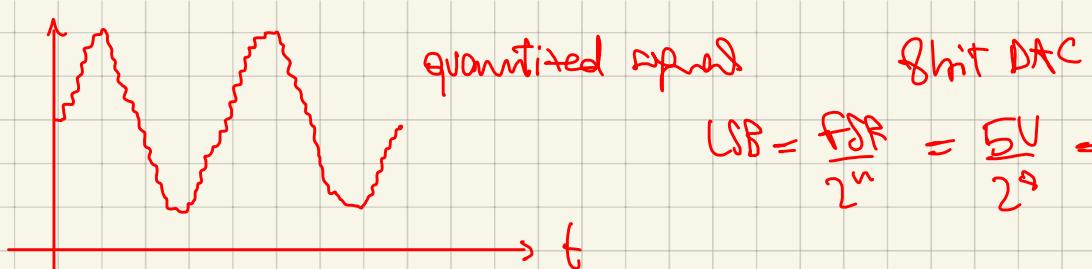
Just plot spectrum b/w 0 and  $f_s/2 \Rightarrow$  BUT remember to multiply by 2



$$V_{pp} = 2V_p \leq f_s R \Rightarrow V_p \leq \frac{f_s R}{2}$$

$$\text{Signal power} = \frac{V_p^2}{2}$$

$$\text{Signal rms} = \frac{V_p}{\sqrt{2}}$$



$$LSB = \frac{f_{SR}}{2^n} = \frac{5V}{2^8} = 19mV$$

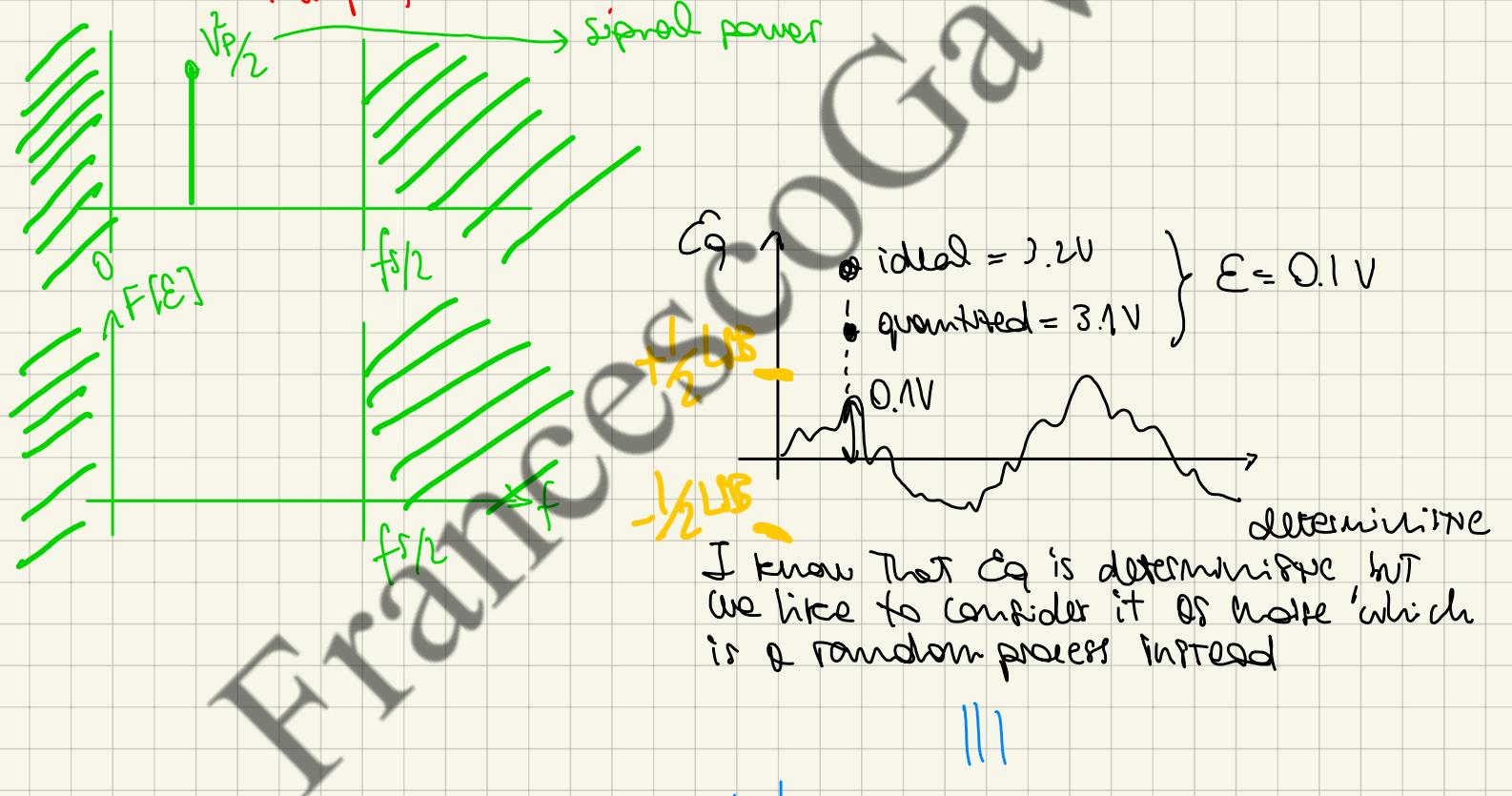
$\epsilon$  = quantization error



real signal = ideal signal + quantization error

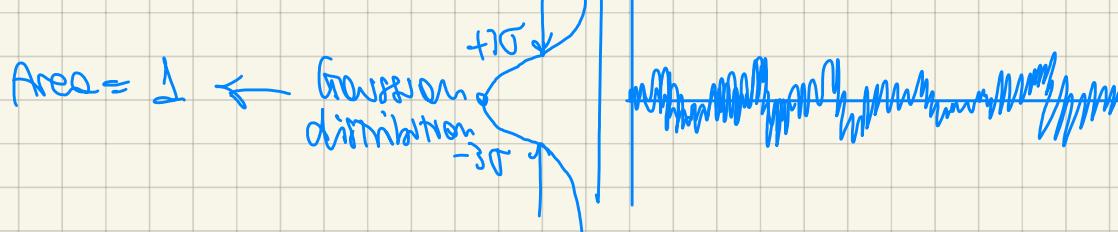
quantized signal

What about the freq. domain?



I know that  $C_q$  is deterministic but we like to consider it as noise 'which is a random process instead'

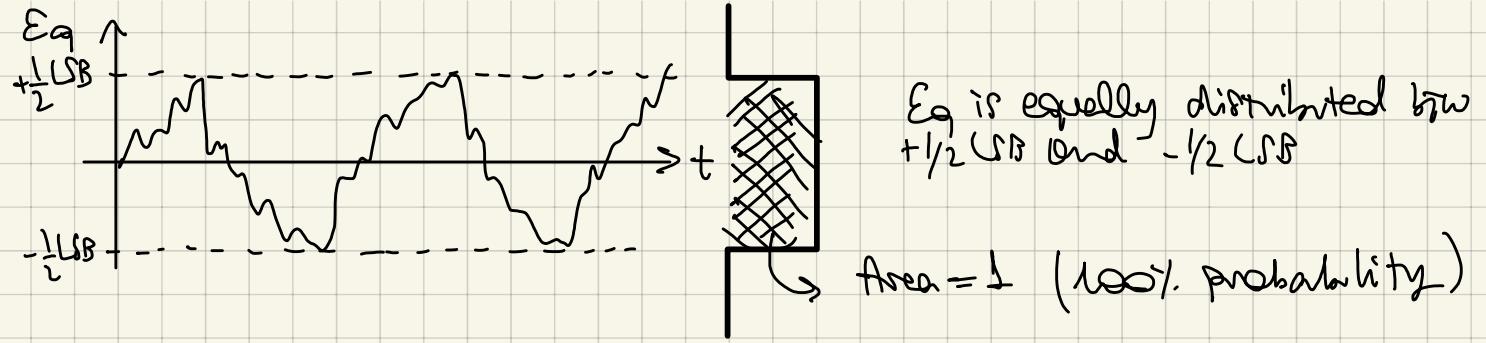
|||



so we can consider:  $1 LSB \equiv 6 \sigma_n$

⇒ so we can say that our  $\epsilon_q$  is identical to a white noise where  $\sigma_n$  is

$$\sigma_n = \frac{1}{6} LSB$$



So instead equating the peak-to-peak value of the error to the peak-to-peak value of white noise, it's better to compare the power

Noise power:  $\sigma_n^2$

$$\begin{aligned} \text{Eq power: } P(E) &= \frac{1}{T_m} \int_0^{T_m} E_q^2(t) dt \\ &= \frac{1}{\text{LSB}} \int_{-\frac{1}{2} \text{ LSB}}^{+\frac{1}{2} \text{ LSB}} P(E) \cdot E^2 dE \end{aligned} \quad \left. \right\}$$

$$\sigma_q^2 = \frac{\text{LSB}^2}{12} \Rightarrow \sigma_q = \frac{\text{LSB}}{\sqrt{12}}$$

$$\sigma_q = \frac{\text{LSB}}{\sqrt{12}}$$

CONCLUSION: we can approximate the real quantized signal + The ideal signal w/ noise w/  $\sigma_n = \frac{\text{LSB}}{\sqrt{12}}$



$$SNR = \begin{cases} \frac{S_{\text{power}}}{N_{\text{power}}} \\ \frac{S_{\text{amplitude}}}{N_{\text{amplitude}}} \end{cases}$$

$$\Rightarrow SNR = 6 \frac{V_p^2}{LSB^2}$$

$$\begin{aligned} S_{\text{power}} &= V_p^2 / 2 \\ N_{\text{power}} &= LSB^2 / 12 \end{aligned}$$

MAX SNR ACHIEVABLE w/ AN ADC/DAC

$$SNR_{\text{ideal}} = \frac{S_{\max}}{N_{\min}} = \frac{(FSR/2)^2 / 2}{LSB^2 / 12} = \frac{FSR^2}{8} \frac{12}{LSB^2} = \frac{12}{8} FSR^2 \cdot \frac{2^{2n}}{FSR^2} = \frac{12}{8} \cdot 2^{n-1}$$

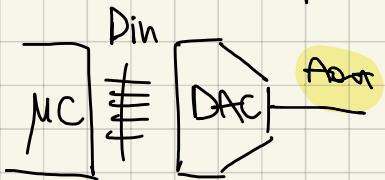
$\hookrightarrow LSB = FSR / 2^n$

$$\Rightarrow SNR_{\text{ideal}} [\text{dB}] = 10 \log \left[ \frac{12}{8} 2^n \right] = 6.02 n + 1.76$$

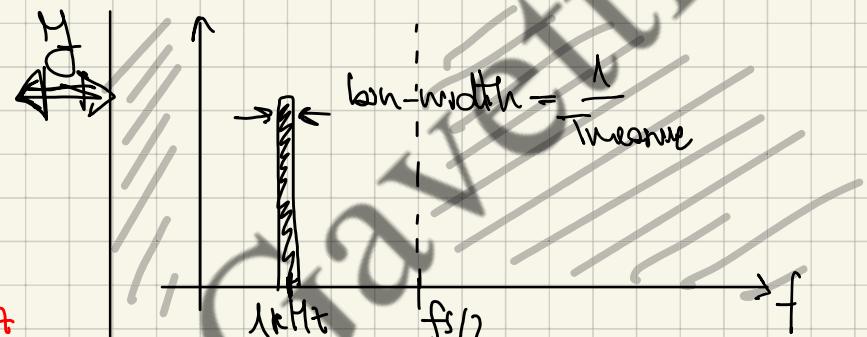
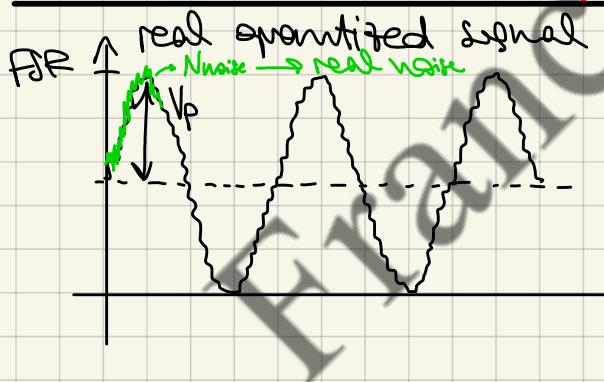
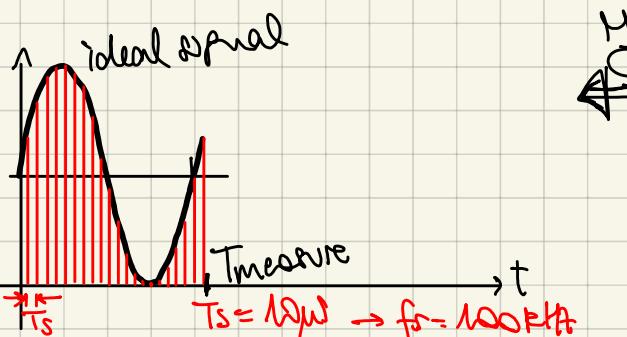
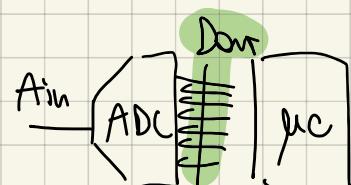
## SPECTRAL PERFORMANCES

NOISE "DUE TO" QUANTIZATION ERROR  $\sigma_q^2 = \frac{LSB^2}{12}$

Beware: Eq doesn't generate noise but it can be approximated to a noise whose power is  $\sigma_q^2$



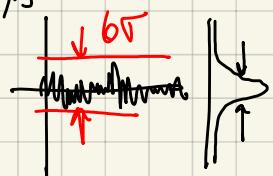
or



$$\begin{aligned} \text{band-width} &= \frac{1}{\text{Time measure}} = \frac{f_s}{\text{Nsamples}} = \frac{f_s/2}{\text{Nsamples}/2} \\ &= \frac{100\text{kHz}}{100 \text{ samples}} = 1\text{kHz} \end{aligned}$$

$$\text{Nsamples} = \frac{\text{Time measure}}{T_s} = \frac{1\text{ms}}{10\mu s} = 100 \text{ samples}$$

$$\text{power } \sigma_q^2 = \frac{LSB^2}{12}$$



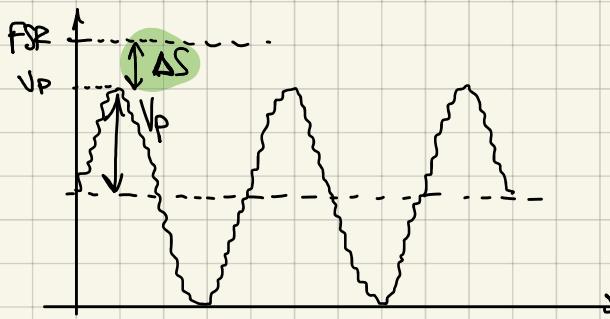
$$\begin{aligned} V_{p,\text{max}} &= \frac{\text{FSR}}{2} \\ \Rightarrow \text{S power} &= \frac{V_p^2}{2} \quad (\text{sinusoid}) \end{aligned}$$

$$S_{\text{rms}} = \frac{V_p}{\sqrt{2}}$$

let's neglect it for the moment

$$N_{\text{power}} = N_{\text{noise}} + N_{\text{quantization error}} = \frac{LSB^2}{12}$$

$$\Rightarrow \text{SNR}_{\text{ideal}} = \text{SNR}_{\text{max}} = \frac{S_{\text{max}}}{N_{\text{min}}} = \frac{(FSR/2)^2 \cdot 1/2}{LSB^2 \cdot 1/12} = 10 \log_{10} \left( \frac{12}{8} 2^h \right) = 6.02h + 1.76$$



$$\text{SNR}_{\text{Theoretical}} = \frac{S_{\text{real}}}{N_{\text{min}}} = \frac{(V_p/2)^2 \cdot \frac{1}{2}}{\text{LSB}^2 \cdot \frac{1}{2}} = \text{SNR}_{\text{ideal}, \text{dB}} - \Delta S_{\text{dB}}$$

THEORETICAL SNR

$$\Rightarrow \Delta S = \frac{V_{\text{PP}}}{\text{FSR}} = \frac{V_p}{\text{FSR}/2} = \frac{2V_p}{\text{FSR}}$$

$$\Delta S_{\text{dB}} = 20 \log_{10} \left( \frac{V_p}{\text{FSR}/2} \right) = 10 \log_{10} \left( \frac{V_p^2/2}{(\text{FSR}/2)^2/2} \right)$$

ratio b/w  
intensities

ratio  
b/w powers

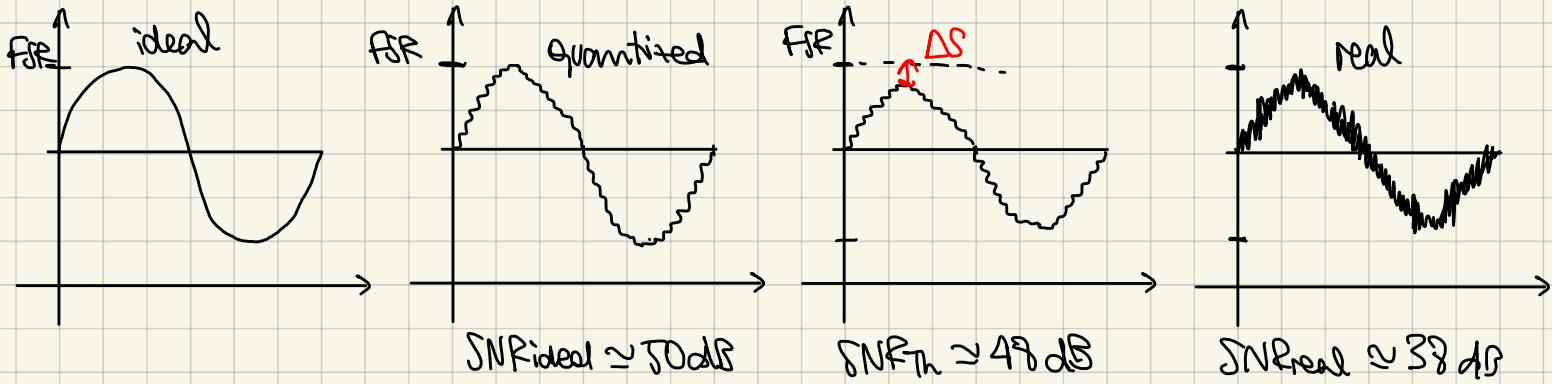
$$\text{if } \begin{cases} n=8 \text{ bit} \\ \text{FSR} = 5V \\ V_p = 2V \end{cases} \quad \text{SNR}_{\text{ideal}} [\text{dB}] = 6.02n + 1.76 \Big|_{n=8} \approx 50 \text{ dB}$$

$$\Delta S = \frac{2V}{2.5V} = 80\% \rightarrow \Delta S_{\text{dB}} = 20 \log_{10} \left( \frac{2V}{2.5V} \right) = -2 \text{ dB}$$

$$\Rightarrow \text{SNR}_{\text{Theoretical}} = \text{SNR}_{\text{ideal}, \text{dB}} - \Delta S_{\text{dB}} = 48 \text{ dB}$$

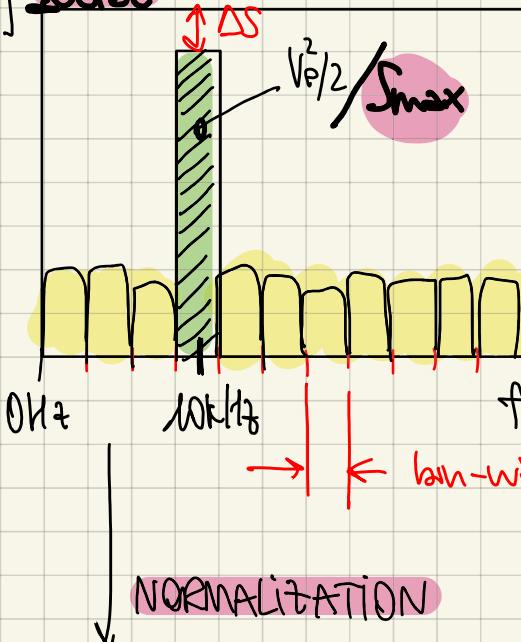
$$\text{SNR}_{\text{real}} = \frac{S_{\text{real}}}{N_{\text{real}}} = \frac{(V_p/2)^2 \cdot \frac{1}{2}}{N_{\text{electronic}} + N_{\text{quantization}}} = \text{SNR}_{\text{ideal}, \text{dB}} - \Delta S_{\text{dB}} - \Delta N_{\text{dB}}$$

$$\Delta N = \frac{N_{\text{electronic}}}{N_{\text{quantization}}} = 12 \text{ dB} \text{ (for instance)} \rightarrow \text{SNR}_{\text{real}} \approx 38 \text{ dB}$$



What about the spectrum

$[V^2]$   $\Delta f \Delta B$



$$S_{\text{real}} = \frac{V^2}{2} = 2V^2$$

$$N_{\text{min}} = N_{\text{quant}} = \frac{L \Delta B^2}{12} = 318 \mu V^2$$

$$NF = \frac{L \Delta B^2 / 12}{N_{\text{samples}} / 2}$$

NF = NOISE FLOOR

$N_{\text{samples}} = 100 \text{ samples}$

Why do we do That?

In This Way we can Compare different ADCs/ DACs Operating @ different FSRs

$$S_{\text{max}} = FSR = \frac{f_{\text{FSR}}^2 / 2}{\text{intensity}} = \frac{f_{\text{FSR}}^2 / 2}{\text{power}} = \Delta dB_c$$

$$SNR_{\text{ideal}} = \frac{S_{\text{max}}}{N_{\text{min}}} \Rightarrow SNR_{\text{ideal}, \text{dB}} = S_{\text{max}, \text{dB}} - N_{\text{min}, \text{dB}}$$

$$N_{\text{min}} = \frac{L \Delta B}{12} = \frac{L \Delta B^2}{12} \Rightarrow \begin{aligned} N_{\text{min}, \text{dB}} &= S_{\text{max}, \text{dB}} - SNR_{\text{ideal}, \text{dB}} = \\ &= \Delta dB_c - SNR_{\text{ideal}, \text{dB}} \\ &= \Delta dB_c - (6.02 n + 1.76) \text{ dB} \end{aligned}$$



$$N_{\text{min}, \text{dB}} = -SNR_{\text{ideal}, \text{dB}}$$

IDEAL NOISE FLOOR → is just due to Quant.

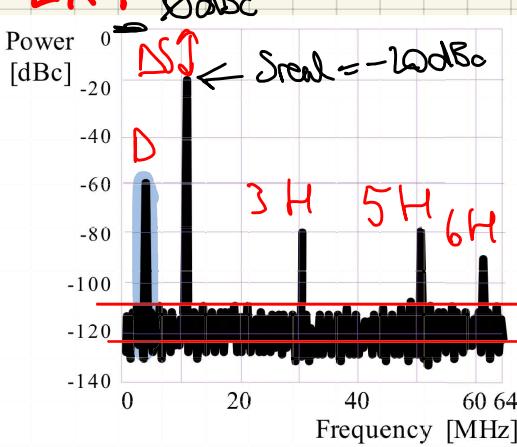
$$NF_{\text{ideal}} = \frac{N_{\text{min}}}{N_{\text{samples}} / 2} = -SNR_{\text{ideal}, \text{dB}} - 10 \log_{10} (N_{\text{samples}} / 2)$$

$$\Delta N = NF_{\text{real}} - NF_{\text{ideal}}$$



from The histogram

# EX1



DAC:  $n=12$  bit  $f_{FSR}=5 \text{ V}$  bin-width =  $2 \text{ kHz}$

distortion tone @ 5 MHz

$$N_{ideal} = N_{real} + \Delta N = 12 \text{ dB}$$

(A) Compute:  $\text{SNR}_{ideal}$ ,  $\text{SNR}_{th}$ ,  $\text{SNR}_{real}$ , and  $\text{ENOS}$

$$f_{S/2} = 64 \text{ Msps} \Rightarrow f_s = 128 \text{ Msps}$$

$$N_{samples} = \frac{f_s}{\text{bin-width}} = \frac{128 \text{ M}}{2 \text{ k}} = 64 \text{ k samples}$$

$$T_s = \frac{1}{f_s} = 7.8 \text{ ns} \quad N_{samples} = \frac{T_m}{T_s} \Rightarrow T_{measure} = T_s \cdot N_{samples} = 0.5 \text{ ms}$$

$$= 500 \mu\text{s}$$

$$S_{max} = (f_{FSR}/2)^2 \cdot \frac{1}{2} = 3.125 \text{ V}^2 = 0 \text{ dBc}$$

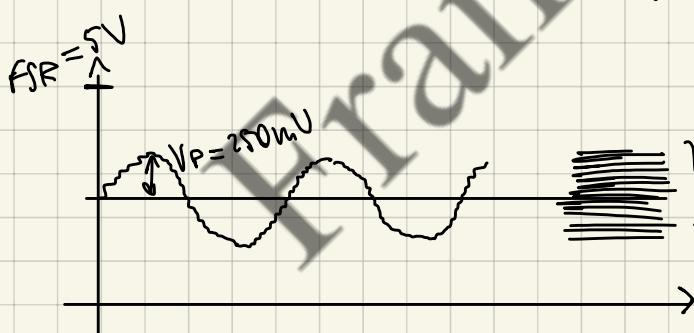
$$S_{real} = -20 \text{ dBc} \quad (= S_{max} - 20 \text{ dB})$$

$$\Delta S = \frac{2V_p}{f_{FSR}} = -20 \text{ dBc}$$

$$\text{if } 10^{-20/20} = 10^{-1} = 1/10$$

$$\Rightarrow \frac{2V_p}{f_{FSR}} = \frac{1}{10} = 0.1$$

$$\Rightarrow V_p = \frac{0.1}{2} \cdot 5 \text{ V} = 0.25 \text{ V} = 250 \text{ mV}$$



$$\left. \right\} 2^n = 2^{12} = 4096 \text{ levels}$$

but we'll exploit a lower # of levels:

$$4096 \cdot \frac{2 \cdot 250 \text{ mV}}{5 \text{ V}} = 410 \text{ levels}$$

# of LEVELS we use

$$\text{SNR}_{ideal} = 6.02n + 1.76 = 6.02 \cdot 12 + 1.76 = 74 \text{ dB}$$

$$\text{SNR}_{th} = \text{SNR}_{ideal} - \Delta S = 74 \text{ dB} - 20 \text{ dB} = 54 \text{ dB}$$

$$\text{SNR}_{real} = \text{SNR}_{ideal} - \Delta S - \Delta N = 74 \text{ dB} - 20 \text{ dB} - \Delta N$$

Noise Floor:  $N_{\text{real}} \approx -110 \text{ dBc}$

$$N_{\text{min}} = -\text{SNR}_{\text{ideal}} = -74 \text{ dBc}$$

$$N_{\text{ideal}} = N_{\text{min}} - 10 \log\left(\frac{N_{\text{samples}}}{2}\right) = -74 \text{ dBc} - 48 \text{ dB} = -122 \text{ dBc}$$

$$\Delta N = N_{\text{real}} - N_{\text{ideal}} = -110 \text{ dBc} - (-122 \text{ dBc}) = \underline{\underline{12 \text{ dB}}}$$

$$\Rightarrow \text{SNR}_{\text{real}} = -74 \text{ dB} - 20 \text{ dB} - 12 \text{ dB} = 42 \text{ dB}$$

\* ENOB is still missing

### (B) Compute The THD and The Si:NAD

$$\text{Distortion tone: } D = -60 \text{ dBc} = 0 \text{ dBc} - 60 \text{ dB} = \left(\frac{f_{\text{FSR}}}{2}\right)^2 \cdot \frac{1}{2} / 10^{60/10}$$
$$\stackrel{!}{=} \frac{(f_{\text{FSR}}/2)^2 \cdot \frac{1}{2}}{10^6} = 3.125 \mu\text{V}^2 \text{ (Power)}$$

$$D = \frac{f_{\text{FSR}}}{2\sqrt{2}} / 10^{60/10} = \frac{(f_{\text{FSR}}/2) \cdot \frac{1}{\sqrt{2}}}{10^3} = 1.77 \text{ mV}_{\text{rms}} \text{ (intensity)}$$

$$H = -90 \text{ dBc} - 90 \text{ dBc} - 90 \text{ dBc} = -270 \text{ dBc}$$

we cannot say that, bct we are dealing w/ dBc so w/ power



We have to convert each term to power

$$H = 10^{-90/10} + 10^{-90/10} + 10^{-90/10} =$$
$$\stackrel{!}{=} 10^{-9} + 10^{-9} + 10^{-9} =$$
$$\stackrel{!}{=} 2.1 \cdot 10^{-9} = 21 \cdot 10^{-9} = 10 \log_{10}(21 \cdot 10^{-9}) = -77 \text{ dBc}$$

$$\text{THD} = \frac{H}{S_{\text{real}}} = \frac{-77 \text{ dBc}}{-20 \text{ dBc}} = 3.85$$

$$= -77 \text{ dBc} - (-20 \text{ dBc}) = \underline{\underline{-57 \text{ dB}}}$$

TOTAL HARMONIC DISTORTION :

Notice: in this computation, of course  $H = H_{\text{real}}$  bct  $H_{\text{ideal}}$  should be 0

SIGNAL-TO-NOISE & DISTORTION RATIO

$$\text{Si:NAD} = \frac{S_{\text{real}}}{N_{\text{real}} + H + D} = \frac{-20 \text{ dBc}}{N_{\text{real}} - 77 \text{ dBc} - 60 \text{ dBc}}$$

$$N_{\text{real}} = N_{\text{ideal}} + \Delta N = N_{\text{min}} + \Delta N = -74 \text{ dBc} + 12 \text{ dB} = -62 \text{ dBc}$$

$$\Rightarrow S_{\text{iNAD}} = \frac{-20 \text{ dBc}}{-62 \text{ dBc} - 77 \text{ dBc} - 60 \text{ dBc}} =$$

$$\frac{-20 \text{ dBc}}{10^{-6.2} + 10^{-7.7} + 10^{-6}} = \frac{-20 \text{ dBc}}{1.65 \cdot 10^{-6}} = \frac{-20 \text{ dBc}}{10 \log_{10}(1.65 \cdot 10^{-6})} = \frac{-20 \text{ dBc}}{-58 \text{ dBc}}$$

$$= -20 \text{ dBc} + 58 \text{ dBc} = +38 \text{ dB}$$

NG c!

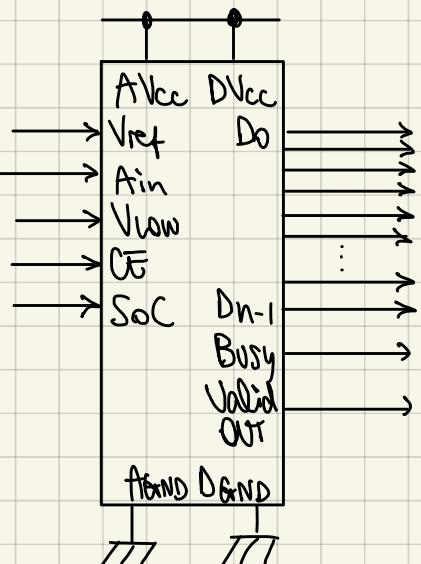
$$SNR_{\text{ideal}} = S_{\text{iNAD}}_{\text{real}}$$

$$6.02 \text{ ENOB} + 1.76 = S_{\text{iNAD}} \Rightarrow \boxed{\text{ENOB} = \frac{S_{\text{iNAD}} - 1.76}{6.02} = 6.6 \text{ bit}}$$

EFFECTIVE NUMBER OF BITS

### NOTICE:

- $A \text{ dBc} + B \text{ dBc} = 10 \underbrace{\text{dBc}/10}_{X} + 10 \underbrace{\text{dBc}/10}_{X} = 10 \log_{10} X = C \text{ dBc}$
- $A \text{ dB} \pm B \text{ dB} = (A \pm B) \text{ dB}$
- $A \text{ dBc} \pm B \text{ dB} = (A \pm B) \text{ dBc}$



$n = \# \text{ of bits}$	8	16
$2^n = \# \text{ of levels}$	256	65536
$FSR = V_{ref} - V_{low}$	5V	5V
$LSB = \frac{FSR}{2^n}$	19.5mV	76μV

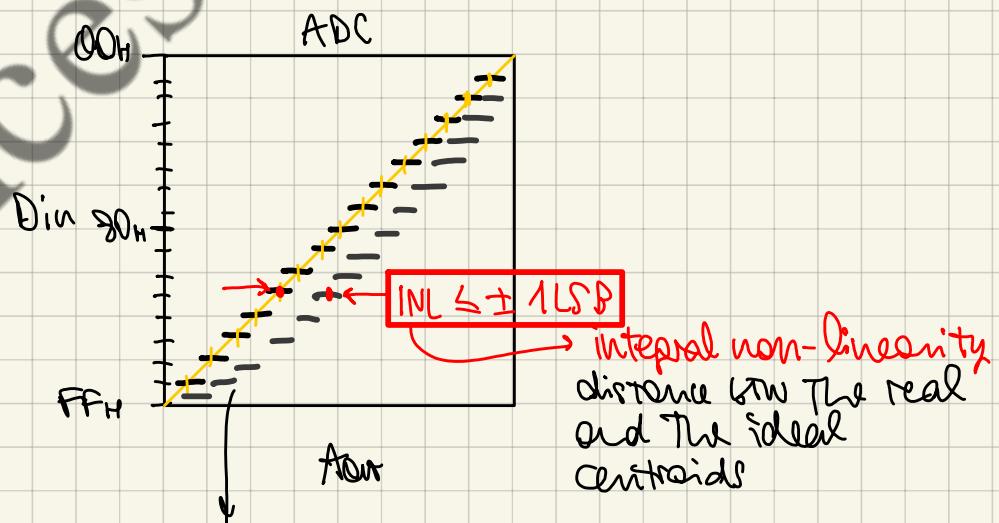
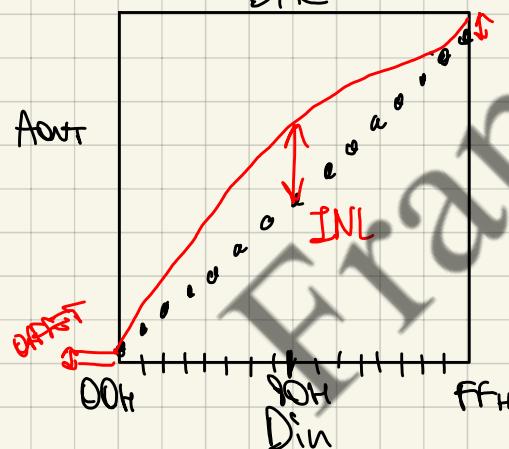
Busy : if Busy = 1 → you cannot read the output but the ADC is still converting

Busy = 0 → conversion is completed

CE : if CE = 1 → The ADC is ready to receive an input and start converting

if CE = 0 → The ADC is in LOW POWER CONSUMPTION MODE, so it's not working

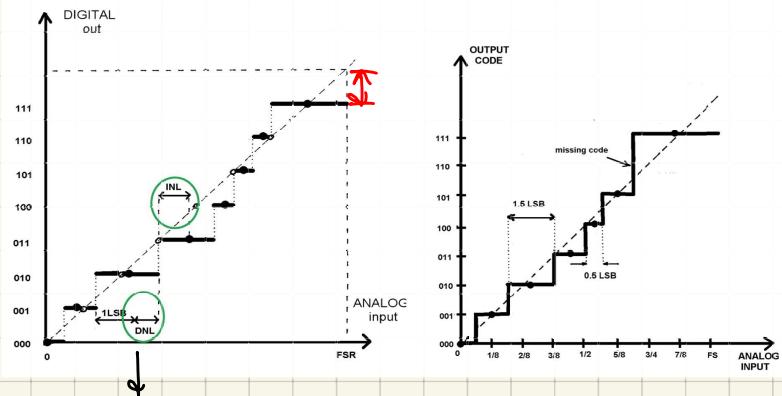
→ (notice: it's active high)  
 $\overline{CE} \rightarrow \text{active low}$   
 DAC



The output is formed by different steps whose centroids lie on the A<sub>in</sub> line

## DNL and INL

## Missing codes



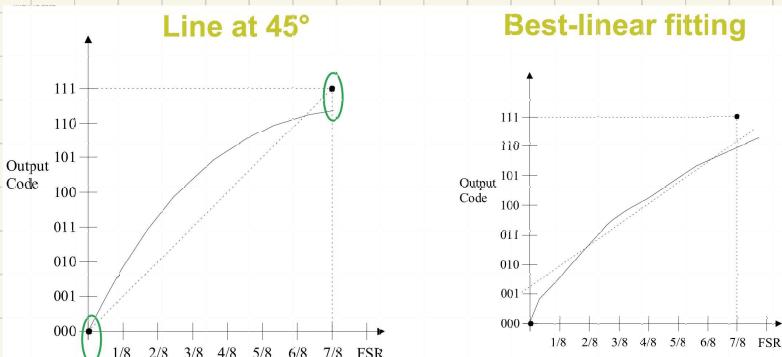
If the 1st step is @ 0V the last step is not @ FSR, but it's one code below

$$DNL_{ideal} = 1 \text{ LSB}$$

???

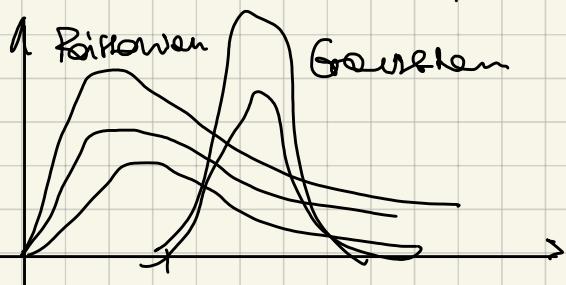
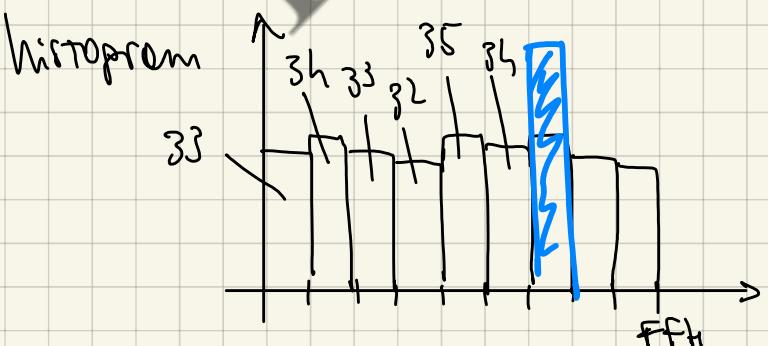
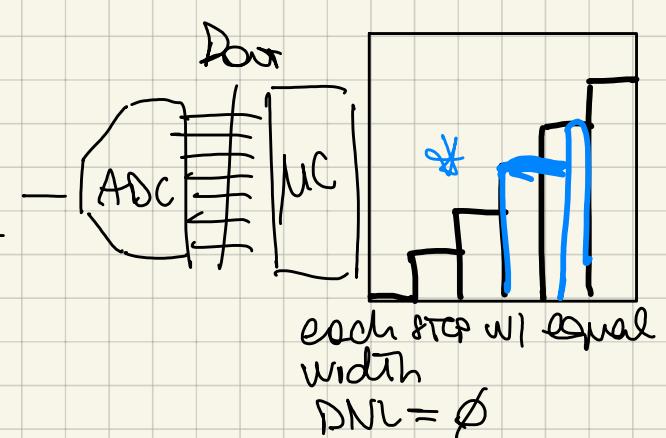
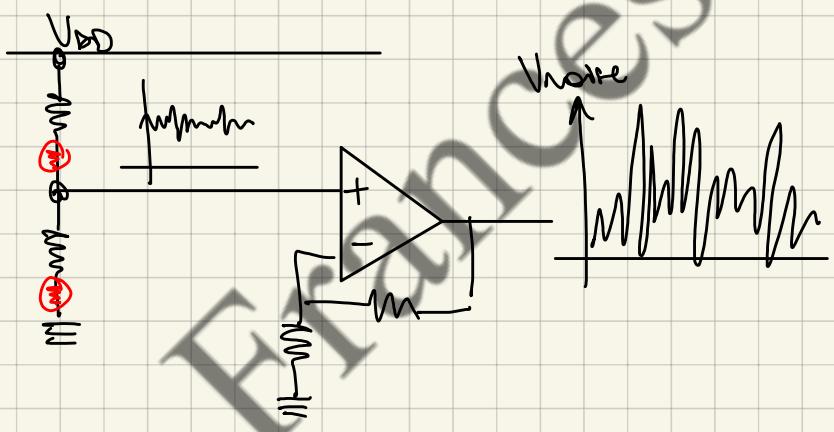
The DNL is related to the width of the steps  
if  $DNL = -1 \text{ LSB} \rightarrow \text{missing code}$

for some applications DNL and INL are not important, but just linearity is



Which applications require a good INL, which a good DNL and which a good linearity?

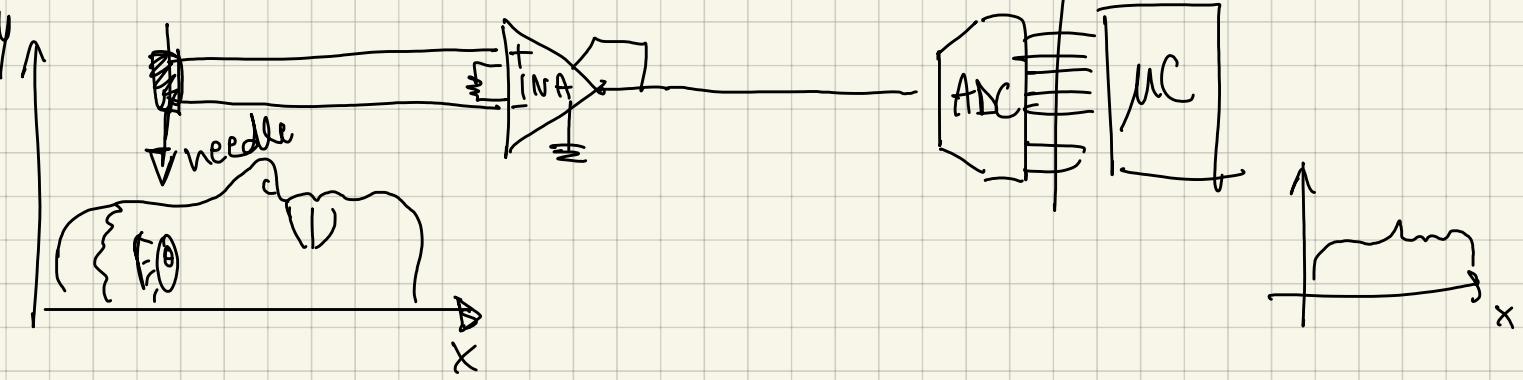
① Generation of a random number



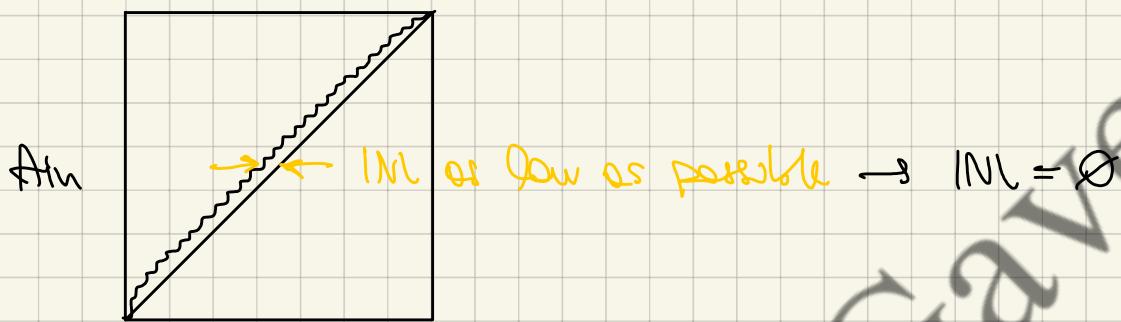
DNL is a random number only if  $DNL = 0$  (all steps have same width)  
if a step had a different width \*

$\hookrightarrow$  or  $DNL = \text{constant}$  at least

## ② Photometer

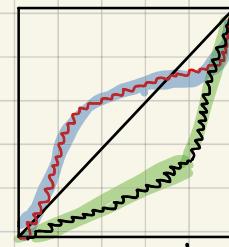
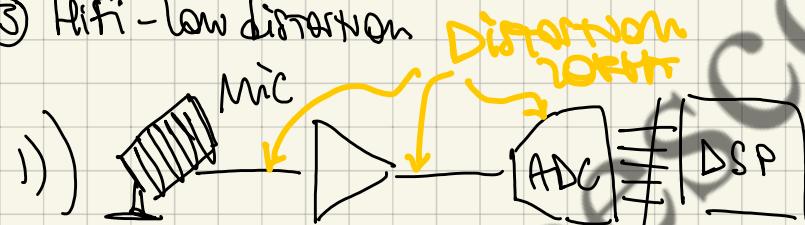


In this case what's important is the INL bct for each height of the needle we want the obtained value to be as ideal as possible

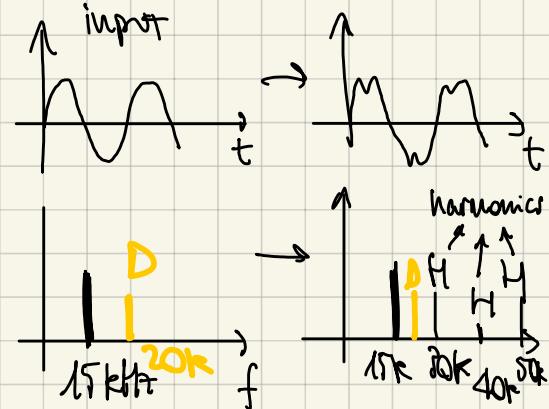


Even in this case it's not very realistic having  $INL = 0$  for any possible value

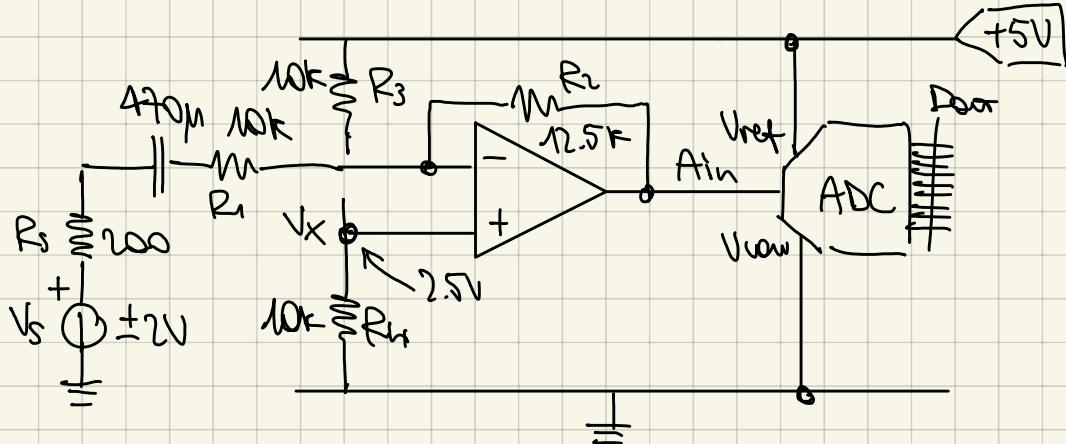
## ③ HiFi - low distortion



A non-linear input-output curve causes distortion



## DRIVING AN ADC



Only if  $A_{in} = [0V, 5V] \rightarrow D_{out} = [00H, FFH]$

if The sensor has a limited swing, we have to amplify it to properly add a so called non-conditioning stage

This means that in case of a 8 bit ADC for instance, we are able to read all the 256 levels only if  $A_{in}$  moves from 0 to 5V

In This case we need an amplification that brings The 4V input swing to be 5V

when  $V_s = 0V \Rightarrow V_{out} = 2.5V$

when  $V_s = \pm 2V \Rightarrow V_{out} = +5V$  or  $0V$

We also need to introduce The capacitor, b/c we want That  $V_x$  goes to The output w/  $f=1$  while  $V_s$  goes to The output w/ a different gain

@DC  $\rightarrow G = 1 + R_2/R_1$  where  $R_1 = \infty \Rightarrow G = 1 \Rightarrow A_{out} = 2.5V$

@HF  $(f > \frac{1}{2\pi R_1 C_{eq}}) \rightarrow G = -\frac{R_2}{R_1 + R_S} = -\frac{12.5k}{10.2k}$

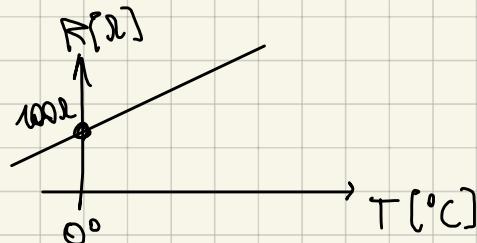
## EXAMPLE: TEMPERATURE METER

Specs: precision =  $0.1^\circ C$

temperature =  $-100^\circ C \div +200^\circ C$

let's use The thermoresistance PT100

$$\begin{cases} 100\Omega @ 0^\circ C \\ +0.385\Omega / ^\circ C \end{cases}$$



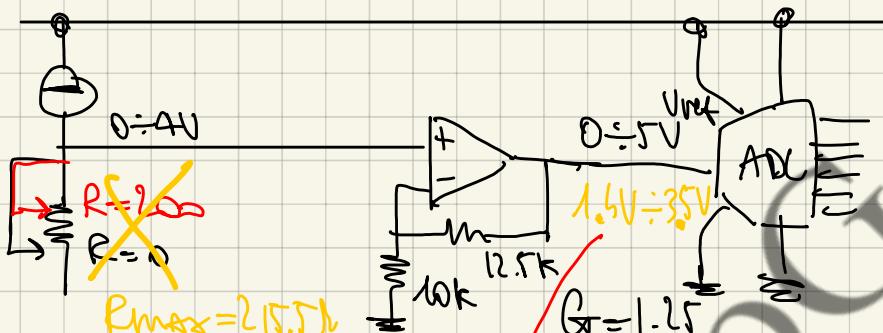
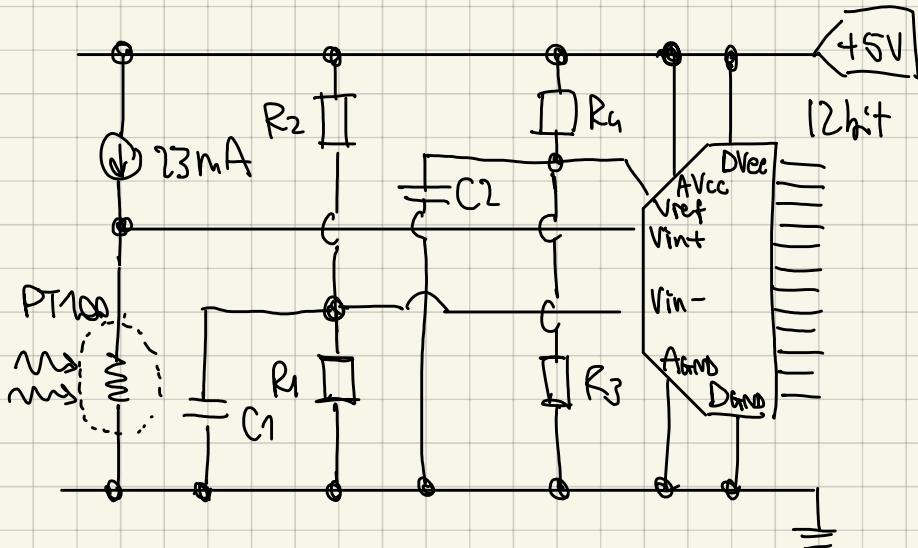
$$\Rightarrow R(T = -100^\circ C) = 100\Omega - 0.385 \cdot 100 = 100\Omega - 38.5\Omega = 61.5\Omega$$

$$R(T = +200^\circ C) = 100\Omega + 0.385 \cdot 200 = 100\Omega + 77\Omega = 177\Omega$$

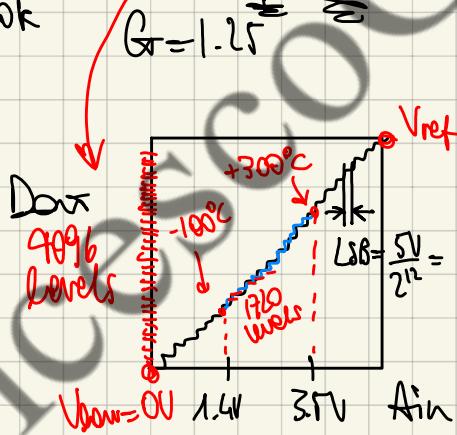
$$\Rightarrow R = 61.5\Omega \div 177\Omega$$

DISCRETIZATION  $400^\circ C / 0.1^\circ C = 4000 \approx 4096 = 2^{12} \Rightarrow 12$  bit

$$LSB = \frac{FSR}{2^n} = \frac{215.5 - 61.5}{2^12} = 39.5 \text{ mV}$$



$$\begin{aligned} R_{max} &= 215.5 \Omega \\ R_{min} &= 61.5 \Omega \end{aligned}$$



$$\begin{aligned} \text{fixed levels} \\ V_{ref} = 5V \end{aligned}$$

$$\begin{aligned} 4096 \\ \text{actual levels} = 2^12 \cdot \frac{(3.5 - 1.4)}{5} \\ = 4096 \cdot 0.32 = \\ = 1720 \text{ levels} \end{aligned}$$

We don't exploit the full dynamic of our ADC

Notice: we have this limitation but we set

$$\begin{cases} V_{low} = 0V \\ V_{ref} = 5V \end{cases}$$

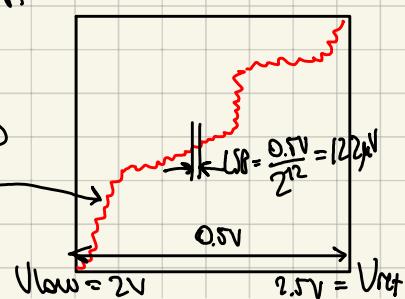
How to solve? EASY! → Let's connect  $\begin{cases} V_{low} = 1.4V \\ V_{ref} = 3.5V \end{cases}$

In this way when  $T = -100^\circ\text{C} \rightarrow V_{in}^+ = V_{in}^- = 1.43V \Rightarrow Dout = 00H$

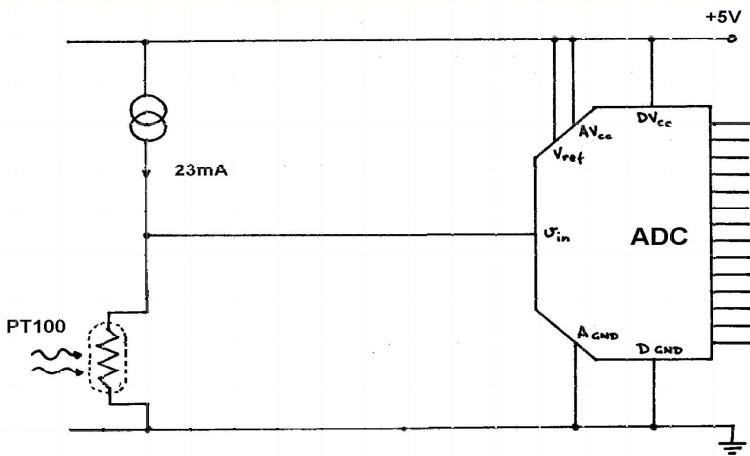
$$\begin{aligned} T = +300^\circ\text{C} \rightarrow V_{in}^+ = +3.5V \\ V_{in}^- = 1.4V \Rightarrow Dout = ffH \end{aligned}$$

What happens if we drastically change  $V_{low}$  and  $V_{ref}$ ?  $\Rightarrow$

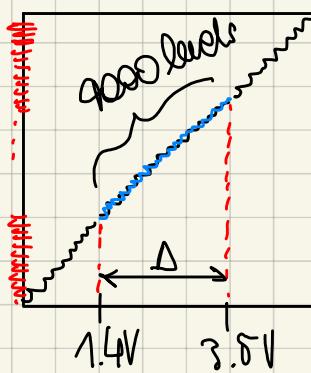
Quality degrades



## BEST SIZING



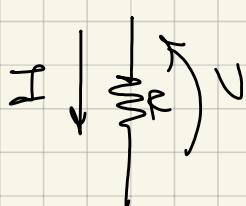
We want an ADC that allows us to have 4000 levels b/w 1.4V and 3.5V



$$\text{Actual levels} = 2^n \frac{(3.5 - 1.4)}{5} = 4000$$

$$\Rightarrow n = \log_2 \left( 4000 \frac{5}{3.5 - 1.4} \right) = 13.21 \rightarrow \text{let's choose } \boxed{n = 14 \text{ bit}}$$

ISSUE: we are pumping current into a resistor  
 ↓  
 SELF-HEATING

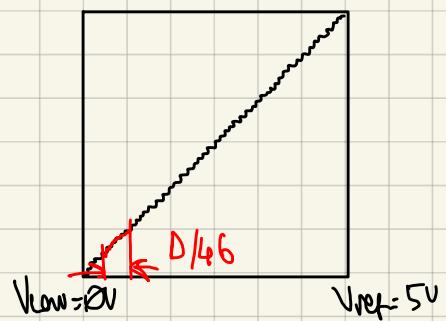
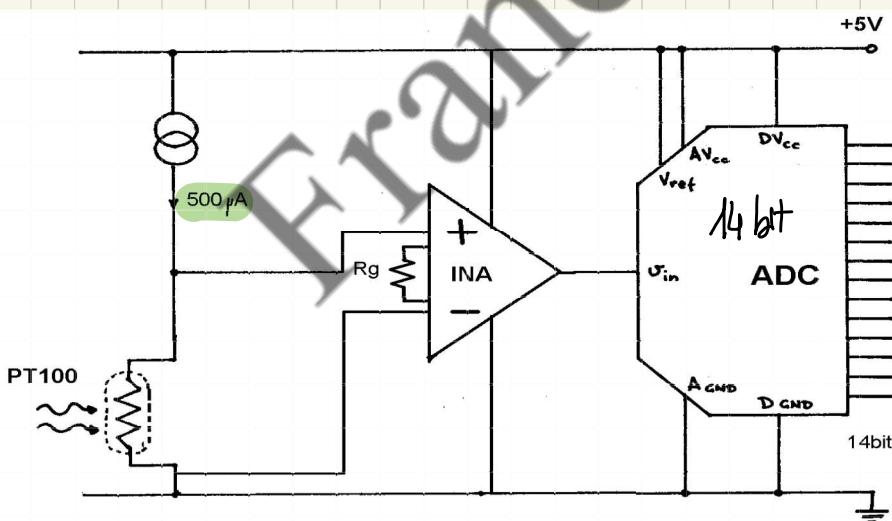


$$P = RI^2 = \frac{V^2}{R} = VI \quad [\text{W}]$$

which transforms in heat

In this way we are heating up the sensor

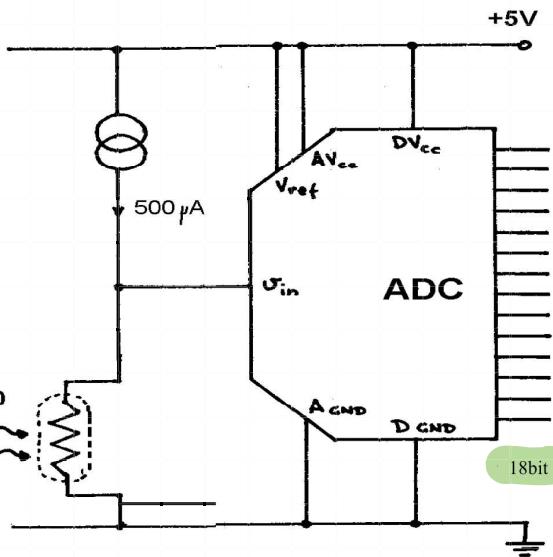
How can we solve this issue? → reduce P → reduce I



To regain the factor 46 that has been lost we use an INA w/ gain equal to 46

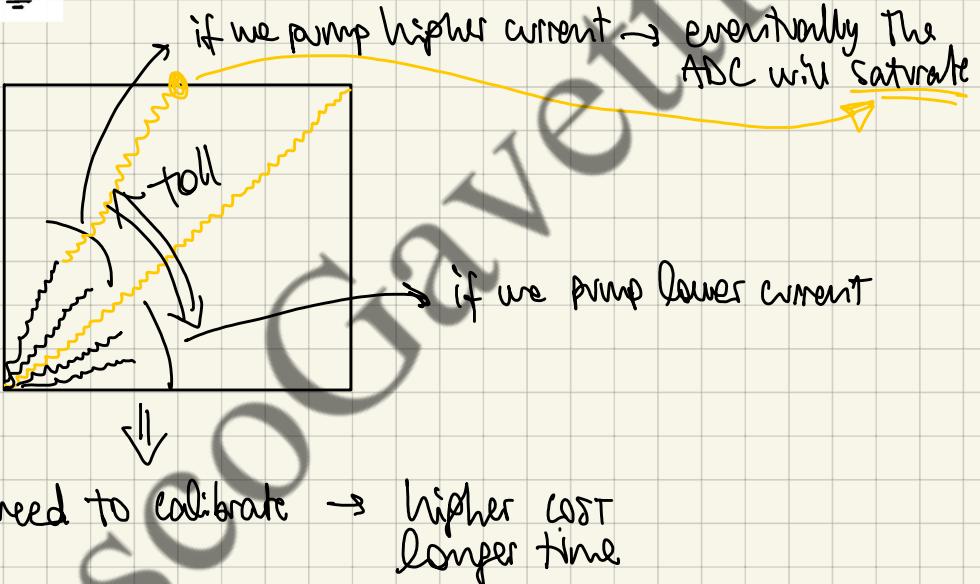
ISSUE: EXPENSIVE  $\begin{cases} 46 \text{ ADC} \\ 3 \text{ INA} \end{cases}$  for mass production

FINAL SOLUTION: higher resolution ADC

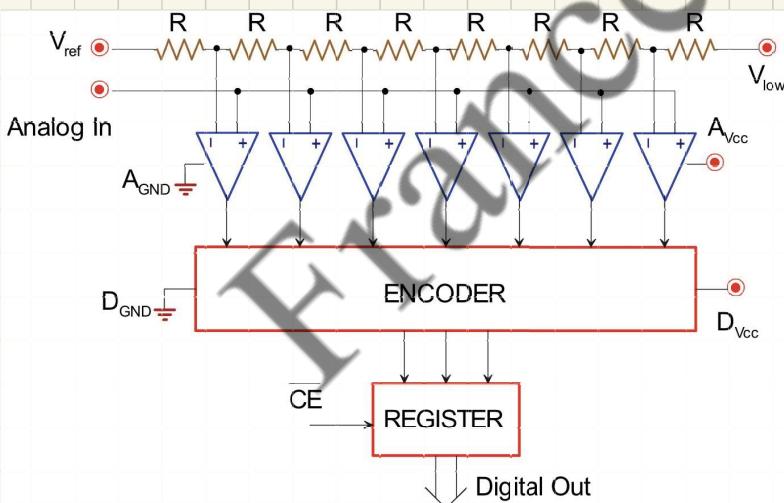


→ 5€ → cheaper and it needs no calibration

if  $0.5\text{mA} (1 \pm \text{toll}) \Rightarrow$



## FLASH ADC



ISSUE: we have to "create" all the potentiometer values

for a 8 bit ADC we need 256 resistors

Components {  
 $2^n$  resistors  
 $2^n$  comparators  
1 "Thermometric" code
}

What does "Thermometric" mean?

The DIGITAL ENCODING NETWORK (ENCODER) converts The  $2^n$  inputs into  $n$  outputs

$$0000 \quad 0000 = 0V$$

$0$        $0_H$

$$0000 \quad 0001 = 19mV = LSB$$

$0$        $1_H$

|      |

$$1000 \quad 0000 = 2.5V$$

$8$        $0_H$   
|      |

$$1111 \quad 1111 = +5V = FSR$$

$F$        $F_H$

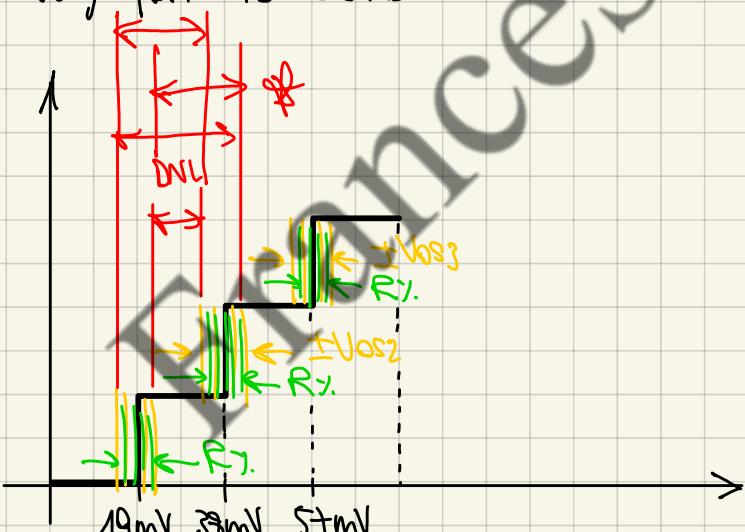
The MSB is in charge to set half of FSR

The immediately "lower" bit is in charge to set half of FSR/2

$$\hookrightarrow 0100 \quad 0000 = 1.25V = \frac{FSR}{2} = \frac{2.5V}{2}$$

This means that the MSB has a weight of  $\frac{1}{2} FSR$  while the LSB has a weight of  $FSR/2^n$

PRO: very fast  $T_c < 50\text{ ns}$



$\Rightarrow$  These "issues" cause the DNL  $\star$

$$LSB_{ideal} = 19mV$$

if  $WL \leq \pm 100mV = \pm 5 LSB \rightarrow$  NOT good  $\textcircled{z}$

$\hookrightarrow$  The ADC is 4 times worse

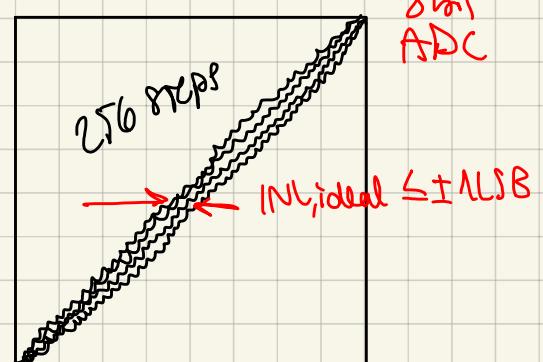
$\hookrightarrow$  The ADC behaves like a 6-bit ADC

Each comparator has its own offset which causes jitter in output

Each R has its own tolerance which causes jitter too



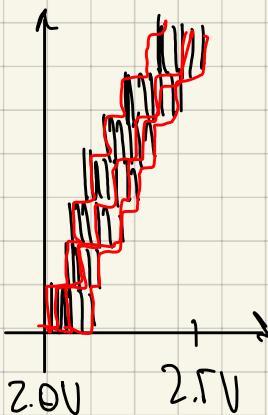
I want the resistors to be equal one to the other



let's suppose we design the ADC in a very good way, in order to have  
 $V_{os} = \pm 1\text{mV} < 1\text{LSB} = 19\text{mV}$

let's suppose we apply  $V_{ref} = 2.5\text{V}$  and  $V_{in} = 2\text{V}$

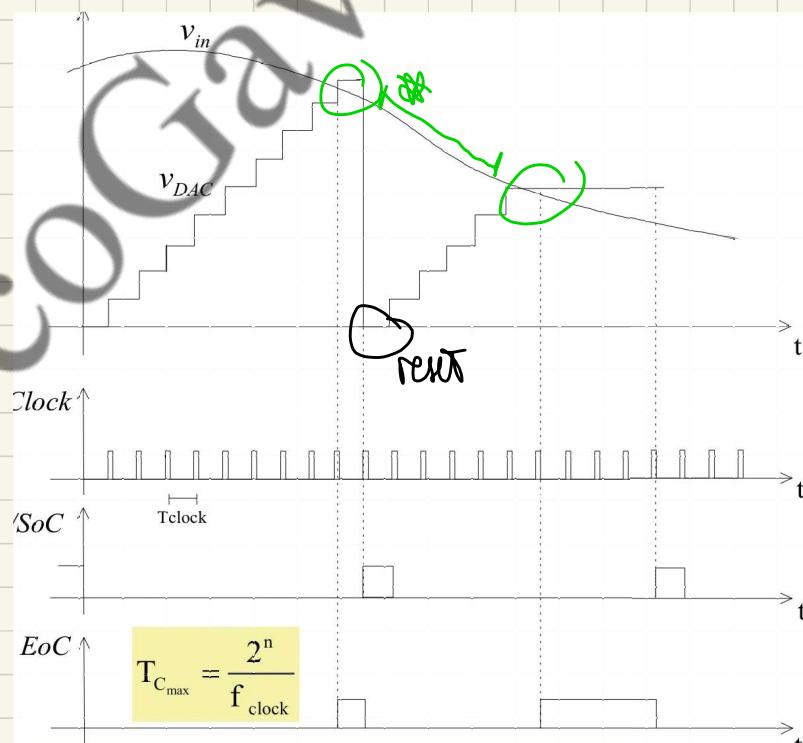
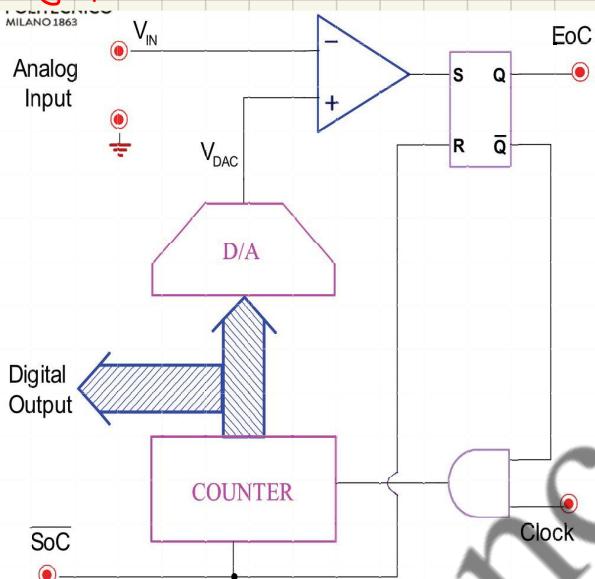
$$\text{w/ a 8bit ADC} \rightarrow 0.5\text{V}/256 = 1.95\text{ mV} = 1\text{LSB}$$



$\Rightarrow$  we have overflowing

Very bad! ( ): we have reduced the width b/w one "Tap" and the other, but the offset of the comparator stays constant

### STAIRCASE ADC



MAXIMUM CONVERSION TIME

$$T_{Cmax} = 2^n T_{clock} = \frac{2^n}{f_{clock}}$$

Components } 1 DAC  
  1 counter  
  1 comparator

PRO: precision depends on DAC

CON: not very fast  $T_c > 1\text{ms}$

The idea is to change, w/ subsequent adjustments, the binary code @ The DAC input until its output voltage reaches the input signal value

The code that gives this condition will be the ADC output

This way to proceed requires a comparator w/ precision (hence offset) lower than  $\pm \frac{1}{2}\text{LSB}$

The staircase ADC implements a simple sequential search feeding the DAC w/ a binary counter, which forces a staircase at the output of the DAC

if  $S_{oC} = 1 \rightarrow \overline{S_{oC}} = 0 \rightarrow$  The flip flop (ff) is held w/  $\frac{Q}{Q} = Q$   
 $\overline{Q} = 1$

which means that the clock signal  $Clk$  can get to the counter through the AND  
 BUT since  $S_{oC} = R = 0$  the counter is kept at zero!

when  $S_{oC} = 0 \rightarrow \overline{S_{oC}} = 1 \rightarrow R = 1 \rightarrow$  The counter starts its counting which will stop when  $V_{DAC} = V_{in}$   
 → at this point the FF will set the EoC and simultaneously disable the clock to reach the counter, setting  $\overline{Q} = 0$   
 ⇒ The value in the counter will be the output of the ADC

We can easily understand why the precision of the conversion depends on that of the DAC which must have small offset and non-linearity errors

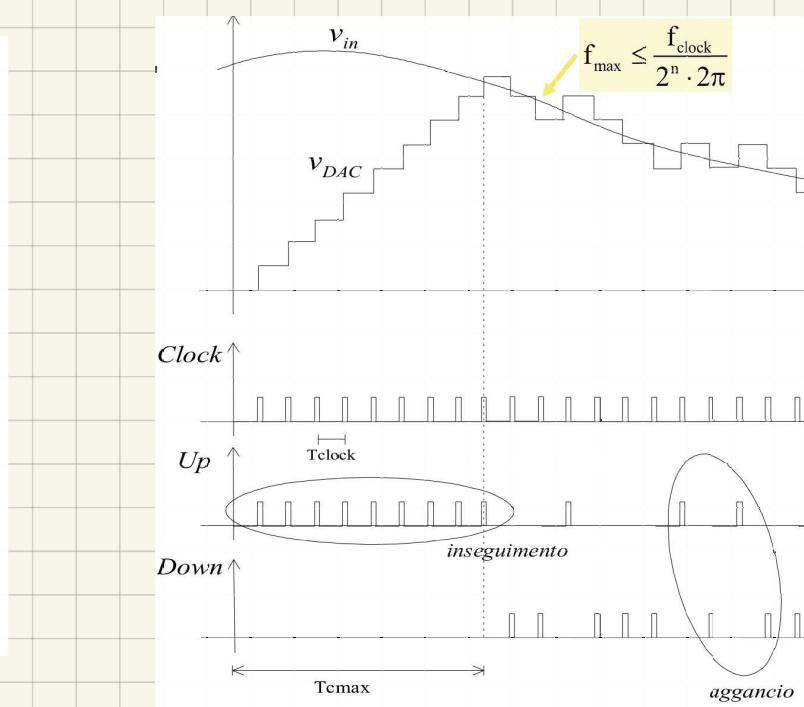
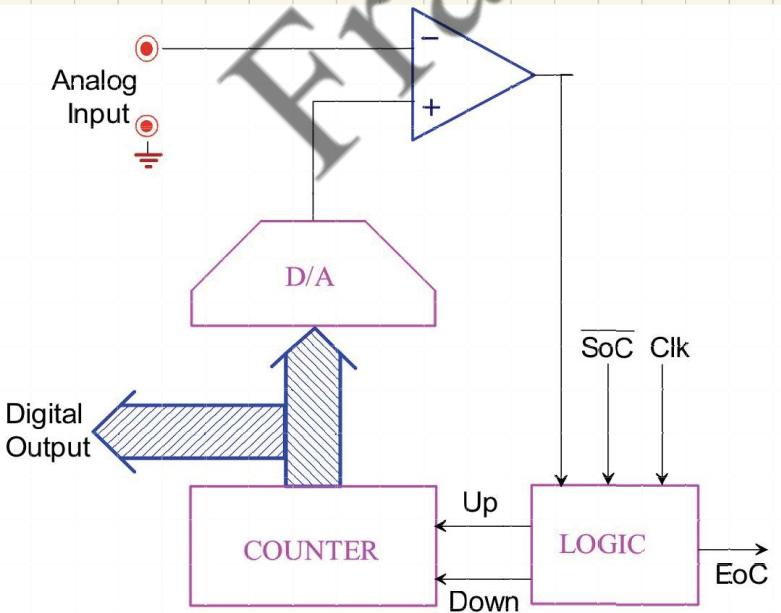
When  $V_{DAC} = V_{in}$  the counting is resetted so the ADC cannot properly follow the varying of the input signal, as we can easily see from the plot \*

example: 10 bit ADC w/  $f_{clock} = 10 \text{ MHz} \rightarrow T_c = 2^{10} / 10 \text{ MHz} = 102.4 \mu\text{s}$

$$\Rightarrow f_s = \frac{1}{T_c} \approx 10 \text{ kHz} \rightarrow f_{in, MAX} < \frac{1}{2} f_s = 5 \text{ kHz}$$

Another disadvantage of the STAIRCASE ADC is represented by the fact that the sampling comb is not constant

### TRACKING ADC



In The TRACKING ADC The counter is not simply reset and progressively increased as in the previous case, but The counting increases or decreases depending on whether The input voltage is greater or lower than that given by The DAC

↓  
doing This The DAC is able to follow the signal which slowly varies in time remaining attached to it at every clock period

The UP-DOWN COUNTER is driven by a simple VGTIC gate

$SOC = 1 \rightarrow \overline{SOC} = 0 \rightarrow$  counter is reset

$SOC = 0 \rightarrow \overline{SOC} = 1 \rightarrow$  different phases:

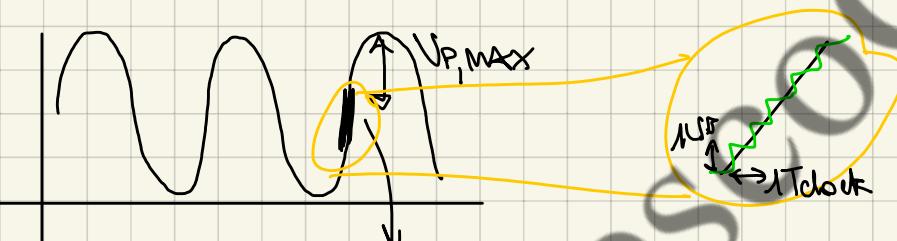
- "ATTACHING" PHASE  $\rightarrow$  only up

- Once  $V_{DAC}$  attached  $V_{IN} \rightarrow$  up and down  
 $\Rightarrow$  TRACKING PHASE

Notice: every  $T_{clock}$   $V_{DAC}$  changes by just 1LSB



So let's decide what's  $T_{clock}$  to properly track  $V_{IN}$



$$\frac{dV}{dt} = 2\pi V_p f \cos(2\pi f t) \rightarrow \left| \frac{dV}{dt} \right|_{MAX} = 2\pi V_{P, MAX} f_{MAX}$$

$$\frac{dV}{dt} = \frac{1 \text{ LSB}}{T_{clock}} = FSR \cdot f_{clock}$$

$$\Rightarrow f_{clock} = \frac{2^n}{FSR} \cdot 2\pi V_{P, MAX} f_{MAX}$$

$$\Rightarrow f_{MAX} \leq \frac{f_{clock}}{2^n \pi}$$

example: 10 bit ADC  $f_{clock} = 10 \text{ MHz}$

$$f_{MAX} \leq \frac{10 \text{ MHz}}{1024 \cdot \pi} \approx 3 \text{ kHz}$$

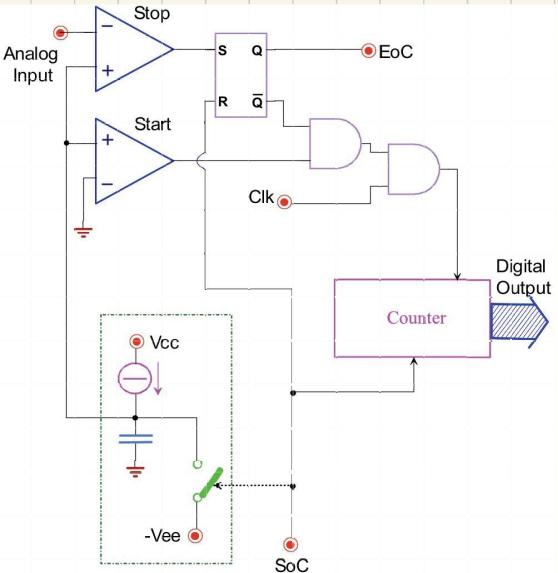
Components

1 DAC
1 Counter
1 Comparator
1 Up/Down combinational logic

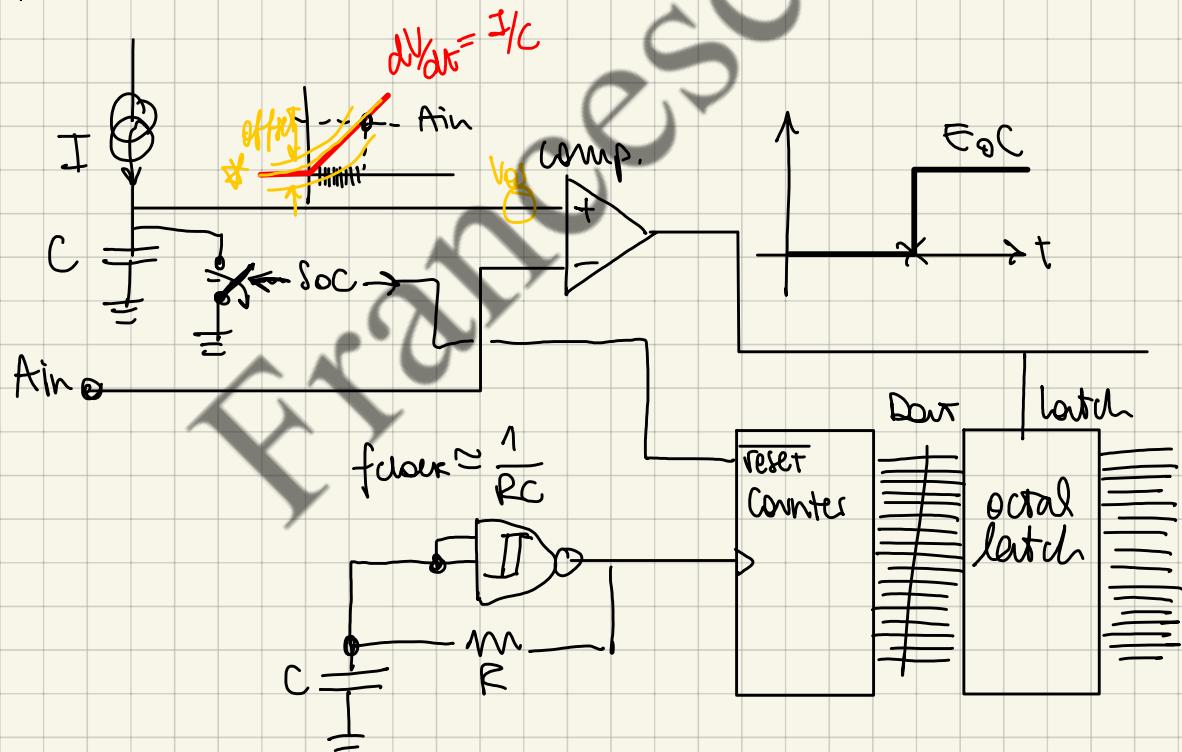
PROS : { precision depends on DAC  
fast :  $T_c > 100\text{ns}$

Notice : The signal of EoC (to make sure that Dout is correct, so that the counter has effectively hooked Vin) should be obtained through a simple logic network that checks the alternation of ups and downs

## SINGLE-SLOPE ADC (SINGLE RAMP)



This converter is based on a working principle similar to that of the staircase ADC but it uses an analog ramp instead of a digital staircase to make the comparison, thanks to a constant current source and a capacitor, instead of a clocker and a counter.



\* Ifnes

Going back to the actual circuit, we can see:

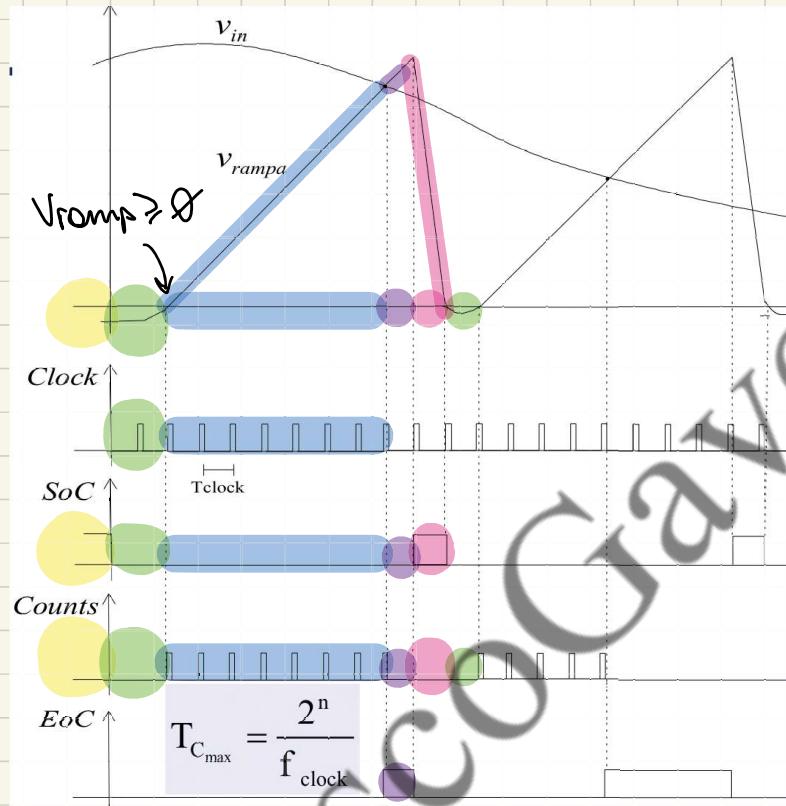
Until  $\text{SoC} = 1$  the ramp doesn't start and the counter is kept @ 0

When  $\text{SoC} = 0 \rightarrow$  a linear charge will develop across the capacitor, just like a ramp  $\frac{dv}{dt} = \frac{I}{C}$

When the ramp exceeds  $\delta$ , thanks to the start comparator, the clock signal can reach the counter and the counting effectively starts.

When the ramp reaches  $V_{in}$ , the stop comparator will set  $EoC = 1$  and the counting stops.

At this point, SoC is set again ( $=1$ ) in order to reset the counter which is then able to start the counting again.



$SoC = 1 \rightarrow$  The ramp doesn't start, the counting neither as the clock signal cannot reach the counter.

The start comparator is introduced before the closure of the switch which enables the capacitor charge is not instantaneous.

So the start comparator enables the counting only when  $V_{rampa} \geq \delta$

Components

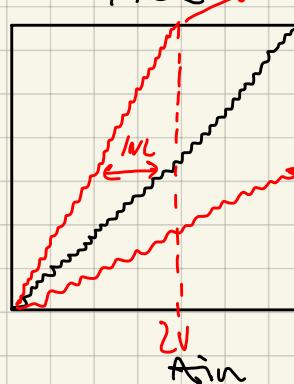
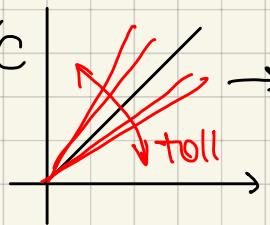
- 2 comparators
- 1 FF
- 1 logic
- 1 counter
- 1 current generator
- 1 capacitor

ISSUE① : very slow  $T_c > 1ms$  (MAIN)

ISSUE② → tolerances  $\rightarrow 45^\circ$

If the ramp is ideal  $\frac{dV}{dt} = I/C$

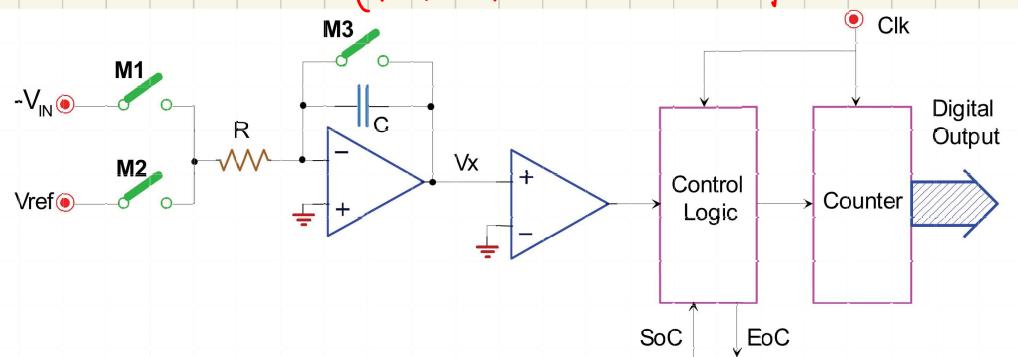
$$\frac{dV}{dt} = \frac{I(1+toll, I)}{C(1+toll, C)} = \frac{I}{C} (1 \pm 2 toll)$$



Due to tolerances of  $I$  and of  $C$ , the slope  $(dV/dt)$  can change a lot, so  $Dout$  may change a lot too.

How can we improve?  $\rightarrow$  Let's buy components w/ low tolerance  $\rightarrow$  1% tolerance is not sufficient

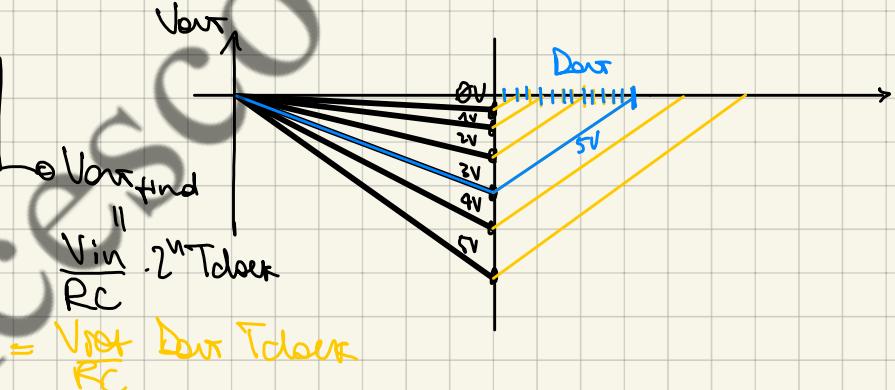
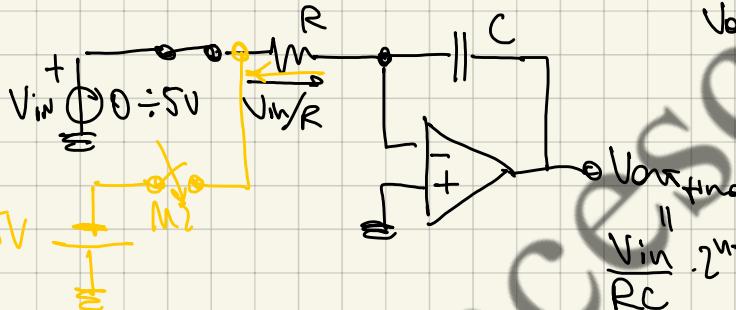
## DUAL-SLOPE ADC (INTEGRATING ADC)



$$T_{\text{clock}} = 2 \frac{2^n}{f_{\text{clock}}}$$

Integrate the two different currents into the capacitor in order to compensate the band behavior

1. M1 and M2 open, M3 close  $\rightarrow$  in order to completely discharge C  
done this, we open M3
2. reset control logic and counter
3. M1 close, M2 and M3 still open  $\rightarrow$   $V_{in}/R$  starts integrating into C



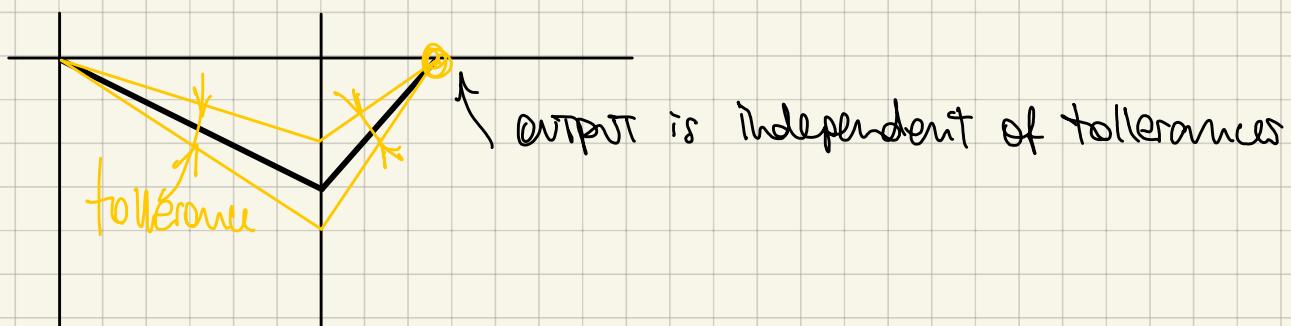
I equate the two equations and I find Dout

$$\frac{V_{\text{in}} \cdot 2^n \cdot T_{\text{clock}}}{R \cdot C} = \frac{V_{\text{ref}} \cdot D_{\text{out}} \cdot T_{\text{clock}}}{R \cdot C} \Rightarrow D_{\text{out}} = 2^n \frac{V_{\text{in}}}{V_{\text{ref}}}$$

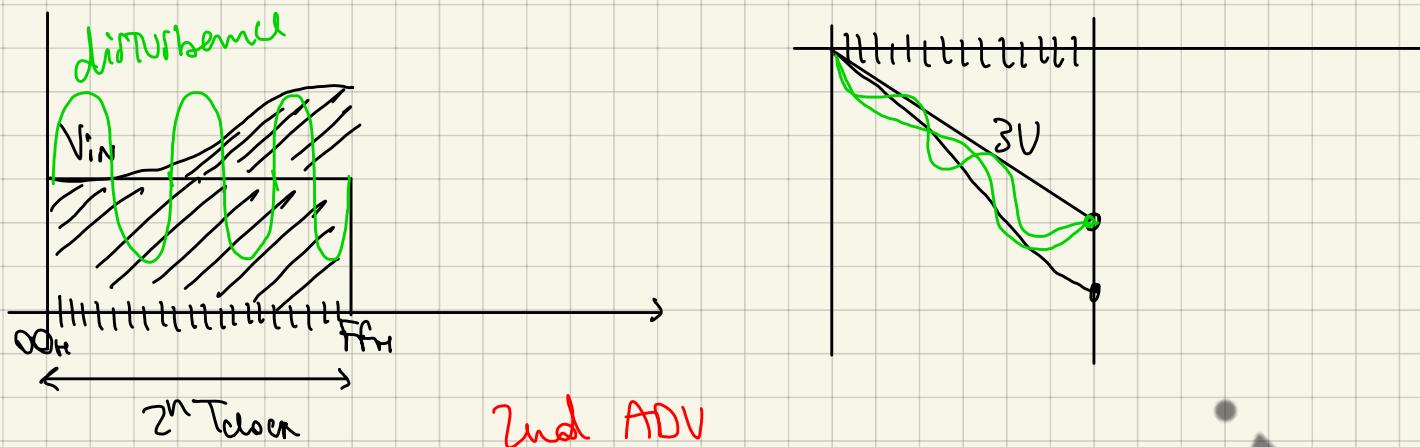
- independent of C
- independent of R
- independent of Tclock

1ST ADV

$\Rightarrow$  This means that Dout is independent of the tolerance too!!! 😊



GREAT ADVANTAGE → we are integrating  $V_{IN}$  (and not just a constant current)



⇒ This Dual-Slope ADC is able to reject disturbances w/ frequencies that are multiple of the integration period!

so if  $f_{disturb} = X \cdot \frac{1}{2^n T_{clock}}$  → the disturbance will be rejected

ES13 - ADC (2)  
24/11/2021

## SUMMARY ABOUT STANDARD ADCs

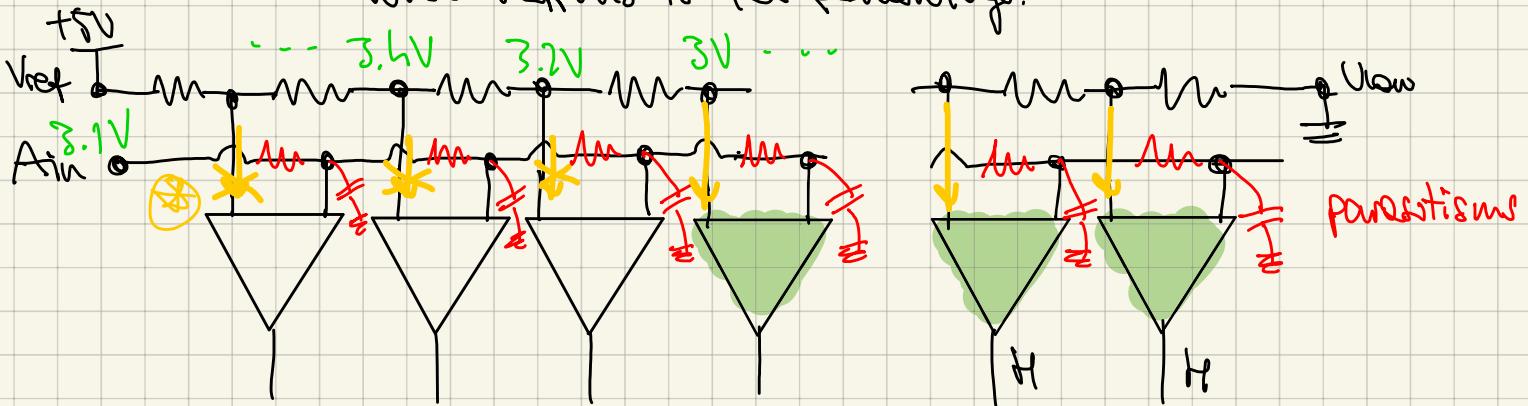
### ① FLASH ADC

↳ Many issues given by the presence of many resistors and comparators and so by the presence of their tolerance and offset respectively

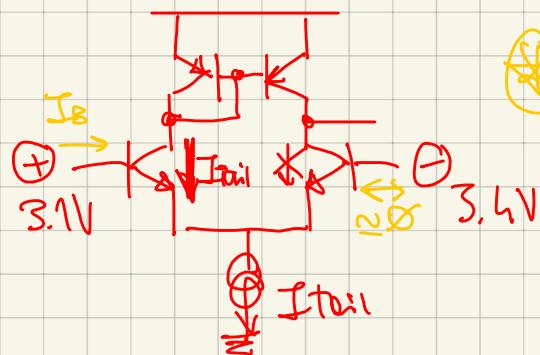
↓  
tolerance of resistors and offset of comparators cause jitter in the commutation threshold

furthermore, since these opamps are used as comparators, so they do not have a negative PS but a positive one, if the inputs differ too much it may happen that the comparator is completely imbalanced @ the input

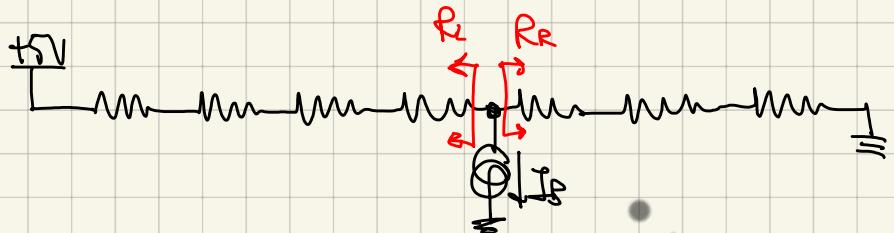
↓  
so  $I_{S1} \neq I_S \rightarrow$  the input bias currents completely mismatch and what happens is the following:



Since  $A_{in} = 3.1V$ , The comparators at the right of  $3V$  are completely triggered so their output is  $H$ , while the output of the comparators before  $3V$  is still  $L$ , but they're not triggered yet.



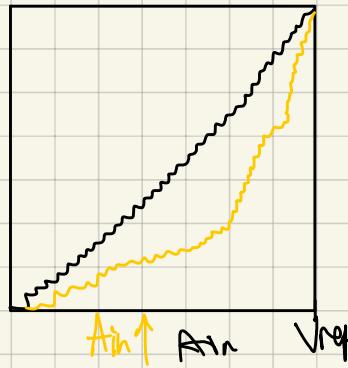
If the comparator is too much unbalanced in input what happens is that we have  $I_{S1}$  only on one input of the comparator



$$DV = I_S \cdot R_{eq} \quad \text{where } R_{eq} = R_L \parallel R_R$$

The voltage drop changes a lot and this is another reason why in a typical flash ADC the  $A_{in}$ - $Dout$  relationship is not ideal or expected to be

Dout



By changing  $A_{in}$  we change the comparators that are triggered and that ones that are not

↓  
The triggered comparators sink current from the ladder while the not-triggered ones don't

We could improve the performance by reducing the # of comparators and the value of their parasitic resistances

## ② STAIRCASE ADC

It's based on:

- 1 comparator
- 1 counter
- 1 DAC → it generates a staircase

Once the staircase reaches  $V_{in}$ , then the comparator triggers and stops the conversion and sets  $f_{osc} (=1)$

ISSUE: not fast  $T_C > 100\mu s$

↓ SOLUTION

③ TRACKING ADC → it improves the staircase ADC by introducing a counter that can go both upwards or downwards and so in this way is able to track  $V_{in}$  if  $f_{max} \leq \frac{f_{clock}}{2^n T}$

④ SINGLE-SLOPE ADC → instead of using an ADC which generates a staircase we could use a DC current generator and a capacitor which generate a ramp

Even in this case, once  $V_{IN}$  is reached, the conversion stops

ISSUE: very slow  $T_C > 1ms \Rightarrow$  we need to improve it

another relevant issue is that due to tolerances of  $I$  and  $C$  the slope  $dV/dt$  can change a lot, consequently also the reaching of  $V_{IN}$  (the crossing point) changes a lot and so even  $DOUT$  changes a lot

↳ we could decrease the tolerances or even better, we could implement a double integration in order to compensate the bad behavior

#### (4) Dual-Slope ADC

1st phase: ( $T_1 = 2^n T_{clock}$ ) we integrate  $V_{IN}$  (actually deintegrate)

2nd phase: ( $T_2 = n T_{clock}$ ) we integrate  $V_{ref}$  which is the highest possible  $V_{IN}$  value and so the slope is very steep

We obtain that  $DOUT = 2^n \frac{V_{IN}}{V_{ref}}$  which is independent of  $R$  and  $C$



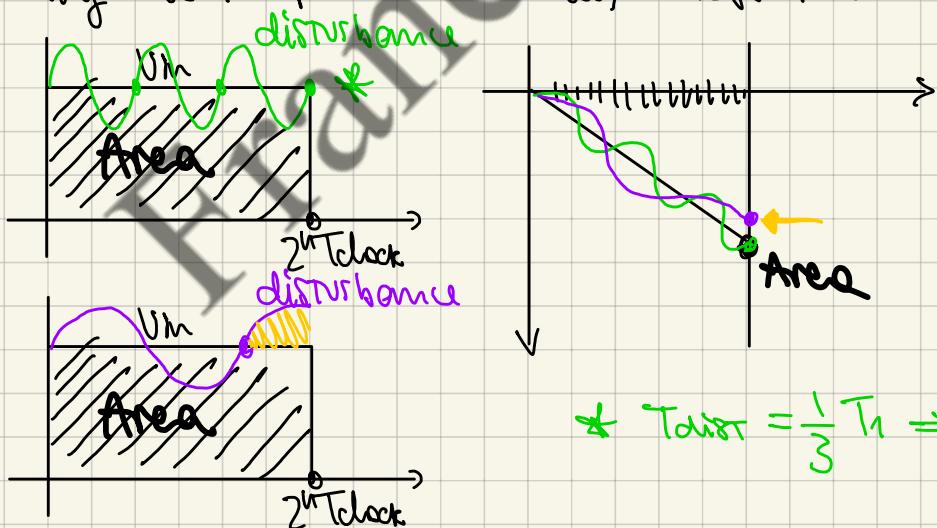
This leads to two advantages:

1. Since we integrate in the 1st phase and we deintegrate in the 2nd one, through the same  $R$  and  $C$ , if due to tolerances we have a spread in the slope of the 1st phase, the same spread happens also in the slope of the 2nd phase



They compensate each other →  $DOUT$  is independent of tolerances

2. During the 1st phase we really integrate  $V_{IN}$



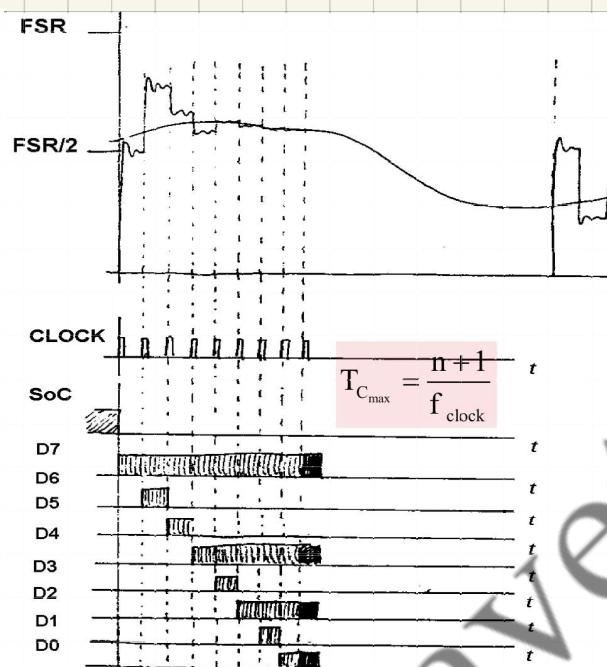
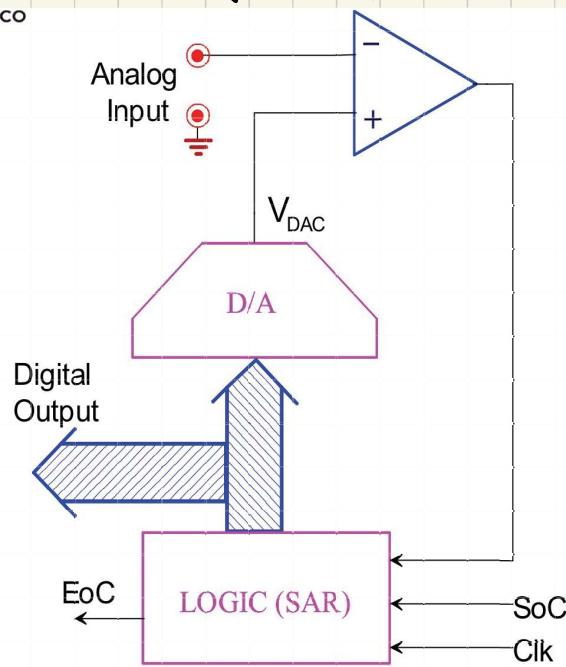
$$* T_{dist} = \frac{1}{3} T_1 \Rightarrow f_{dist} = 3 \frac{1}{T_1}$$

If the disturbance has a freq which is an integer multiple of the inverse of the integration time ( $T_1 = 2^n T_{clock}$ ) then it will be rejected

↳ GOOD ADVANTAGE ☺ → REJECTION OF DISTURBANCE HARMONICS

# SAR-ADC (SUCCESSIVE APPROXIMATION REGISTER ADC)

It's very similar to the staircase ADC, so only when  $V_{DAC}$  reaches  $V_{in}$  the conversion gets stopped.



Components:  
 1 comparator  
 1 DAC  
 1 sequential SAR

ADV: here we do not use a standard counter, but the idea is to proceed w/ a binary approach  $\rightarrow$  BINARY SEARCH

The sequential SAR logic network begins by asserting the MSB of the digital code and comparing the corresponding analog value (that is  $FSR/2$ ), generated by the internal DAC, w/ the voltage at the input  $V_{in}$ .

- if  $V_{in} > V_{DAC}$   $\rightarrow$  The level of the bit is kept
- if  $V_{in} < V_{DAC}$   $\rightarrow$  The bit is reset to 0

So, at every clock stroke, the SAR sets a bit at a time and decides whether to keep it that way or to reset the level, until the LSB is reached.

ADVANTAGE: A conversion requires only  $(n+1)$  clock pulses instead of  $2^n$  of the ADCs seen so far:

$$T_{Cmax} = \frac{(n+1)}{f_{clock}} = (n+1) T_{clock}$$

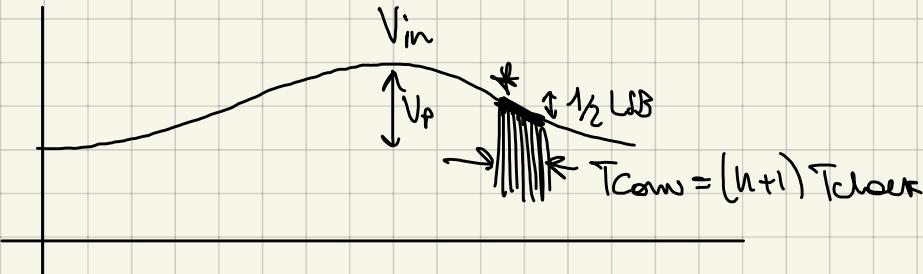
ISSUE: in order for the conversion to be successful, it's important that  $V_{in}$  stays constant w/in 1/2 LSB during the entire search for the correct code.

$$f_{in,MAX} \leq \frac{f_{clock}}{2\pi \cdot 2^n \cdot (n+1)}$$

→ very limiting 😞

↳ if the input signal is too variable during the conversion time this would lead to an error

## Demonstration:



$$*\left| \frac{dV}{dt} \right|_{\text{max}} = 2\pi f_{\text{MAX}} V_{p,\text{MAX}} \leq \frac{1/2 \text{ LSB}}{(n+1) T_{\text{clock}}}$$

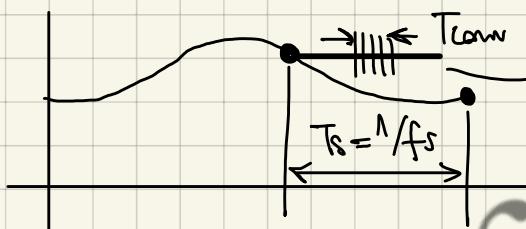
$$\Rightarrow f_{\text{MAX}} \leq \frac{1/2 \text{ LSB}}{(n+1) 2\pi V_{p,\text{MAX}}} f_{\text{clock}} = \frac{\cancel{\times} (f_{\text{clock}} / 2^n)}{(n+1) 2\pi (\cancel{f_{\text{clock}}} / 2)} f_{\text{clock}}$$

$$= \frac{f_{\text{clock}}}{2\pi 2^n (n+1)}$$

if  $f_{\text{clock}} = 100 \text{ MHz}$  and  $n = 10$   $\rightarrow f_{\text{MAX}} \leq \frac{100 \text{ MHz}}{2\pi \cdot 1024 \cdot 11} \approx 1.6 \text{ kHz}$  ☹

We obtain this awful result b/c we do not use a S&H (The signal may change, but not that much)

Using S&H:

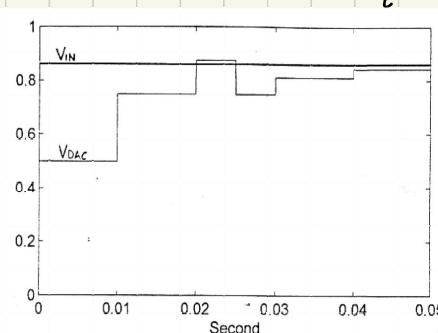
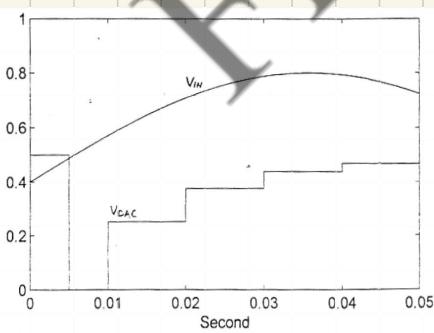


now, thanks to the S&H, the signal remains constant

we do not have the former limitation anymore

but in this case, anyway  $f_{\text{MAX}} \leq \frac{1}{2} f_s = \frac{1}{2} \frac{f_{\text{clock}}}{(n+1)}$  w/ S&H

so w/  $f_{\text{clock}} = 100 \text{ MHz}$ ,  $n = 10$   $\rightarrow f_{\text{MAX}} \leq \frac{100 \text{ M}}{2 \cdot 11} \approx 4.5 \text{ MHz}$  ☺



With NO S&H at the input:

$$f_{\text{in,max}} \leq \frac{f_{\text{clock}}}{2\pi \cdot 2^n \cdot (n+1)}$$

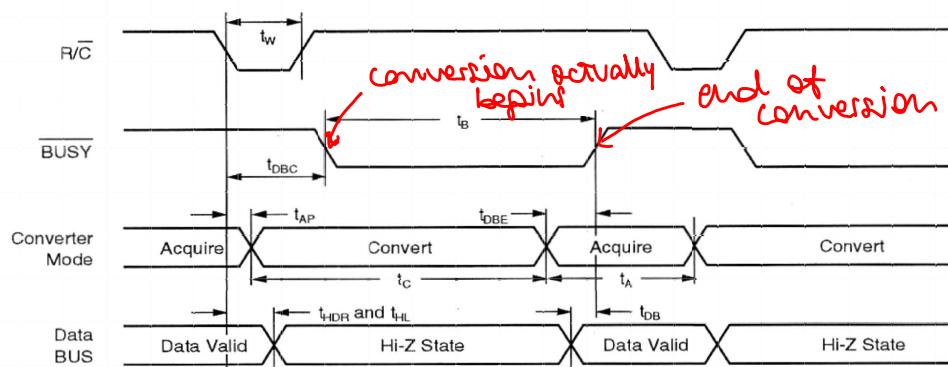
with S&H at the input:

$$f_{\text{in,max}} \leq \frac{f_{\text{sampling}}}{2} = \frac{f_{\text{clock}}}{2 \cdot (n+1)}$$

## TIMINGS:

### ① PARALLEL NON-Pipelined ADC (SINGLE SHOT)

single-shot ADCs:



$$R/\bar{C} = S_{OL}$$

- $R/\bar{C} = 1 \rightarrow$  ready phase
- The request for a new conversion is done by lowering  $R/\bar{C}$
- The SRH inside the ADC open the switch that connects  $A_{in}$  to the capacitor inside the ADC, so the SRH moves from the **ACQUISITION PHASE** to the **SAMPLING PHASE**, during which ADC converts  $A_{in}$  stored during the ready phase
- The result of the conversion is started to the output data bus
- Once the output data has been applied, the internal electronics of the ADC will inform the MCU that the conversion is completed which set **BUSY** from 0 to 1

Notice:

- The conversion actually begins only after a time  $t_{DBC}$  starting from the falling edge of  $R/\bar{C}$  and **BUSY** is set low
- In the meanwhile after  $t_{AP}$  ( $< t_{DBC}$ ) the SRH inside the ADC switch from the acquisition to the conversion phase, so that it's ready when the conversion can effectively start
- From the end of the conversion, it may take  $t_{DBE}$  before the ADC communicates the conversion is finished. At that point **BUSY** is set to H
- The effective conversion lasts for a time  $t_c$  = INTRINSIC CONVERSION TIME

$$\Rightarrow T_{conv, total} = t_{DBC} + t_p = t_{AP} + t_c + t_{DBE} > t_c$$

$$\Rightarrow \text{Throughput} = 1/T_{conv, tot}$$

What does single-shot ADC mean?

It means that for each pulse we have a single conversion

We'll see that some ADCs have a much more complex architecture: a **Pipelined** one

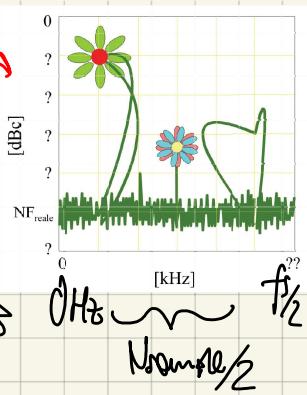
↓  
 it will may take a long time to get DATA VALID, but the advantage of the pipelined config. is that you can provide more pulses at a time

⇒ The THROUGHPUT is much higher!!! 😊

## EX 2

DAC  $n=16$  FSR = 5V

Power w/in each bin →



Def:  $f_s = 2 \text{ Msps}$  of sinusoidal signal @  $f_c = 400 \text{ kHz}$   
 $\text{w/ } V_p = 200 \text{ mV}$

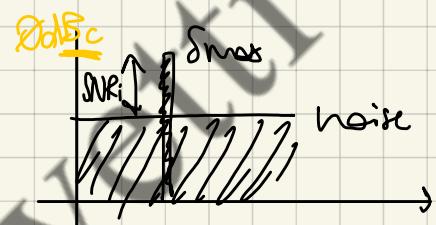
The noise is overimposed to the signal and lowers the SNR by 20dB

$N_{\text{samples}} = 512 \text{ k}$  for FFT

A) Compute SNRideal, SNRreal, ENOB and NFreal

$$\text{SNR}_{\text{ideal}} = \frac{S_{\text{max}}^2}{N_{\text{min}}^2 \text{ dB}} = \frac{(V_p/\sqrt{2})^2}{(\text{LSB}/\sqrt{12})^2 \text{ dB}} = \frac{(FSR/2\sqrt{2})^2}{(\text{LSB}/\sqrt{12})^2 \text{ dB}} = 6.02n + 1.76 = 9.8 \text{ dB}$$

↳ Quantization error



normalization →  $S_{\text{max}} = QdBC$

$$\text{SNR}_{\text{ideal, dB}} = S_{\text{max, dB}}^2 - N_{\text{min, dB}}$$

$$N_{\text{min}} = N_{\text{quant}} = \left( \frac{\text{LSB}}{\sqrt{12}} \right)^2 = QdBC - \text{SNR}_{\text{ideal}} = -9.8 \text{ dBc}$$

$$N_{\text{samples}} = 512 \text{ k}$$

$$f_s = 2 \text{ Msps}$$

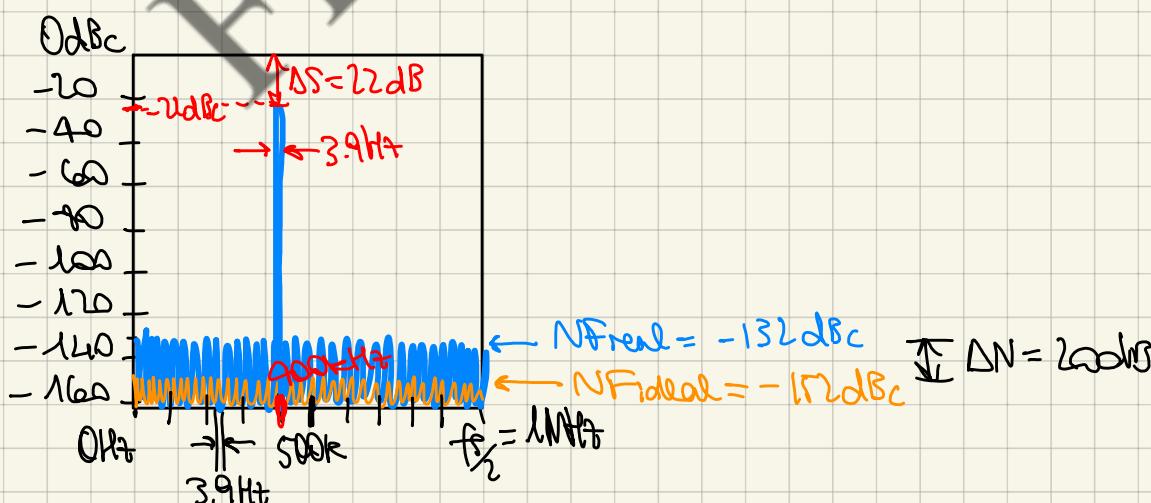
$$\rightarrow \text{bin-width} = \frac{f_s}{N_{\text{samples}}} = \frac{f_s/2}{N_{\text{samples}}/2} = \frac{2M}{512 \text{ k}} = 3.9 \text{ Hz}$$

$$\text{NF}_{\text{ideal}} = \frac{N_{\text{min}}}{N_{\text{samples}}/2} = -9.8 \text{ dBc} - 10 \log_{10} \left( \frac{N_{\text{samples}}}{2} \right) = -9.8 \text{ dBc} - 54 \text{ dB} = -152 \text{ dBc}$$

This is the power of each histogram that composes my NF

$$N_{\text{real}} = N_{\text{min}} + \Delta N = -9.8 \text{ dBc} + 20 \text{ dB} = -7.8 \text{ dBc}$$

$$\rightarrow \text{NF}_{\text{real}} = \text{NF}_{\text{ideal}} + \Delta N = -152 \text{ dBc} + 20 \text{ dB} = -132 \text{ dBc}$$



$S_{\text{real}} = 200 \text{ mV}$  and not  $S_{\text{max}} = FSR/2 = 2.5 \text{ V}$

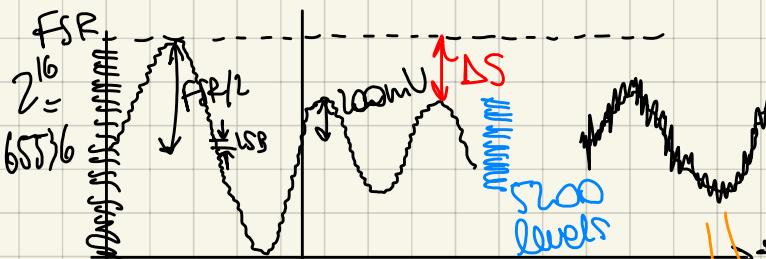
$$\Rightarrow S_{\text{real}}^2 = \left( \frac{200mV}{\sqrt{2}} \right)^2 = \dots = S_{\text{max}}^2 - \Delta S$$

↓  
ΔdBc

where  $\Delta S = \frac{\text{FSR}/2}{\sqrt{P}} = \frac{2.5V}{\sqrt{P}} = 12.5 \equiv 20 \log_{10}(12.5) = 22 \text{ dB}$   
 but it's a ratio between amplitudes

$$\Rightarrow S_{\text{real}}^2 = S_{\text{max}}^2 - \Delta S = \text{ΔdBc} - 22 \text{ dB} = -22 \text{ dBc} \quad (@ 400 \text{ kHz})$$

$$\text{SNR}_{\text{real}} = \text{SNR}_{\text{ideal}} - \Delta S - \Delta N = 98 \text{ dB} - 22 \text{ dB} - 20 \text{ dB} = 56 \text{ dB}$$



$$200mV : 2.5V = x : 100$$

$$x = \frac{200mV \cdot 100}{2.5} = \frac{20}{2.5} = 8.$$

Ideal      Theoretical  
 $\text{SNR}_{\text{ideal}} = 98 \text{ dB}$        $98 \text{ dB} - 22 \text{ dB} = 76 \text{ dB}$

real (w/ extra noise  $\Delta N$ )  
 $76 \text{ dB} - 20 \text{ dB} = 56 \text{ dB}$

$$65536 \cdot 0.09 \approx 5120 \text{ levels}$$

$$76 \text{ dB} - 20 \text{ dB} = 56 \text{ dB}$$

$$\left. \begin{array}{l} 6.02 \text{ ENOB} + 1.76 = \text{SNR}_{\text{ideal}} \\ \text{equivalent ADC} \end{array} \right.$$

$$\text{SNR}_{\text{ideal equivalent ADC}} = \frac{\text{SNR}_{\text{real actual ADC}}}{10^{56/10}}$$

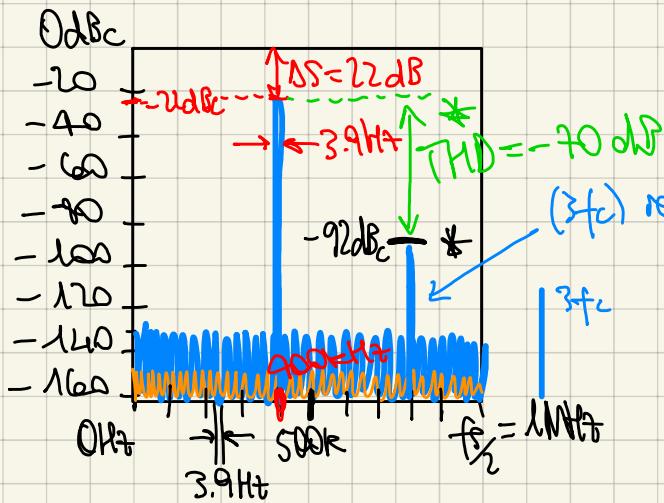
$$\Rightarrow \text{ENOB} = \frac{\text{SNR}_{\text{real}} - 1.76}{6.02} = \frac{56 \text{ dB} - 1.76}{6.02} = (9 \text{ bits})$$

The quality I end up w/ is equal to the quality I'd have obtained using an ideal 9 bit ADC

- ⑧ Draw the spectrum, properly quoted in [Hz] and [dBc], adding also an harmonic @ 3fc due to a THD = -70 dB

THD = TOTAL HARMONIC DISTORTION

$3fc = 1.2 \text{ MHz}$ , but since  $f_s = 1 \text{ MHz}$  and the spectrum is symmetric around  $f_s/2$ , it means that the harmonic lies @ 300 kHz



(3fc) reflected into baseband  
What's the height of such harmonic

Worst case scenario  $\rightarrow$  THD is due to just one harmonic \* in this case

$$* -22 \text{ dBc} - 70 \text{ dB} = -92 \text{ dBc}$$

### EX3

ADC:  $n=14$  FSR = 3.3V spectrum w/ 680ms acquisition

Ⓐ Compute SNRideal, SNRtheoretical, SINAD and THD

$$f_r = 2 \cdot 30 \text{ MHz} = 60 \text{ Msps}$$

$$T_m = 680 \text{ ms}$$

$$\rightarrow N_{\text{samples}} = \frac{T_m}{T_s} = T_m \cdot f_r = 40.8 \text{ Msamples}$$

$$\text{SNRideal} = \frac{\delta_{\text{max}}^2}{N_{\text{min}}^2} \text{ dB} = 6.02 n + 1.76 = 86 \text{ dB}$$

$$\text{SNR}_T = \text{SNRideal} - DS = 86 \text{ dB} - 30 \text{ dBc} = 56 \text{ dBc}$$

$$\text{SNRreal} = \text{SNRideal} - DS - DN$$

$$N_{\text{min}} = S_{\text{max}}^2 - \text{SNRideal} = 86 \text{ dBc} - 86 \text{ dB} = -86 \text{ dBc}$$

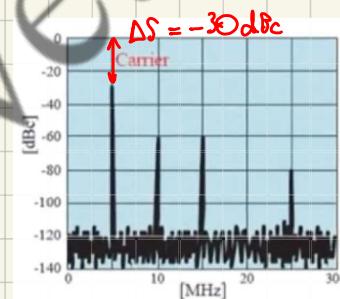
$$N_{\text{ideal}} = \frac{N_{\text{min}}}{N_{\text{samples}}/2} = -86 \text{ dBc} - 10 \log_{10} \left( \frac{N_{\text{samples}}}{2} \right) = -86 \text{ dBc} - 73 \text{ dB} = -159 \text{ dBc}$$

But from the plot we see that  $N_{\text{real}} \approx -120 \text{ dBc}$

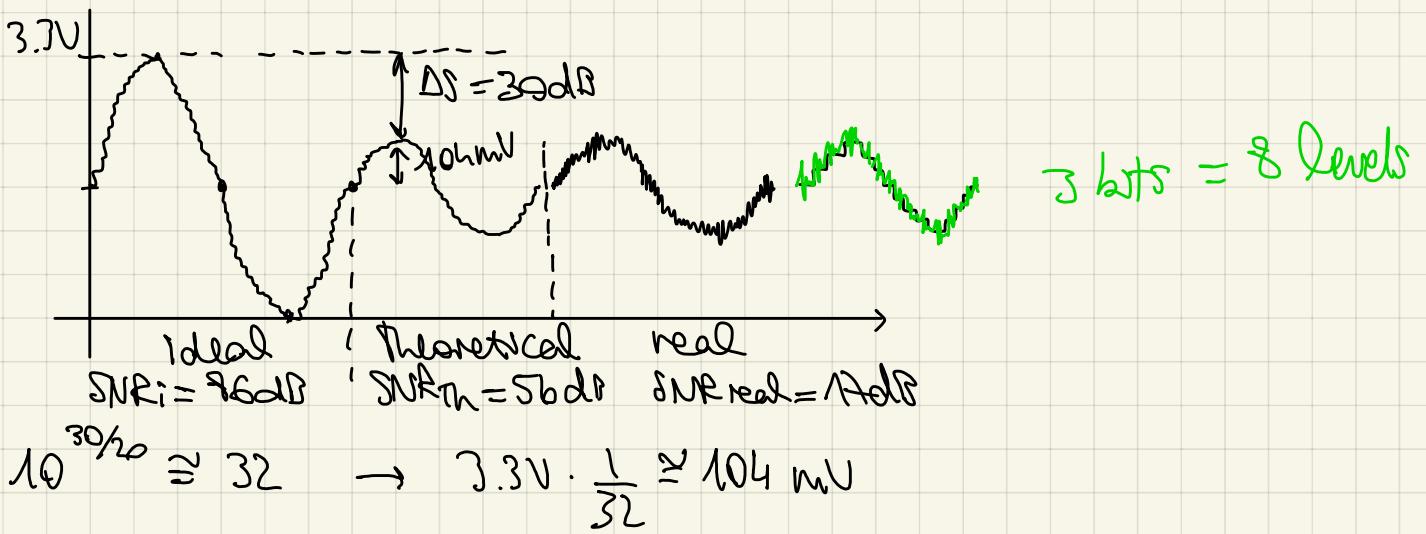
$$\Rightarrow DN = N_{\text{real}} - N_{\text{ideal}} = -120 \text{ dBc} + 159 \text{ dBc} = 39 \text{ dB}$$

$$\text{SNRreal} = 56 \text{ dBc} - 39 \text{ dB} = 17 \text{ dBc}$$

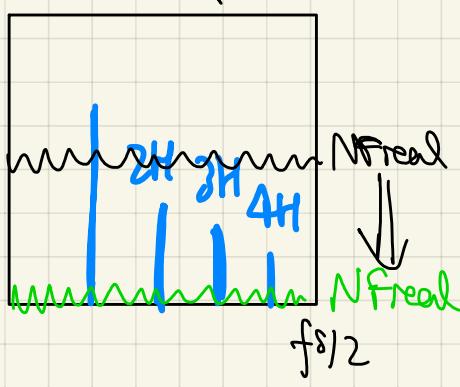
$$ENOB = \frac{\text{SNRreal} - 1.76}{6.02} = 2.5 \text{ bits} \quad (\approx) \quad = 3 \text{ bits}$$



$f_r/2$



- ⑤ In case The 6th harmonic power is  $10^6$  lower than the carrier, compute the required duration of the acquisition stream for detecting the harmonic when  $\text{SNR}=10 \text{ dB}$  over the noise floor



$$\text{NF} = \frac{N_{\text{min}}}{N_{\text{samples}}/2} \quad \text{so to decrease it let's increase } N_{\text{samples}}$$

$$N_{\text{samples}} = \frac{T_m}{T_s} = T_m f_s$$

- ⇒ • increase  $T_m$
- increase  $f_s$

if  $N=40 \text{ M} \rightarrow 400 \text{ M}$  it increases by a factor 10 which means that NF decreases by a factor 10 which corresponds to 10dB

