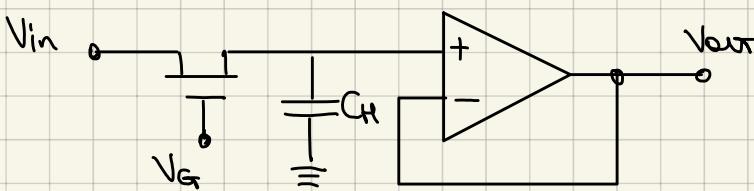
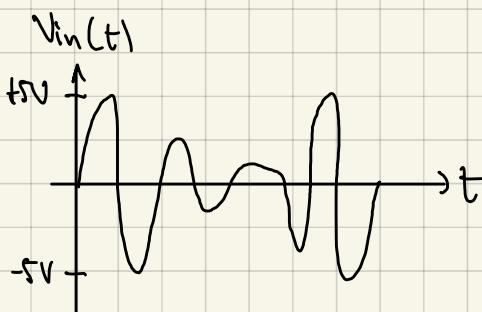


BASIC S&H CIRCUIT



in correspondence of a control signal (V_G), it samples the input voltage value and stores it (through C_H) until the next command



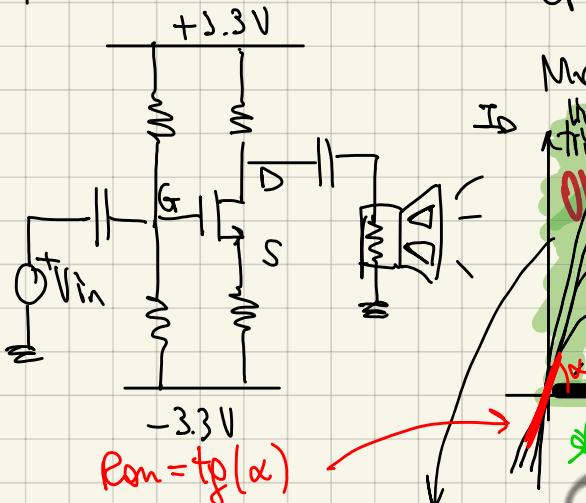
SPECS: input signal: $-5V \div +5V$ $20k\text{Hz} = \text{BW}$

$$E_{MAX} \leq 0.01\% \text{ of fSR} \Rightarrow E_{MAX} \leq \frac{1mV}{10V}$$

$$f_S = 100\text{kHz}$$

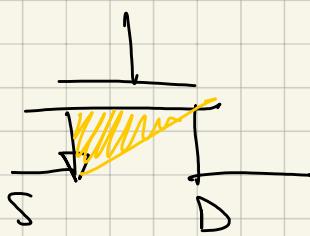
Opamp: $A_0 = 100dB$ $I_{bias} = 50\mu A$

Mosfet: $V_T = 2V$, $R_{ON} = 50\Omega$ $C_{GS} = 0.5pF$
 $C_{DS} = 0.1pF$



SATURATION

$$I_D = \frac{1}{2} \mu n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 (1 + \gamma V_D)$$



Pinch-off

channel @ S
no channel @ D

We want this condition when the switch is close

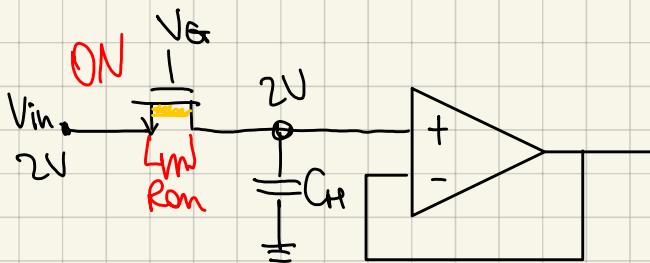
Full-channel

$R_{ON} \rightarrow \text{very small}$

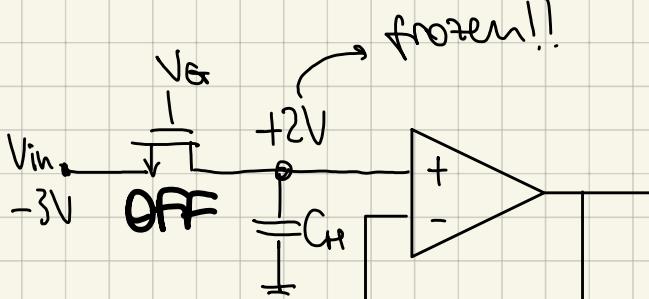
when the switch is open, we want the mosfet to operate in OFF condition

* we'll work just in these two conditions

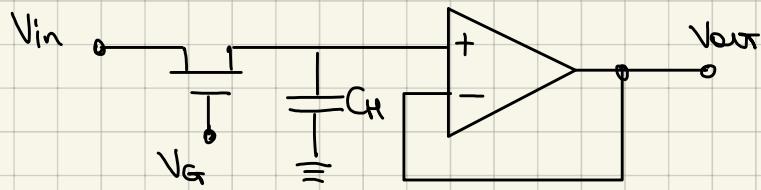
• SAMPLING PHASE



• HOLD / FREEZE PHASE



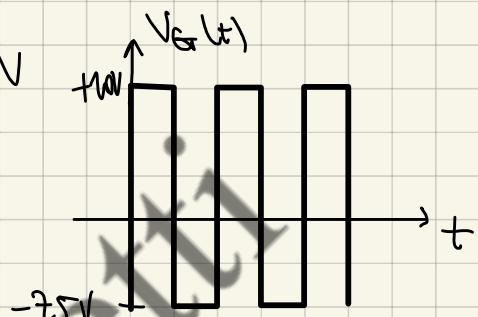
$$V_{in} = -5V \div +5V$$



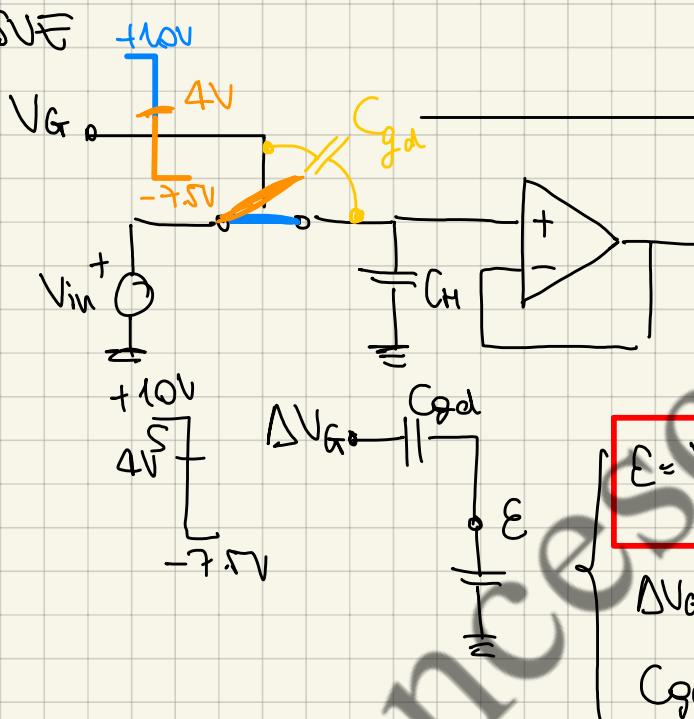
SAMPLING: if $V_{in} = +5V \rightarrow V_{in,samp} > V_{in,max} + V_T = +5V + 2V = +7V$

HOUD: if $V_{in} = -5V \rightarrow V_{in,hold} < V_{in,min} + V_T = -5V + 2V = -3V$

To be sure let's choose $\begin{cases} V_{G, sampling} = +10V \\ V_{G, hold} = -7.5V \end{cases}$



ISSUE



Due to this parasitic cap. we have an issue

The voltage on C_H wants to stay @ 2V, when the switch opens, but due to C_{gd} the voltage changes

$$\boxed{E = V_{injection} = \Delta V_G \frac{C_{gd}}{C_{gd} + C_H} \leq 1mV}$$

$$\Delta V_G = \Delta V_{G, max} = 17.5V$$

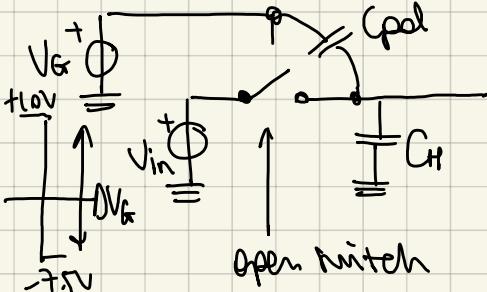
$$C_{gd} =$$

$$\Downarrow$$

$$C_H \geq 9nF$$

ES 10 - S&H CIRCUITS (1)

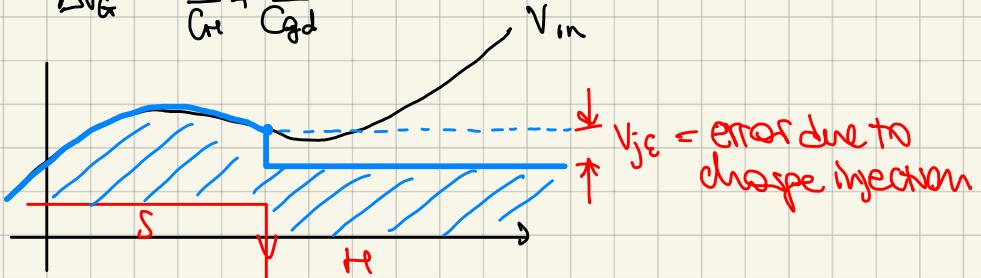
03/11/2021



$$C = \frac{Q}{V}$$

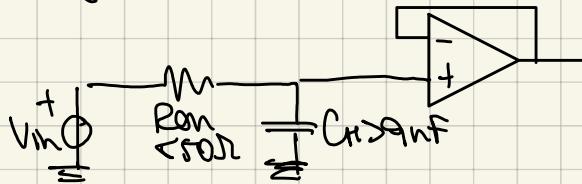
$$\frac{\Delta Q}{\Delta V_G} = \frac{1}{\frac{1}{C_H} + \frac{1}{C_{gd}}}$$

CHARGE PUMPING EFFECT



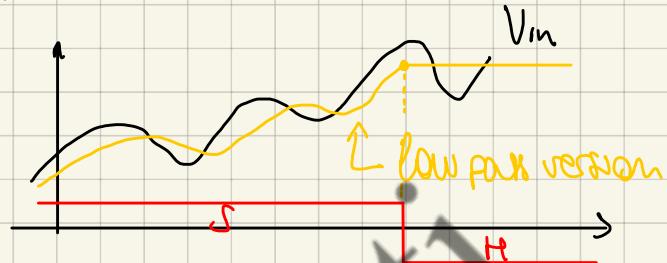
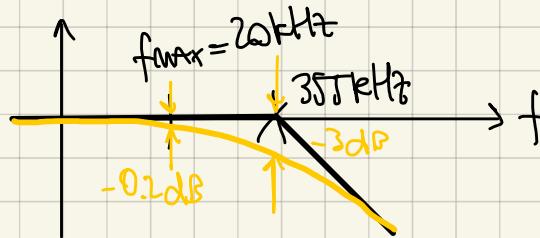
$$V_{JE} = \Delta V_G \frac{C_{GD}}{C_{GD} + C_T} \rightarrow \text{from which we can compute the value of } C_T$$

Sampling:



During the sampling the S/H behaves like a LPF

$$f_p = \frac{1}{2\pi R_{in} C_T} = 35\text{ kHz}$$



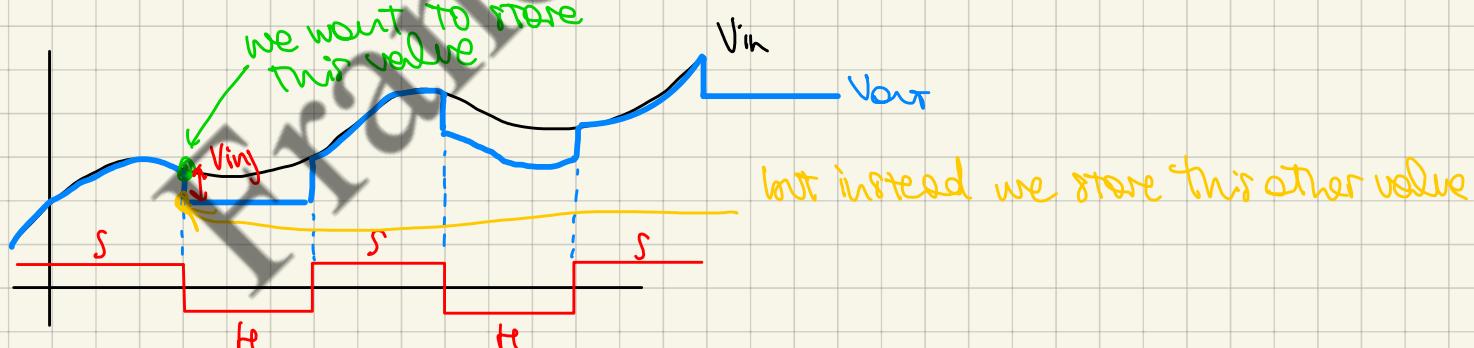
if $V_{in} = 8V \rightarrow 3V + V_t \leq V_G \leq +10V \Rightarrow$ the transistor is ON \rightarrow sampling
 \rightarrow no charge injection

for $-7.5V \leq V_G \leq 5V \rightarrow$ the transistor is OFF \rightarrow holding
 \rightarrow There's charge injection

\Rightarrow This means that charge injection is not a constant error: if V_{in} varies also ΔV_G varies b/c ΔV_G depends on $(V_{in} + V_t)$

$$\Delta V_{G,\min} = V_{in,\min} + V_t - V_{G,\text{hold}} = -5V + 2V - (-7.5V) = +4.5V \Rightarrow V_{JE} = 250\mu V$$

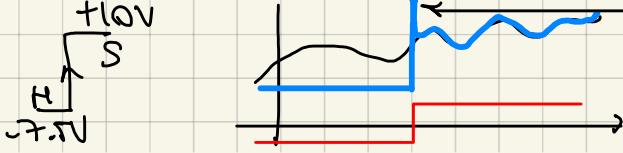
$$\Delta V_{G,\max} = V_{in,\max} + V_t - V_{G,\text{hold}} = +5V + 2V - (-7.5V) = +14.5V \Rightarrow V_{JE} = 906\mu V$$



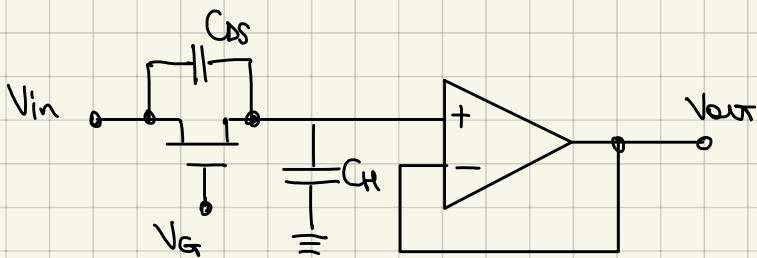
This is bad b/c if it were a constant error we could subtract it, considering it as an offset

it's called APERTURE-INDUCED NON LINEARITY b/c it's about the aperture: when we open the switch and we freeze the value

We also have a closure-induced charge injection but it has no effects:



2nd ERROR : SIGNAL-FEEDTHROUGH



$$V_{\text{feedthrough}} = \Delta V_{\text{IN}} \frac{C_{\text{ds}}}{C_{\text{ds}} + C_{\text{th}}} \Rightarrow \text{w/ } \Delta V_{\text{IN}, \text{max}} = 10\text{V} \rightarrow V_{\text{feedthrough}} = 1.1 \mu\text{V}$$

This is \downarrow $< 1\text{mV}$ but it sums up to the other error and

We must minimize the overall error \Rightarrow The higher C_{th} , the lower $V_{\text{injection}}$ and $V_{\text{feedthrough}}$ are !!

3rd ERROR: DROP

\hookrightarrow The voltage stored on C_{th} changes over time b/c there is a leakage current which may be caused by:

- bias current of the OpAmp
- leakage through the MOSFET
- leakage through the cap
- or any other leakage

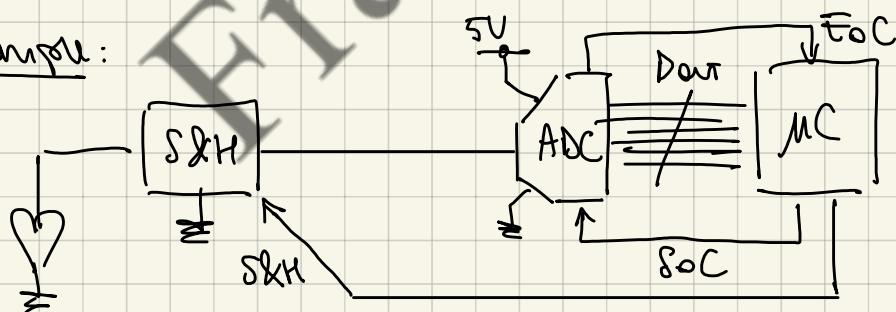
$$\Rightarrow \Delta V_c = \frac{\text{Leakage}}{C_{\text{th}}} \cdot t$$

w/ $\text{Leakage} = 100\text{fA}$ and $C_{\text{th}} = 9\text{nF} \Rightarrow$ The stored voltage will drop by 1mV/s

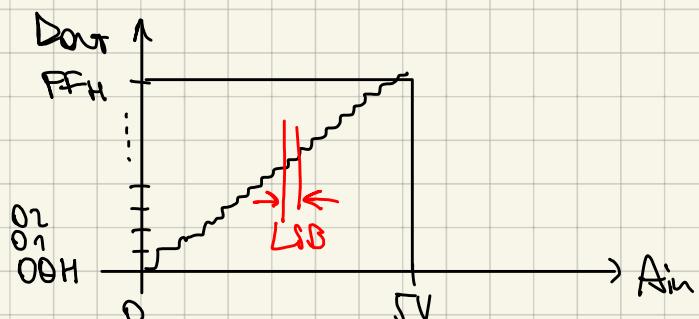
\Rightarrow w/ $f_s = 100\text{kHz} \Rightarrow T = \frac{1}{0.1\text{MHz}} = 10\text{ns} \Rightarrow \Delta V_c = 0.1\text{ }\mu\text{V}$ every 10ns hold duration

Is 1mV/s big or not? \rightarrow It depends on the following electronics

example:



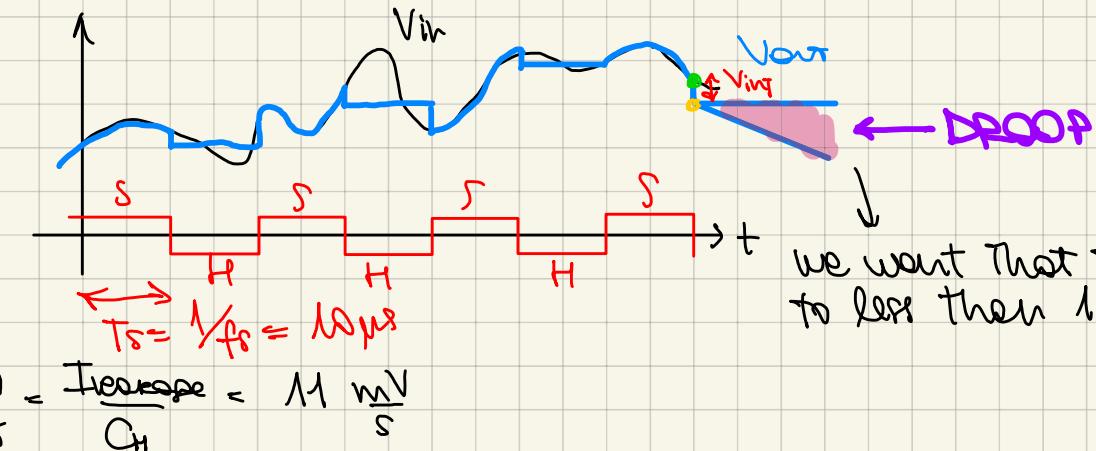
ADC:



$$\text{LSB} = \frac{F_{\text{SR}}}{2^n} = \frac{5\text{V}}{2^8} = 19\text{mV}$$

$$n = \# \text{ bits} = 8$$

This means that when we consider droop we want that it is less than 1 LSB



we want that this droop is limited to less than 1 LSB

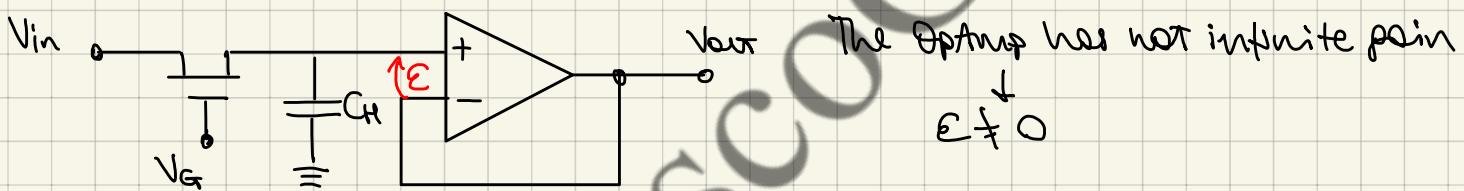
$$dt = \frac{dV}{I_{\text{load}}/C_H} = \frac{1 \text{ LSB}}{11 \text{ mV/s}} = \frac{19 \text{ mV}}{11 \text{ mV/s}} = 1.7 \text{ s} > T_{\text{hold}}$$

MAXIMUM DURATION OF OUR HOLD PHASE

⇒ This means that the cap. can stay open for 1.7s → if $T_{\text{hold}} > 1.7s$ the discharge across the cap becomes too huge

WORST-CASE SCENARIO

4TH ERROR: BUFFER-INDUCED NON-LINEARITY

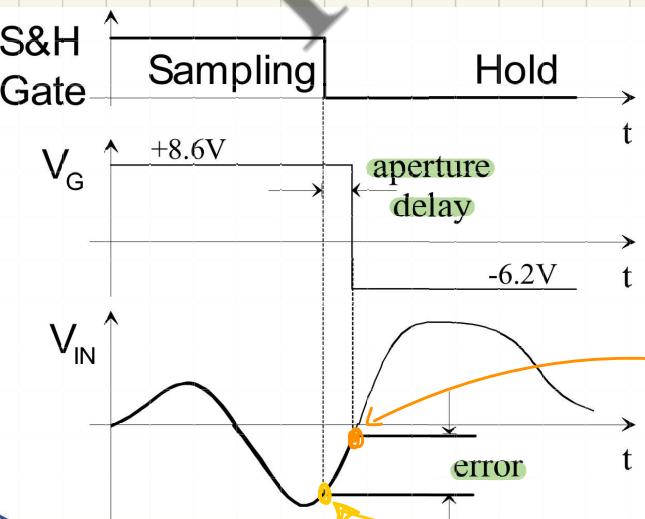


$$V_{\text{out}} = A_O \cdot \epsilon, \text{ so if we want } \epsilon < 1 \text{ mV} \Rightarrow \epsilon = \frac{V_{\text{out}}}{A_O} < 1 \text{ mV}$$

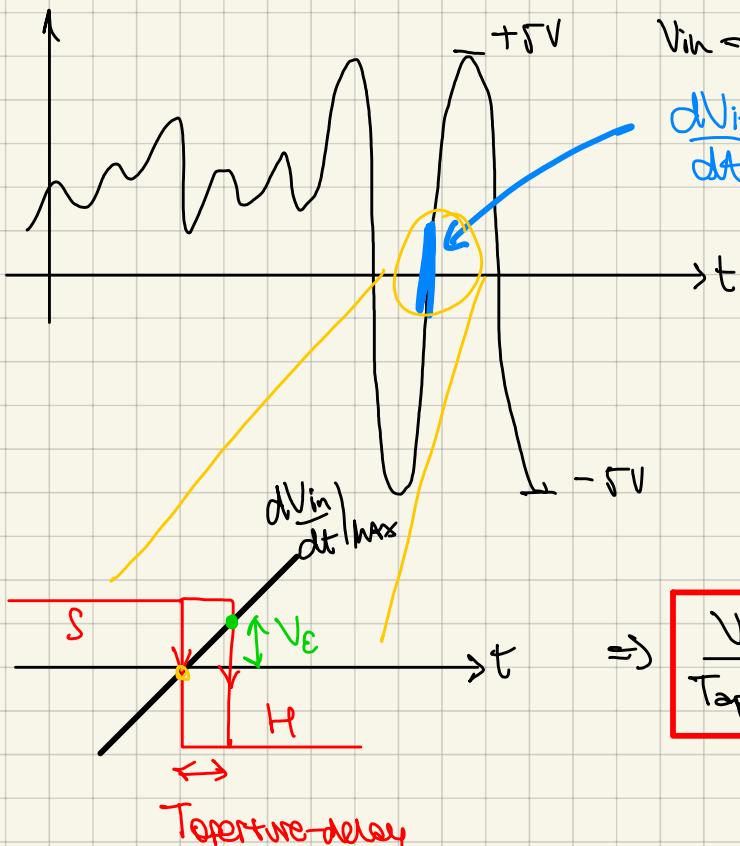
$$\Rightarrow A_O > \frac{V_{\text{out}, \text{max}}}{\epsilon} \Rightarrow A_{O, \text{min}} = \frac{V_{\text{out}, \text{max}}}{\epsilon}$$

$$\text{if } V_{\text{out}, \text{max}} = 5 \text{ V and } \epsilon = 1 \text{ mV} \Rightarrow A_{O, \text{min}} = 5000 = 74 \text{ dB}$$

5TH ERROR: APERTURE DELAY TIME



Due to the aperture delay we store this value instead of this one



$$V_{in} = V_p \sin(2\pi f t)$$

$$\left| \frac{dV_{in}}{dt} \right|_{max} = V_{p,max} \cos(2\pi f_{max} t) \cdot 2\pi f_{max}$$

$$= V_{p,max} \cdot 1 \cdot 2\pi f_{max}$$

$$\left| \frac{dV_{in}}{dt} \right|_{max} = 2\pi f_{max} V_{p,max}$$

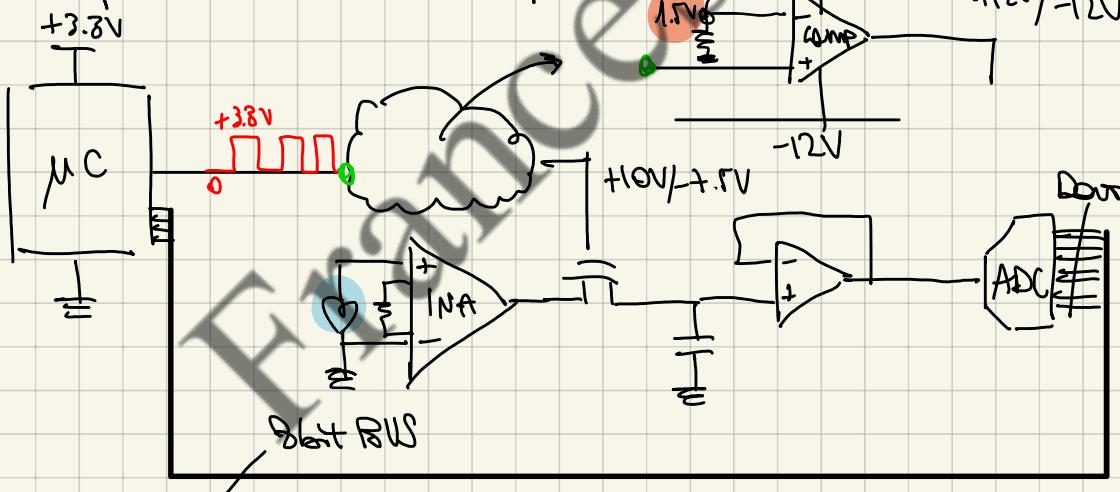
$$\frac{V_E}{\text{Tapering}} = \left| \frac{dV_{in}}{dt} \right|_{max}$$

if $Tape = 1ns \Rightarrow V_E = \Delta V_{\text{Tapering}} = \left| \frac{dV_{in}}{dt} \right|_{max}$ Tapering = $2\pi f_{max} V_{p,max}$

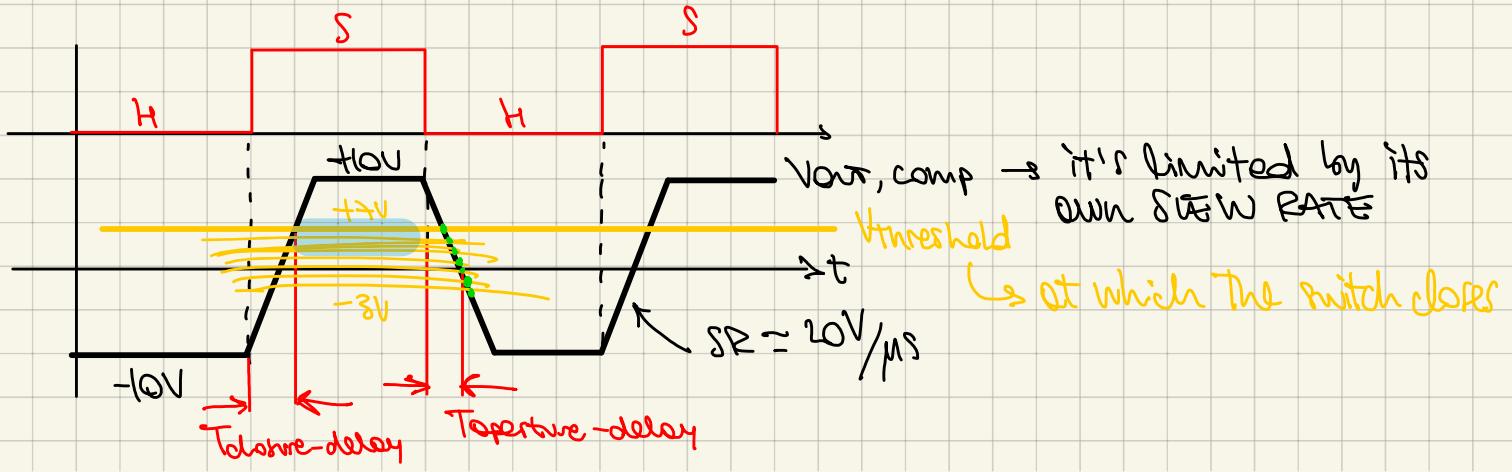
$$= 2\pi \cdot 20MHz \cdot 5V \cdot 1ns = 0.63mV$$

↓ absolutely not negligible ☺

Example:



even if we use a $V_{out,H}$ which is higher than needed and a $V_{out,L}$ that is lower than needed it is okay



if $V_{threshold}$ is constant \Rightarrow $T_{aperture}$ is constant

But the problem, as we have already seen, is that $V_{threshold}$ is not constant

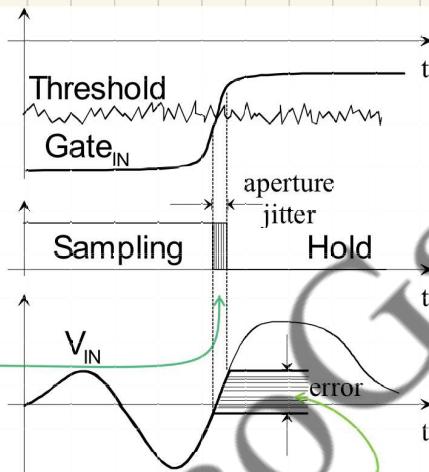
if $V_{in} = +5V \div -5V$ and $V_T = 2V \Rightarrow V_{threshold} = +7V \div -3V$

so we can say that the aperture delay is given by the sum of two terms: an average $T_{aperture}$ ($\bar{T}_{aperture}$) and $T_{aperture,jitter}$

↓
when $V_{threshold}$ is in the middle for instance

↓
this fluctuation is not predictable but we don't know what V_{in} will be!

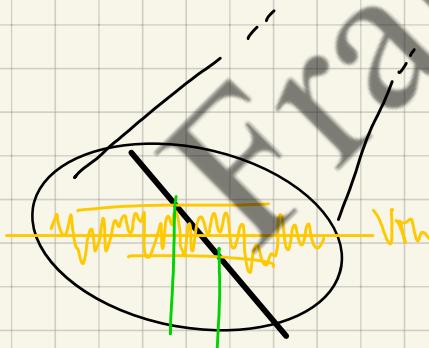
6th ERROR: APERTURE TIME JITTER



$$t_{aperture} = \frac{\sigma_{threshold}}{\left. \frac{dV_{command}}{dt} \right|_{\min}} = \frac{10mV}{\frac{5V}{10ns}} = 20ps$$

$$\sigma_{aperture} = \left. \frac{dV_{in}}{dt} \right|_{\max} \cdot t_{aperture} = 2\pi \cdot f_{\max} \cdot V_{in,\max} \cdot t_{aperture} = 13\mu V$$

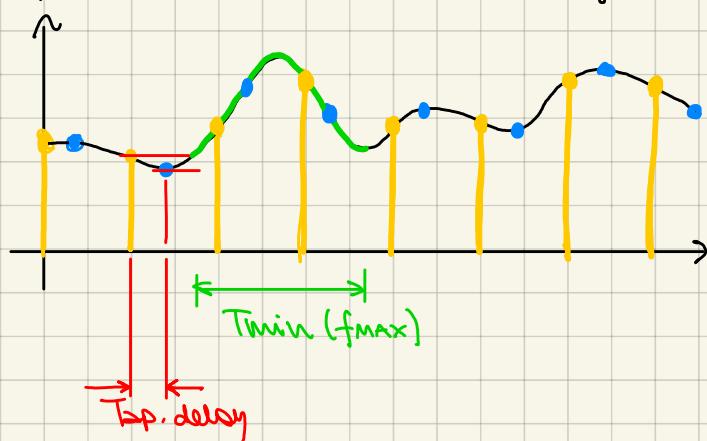
so one possible cause of $T_{aperture,jitter}$ is the SLOW RATE of $V_{in,comp}$
furthermore, we have another error:



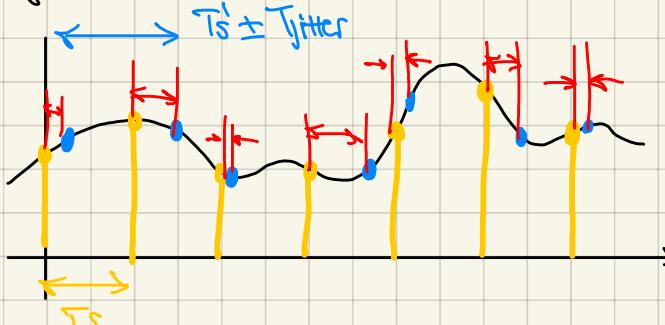
V_{in} → due to the variation of the comparator input

$$\frac{10V}{T_{jitter}} = SR = 20V/\mu s \rightarrow T_{jitter} = \frac{10V}{20V/\mu s} = \frac{1\mu s}{2} = 0.5\mu s \text{ absolutely not negligible}$$

Let's go back to basics of sampling

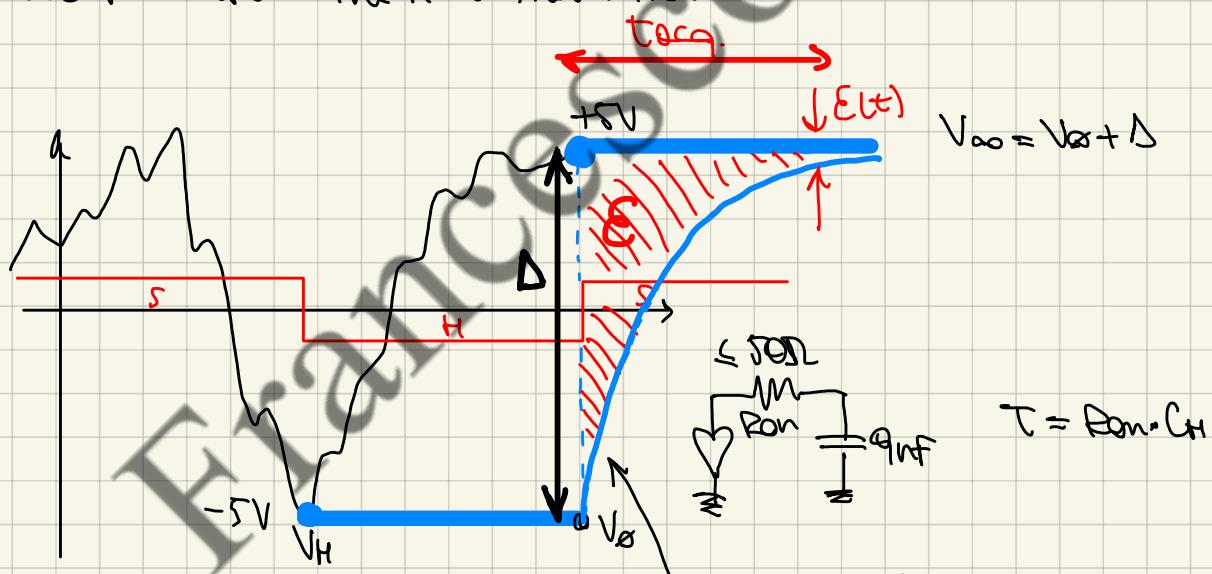


T_ap. delay is an issue depending on the application, while jitter is always a big issue



ACQUISITION TIME

So far we have considered all the errors concerning the S → H transition, now we have to consider the H → S transition



$$V_{out} = \Delta \left(1 - e^{-t/T}\right) + V_\infty$$

$$\text{full-range} = 10V$$

$$\epsilon = V_{out}(t) - V_\infty = \Delta e^{-t/T}$$

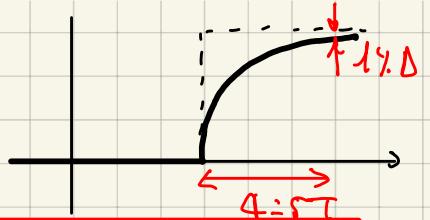
$$\epsilon < \frac{1}{2} LSS = \frac{1}{2} \frac{FSR}{2^n} = \frac{FSR}{2^{n+1}}$$

$$\Rightarrow t_{acq} \geq T \cdot \ln \left(\frac{\Delta}{\epsilon} \right)$$

ACQUISITION TIME

If the exp. charge discharge after $(4 \div 5)\tau$

$$\Rightarrow \ln\left(\frac{D}{E}\right) = 4 : 5 \rightarrow \frac{D}{E} = 100 \rightarrow E = 1\% \cdot D$$



$$t_{eq} \geq \tau \ln \frac{D}{E} = \tau \ln \frac{f_{SR}}{\frac{1}{2^n} f_{SR}} = \tau \ln (2^{n+1}) = \tau(n+1) \ln 2 = 0.7 \cdot \tau(n+1)$$

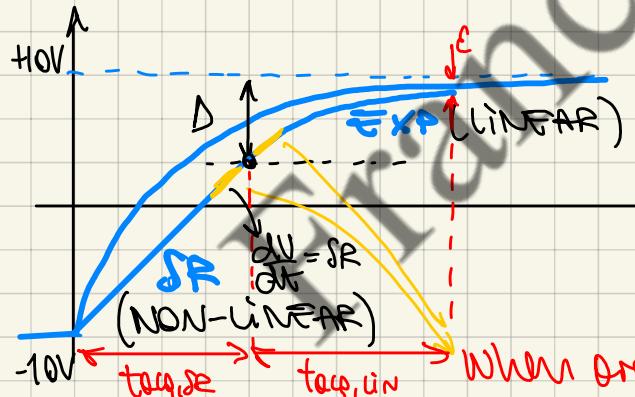
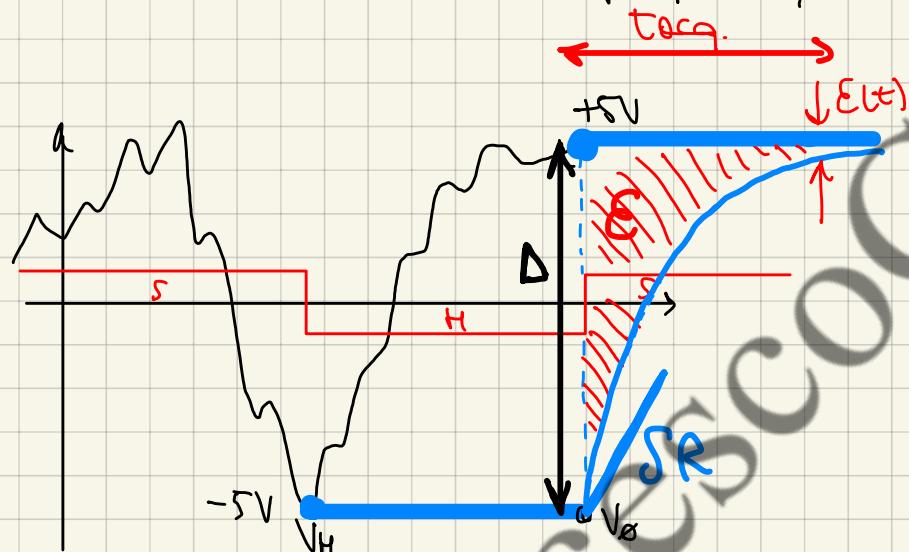
if $f_{SR} = 5V$ and $n=16$ bits $\rightarrow t_{eq} \geq 12\tau$

$$LSB = \frac{f_{SR}}{2^n} = \frac{5V}{2^{16}} = 76\mu V \rightarrow \text{if we want to have an error less than } 38\mu V \quad (E < \frac{1}{2} LSB) \text{ we have to wait } 12\tau$$

t_{eq} = minimum duration of our sampling phase

$$T_{amp} \geq t_{eq}$$

There's another issue \rightarrow our Optamp may move only W & limited SR



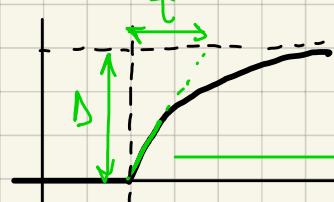
• circuit NON-LINEAR

↓
its transition is a straight line

• circuit is LINEAR

↓
its transition is an exponential

When are These slopes equal?



$$\left. \frac{dV}{dt} \right|_{max, exp} = \frac{\Delta}{T} \quad \text{max slope of an exponential increase}$$

if we know $T = R_{on} + C_L = 50\Omega \cdot 9nF = 450\text{ns}$ and $SR = 20V/\mu s$

$$\frac{dV}{dt} = SR = \left. \frac{dV}{dt} \right|_{max, exp} = \frac{\Delta}{T} \Rightarrow \boxed{\Delta = SR \cdot T} = \frac{20V}{\mu s} \cdot 0.45\mu s = 9V$$

This means that:

$$\Rightarrow 10V - \Delta : \text{performed SR limited} \rightarrow \text{torq,SR} = \frac{10V - \Delta}{SR}$$

$$\Delta : \text{performed LINEARLY} \rightarrow \text{torq,Lin} = T \ln\left(\frac{\Delta}{E}\right)$$

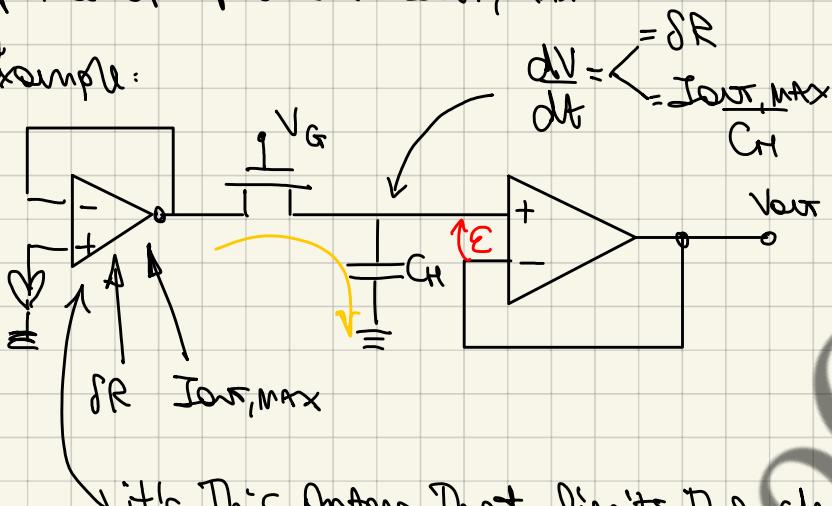
$$\left. \begin{array}{l} \text{OVERALL ACQ. TIME} \\ \text{torq} = \text{torq,SR} + \text{torq,Lin} \end{array} \right\}$$

So we have 2 transitions: The 1st one limited by the SR of the Opamp and the 2nd one which is linear (exponential curve)

BUT:

Obviously torq,SR can be given by the SR of the Opamp or by the limitation of the Opamp due to $I_{out, max}$.

Example:



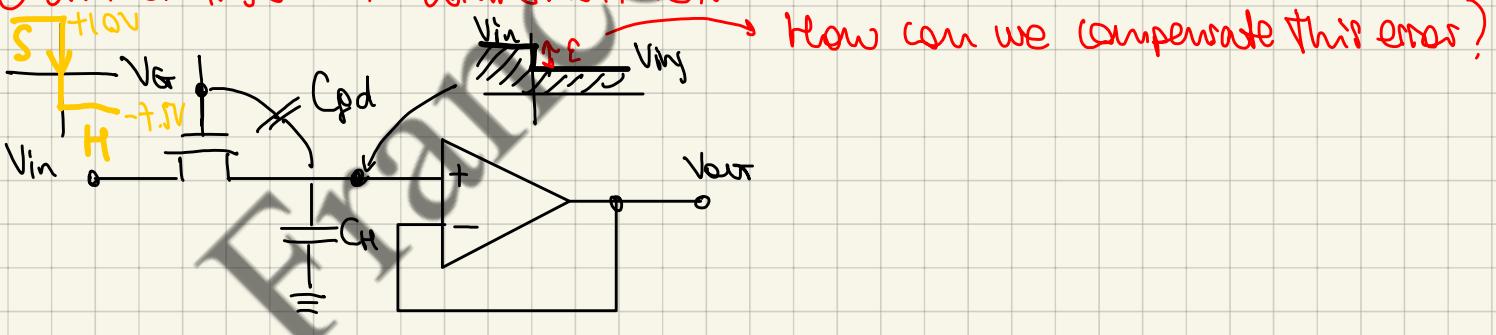
\Rightarrow We have to check which is the most limiting factor

it's this Opamp that limits the charging

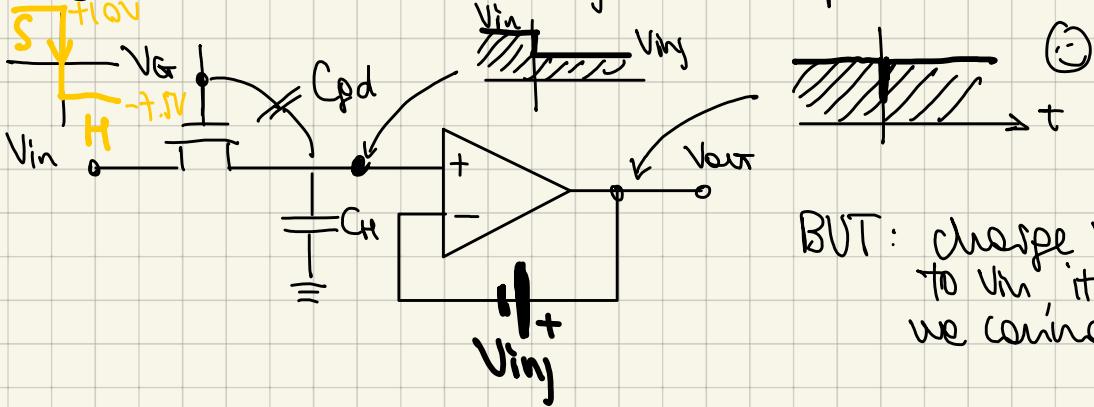
ADVANCED S&H CIRCUITS

Now we would like to solve some issues of the simple S&H circuit

① CHARGE INJECTION COMPENSATION

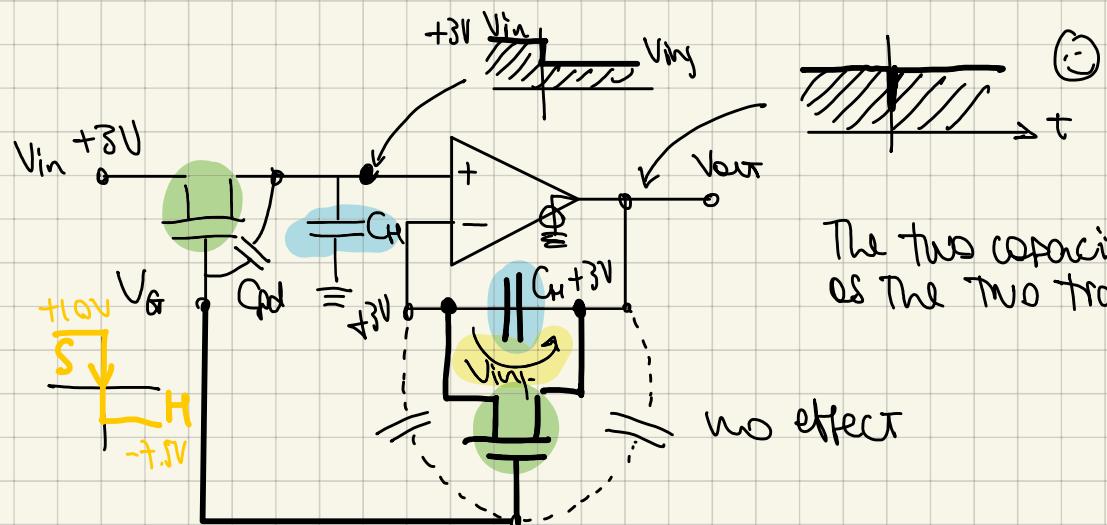


SOL ①: we can add a battery in the FB path whose value is equal to V_{inj}



BUT: charge injection varies according to V_{in} , it's a dynamic error so we cannot use a battery

SOL. ②: Let's use a capacitor instead of a battery



The two capacitors are equal as well as the two transistors

The two transistors are controlled by the same V_g , so they open at the same time. They both experience charge injection, but they compensate each other.

Previously we selected $C_m = 9\text{nF}$ to minimize charge injection, but now since we have compensated it, we can choose a lower value for C_m and in this way we:

- increase the BW
- reduce the t_{eq}

BUT: unfortunately there are mismatches $\rightarrow M_1 \neq M_2$



$$C_{m1} \neq C_{m2}$$

There will be a residual error

$$V_{injection, residual} = \Delta V_g \frac{C_{gd}}{C_m} \left(\frac{\Delta C_{gd}}{C_{gd}} + \frac{\Delta C_m}{C_m} \right)$$

if the mismatch b/w the two capacitors is 1% $\Rightarrow \Delta C_m / C_m = 1\%$

if the mismatch b/w the two transistors is 1% $\Rightarrow \Delta C_{gd} / C_{gd} = 1\%$

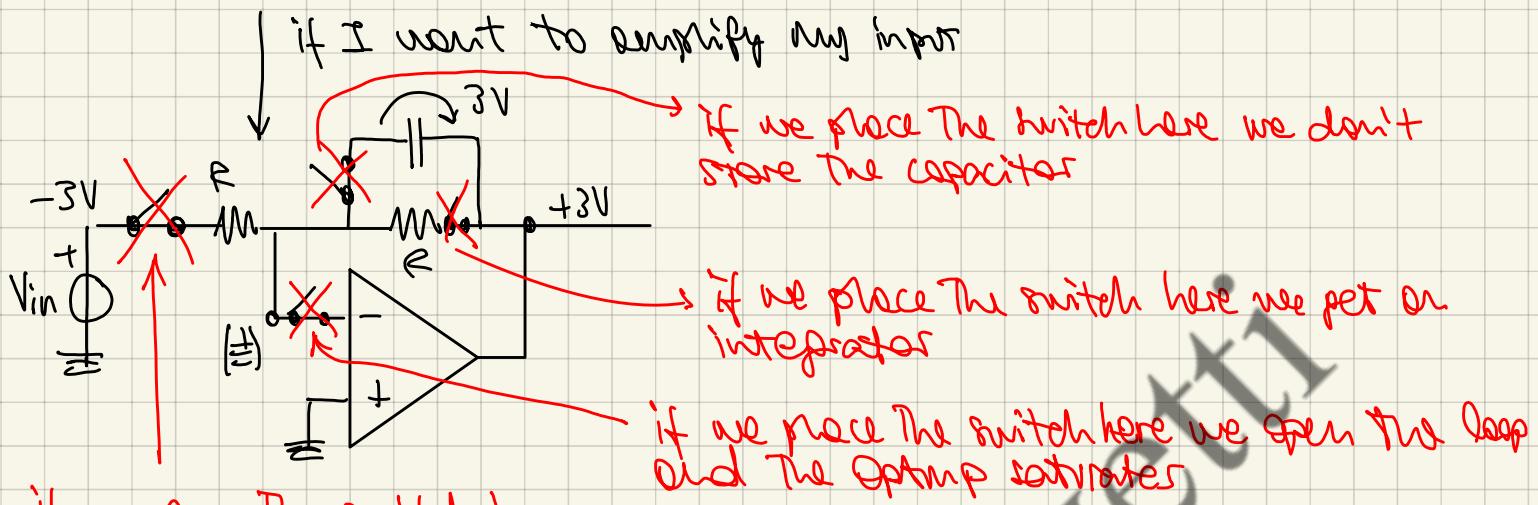
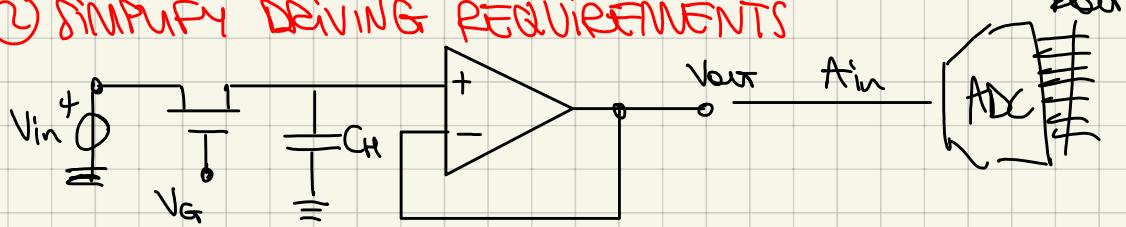
$$\Rightarrow V_{inj, residual} \approx 2\%. V_{inj, original} = 0.02 \cdot 1\text{mV} = 20\text{ }\mu\text{V}$$

if we decrease $C_m = 9\text{nF} \rightarrow 450\text{pF}$ \Rightarrow charge injection is still 1mV

$$\Rightarrow t_{eq} = 300\text{ns} \rightarrow 6.3\text{ }\mu\text{s}$$

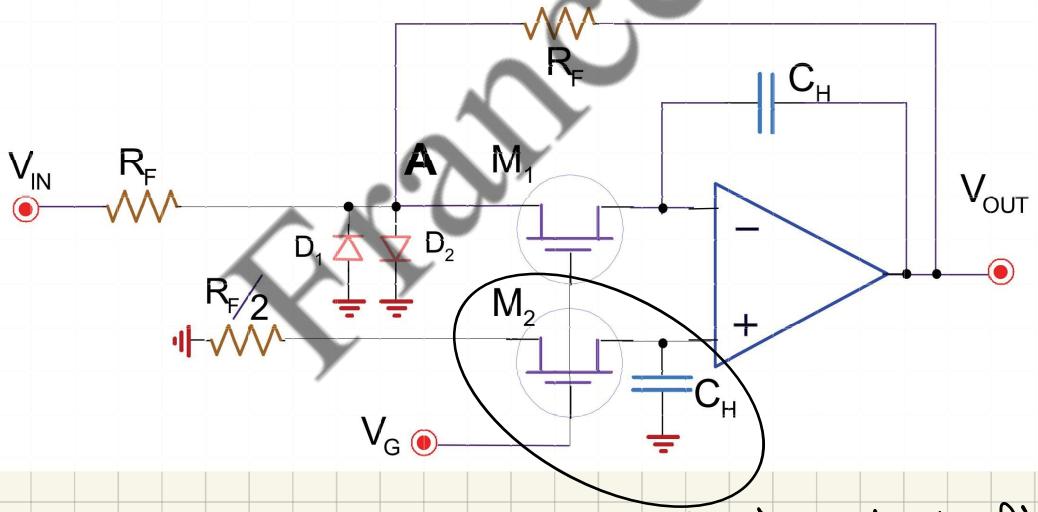
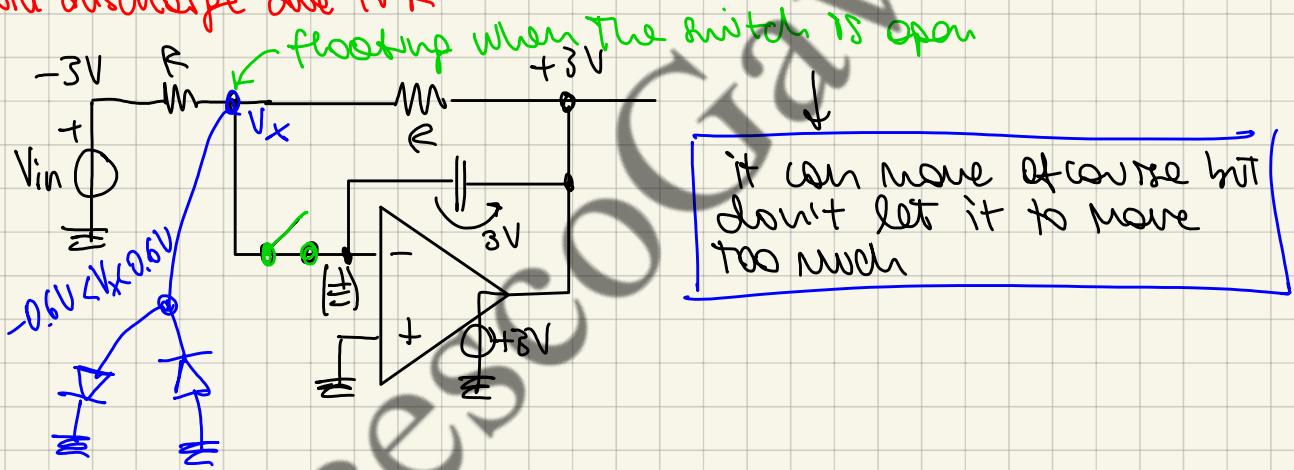
\Rightarrow BUT signal feedthrough worsens

② SIMPLIFY DRIVING REQUIREMENTS



if we place the switch here
The cap. will discharge due to R

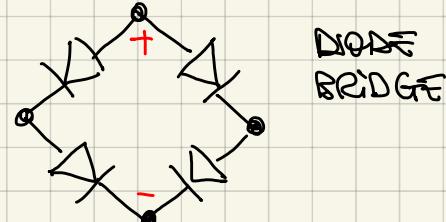
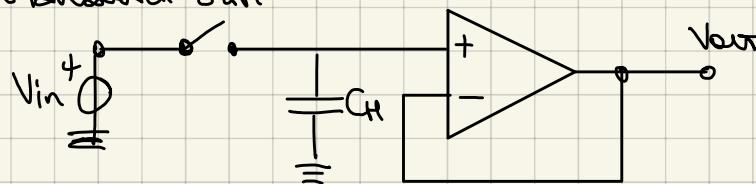
SOLUTION



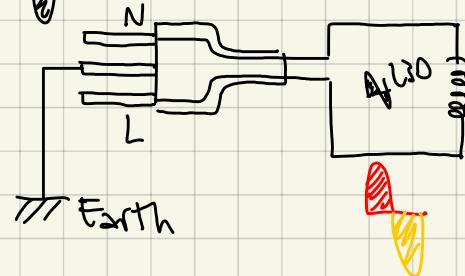
09/11/2021

③ SPEED UP THE SWITCH

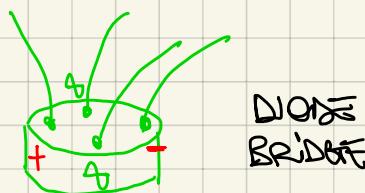
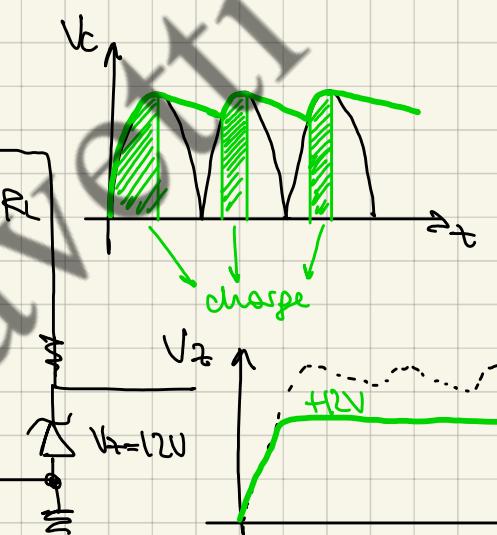
Standard S&H

DOUBLE RECTIFIER

230V 50Hz

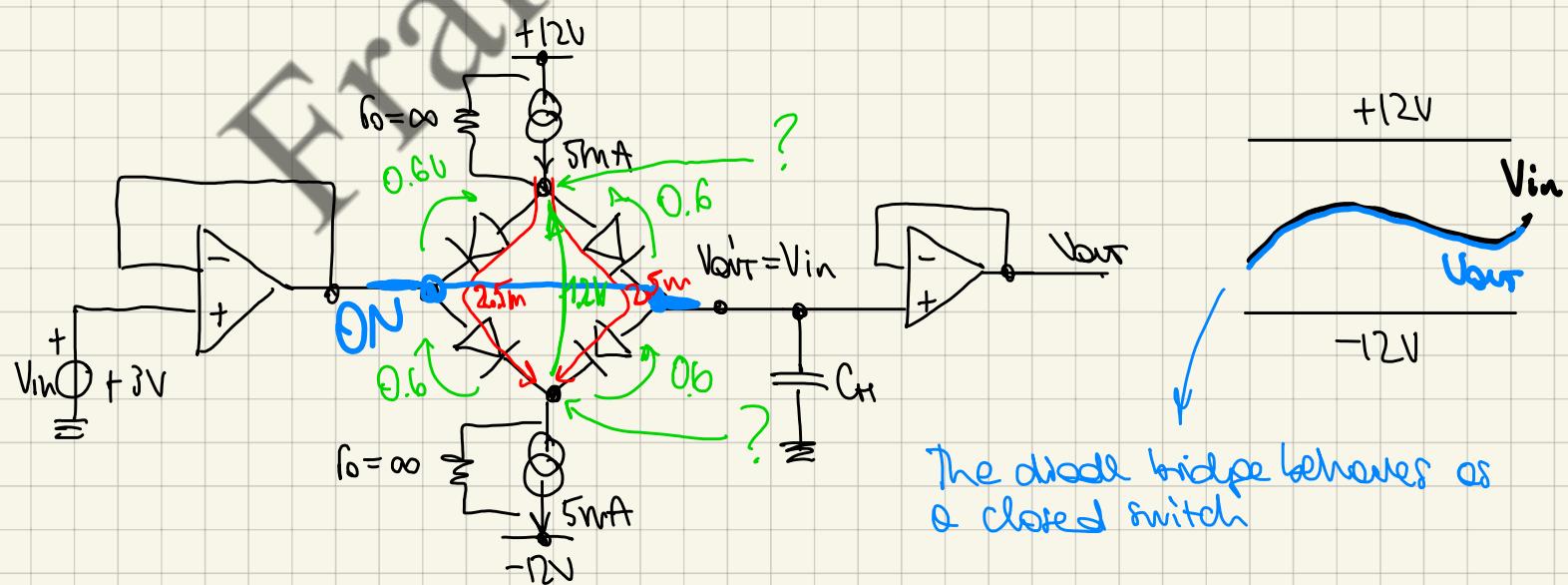


$$V_P = 12V \cdot \sqrt{2} = 17V$$

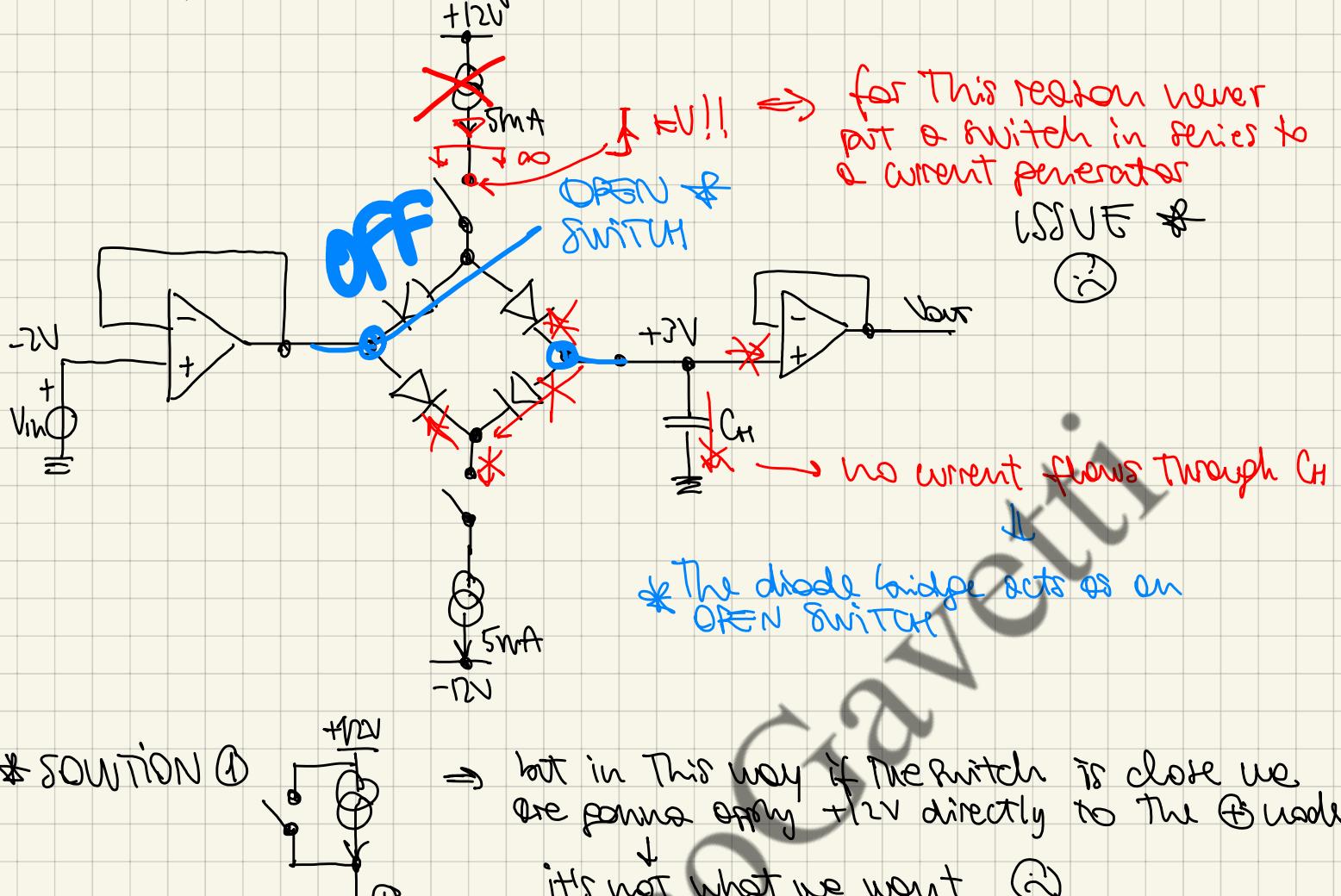


- + : where the two cathodes are connected → from the + we see the positive half period
- : where the two anodes are connected → from the - we see the return of the current

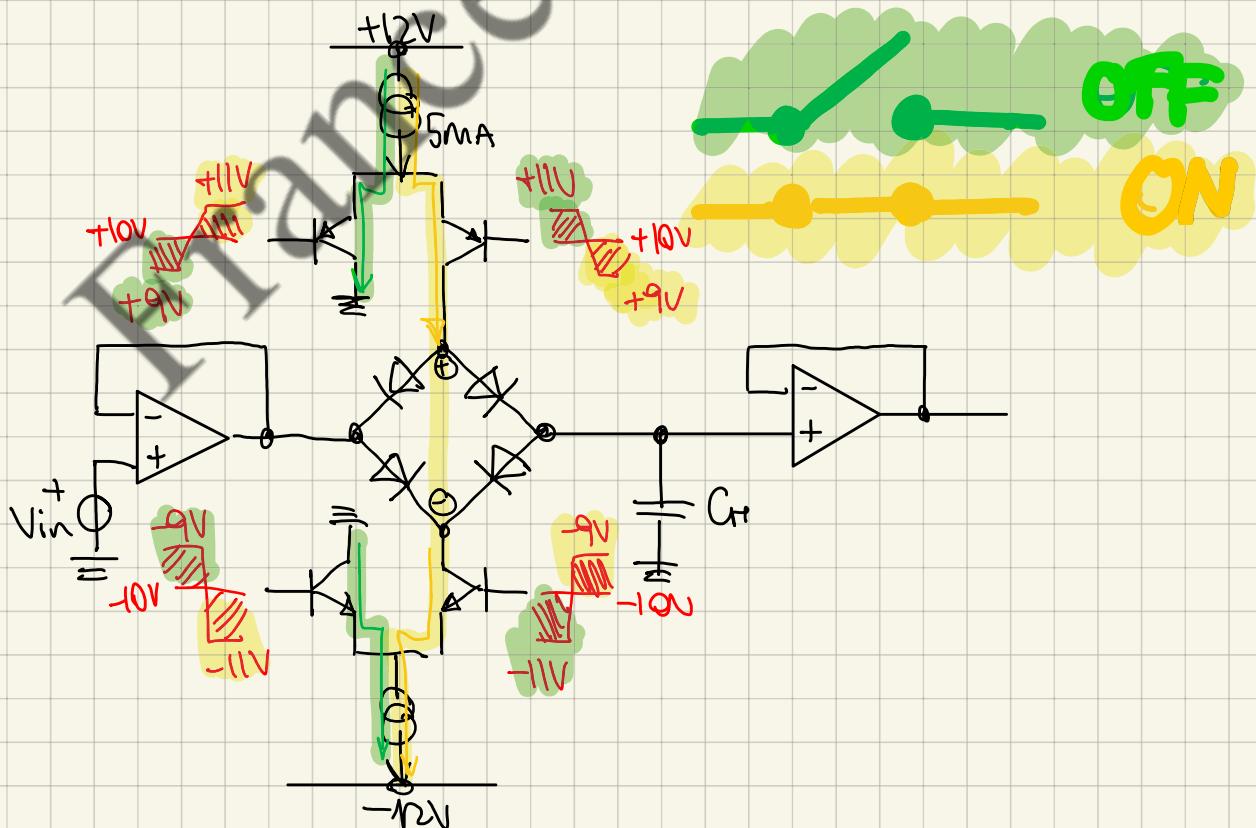
Goal: operate the diode bridge in order to act as a switch



Now let's remove the current generators

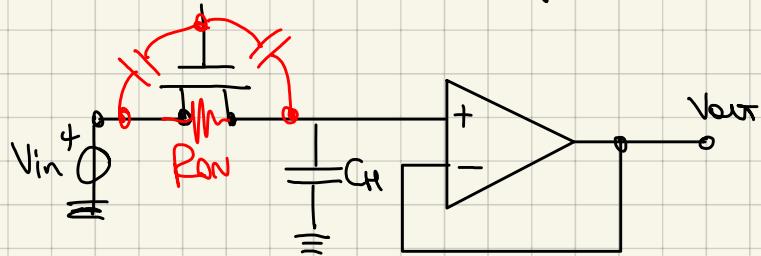


SOLUTION ② : Let's use a differential pair



What's the advantage of this configuration?

In the standard SRH config.



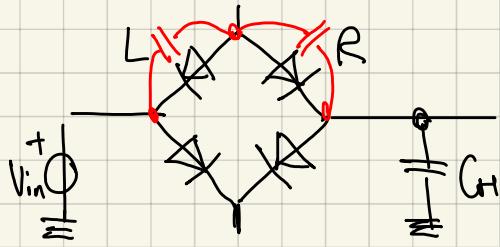
R_{ON} is NOT mil

$$R_{ON} \approx 10 \div 100 \Omega$$

\Rightarrow BW is limited

C_{gd}, C_{gs}, C_{ds} are not mil (parasitics) \Rightarrow They cause charge injection when we open the switch

In this H-configuration:



$$R_{ON} = \frac{1}{2} \left(\frac{1}{g_{m,\text{left}}} + \frac{1}{g_{m,\text{right}}} \right)$$

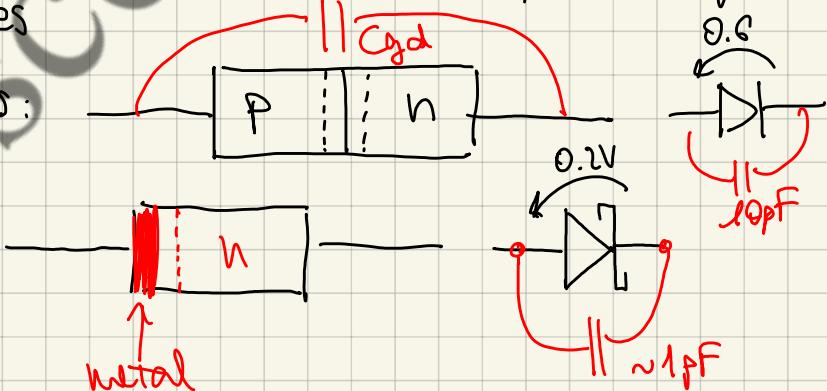
$\Rightarrow R_{ON} \approx 1 \div 10 \Omega$ very low

• BW is much larger

• Parasitics can be minimized, since they are in series

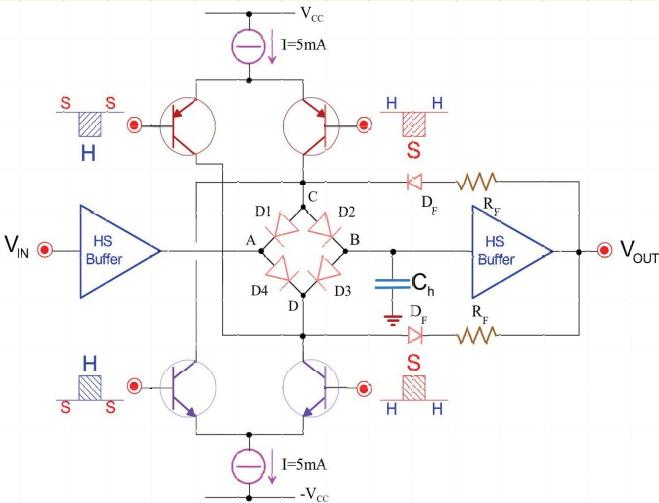
Instead of using standard diodes:

we can use Schottky diodes:



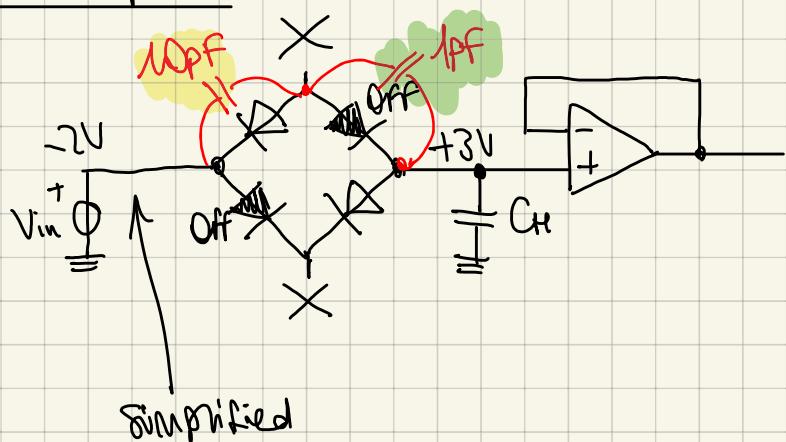
Having smaller parasitic capacitances means having a good improvement in terms of switch-on / switch-off performances.

FINAL CONFIGURATION:



Why this crisscross configuration?

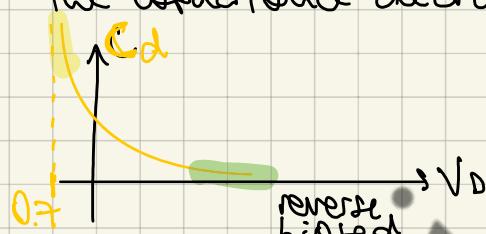
Hold phase:



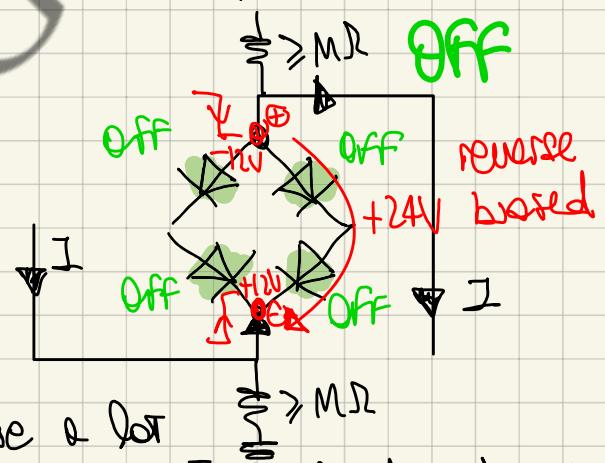
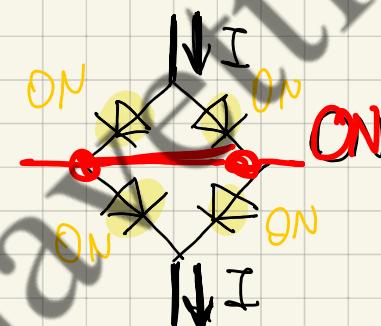
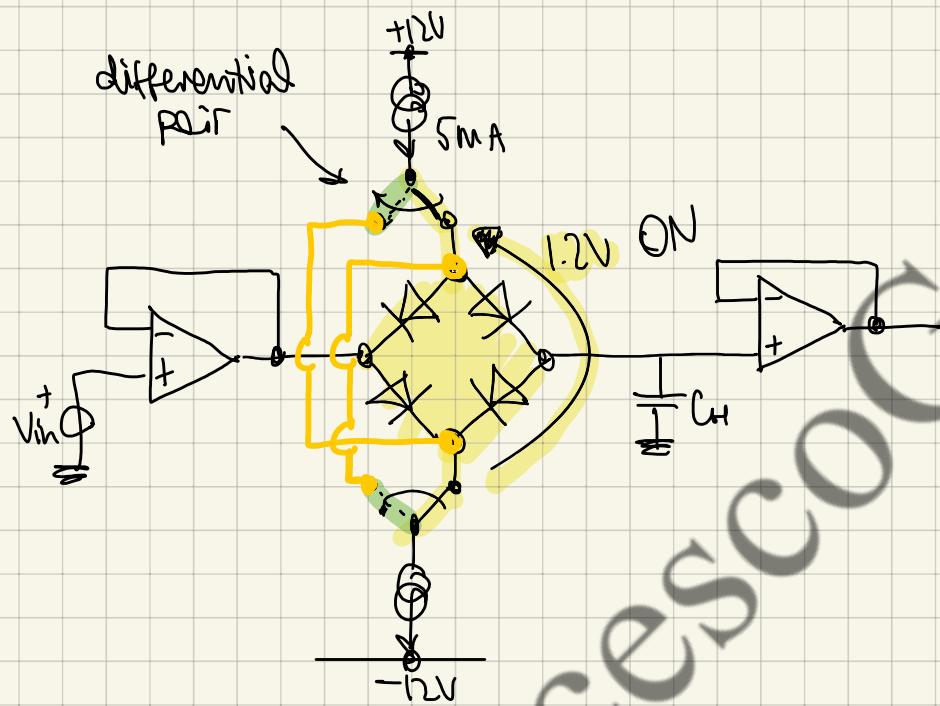
Everything we have a diode, if we increase the reverse voltage

↓
The depleted region increases

the capacitance decreases



differential pair



Thanks to the crisscross the reverse bias can increase a lot and reach +74V and so the parasitic capacitances can get very much reduced till 0.1 pF

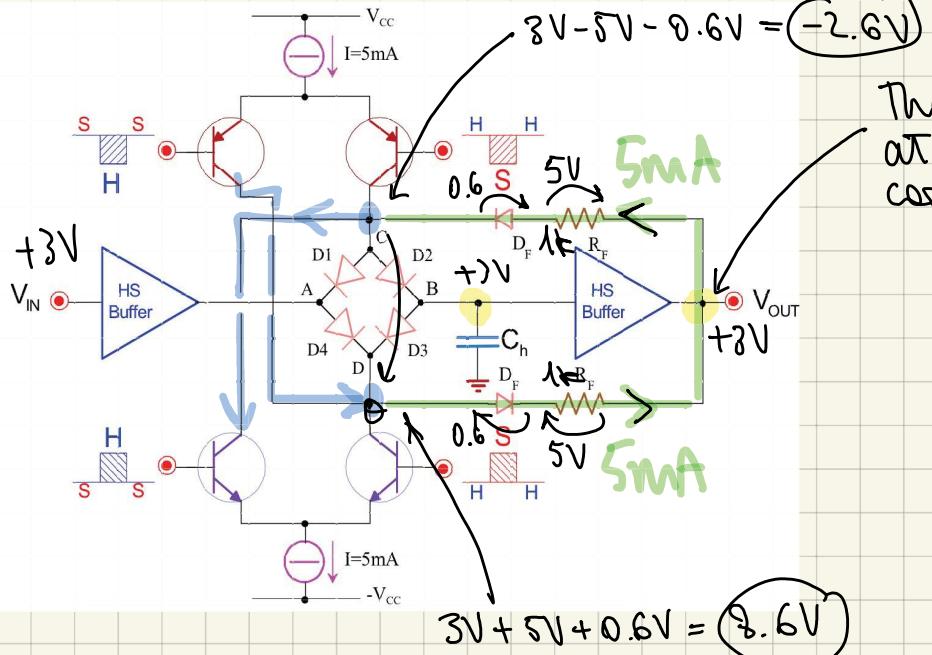
↓
This means that during the OFF condition :

- charge injection will be very low
 - supply feedthrough will be very low
- and so on, so on.

V^+ and V^- will increase in an unpredictable way and they could saturate to the PS. And if $(V^- - V^+)$ increases too much, it will take a longer time to move from OFF back to ON

↓
In order to speed up the ON-OFF and OFF-ON transitions we add a further path which doesn't draw V^+ and V^- to reach respectively -12V and +12V



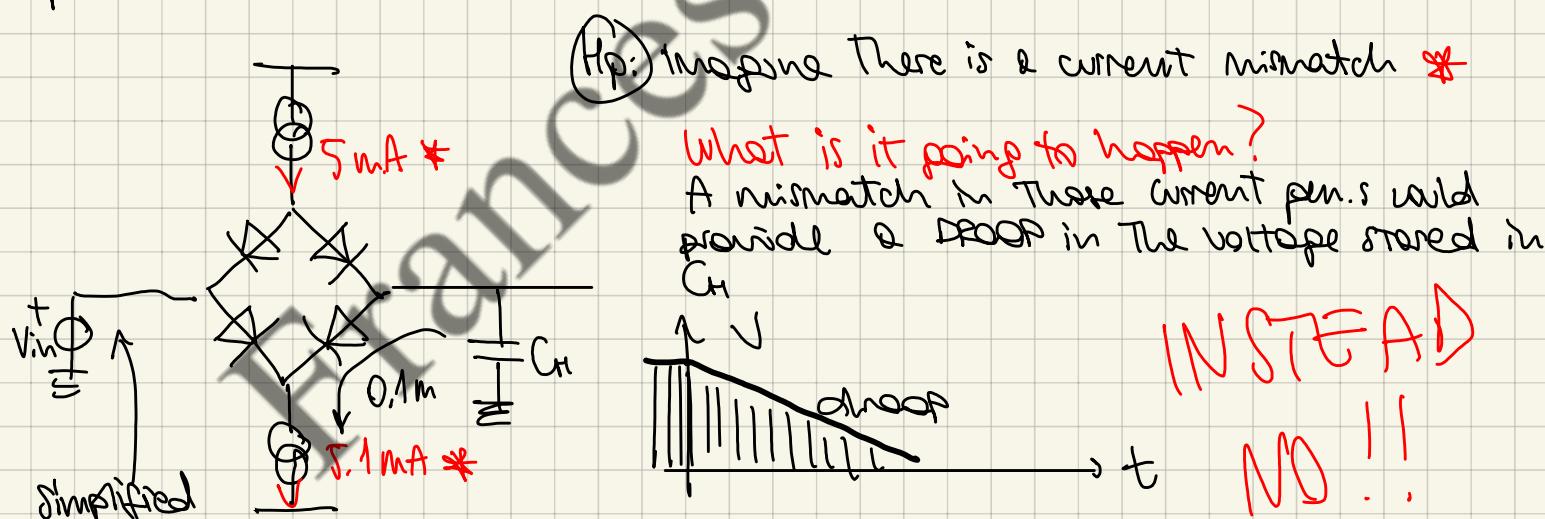


Thanks to The buffer, This node stays at The same voltage stored in the capacitor

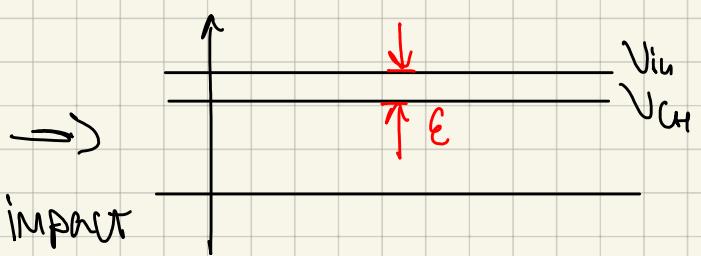
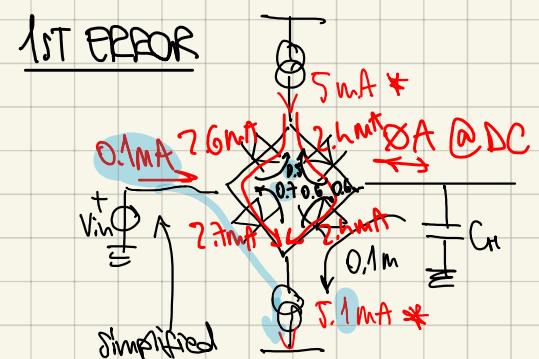
→ in This way $V_- - V_+ = 8.6V - (-2.6V) = 11.2V < 24V \Rightarrow$ faster transitions ON-OFF & OFF-ON
 $V_D - V_C$

This configuration suffers of **POOR ACCURACY** anyway b/c The diodes forming The bridge can experience different voltage drops due to mismatches which translates in an offset voltage much higher than That one we could have in a standard S&H config.

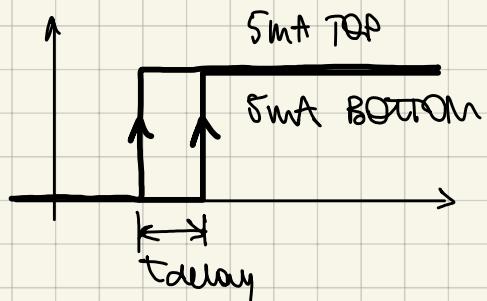
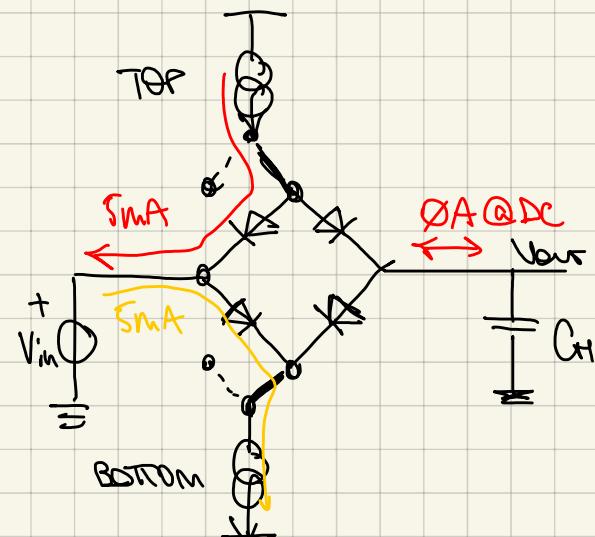
There is also the **TIMING ISSUE** to solve, that is the time to properly drive the bases of The diff pair of The upper-side and The bases of The diff. pair of The bottom side



A different error comes up from This current mismatch

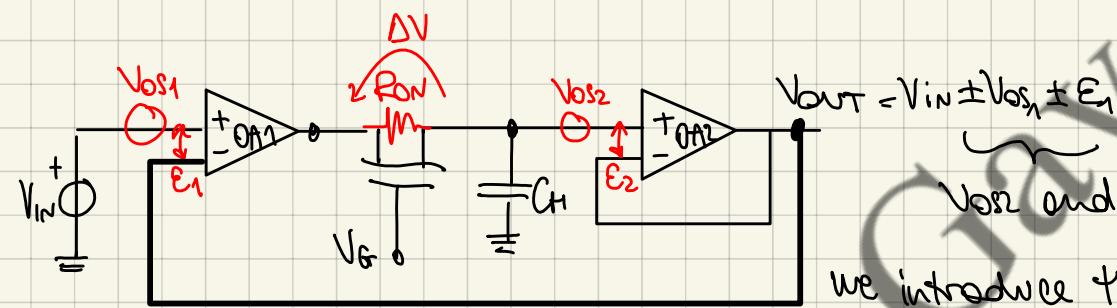


2nd ERROR



What's the error due to a mismatch in timing of the generators?

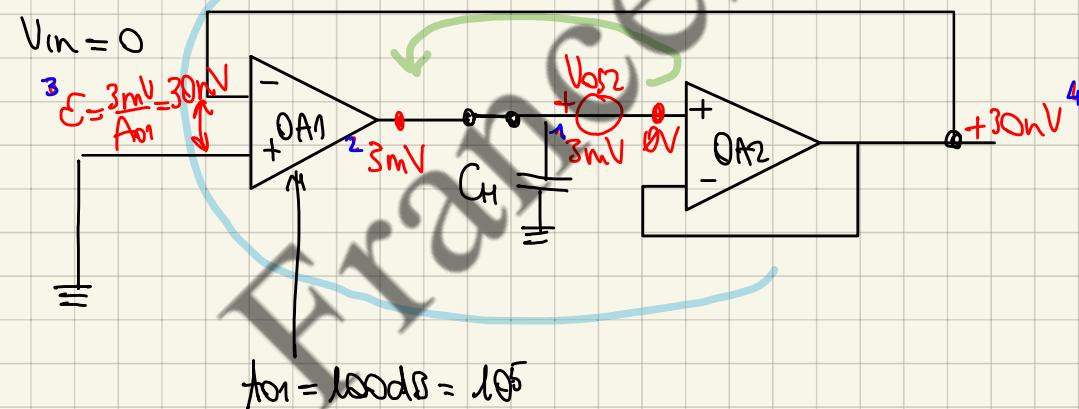
④ FEEDBACK S&H CONFIGURATION



Vos2 and E2 are killed by the FB

We introduce the FB to force the output to be equal to Vin, thanks to the wire

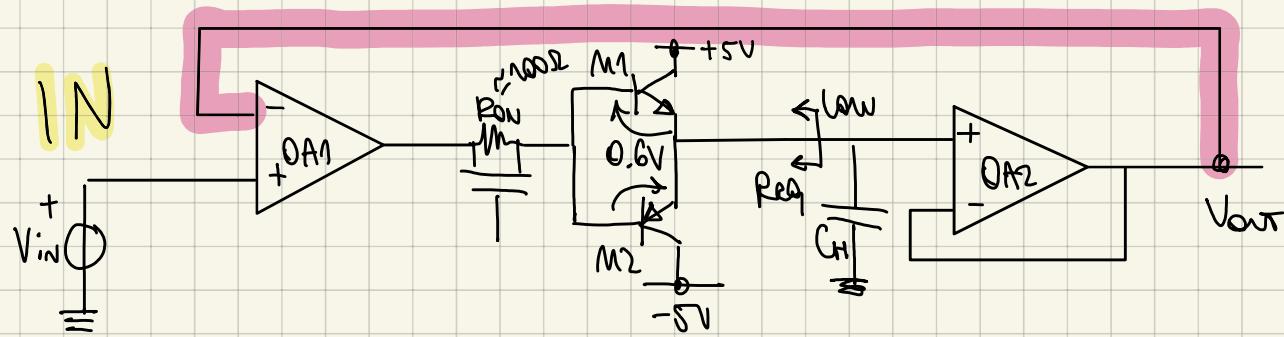
We proceed in the opposite way compared to the real signal



$$\left. \begin{aligned} V_C (Vos_2) &= \frac{Vos_2}{A_{01}} \\ V_C (Vos_1) &= Vos_1 \cdot 1 \end{aligned} \right\} \quad V_C = Vos_1 + \frac{Vos_2}{A_{01}}$$

Now we want to reduce the value of R_{ON} as much as we can

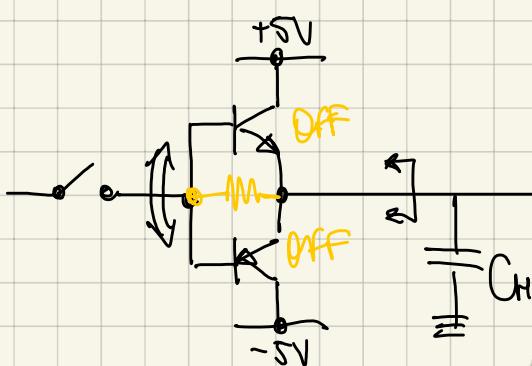
- SAMPLING



- if $V_{in} > 0 \rightarrow M_1$ is ON $\rightarrow V_{out} = V_{in}$
- if $V_{in} < 0 \rightarrow M_2$ is ON $\rightarrow V_{out} = V_{in}$

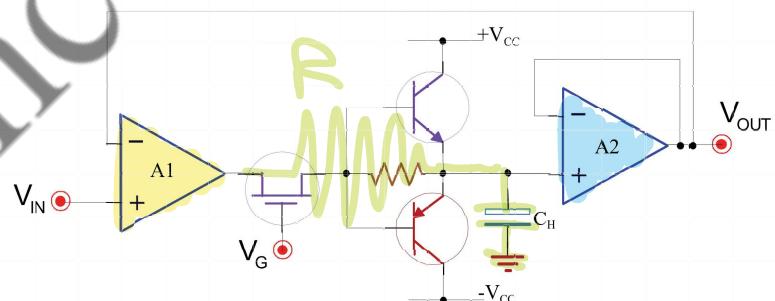
$$R_{eq} = \frac{1}{g_m} + \frac{R_{on}}{(\beta + 1)} \approx \frac{1}{g_m} = 10\Omega \ll R_{on} = 100\Omega$$

- HOLD



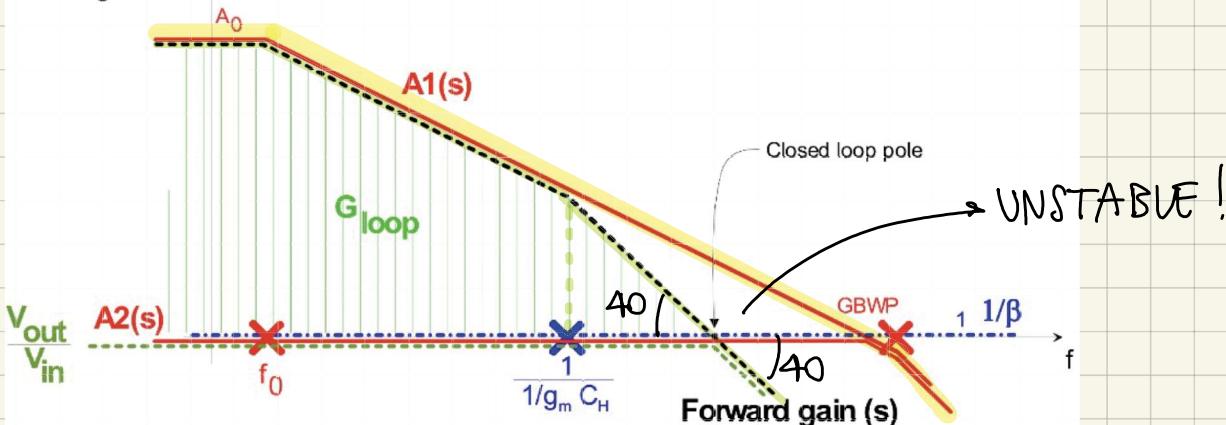
We want to be sure that in the hold phase the two transistors are off otherwise the capacitor can charge up or discharge depending on what transistor is on

- when the switch is closed, it works as a buffer
- when the switch open

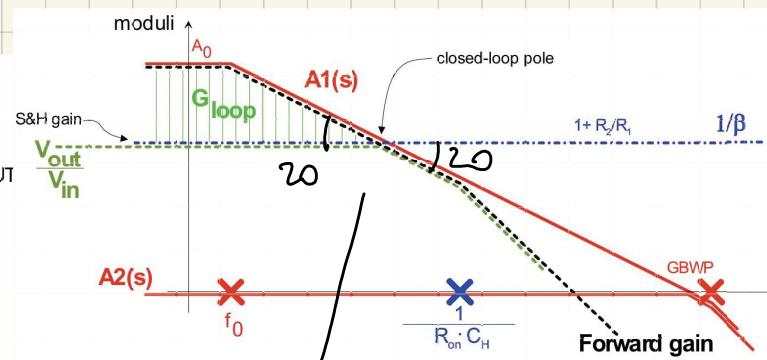
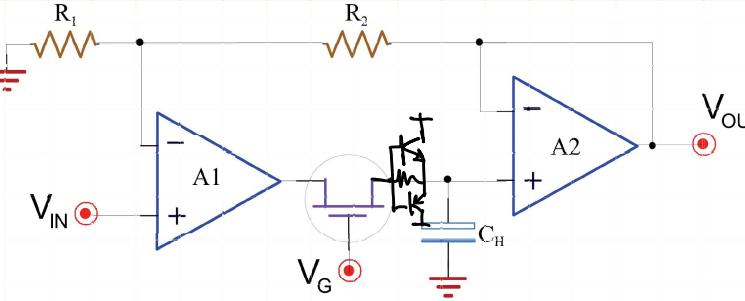


let's study the stability

magnitudes

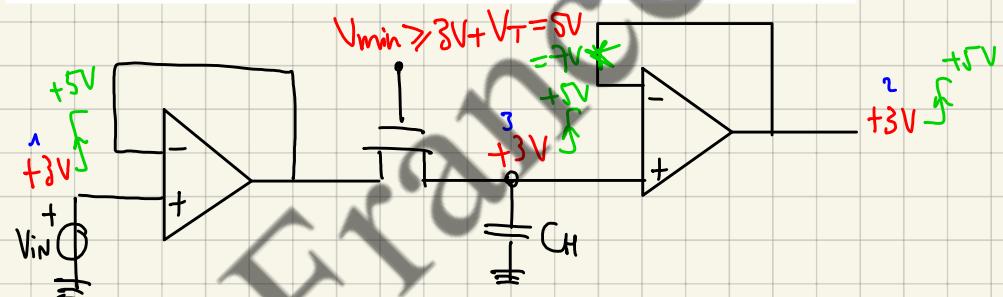
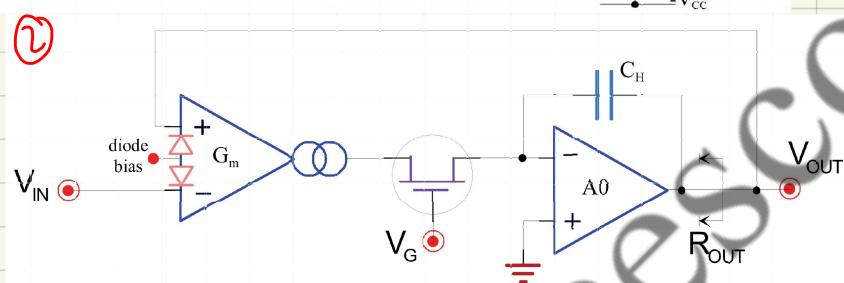
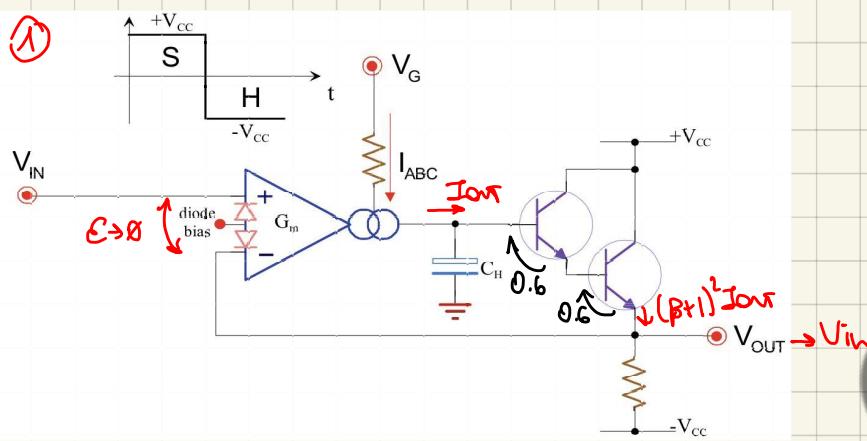


How can we repair stability?



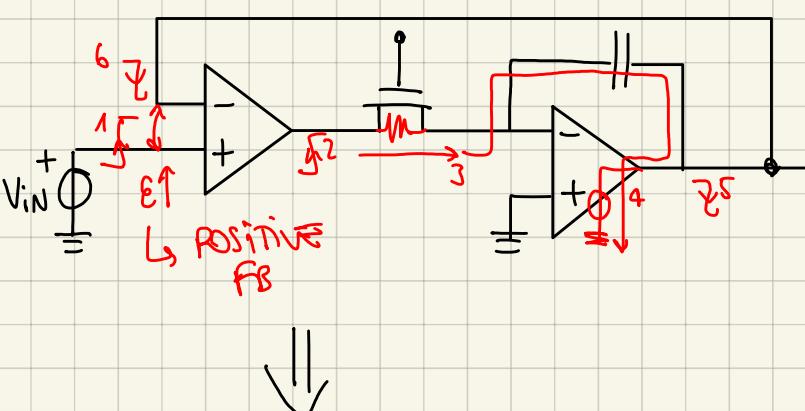
STABUE!

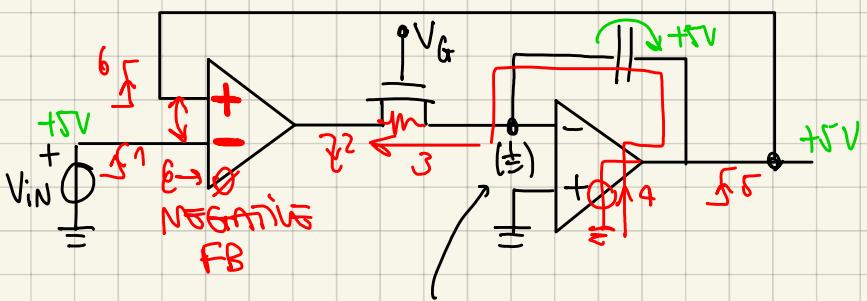
OTHER S&H CIRCUITS



* if the PI is +5V, it's not possible

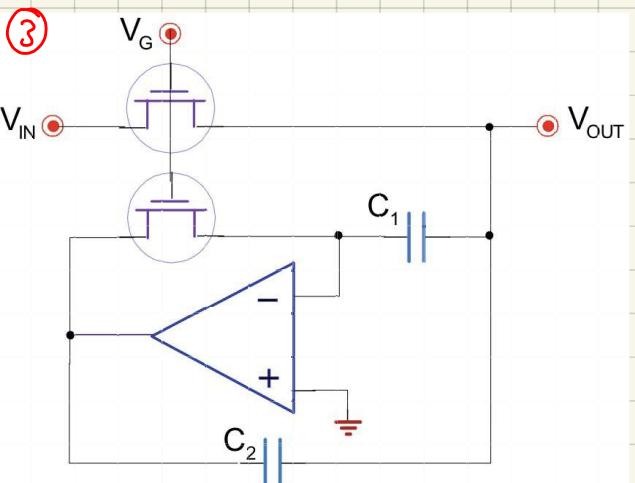
SOLUTION:



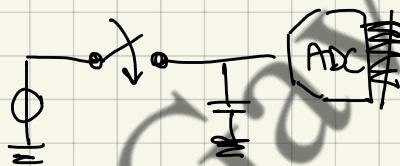


Since it is V_F. $\Rightarrow V_{F, \min} > \text{CMOS level } (+3.3\text{V})$

If The 2nd OpAmp keep V⁻ at 0V (v.p.), it has no sense to use a standard OpAmp as 1st OpAmp, but it's better to use a OTA which pumps current into the V_G.

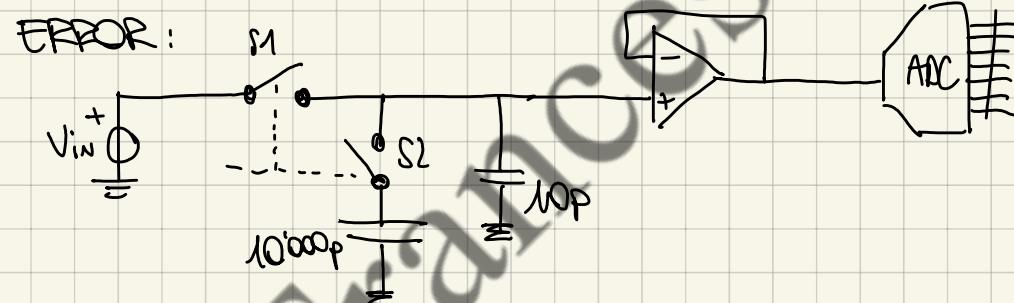


- In a S/H circuit when we close the switch, in order to reduce $T_{eq} = T \ln(1/e)$ we should reduce T and in order to reduce T we should use a small C_H ($\sim 1\text{pF}$)



- When we open the switch instead, in order to reduce droop we should use a big C_H ($\sim 10\text{nF}$)

\Rightarrow We need something that is adjustable!!

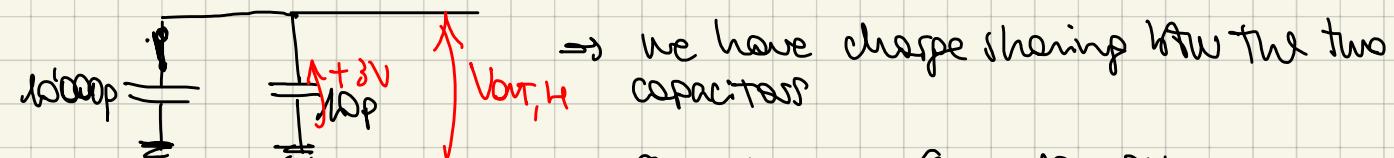


When S1 opens, S2 closes and vice versa.

- HOLD \rightarrow S1 open, S2 close $\rightarrow C_H = 10'010\text{pF}$
- SAMPLING \rightarrow S1 closes, S2 opens $\rightarrow C_H = 10\text{pF}$

What's the error?

When we close S2 and open S1, we connect the 10pF cap. which is charged @ +3V to a big capacitor:



\Rightarrow we have charge sharing b/w the two capacitors

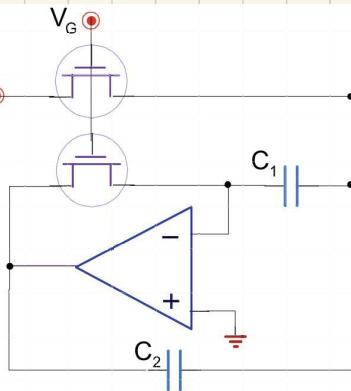
$$Q = CV \Rightarrow Q_S = 10\text{pF} \cdot 3\text{V}$$

$$Q_H = 10'010\text{pF} \cdot V_{out}$$

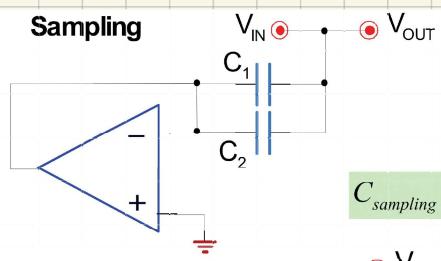
$$Q_H = Q_S \rightarrow 10'010\text{p} V_{OUT,H} = 10\text{p} \cdot 3V \Rightarrow V_{OUT,H} = 3V \frac{10\text{p}}{10'010\text{p}} = 3mV$$

\Rightarrow This circuit is not smart !! 😒

SOLUTION :

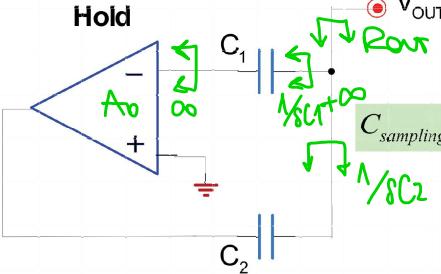


Sampling



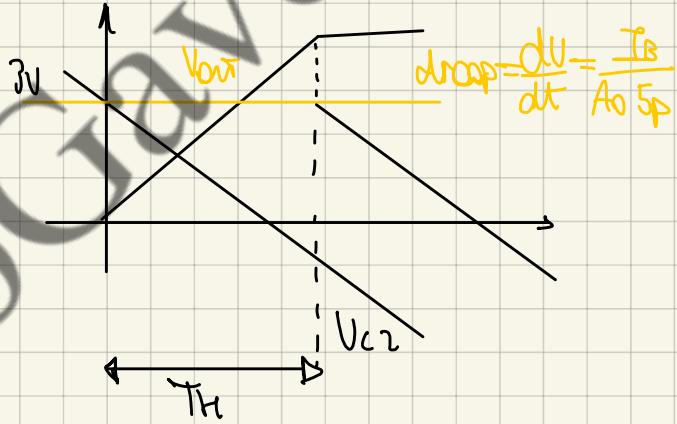
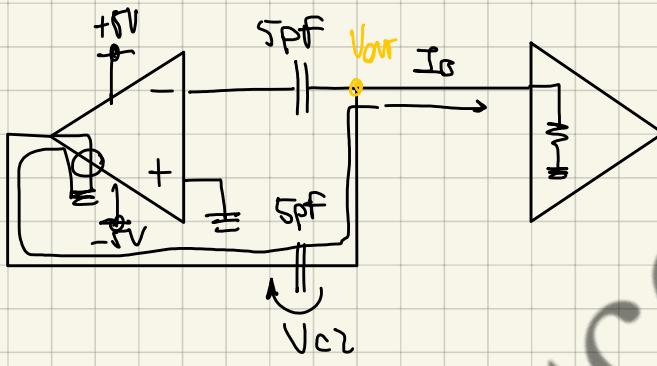
$$C_{sampling} = C_1 + C_2$$

Hold



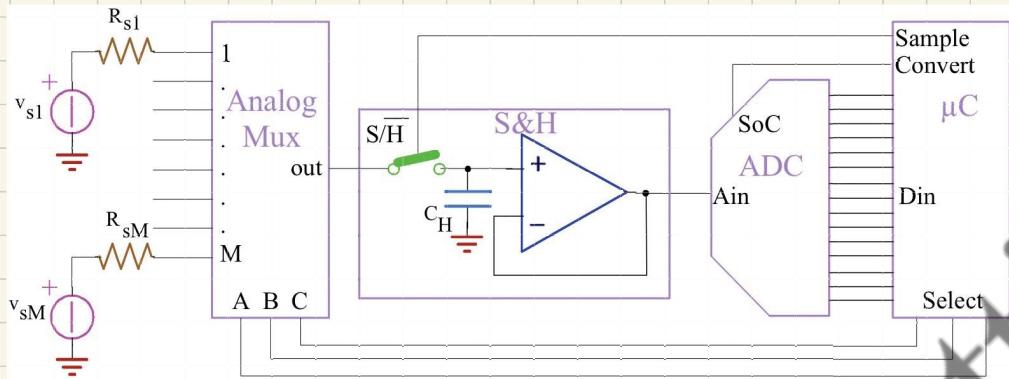
$$C_{sampling} = C_2 \cdot A_0$$

$$V_{OUT} = \frac{1/S_C_2 || \infty}{1 + A_0} = \frac{1/S_C_2 || \infty}{1 + A_0} \approx \frac{1}{S_C_2 A_0}$$



ANALOG MULTIPLEXER

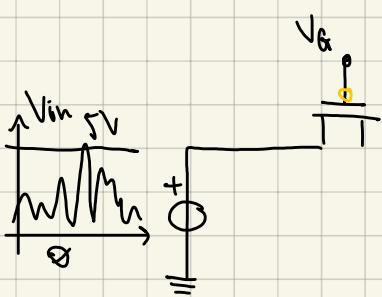
Often is very important to acquire many analog signals from various sources and to process them by means of a single digital processor, DSP or MC



An ANALOG MULTIPLEXER consists of very different channels at the input and just one channel at the output (or vice versa) and each input channel presents a switch which we can open close depending on what source we wanna read. The switches closure is regulated by a DIGITAL DECODER

* bcz The MUX is symmetric

How are those switches made?

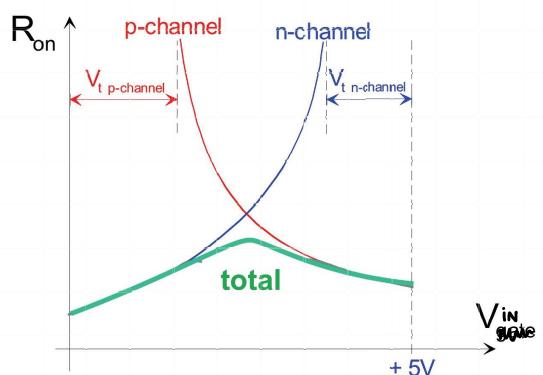
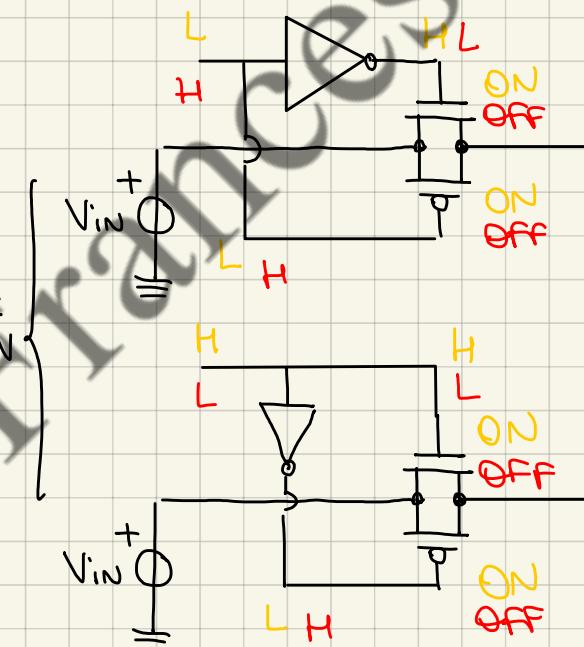


NMOS $\begin{cases} V_G = 0V \rightarrow \text{ON} \\ V_G = 5V \rightarrow \text{OFF} \end{cases}$

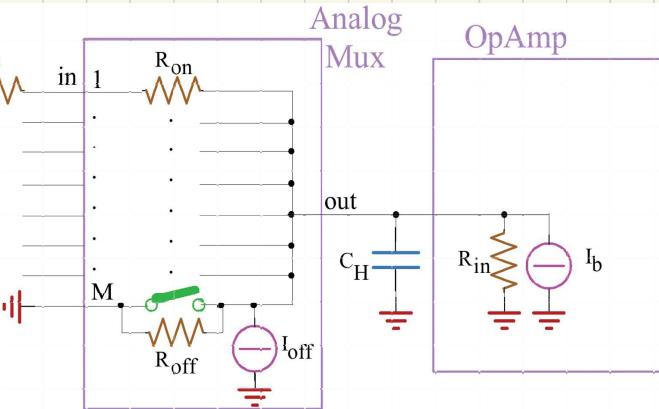
PMOS $\begin{cases} V_G = 0V \rightarrow \text{ON} \text{ only for } V_{in} < 5V - V_T \\ V_G = 5V \rightarrow \text{OFF} \end{cases}$

So The idea is:

PASS-TRANSISTOR CONFIGURATION



ANALOG MULTIPLEXER'S ERRORS :



$$R_{ON} = 10\Omega \div 10k\Omega$$

↳ it can be very high

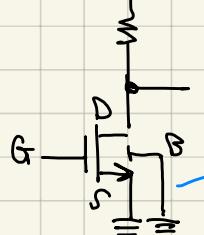
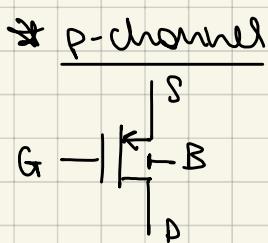
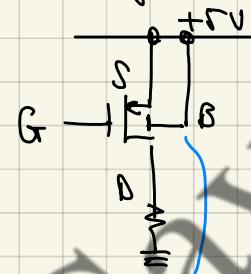
$$R_{OFF} > 10M\Omega$$

↳ it's not infinite

$$I_{OFF} < 100nA$$

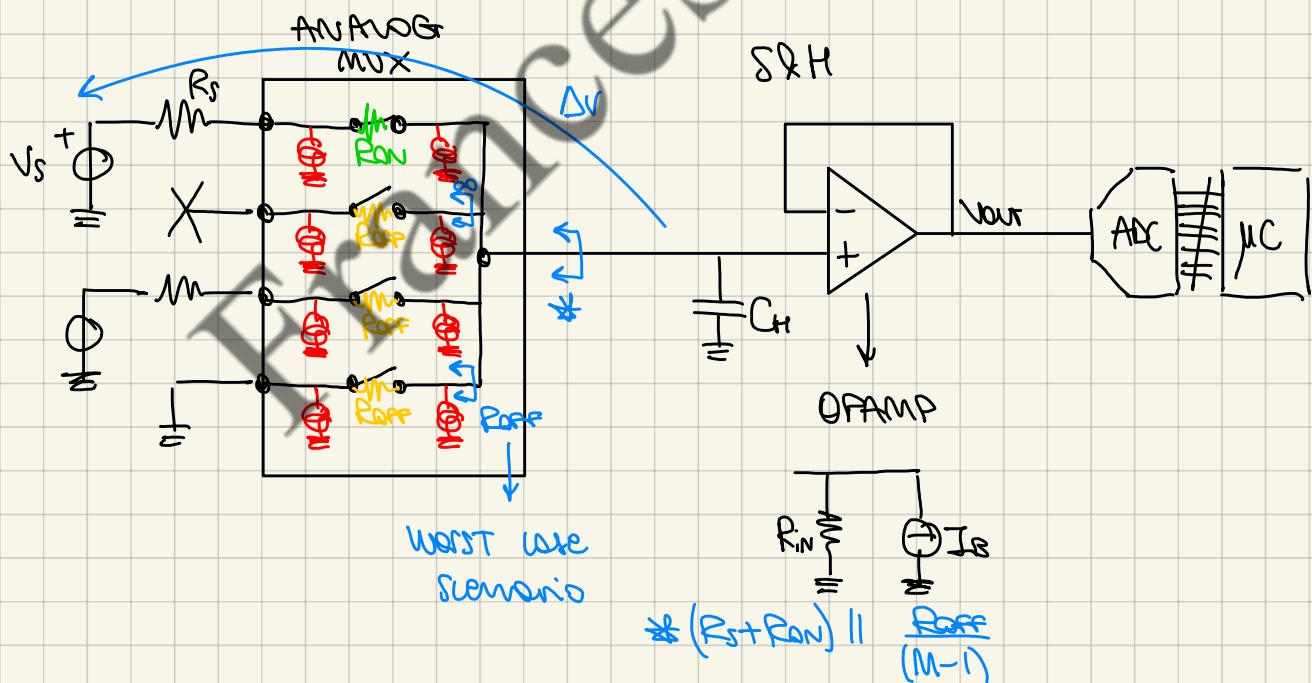
↳ both on the right and left side of each switch there's a leakage

* Both on the right and left side of each switch there's a leakage



in order to avoid S-B and D-B leakage

Which is the total error when we close a switch?



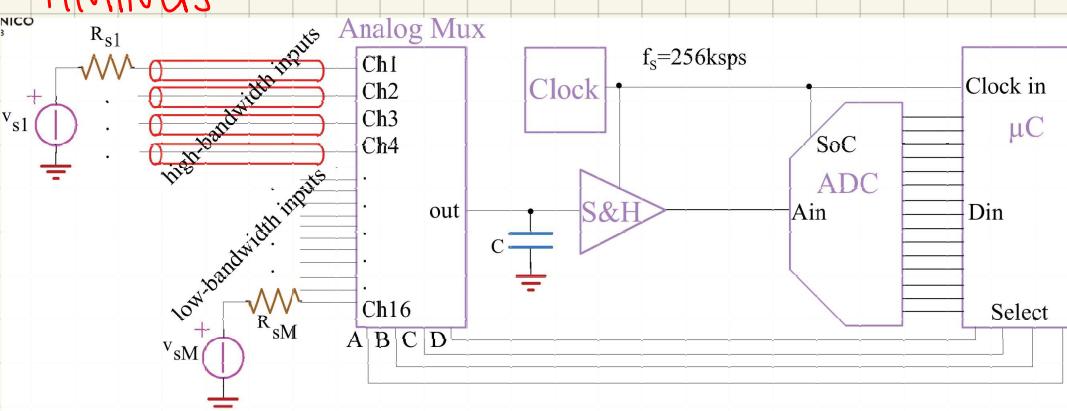
$$*(R_s + R_{ON}) \parallel \frac{R_{OFF}}{(M-1)}$$

$$\Delta V = \pm v_s \frac{R_s + R_{ON}}{R_s + R_{ON} + \left\{ R_{IN} \parallel \left[\frac{R_{OFF}}{(M-1)} \right] \right\}} \pm [I_{OFF}(M-1) + I_B] \left\{ (R_s + R_{ON}) \parallel R_{IN} \parallel \left[\frac{R_{OFF}}{(M-1)} \right] \right\}$$

Conclusion: in a configuration like this let's try to use:

- as low as possible R_s
- as low as possible R_{ON}
- as high as possible R_{OFF}
- as low as possible I_B
- as low as possible I_{OFF}

TIMINGS



if $ABCD = 0000 \rightarrow \text{Ch1 is selected}$
 if $ABCD = 0001 \rightarrow \text{Ch2 is selected}$
 :
 if $ABCD = 1111 \rightarrow \text{Ch16 is selected}$

The value of $ABCD$ is decided by the μC

The proper timing for the S&H and for the ADC can be provided by the μC w/ its clock-out or can be even used an EXTERNAL CLOCK which drives the S&H. The conversion of the ADC and the acquisition of the μC

if we have an ADC w/ $f_s = 256\text{ kspS}$

Which is the maximum freq. we can apply at each individual channel?
 (in order to compute which is BW max)

We acquire Ch1 every 16 acquisitions and each acquisition lasts $\frac{1}{f_s} = 3.9\text{ }\mu\text{s}$
 so Ch1 will be acquired every $16 \cdot 3.9\text{ }\mu\text{s} = 62.4\mu\text{s}$ which means that each channel will be acquired w/ a freq. of $\sim 16\text{ kspS}$ ($= f_s/16$)

↓
 This means that the maximum input BW must be $\frac{1}{2} \cdot 16\text{ kspS} = 8\text{ kspS}$
 according to Shannon \rightarrow Nyquist

Hp: Now let's imagine that of the 16 channels we want to preserve 4 high-BW inputs while the others will be low-BW

↓
 we want to use different timings for the input channels

We want the first 4 channels w/ a 20kHz BW: this means that they will be sampled every $f_s/5 = 51.2\text{ kspS}$ (but $2 \cdot 20\text{ kHz} < f_s = 256\text{ kspS}$ ✓)

The remaining 12 channels instead will be acquired every:

$$f_s = 4 \cdot f_s/5 + 12 \cdot f_s/x \Rightarrow 1 = 4/5 + 12/x \Rightarrow \frac{1}{f} = \frac{12}{x} \Rightarrow x = 12.5 = 60$$

↳ The other 11 channels will have $f_s/60 = 4.2 \text{ kspS}$

EXAMPLE: 12 bit ADC, requested accuracy lower than 1/2 LSB ($\epsilon < 1/2 \text{ LSB}$)

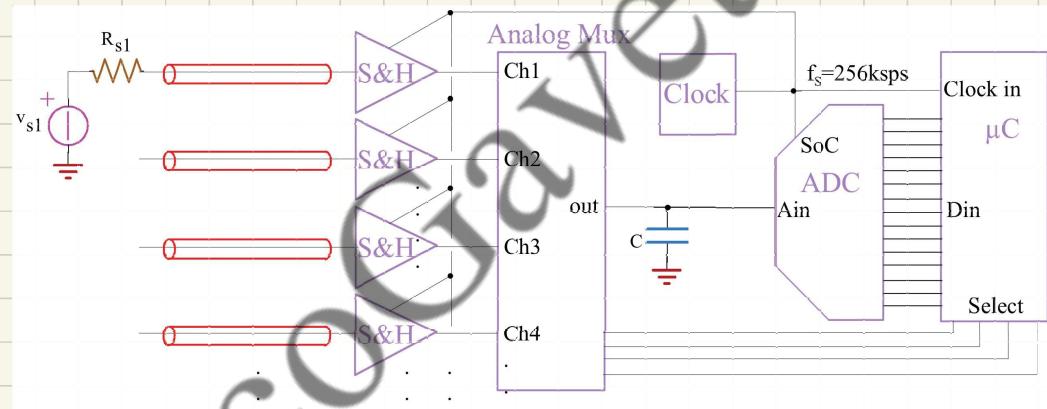
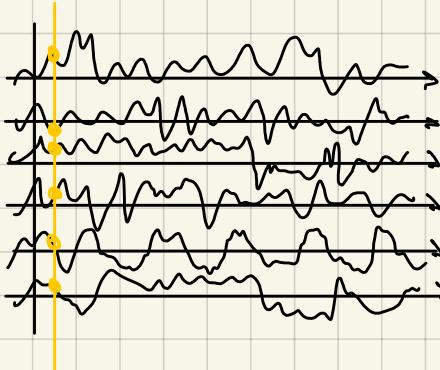
$T = \frac{1}{f_s} = 3.9 \mu\text{s} \rightarrow$ let's take $T = 3.8 \mu\text{s}$ in order to leave the remaining $0.1 \mu\text{s}$ for the conversion

$$\text{ACQUISITION TIME } T \leq \frac{T}{\ln\left(\frac{\text{FSR}}{1/2 \text{ LSB}}\right)} = \frac{T}{\ln(2.2^n)} \approx \frac{3.8 \mu\text{s}}{9} \approx 422 \text{ ns}$$

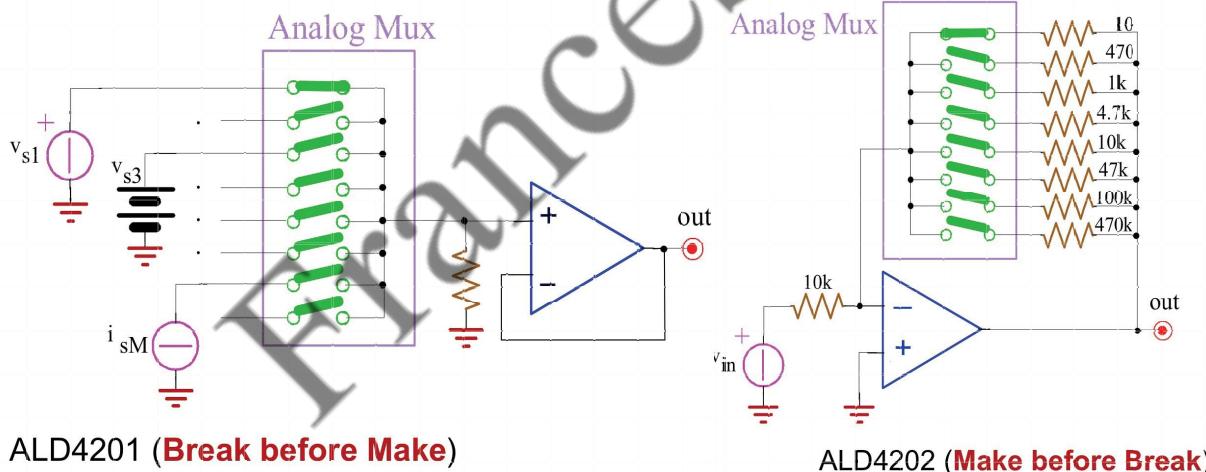
$$\text{w/ } C_H = 40 \text{ pF} \rightarrow T = C_H(R_s + R_{ON}) \leq 422 \text{ ns}$$

$\Rightarrow R_s + R_{ON} \leq 11 \text{ k}\Omega \rightarrow$ we cannot use whatever mic we want

SYNCHRONOUS COHERENT ACQUISITION



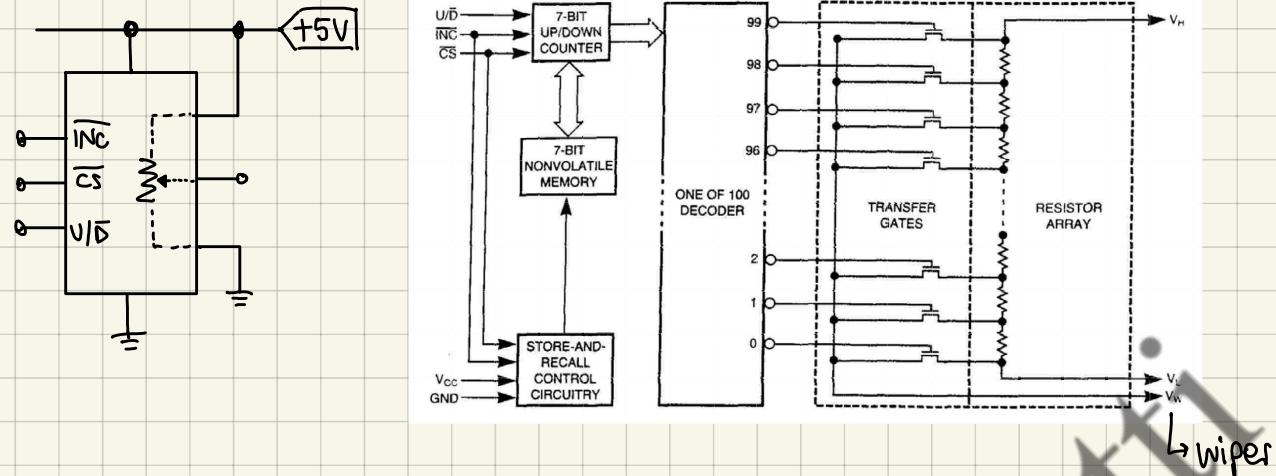
An A-MUX can be used also to change the gain of an OpAmp by changing what resistor it is connected to it:



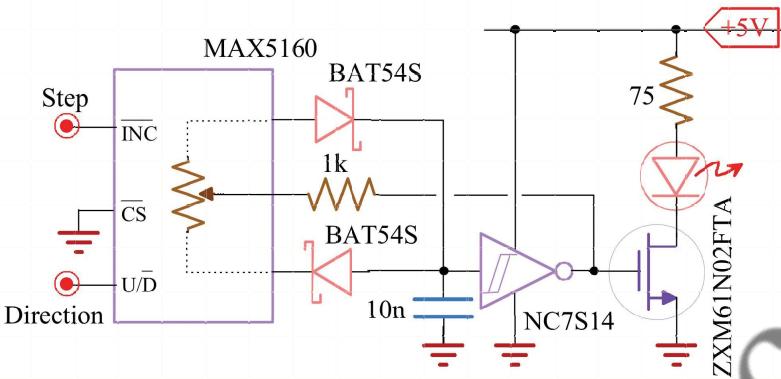
ES11 - MUX AND DIGPOT (1)

10/11/2021

DigPOT - DIGITAL POTENTIOMETER



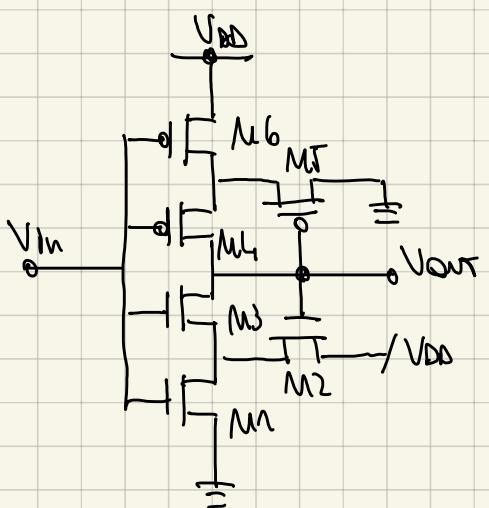
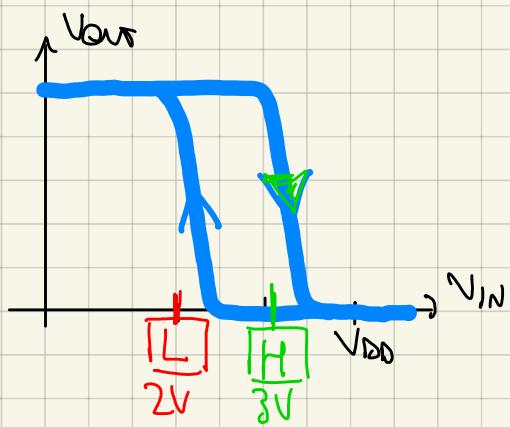
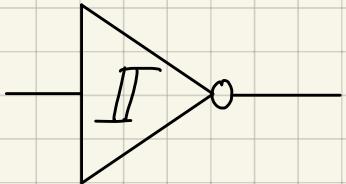
EXAMPLE:



typical inverting gate:

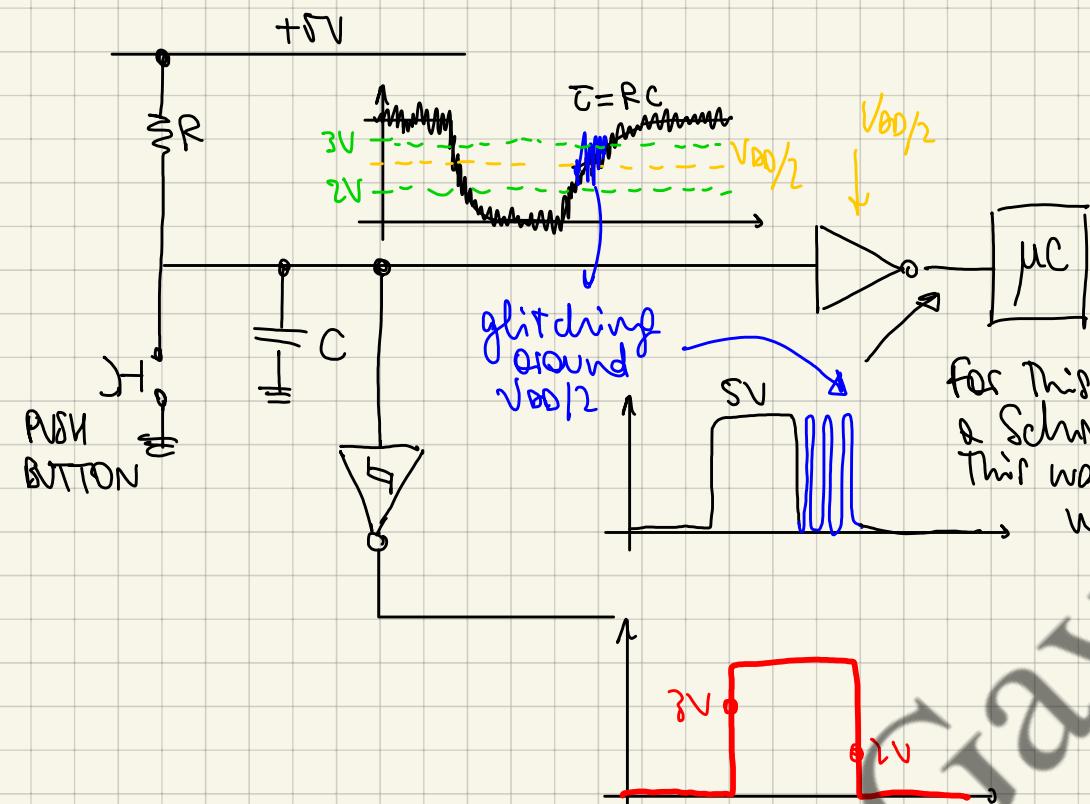


SCHMIDT TRIGGER



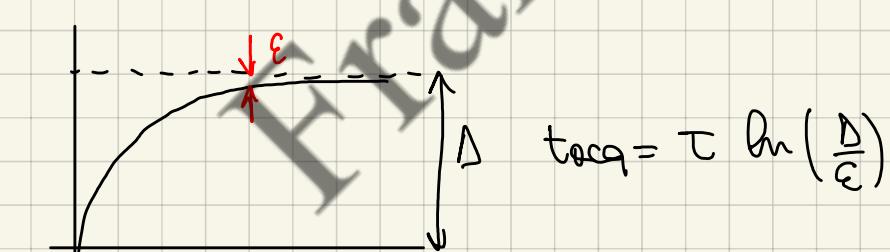
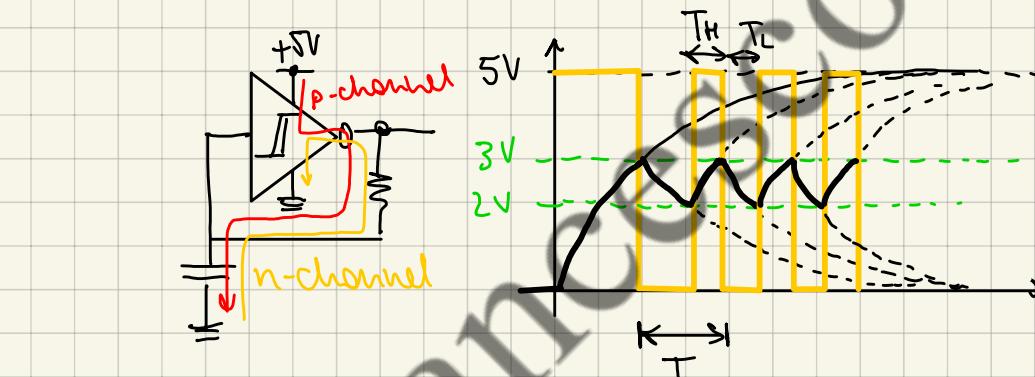
Why do we need a Schmitt trigger?

If we have a circuit like this:



for this reason we prefer to use a Schmitt trigger: SCT in this way the commutation will be much cleaner.

A useful implementation of The Schmitt trigger is to design an oscillator:



$$DC = 50\%$$

$$T_H = RC \ln\left(\frac{5V - 2V}{5V - 3V}\right) = RC \ln\left(\frac{3}{2}\right) = 0.4 RC$$

$$T_L = RC \ln\left(\frac{3V - 0V}{2V - 0V}\right) = RC \ln\left(\frac{3}{2}\right) = 0.4 RC$$

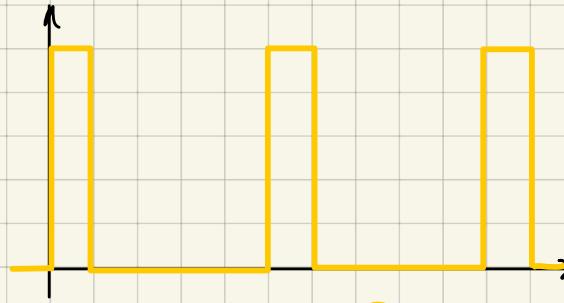
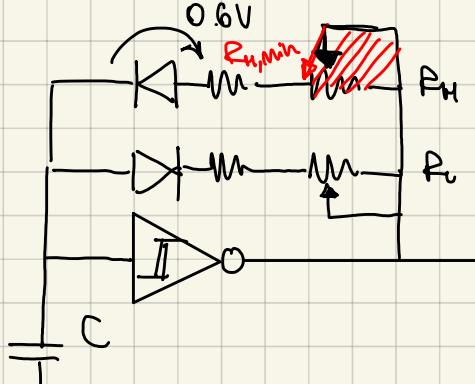
$$T = T_H + T_L = 0.8 RC \approx RC \Rightarrow f_{\text{osc}} = \frac{1}{T} \approx 1/RC$$

Now imagine we have an oscillation where the duty cycle varies

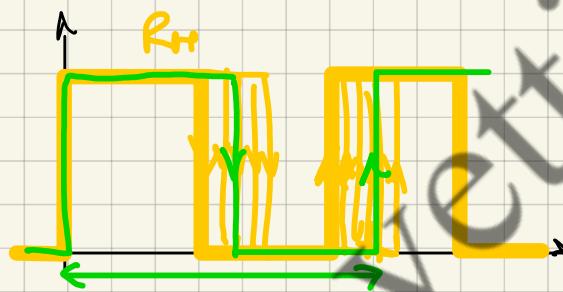
$$DC = \frac{T_H}{T} = \frac{T_H}{T_H + T_L}$$



DC ≈ 80%.



$DC \approx 20\%$



$$R_H + R_L = 10k\Omega$$

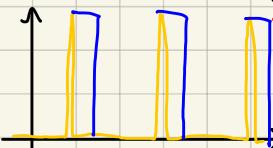
$$T_H \approx R_H C$$

$$T_L \approx R_L C$$

$$DC = \frac{D}{D+I}$$

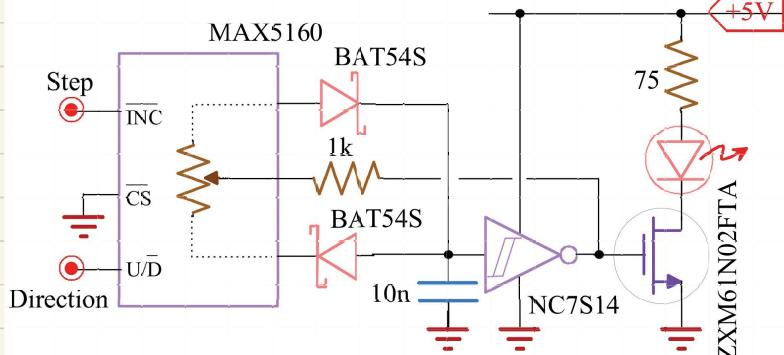
we don't have time
to settle

* ISSUE: if $(R_H + R_L) = 0 \rightarrow T = 0 \rightarrow$

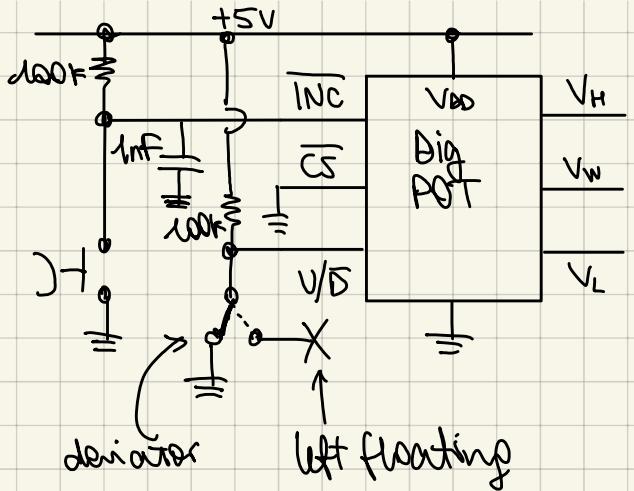


\rightarrow = SCHOTTKY DIODE

it's a metal-semiconductor junction whose bias voltage is not 0.6V but 0.2V



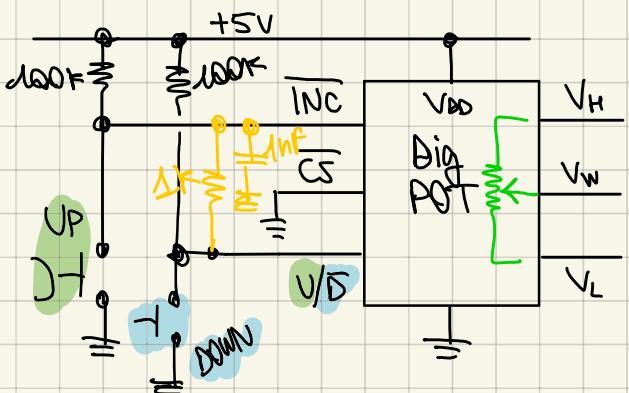
* SOLUTION: in order to include a minimum duration, it's better to include a R_{min} in order to avoid resistance degeneration



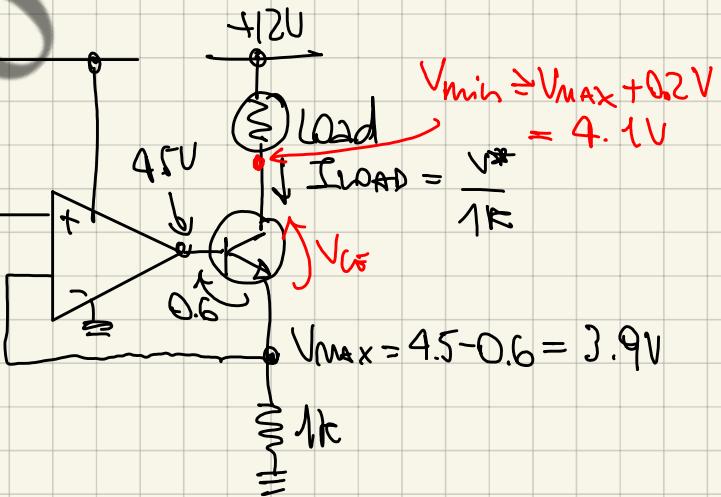
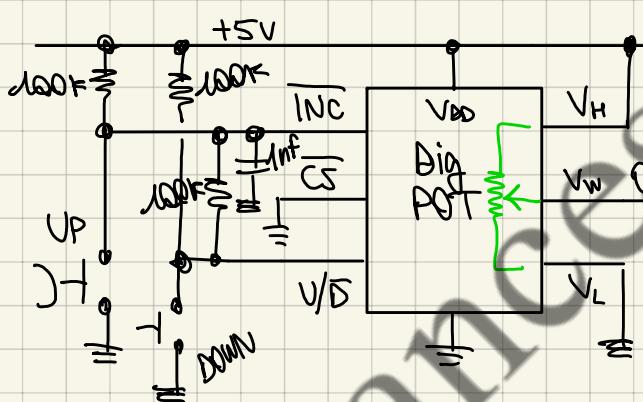
This configuration is not that handy bcz to increment we have to press the button while to decrement we have to switch the depositor to the floating pin and then push again the button



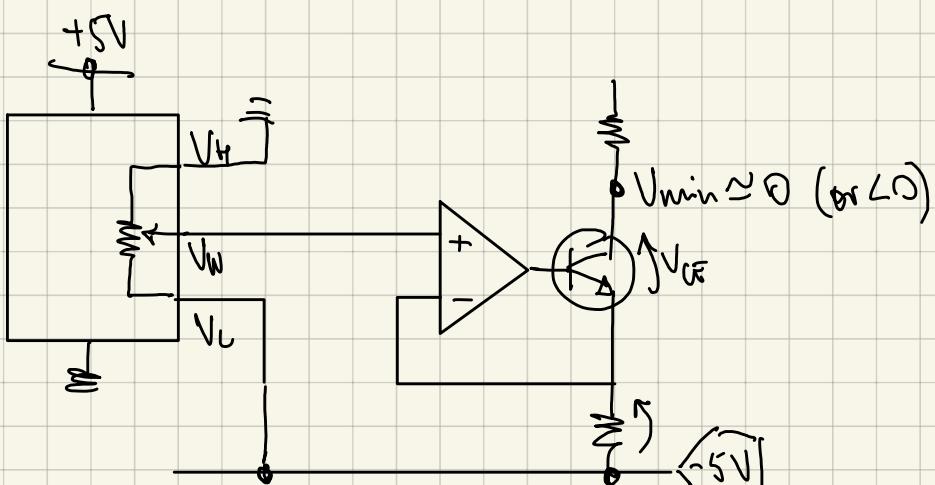
SOLUTION:



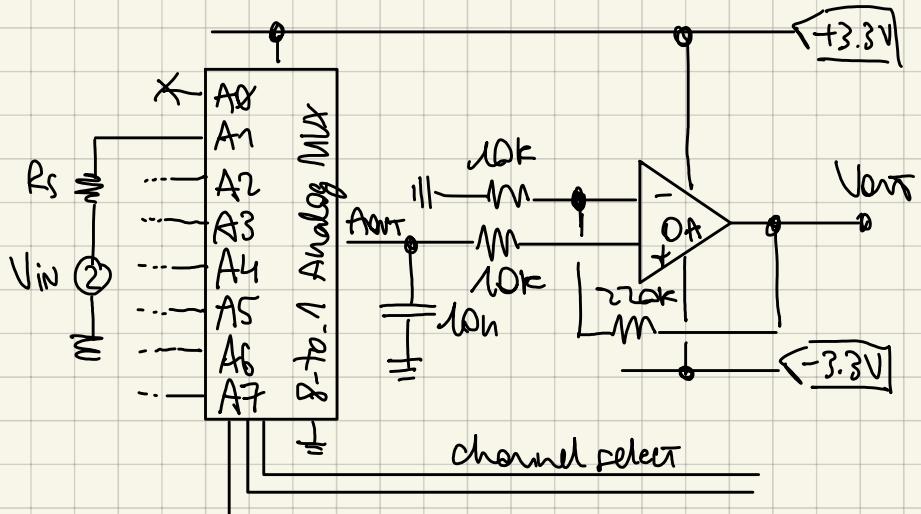
PROGRAMMABLE CURRENT GENERATOR



$$V_{DS} > 0.2V \quad V_{DS} > V_{DS} = V_{DS} - V_T \\ = 2V - 0.9 = 1.2V$$



E1:



$$R_s = 100\Omega - 1k\Omega$$

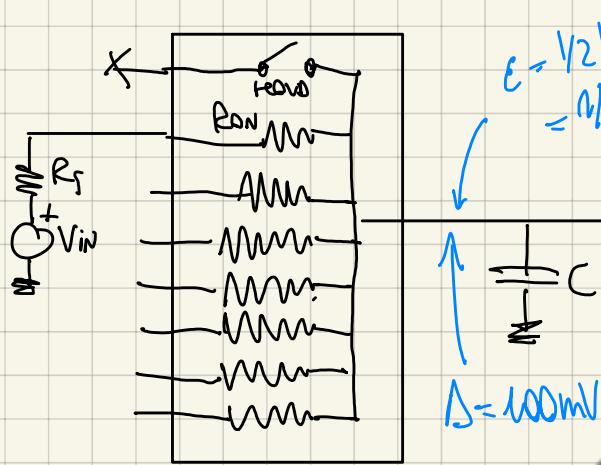
$$I_B = \ln A \cdot V_{OS} - 0.2mV$$

$$\text{MUX: } R_{ON} = 5-50\Omega$$

$$R_{OFF} = 2M\Omega - 20M\Omega$$

$$I_{VOLTAGE} = 5\mu A$$

- 2) Compute sampling and hold times for 12 bit resolution and $V_{IN,MAX} = \pm 50mV$ and specify if they are max or min values

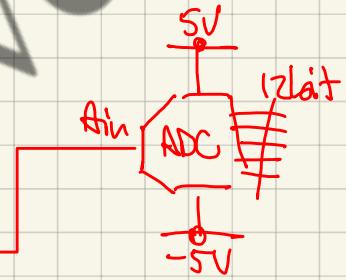


$$E = \frac{1}{2} L_{SB} = \frac{1}{2} 2.4mV = 1.2mV$$

$$G = 1 + R_2/R_1 = 23$$

$$\Delta = 100mV$$

$$L_{SB} = \frac{5V}{2^{11}} = 2.4mV$$



$$FJR = \pm 5V$$

$$L_{SB} = \frac{5V}{2^{11}} = 2.4mV$$

one bit is left for the sign

$$T_{Sampling} \geq t_{req} = T_{max} \ln \left(\frac{\Delta}{E} \right)$$

$$\text{Worst-case: } t_{req,min} = T_{max} \ln \left(\frac{\Delta_{max}}{E_{min}} \right) = (R_s, \text{max} + R_{ON, \text{mix}}) C_H (1 + \cancel{t_{req}}) \ln \left(\frac{100mV}{52\mu V} \right)$$

$$= 10\mu s \cdot 7.5 = 75\mu s$$

$$T_{Sampling} \approx 100\mu s \geq t_{req,min} = 75\mu s$$

we compute the drop:

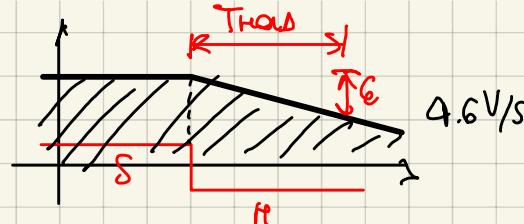
$$\frac{dV}{dt} = \frac{I_{VOLTAGE, tot}}{C_H}$$



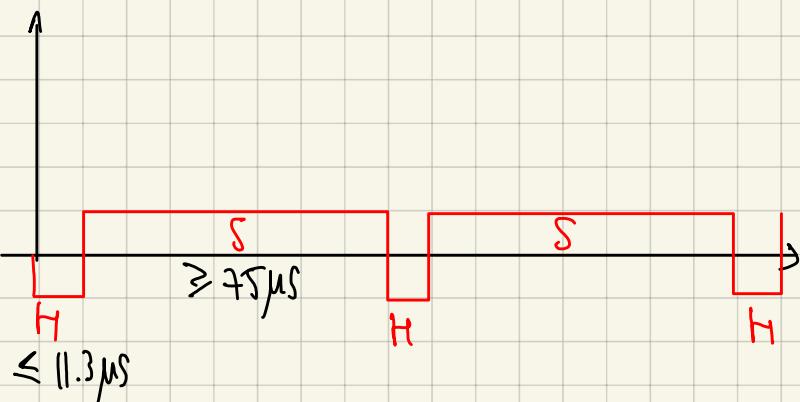
9 generators in total

$$\rightarrow \text{INTEGRATE, TOT} = 9 \cdot 5 \text{nA} + I_B = 46 \text{nA}$$

$$\frac{dV}{dt} = \frac{46 \text{nA}}{10 \text{nF}} = 4.6 \frac{\text{V}}{\text{s}}$$



$$T_{\text{read}} \leq \frac{e}{\frac{dV}{dt}_{\text{drop}}} = \frac{52 \mu\text{V}}{4.6 \text{V/S}} = 11.3 \mu\text{s}$$

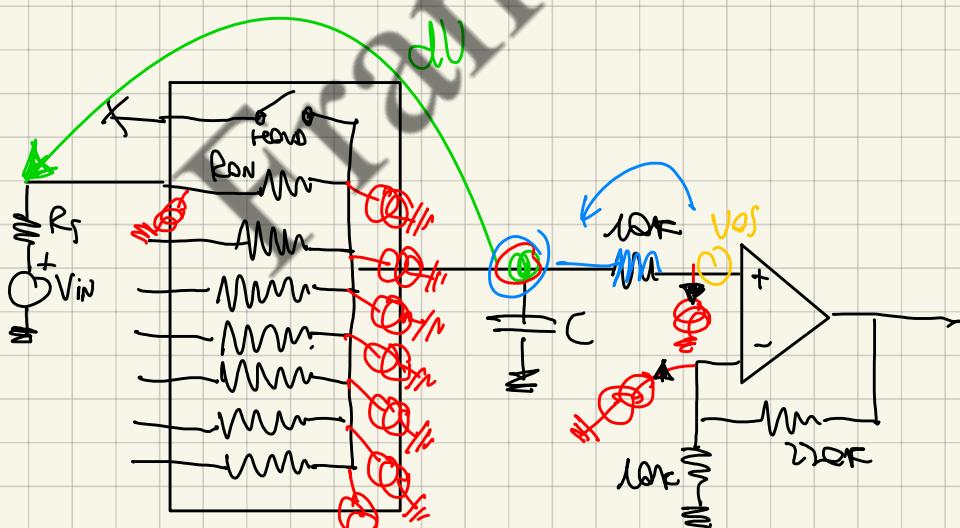


$$T_{\text{conv, ADC}} \leq T_{\text{read}} = 11.3 \mu\text{s}$$

$$T_s = \frac{1}{f_s} = (T_{\text{reading}} + T_{\text{read}}) = 96.3 \mu\text{s} \approx 90 \mu\text{s} \rightarrow f_{s,\text{MAX}} \leq 11 \text{ kSps}$$

$$f_{\text{MAX,signal}} \leq \frac{f_s}{2} = 5 \text{ kHz} \quad \leftarrow \text{max freq @ which the circuit will operate}$$

③ Compute all static errors and properly add them to compute the total output error in LSBs



$$dV = V_{in,\text{max}} \cdot \frac{R_{\text{fb, max}} + R_{\text{ON, max}}}{R_f + R_{\text{ON}} + \left(\frac{R_{\text{off}} + R_f}{6} \right)} = \pm 50 \text{ mV} \cdot \frac{1050}{105 + \frac{2M}{6}} = \pm 0.16 \text{ mV} = \pm 160 \mu\text{V}$$

for the denominator we can choose the minimum or the nominal values

$$\Delta V = \left(9I_{V\text{average}} + I_0 \right) \frac{(R_s + R_{on})}{\max} \left| \frac{R_{off} + R_{on}}{6} \right| = \pm 46 \text{nA} \left\{ 1050 \parallel 3 \text{M}\Omega \right\} \approx \pm 48 \mu\text{V}$$

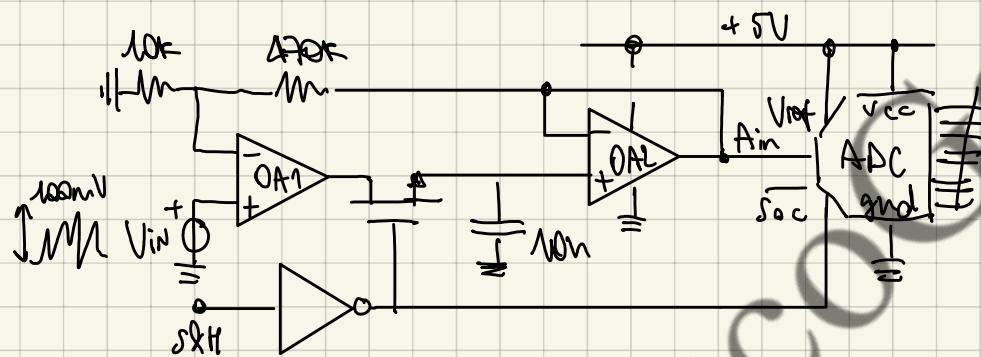
$$\Delta V = +I_0 \cdot 10\text{k}\Omega = 1 \text{nA} \cdot 10\text{k}\Omega = -10 \mu\text{V} \quad \text{input}$$

$$\Delta V = V_{os} \cdot G = \pm 0.2 \text{mV} \cdot 23 = \pm 4.6 \text{mV} \quad \text{output}$$

$$\Delta V = I_0 \cdot 220\text{k}\Omega = -1 \text{nA} \cdot 220\text{k}\Omega = +220 \mu\text{V} \quad \text{output}$$

$$\begin{aligned} E_{\text{tot}} &= (\pm 0.16 \text{ mV} \pm 48 \mu\text{V} - 10 \mu\text{V}) \cdot G \pm 4.6 \text{ mV} + 220 \mu\text{V} = \\ &= (\pm 20 \mu\text{V} - 10 \mu\text{V}) \cdot 23 \pm 4.6 \text{ mV} + 220 \mu\text{V} = \\ &\approx \pm 4.6 \text{ mV} \pm 4.6 \text{ mV} \approx \pm 9.2 \text{ mV} \end{aligned}$$

E2:



OpAmp1:
 $A_o = 100 \text{dB} = 10^5$
 $G_BWP = 100 \text{MHz}$
 MRR: $R_{on} < 100 \Omega$
 $V_T = 0.9 \text{V}$
 ADC: 12 bit

(a) Compute the acquisition time

$$G_1 = 1 + \frac{470\text{k}\Omega}{10\text{k}\Omega} = 48 \Rightarrow A_{im} = V_{in} \cdot 48 = 4.8 \text{V}$$

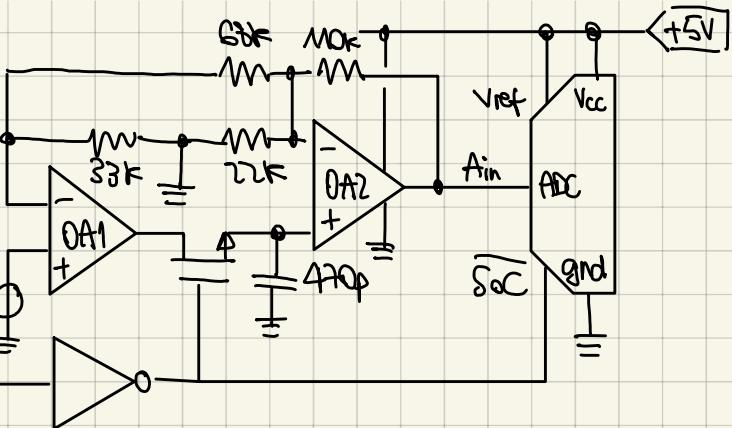
since OA2 is a buffer, it means that we want to store 9.9V in the capacitor

In order to store 4.9V in the capacitor, since $V_T = 0.9 \text{V} \Rightarrow V_G = 5.6 \text{V}$

\Rightarrow in order to properly close the switch $V_G \geq 5.6 \text{V}$

DO IT AT HOME!

E3



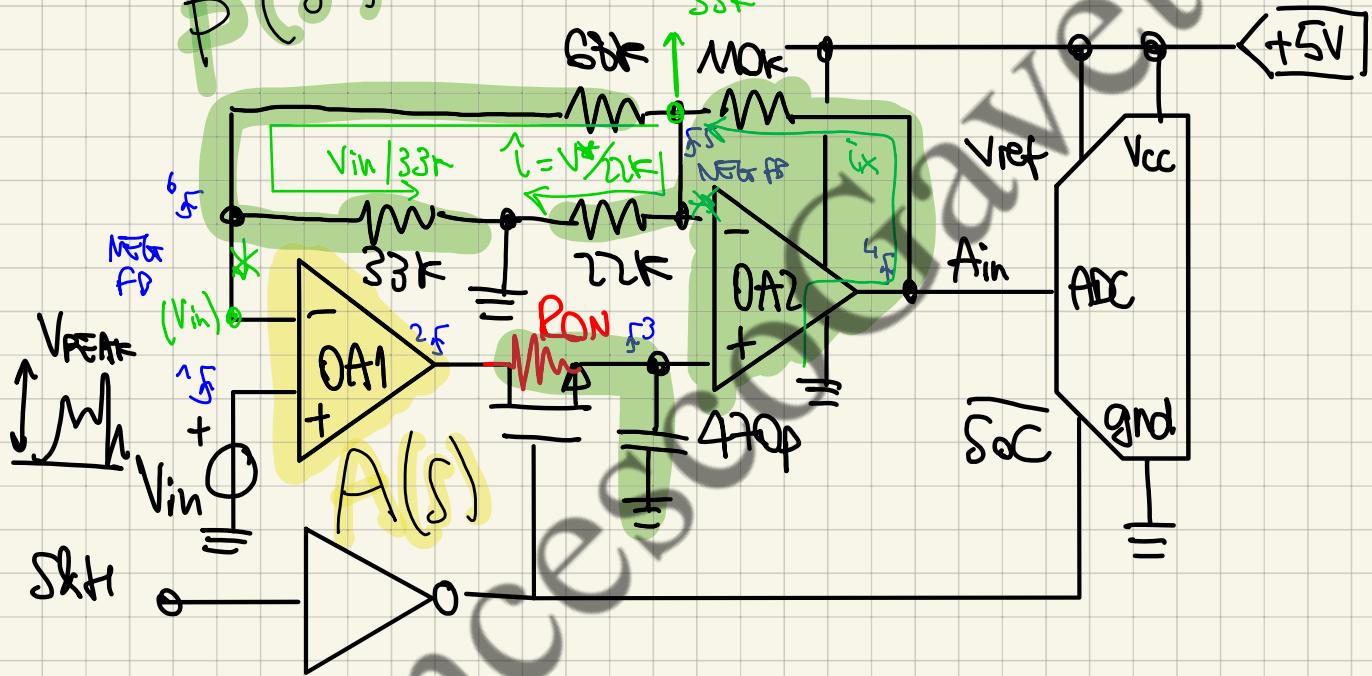
OpAmps: $A_0 = 100dB$ $G_{BW}P = 50MHz$
 ADC: 10 bit, $T_{CONN} = 1\mu s$
 MOSFET: $V_t = 0.8V$, $R_{ON} < 80\Omega$
 $C_{DS} = C_{GD} - C_{GS} < 1\mu F$

① Compute the ideal gain of the S/H during sampling and its bandwidth

sampling phase $\rightarrow V_Q$ is sufficiently high to close the switch

$B(s)$

$$V^* = \frac{V_{in}}{33k} (33k + 67k)$$



$$\hat{V} = \frac{V^*}{22k} = \frac{V_{in}}{22k} \left(1 + \frac{67k}{33k} \right)$$

$$\hat{i}_x = \frac{V_{in}}{33k} + \frac{V_{in}}{22k} \left(1 + \frac{67k}{33k} \right) \approx V_{in} \left(\frac{1}{33k} + \frac{3}{22k} \right) = \frac{V_{in}}{6k}$$

$$V_{out} = V^* + i_x \cdot 10k \approx 3V_{in} + \frac{V_{in}}{6k} \cdot 110k$$

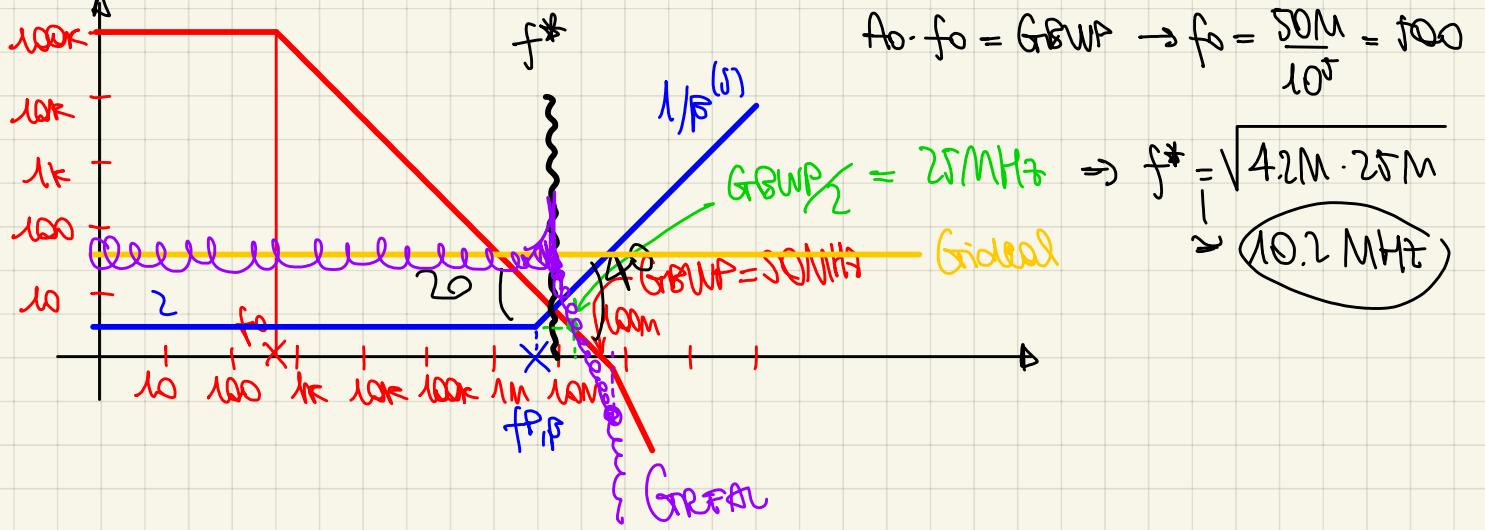
$$G_{ideal} \approx 21$$

$A(s)$: Open-Loop OpAmp

$\beta(s)$: pole $\cdot 1 \cdot \frac{33k}{67k}$
 ↓ pole
 ↓ gain
 of $R_{ON} G_H$ of the block

$$\text{pole } \beta = \frac{1}{2\pi R_{ON} G_H} = 4.2 \text{ MHz}$$

$$\text{attenuation } \frac{1}{\beta(\omega)} = \frac{67}{33} \approx 2$$



$$\begin{aligned}
 PM &= 180 - \tan^{-1}\left(\frac{f^*}{f_0}\right) - \tan^{-1}\left(\frac{f^*}{f_{P,B}}\right) - \tan^{-1}\left(\frac{f^*}{f_{P,P}}\right) \\
 &\approx 180 - 90^\circ - \tan^{-1}\left(\frac{10.2\text{M}}{4.2\text{M}}\right) - \tan^{-1}\left(\frac{10.2\text{M}}{50\text{M}}\right) \\
 &\approx 90^\circ - 68^\circ - 11.5^\circ \approx 11^\circ
 \end{aligned}$$