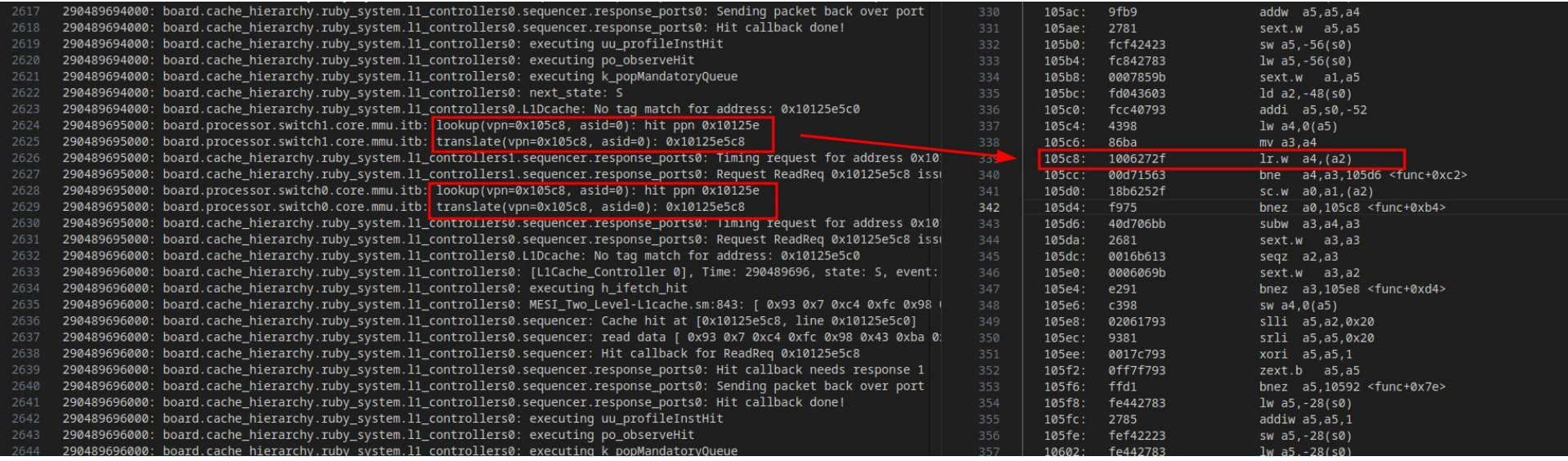
Analisi aapprofondita ATOMIC

Debug flags utilizzati

TLB, TLBVerbose, PageTableWalker, RubySlicc, RubyCache, RubyCacheTrace, RubyHitMiss, RubyPort, RubySequencer, RubyGenerated, LLSC

riga 2624: entrambi i thread arrivano alla prima load reserve ed entrambe hanno come next state S (poiché quella pagina contiene un'istruzione, quindi non da modificare)



```
149 {
150 }
151
152 void
153 Sequencer::llscLoadLinked(const Addr claddr)
154 {
155     fatal_if(m_dataCache_ptr == NULL,
156         "%s must have a dcache object to support LLSC requests.", name());
157     AbstractCacheEntry *line = m_dataCache_ptr->lookup(claddr);
158     if (line) {
159         line->setLocked(m_version);
160         DPRINTF(LLSC, "LLSC Monitor - inserting load linked - "
161                       "addr=0x%lx - cpu=%u\n", claddr, m_version);
162     }
163 }
```

```
void gem5::ruby::Sequencer::llscLoadLinked(gem5::Addr claddr)

Places the cache line address into the global monitor
tagged with this Sequencer object's version id.
```

riga 2672: il core 1 è il primo ad acquisire il lock con:

- Issuing LL
- LLSC Monitor - inserting load linked - addr=0x10107d880 - cpu=1
  ^-- riga 153 gem5/src/mem/ruby/system/Sequencer.cc
- Cache hit at [0x10107d8b4, line 0x10107d880]
- next_state: M

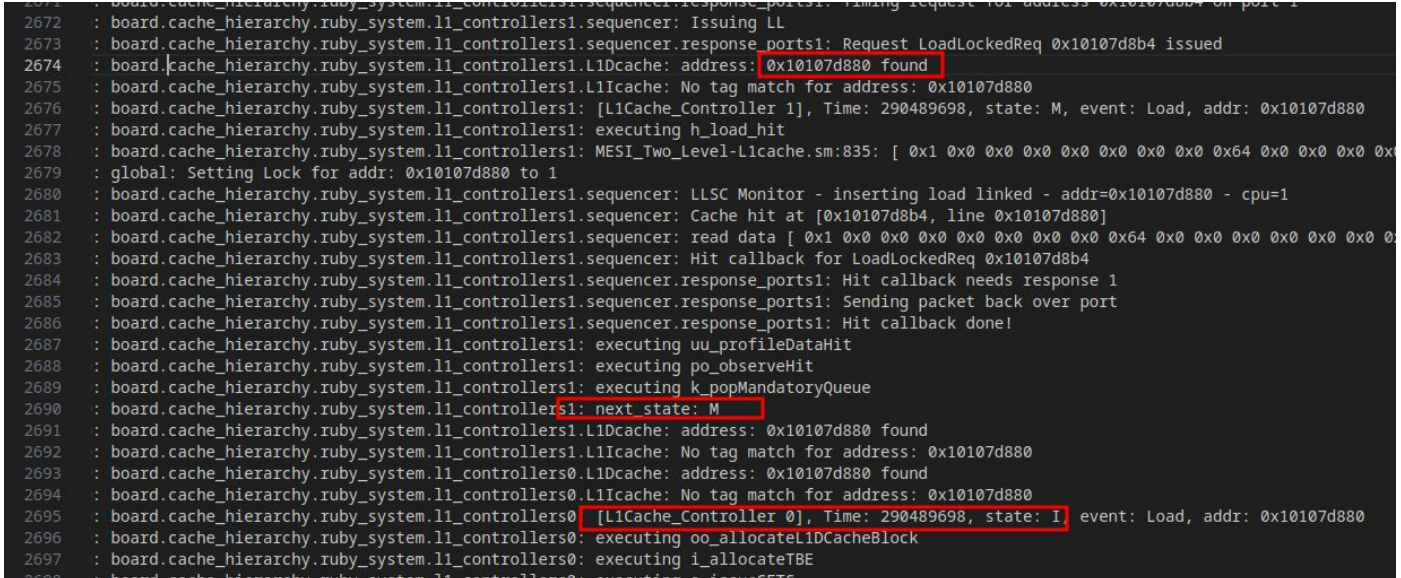
(qui next state è M, nonostante basti lo stato S, poiché già era in M prima della load e non ha ancora fatto la write back)

N.B: qualsiasi richiesta la inoltra ad entrambe le cache (ICache e DCache), semplicemente una delle 2 fallirà.

```
2661  290489696000: board.cache_hierarchy.ruby_system.l1_controllers1.L1Dcache: No tag match for address: 0x10125e5c0
2662  290489697000: board.processor.switch0.core.mmu.dtb: lookup(vpn=0x8a8b4, asid=0): hit ppn 0x10107d
2663  290489697000: board.processor.switch0.core.mmu.dtb: translate(vpn=0x8a8b4, asid=0): 0x10107d8b4
2664  290489697000: board.processor.switch0.core.isa: [cid:0]: Reserved address 10107d8b4.
2665  290489697000: board.cache_hierarchy.ruby_system.l1_controllers0.sequencer.response_ports1: Timing request for address 0x10107d8b4 on port 1
2666  290489697000: board.cache_hierarchy.ruby_system.l1_controllers0.sequencer: Issuing LL
2667  290489697000: board.cache_hierarchy.ruby_system.l1_controllers0.sequencer.response_ports1: Request LoadLockedReq 0x10107d8b4 issued
2668  290489697000: board.processor.switch1.core.mmu.dtb: lookup(vpn=0x8a8b4, asid=0): hit ppn 0x10107d
2669  290489697000: board.processor.switch1.core.mmu.dtb: translate(vpn=0x8a8b4, asid=0): 0x10107d8b4
2670  290489697000: board.processor.switch1.core.isa: [cid:1]: Reserved address 10107d8b4.
2671  290489697000: board.cache_hierarchy.ruby_system.l1_controllers1.sequencer.response_ports1: Timing request for address 0x10107d8b4 on port 1
2672  290489697000: board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: Issuing LL
2673  290489697000: board.cache_hierarchy.ruby_system.l1_controllers1.sequencer.response_ports1: Request LoadLockedReq 0x10107d8b4 issued
2674  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1.L1Dcache: address: 0x10107d880 found
2675  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1.L1Icache: No tag match for address: 0x10107d880
2676  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1: [L1Cache_Controller 1], Time: 290489698, state: M, event: Load, addr: 0x10107d880
2677  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1: executing h_load_hit
2678  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1: MESI_Two_Level-L1cache.sm:835: [ 0x1 0x0 0x0 0x0 0x0 0x0 0x0 0x0 0x64 0x0 0x0 0x0 0x0 0x0 0x0
2679  290489698000: global: Setting Lock for addr: 0x10107d880 to 1
2680  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: LLSC Monitor - inserting load linked - addr=0x10107d880 - cpu=1
2681  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: Cache hit at [0x10107d8b4, line 0x10107d880]
2682  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: read data [ 0x1 0x0 0x0 0x0 0x0 0x0 0x0 0x0 0x64 0x0 0x0 0x0 0x0 0x0 0x0 0x0 0x75 0x
2683  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: Hit callback for LoadLockedReq 0x10107d8b4
2684  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1.sequencer.response_ports1: Hit callback needs response 1
2685  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1.sequencer.response_ports1: Sending packet back over port
2686  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1.sequencer.response_ports1: Hit callback done!
2687  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1: executing uu_profileDataHit
2688  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1: executing po_observeHit
2689  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1: executing k_popMandatoryQueue
2690  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1: next_state: M
2691  290489698000: board.cache_hierarchy.ruby_system.l1_controllers1.L1Dcache: address: 0x10107d880 found
```

il core 1 ottiene il lock a seguito della found (a riga 2674) per la pagina della shared variable. Successivamente a riga 2676 c'è la risposta (come detto prima in stato M)

mentre a riga 2693 anche il core 0 fa address found, ma a riga 2695 gli ritorna con lo stato I



riga 2744 a riga 2749: il core 1 finisce con la store conditional

riga 2766-2767 e riga 2777 (con next state M)

```
2743  : board.cache_hierarchy.ruby_system.l1_controllers1.L1Dcache: No tag match for address: 0x10125e5c0
2744  : board.processor.switch1.core.mmu.dtb: lookup(vpn=0x8a8b4, asid=0): hit ppn 0x10107d
2745  : board.processor.switch1.core.mmu.dtb: translate(vpn=0x8a8b4, asid=0): 0x10107d8b4
2746  : board.processor.switch1.core.isa: [cid:1]: load_reservation_addrs empty? no.
2747  : board.processor.switch1.core.isa: [cid:1]: addr = 10107d880.
2748  : board.processor.switch1.core.isa: [cid:1]: last locked addr = 10107d880.
2749  : board.processor.switch1.core.isa: [cid:1]: SC success! Current locked addr = fffffffffffffc0.
2750  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer.response_ports1: Timing request for address 0x1010
2751  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: Issuing SC
2752  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer.response_ports1: Request StoreCondReq 0x10107d8b4
2753  : board.cache_hierarchy.ruby_system.l2_controllers0: MESI_Two_Level-L2cache.sm:373: Addr: 0x10107d880 State: MT
2754  : board.cache_hierarchy.ruby_system.l2_controllers0: [L2Cache_Controller 0], Time: 290489704, state: MT, event:
2755  : board.cache_hierarchy.ruby_system.l2_controllers0: executing b_forwardRequestToExclusive
2756  : board.cache_hierarchy.ruby_system.l2_controllers0: executing uu_profileMiss
2757  : board.cache_hierarchy.ruby_system.l2_controllers0: executing set_setMRU
2758  : board.cache_hierarchy.ruby_system.l2_controllers0: executing jj_popL1RequestQueue
2759  : board.cache_hierarchy.ruby_system.l2_controllers0: next_state: MT_IIB
2760  : board.cache_hierarchy.ruby_system.l1_controllers1.L1Dcache: address: 0x10107d880 found
2761  : board.cache_hierarchy.ruby_system.l1_controllers1.L1Icache: No tag match for address: 0x10107d880
2762  : board.cache_hierarchy.ruby_system.l1_controllers1: [L1Cache_Controller 1], Time: 290489704, state: M, event: S
2763  : board.cache_hierarchy.ruby_system.l1_controllers1: executing hh_store_hit
2764  : board.cache_hierarchy.ruby_system.l1_controllers1: MESI_Two_Level-L1cache.sm:860: [ 0x1 0x0 0x0 0x0 0x0 0x0 0x
2765  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: LLSC Monitor - clearing due to store conditional
2766  : global: Testing Lock for addr: 0x10107d880 cur 1 con 1
2767  : global: Clear Lock for addr: 0x10107d880
2768  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: Cache hit at [0x10107d8b4, line 0x10107d880]
2769  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: set data [ 0x1 0x0 0x0 0x0 0x0 0x0 0x0 0x0 0x64 0
2770  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: Hit callback for StoreCondReq 0x10107d8b4
2771  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer.response_ports1: Hit callback needs response 1
2772  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer.response_ports1: Sending packet back over port
2773  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer.response_ports1: Hit callback done!
2774  : board.cache_hierarchy.ruby_system.l1_controllers1: executing uu_profileDataHit
2775  : board.cache_hierarchy.ruby_system.l1_controllers1: executing po_observeHit
2776  : board.cache_hierarchy.ruby_system.l1_controllers1: executing k_popMandatoryQueue
2777  : board.cache_hierarchy.ruby_system.l1_controllers1: next_state: M
2778  : board.cache_hierarchy.ruby_system.l1_controllers1.L1Dcache: address: 0x10107d880 found
2779  : board.cache_hierarchy.ruby_system.l1_controllers1.L1Icache: No tag match for address: 0x10107d880
2780  : board.processor.switch1.core.mmu.itb: lookup(vpn=0x105d4, asid=0): hit ppn 0x10125e
```

```
818  ISA::handleLockedWrite(const RequestPtr &req, Addr cacheBlockMask)
819  {
820      Addr& load_reservation_addr = load_reservation_addrs[tc->contextId()];
821      bool lr_addr_empty = (load_reservation_addr == INVALID_RESERVATION_ADDR);
822
823      // Normally RISC-V uses zero to indicate success and nonzero to indicate
824      // failure (right now only 1 is reserved), but in gem5 zero indicates
825      // failure and one indicates success, so here we conform to that (it should
826      // be switched in the instruction's implementation)
827
828      DPRINTF(LLSC, "[cid:%d]: load_reservation_addrs empty? %s.\n",
829              req->contextId(),
830              lr_addr_empty ? "yes" : "no");
831      if (!lr_addr_empty) {
832          DPRINTF(LLSC, "[cid:%d]: addr = %x.\n", req->contextId(),
833                  req->getPaddr() & cacheBlockMask);
834          DPRINTF(LLSC, "[cid:%d]: last locked addr = %x.\n", req->contextId(),
835                  load_reservation_addr & cacheBlockMask);
836      }
837      if (lr_addr_empty ||
838              (load_reservation_addr & cacheBlockMask)
839              != ((req->getPaddr() & cacheBlockMask))) {
840          req->setExtraData(0);
841          int stCondFailures = tc->readStCondFailures();
842          tc->setStCondFailures(++stCondFailures);
843          if (stCondFailures % WARN_FAILURE == 0) {
844              warn("%i: context %d: %d consecutive SC failures.\n",
845                      curTick(), tc->contextId(), stCondFailures);
846          }
847
848          // Must clear any reservations
849          load_reservation_addr = INVALID_RESERVATION_ADDR;
850
851          return false;
852      }
853      if (req->isUncacheable()) {
854          req->setExtraData(2);
855      }
856
857      // Must clear any reservations
858      load_reservation_addr = INVALID_RESERVATION_ADDR;
859
860      DPRINTF(LLSC, "[cid:%d]: SC success! Current locked addr = %x.\n",
861              req->contextId(), load_reservation_addr & cacheBlockMask);
862      return true;
863  }
```

riga 828
gem5/src/arch/riscv/isa.cc

riga 2899: il core 0 fa miss sulla entry di cache della shared variable, quindi recupera la entry che adesso può tornare in stato S (riga 2909) (viene fatta fare la write back dal core 1)

in gem5/src/mem/ruby/system/RubyPort.cc a riga 454 ho la callback dell'evento di ricerca stimolato dalla miss

```
452  RubyPort::ruby_hit_callback(PacketPtr pkt)
453  {
454      DPRINTF(RubyPort, "Hit callback for %s 0x%x\n", pkt->cmdString(),
455              pkt->getAddr());
456
457      // The packet was destined for memory and has not yet been turned
458      // into a response
459      assert(system->isMemAddr(pkt->getAddr()) || system->isDeviceMemAddr
460      assert(pkt->isRequest());
461
462      // First we must retrieve the request port from the sender State
463      RubyPort::SenderState *senderState =
464          safe_cast<RubyPort::SenderState *>(pkt->popSenderState());
465      MemResponsePort *port = senderState->port;
466      assert(port != NULL);
467      delete senderState;
468
469      port->hitCallback(pkt);
470
471      trySendRetries();
472  }
```

```
2895  : board.cache_hierarchy.ruby_system.l1_controllers0: MESI_Two_Level-L1cache.sm:814: 0x10107d880
2896  : board.cache_hierarchy.ruby_system.l1_controllers0: executing hx_load_hit
2897  : board.cache_hierarchy.ruby_system.l1_controllers0: MESI_Two_Level-L1cache.sm:851: [ 0x1 0x0 0x0 0x0 0x0 0x0 0x0 0x0 0x64 0x0 0x0 0x0 0x0 0x0 0x0 0x
2898  : global: Setting Lock for addr: 0x10107d880 to 0
2899  : board.cache_hierarchy.ruby_system.l1_controllers0.sequencer: LLSC Monitor - inserting load linked - addr=0x10107d880 - cpu=0
2900  : board.cache_hierarchy.ruby_system.l1_controllers0.sequencer: Cache miss at [0x10107d8b4, line 0x10107d880]
2901  : board.cache_hierarchy.ruby_system.l1_controllers0.sequencer: read data [ 0x1 0x0 0x0 0x0 0x0 0x0 0x0 0x0 0x64 0x0 0x0 0x0 0x0 0x0 0x0 0x0 0x75 0x7f
2902  : board.cache_hierarchy.ruby_system.l1_controllers0.sequencer: Hit callback for LoadLockedReq 0x10107d8b4
2903  : board.cache_hierarchy.ruby_system.l1_controllers0.sequencer.response_ports1: Hit callback needs response 1
2904  : board.cache_hierarchy.ruby_system.l1_controllers0.sequencer.response_ports1: Sending packet back over port
2905  : board.cache_hierarchy.ruby_system.l1_controllers0.sequencer.response_ports1: Hit callback done!
2906  : board.cache_hierarchy.ruby_system.l1_controllers0: executing s_deallocateTBE
2907  : board.cache_hierarchy.ruby_system.l1_controllers0: executing o_popIncomingResponseQueue
2908  : board.cache_hierarchy.ruby_system.l1_controllers0: executing kd_wakeUpDependents
2909  : board.cache_hierarchy.ruby_system.l1_controllers0: next_state: S
2910  : board.cache_hierarchy.ruby_system.l1_controllers0.L1Dcache: address: 0x10107d880 found
2911  : board.cache_hierarchy.ruby_system.l1_controllers0.L1Icache: No tag match for address: 0x10107d880
2912  : board.cache_hierarchy.ruby_system.l2_controllers0: [L2Cache_Controller 0], Time: 290489715, state: MT_IIB, event: WB_Data, addr: 0x10107d880
```

```
4719  : board.processor.switch0.core.mmu.itb: lookup(vpn=0x105c8, asid=0): hit ppn 0x10125e
4720  : board.processor.switch0.core.mmu.itb: translate(vpn=0x105c8, asid=0): 0x10125e5c8
4721  : board.cache_hierarchy.ruby_system.l1_controllers0.sequencer.response_ports0: Timing request
```

riga 4719: il core 0 raggiunge la load reserve
riga 4757: il core 0 fa lookup sulla shared variable
riga 4784: il core 0 riesce a concludere la load reserve con la riga

N.B: da qui in poi quando prendo la load reserve sulla shared variable lo stato è S e va in stato M solo dopo la store conditional (riga 5122)

```
4757  : board.processor.switch0.core.mmu.dtb: lookup(vpn=0x8a8b4, asid=0): hit ppn 0x10107d
4758  : board.processor.switch0.core.mmu.dtb: translate(vpn=0x8a8b4, asid=0): 0x10107d8b4
4759  : board.processor.switch0.core.isa: [cid:0]: Reserved address 10107d8b4.
4760  : board.cache_hierarchy.ruby_system.l1_controllers0.sequencer.response_ports1: Timing request for address 0x10107d8b4 on port 1
4761  : board.cache_hierarchy.ruby_system.l1_controllers0.sequencer: Issuing LL
4762  : board.cache_hierarchy.ruby_system.l1_controllers0.sequencer.response_ports1: Request LoadLockedReq 0x10107d8b4 issued
4763  : board.cache_hierarchy.ruby_system.l1_controllers1.L1Dcache: No tag match for address: 0x10125e580
4764  : board.cache_hierarchy.ruby_system.l1_controllers1: [L1Cache_Controller 1], Time: 290489810, state: S, event: Ifetch, addr: 0x10125e580
4765  : board.cache_hierarchy.ruby_system.l1_controllers1: executing h_ifetch_hit
4766  : board.cache_hierarchy.ruby_system.l1_controllers1: MESI_Two_Level-L1cache.sm:843: [ 0xe1 0xd3 0x23 0x22 0x4 0xfe 0xb5 0xa8 0x83 0x27 0xc
4767  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: Cache hit at [0x10125e5bc, line 0x10125e580]
4768  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: read data [ 0xe1 0xd3 0x23 0x22 0x4 0xfe 0xb5 0xa8 0x83 0x27 0xc4 0xfc 0x23
4769  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: Hit callback for ReadReq 0x10125e5bc
4770  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer.response_ports0: Hit callback needs response 1
4771  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer.response_ports0: Sending packet back over port
4772  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer.response_ports0: Hit callback done!
4773  : board.cache_hierarchy.ruby_system.l1_controllers1: executing uu_profileInstHit
4774  : board.cache_hierarchy.ruby_system.l1_controllers1: executing po_observeHit
4775  : board.cache_hierarchy.ruby_system.l1_controllers1: executing k_popMandatoryQueue
4776  : board.cache_hierarchy.ruby_system.l1_controllers1: next_state: S
4777  : board.cache_hierarchy.ruby_system.l1_controllers1.L1Dcache: No tag match for address: 0x10125e580
4778  : board.processor.switch1.core.mmu.dtb: lookup(vpn=0x3fd4660c00, asid=0): hit ppn 0x2781c4
4779  : board.processor.switch1.core.mmu.dtb: translate(vpn=0x3fd4660c00, asid=0): 0x2781c4c00
4780  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer.response_ports1: Timing request for address 0x2781c4c00 on port 1
4781  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer.response_ports1: Request ReadReq 0x2781c4c00 issued
4782  : board.cache_hierarchy.ruby_system.l1_controllers0.L1Dcache: address: 0x10107d880 found
4783  : board.cache_hierarchy.ruby_system.l1_controllers0.L1Icache: No tag match for address: 0x10107d880
4784  : board.cache_hierarchy.ruby_system.l1_controllers0: [L1Cache_Controller 0], Time: 290489811, state: S, event: Load, addr: 0x10107d880
4785  : board.cache_hierarchy.ruby_system.l1_controllers0: executing h_load_hit
```

riga 5034: il core 0 sta per fare la store quindi la entry di shared variable della sua cache va da stato S a SM, invalidando così le altre cache.
Infatti a riga 5043 il core 1 si trova in stato I per quella entry

```
5031  : board.cache_hierarchy.ruby_system.l1_controllers0: [L1Cache_Controller 0], Time: 290489828, state: SM, event: Ack, addr: 0x10107d880
5032  : board.cache_hierarchy.ruby_system.l1_controllers0: executing q_updateAckCount
5033  : board.cache_hierarchy.ruby_system.l1_controllers0: executing o_popIncomingResponseQueue
5034  : board.cache_hierarchy.ruby_system.l1_controllers0: next_state: SM
5035  : board.cache_hierarchy.ruby_system.l1_controllers0.L1Dcache: address: 0x10107d880 found
5036  : board.cache_hierarchy.ruby_system.l1_controllers0.L1Icache: No tag match for address: 0x10107d880
5037  : board.cache_hierarchy.ruby_system.l1_controllers1.L1Dcache: address: 0x10107d880 found
5038  : board.cache_hierarchy.ruby_system.l1_controllers1.L1Icache: No tag match for address: 0x10107d880
5039  : board.cache_hierarchy.ruby_system.l1_controllers1: [L1Cache_Controller 1], Time: 290489828, state: S, event: Inv, addr: 0x10107d880
5040  : board.cache_hierarchy.ruby_system.l1_controllers1: executing forward_eviction_to_cpu
5041  : board.cache_hierarchy.ruby_system.l1_controllers1: executing fi_sendInvAck
5042  : board.cache_hierarchy.ruby_system.l1_controllers1: executing l_popRequestQueue
5043  : board.cache_hierarchy.ruby_system.l1_controllers1: next_state: I
5044  : board.cache_hierarchy.ruby_system.l1_controllers1.L1Dcache: address: 0x10107d880 found
5045  : board.cache_hierarchy.ruby_system.l1_controllers1.L1Icache: No tag match for address: 0x10107d880
5046  : board.cache_hierarchy.ruby_system.l1_controllers1.L1Dcache: No tag match for address: 0x10125e5c0
5047  : board.cache_hierarchy.ruby_system.l1_controllers1: [L1Cache_Controller 1], Time: 290489828, state: S, event: Ifetch, addr: 0x10125e5c0
5048  : board.cache_hierarchy.ruby_system.l1_controllers1: executing h_ifetch_hit
5049  : board.cache_hierarchy.ruby_system.l1_controllers1: MESI_Two_Level-L1cache.sm:843: [ 0x93 0x7 0xc4 0xfc 0x98 0x43 0xba 0x86 0x2f 0x27 0
5050  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: Cache hit at [0x10125e5d4, line 0x10125e5c0]
5051  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: read data [ 0x93 0x7 0xc4 0xfc 0x98 0x43 0xba 0x86 0x2f 0x27 0x6 0x10 0x6
5052  : board.cache_hierarchy.ruby_system.l1_controllers1.sequencer: Hit callback for ReadReq 0x10125e5d4
```

N.B: quando passa da stato S a M, invalida anche la entry nella propria cache, tanto è vero che la prima volta, era già in stato M e dopo i messaggi

LLSC Monitor - clearing due to store conditional - addr=0x10107d880 - cpu=0

^-- riga 180 gem5/src/mem/ruby/system/Sequencer.cc

global: Testing Lock for addr: 0x10107d880 cur 0 con 0

global: Clear Lock for addr: 0x10107d880

faceva comunque hit.

Mentre da quel punto in poi, dopo la transizione da S a M, abbiamo sempre una miss

```
173             line->clearLocked();
174             DPR
175
176         }
177     }
178
179     bool
180     Sequencer::llscStoreConditional(const Addr claddr)
181     {
182         fatal_if(m_dataCache_ptr == NULL,
183             "%s must have a dcache object to support LLSC requests.", name());
184         AbstractCacheEntry *line = m_dataCache_ptr->lookup(claddr);
185         if (!line)
186             return false;
187
188         DPRINTF(LLSC, "LLSC Monitor - clearing due to "
189                       "store conditional - "
190                       "addr=0x%lx - cpu=%u\n",
191                       claddr, m_version);
192
193         if (line->isLocked(m_version)) {
194             line->clearLocked();
195             return true;
196         } else {
197             line->clearLocked();
198             return false;
199         }
200     }
```

bool gem5::ruby::Sequencer::llscStoreConditional(gem5::Addr claddr)

Searches for cache line address in the global monitor tagged with this Sequencer object's version id. If a match is found, the entry is is erased from the global monitor.

Returns:
a boolean indicating if the line address was found.