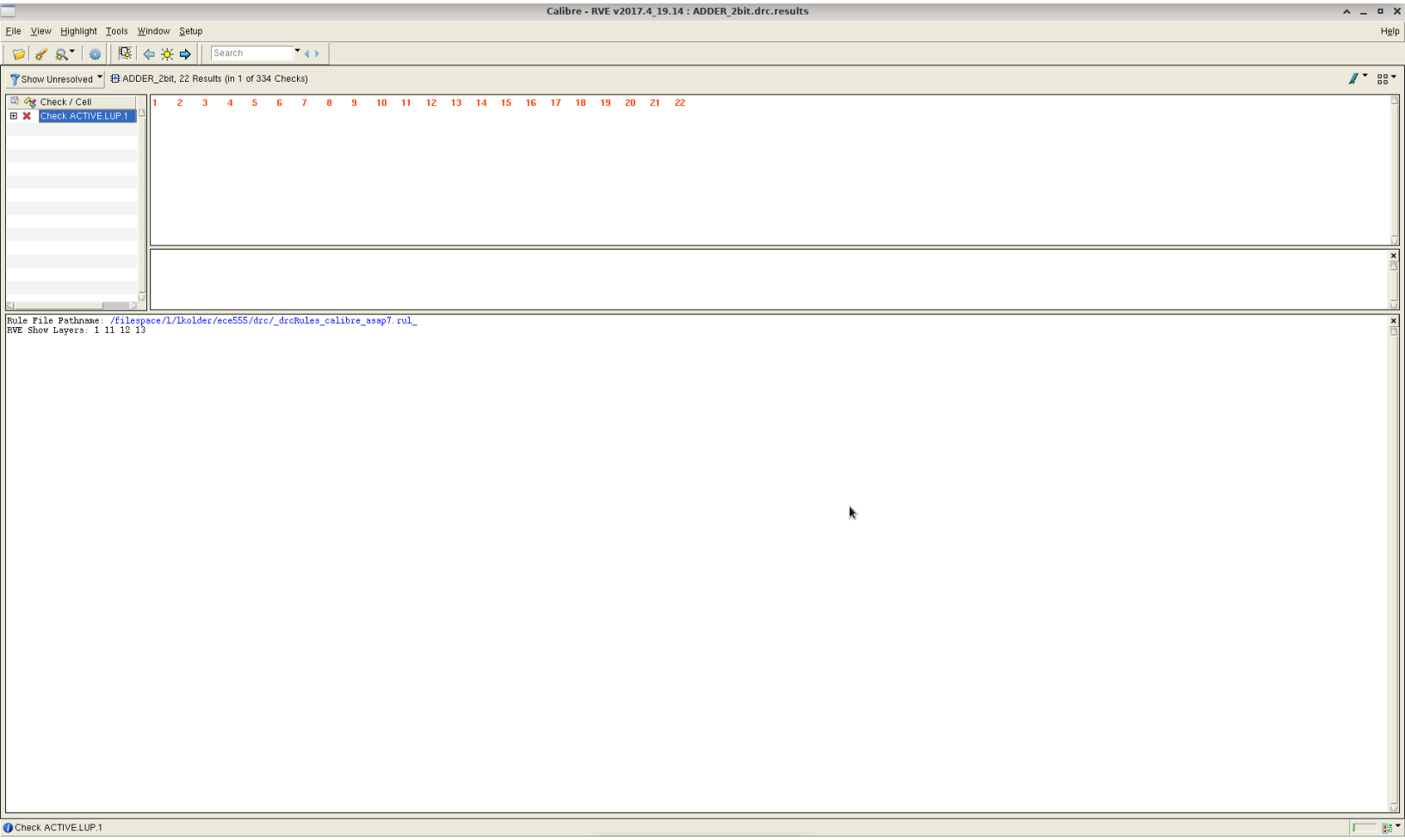
555 Final Report

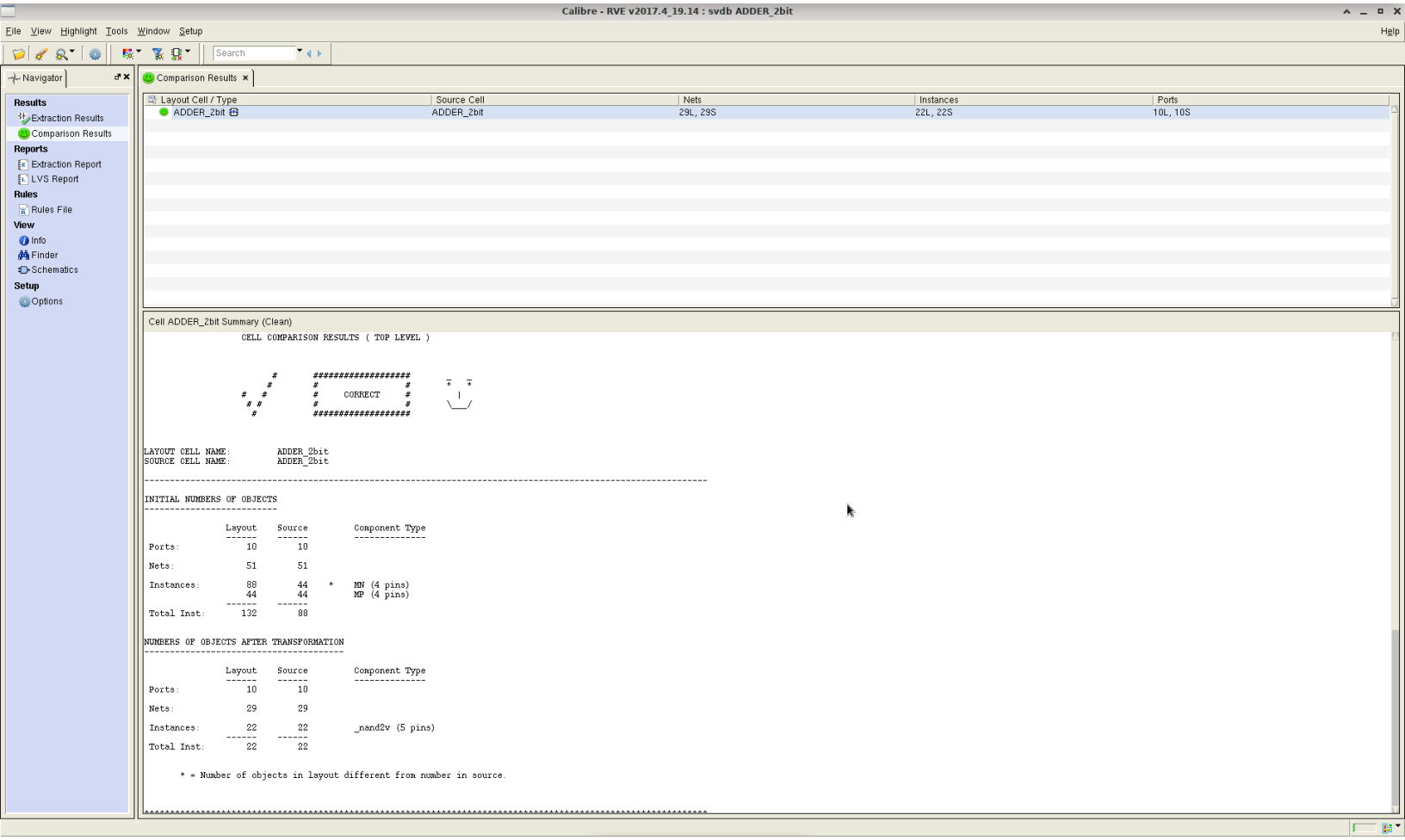
Milestone 3- KOLDER, LU

1. We believe that the layout could have been improved. There is a decent amount of unused white space due to the modularization of our design. The routing in our design is quite good and does not stand for much improvement due to only M1 and M2 layers being used. Perhaps some routes could have been decreased in length. Optimization will focus on decreasing the area of our neuron. The critical path passes through a multiplier, ADDER2, ADDER3 and finally the mux. Thanks to the modularization of our design and arrangement of cells these routing length and distance between these cells has been minimized to optimize the critical path.
2. The optimization has resulted in a decreased area of our cell by around 15%.
3. DRC and LVS screenshots of submodules and total neuron are below.
4. Calibre Extraction of neuron is below.
5. The parasitic capacitance of the pre optimized neuron was 2.2909 e-16 f and the parasitic capacitance of the optimized neuron was 2.2909 e-16 f. The parasitic capacitance did not change.
6. The final area of our design is 22.57 square micrometers

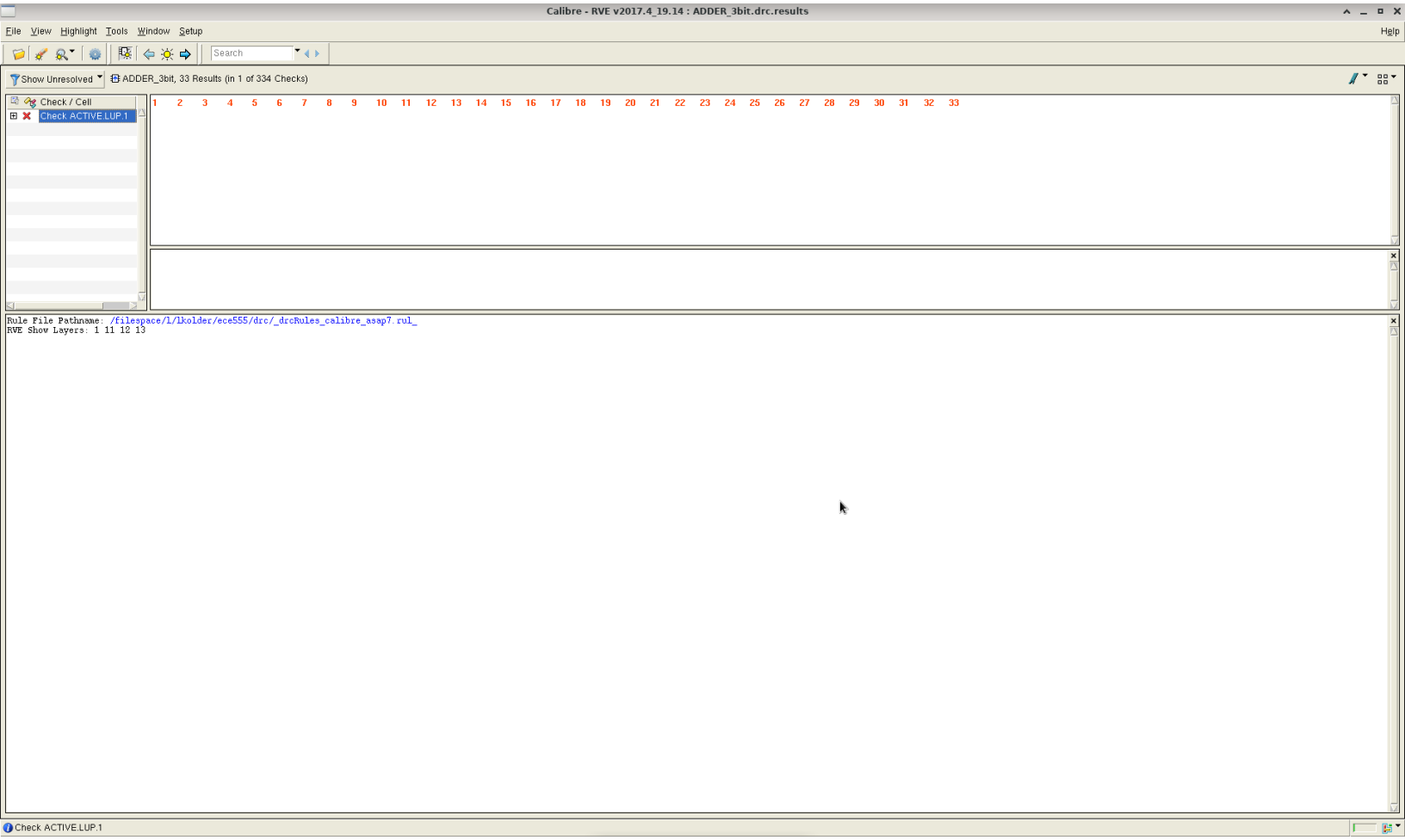
ADDER2 DRC


Calibre - RVE v2017.4_19.14 : ADDER_2bit.drc.results
File View Highlight Tools Window Setup
Help
Search
Show Unresolved
ADDER_2bit, 22 Results (in 1 of 334 Checks)
Check / Cell
Check ACTIVE.LUP.1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
Rule File Pathname: /filespace/l/lkolder/ece555/drc/_drcRules_calibre_asap7.rul_
RVE Show Layers: 1 11 12 13
Check ACTIVE.LUP.1

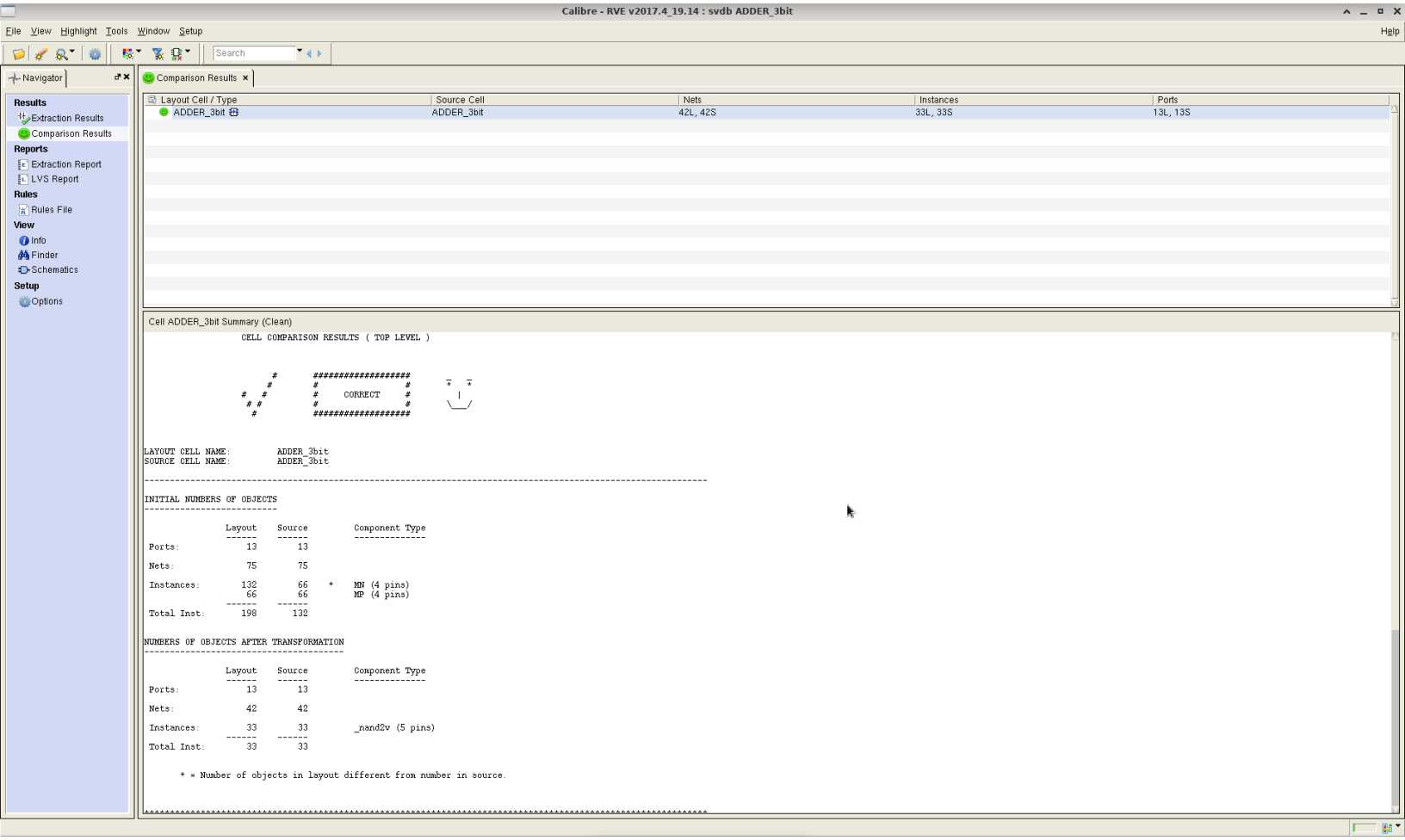
ADDER2 LVS


Calibre - RVE v2017.4_19.14 : svdb ADDER_2bit
File View Highlight Tools Window Setup
Help
Search
Navigator
Comparison Results
Results
Extraction Results
Comparison Results
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Layout Cell / Type
Source Cell
Nets
Instances
Ports
ADDER_2bit
ADDER_2bit
29L, 29S
22L, 22S
10L, 10S
Cell ADDER_2bit Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: ADDER_2bit
SOURCE CELL NAME: ADDER_2bit
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 10 10
Nets: 51 51
Instances: 88 44 * MN (4 pins)
44 44 MP (4 pins)
Total Inst: 132 88
NUMBERS OF OBJECTS AFTER TRANSFORMATION
Layout Source Component Type
Ports: 10 10
Nets: 29 29
Instances: 22 22 _nand2v (5 pins)
Total Inst: 22 22
* = Number of objects in layout different from number in source.

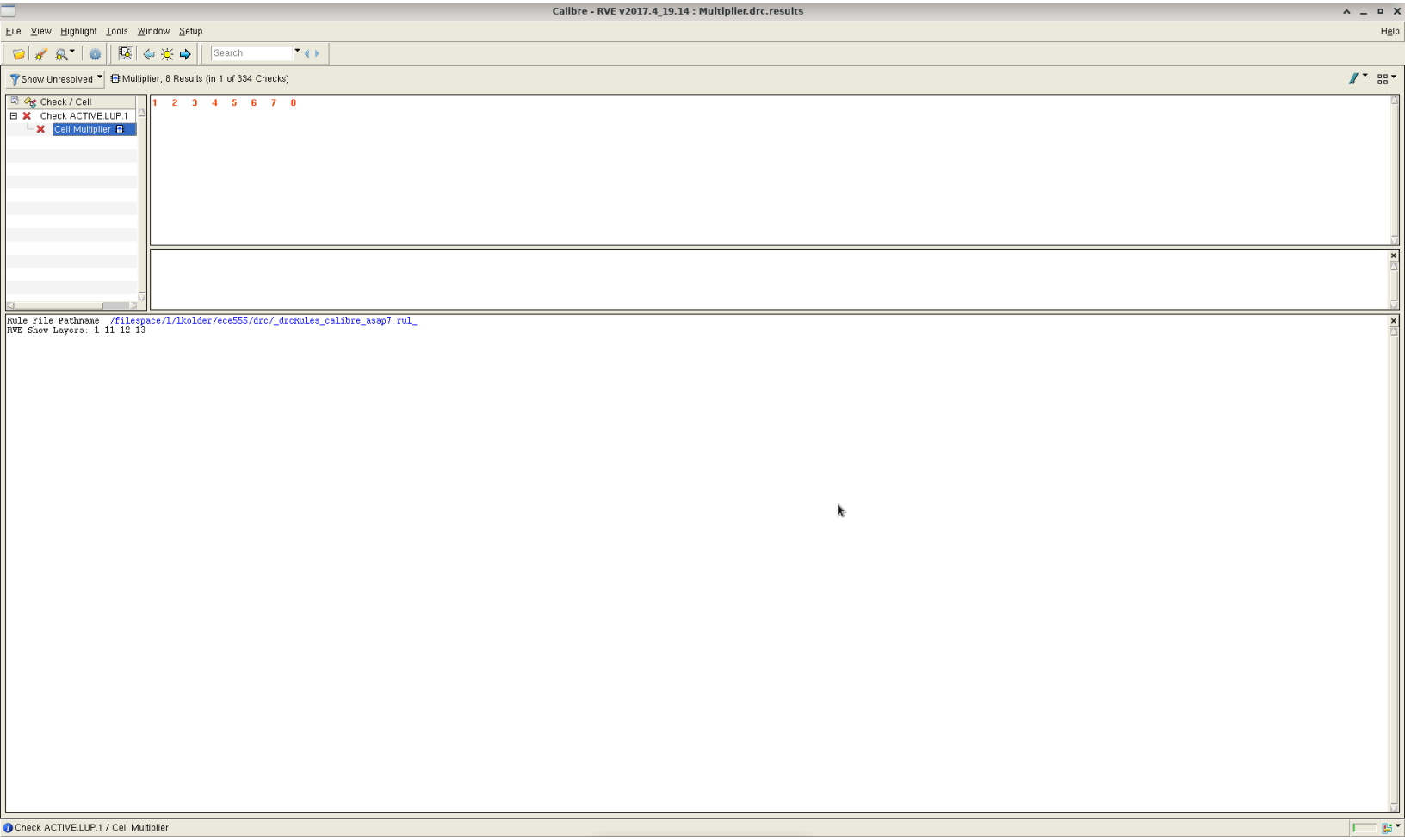
ADDER3 DRC


Calibre - RVE v2017.4_19.14 : ADDER_3bit.drc.results
File View Highlight Tools Window Setup
Help
Search
Show Unresolved
ADDER_3bit, 33 Results (in 1 of 334 Checks)
Check / Cell
Check ACTIVE.LUP.1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33
Rule File Pathname: /filespace/l/lkolder/ece555/drc/_drcRules_calibre_asap7.rul_
RVE Show Layers: 1 11 12 13
Check ACTIVE.LUP.1

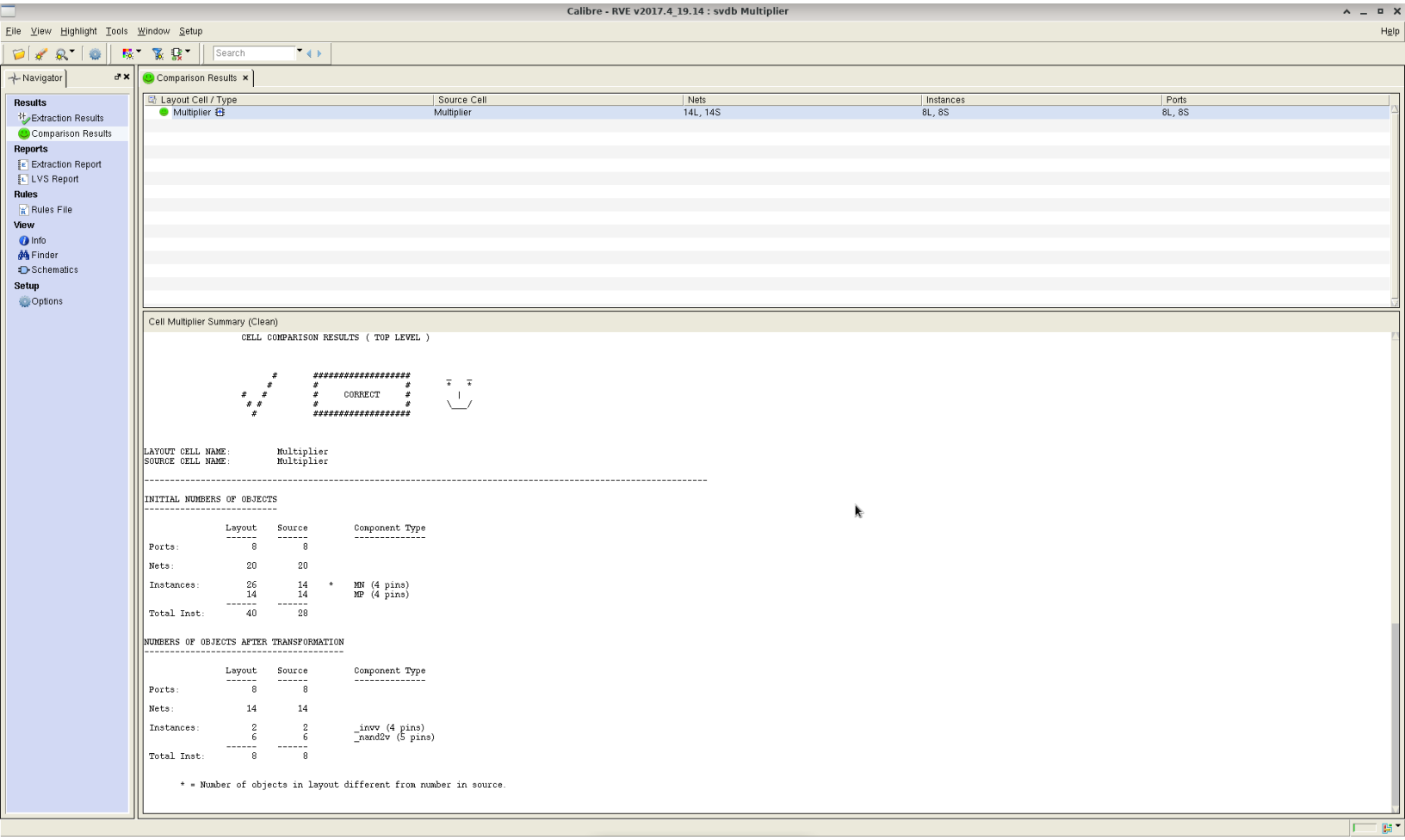
ADDER3 LVS


Calibre - RVE v2017.4_19.14 : svdb ADDER_3bit
File View Highlight Tools Window Setup
Help
Search
Navigator
Results
Extraction Results
Comparison Results
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
ADDER_3bit
ADDER_3bit
42L, 42S
33L, 33S
13L, 13S
Cell ADDER_3bit Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: ADDER_3bit
SOURCE CELL NAME: ADDER_3bit
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 13 13
Nets: 75 75
Instances: 132 66 * MN (4 pins)
66 66 MP (4 pins)
Total Inst: 198 132
NUMBERS OF OBJECTS AFTER TRANSFORMATION
Layout Source Component Type
Ports: 13 13
Nets: 42 42
Instances: 33 33 _nand2v (5 pins)
Total Inst: 33 33
* = Number of objects in layout different from number in source.

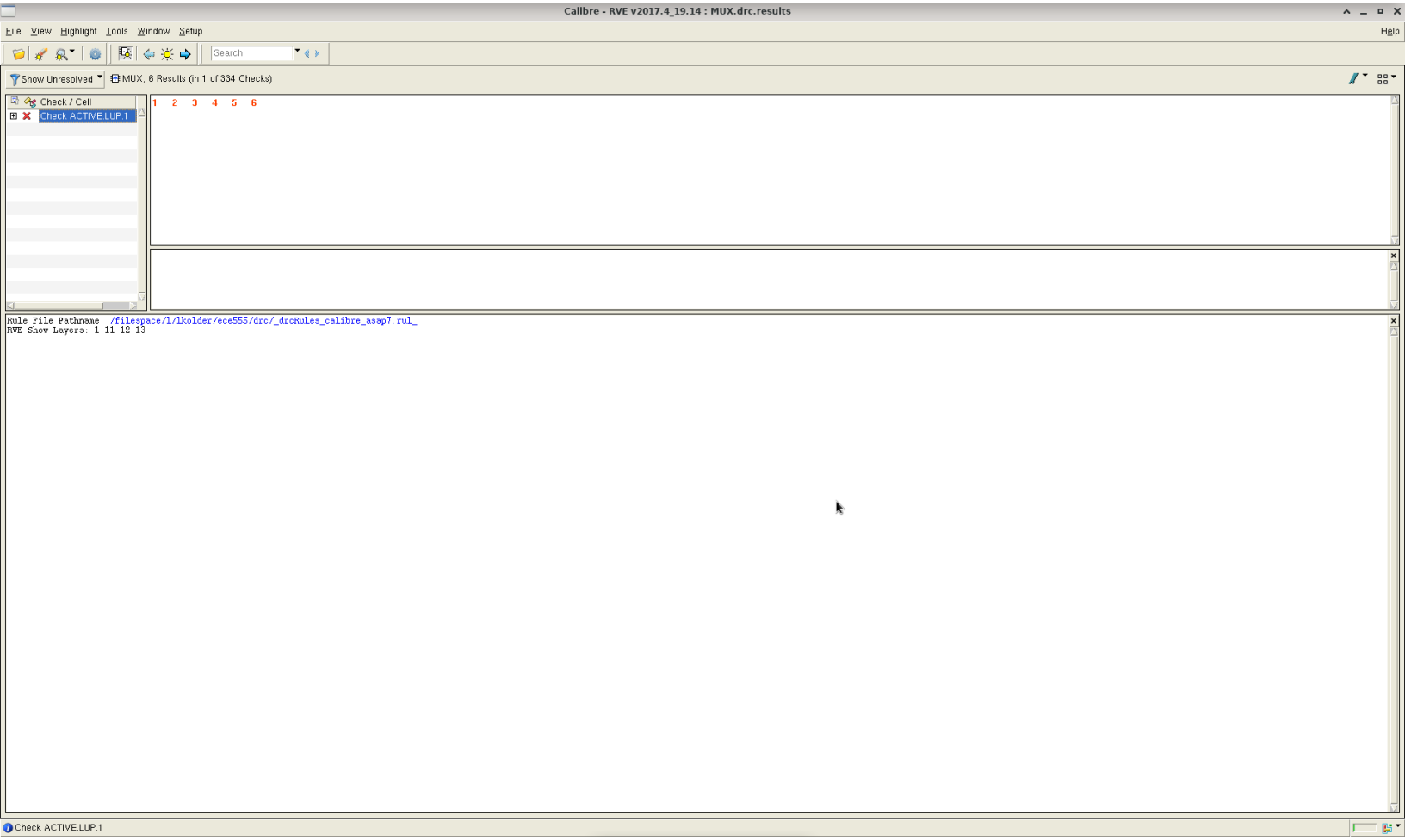
Mult DRC


Calibre - RVE v2017.4_19.14 : Multiplier.drc.results
File View Highlight Tools Window Setup
Help
Search
Show Unresolved
Multiplier, 8 Results (in 1 of 334 Checks)
Check / Cell
Check ACTIVE.LUP.1
Cell Multiplier
1 2 3 4 5 6 7 8
Rule File Pathname: /filespace/l/lkolder/ece555/drc/_drcRules_calibre_asap7.rul_
RVE Show Layers: 1 11 12 13
Check ACTIVE.LUP.1 / Cell Multiplier

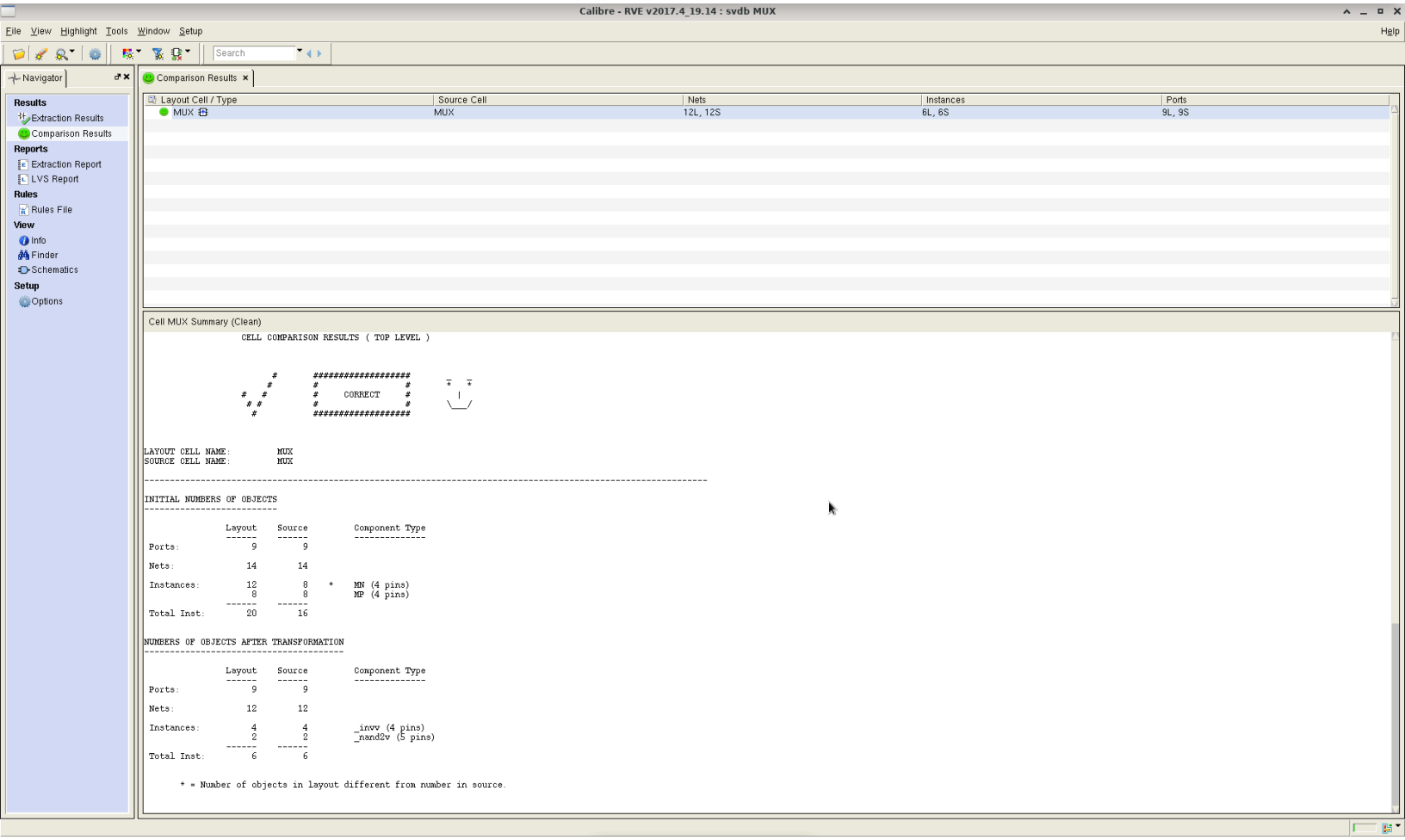
Mult LVS


Calibre - RVE v2017.4_19.14 : svdb Multiplier
File View Highlight Tools Window Setup
Help
Search
Navigator
Comparison Results
Results
Extraction Results
Comparison Results
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Layout Cell / Type
Source Cell
Nets
Instances
Ports
Multiplier
Multiplier
14L, 14S
8L, 8S
8L, 8S
Cell Multiplier Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: Multiplier
SOURCE CELL NAME: Multiplier
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 8 8
Nets: 20 20
Instances: 26 14 * MN (4 pins)
14 14 MP (4 pins)
Total Inst: 40 28
NUMBERS OF OBJECTS AFTER TRANSFORMATION
Layout Source Component Type
Ports: 8 8
Nets: 14 14
Instances: 2 2 _invv (4 pins)
6 6 _nand2v (5 pins)
Total Inst: 8 8
* = Number of objects in layout different from number in source.

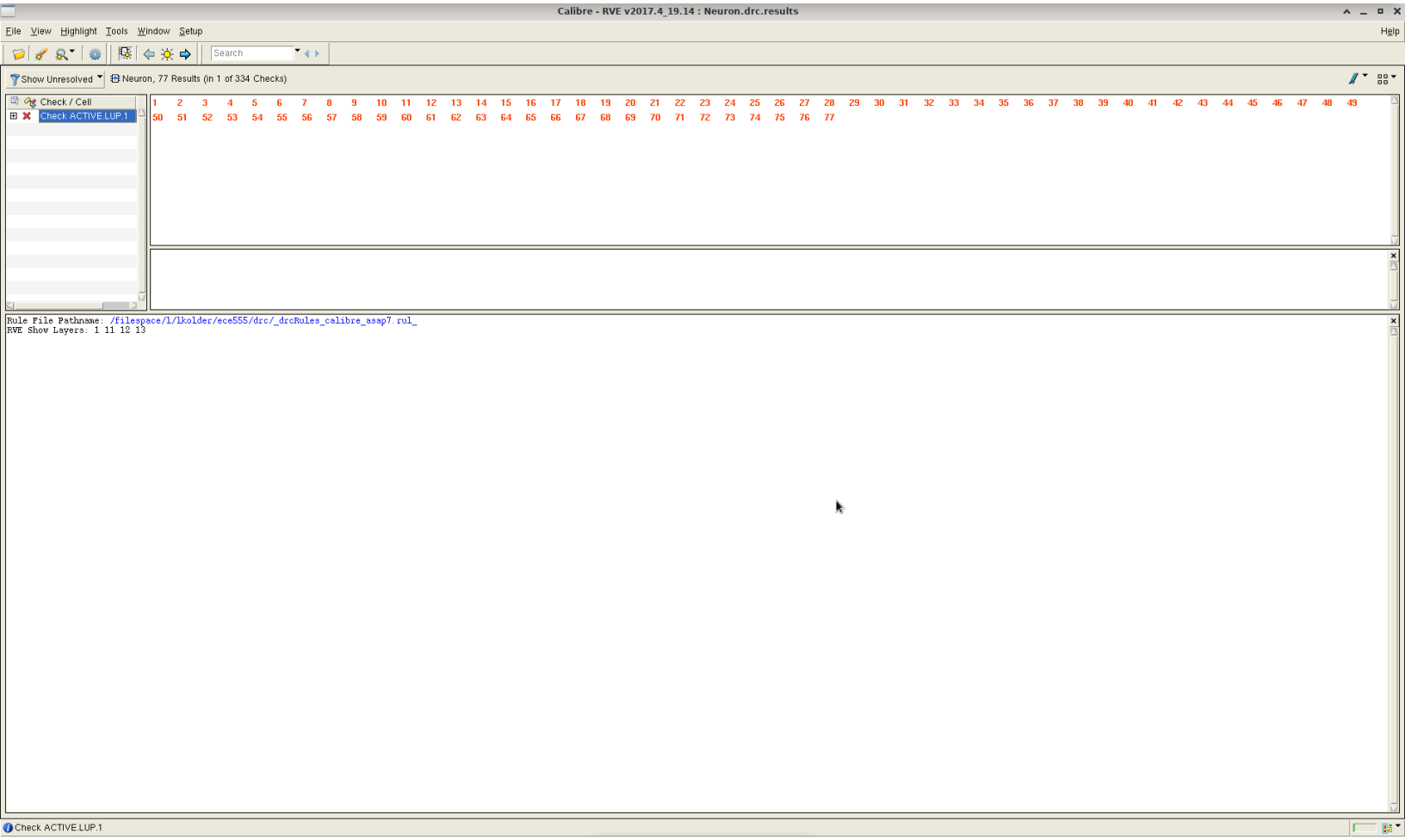
MUX DRC


Calibre - RVE v2017.4_19.14 : MUX.drc.results
File View Highlight Tools Window Setup
Help
Search
Show Unresolved
MUX, 6 Results (in 1 of 334 Checks)
Check / Cell
Check ACTIVE.LUP.1
1 2 3 4 5 6
Rule File Pathname: /filespace/l/lkolder/ece555/drc/_drcRules_calibre_asap7.rul_
RVE Show Layers: 1 11 12 13
Check ACTIVE.LUP.1

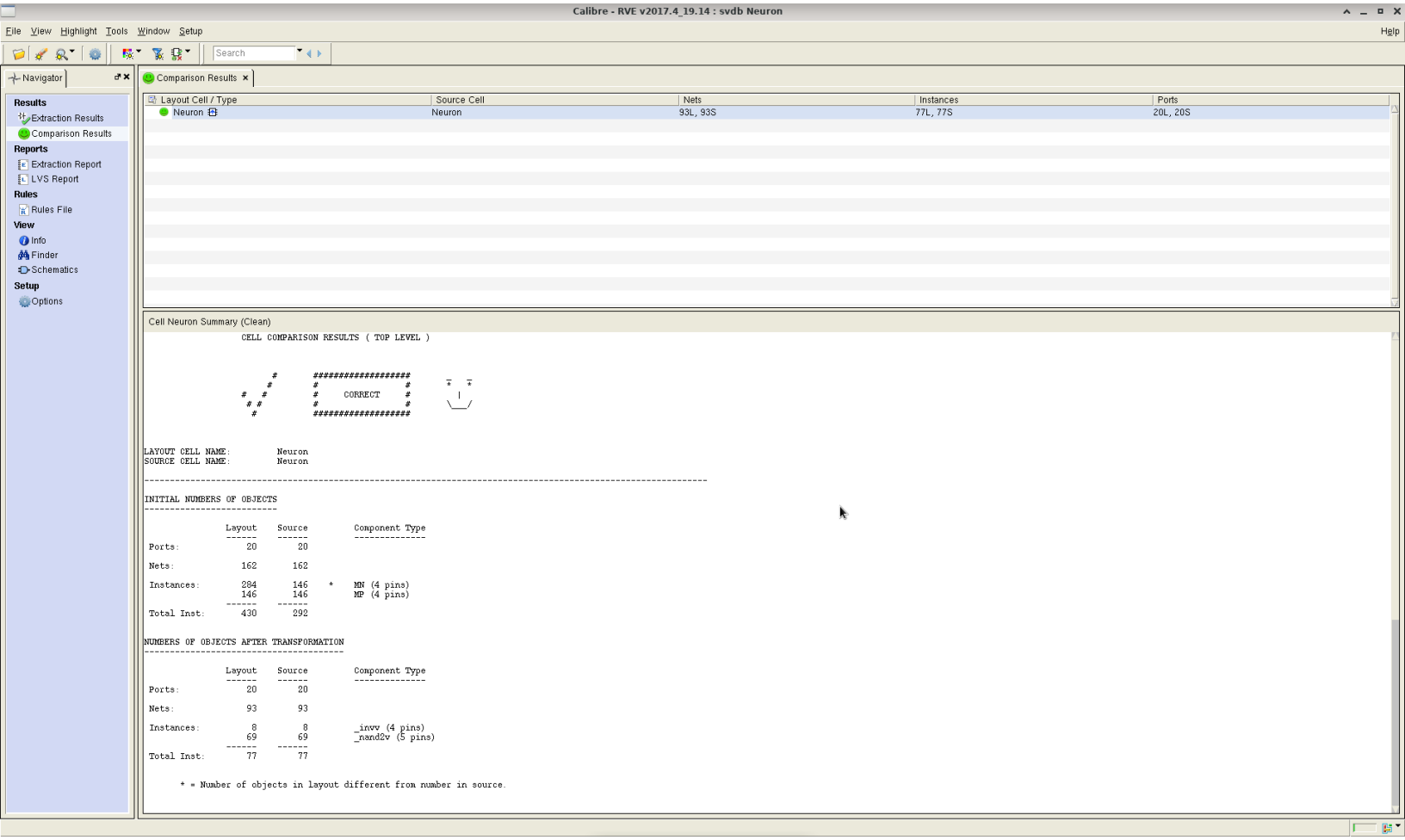
MUX LVS


Calibre - RVE v2017.4_19.14 : svdb MUX
File View Highlight Tools Window Setup
Help
Search
Navigator
Comparison Results
Results
Extraction Results
Comparison Results
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Layout Cell / Type
Source Cell
Nets
Instances
Ports
MUX
MUX
12L, 12S
6L, 6S
9L, 9S
Cell MUX Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: MUX
SOURCE CELL NAME: MUX
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 9 9
Nets: 14 14
Instances: 12 8 * MN (4 pins)
8 8 MP (4 pins)
Total Inst: 20 16
NUMBERS OF OBJECTS AFTER TRANSFORMATION
Layout Source Component Type
Ports: 9 9
Nets: 12 12
Instances: 4 4 _invv (4 pins)
2 2 _nand2v (5 pins)
Total Inst: 6 6
* = Number of objects in layout different from number in source.

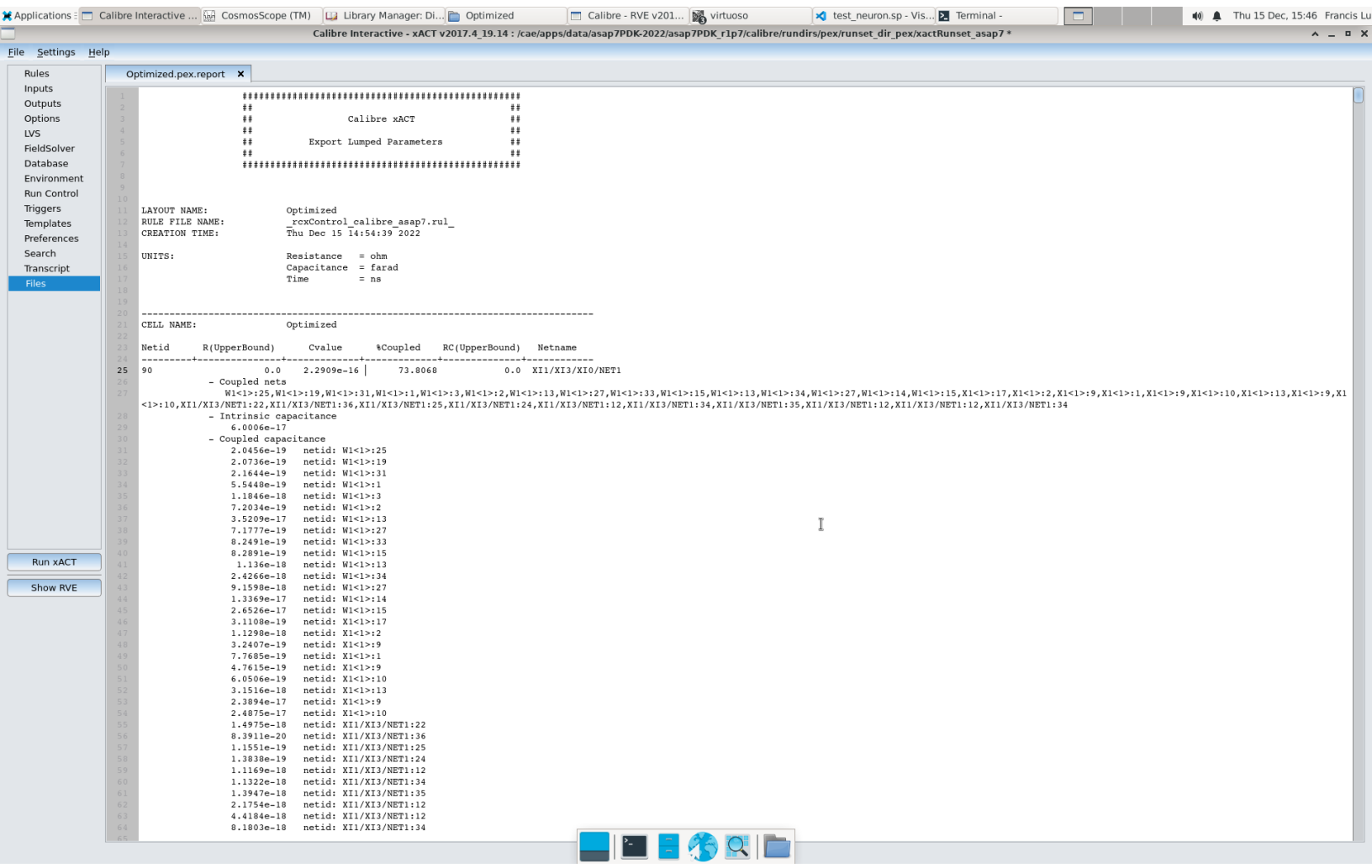
Neuron DRC


Calibre - RVE v2017.4_19.14 : Neuron.drc.results
File View Highlight Tools Window Setup
Help
Search
Show Unresolved
Neuron, 77 Results (in 1 of 334 Checks)
Check / Cell
Check ACTIVE.LUP.1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49
50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77
Rule File Pathname: /filespace/l/lkolder/ece555/drc/_drcRules_calibre_asap7.rul_
RVE Show Layers: 1 11 12 13
Check ACTIVE.LUP.1

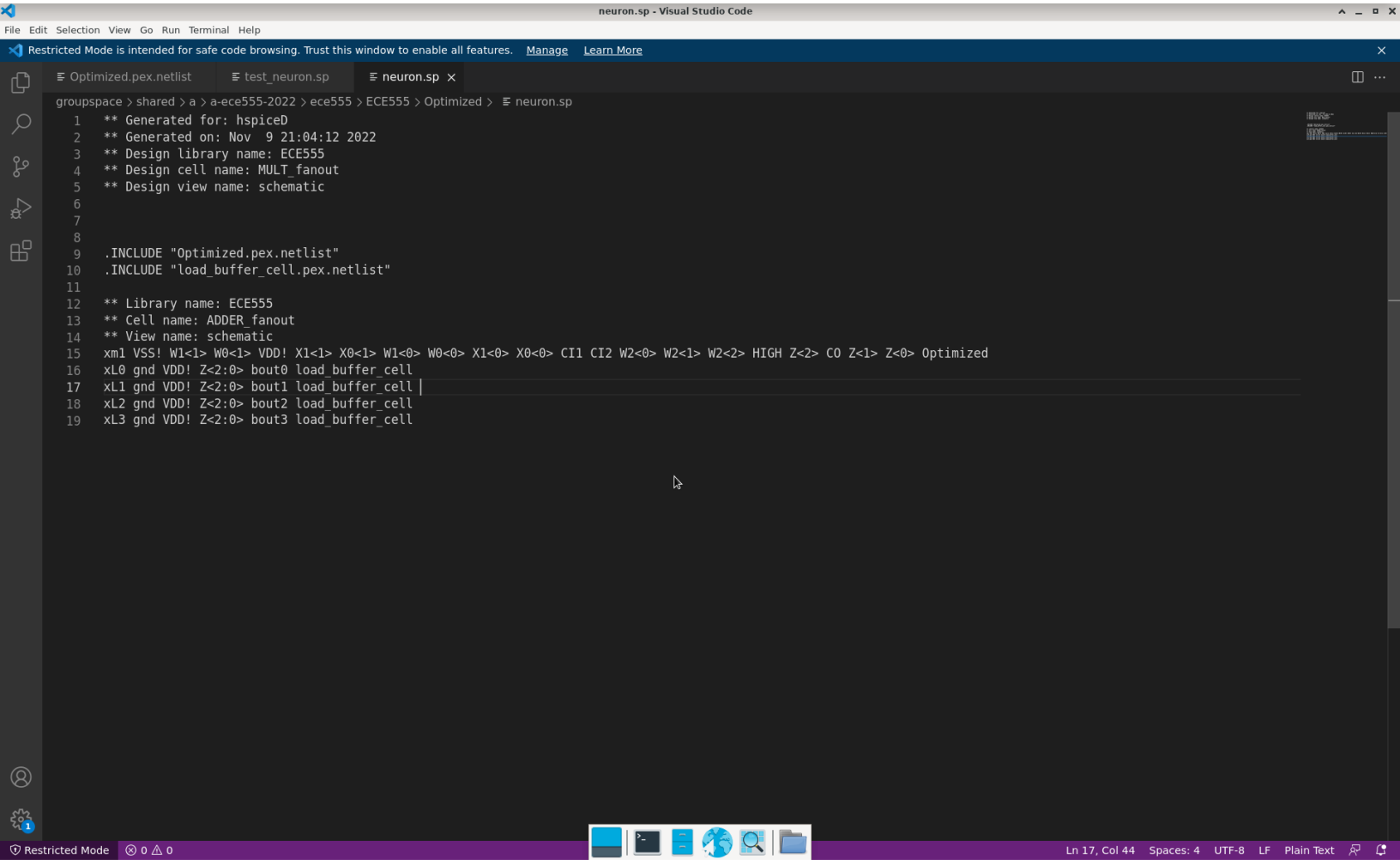
Neuron LVS


Calibre - RVE v2017.4_19.14 : svdb Neuron
File View Highlight Tools Window Setup
Help
Search
Navigator
Comparison Results
Results
Extraction Results
Comparison Results
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Layout Cell / Type
Source Cell
Nets
Instances
Ports
Neuron
Neuron
93L, 93S
77L, 77S
20L, 20S
Cell Neuron Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: Neuron
SOURCE CELL NAME: Neuron
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 20 20
Nets: 162 162
Instances: 284 146 * MN (4 pins)
146 146 MP (4 pins)
Total Inst: 430 292
NUMBERS OF OBJECTS AFTER TRANSFORMATION
Layout Source Component Type
Ports: 20 20
Nets: 93 93
Instances: 8 8 _invv (4 pins)
69 69 _nand2v (5 pins)
Total Inst: 77 77
* = Number of objects in layout different from number in source.

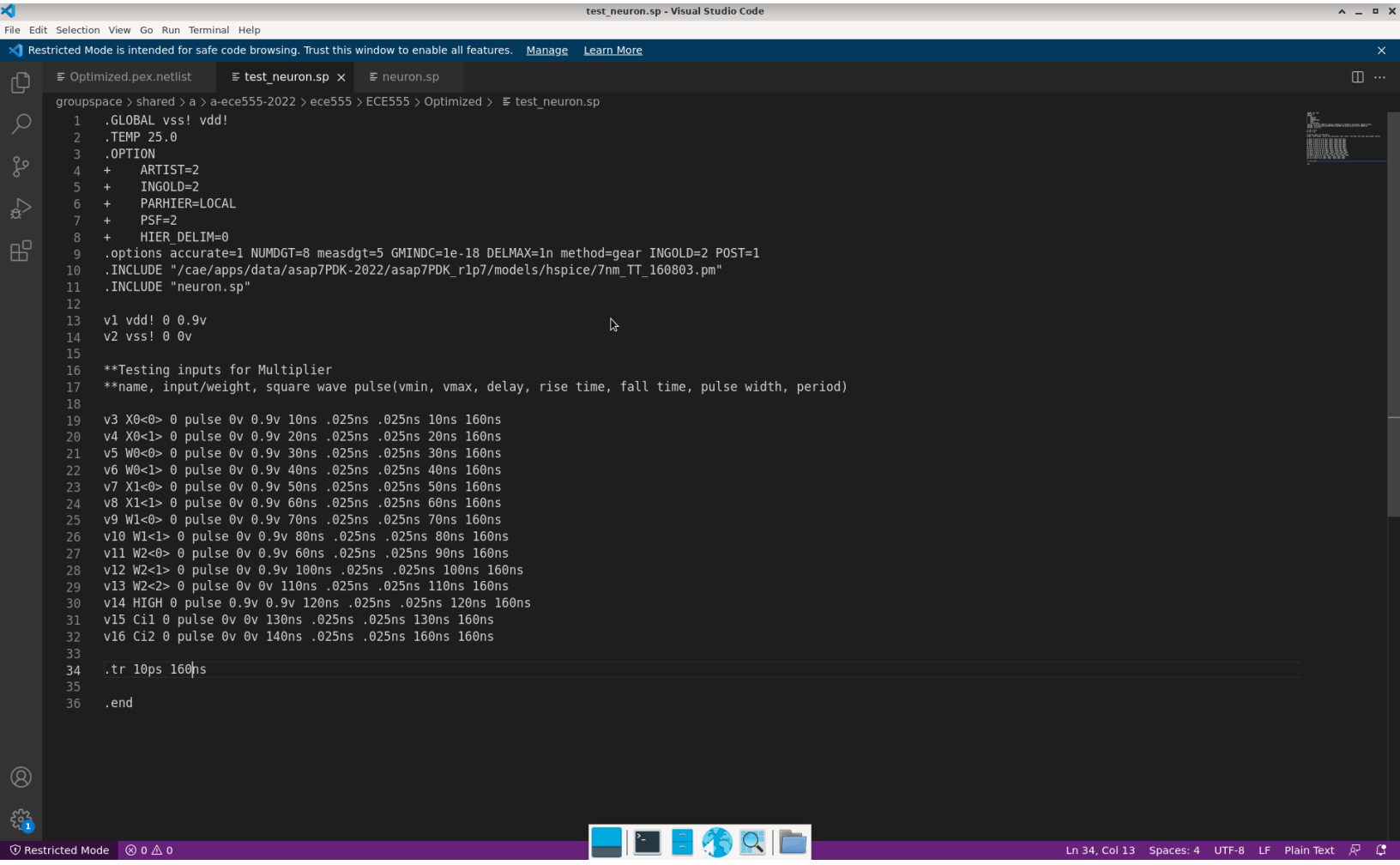
Calibre Extraction for Neuron



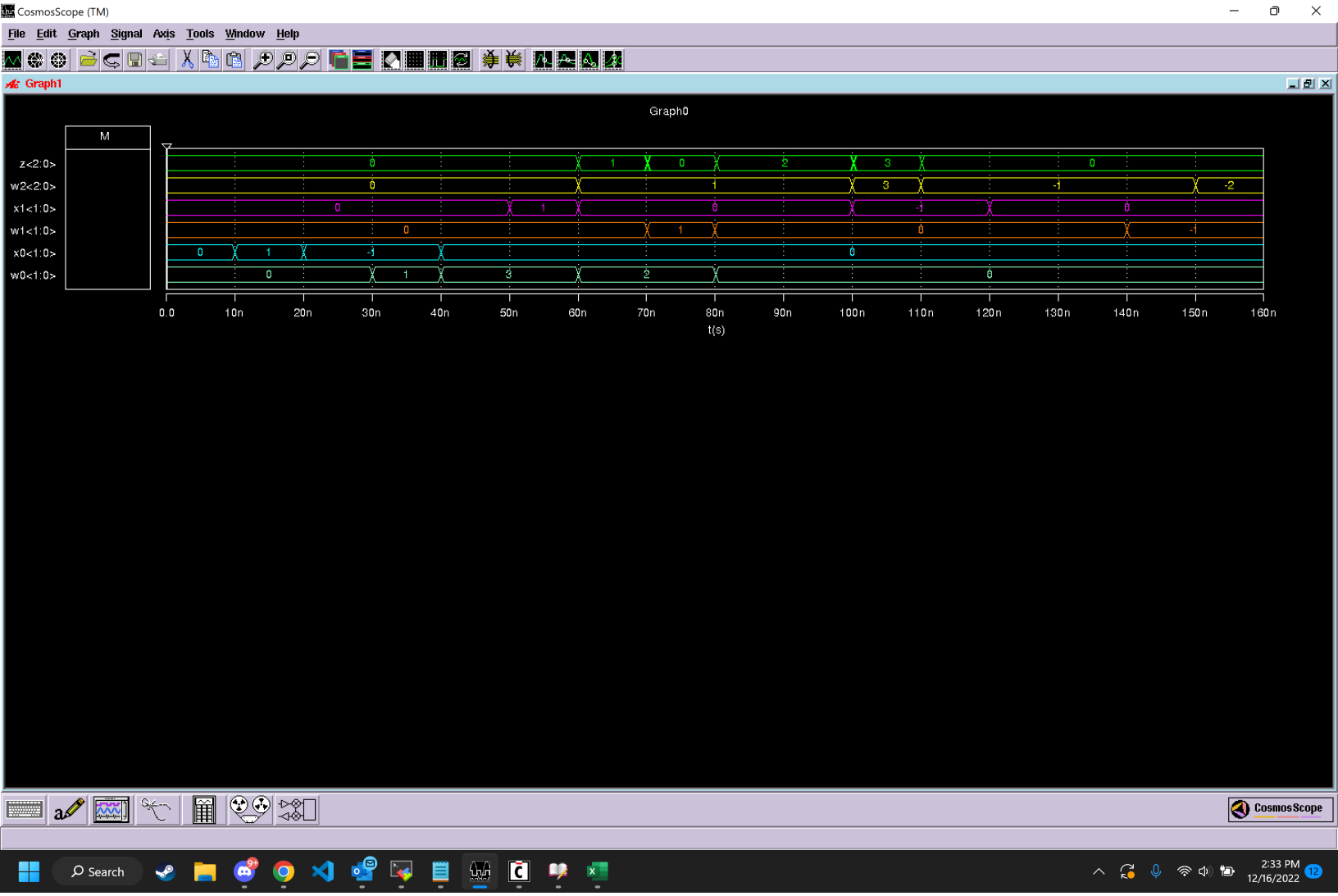
Testbench with load



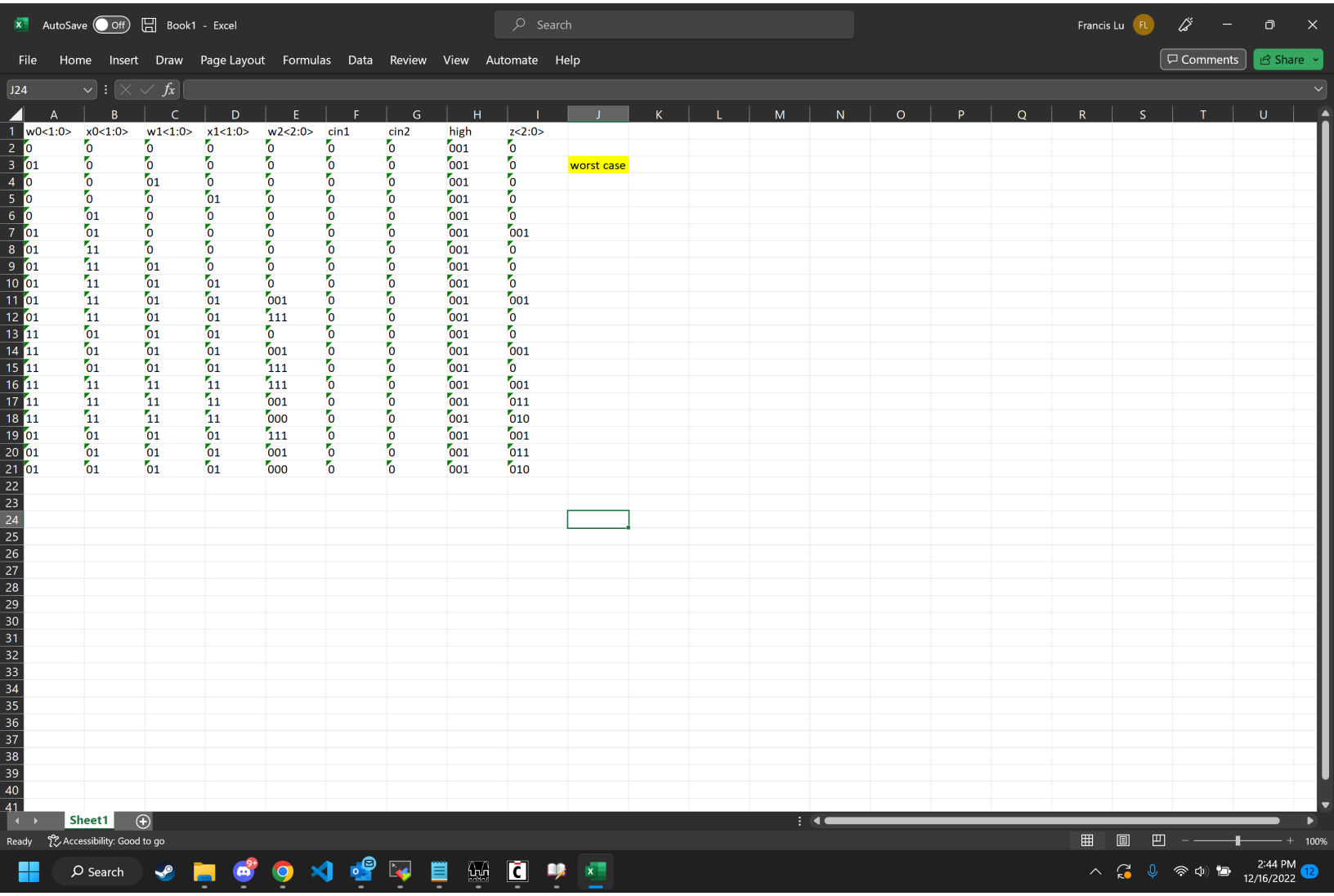
Testbench with inputs



Input and Output Waveform



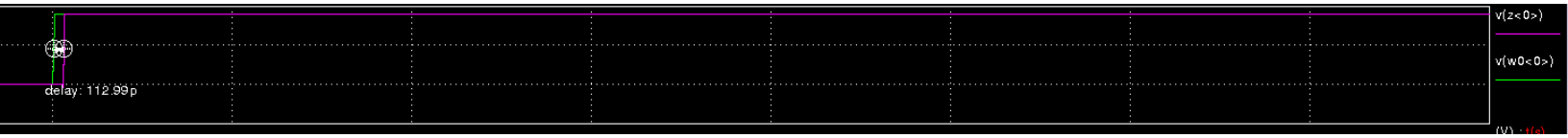
Compilation of example inputs and expected output



w0<1:0>	x0<1:0>	w1<1:0>	x1<1:0>	w2<2:0>	cin1	cin2	high	z<2:0>	
0	0	0	0	0	0	0	001	0	
01	0	0	0	0	0	0	001	0	worst case
0	0	01	0	0	0	0	001	0	
0	0	0	01	0	0	0	001	0	
0	01	0	0	0	0	0	001	0	
01	01	0	0	0	0	0	001	001	
01	11	0	0	0	0	0	001	0	
01	11	01	0	0	0	0	001	0	
01	11	01	01	0	0	0	001	0	
01	11	01	01	001	0	0	001	001	
01	11	01	01	111	0	0	001	0	
11	01	01	01	0	0	0	001	0	
11	01	01	01	001	0	0	001	001	
11	01	01	01	111	0	0	001	0	
11	11	11	11	111	0	0	001	001	
11	11	11	11	001	0	0	001	011	
11	11	11	11	000	0	0	001	010	
01	01	01	01	111	0	0	001	001	
01	01	01	01	001	0	0	001	011	
01	01	01	01	000	0	0	001	010	

Delay of critical path

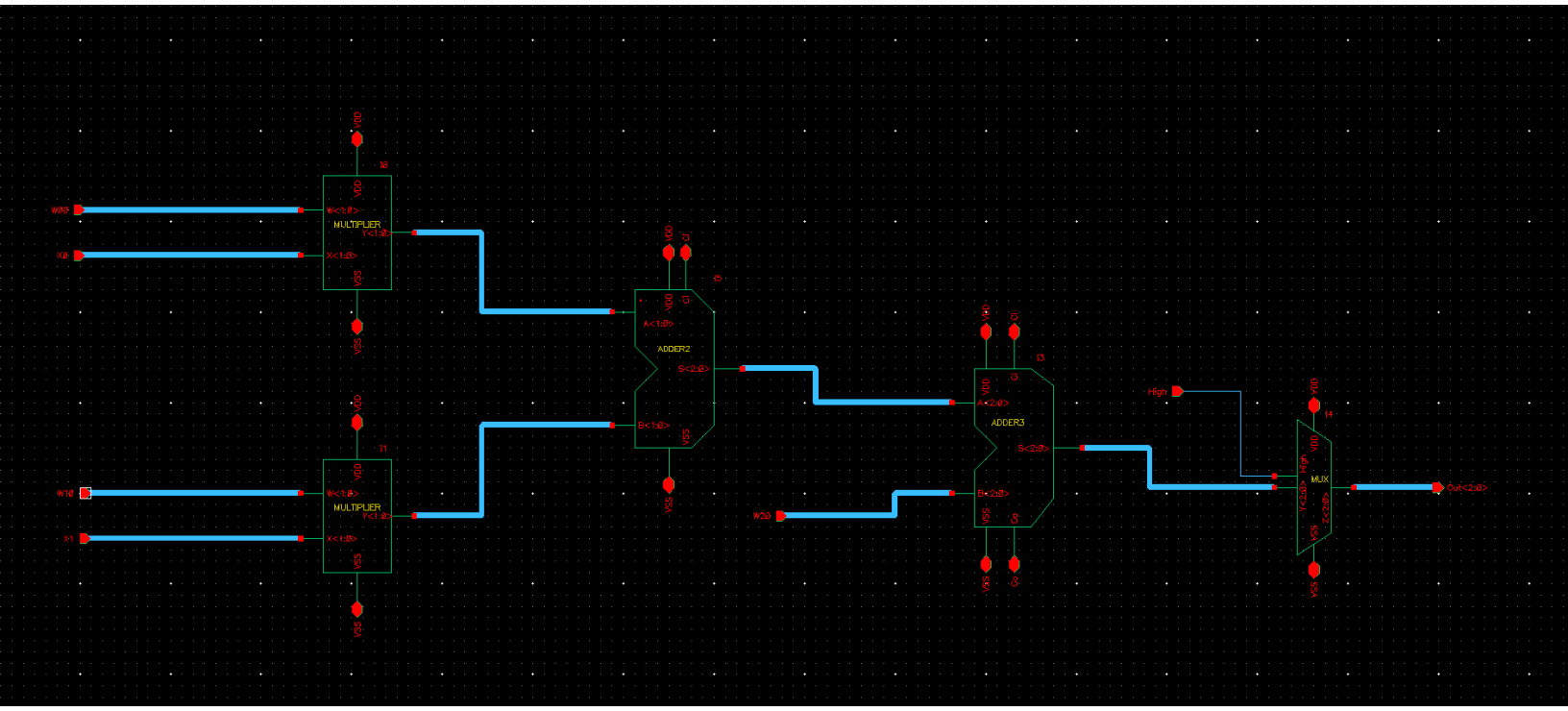
T = 112.99 ps
F = 8.85 GHz



Area of Cell

22.57 Square Micrometers

Neuron Schematic



Neuron Optimized Layout