

555 Final Report

Milestone 3- KOLDER, LU

1. We believe that the layout could have been improved. There is a decent amount of unused white space due to the modularization of our design. The routing in our design is quite good and does not stand for much improvement due to only M1 and M2 layers being used. Perhaps some routes could have been decreased in length. Optimization will focus on decreasing the area of our neuron. The critical path passes through a multiplier, ADDER2, ADDER3 and finally the mux. Thanks to the modularization of our design and arrangement of cells these routing length and distance between these cells has been minimized to optimize the critical path.
2. The optimization has resulted in a decreased area of our cell by around 15%.
3. DRC and LVS screenshots of submodules and total neuron are below.
4. Calibre Extraction of neuron is below.
5. The parasitic capacitance of the pre optimized neuron was 2.2909 e-16 f and the parasitic capacitance of the optimized neuron was 2.2909 e-16 f. The parasitic capacitance did not change.
6. The final area of our design is 22.57 square micrometers

ADDER2 DRC

Calibre - RVE v2017.4_19.14 : ADDER_2bit.drc.results

FileViewHighlightToolsWindowSetup

Search

Show Unresolved

ADDER_2bit, 22 Results (in 1 of 334 Checks)

Check / Cell

Check ACTIVE LUP.1

12345678910111213141516171819202122

Rule File Pathname: /fileSpace/L/kolder/ece555/drc/_drcRules_calibre_assp7.rul_
RVE Show Layers: 1 11 12 13

Check ACTIVE LUP.1

ADDER2 LVS

Calibre - RVE v2017.4_19.14 : svdb ADDER_2bit

File View Highlight Tools Window Setup

Search

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
ADDER_2bit	ADDER_2bit	29L, 29S	22L, 22S	10L, 10S

Cell ADDER_2bit Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

#

CORRECT #

~ ~
|
_ _

LAYOUT CELL NAME: ADDER_2bit
SOURCE CELL NAME: ADDER_2bit

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	10	10	
Nets:	51	51	
Instances:	88	44	* MN (4 pins)
	44	44	MP (4 pins)
Total Inst:	132	88	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	10	10	
Nets:	29	29	
Instances:	22	22	_nand2v (5 pins)
Total Inst:	22	22	

* * Number of objects in layout different from number in source.

ADDER3 DRC

Calibre - RVE v2017.4_19.14 : ADDER_3bit.drc.results

FileViewHighlightToolsWindowSetup

Search

Show Unresolved

ADDER_3bit, 33 Results (in 1 of 334 Checks)

Check / Cell

Check ACTIVE LUP.1

123456789101112131415161718192021222324252627282930313233

Rule File Pathname: /fileSpace/L/kolder/ece555/drc/_drcRules_calibre_assp7.rul_

RVE Show Layers: 1 11 12 13

Check ACTIVE LUP.1

ADDER3 LVS

Calibre - RVE v2017.4_19.14 : svdb ADDER_3bit

FileViewHighlightToolsWindowSetup

Search

Navigator

Results

Extraction Results

Comparison Results

Reports

Extraction Report

LVS Report

Rules

Rules File

View

Info

Finder

Schematics

Setup

Options

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
ADDER_3bit	ADDER_3bit	42L, 42S	33L, 33S	13L, 13S

Cell ADDER_3bit Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

#

CORRECT #

~ ~
|
_ _

LAYOUT CELL NAME: ADDER_3bit
SOURCE CELL NAME: ADDER_3bit

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	13	13	
Nets:	75	75	
Instances:	132	66	* MN (4 pins)
	66	66	MP (4 pins)
Total Inst:	198	132	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	13	13	
Nets:	42	42	
Instances:	33	33	_nand2v (5 pins)
Total Inst:	33	33	

* * Number of objects in layout different from number in source.

Mult DRC

Calibre - RVE v2017.4_19.14 : Multiplier.drc.results

FileViewHighlightToolsWindowSetup

Search

Show Unresolved

Multiplier, 8 Results (in 1 of 334 Checks)

Check / Cell

Check ACTIVE LUP.1

Cell Multiplier

1

2

3

4

5

6

7

8

Rule File Pathname: /fileSpace/L/ikolder/ece555/drc/_drcRules_calibre_osp7.rul_

RVE Show Layers: 1 11 12 13

Check ACTIVE LUP.1 / Cell Multiplier

Mult LVS

Calibre - RVE v2017.4_19.14 : svdb Multiplier

FileViewHighlightToolsWindowSetup

Search

Navigation

Results

Extraction Results

Comparison Results

Reports

Extraction Report

LVS Report

Rules

Rules File

View

Info

Finder

Schematics

Setup

Options

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
Multiplier	Multiplier	14L, 14S	8L, 8S	8L, 8S

Cell Multiplier Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

#

CORRECT

~ ~
|
_ _

LAYOUT CELL NAME: Multiplier
SOURCE CELL NAME: Multiplier

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	8	8	
Nets:	20	20	
Instances:	26	14	* MN (4 pins)
	14	14	MP (4 pins)
Total Inst:	40	28	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	8	8	
Nets:	14	14	
Instances:	2	2	_invv (4 pins)
	6	6	_rand2v (5 pins)
Total Inst:	8	8	

* * Number of objects in layout different from number in source.

MUX DRC

Calibre - RVE v2017.4_19.14 : MUX.drc.results

File View Highlight Tools Window Setup

Show Unresolved MUX, 6 Results (n 1 of 334 Checks)

Check / Cell

Check ACTIVE LUP.1

1 2 3 4 5 6

Rule File Pathname: /fileSpace/L/ldolder/ece555/drc/_drcRules_calibre_assp7.rul_
RVE Show Layers: 1 11 12 13

Check ACTIVE LUP.1

MUX LVS

FileViewHighlightToolsWindowSetup

Search

Navigator

Results

Extraction Results

Comparison Results

Reports

Extraction Report

LVS Report

Rules

Rules File

View

Info

Finder

Schematics

Setup

Options

Calibre - RVE v2017.4.19.14 : svdb MUX

Help

Comparison Results x

Layout Cell / Type	Source Cell	Nets	Instances	Ports
MUX	MUX	12L, 12S	6L, 6S	9L, 9S

Cell MUX Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

#

#####

#

CORRECT

#

#####

#

LAYOUT CELL NAME: MUX

SOURCE CELL NAME: MUX

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	9	9	
Nets:	14	14	
Instances:	12	8	* MN (4 pins)
	8	8	MP (4 pins)
Total Inst:	20	16	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	9	9	
Nets:	12	12	
Instances:	4	4	_invv (4 pins)
	2	2	_rand2v (5 pins)
Total Inst:	6	6	

* * Number of objects in layout different from number in source.

Neuron DRC

Calibre - RVE v2017.4_19.14 : Neuron.drc.results

FileViewHighlightToolsWindowSetup

Search

Show Unresolved

Neuron, 77 Results (in 1 of 334 Checks)

Check / Cell

Check ACTIVE LUP.1

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	
50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77																						

Rule File Pathname: /fileSpace/L/klolder/ece555/drc/_drcRules_calibre_essp7.rul_

RVE Show Layers: 1 11 12 13

Check ACTIVE LUP.1

Neuron LVS

Calibre - RVE v2017.4_19.14 : svdb Neuron

File View Highlight Tools Window Setup

Search

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
Neuron	Neuron	93L, 93S	77L, 77S	20L, 20S

Results

- Extraction Results
- Comparison Results

Reports

- Extraction Report
- LVS Report

Rules

- Rules File

View

- Info
- Finder
- Schematics

Setup

- Options

Cell Neuron Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

#

CORRECT

~ ~
|
~ ~

LAYOUT CELL NAME: Neuron
SOURCE CELL NAME: Neuron

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	20	20	
Nets:	162	162	
Instances:	284	146	* MN (4 pins)
	146	146	MP (4 pins)
Total Inst:	430	292	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	20	20	
Nets:	93	93	
Instances:	8	8	_invv (4 pins)
	69	69	_rand2v (5 pins)
Total Inst:	77	77	

* * Number of objects in layout different from number in source.

Calibre Extraction for Neuron

Applications: Calibre Interactive ... CosmosScope (TM) Library Manager: Di... Optimized Calibre - RVE v201... virtuoso test_neuron.sp - Vis... Terminal - Thu 15 Dec, 15:46 Francis Lu

Calibre Interactive - xACT v2017.4_19.14 : /cae/apps/data/asap7PDK-2022/asap7PDK_r1p7/calibre/rundirs/pex/runset_dir_pex/xactRunset_asap7 *

File Settings Help

Rules
Inputs
Outputs
Options
LVS
FieldSolver
Database
Environment
Run Control
Triggers
Templates
Preferences
Search
Transcript
Files

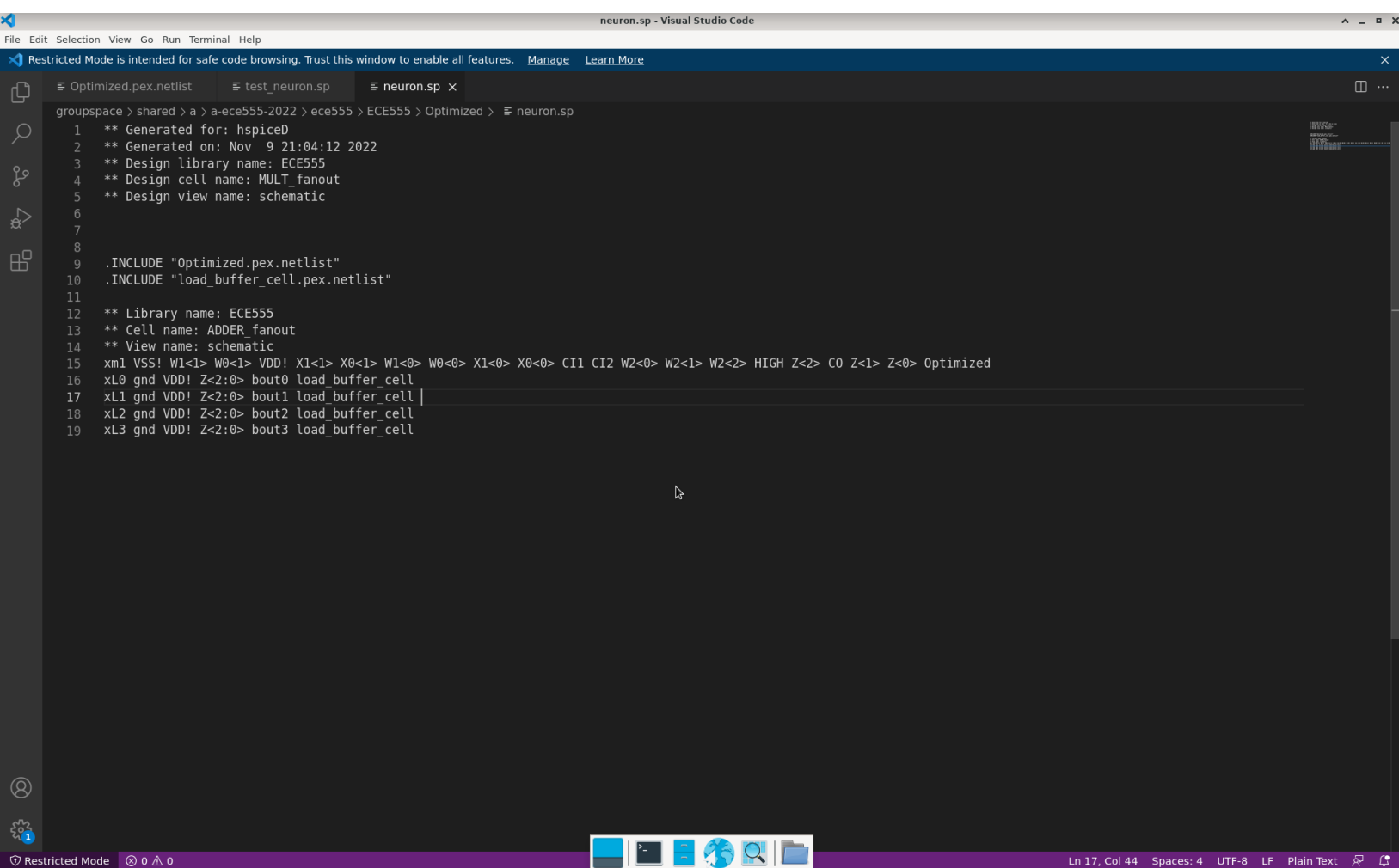
Optimized.pex.report x

```
1 #####
2 ##
3 ## Calibre xACT ##
4 ##
5 ## Export Lumped Parameters ##
6 ##
7 #####
8
9
10
11 LAYOUT NAME: Optimized
12 RULE FILE NAME: _pexControl_calibre_asap7.rul_
13 CREATION TIME: Thu Dec 15 14:54:39 2022
14
15 UNITS: Resistance = ohm
16 Capacitance = farad
17 Time = ns
18
19
20 -----
21 CELL NAME: Optimized
22
23 Netid R(UpperBound) Cvalue %Coupled RC(UpperBound) Netname
24 -----
25 90 0.0 2.2909e-16 73.8068 0.0 XI1/XI3/XI0/NET1
26
27 - Coupled nets
28 W1<1>:25,W1<1>:19,W1<1>:31,W1<1>:1,W1<1>:3,W1<1>:2,W1<1>:13,W1<1>:27,W1<1>:33,W1<1>:15,W1<1>:13,W1<1>:34,W1<1>:27,W1<1>:14,W1<1>:15,W1<1>:17,X1<1>:2,X1<1>:9,X1<1>:1,X1<1>:9,X1<1>:10,X1<1>:13,X1<1>:9,X1<1>:10,XI1/XI3/NET1:22,XI1/XI3/NET1:36,XI1/XI3/NET1:25,XI1/XI3/NET1:24,XI1/XI3/NET1:12,XI1/XI3/NET1:34,XI1/XI3/NET1:35,XI1/XI3/NET1:12,XI1/XI3/NET1:12,XI1/XI3/NET1:34
29 - Intrinsic capacitance
30 6.0006e-17
31 - Coupled capacitance
32 2.0456e-19 netid: W1<1>:25
33 2.0736e-19 netid: W1<1>:19
34 2.1644e-19 netid: W1<1>:31
35 5.5448e-19 netid: W1<1>:1
36 1.1846e-18 netid: W1<1>:3
37 7.2034e-19 netid: W1<1>:2
38 3.5209e-17 netid: W1<1>:13
39 7.1777e-19 netid: W1<1>:27
40 8.2491e-19 netid: W1<1>:33
41 8.2891e-19 netid: W1<1>:15
42 1.136e-18 netid: W1<1>:13
43 2.4266e-18 netid: W1<1>:34
44 9.1598e-18 netid: W1<1>:27
45 1.3369e-17 netid: W1<1>:14
46 2.6526e-17 netid: W1<1>:15
47 3.1108e-19 netid: X1<1>:17
48 1.1298e-18 netid: X1<1>:2
49 3.2407e-19 netid: X1<1>:9
50 7.7605e-19 netid: X1<1>:1
51 4.7615e-19 netid: X1<1>:9
52 6.0506e-19 netid: X1<1>:10
53 3.1516e-18 netid: X1<1>:13
54 2.3894e-17 netid: X1<1>:9
55 2.4875e-17 netid: X1<1>:10
56 1.4975e-18 netid: XI1/XI3/NET1:22
57 8.3911e-20 netid: XI1/XI3/NET1:36
58 1.1551e-19 netid: XI1/XI3/NET1:25
59 1.3838e-19 netid: XI1/XI3/NET1:24
60 1.1169e-18 netid: XI1/XI3/NET1:12
61 1.1322e-18 netid: XI1/XI3/NET1:34
62 1.3947e-18 netid: XI1/XI3/NET1:35
63 2.1754e-18 netid: XI1/XI3/NET1:12
64 4.4104e-18 netid: XI1/XI3/NET1:12
65 8.1803e-18 netid: XI1/XI3/NET1:34
```

Run xACT

Show RVE

Testbench with load

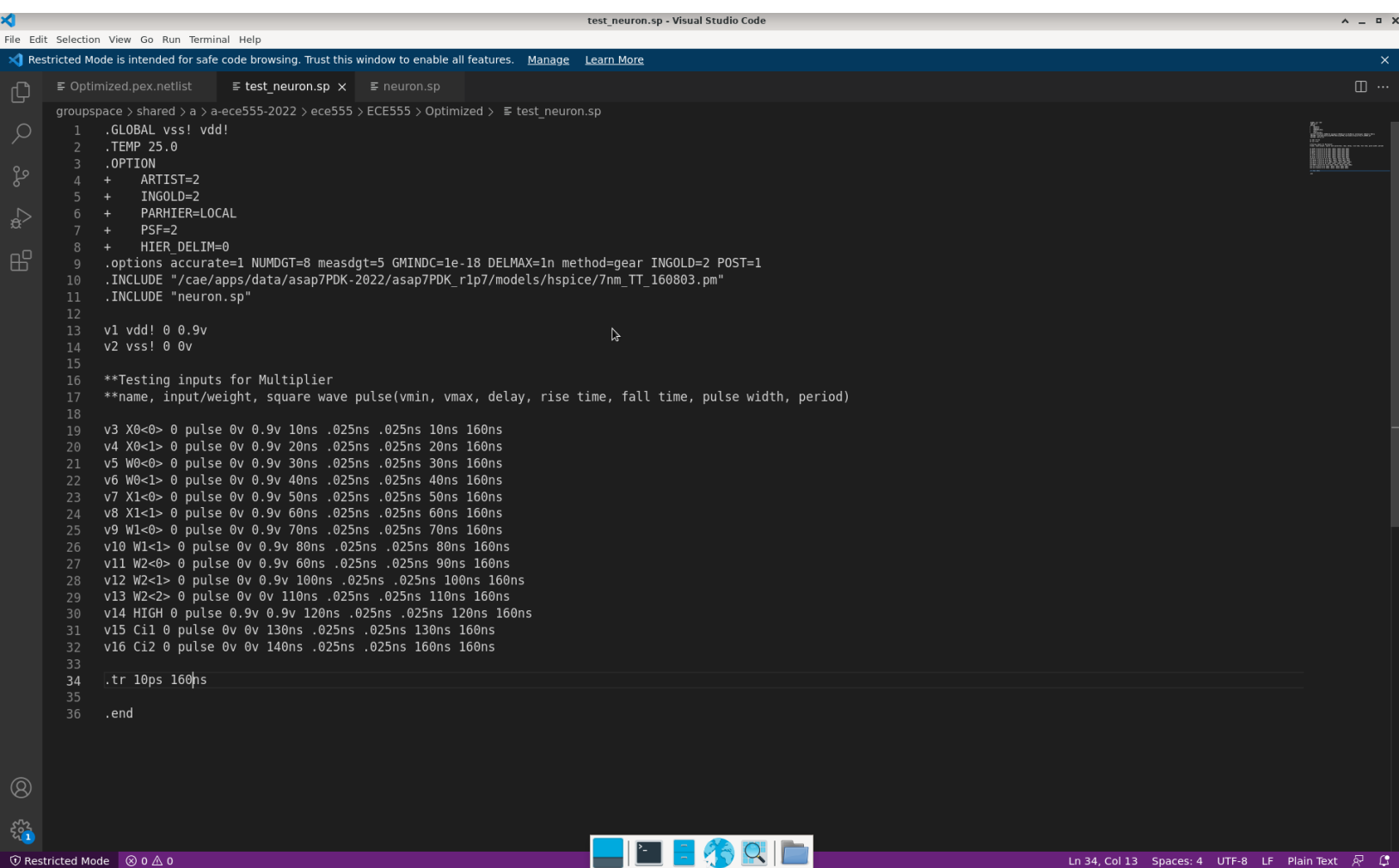


```
neuron.sp - Visual Studio Code
File Edit Selection View Go Run Terminal Help
Restricted Mode is intended for safe code browsing. Trust this window to enable all features. Manage Learn More

Optimized.pex.netlist test_neuron.sp neuron.sp x
groupspace > shared > a > a-ece555-2022 > ece555 > ECE555 > Optimized > neuron.sp
1  ** Generated for: hspiceD
2  ** Generated on: Nov  9 21:04:12 2022
3  ** Design library name: ECE555
4  ** Design cell name: MULT_fanout
5  ** Design view name: schematic
6
7
8
9  .INCLUDE "Optimized.pex.netlist"
10 .INCLUDE "load_buffer_cell.pex.netlist"
11
12 ** Library name: ECE555
13 ** Cell name: ADDER_fanout
14 ** View name: schematic
15 xm1 VSS! W1<1> W0<1> VDD! X1<1> X0<1> W1<0> W0<0> X1<0> X0<0> CI1 CI2 W2<0> W2<1> W2<2> HIGH Z<2> C0 Z<1> Z<0> Optimized
16 xL0 gnd VDD! Z<2:0> bout0 load_buffer_cell
17 xL1 gnd VDD! Z<2:0> bout1 load_buffer_cell |
18 xL2 gnd VDD! Z<2:0> bout2 load_buffer_cell
19 xL3 gnd VDD! Z<2:0> bout3 load_buffer_cell
```

Ln 17, Col 44 Spaces: 4 UTF-8 LF Plain Text

Testbench with inputs

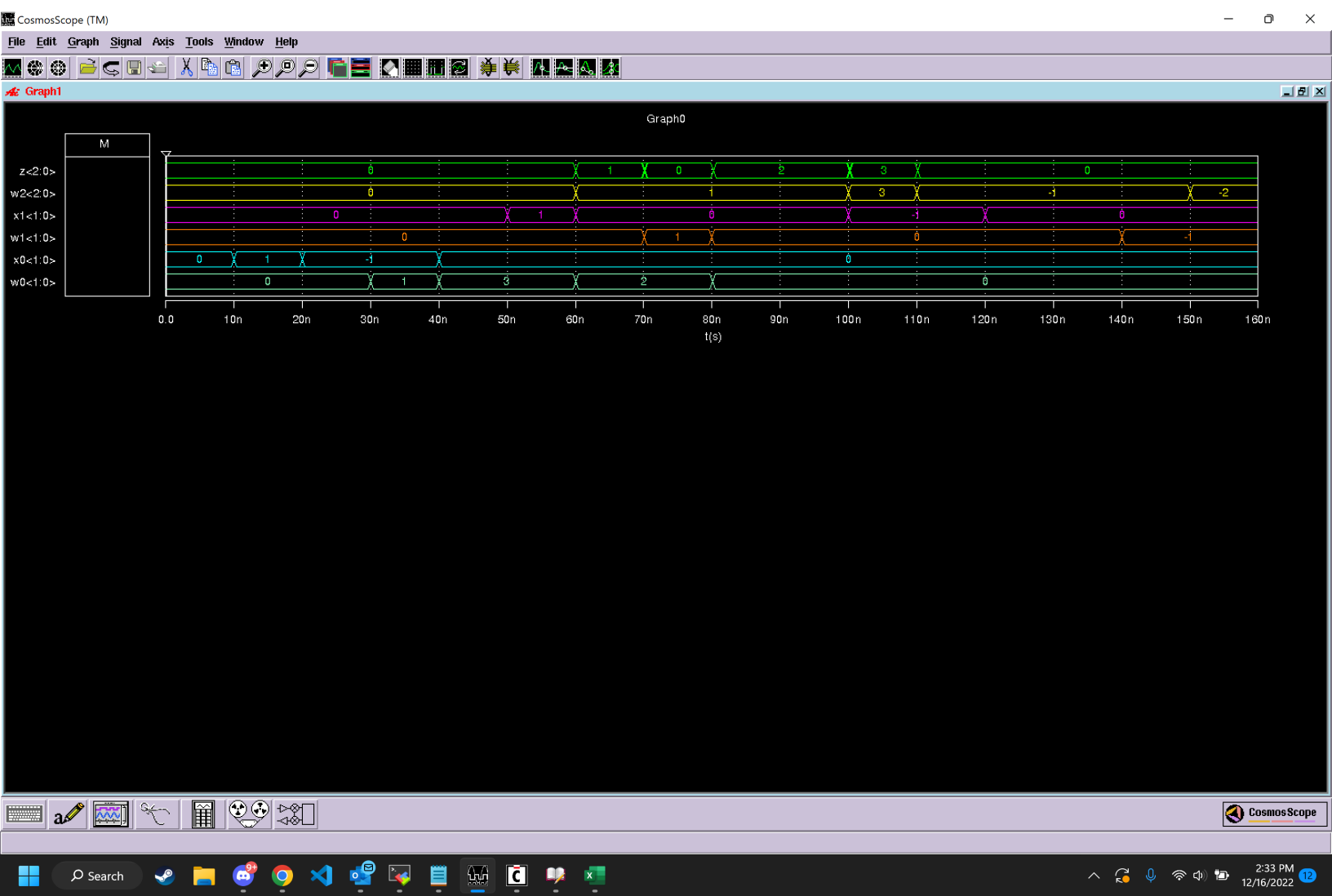


```
test_neuron.sp - Visual Studio Code
File Edit Selection View Go Run Terminal Help
Restricted Mode is intended for safe code browsing. Trust this window to enable all features. Manage Learn More

Optimized.pex.netlist test_neuron.sp x neuron.sp
groupspace > shared > a > a-ece555-2022 > ece555 > ECE555 > Optimized > test_neuron.sp
1 .GLOBAL vss! vdd!
2 .TEMP 25.0
3 .OPTION
4 + ARTIST=2
5 + INGOLD=2
6 + PARHIER=LOCAL
7 + PSF=2
8 + HIER DELIM=0
9 .options accurate=1 NUMDGT=8 measdgt=5 GMINDC=1e-18 DELMAX=1n method=gear INGOLD=2 POST=1
10 .INCLUDE "/cae/apps/data/asap7PDK-2022/asap7PDK_r1p7/models/hspice/7nm_TT_160803.pm"
11 .INCLUDE "neuron.sp"
12
13 v1 vdd! 0 0.9v
14 v2 vss! 0 0v
15
16 **Testing inputs for Multiplier
17 **name, input/weight, square wave pulse(vmin, vmax, delay, rise time, fall time, pulse width, period)
18
19 v3 X0<0> 0 pulse 0v 0.9v 10ns .025ns .025ns 10ns 160ns
20 v4 X0<1> 0 pulse 0v 0.9v 20ns .025ns .025ns 20ns 160ns
21 v5 W0<0> 0 pulse 0v 0.9v 30ns .025ns .025ns 30ns 160ns
22 v6 W0<1> 0 pulse 0v 0.9v 40ns .025ns .025ns 40ns 160ns
23 v7 X1<0> 0 pulse 0v 0.9v 50ns .025ns .025ns 50ns 160ns
24 v8 X1<1> 0 pulse 0v 0.9v 60ns .025ns .025ns 60ns 160ns
25 v9 W1<0> 0 pulse 0v 0.9v 70ns .025ns .025ns 70ns 160ns
26 v10 W1<1> 0 pulse 0v 0.9v 80ns .025ns .025ns 80ns 160ns
27 v11 W2<0> 0 pulse 0v 0.9v 60ns .025ns .025ns 90ns 160ns
28 v12 W2<1> 0 pulse 0v 0.9v 100ns .025ns .025ns 100ns 160ns
29 v13 W2<2> 0 pulse 0v 0v 110ns .025ns .025ns 110ns 160ns
30 v14 HIGH 0 pulse 0.9v 0.9v 120ns .025ns .025ns 120ns 160ns
31 v15 Ci1 0 pulse 0v 0v 130ns .025ns .025ns 130ns 160ns
32 v16 Ci2 0 pulse 0v 0v 140ns .025ns .025ns 160ns 160ns
33
34 .tr 10ps 160ps
35
36 .end

Ln 34, Col 13 Spaces: 4 UTF-8 LF Plain Text
```

Input and Output Waveform



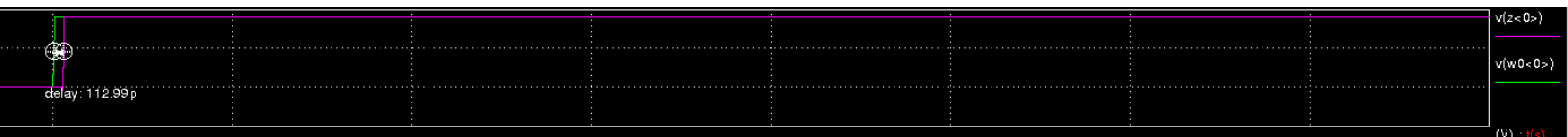
Compilation of example inputs and expected output

[illegible]

Delay of critical path

$T = 112.99 \text{ ps}$

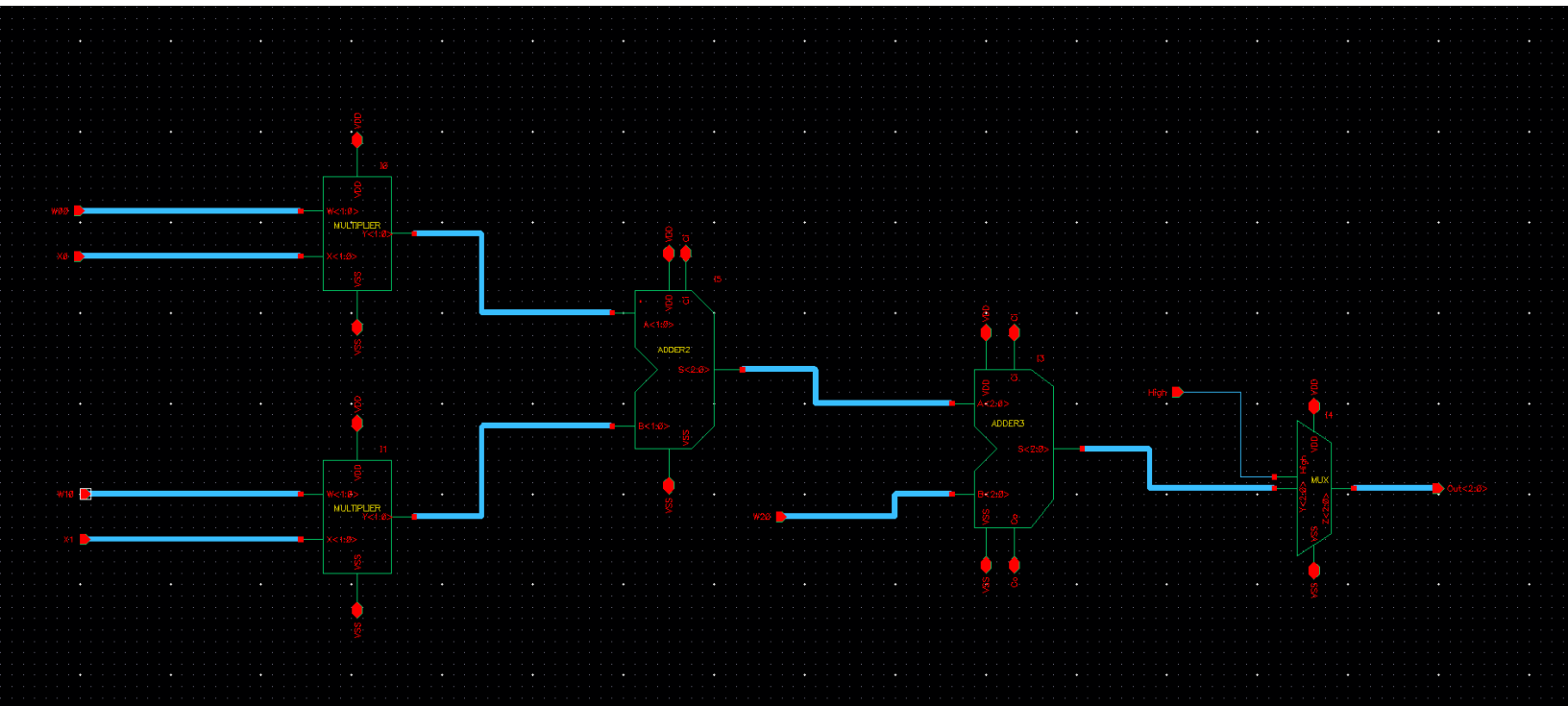
$F = 8.85 \text{ GHz}$



Area of Cell

22.57 Square Micrometers

Neuron Schematic



Neuron Optimized Layout

