Design of 16x16 Magnitude Comparator Using High Speed technique

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Abstract

while in general comparators are “fast”, their circuits are not immune to the classic speed-power tradeoff. High speed comparators use transistors with larger aspect ratios and hence also consume more power. Depending on the application, select either a comparator with high speed or one that saves power. The paper present HIGH-SPEED technique using CMOS logic for implementation of digital logic circuit. In this paper, 16x16 bit magnitude comparator is designed using two 8x8-bit comparators, which are constructed from 4x4-bit comparators, employing high-speed techniques. The proposed HIGH-SPEED magnitude Comparator requires 722 transistors and the power consumed by the 16x16 HIGH-SPEED magnitude is 25mWatT. Our comparator considered small as compared to conventional CMOS Style since our 4x4 bit comparator requires 158 transistors while the conventional CMOS magnitude comparator requires 226 transistors. Delay present in the conventional CMOS magnitude comparator is 13nsec [1] whereas the delay produced by our High-Speed technique for magnitude comparator is 5ns which is our goal. All this circuit simulation is done by using ELECTRIC TOOL EDA at 2microm process technology.

Keywords-: comparator, CMOS technology, High Speed technique, LTSpice.

1. Introduction

Comparators are fundamental components in digital circuits, serving crucial roles in determining the relationship between two input signals. They are integral to various applications, from simple decision-making processes to more complex systems requiring precise voltage or signal level comparisons. Therefore, choosing the best comparator with fast speed is considered very important step. After doing an extensive search in order to achieve our goal in increasing the speed as much as we can, a 158 transistor 4x4 bit comparator was chosen to build the 8x8 bit comparator. Our purposed 16x16-bit comparator is then built from the 8x8 comparator. The 4x4 comparator consists of 8 inverters, 10 two input AND, 4 two input NOR, 3 input AND, 4 input AND, 4 input OR. LTSpice schematics were used to determine the propagation delay, the rise and fall times with PMOS width = 20micron, NMOS width = 10micron) and process length L=2micron. Then, LTSpice’s errors and design rules checking were used to verify if our circuits were correctly connected and if the comparators produced the correct results.

2. Magnitude Comparator

A magnitude digital comparer is a combinational circuit that compares two binary numbers to determine their relationship. It has two input terminals, one for each binary number (A and B), and three output terminals indicating the comparison results: one for A > B, one for A = B, and one for A < B [2].

Fig. 1: N - bit Magnitude comparator [2]

2.1 Four Bit Magnitude Comparator

4-bit magnitude comparator [2] is shown in Fig. 2 below is used to compare two binary numbers each of four bits. If we made all the input combinations then the o/p obtained is given below in Table 1.

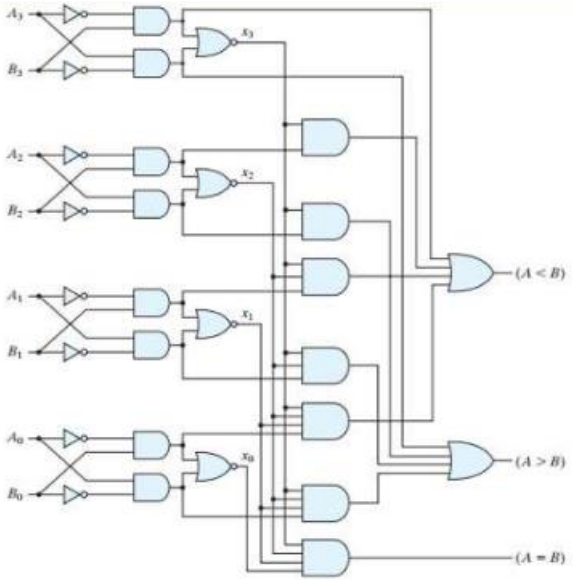


Fig. 2: 4-bit Magnitude comparator [3]

Table 1: 4-bit Magnitude Comparator [3]

A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	1	0	0
A3 < B3	X	X	X	X	X	X	0	1	0
A3 = B3	A2 > B2	X	X	X	X	X	1	0	0
A3 = B3	A2 < B2	X	X	X	X	X	0	1	0
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	0	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	0	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	1	0	0	0	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	0	1	1	0

The condition for A > B:

1. If A3 = 1 and B3 = 0
2. If A3 = B3 and A2 = 1 and B2 = 0
3. If A3 = B3, A2 = B2 and A1 =1 and B1 = 0
4. If A3= B3, A2 = B2, A1 = B1 and A0 = 1 and B0 = 0

The condition for A < B:

1. If A3 = 0 and B3 = 1
2. If A3 = B3 and A2 = 0 and B2 = 1
3. If A3 = B3, A2 = B2 and A1 = 0 and B1 = 1
4. If A3 = B3, A2 = B2, A1 = B1 and A0 = 0 and B0 = 1

The condition A = B is met only when each bit of one number exactly matches the corresponding bit of the other number.

3. Design of 4-bit magnitude comparator

A 4-bit magnitude comparator is a hardware electronic device designed to compare two 4- bit binary numbers and determine whether one number is greater than, less than, or equal to the other. The 4-bit magnitude comparator shown in Fig. 3 compares two 4-bit binary numbers, A and B, and produces three binary outputs: F1 (A > B), F2 (A = B), and F3 (A < B). the inputs to the 4-bit magnitude comparator are the bits of the numbers A (A3, A2, A1, A0) and B (B3, B2, B1, B0).

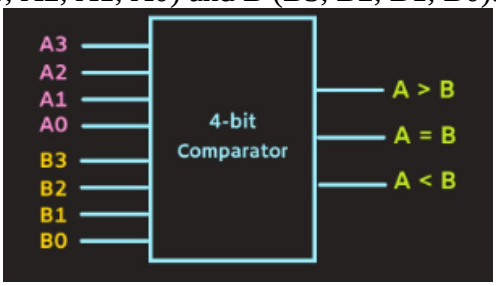


Figure 3: Four-bit magnitude comparator [3]

3.1 Design of 4-bit magnitude comparator using High Speed Technique

The 4-bit magnitude comparator using conventional CMOS logic uses 226 transistors which requires large power, larger area and lower speed also the circuit becomes more complex. The 4-bit high speed magnitude comparator is shown in Fig .4 which uses 158 transistors which is less as compared to the transistors in the conventional CMOS logic style as a result of which it requires less power, smaller area, more speed and complexity is also reduced.

The schematic and layout designs for the 4x4 bit magnitude comparator are shown in Fig. 4 and Fig. 5 below.

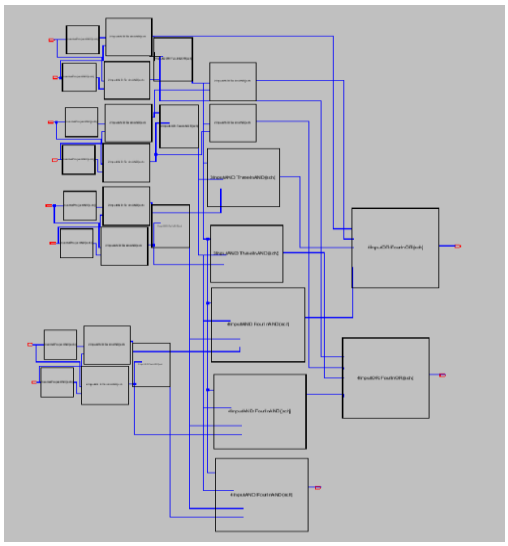


Fig. 4: Schematic design of 4-bit magnitude comparator using High Speed Technique

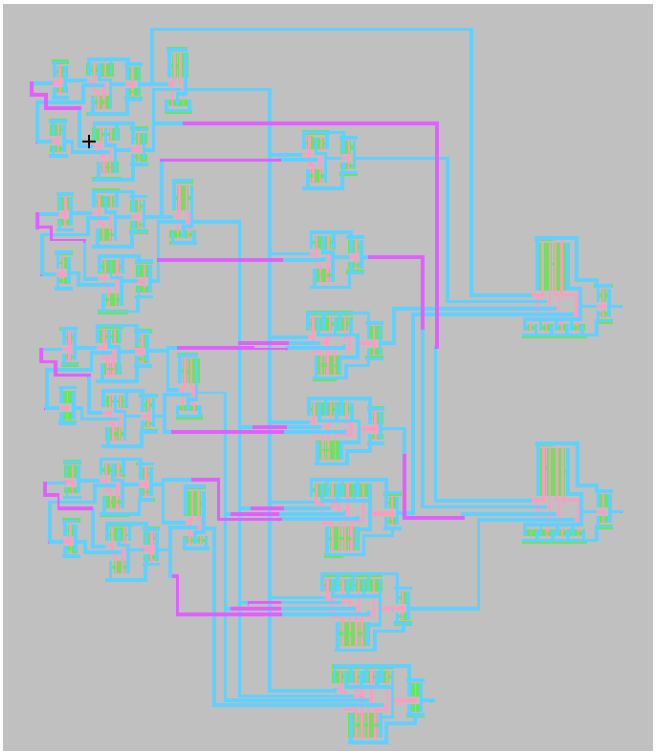
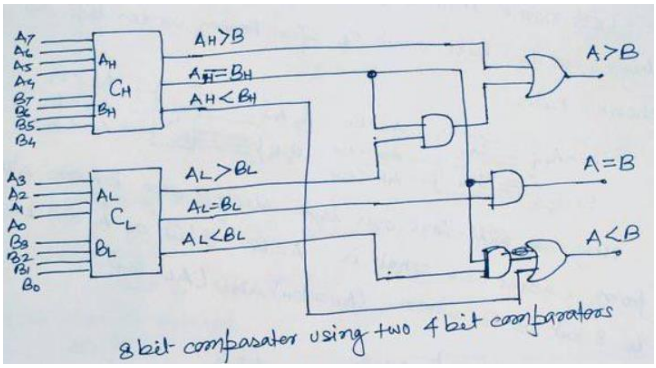


Fig. 5: Layout design of 4-bit magnitude comparator using High Speed Technique

4. Design of 8x8 High Speed magnitude comparator using two 4x4 magnitude comparator

An 8-bit comparator is constructed using two 4-bit comparators and additional logic gates as shown in Fig. 6. The 8-bit numbers are split into two 4-bit segments, which are compared separately by the 4-bit comparators. The results are then combined to determine the overall comparison. Specifically, the 8-bit comparison outputs (greater than, equal to, less than) are derived from logical combinations of the 4-bit comparator outputs, ensuring accurate and efficient comparison of the 8-bit numbers.



The schematic and layout designs for the 8x8 bit magnitude comparator are shown in Fig. 6 and Fig. 7 below.

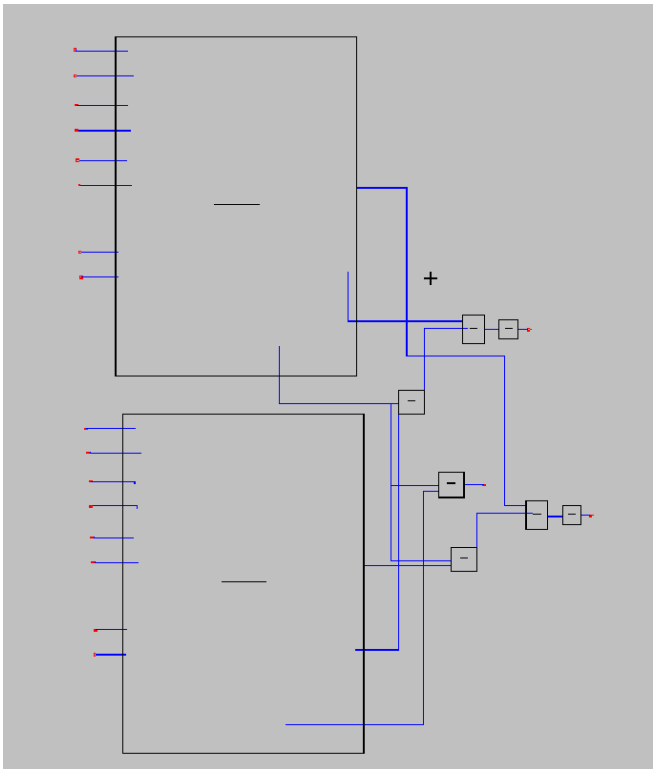


Fig. 6: Schematic of 8x8 bit comparator using two 4x4 comparators

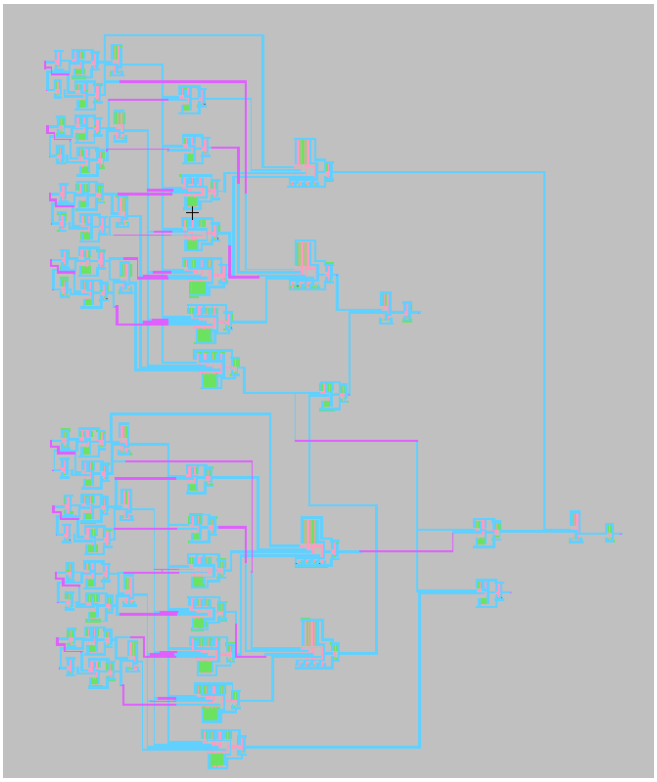


Fig. 7: Layout of 8x8 bit comparator using two 4x4 comparators

5. Design of 16x16 High Speed magnitude comparator using two 8x8 magnitude comparator

Subsequently, we used the 8x8 comparator to construct a 16x16 bit comparator to further increase speed and enhance performance.

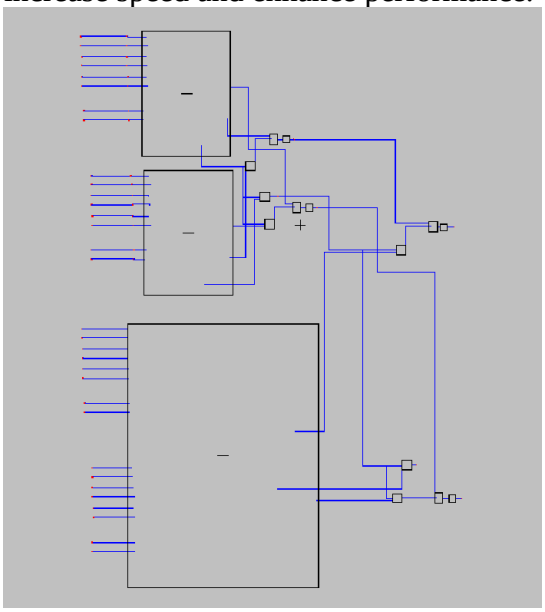


Fig. 8: Schematic of 16x16 **bit comparator using two** 8x8 **comparators**

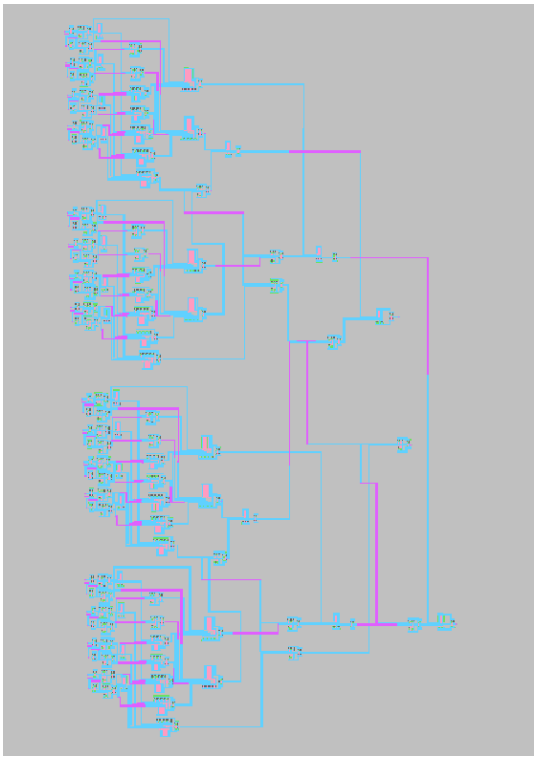


Figure 9: Layout of 16x16 bit comparator using two 8x8 comparators

6. Simulation result and performance analysis

Choosing most suitable parameters (process = 2micron P-MOS width = 20-micron, N-MOS = 10micron), we start making a 4-bit comparator using 10 two input AND, 4 two input NOR, 3 input AND, 4 input AND, 4 input OR gate and a NOR gate on LTspice tool. Check Fig. 4 shown above.

6.1 The output waveform for 4x4 bit magnitude comparator

Fig .10 shows the simulation for 4x4 Comparator

- when A is greater than B ➔ GreaterThan is high reaches 5 volts and LessThan and Equal are low reach almost 0V.
- when A is less than B ➔ GreaterThan and Equal are low reach almost 0V.
- when A is Equal to B ➔ GreaterThan and LessThan are low reach 0v and Equal is high reaches 5 volts.

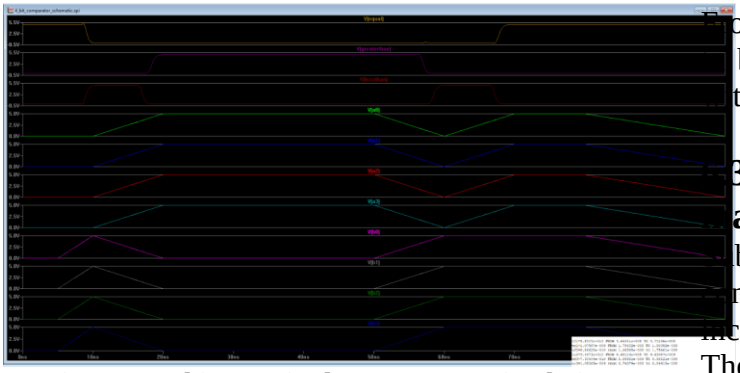


Fig. 10: 4x4 bit magnitude comparator simulation

The time falling and rising time for each output:

```
tf1=8.8545e-010 FROM 5.66341e-008 TO 5.75196e-008
tr1=1.07597e-009 FROM 1.79632e-008 TO 1.90392e-008
tf2=8.86628e-010 FROM 1.66595e-008 TO 1.75461e-008
tr2=9.4973e-010 FROM 8.68114e-009 TO 9.63087e-009
tf3=7.30404e-010 FROM 8.85581e-009 TO 9.58621e-009
tr3=1.05365e-009 FROM 6.74379e-008 TO 6.84915e-008
```

Where tf1 and tr1 represents the falling and rising time for the output GreaterThan “A>B”, tf2 and tr2 represents the falling and rising time for the output LessThan “A<B” and tf3 and tr3 represents the falling and rising time for the output Equal “A=B”.

6.2 The output waveform for 8x8 bit magnitude comparator

Then, an 8x8 bit comparator is built from the 4x4 bit comparator in order to enhance the speed “time”. Hence, the output waveform for 8-bit magnitude comparator is shown in Fig. 11 below.

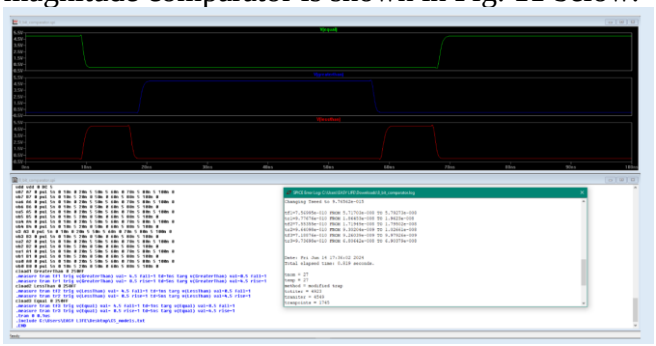
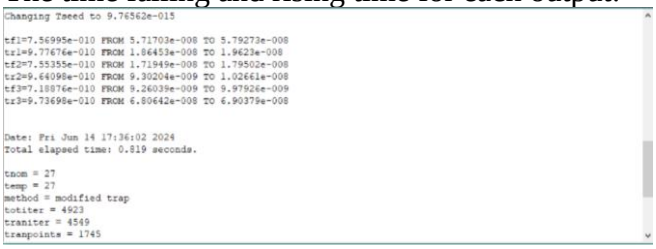


Fig. 11: 8x8 bit magnitude comparator simulation

The time falling and rising time for each output:



```
Changing Tseed to 9.76562e-015

tf1=7.56995e-010 FROM 5.71703e-008 TO 5.79273e-008
tr1=9.77676e-010 FROM 1.86453e-008 TO 1.9623e-008
tf2=7.55355e-010 FROM 1.71949e-008 TO 1.79502e-008
tr2=9.64098e-010 FROM 9.30204e-009 TO 1.02661e-008
tf3=7.18076e-010 FROM 9.26039e-009 TO 9.97926e-009
tr3=9.73698e-010 FROM 6.80642e-008 TO 6.90379e-008


Date: Fri Jun 14 17:36:02 2024
Total elapsed time: 0.819 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 4923
traniter = 4549
tranpoints = 1745
```

Fig. 12: Outputs rising and falling time for 8x8 comparator

om Fig. 10, we observed a significant decrease both the falling and rising times, which aligns th our objectives.

3 The output waveform for 16x16 bit agnitude comparator

bsequently, we used the 8x8 comparator to nstruct a 16x16 bit comparator to further ncrease speed and enhance performance.

The output waveform for 16-bit magnitude comparator is shown in Fig. 13 below.

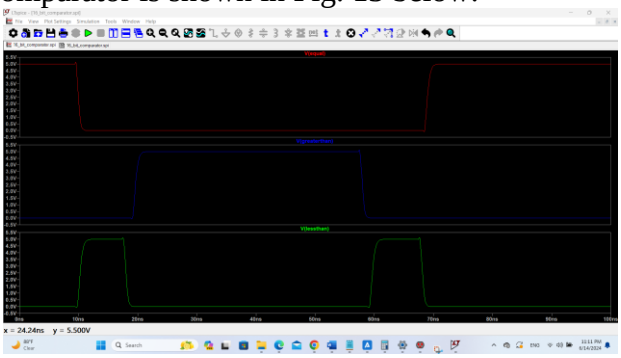
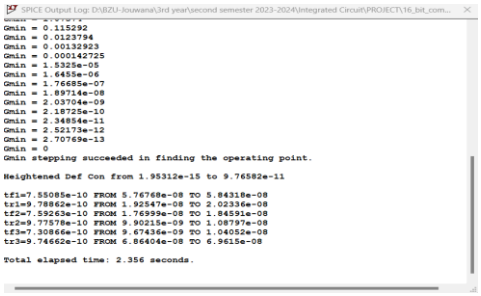


Fig. 13: 16x16 bit magnitude comparator simulation



```
Gmin = 0.115292
Gmin = 0.0123794
Gmin = 0.00132923
Gmin = 0.000142725
Gmin = 1.5325e-05
Gmin = 1.6455e-06
Gmin = 1.76685e-07
Gmin = 1.89714e-08
Gmin = 2.03704e-09
Gmin = 2.18725e-10
Gmin = 2.34854e-11
Gmin = 2.52173e-12
Gmin = 2.70769e-13
Gmin = 0
Gmin stepping succeeded in finding the operating point.

Heightened Def Con from 1.95312e-15 to 9.76582e-11

tf1=7.55085e-10 FROM 5.76768e-08 TO 5.84318e-08
tr1=9.78862e-10 FROM 1.92547e-08 TO 2.02336e-08
tf2=7.59263e-10 FROM 1.76999e-08 TO 1.84591e-08
tr2=9.77578e-10 FROM 9.90215e-09 TO 1.08797e-08
tf3=7.30866e-10 FROM 9.67436e-09 TO 1.04052e-08
tr3=9.74662e-10 FROM 6.86404e-08 TO 6.9615e-08

Total elapsed time: 2.356 seconds.
```

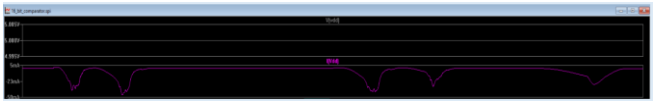
Fig. 14: 16x16 bit magnitude comparator rising and falling time

From Fig. 14, we observe that there is no reduction in time, but the key difference is that we can now compare 16 bits instead of 8 bits, indicating better performance, especially in terms of speed.

7. 16x16 bit magnitude comparator power and speed

7.1 power

From Fig. 12, we extract the power which equals 25mW.



Where Imax = 5mA and VDD = 5v. Then:
Power = Imax x VDD = 5V x 5mA = 25mWatt.
For our 2 micron technology, and for our high speed goal, the 5V DC was the best power option.

It is a hard process to balance between the speed requirements and the power dissipation especially when designing a high-speed circuit, but we've done our best to reduce the power dissipation as much as we could, as follows:
A 2 micron technology might seems a little large, but we've chosen this technology to achieve the balance between the high speed and the power consumption, in which:

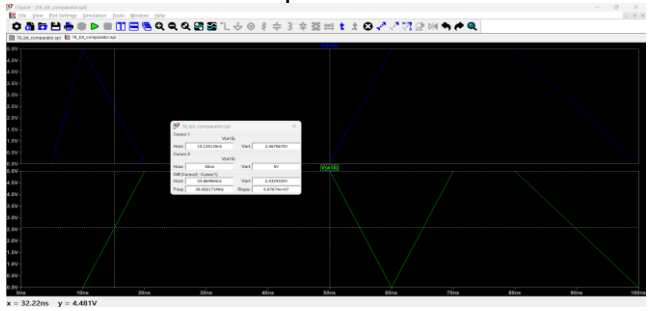
- The larger the technology was, the less the capacitors coupling will be, which will decrease the power.

- The greater the channel length was, the less the leakage current will be, which will lead to a less static power dissipation.

- Also the minimum width for the nmos and the pmos helps in reducing the power consumption, since proper transistor sizing can help in minimizing power.

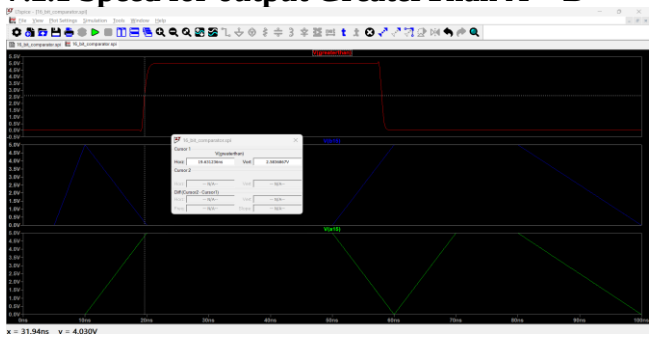
7.2 Speed

The speed is determined by calculating the propgation delay of each output__GreaterThan, LessThan, and Equal. The propgation delay is measured by taking the difference between the time when the input reaches 50% of its value and the time when the output reaches 50% of its value.



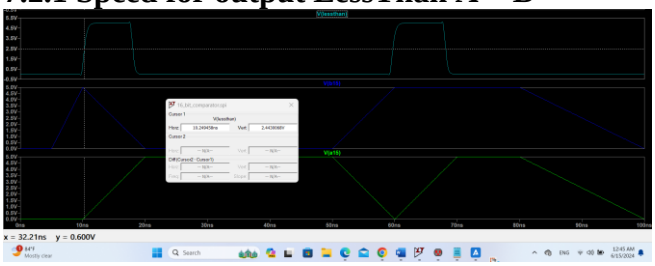
the time when the input reaches 50% of its value "2.5V" is almost 15ns.

7.2.1 Speed for output GreaterThan A > B



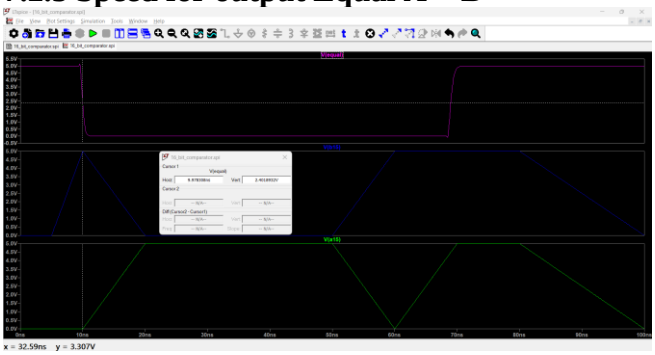
The time when the GreaterThan output reaches 50% of its value is almost 19ns. Hence, the propagation delay is 19ns – 15ns = 4ns.

7.2.1 Speed for output LessThan A < B



The time when the LessThan output reaches 50% of its value is almost 10ns. Hence, the propagation delay is 15ns – 10ns = 5ns.

7.2.3 Speed for output Equal A = B



The time when the Equal output reaches 50% of its value is almost 10ns. Hence, the propagation delay is 15ns – 10ns = 5ns.

Hence, based on the calculated speed for each output: A > B, A < B and A = B, our 16x16 bit comparator appears to be fast, with a speed of 4-5ns.

8. Conclusion

In this paper, we successfully designed and implemented a high-speed 16x16-bit magnitude comparator using a hierarchical approach that builds upon smaller comparators. By starting with a 4x4-bit comparator composed of 158 transistors, we constructed an 8x8-bit comparator and then a 16x16-bit comparator, achieving our goal of enhancing speed while maintaining reasonable power consumption. Our proposed high-speed technique demonstrated a significant improvement in delay reduction, achieving a delay of 5ns compared to the 13ns delay of conventional CMOS logic. Additionally, the power consumption of our design was measured at 25mW. These results were validated through

extensive simulations using LTSpice, confirming the correctness and efficiency of our circuit. The implementation of the high-speed technique in a 2-micron process technology effectively balanced speed and power requirements, making our design Suitable for applications demanding high performance and low power consumption.

9. References

[1]: https://www.ti.com/lit/ds/symlink/cd74hc85.pdf

[2]: https://www.geeksforgeeks.org/magnitude-comparator-in-digital-logic/

[3]: https://images.search.yahoo.com/search/images;_ylt=AwrEmv0xymxm6PID2TJXNyoA;_ylu=Y29sbwNiZjEEcG9zAzEEdnRpZAMEc2VjA3BpdnM-?p=four+bit+magnitude+comparator&fr2=piv-web&type=E210US91215G0&fr=mcafee