



Program:

Course Number	2005
Section Number	1
Course Title	EMBEDDED SYSTEMS ARCHITECTURE 1
Semester/Year	WINTER/2019

Instructor	<b>Mohsen Salahi</b>
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<b>Assignment</b>	<b>1</b>
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Submission Date	<b>02/24/2019</b>
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**Exercise 2.26** Using De Morgan equivalent gates and bubble pushing methods, redraw the circuit in Figure 2.83 so that you can find the Boolean equation by inspection. Write the Boolean equation.

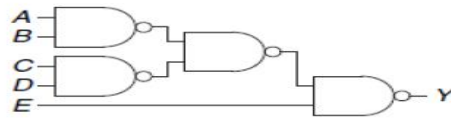
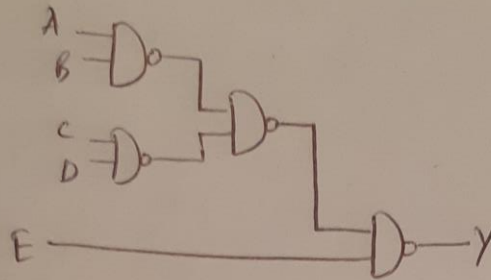
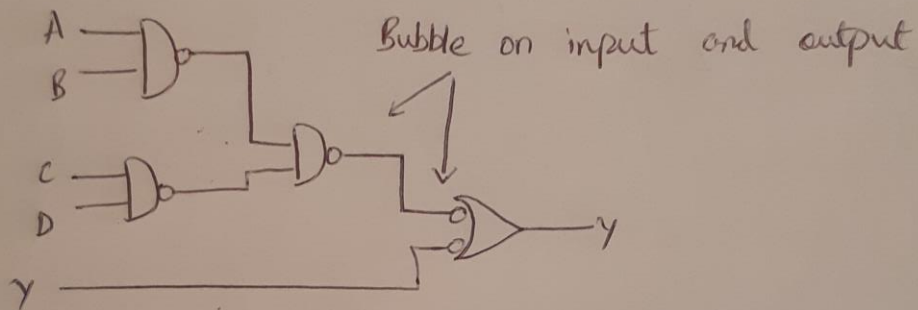


Figure 2.83 Circuit schematic

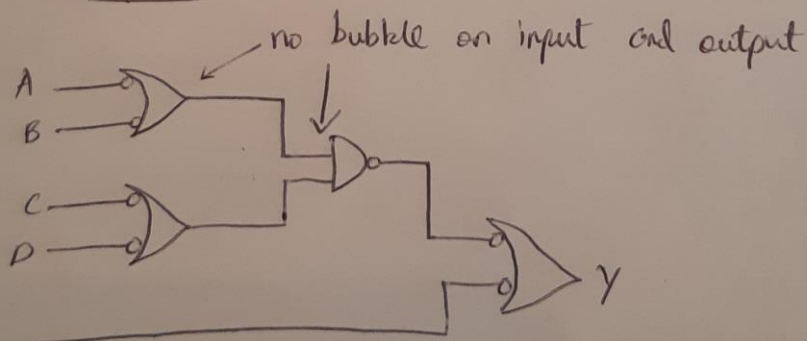
### Exercise 2.26



#### Step 1



#### Step 2

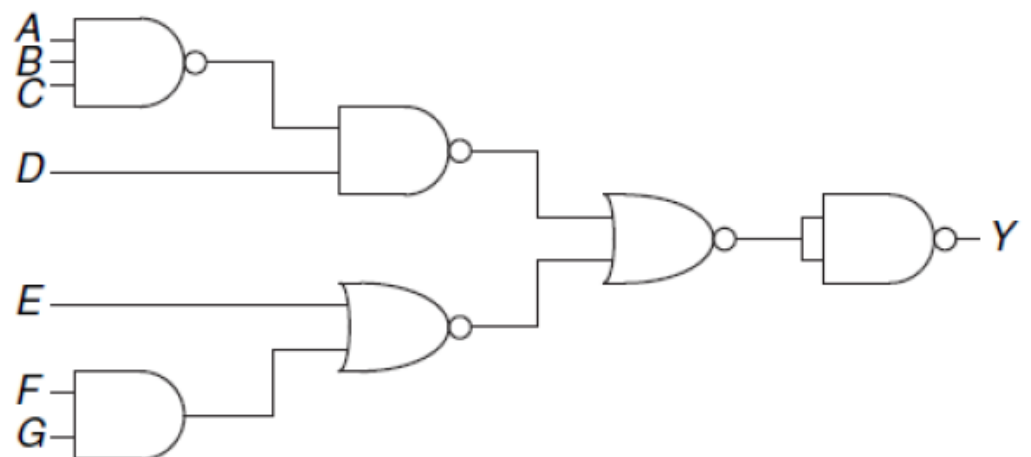


$$Y = (\overline{A+B}) \cdot (\overline{C+D}) + \overline{E}$$

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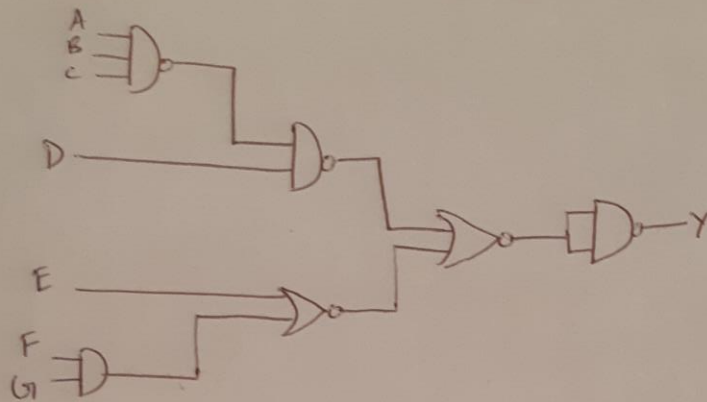
$$Y = \underline{\underline{(\overline{AB}) \cdot (\overline{CD})}} + \overline{E}$$

**Exercise 2.27** Repeat Exercise 2.26 for the circuit in Figure 2.84.

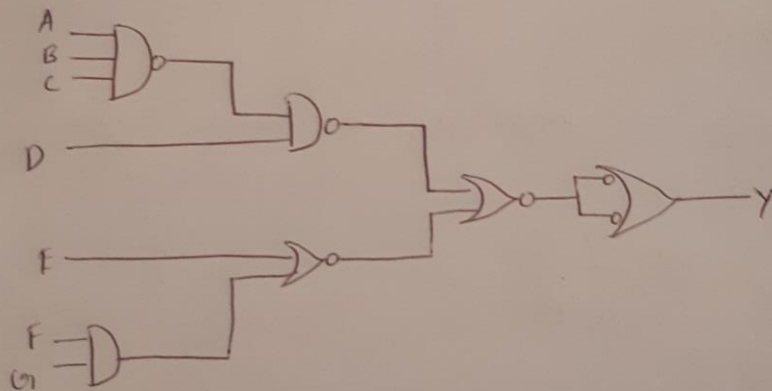


**Figure 2.84** Circuit schematic

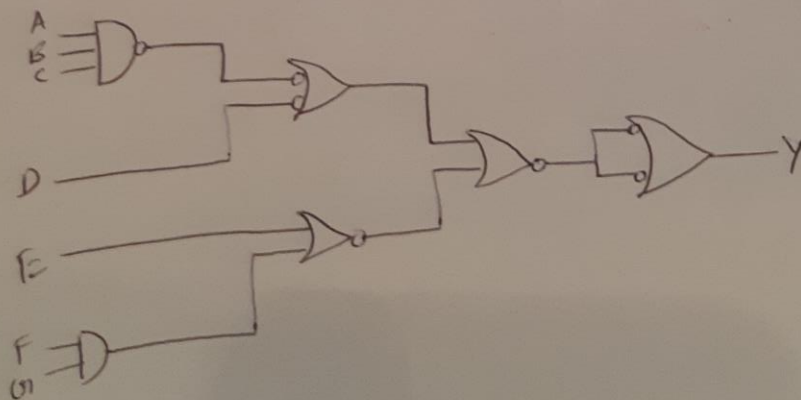
### Exercise 2.27:



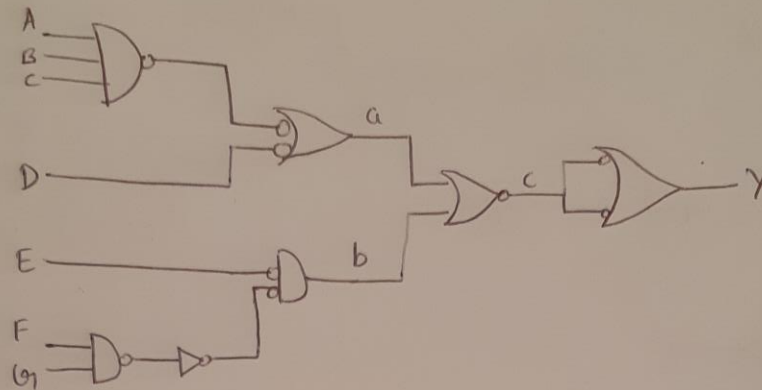
### Step 1:



### Step 2:



Step 3:



$$a = \overline{\overline{A \cdot B \cdot C}} + \overline{D}$$

$$b = \overline{E} + \overline{\overline{F \cdot G}}$$

$$= \overline{E} + \overline{F \cdot G} \Rightarrow \overline{E} \cdot \overline{F \cdot G}$$

$$c = \overline{((A \cdot B \cdot C) + \overline{D}) + (\overline{E} + \overline{F \cdot G})}$$

$$= \overline{(A \cdot B \cdot C) + \overline{D}} \cdot \overline{\overline{E} + \overline{F \cdot G}}$$

$$= \overline{(A \cdot B \cdot C) + \overline{D}} \cdot \overline{\overline{E}} \cdot \overline{\overline{F \cdot G}}$$

$$Y = \overline{\overline{c} + \overline{c}} = \overline{\overline{c}}$$

$$= \overline{(A \cdot B \cdot C) + \overline{D}} \cdot \overline{\overline{E}} \cdot \overline{\overline{F \cdot G}}$$

$$Y = \underline{\underline{(A \cdot B \cdot C) + \overline{D} + (\overline{E} \cdot \overline{F \cdot G})}}$$

**Exercise 2.28** Find a minimal Boolean equation for the function in Figure 2.85. Remember to take advantage of the don't care entries.

A	B	C	D	Y
0	0	0	0	X
0	0	0	1	X
0	0	1	0	X
0	0	1	1	0
0	1	0	0	0
0	1	0	1	X
0	1	1	0	0
0	1	1	1	X
1	0	0	0	1
1	0	0	1	0
1	0	1	0	X
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	X
1	1	1	1	1

**Figure 2.85** Truth table for Exercise 2.28

Exercise 2.28

K-map

		00	01	11	10
AB	00	X	X	0	X
	01	0	X	X	0
	11	1	1	1	X
	10	1	0	1	X

$Y = \underline{BD + A\bar{D} + AC}$

**Exercise 3.16** Suppose a ring oscillator is built from  $N$  inverters connected in a loop. Each inverter has a minimum delay of  $t_{cd}$  and a maximum delay of  $t_{pd}$ . If  $N$  is odd, determine the range of frequencies at which the oscillator might operate.

Exercise 3.16

Number of inverters =  $N$  (odd number)

minimum gate delay =  $t_{cd}$

maximum gate delay =  $t_{pd}$

$$\text{Frequency} = \frac{1}{N \times 2T}$$

The range of frequency at which the oscillator might operate is between  $\Rightarrow$

$$\underline{\underline{\frac{1}{2t_{cd}N} \quad \text{and} \quad \frac{1}{2t_{pd}N}}}$$

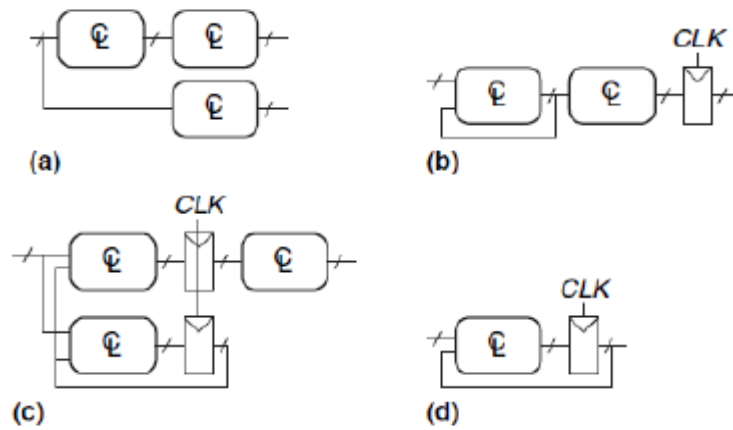
**Exercise 3.17** Why must  $N$  be odd in Exercise 3.16?

Exercise 3.17

For the ring oscillator to oscillate, a stable condition must not be attained. Even number of inverters stabilizes the oscillation. Therefore the number of inverters must be an odd number.



**Exercise 3.18** Which of the circuits in Figure 3.68 are synchronous sequential circuits? Explain.



### Exercise 3.18

Figure (a) and (b) are not synchronous sequential circuits because clock is not connected to each flip flops while figure (c) and (d) are synchronous sequential circuits because ~~each~~ each flip flops has its own clock.