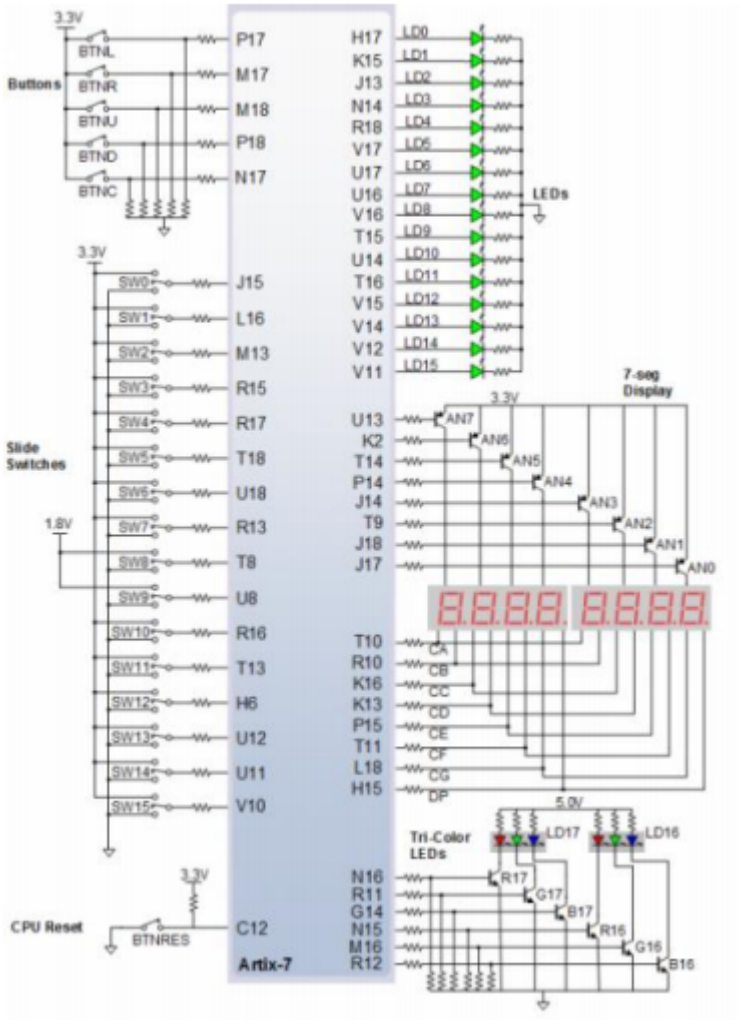
Lab 3: Introduction to Vivado

1. Figure with connection of 16 slide switches and 16 LEDs on Nexys A7 board.



2. Two-bit wide 4-to-1 multiplexer. Submit:

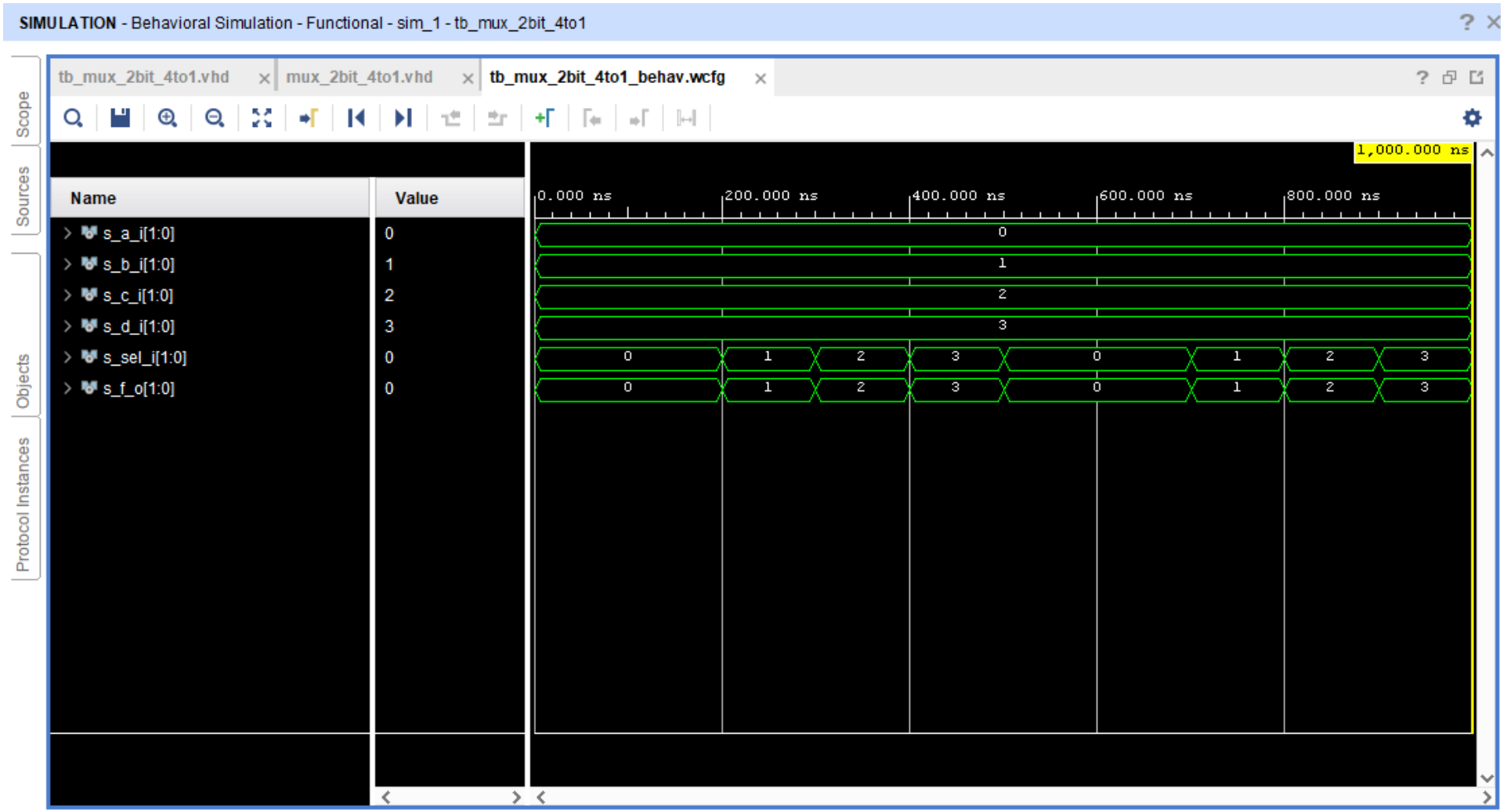
```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03.03.2021 19:54:51
-- Design Name:
```

```
-- Module Name: mux_2bit_4to1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity mux_2bit_4to1 is
    Port ( a_i : in STD_LOGIC_VECTOR (1 downto 0);
           b_i : in STD_LOGIC_VECTOR (1 downto 0);
           c_i : in STD_LOGIC_VECTOR (1 downto 0);
           d_i : in STD_LOGIC_VECTOR (1 downto 0);
           sel_i : in STD_LOGIC_VECTOR (1 downto 0);
           f_o : out STD_LOGIC_VECTOR (1 downto 0));
end mux_2bit_4to1;

architecture Behavioral of mux_2bit_4to1 is
begin
```

```
f_o <= a_i when sel_i = "00" else
       b_i when sel_i = "01" else
       c_i when sel_i = "10" else
       d_i when sel_i = "11";


end Behavioral;



----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03.03.2021 20:25:32
-- Design Name:
-- Module Name: tb_mux_2bit_4to1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
```

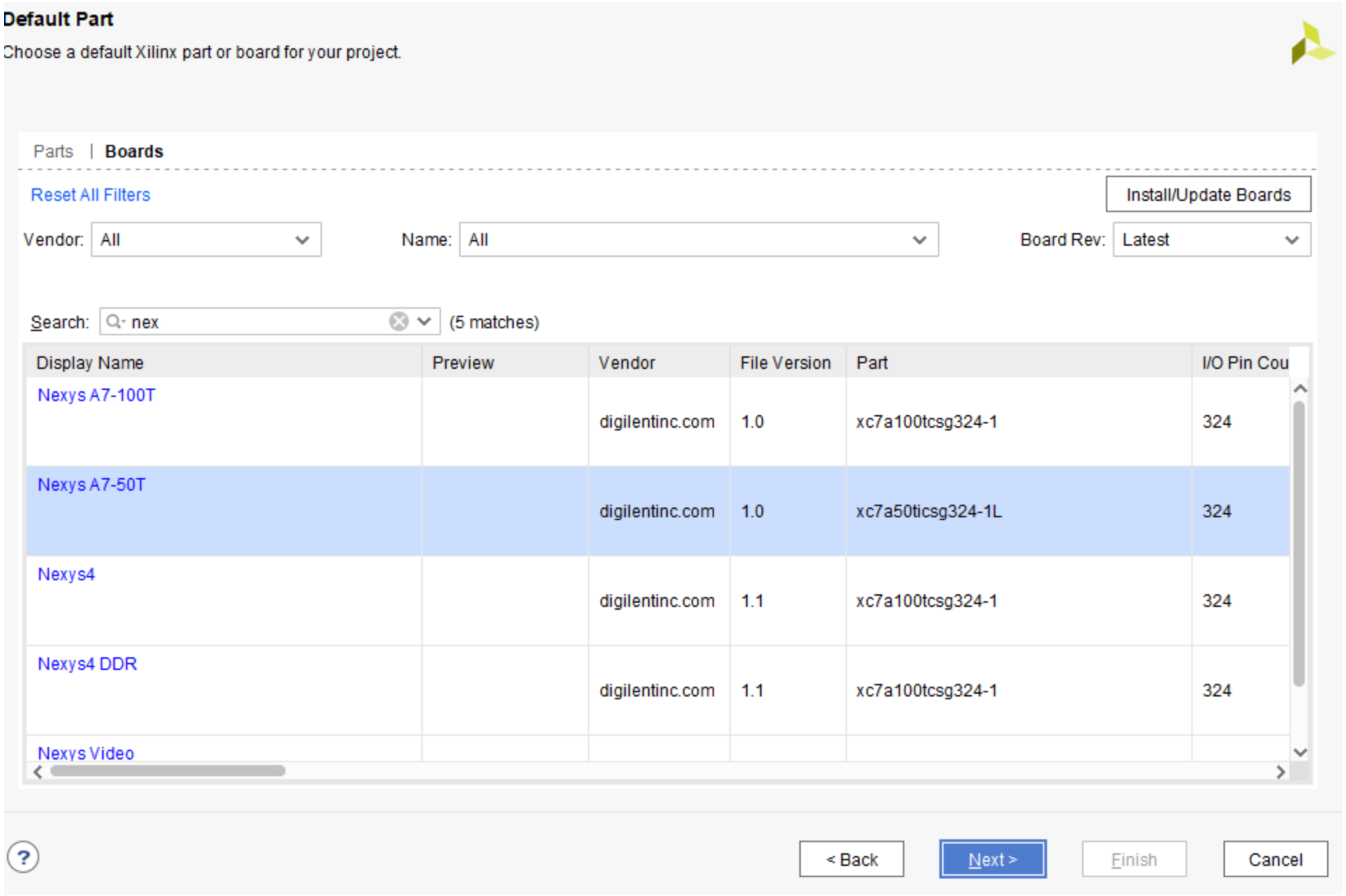
```
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity tb_mux_2bit_4to1 is
end entity;

architecture test of tb_mux_2bit_4to1 is

    signal s_a_i : std_logic_vector(1 downto 0);
    signal s_b_i : std_logic_vector(1 downto 0);
    signal s_c_i : std_logic_vector(1 downto 0);
    signal s_d_i : std_logic_vector(1 downto 0);
    signal s_sel_i : std_logic_vector(1 downto 0);
    signal s_f_o : std_logic_vector(1 downto 0);

begin
    -- Connecting testbench signals with comparator_2bit entity (Unit Under Test)
    uut_mux_2bit_4to1: entity work.mux_2bit_4to1
        port map(
            a_i           => s_a_i,
            b_i           => s_b_i,
            c_i           => s_c_i,
            d_i           => s_d_i,
            sel_i         => s_sel_i,
            f_o           => s_f_o
        );

    ------------------------------------------------------------------
    -- Data generation process
    ------------------------------------------------------------------
    p_stimulus : process
    begin
        -- Report a note at the beginning of stimulus process
        report "Stimulus process started" severity note;

        s_a_i <= "00";
        s_b_i <= "01";
        s_c_i <= "10";
```

```
        s_d_i <= "11";
        s_sel_i <= "00";

        wait for 100 ns;
        -- First test values

        s_sel_i <= "00";  wait for 100 ns;
        s_sel_i <= "01";  wait for 100 ns;
        s_sel_i <= "10";  wait for 100 ns;
        s_sel_i <= "11";  wait for 100 ns;


    end process  p_stimulus;

end test;
```

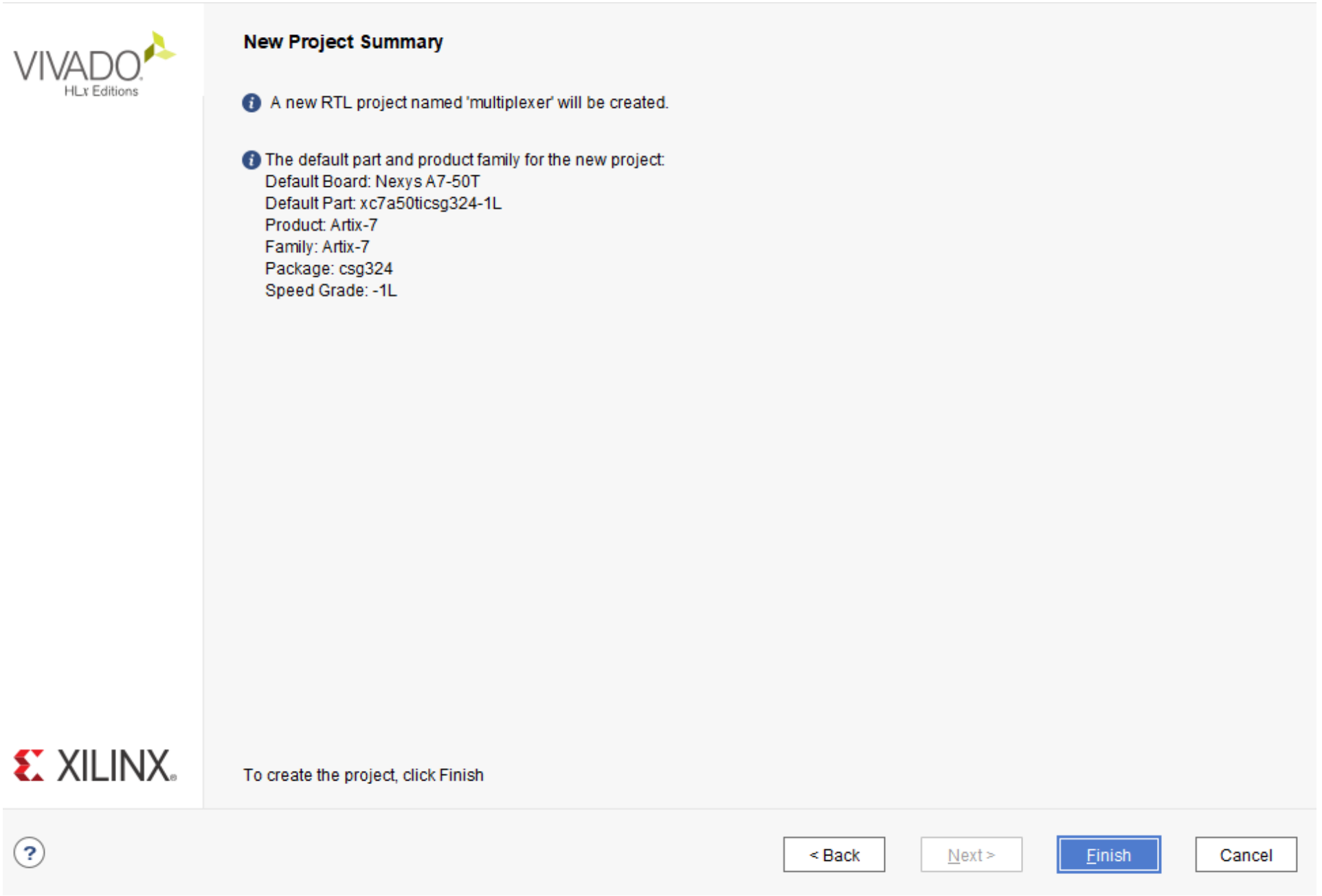


3. Vivado Tutorial

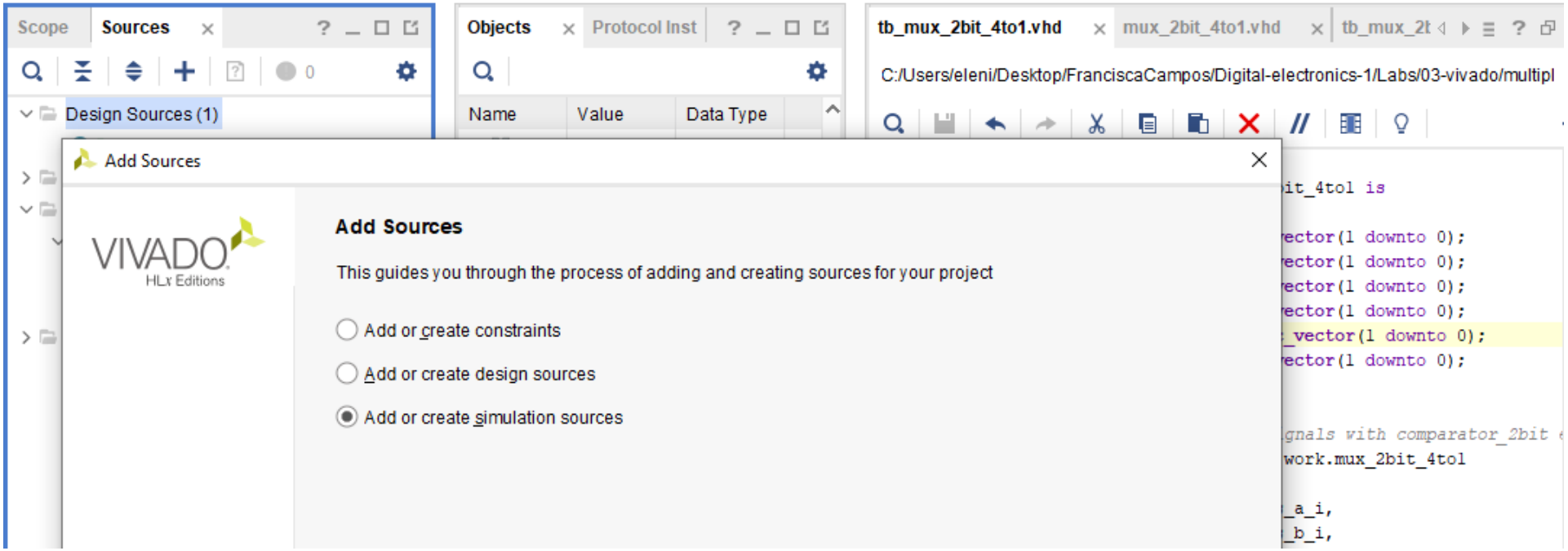
First we create a project and pick the corresponding board. In our case Nexys A7-50T

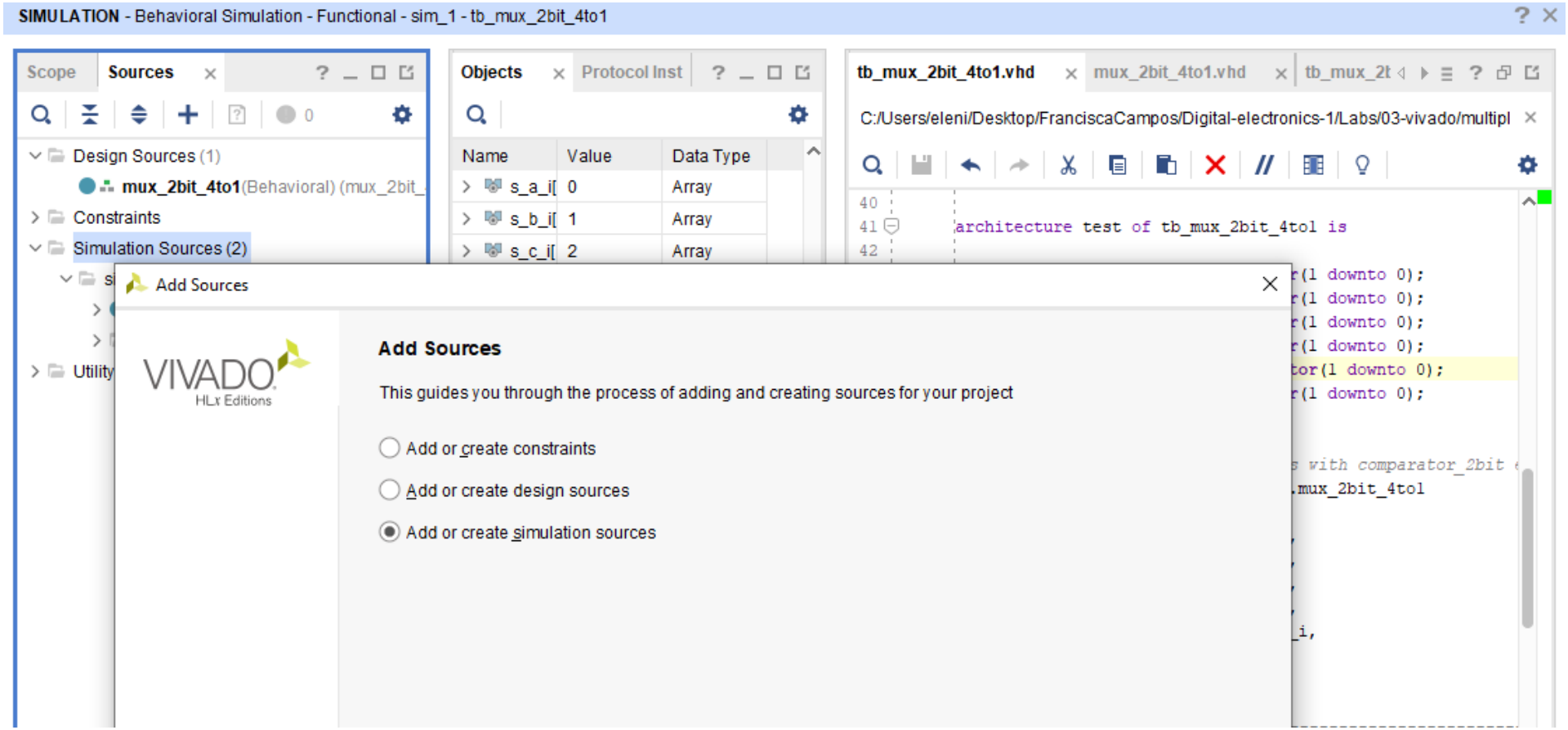


Then we´ll see the summary of the created project



Once we have our project created, we add the design and the simulation files, in our case the design and the testbench. Also, we edit the .xdc file and save it.





tb_mux_2bit_4to1.vhd | mux_2bit_4to1.vhd | tb_mux_2bit_4to1_behav.wcfg | **nexys-a7-50t.xdc**

C:/Users/eleni/Desktop/FranciscaCampos/Digital-electronics-1/Labs/03-vivado/multiplexer/multiplexer.srcs/constrs_1/imports/XDCFile/nexys-a7-50t.xdc

```
4  ## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
5
6  ## Clock signal
7  #set_property -dict { PACKAGE_PIN E3    IOSTANDARD LVCMOS33 } [get_ports { CLK100MHZ }]; #IO_L12P_T1_MRCC_35 Sch=clk100mhz
8  #create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports {CLK100MHZ}];
9
10
11 ##Switches
12 set_property -dict { PACKAGE_PIN J15   IOSTANDARD LVCMOS33 } [get_ports { a_i[0] }]; #IO_L24N_T3_RS0_15 Sch=sw[0]
13 set_property -dict { PACKAGE_PIN L16   IOSTANDARD LVCMOS33 } [get_ports { a_i[1] }]; #IO_L3N_T0_DQS_EMCCLK_14 Sch=sw[1]
14 set_property -dict { PACKAGE_PIN M13   IOSTANDARD LVCMOS33 } [get_ports { b_i[0] }]; #IO_L6N_T0_D08_VREF_14 Sch=sw[2]
15 set_property -dict { PACKAGE_PIN R15   IOSTANDARD LVCMOS33 } [get_ports { b_i[1] }]; #IO_L13N_T2_MRCC_14 Sch=sw[3]
16 set_property -dict { PACKAGE_PIN R17   IOSTANDARD LVCMOS33 } [get_ports { c_i[0] }]; #IO_L12N_T1_MRCC_14 Sch=sw[4]
17 set_property -dict { PACKAGE_PIN T18   IOSTANDARD LVCMOS33 } [get_ports { c_i[1] }]; #IO_L7N_T1_D10_14 Sch=sw[5]
18 set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports { d_i[0] }]; #IO_L17N_T2_A13_D29_14 Sch=sw[6]
19 set_property -dict { PACKAGE_PIN R13   IOSTANDARD LVCMOS33 } [get_ports { d_i[1] }]; #IO_L5N_T0_D07_14 Sch=sw[7]
20 #set_property -dict { PACKAGE_PIN T8    IOSTANDARD LVCMOS18 } [get_ports { SW[8] }]; #IO_L24N_T3_34 Sch=sw[8]
21 #set_property -dict { PACKAGE_PIN U8    IOSTANDARD LVCMOS18 } [get_ports { SW[9] }]; #IO_25_34 Sch=sw[9]
22 #set_property -dict { PACKAGE_PIN R16   IOSTANDARD LVCMOS33 } [get_ports { SW[10] }]; #IO_L15P_T2_DQS_RDWR_B_14 Sch=sw[10]
23 #set_property -dict { PACKAGE_PIN T13   IOSTANDARD LVCMOS33 } [get_ports { SW[11] }]; #IO_L23P_T3_A03_D19_14 Sch=sw[11]
24 #set_property -dict { PACKAGE_PIN H6    IOSTANDARD LVCMOS33 } [get_ports { SW[12] }]; #IO_L24P_T3_35 Sch=sw[12]
25 #set_property -dict { PACKAGE_PIN U12   IOSTANDARD LVCMOS33 } [get_ports { SW[13] }]; #IO_L20P_T3_A08_D24_14 Sch=sw[13]
26 set_property -dict { PACKAGE_PIN U11   IOSTANDARD LVCMOS33 } [get_ports { sel_i[0] }]; #IO_L19N_T3_A09_D25_VREF_14 Sch=sw[14]
27 set_property -dict { PACKAGE_PIN V10   IOSTANDARD LVCMOS33 } [get_ports { sel_i[0] }]; #IO_L21P_T3_DQS_14 Sch=sw[15]
28
29 ## LEDs
```