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Francisco E. Soriano

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EDUCATION

M.S. Computer Engineering, *University of Central Florida, Orlando, FL.* **Jan. 2025 - Dec. 2026**
GPA: 4.0 - Computer Systems & VLSI Design Specialization

B.S. Computer Engineering, *University of Central Florida, Orlando, FL.* **Jun. 2021 - Dec. 2024**
GPA: 3.8 - Digital VLSI Circuits Track

A.A. General Studies, *Eastern Florida State College, Cocoa, FL.* **Jun. 2018 - May 2021**
GPA: 4.0 - Recipient of 31st Annual Community Service-Learning Award

Graduate Courses: *Verification & Validation of Digital Systems: The Complete Industry Lifecycle, CAD of VLSI, Modern EDA Algorithms in VLSI, Performance Analysis of Computer & Communication Systems*

WORK & RESEARCH EXPERIENCE

Silicon Design Engineer Intern **May 2024 - Aug. 2024**
Advanced Micro Devices (AMD) Inc.

- Analyzing current bottleneck in the RDNA Graphics Pipeline & micro-architecture for GPU optimization and collaborating with Engineers regarding potential solutions to reduce latency within it.
- Utilizing AsciiDoc to document/update proposal for Hardware Architecture designed for speed-up.
- Tracing & tying ports/signals within RTL datapath via top-down approach between corresponding Verilog files.
- Utilizing Verdi to view waveforms & verify existing latency within datapath of Graphics Pipeline using load/drive signals.
- Giving intermediate technical presentations depicting RTL signal traces & proposed Architecture for latency optimization.
- Designing & implementing a custom RISC-V instruction extension designed for decreasing existing latency.
- Designing & modifying RTL to support the new instruction's functionality, in addition to running specific validation tests.
- Creating & modifying Firmware to support instruction integration followed by running tests & strategic debugging.
- Analyzing the existing Design Verification Testbench designed for where the instruction extension would be used.
- Analyzing the Static Timing Analysis workflow performed, in addition to learning how to architect for speed.
- Creating an inaugural Intern Reference Guide for future AMD Orlando Interns containing essential links, commands, and FAQs that will rapidly speed up intern adaptation to the company.
- Presenting Summer accomplishments/deliverables to Orlando site & Hardware Architecture Team.

AMD x UCF Undergraduate Research Fellow **Sep. 2023 - Now**
University of Central Florida (UCF) - College of Engineering & Computer Science (CECS)

- Analyzing how low power design strategies are specified and managed by Unified Power Format (UPF).
- Debugging/revising lab colleagues' Verilog implementations and providing extensive Industry standard feedback.
- Designing efficient RTL & testbenches to generate waveform solutions for Digital Systems Lab Curriculum at UCF.
- Implementing a parameterized ALU in Verilog of a RISC-V Single Cycle 32 instruction set according to its specifications.
- Implementing and pipelining bit-width parameterized RTL modules in Verilog for a Barrett Multiplier & Montgomery Multiplier to increase throughput & reduce latency.
- Designing comprehensive testbenches in Verilog to simulate & verify correct module functionality based on expected outputs/generated simulation waveforms.
- Delivering technical presentations to Research team and AMD Executives on fellowship findings.

Generative AI Projection Mapping Capstone Project Manager/Leader **Jan. 2024 - Now**
University of Central Florida (UCF) - College of Engineering & Computer Science (CECS)

- Designing a PCB with strategic placement/layout/traces using Fusion360 to supply power to a Raspberry Pi 4B.
- Integrating API data fetching and dynamic image display in project Qt application, improving user interaction by asynchronously displaying fetched images.
- Designing a strategic & compact 3D CAD enclosure to house the main project components.

EDUCATIONAL OUTREACH

UCF IEEE GBM Panelist, *UCF x AMD* **Sep. 5th, 2024**
UCF ACM GBM Panelist, *UCF x AMD* **Sep. 6th, 2024**
Introduction to Engineering - Undergraduate Lab Instructor, *UCF* **Aug. 2023 - Dec. 2023**

SKILLS

Communication:	English & Spanish (Native: Read, Speak, Write), Portuguese (Read)
Languages:	Verilog, SystemVerilog, Python, C/C++, Java, HTML, CSS, AsciiDoc, LaTeX
Hardware:	PCB Design/Layout/Routing/Assembly, Soldering, CAD, BASYS 3 FPGA, Digital Multimeter
Software:	Verdi, Linux, VSCode, Xilinx-Vivado, Fusion 360, Perforce, ETX, Git/Github, MobaXterm