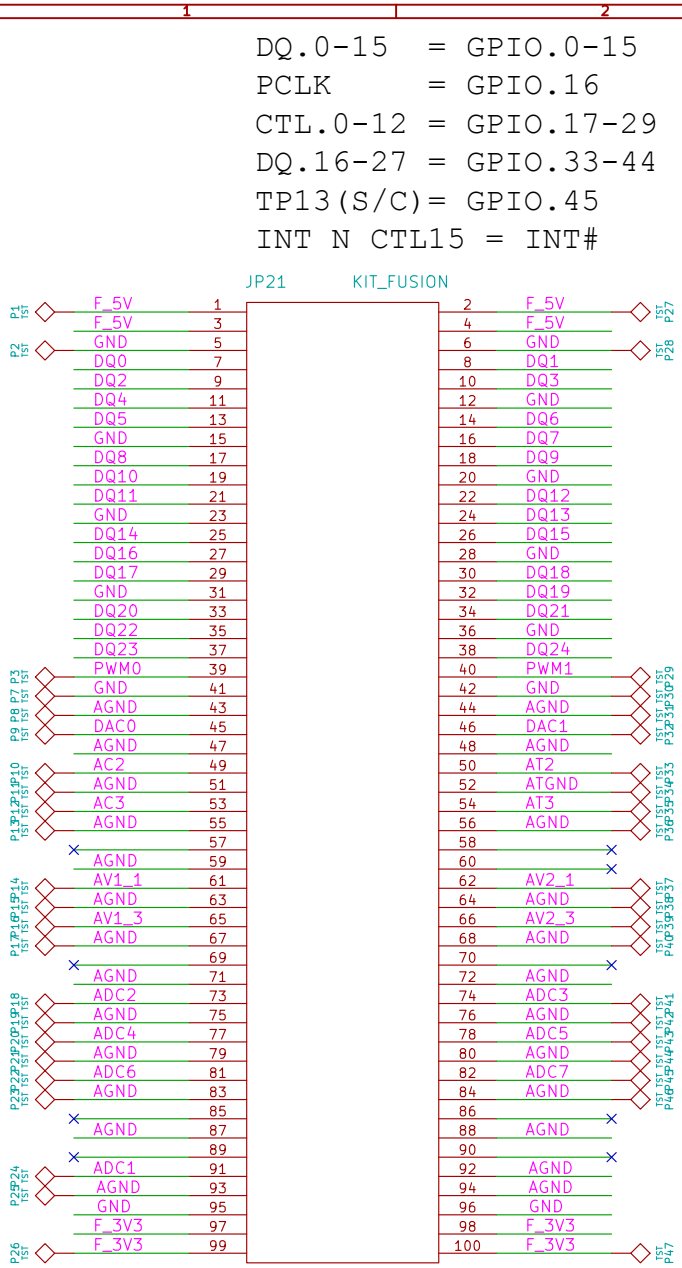
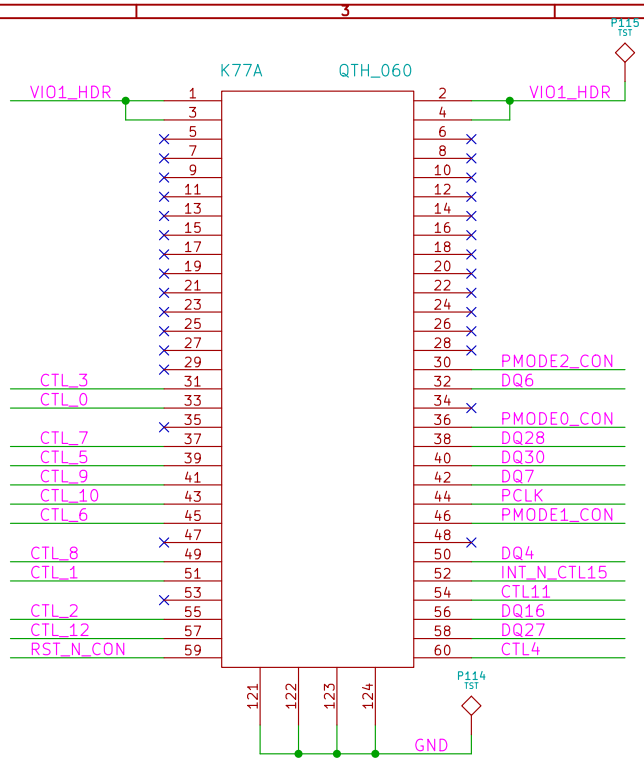
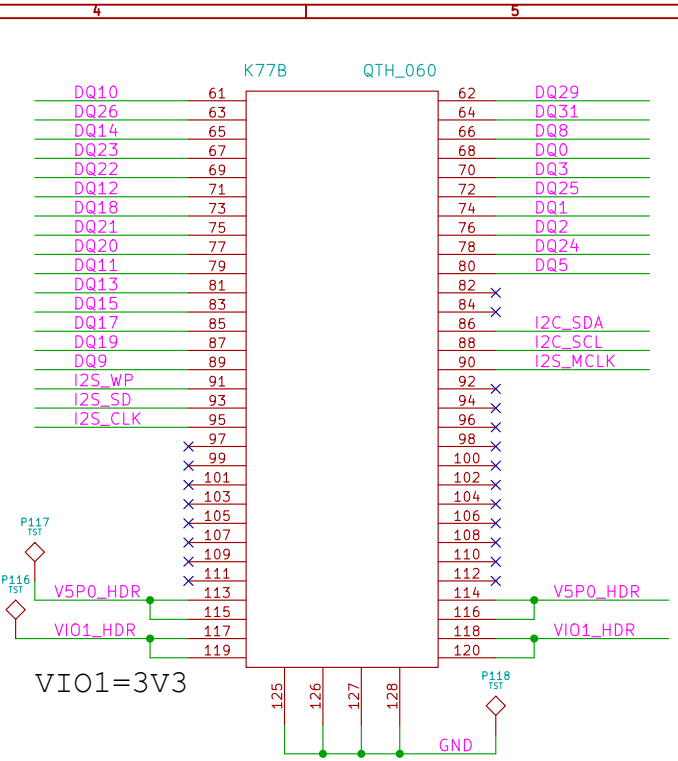
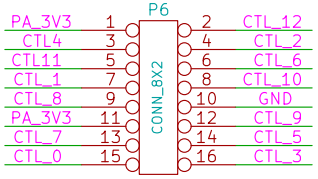
DQ.0-15 = GPIO.0-15
PCLK = GPIO.16
CTL.0-12 = GPIO.17-29
DQ.16-27 = GPIO.33-44
TP13(S/C)= GPIO.45
INT N CTL15 = INT#

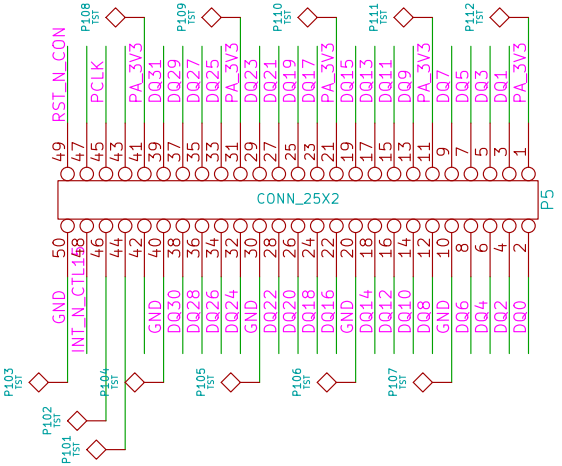




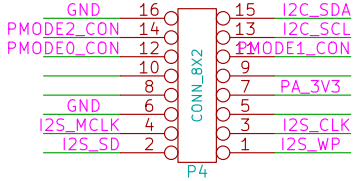


VIO1=3V3





PMODE.0-2=GPIO.30-32
I2C SDA/SCL=GPIO59/58

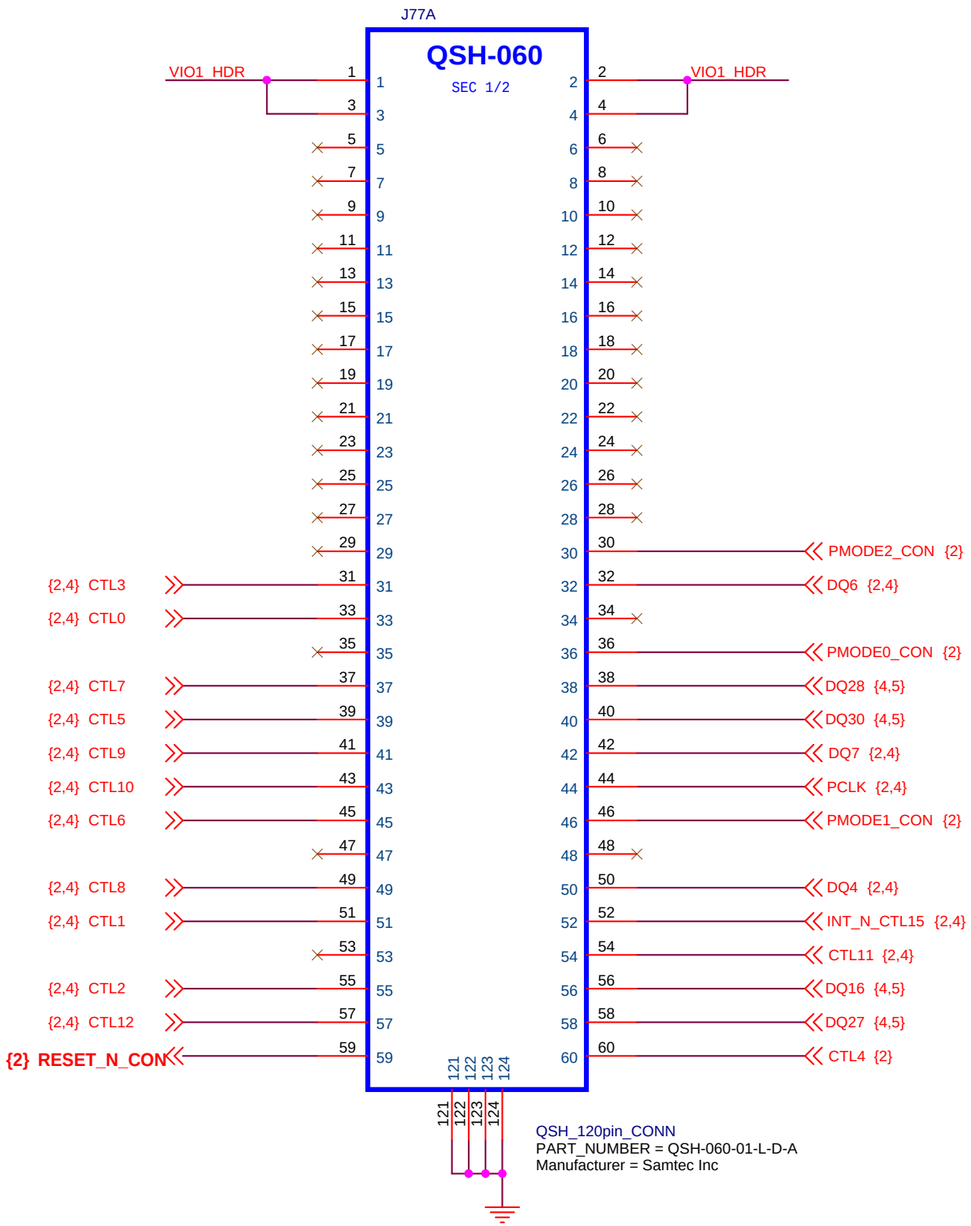


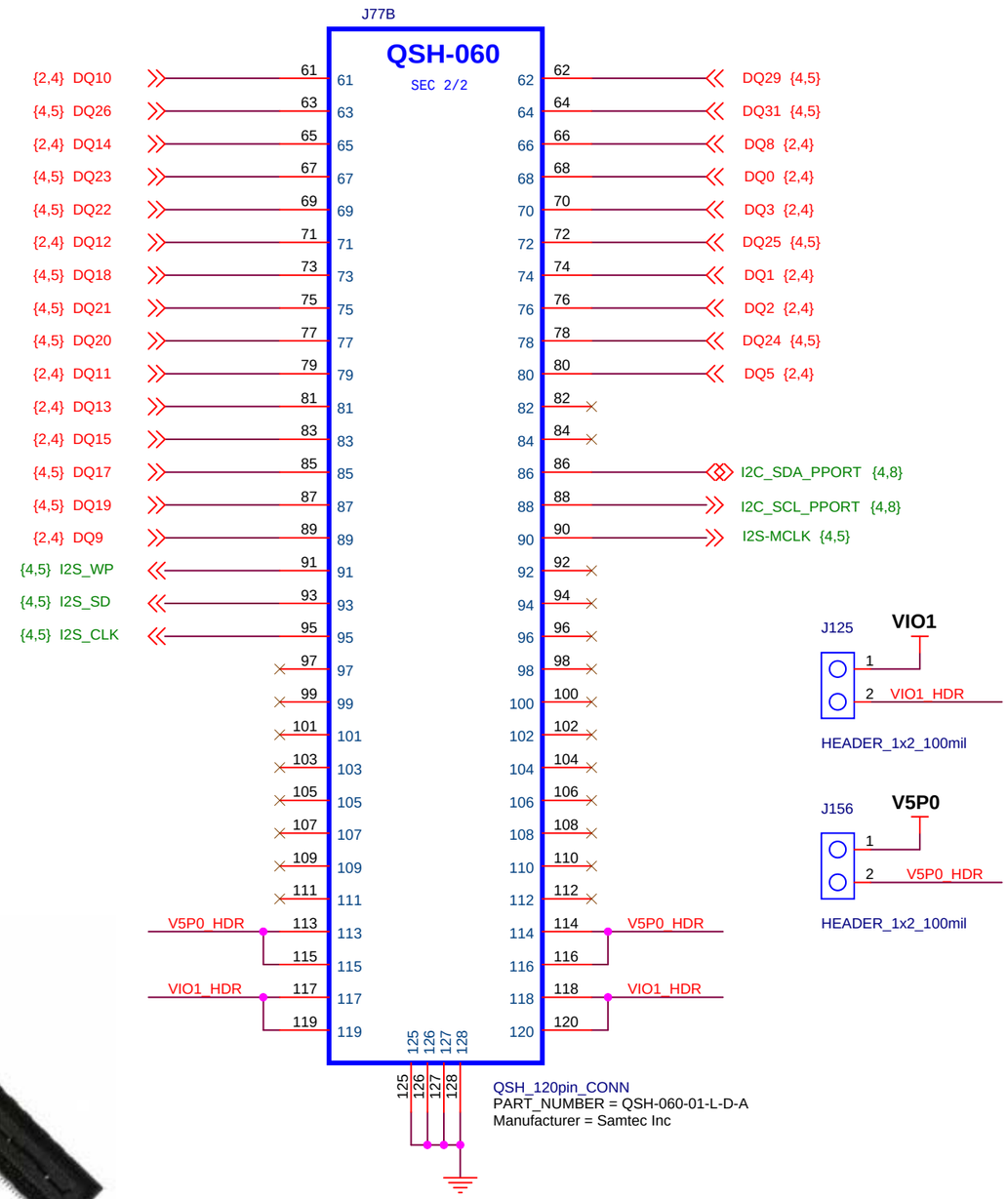
I2S_MCLK = GPIO.57
I2S_CLK = GPIO.50
I2S_SD = GPIO.51
I2S_WP = GPIO.52

DQ.28 = UART_RTS = GPIO.46
DQ.29 = UART_CTS = GPIO.47
DQ.30 = UART_TX = GPIO.48
DQ.31 = UART_RX = GPIO.49

FIUBA-LABCATyP-2014		
File: u3_fusion.sch		
Sheet: /		
Title: Interfaz entre kit CYUSB3KIT-001-FX3 y kit fusion		
Size: A4	Date: 10 dec 2013	Rev: 01
KiCad E.D.A.		Id: 1/1

P PORT TO SAMTEC





Title: FX3 DVK DEVICE BOARD		
Size: B	Document Number: 630-60013-01 REV02	Rev: 2.0
Date: Thursday, September 08, 2011	Sheet 3 of 14	

P-PORT CONNECTIONS

U1A

P - PORT

SEC 1/7

VIO1

DQ0	F10	R5	22	DQ0	DQ0 {3,4}
DQ1	F9	R205	22	DQ1	DQ1 {3,4}
DQ2	F7	R206	22	DQ2	DQ2 {3,4}
DQ3	G10	R207	22	DQ3	DQ3 {3,4}
DQ4	G9	R208	22	DQ4	DQ4 {3,4}
DQ5	F8	R209	22	DQ5	DQ5 {3,4}
DQ6	H10	R210	22	DQ6	DQ6 {3,4}
DQ7	H9	R211	22	DQ7	DQ7 {3,4}
DQ8	J10	R212	22	DQ8	DQ8 {3,4}
DQ9	J9	R213	22	DQ9	DQ9 {3,4}
DQ10	K11	R214	22	DQ10	DQ10 {3,4}
DQ11	L10	R215	22	DQ11	DQ11 {3,4}
DQ12	K10	R216	22	DQ12	DQ12 {3,4}
DQ13	K9	R217	22	DQ13	DQ13 {3,4}
DQ14	J8	R218	22	DQ14	DQ14 {3,4}
DQ15	G8	R219	22	DQ15	DQ15 {3,4}
PCLK	J6	R220	22	PCLK	PCLK {3,4}
CTL0	K8	R221	22	CTL0	CTL0 {3,4}
CTL1	K7	R222	22	CTL1	CTL1 {3,4}
CTL2	J7	R223	22	CTL2	CTL2 {3,4}
CTL3	H7	R224	22	CTL3	CTL3 {3,4}
CTL4	G7	R225	22	CTL4_SW	CTL4_SW {4}
CTL5	G6	R226	22	CTL5	CTL5 {3,4}
CTL6	K6	R227	22	CTL6	CTL6 {3,4}
CTL7	H8	R228	22	CTL7	CTL7 {3,4}
CTL8	G5	R229	22	CTL8	CTL8 {3,4}
CTL9	H6	R230	22	CTL9	CTL9 {3,4}
CTL10	K5	R231	22	CTL10	CTL10 {3,4}
CTL11	J5	R232	22	CTL11	CTL11 {3,4}
CTL12	H5	R233	22	CTL12	CTL12 {3,4}
PMODE0	G4	R234	22	PMODE_0	
PMODE1	H4	R235	22	PMODE_1	
PMODE2	L4	R236	22	PMODE_2	
INT_N_CTL15	L8			INT_N_CTL15	INT_N_CTL15 {3,4}
RESET_N	C5			RESET_N	RESET_N {4}

VIO1 — R170 DNL

FX3_121_BUMP

{3} PMODE0_CON — J96: 1 PMODE_0, 2 PMODE_0_DIP, 3

{3} PMODE1_CON — J97: 1 PMODE_1, 2 PMODE_1_DIP, 3

{3} PMODE2_CON — J98: 1 PMODE_2, 2 PMODE_2_DIP, 3

{3} CTL4 — J100: 1 CTL4_SW, 2 CTL4_LT, 3

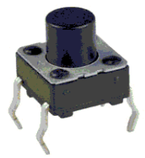
VIO1

R7 10K, R8 10K, R19 10K

SW25: PMODE_0_DIP 1/8, PMODE_1_DIP 2/7, PMODE_2_DIP 3/6, 4/5

DIP_SWITCH_4POS
PART_NUMBER = 218-4LPST
Manufacturer = CTS Electrocomponents

RESET_CONNECTION



SW8 PBSwitch
A1, A2, B1, B2
GND
PART_NUMBER = EVQPAC07K
Manufacturer = Panasonic

CVDDQ — R63 100K

C1 0.1uF C0402

CVDDQ — R10 10K R0402

RESET_SWITCH
RESET_N
{3} RESET_N_CON

J72: 1, 2, 3

HEADER_1x3_100mil

VIO1 — C2 0.1uF C0402

VIO1 — R11 10K R0402

U45

1	VCCA	VCCB	6
CTL4_LT 3	A	B	4 — USB_DRV_VBUS {9}
5	OE	GND	2

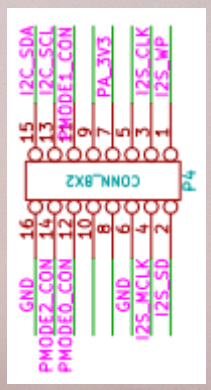
V5P0 — C3 0.1uF C0402

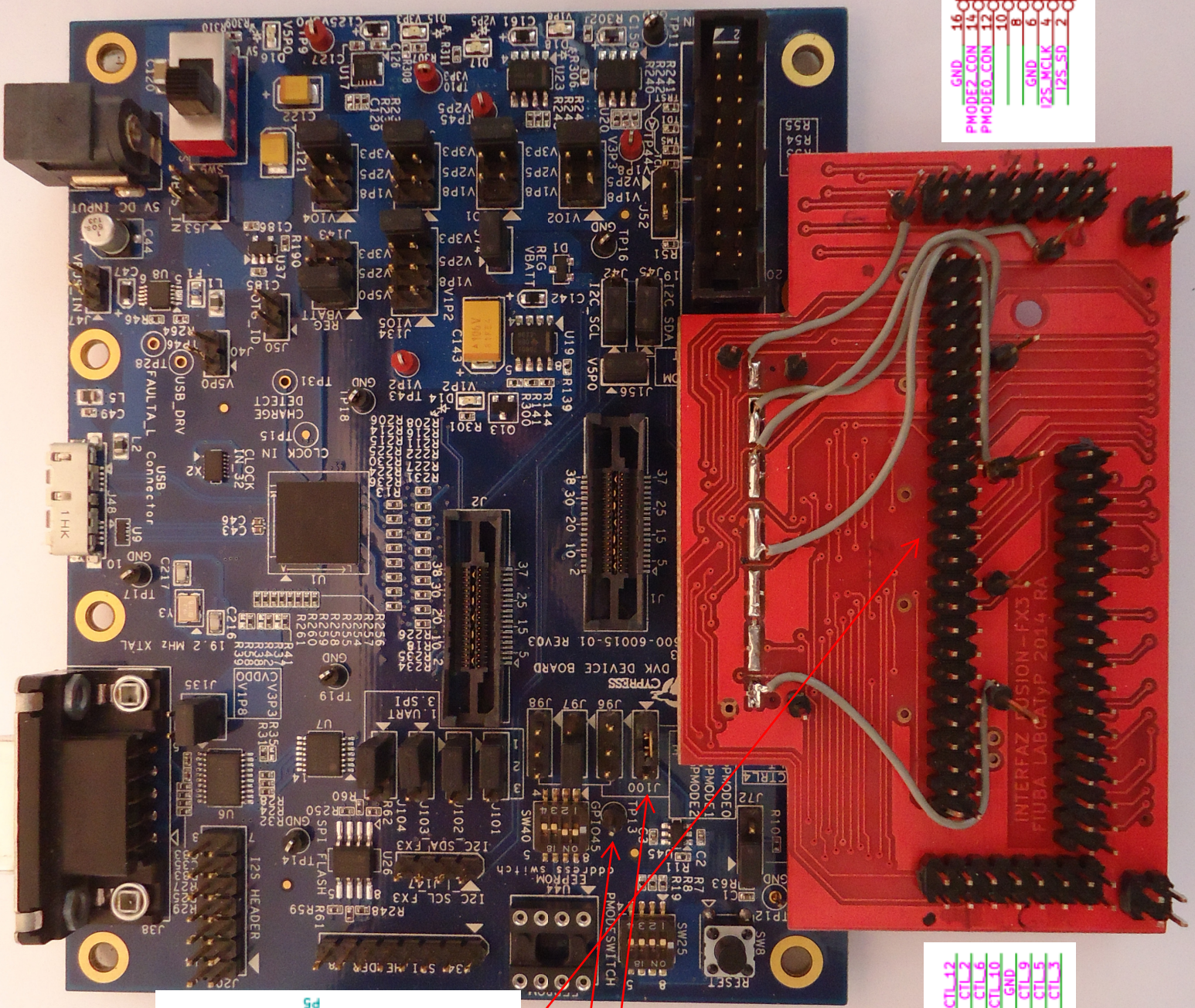
BI_LVL_TRANS_1BIT
PART_NUMBER = TXS0101DBVR
Manufacturer = TI

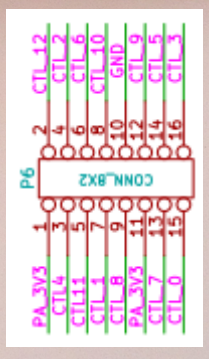
Title	FX3 DVK DEVICE BOARD		
Size B	Document Number 630-60013-01 REV02		Rev 2.0
Date: Thursday, September 08, 2011	Sheet 2 of 14		

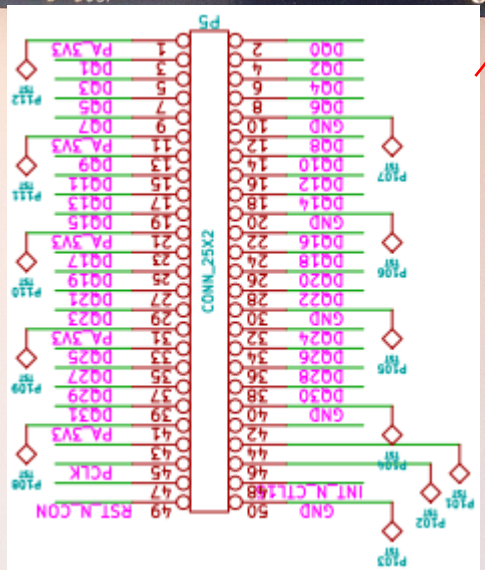
DQ.0-15 = GPIO.0-15
PCLK = GPIO.16
CTL.0-12 = GPIO.17-29
DQ.16-27 = GPIO.33-44
TP13(S/C)= GPIO.45
INT N CTL15 = INT#

PMODE.0-2=GPIO.30-32
I2C_SDA/SCL=GPIO59/58
I2S_MCLK = GPIO.57
I2S_CLK = GPIO.50
I2S_SD = GPIO.51
I2S_WP = GPIO.52









TP13=GPIO45

J100
3. 2. 1.
CTL4_SW puenteado con CTL4

DQ.28 = UART_RTS = GPIO.46
DQ.29 = UART_CTS = GPIO.47
DQ.30 = UART_TX = GPIO.48
DQ.31 = UART_RX = GPIO.49

Pin Description

Table 16. Pin List

Pin		I/O	Name	Description	
				GPIFII (VIO1 Power Domain) J136: 3V3	
				GPIF™II Interface	Slave FIFO Interface
F10	VIO1	I/O	GPIO[0]	DQ[0]	DQ[0]
F9	VIO1	I/O	GPIO[1]	DQ[1]	DQ[1]
F7	VIO1	I/O	GPIO[2]	DQ[2]	DQ[2]
G10	VIO1	I/O	GPIO[3]	DQ[3]	DQ[3]
G9	VIO1	I/O	GPIO[4]	DQ[4]	DQ[4]
F8	VIO1	I/O	GPIO[5]	DQ[5]	DQ[5]
H10	VIO1	I/O	GPIO[6]	DQ[6]	DQ[6]
H9	VIO1	I/O	GPIO[7]	DQ[7]	DQ[7]
J10	VIO1	I/O	GPIO[8]	DQ[8]	DQ[8]
J9	VIO1	I/O	GPIO[9]	DQ[9]	DQ[9]
K11	VIO1	I/O	GPIO[10]	DQ[10]	DQ[10]
L10	VIO1	I/O	GPIO[11]	DQ[11]	DQ[11]
K10	VIO1	I/O	GPIO[12]	DQ[12]	DQ[12]
K9	VIO1	I/O	GPIO[13]	DQ[13]	DQ[13]
J8	VIO1	I/O	GPIO[14]	DQ[14]	DQ[14]
G8	VIO1	I/O	GPIO[15]	DQ[15]	DQ[15]
J6	VIO1	I/O	GPIO[16]	PCLK	CLK
K8	VIO1	I/O	GPIO[17]	CTL[0]	SLCS#
K7	VIO1	I/O	GPIO[18]	CTL[1]	SLWR#
J7	VIO1	I/O	GPIO[19]	CTL[2]	SLOE#
H7	VIO1	I/O	GPIO[20]	CTL[3]	SLRD#
G7	VIO1	I/O	GPIO[21]	CTL[4]	FLAGA
G6	VIO1	I/O	GPIO[22]	CTL[5]	FLAGB
K6	VIO1	I/O	GPIO[23]	CTL[6]	GPIO
H8	VIO1	I/O	GPIO[24]	CTL[7]	PKTEND#
G5	VIO1	I/O	GPIO[25]	CTL[8]	GPIO
H6	VIO1	I/O	GPIO[26]	CTL[9]	GPIO
K5	VIO1	I/O	GPIO[27]	CTL[10]	GPIO
J5	VIO1	I/O	GPIO[28]	CTL[11]	A1
H5	VIO1	I/O	GPIO[29]	CTL[12]	A0
G4	VIO1	I/O	GPIO[30]	PMODE[0]	PMODE[0]
H4	VIO1	I/O	GPIO[31]	PMODE[1]	PMODE[1]
L4	VIO1	I/O	GPIO[32]	PMODE[2]	PMODE[2]
L8	VIO1	I/O	INT#	INT#/CTL[15]	CTL[15]
C5	CVDDQ	I	RESET#	RESET#	RESET#
				IO2 (VIO2 Power Domain)	
				GPIF II (32-bit data mode)	
K2	VIO2	I/O	GPIO[33]	DQ[16]	GPIO
J4	VIO2	I/O	GPIO[34]	DQ[17]	GPIO
K1	VIO2	I/O	GPIO[35]	DQ[18]	GPIO
J2	VIO2	I/O	GPIO[36]	DQ[19]	GPIO
J3	VIO2	I/O	GPIO[37]	DQ[20]	GPIO

Table 16. Pin List (continued)

Pin		I/O	Name	Description					
J1	VIO2	I/O	GPIO[38]	DQ[21]				GPIO	
H2	VIO2	I/O	GPIO[39]	DQ[22]				GPIO	
H3	VIO2	I/O	GPIO[40]	DQ[23]				GPIO	
F4	VIO2	I/O	GPIO[41]	DQ[24]				GPIO	
G2	VIO2	I/O	GPIO[42]	DQ[25]				GPIO	
G3	VIO2	I/O	GPIO[43]	DQ[26]				GPIO	
F3	VIO2	I/O	GPIO[44]	DQ[27]				GPIO	
F2	VIO2	I/O	GPIO[45]	GPIO					
				IO3 (VIO3 Power Domain) J145: 3V3					
				GPIO+SPI	GPIO+UART	GPIO only	GPIF II - 32 (FX3)+UART+I2S	GPIO+I2S	UART+SPI+ I2S
F5	VIO3	I/O	GPIO[46]	GPIO	GPIO	GPIO	DQ[28]	GPIO	UART_RTS
E1	VIO3	I/O	GPIO[47]	GPIO	GPIO	GPIO	DQ[29]	GPIO	UART_CTS
E5	VIO3	I/O	GPIO[48]	GPIO	GPIO	GPIO	DQ[30]	GPIO	UART_TX
E4	VIO3	I/O	GPIO[49]	GPIO	GPIO	GPIO	DQ[31]	GPIO	UART_RX
D1	VIO3	I/O	GPIO[50]	GPIO	GPIO	GPIO	I2S_CLK	GPIO	I2S_CLK
D2	VIO3	I/O	GPIO[51]	GPIO	GPIO	GPIO	I2S_SD	GPIO	I2S_SD
D3	VIO3	I/O	GPIO[52]	GPIO	GPIO	GPIO	I2S_WS	GPIO	I2S_WS
				IO4 (VIO4) Power Domain					
D4	VIO4	I/O	GPIO[53]	SPI_SCK	UART_RTS	GPIO	UART_RTS	GPIO	SPI_SCK
C1	VIO4	I/O	GPIO[54]	SPI_SSN	UART_CTS	GPIO	UART_CTS	I2S_CLK	SPI_SSN
C2	VIO4	I/O	GPIO[55]	SPI_MISO	UART_TX	GPIO	UART_TX	I2S_SD	SPI_MISO
D5	VIO4	I/O	GPIO[56]	SPI_MOSI	UART_RX	GPIO	UART_RX	I2S_WS	SPI_MOSI
C4	VIO4	I/O	GPIO[57]	GPIO	GPIO	GPIO	I2S_MCLK	I2S_MCLK	I2S_MCLK
				USB Port (VBATT/VBUS Power Domain)					
C9	VBUS/ VBATT	I	OTG_ID	OTG_ID					
				USB Port (U3TXVDDQ/U3RXVDDQ Power Domain)					
A3	U3RXVDDQ	I	SSRXM	SSRX-					
A4	U3RXVDDQ	I	SSRXP	SSRX+					
A6	U3TXVDDQ	O	SSTXM	SSTX-					
A5	U3TXVDDQ	O	SSTXP	SSTX+					
				USB Port (VBATT/VBUS Power Domain)					
A9	VBUS/VBATT	I/O	DP	D+					
A10	VBUS/VBATT	I/O	DM	D-					
A11			NC	No connect					
				Crystal/Clocks (CVDDQ Power Domain)					
B2	CVDDQ	I	FSLC[0]	FSLC[0]					
C6	AVDD	I/O	XTALIN	XTALIN					
C7	AVDD	I/O	XTALOUT	XTALOUT					
B4	CVDDQ	I	FSLC[1]	FSLC[1]					
E6	CVDDQ	I	FSLC[2]	FSLC[2]					
D7	CVDDQ	I	CLKIN	CLKIN					
D6	CVDDQ	I	CLKIN_32	CLKIN_32					
				I2C and JTAG (VIO5 Power Domain) J134: 3V3					
D9	VIO5	I/O	I2C_GPIO[58]	I^2C_SCL					
D10	VIO5	I/O	I2C_GPIO[59]	I^2C_SDA					

Table 16. Pin List (continued)

Pin		I/O	Name	Description
E7	VIO5	I	TDI	TDI
C10	VIO5	O	TDO	TDO
B11	VIO5	I	TRST#	TRST#
E8	VIO5	I	TMS	TMS
F6	VIO5	I	TCK	TCK
D11	VIO5	I/O	O[60]	Charger detect output
				Power
E10		PWR	VBATT	
B10		PWR	VDD	
A1		PWR	U3VSSQ	
E11		PWR	VBUS	
D8		PWR	VSS	
H11		PWR	VIO1	
E2		PWR	VSS	
L9		PWR	VIO1	
G1		PWR	VSS	
F1		PWR	VIO2	
G11		PWR	VSS	
E3		PWR	VIO3	
L1		PWR	VSS	
B1		PWR	VIO4	
L6		PWR	VSS	
B6		PWR	CVDDQ	
B5		PWR	U3TXVDDQ	
A2		PWR	U3RXVDDQ	
C11		PWR	VIO5	
L11		PWR	VSS	
A7		PWR	AVDD	
B7		PWR	AVSS	
C3		PWR	VDD	
B8		PWR	VSS	
E9		PWR	VDD	
B9		PWR	VSS	
F11		PWR	VDD	
H1		PWR	VDD	
L7		PWR	VDD	
J11		PWR	VDD	
L5		PWR	VDD	
K4		PWR	VSS	
L3		PWR	VSS	
K3		PWR	VSS	
L2		PWR	VSS	
A8		PWR	VSS	
				Precision Resistors
C8	VBUS/VBATT	I/O	R_usb2	Precision resistor for USB 2.0 (Connect a 6.04 kΩ+/-1% resistor between this pin and GND)
B3	U3TXVDDQ	I/O	R_usb3	Precision resistor for USB 3.0 (Connect a 200 Ω+/-1% resistor between this pin and GND)