Special reset, USPTO 4,486,827 by Shima et al.

Needed only for FPGAs

fpga_reset

reset_in

M1
T2

clk

(End of patented circuit)

Required 3 clock reset cycles to clear PC and IR

clrpc_int

nclk

resets.bdf

PROJECT	A-Z80	MODULE	resets
DESIGNER	Goran Devic		
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