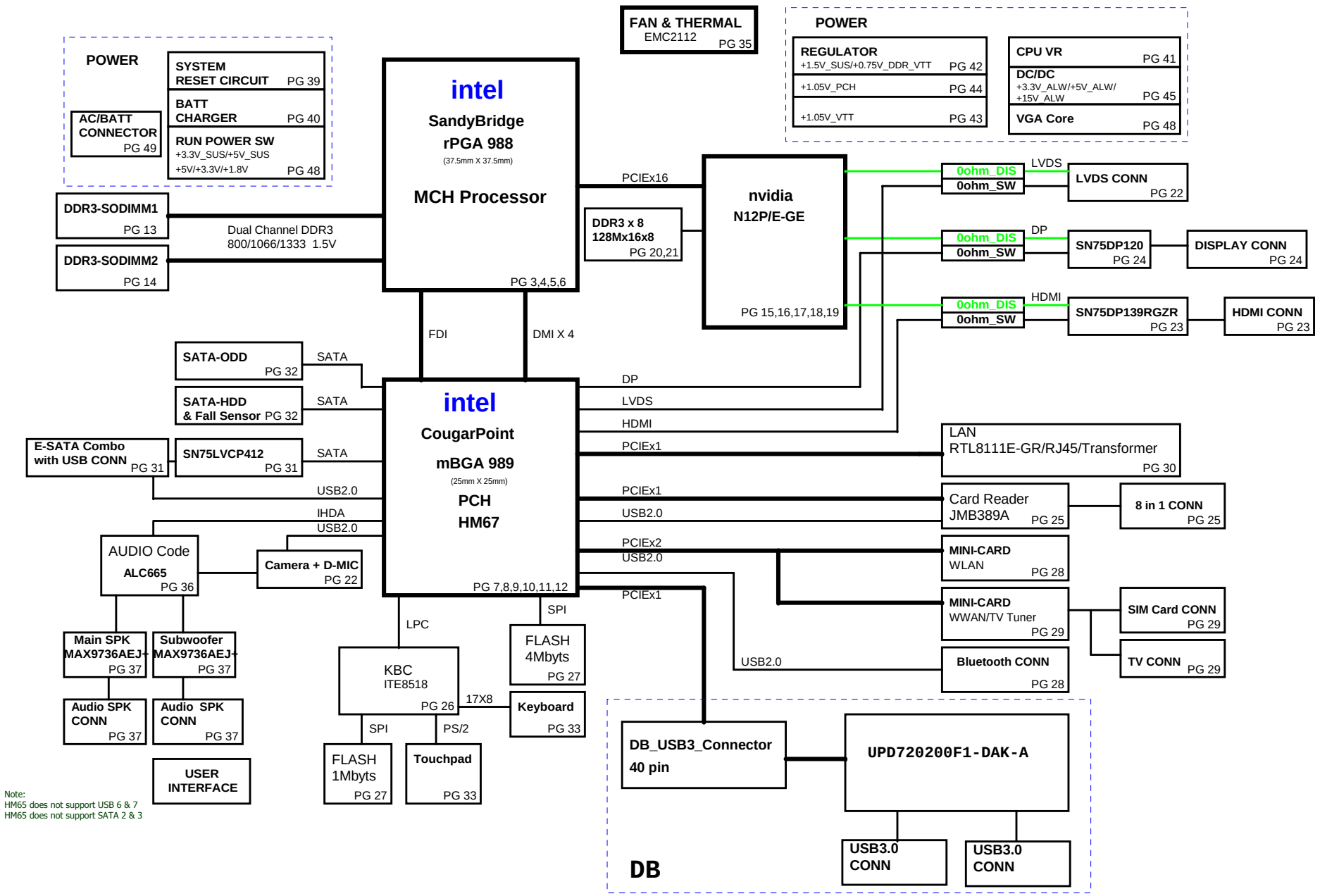
_DIS ==> Discrete Only
_SW ==> Optimus Only
_UMA ==> UMA Only

# GM6C MLK Optimus, Discrete & UMA

VER : 1A
PWA:
PWB:




Note:
HM65 does not support USB 6 & 7
HM65 does not support SATA 2 & 3

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | Block Diagram | 1A |

Date: Friday, August 27, 2010 Sheet 1 of 57

## Table of Contents



## Power States

| POWER PLANE | VOLTAGE | PAGE | DESCRIPTION | CONTROL SIGNAL | ACTIVE IN |
|---|---|---|---|---|---|
| +PWR_SRC | 10V~+19V | 24,30,45,46,47,48,49,50,51 | MAIN POWER | | S0~S5 |
| +RTC_CELL | +3.0V~+3.3V | 08,11,29,30 | RTC | | S0~S5 |
| +5V_ALW2 | +5V | 37,46,52,53 | LARGE POWER | MAIN POWER | S0~S5 |
| +5V_ALW | +5V | 13,33,44,46,47,48,49,50,51,52 | LARGE POWER | ALW_ON | S0~S5 |
| +3.3V_ALW | +3.3V | 29,30,35,36,37,42,44,45,46,47,51,52,53 | 8051 POWER | 3.3V_ALW_ON | S0~S5 |
| +5V_SUS | +5V | 11,33,34,37,51,52 | SLP_S5# CTRLD POWER | SUS_ON | |
| +3.3V_SUS | +3.3V | 07,08,09,10,11,13,14,19,24,28,29,37,41,42,44 ,48,49,50,52 | SLP_S5# CTRLD POWER | SUS_ON | |
| +1.5V_SUS | +1.5V | 03,05,13,14,47,50,52 | SODIMM POWER | SUS_ON | |
| +0.75V_DDR_VTT | +0.75V | 13,14,47,52 | SODIMM POWER | RUN_ON | |
| +5V_RUN | +5V | 11,18,24,25,35,36,38,39,40,51,52 | SLP_S3# CTRLD POWER | RUN_ON | |
| +3.3V_RUN | +3.3V | 3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30 ,31,32,33,35,37,38,39,40,41,42,46,51,52,60 | SLP_S3# CTRLD POWER | RUN_ON | |
| +1.8V_RUN | +1.8V | 05,11,44,52 | SDVO POWER | RUN_ON | |
| +1.8V_RUN_GFX | +1.8V | 17,18,21,22,44,52 | VGA POWER | RUN_ON | |
| +1.5V_RUN | +1.5V | 11,18,19,20,28,31,32,52 | VGA POWER | RUN_ON | |
| +VCC_GFX_CORE | +0.9V~+1.2V | 18,21,50 | VGA POWER | RUN_ON | |
| +1.05V_PCH | +1.05V | 08,09,11,15,48 | PCH POWER | RUN_ON | |
| +VCC_CORE | +0.7V~+1.77V | 05,51 | CPU CORE POWER | IMVP_VR_ON | |
| +LCDVCC | +3.3V | 24 | LCD Power | LCDVCC_TST_EN & ENVDD | |
| +5V_MOD | +5V | 35 | MOD Power | MODC_EN | |
| +5V_HDD | +5V | 35 | HDD Power | HDDC_EN | |
| +1.1V_VTT | +1.1V | 03,05,10,11,49,60 | CPU POWER | RUN_ON | |
| +1.1V_GFX_PCIE | +1.1V | 18,50 | VGA POWER | GFX_ON | |

| GND PLANE | PAGE | DESCRIPTION |
|---|---|---|
| GND | ALL | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | Frontage | 1A |

Date: Friday, August 27, 2010 Sheet 2 of 57

# Sandy Bridge Processor (DMI,PEG,FDI)

# Sandy Bridge Processor (CLK,MISC,JTAG)

WW31.MOW Page 5

U28A

DMI

Intel(R) FDI

PCI EXPRESS* - GRAPHICS

eDP

CPU-989P-rPGA

U28B

MISC

CLOCKS

THERMAL

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

CPU-989P-rPGA

0727

0716

0803

0802

remove PCH_PECI(07/12)

change to R01 schematic (not ready)

If need a buffer? 0624 (NO)

0.22uF AC coupling caps for PCIE GEN1/2/3

level shift for reset pin(07/12)

(07/13)

| IN | OUT |
|---|---|
| L | L |
| H | High-Z |

S3 Power reduce 0803

26.1 change to 25 ohm

| | DIS | SW |
|---|---|---|
| Ra | NA | 0 ohm |
| Rb | 1K ohm | NA |
| Rc | 1K ohm | NA |

Option for Prochot# function
68 ohm for unused, 62 ohm for used

DG(V0.5) P66:
1. FDI_FSYNC[0], FDI_FSYNC[1],
FDI_LSYNC[0],FDI_LSYNC[1]
can be tied to GND (through 1K ±5% resistors);
In addition, can be ganged together
with one resistor[1K ±5% resistors].
2. If left as no connect, there is no functional impact,
but power (~15mW) may be wasted.

## DP & PEG Compensation

3/16 Change topology;
Add AND gate based on DG rev0.9

02/25 Update R8232, R8233 value and routing,
Add R8583 follow PDG 0.71 #440484

S3 Power reduce

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | Sandy Bridge 1/4 | 1A |

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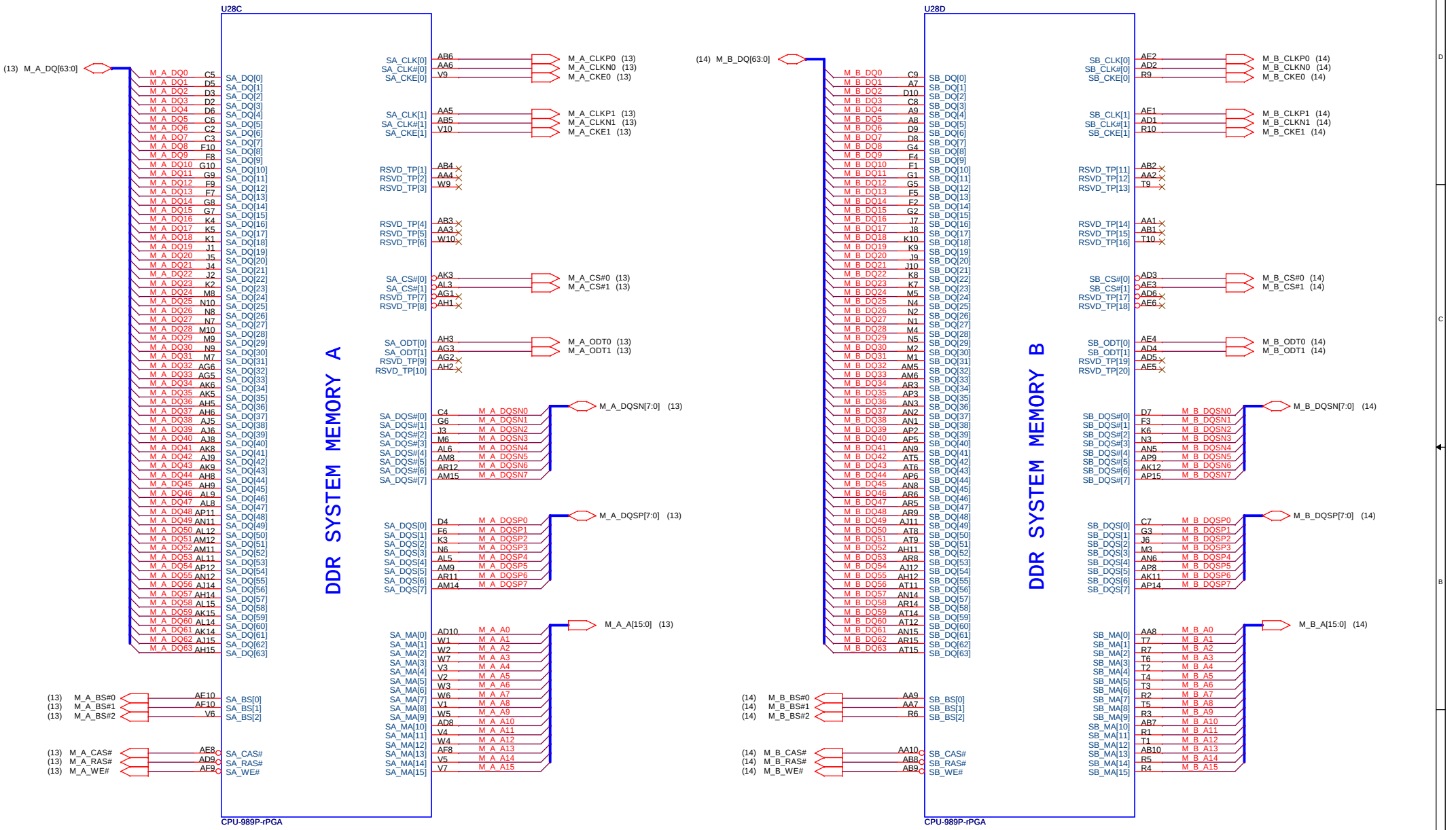
# Sandy Bridge Processor (DDR3)




Quanta Computer Inc.

PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | Sandy Bridge 2/4 | 1A |

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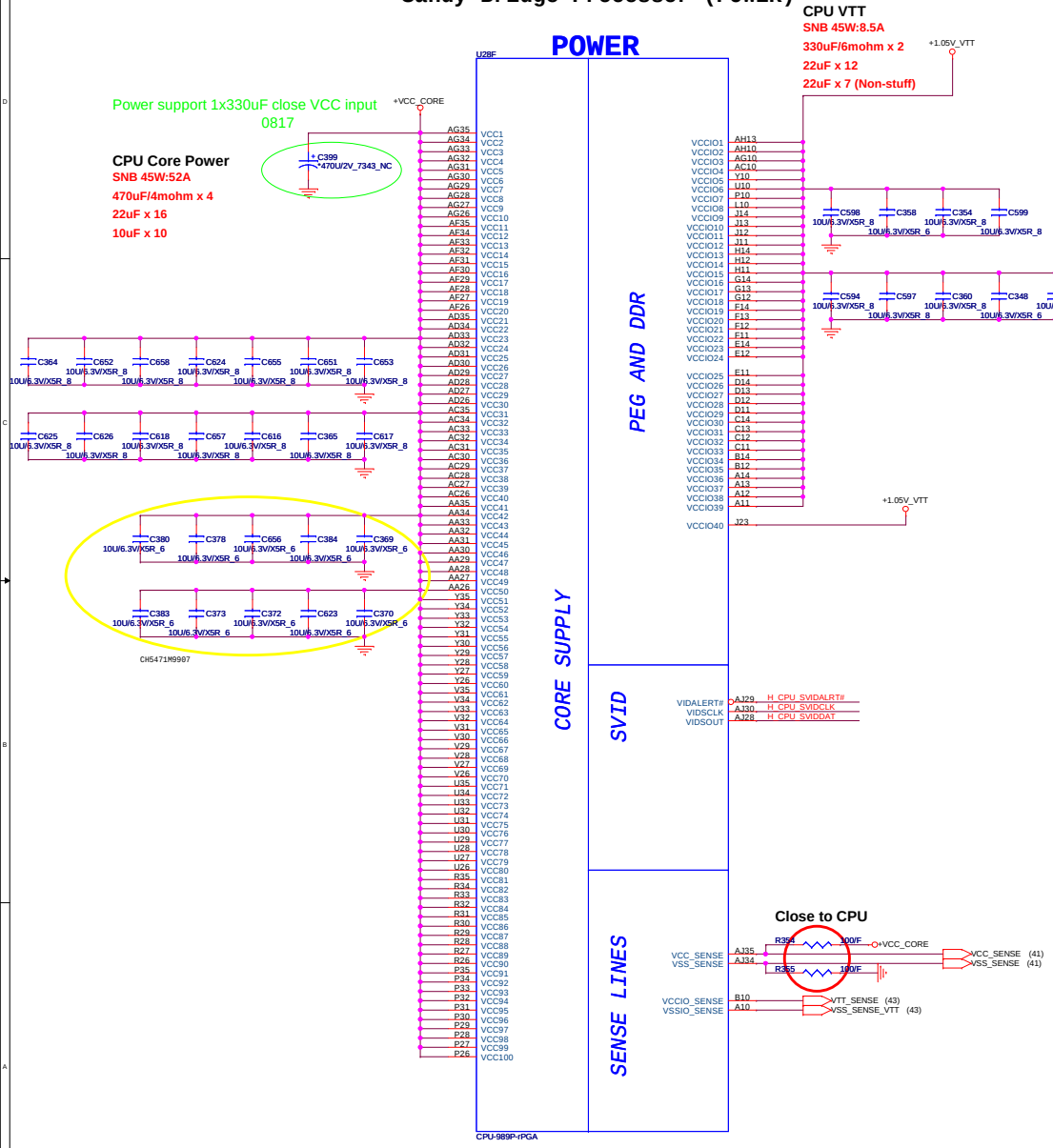
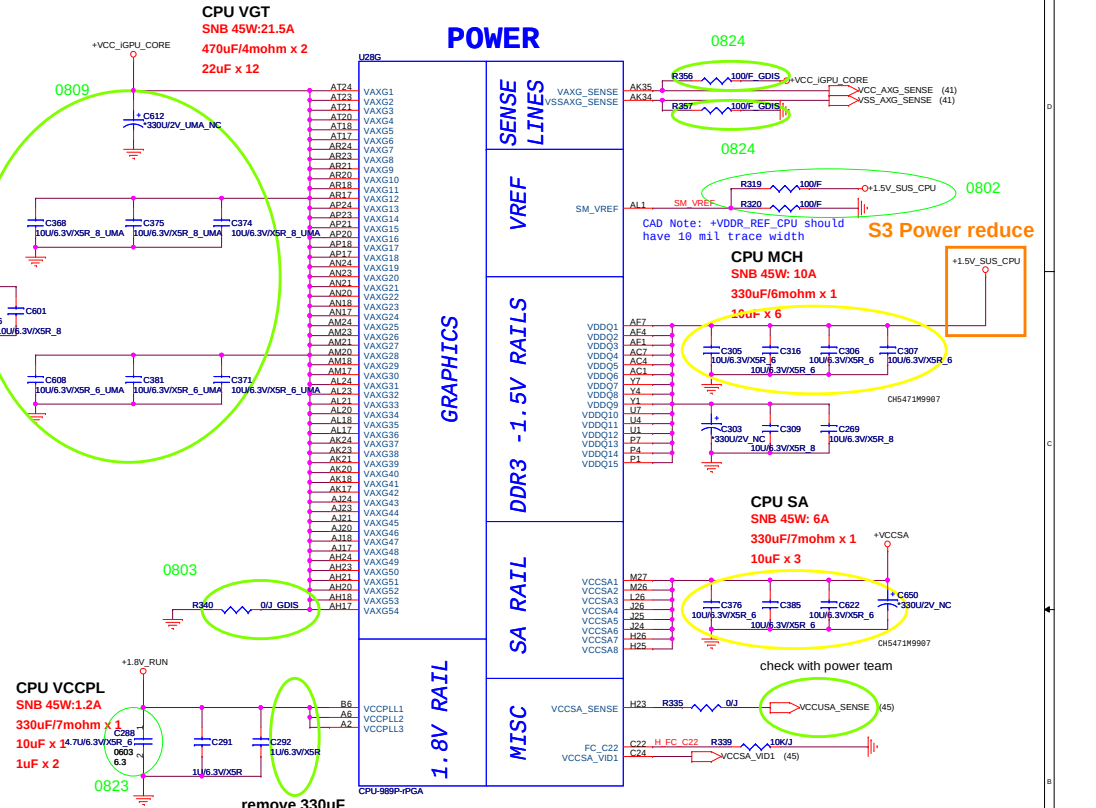
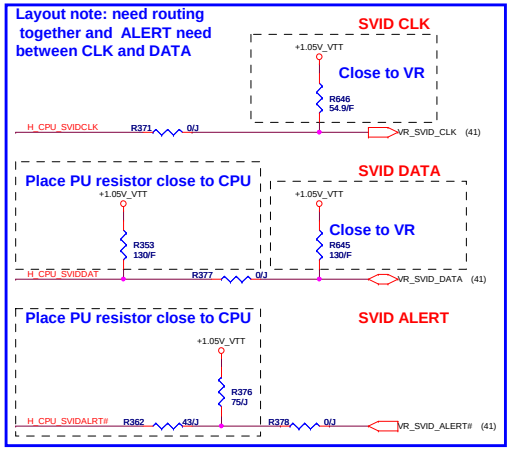
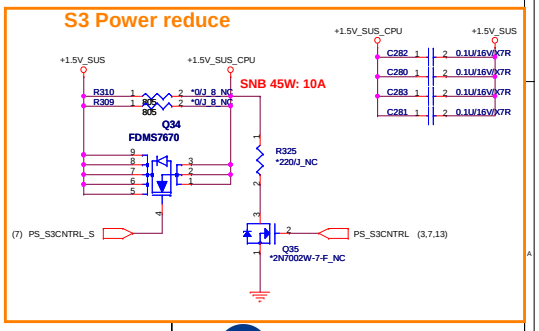
# Sandy Bridge Processor (POWER)




# Sandy Bridge Processor (GRAPHIC POWER)



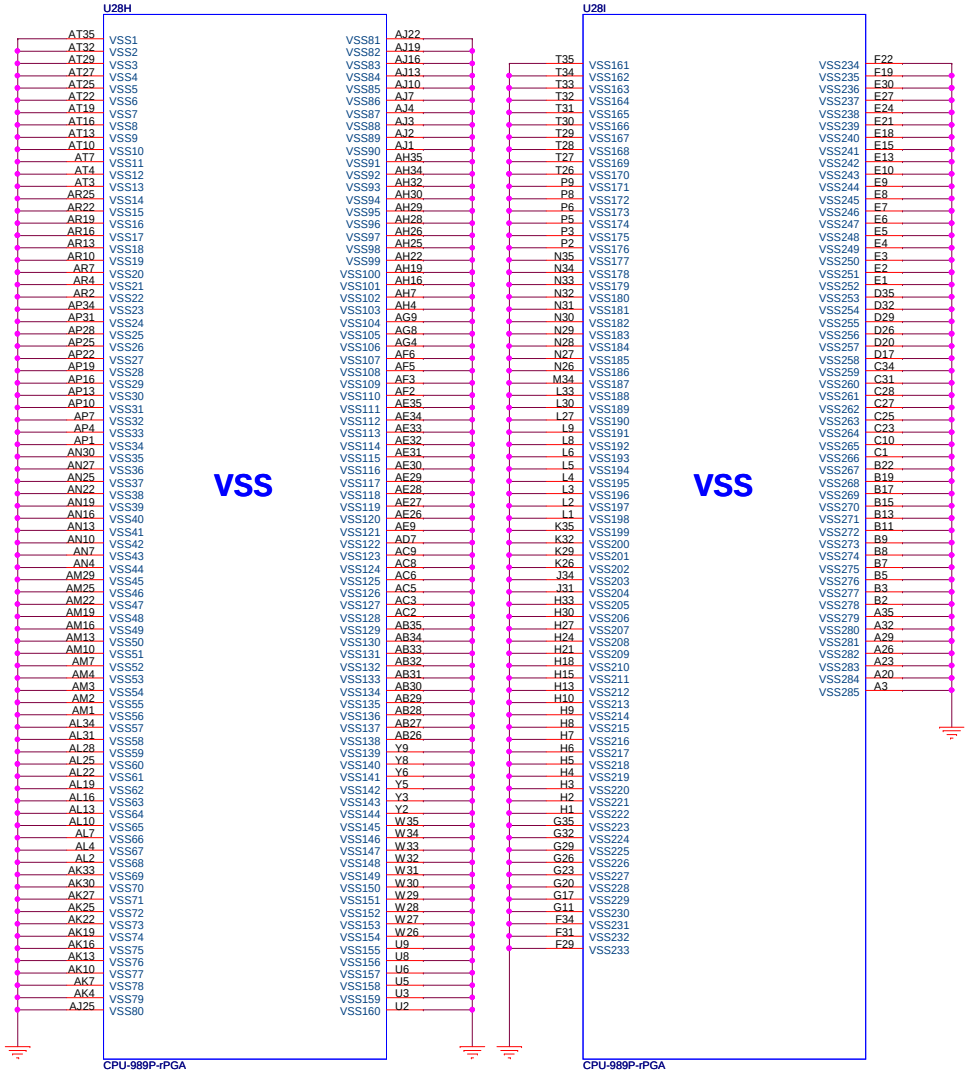



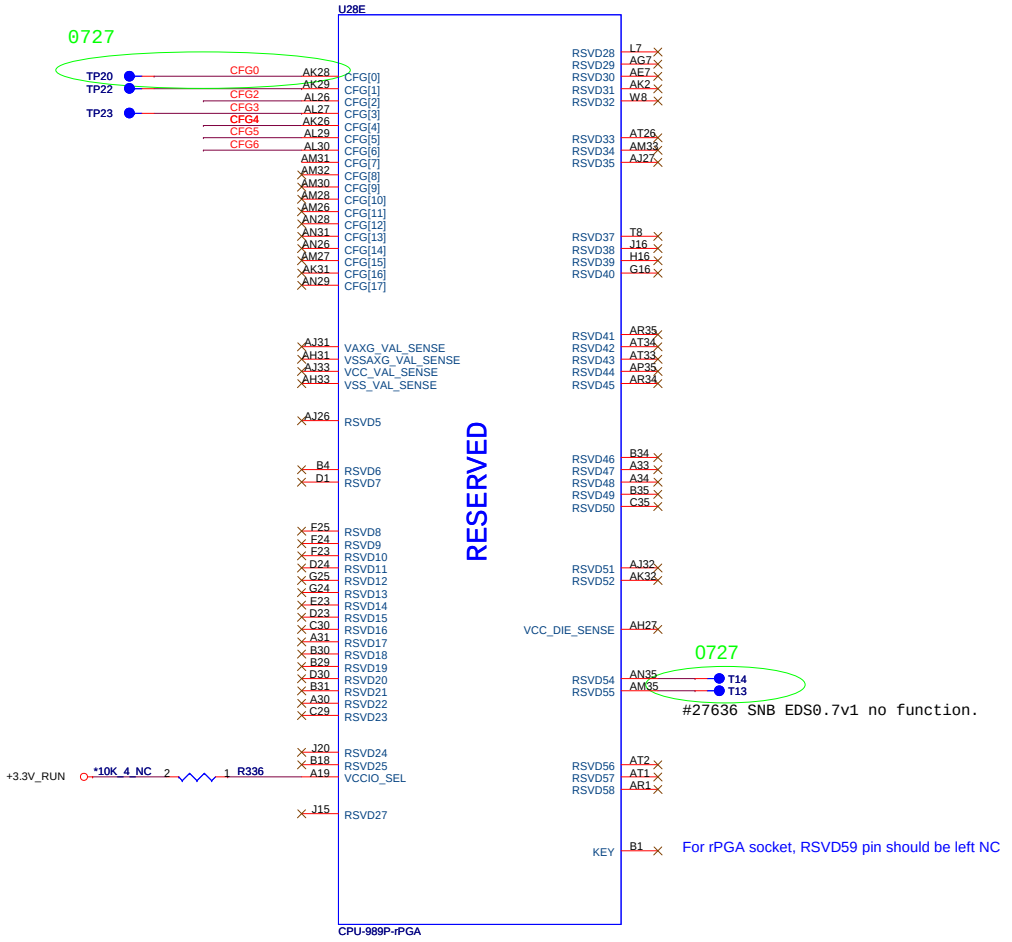

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | Sandy Bridge 3/4 | 1A |
| Date: Friday, August 27, 2010 | Sheet 5 of 57 | |

# Sandy Bridge Processor (GND)



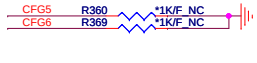

# Sandy Bridge Processor (RESERVED, CFG)




## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

| | 1 | 0 |
|---|---|---|
| CFG2<br>(PEG Static Lane Reversal) | Normal Operation | Lane Number Reversed |
| CFG3<br>(PCI-E Static x4 Lane Reversal) | PCI-E Static x4 Lane Reversal | PEG wait for BIOS training |
| CFG4<br>(DP Presence Strap) | Disable; No physical DP attached to eDP | Enable; An ext DP device is connected to eDP |


CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Quanta Computer Inc.
PROJECT :GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | Sandy Bridge 4/4 | 1A |

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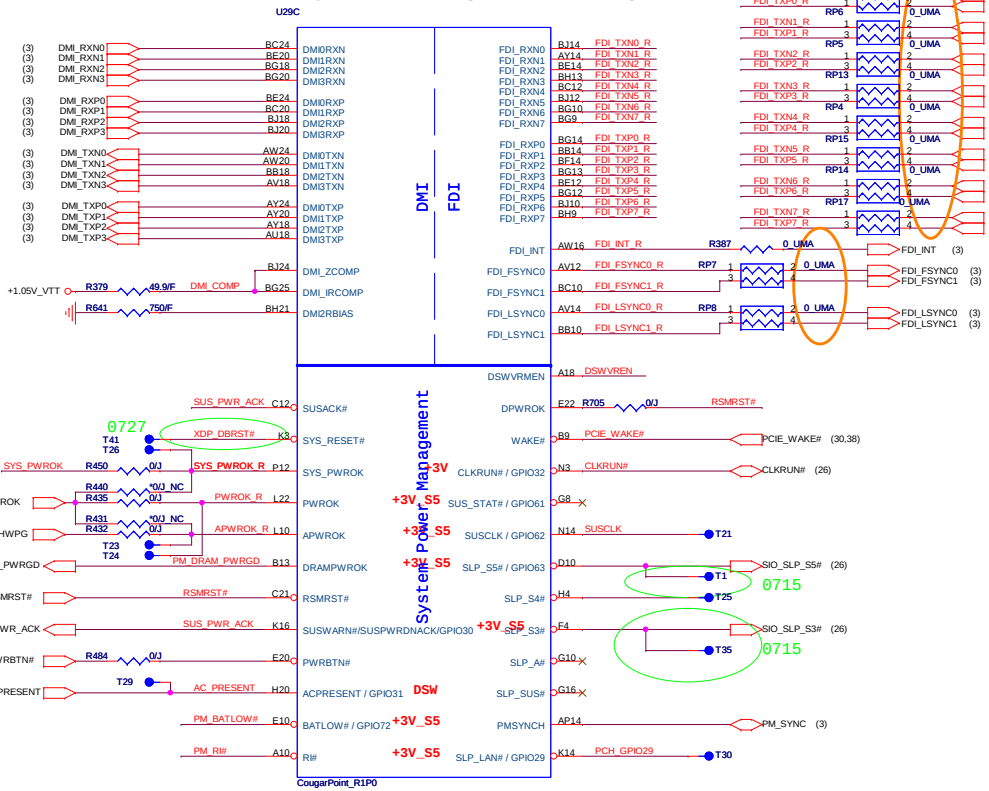
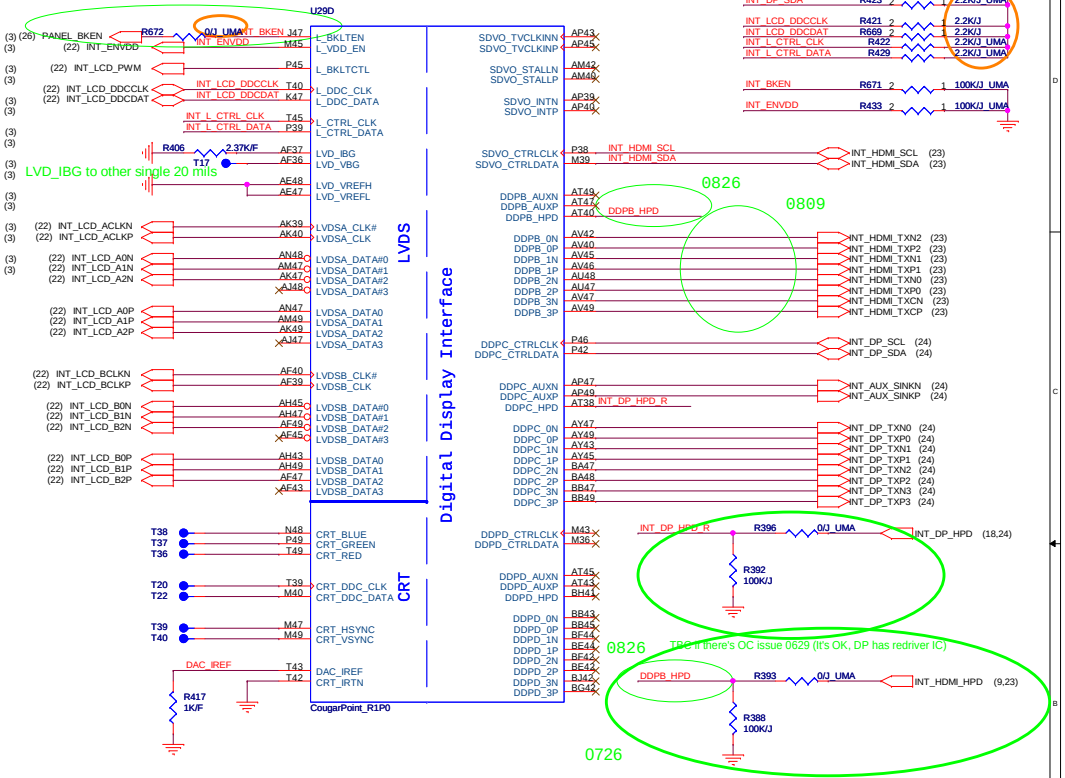
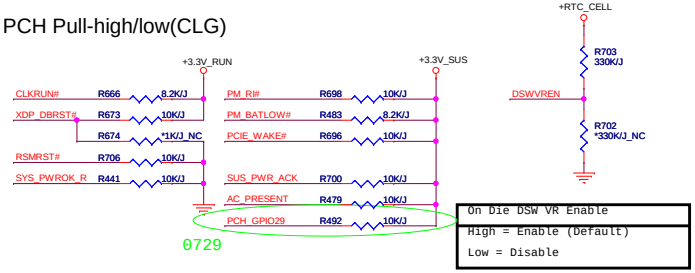
# Cougar Point (DMI,FDI,PM)



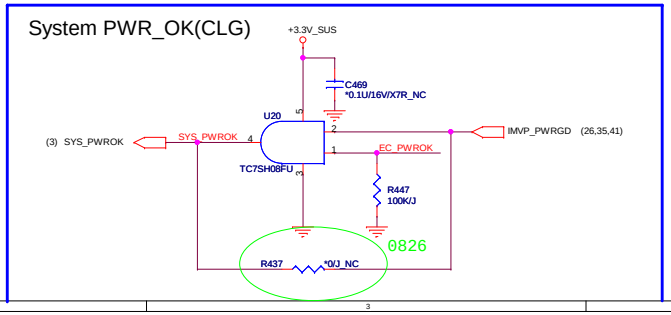

# Cougar Point (LVDS,DDI)



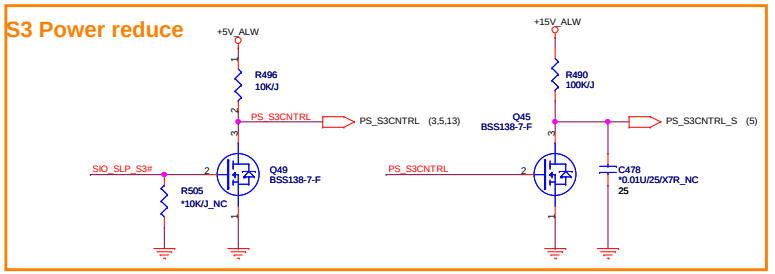

## PCH Pull-high/low(CLG)




## System PWR_OK(CLG)




## S3 Power reduce




Quanta Computer Inc.

PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | Cougar Point 1/6 | 1A |
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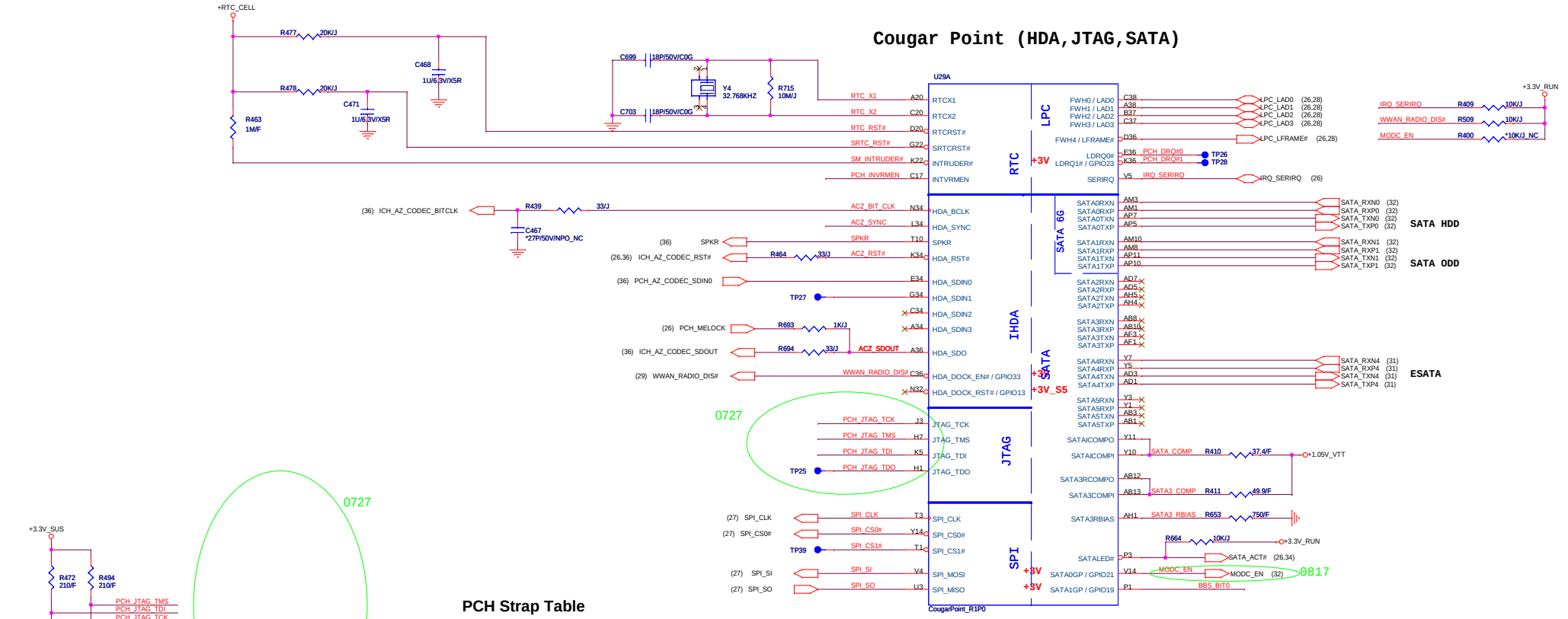
# Cougar Point (HDA,JTAG,SATA)




## PCH Strap Table

| Pin Name | Strap description | Sampled | Configuration | |
|---|---|---|---|---|
| **SPKR** | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode | +3.3V_RUN R408 *1K/J_NC SPKR |
| **GNT3# / GPIO55** | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K) | R454 *1K/J_NC PCI_GNT3# (9) |
| **GNT1# / GPIO51** | Boot BIOS Selection 1 [bit-1] | PWROK | GNT1# / GNT0# / Boot Location:<br>1 / 1 / SPI *<br>0 / 0 / LPC | **Default weak pull-up on GNT0/1#**<br>**[Need external pull-down for LPC BIOS]**<br>R688 *1K/J_NC BBS_BIT1 (9)<br>R665 *1K/J_NC BBS_BIT0 |
| **GPIO19** | Boot BIOS Selection 0 [bit-0] | PWROK | | |
| **HDA_SYNC** | On-Die PLL VR Volatge Select | RSMRST | 0 = Support by 1.8V (weak PD)<br>1 = Support by 1.5V | +3.3V_SUS 0729 R469 0/J Q44 *2N7002W-7-F_NC R461 1K/J 33/J R470 (36) ICH_AZ_CODEC_SYNC ACZ_SYNC +5V_RUN |
| **HDA_SDO** | Flash Descriptor Security | PWROK | 0 = Default (weak pull-down 20K)<br>1 = Override | +3.3V_SUS R692 *1K/J_NC ACZ_SDOUT |
| **GPIO28** | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable<br>1 = Enable (Default) | 0729 +3.3V_SUS R418 *1K/J_NC R424 10K/J PLL_ODVR_EN (10) |
| **INTVRMEN** | Integrated 1.05V VRM enable | ALWAYS | **Should be always pull-up** | +RTC_CELL R704 330K/J PCH_INVRMEN |
| **DF_TVS** | DMI and FDI Tx/Rx Termination Voltage | PWROK | weak pull-down 20kohm<br>**0 = Set to Vss**<br>**1 = Set to Vcc (weak pull-down 20K)** | +1.8V_RUN 0727 R382 2.2K/J DF_TVS (10) |

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | Cougar Point 2/6 | 1A |

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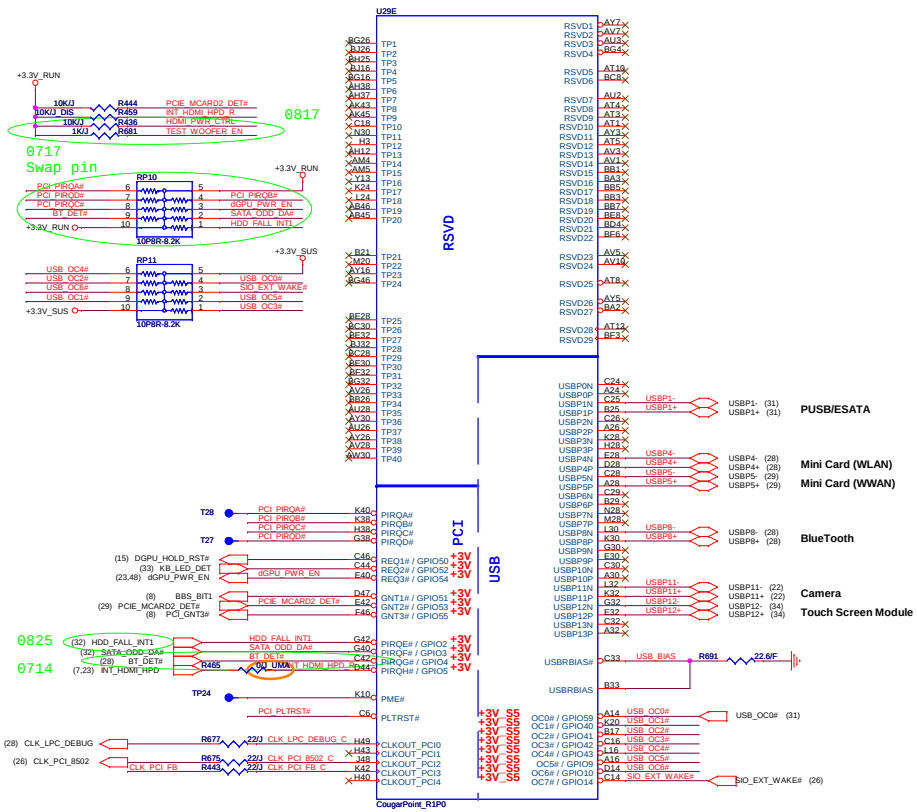
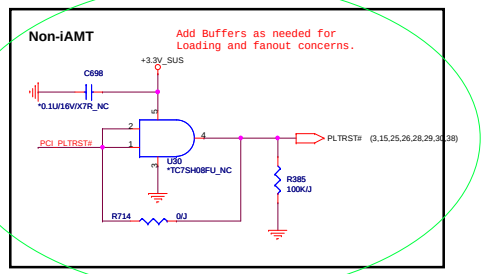
# Cougar Point-M (PCI,USB,NVRAM)

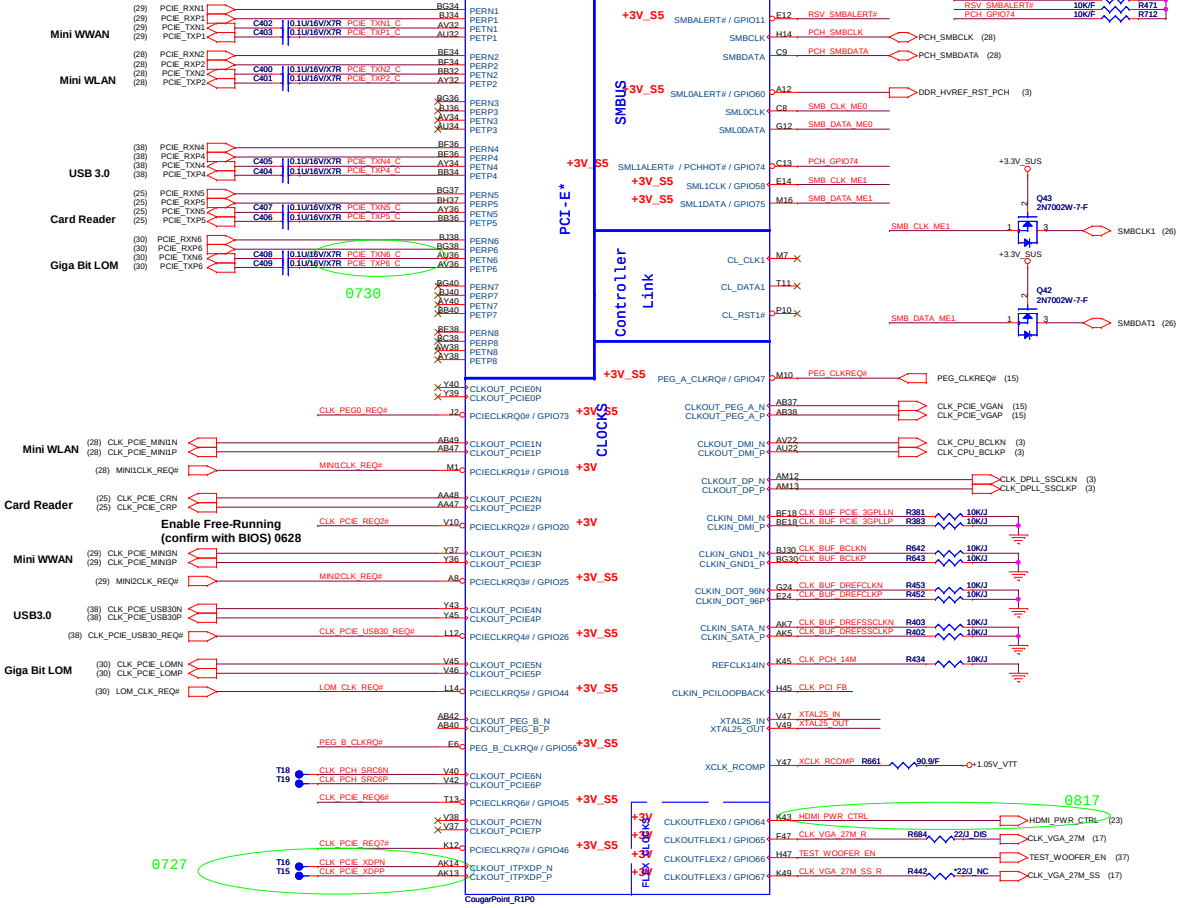


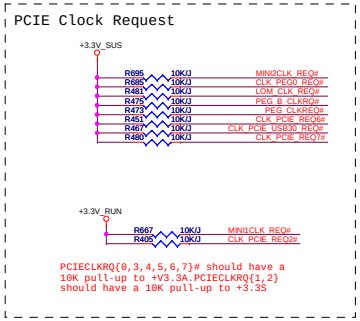



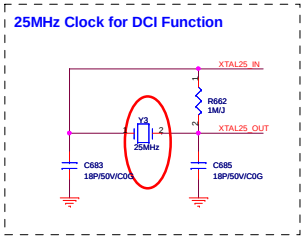

change to R01 schematic

# Cougar Point-M (PCI-E,SMBUS,CLK)

Note:Place TX DC blocking caps close to PCH.




Change as big package (UM9)

| Quanta Computer Inc. | | |
|---|---|---|
| PROJECT : GM6C MLK DIS | | |
| Size | Document Number: Cougar Point 3/6 | Rev: 1A |
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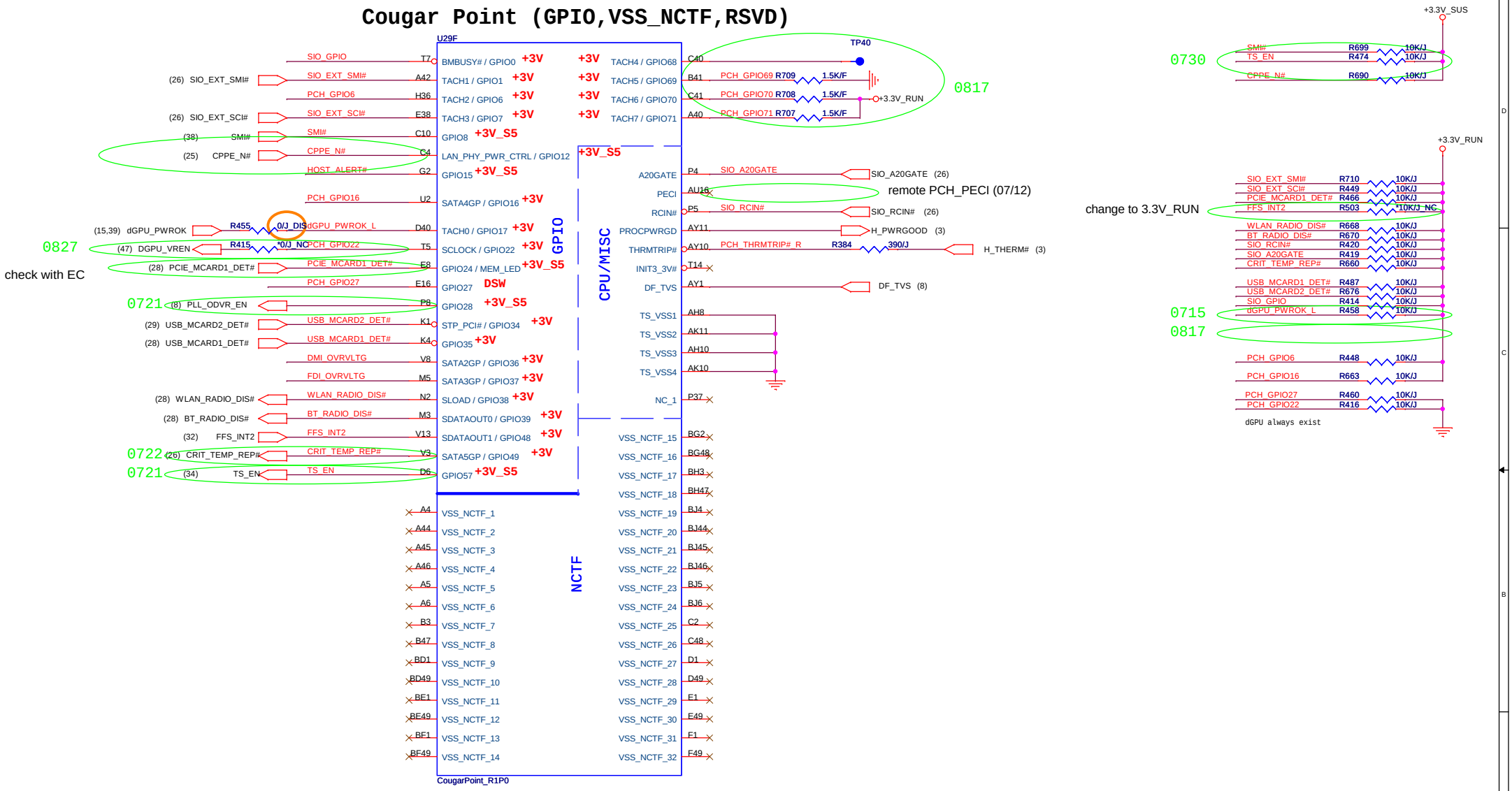
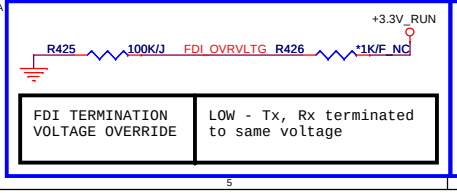
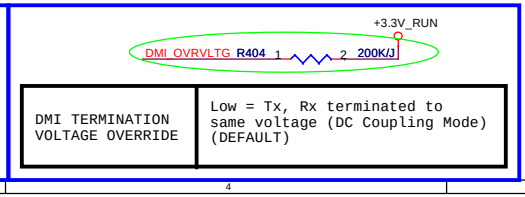
# Cougar Point (GPIO,VSS_NCTF,RSVD)



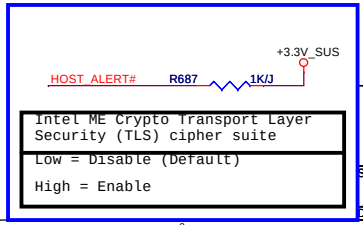




| | |
|---|---|
| FDI TERMINATION VOLTAGE OVERRIDE | LOW - Tx, Rx terminated to same voltage |




| | |
|---|---|
| DMI TERMINATION VOLTAGE OVERRIDE | Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT) |

internal PD resistor 20K-ohm
To avoid voltage be divided,
please change GPIO36 PU resistor from
10K-ohm to 200K-ohm. (07/12)

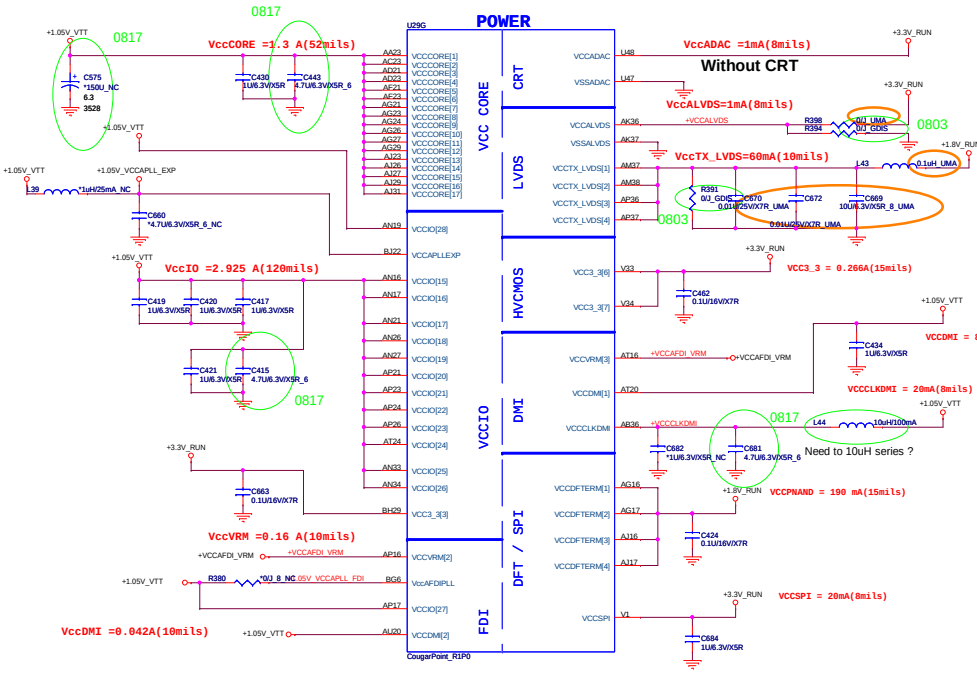



| |
|---|
| Intel ME Crypto Transport Layer Security (TLS) cipher suite |
| Low = Disable (Default) |
| High = Enable |

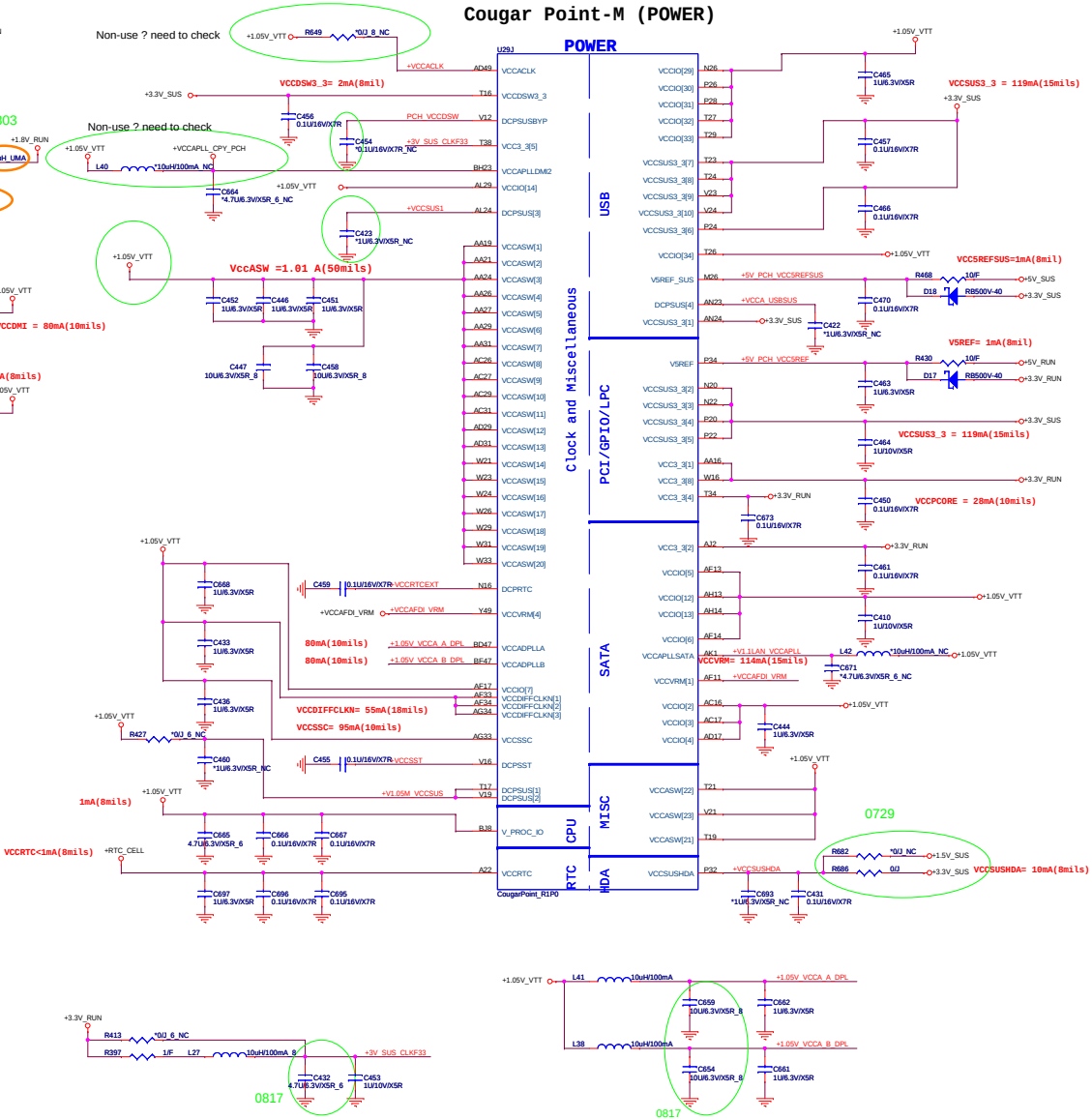
Quanta Computer Inc.
PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | Cougar Point 4/6 | 1A |
| Date: Friday, August 27, 2010 | Sheet 10 of 57 | |

# COUGAR POINT (POWER)




# Cougar Point-M (POWER)



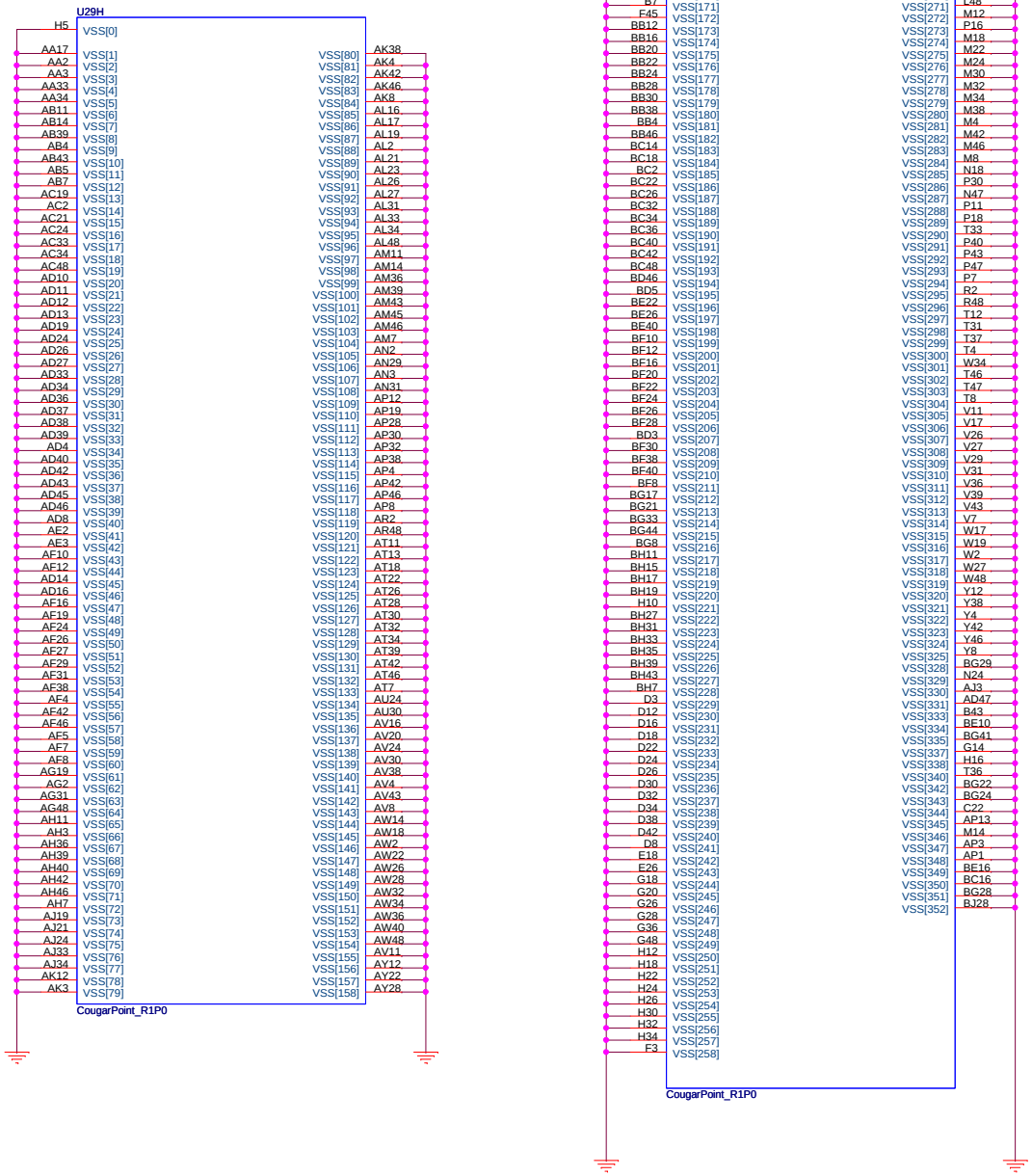





| | | | |
|---|---|---|---|
| Quanta Computer Inc. | | | |
| PROJECT : GM6C MLK DIS | | | |
| Size | Document Number | | Rev |
| | Cougar Point 5/6 | | 1A |
| Date: Friday, August 27, 2010 | | Sheet 11 of 57 | |

# PCH6(CLG)

## IBEX PEAK-M (GND)







Quanta Computer Inc.

PROJECT :GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | Cougar Point 6/6 | 1A |
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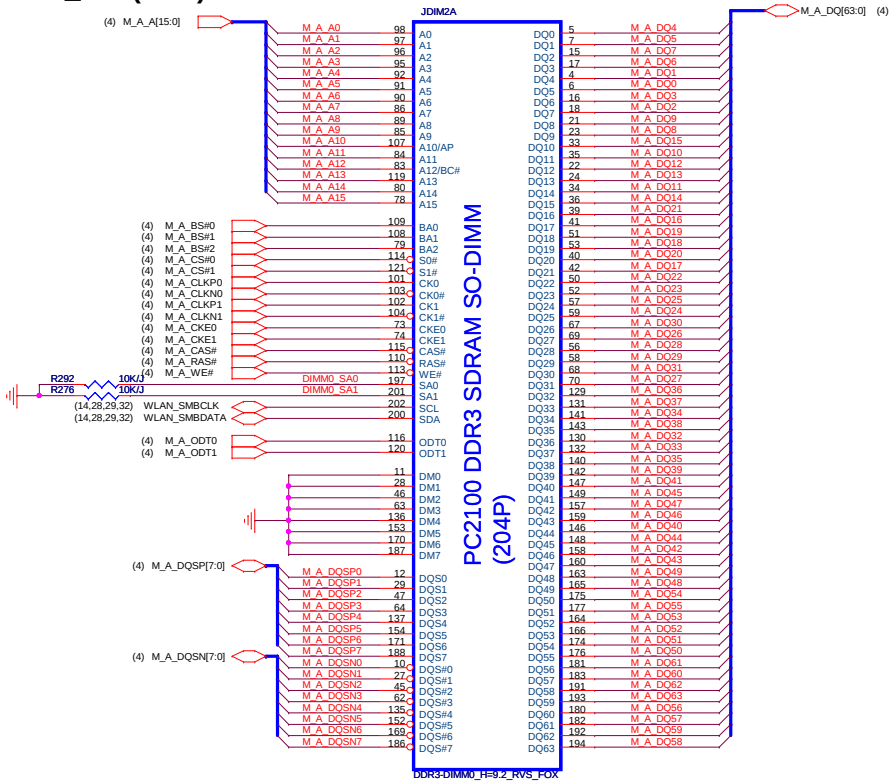
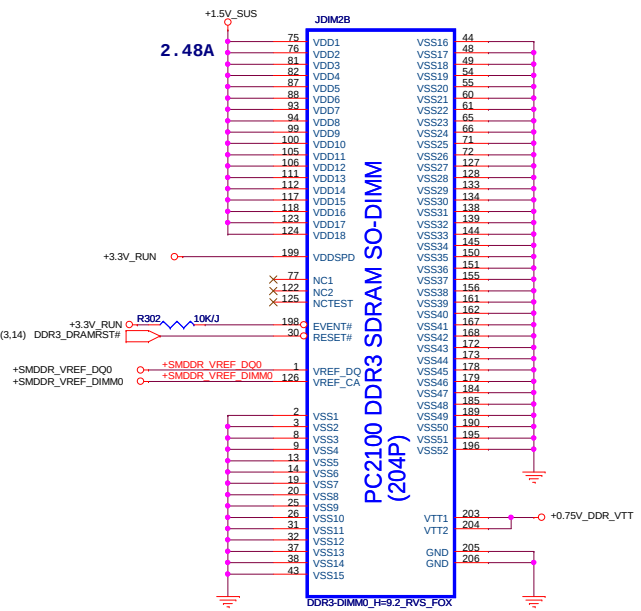
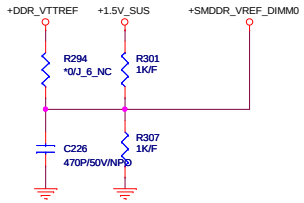
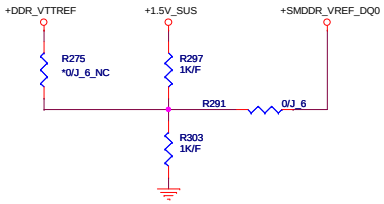
# DDR_STD(DDR)



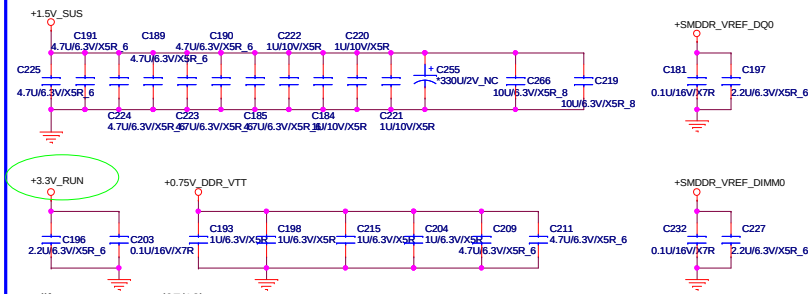




## M1 VREF Solution

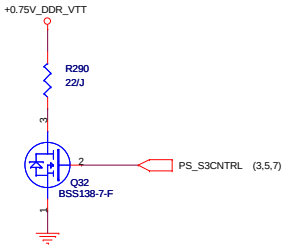



## Place these Caps near So-Dimm0.




modify wrong net name(07/12)

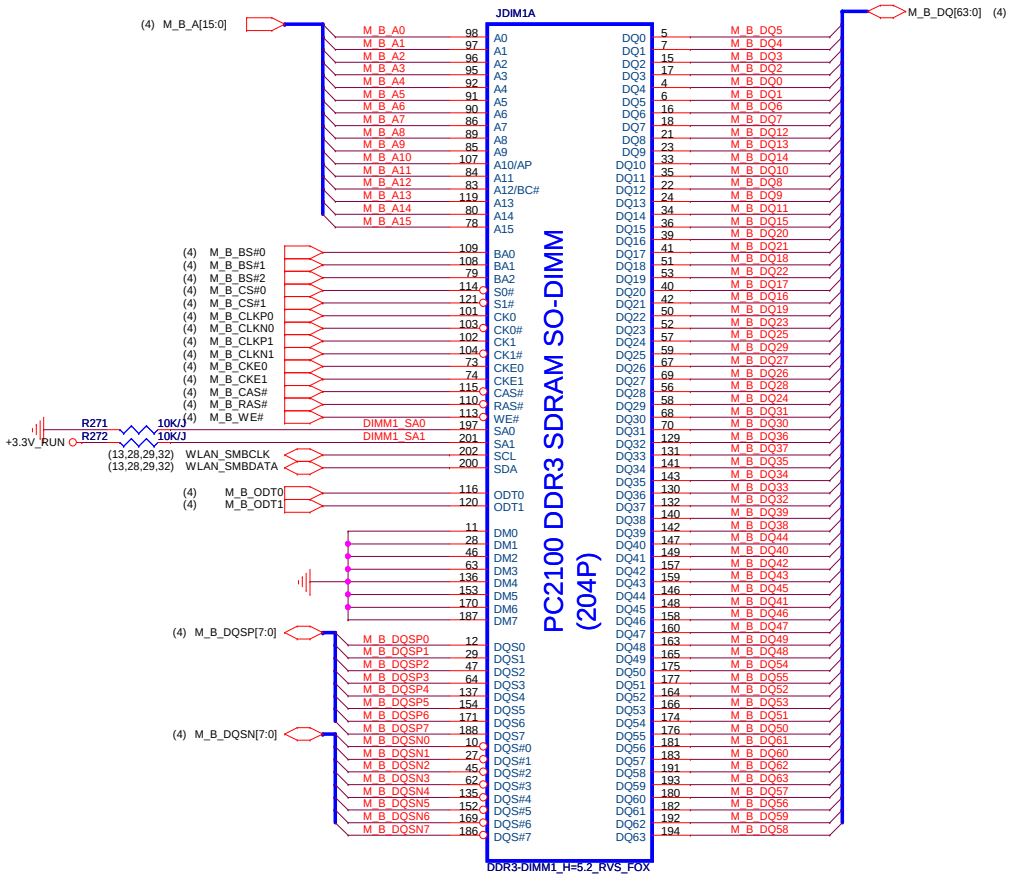
## S3 Power reduce

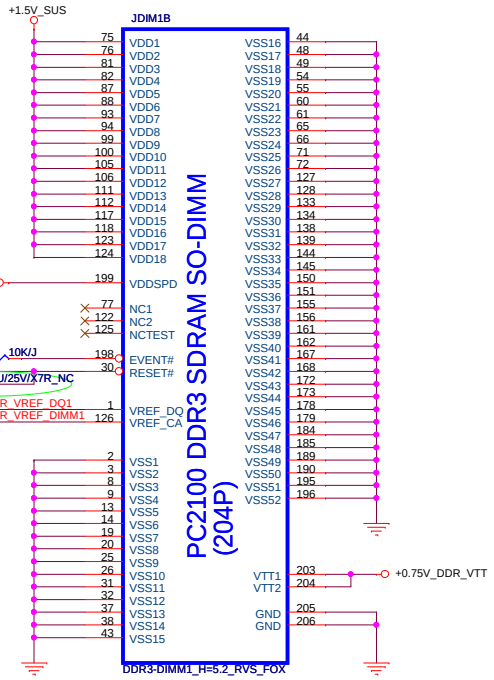


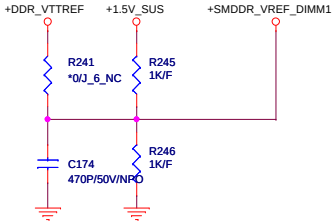

Quanta Computer Inc.

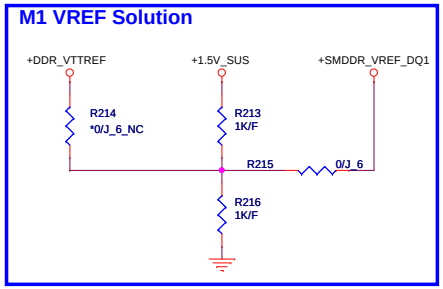
PROJECT : GM6C MLK DIS

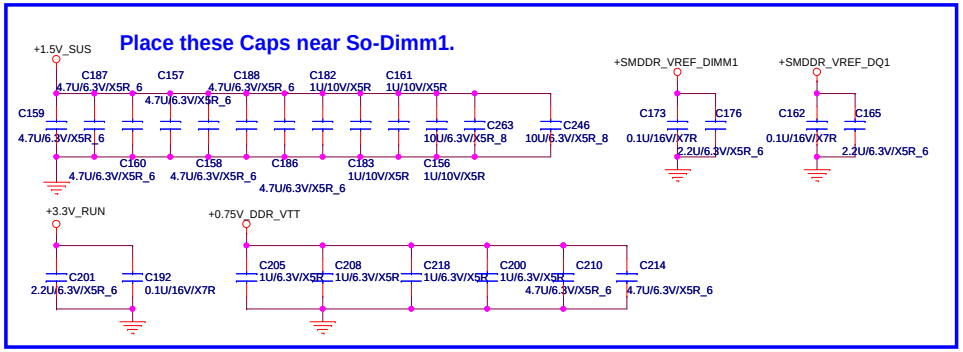
| Size | Document Number | Rev |
|---|---|---|
| | DDRIII SO-DIMM-0 | 1A |
| Date: Friday, August 27, 2010 | Sheet 13 of 57 | |




Quanta Computer Inc.

PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | DDRIII SO-DIMM-1 | 1A |
| Date: Friday, August 27, 2010 | Sheet 14 of 57 | |

# power up sequence

VDD33 (+3.3V_GFX)

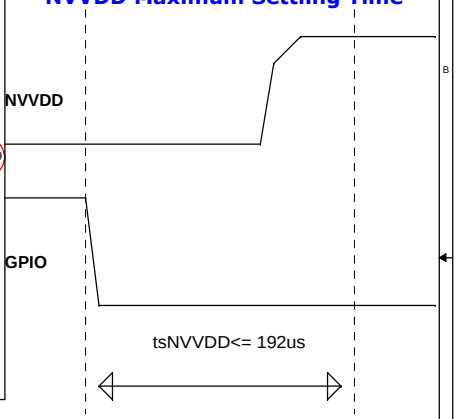
PXE_VDD (+1.05V_GFX)

NVVDD (+VCC_GFX_CORE)

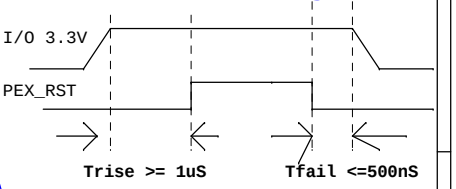
IFPAB_IOVDD (+1.8V_GFX)

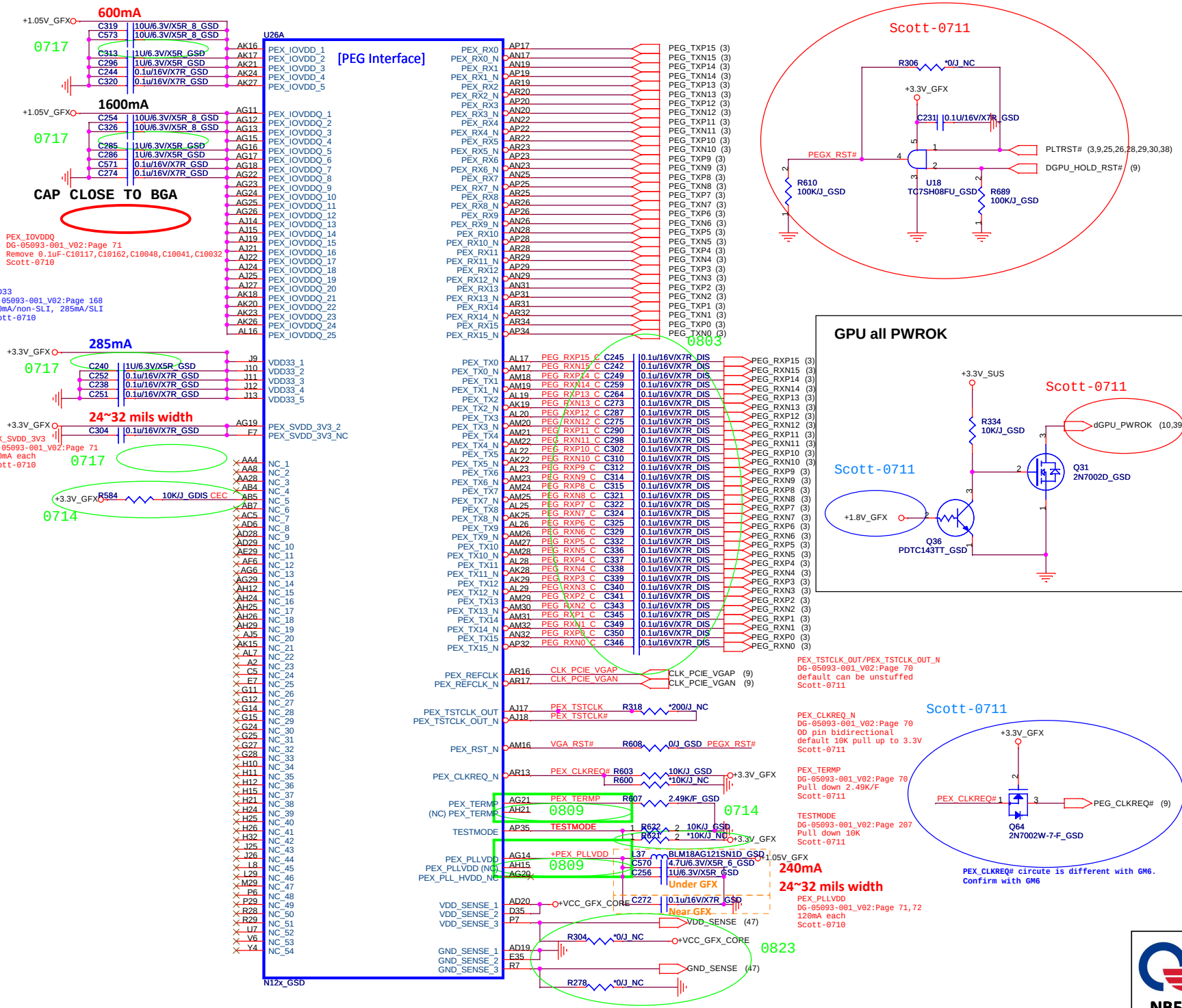
FBVDDQ (+1.5V_GFX)

## NVVDD Maximum Settling Time




## PEX_RST timing





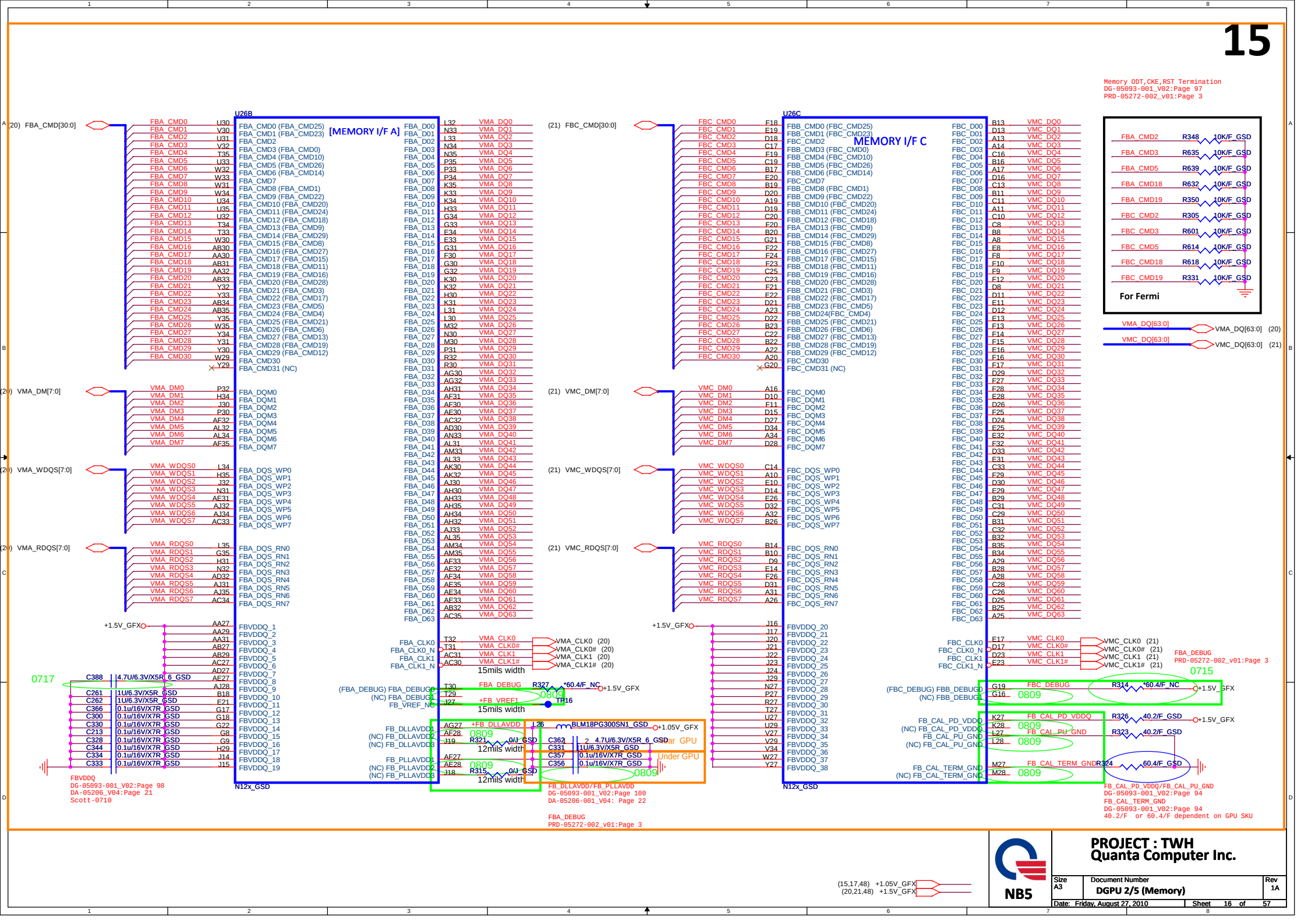


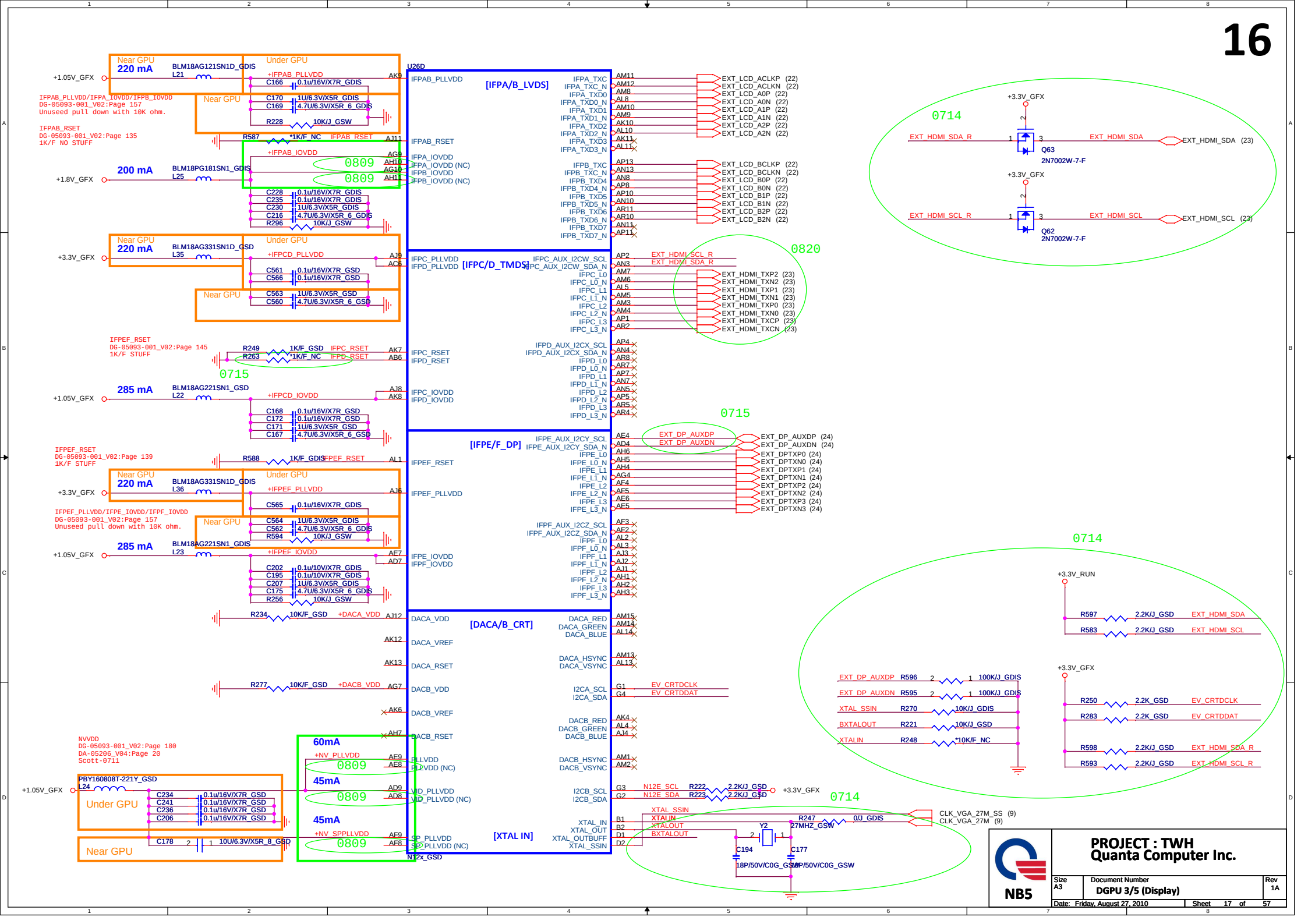


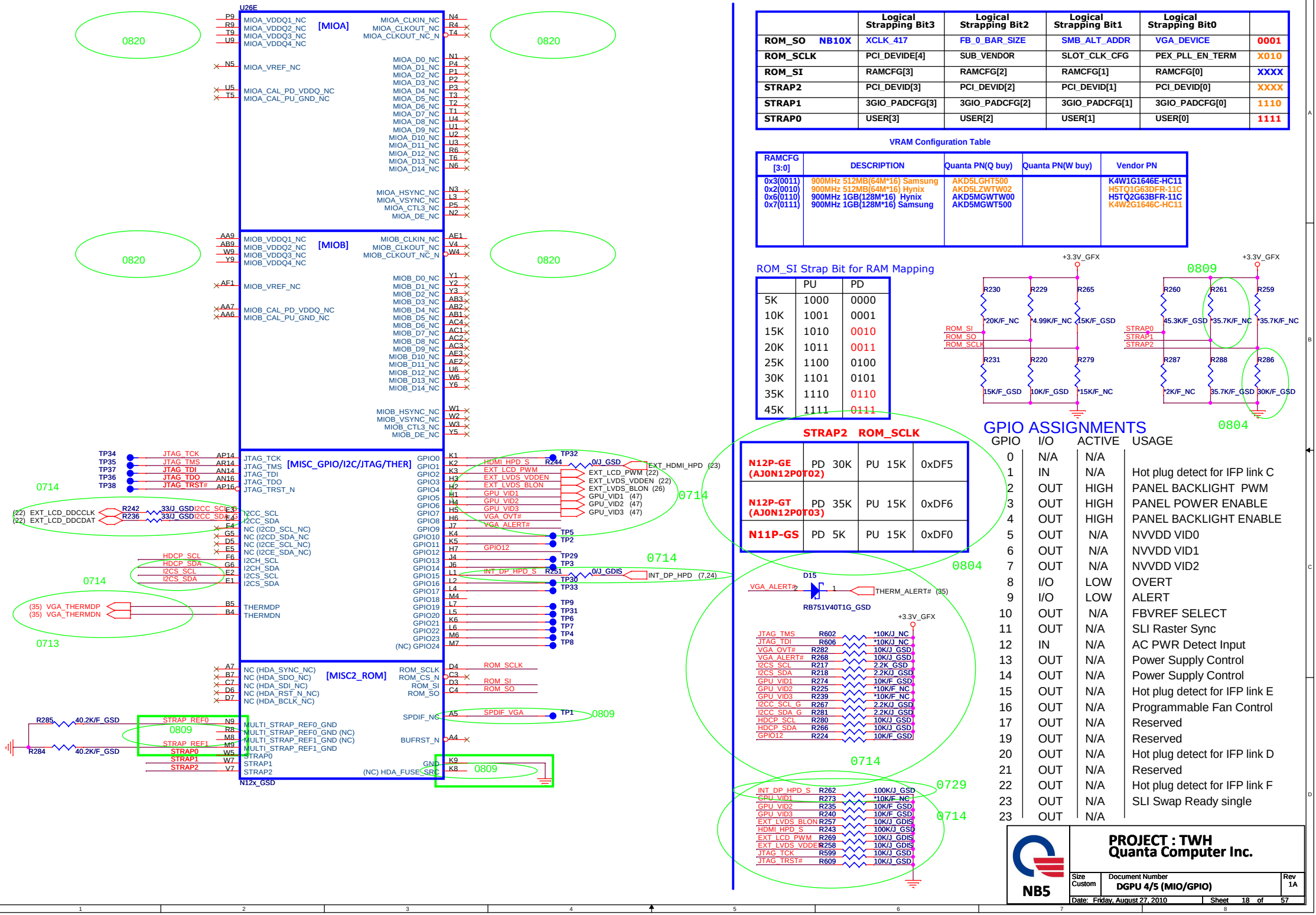




| | | |
|---|---|---|
| NB5 | PROJECT : TWH<br>Quanta Computer Inc. | |
| | Size A3 / Document Number: DGPU 1/5 (PEG) | Rev 1A |
| | Date: Friday, August 27, 2010 | Sheet 15 of 57 |


Memory ODT,CKE,RST Termination
DG-05093-001_V02:Page 97
PRD-05272-002_v01:Page 3
U26B
[MEMORY I/F A]
U26C
MEMORY I/F C
For Fermi
FBVDDQ
DG-05093-001_V02:Page 98
DA-05206_V04:Page 21
Scott-0710
FB_DLLAVDD/FB_PLLAVDD
DG-05093-001_V02:Page 100
DA-05206-001_V04: Page 22
FBA_DEBUG
PRD-05272-002_v01:Page 3
FBA_DEBUG
PRD-05272-002_v01:Page 3
FB_CAL_PD_VDDQ/FB_CAL_PU_GND
DG-05093-001_V02:Page 94
FB_CAL_TERM_GND
DG-05093-001_V02:Page 94
40.2/F or 60.4/F dependent on GPU SKU
N12x_GSD
N12x_GSD
Under GPU
Under GPU
15mils width
15mils width
12mils width
12mils width
0717
0715
0809


U26D
[IFPA/B_LVDS]
[IFPC/D_TMDS]
[IFPE/F_DP]
[DACA/B_CRT]
[XTAL IN]
Near GPU
Under GPU
220 mA
200 mA
285 mA
60mA
45mA
0809
0820
0714
0715
+1.05V_GFX
+1.8V_GFX
+3.3V_GFX
+3.3V_RUN
EXT_HDMI_SDA_R
EXT_HDMI_SCL_R
EXT_HDMI_SDA
EXT_HDMI_SCL
Q63
2N7002W-7-F
Q62
2N7002W-7-F
EXT_DP_AUXDP
EXT_DP_AUXDN
EXT_DPTXP0
EXT_DPTXN0
EXT_DPTXP1
EXT_DPTXN1
EXT_DPTXP2
EXT_DPTXN2
EXT_DPTXP3
EXT_DPTXN3
EXT_HDMI_TXP2
EXT_HDMI_TXN2
EXT_HDMI_TXP1
EXT_HDMI_TXN1
EXT_HDMI_TXP0
EXT_HDMI_TXN0
EXT_HDMI_TXCP
EXT_HDMI_TXCN
EXT_LCD_ACLKP
EXT_LCD_ACLKN
EXT_LCD_A0P
EXT_LCD_A0N
EXT_LCD_A1P
EXT_LCD_A1N
EXT_LCD_A2P
EXT_LCD_A2N
EXT_LCD_BCLKP
EXT_LCD_BCLKN
EXT_LCD_B0P
EXT_LCD_B0N
EXT_LCD_B1P
EXT_LCD_B1N
EXT_LCD_B2P
EXT_LCD_B2N
CLK_VGA_27M_SS
CLK_VGA_27M
EV_CRTDCLK
EV_CRTDDAT
XTAL_SSIN
XTALIN
XTALOUT
BXTALOUT
27MHZ_GSW
IFPAB_PLLVDD/IFPA_IOVDD/IFPB_IOVDD
DG-05093-001_V02:Page 157
Unuseed pull down with 10K ohm.
IFPAB_RSET
DG-05093-001_V02:Page 135
1K/F NO STUFF
IFPEF_RSET
DG-05093-001_V02:Page 145
1K/F STUFF
IFPEF_RSET
DG-05093-001_V02:Page 139
1K/F STUFF
IFPEF_PLLVDD/IFPE_IOVDD/IFPF_IOVDD
DG-05093-001_V02:Page 157
Unuseed pull down with 10K ohm.
NVVDD
DG-05093-001_V02:Page 180
DA-05206_V04:Page 20
Scott-0711
PROJECT : TWH
Quanta Computer Inc.
NB5
Size A3
Document Number
DGPU 3/5 (Display)
Rev 1A
Date: Friday, August 27, 2010
Sheet 17 of 57




| | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 | |
|---|---|---|---|---|---|
| ROM_SO NB10X | XCLK_417 | FB_0_BAR_SIZE | SMB_ALT_ADDR | VGA_DEVICE | 0001 |
| ROM_SCLK | PCI_DEVIDE[4] | SUB_VENDOR | SLOT_CLK_CFG | PEX_PLL_EN_TERM | X010 |
| ROM_SI | RAMCFG[3] | RAMCFG[2] | RAMCFG[1] | RAMCFG[0] | XXXX |
| STRAP2 | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] | PCI_DEVID[0] | XXXX |
| STRAP1 | 3GIO_PADCFG[3] | 3GIO_PADCFG[2] | 3GIO_PADCFG[1] | 3GIO_PADCFG[0] | 1110 |
| STRAP0 | USER[3] | USER[2] | USER[1] | USER[0] | 1111 |

VRAM Configuration Table

| RAMCFG [3:0] | DESCRIPTION | Quanta PN(Q buy) | Quanta PN(W buy) | Vendor PN |
|---|---|---|---|---|
| 0x3(0011) | 900MHz 512MB(64M*16) Samsung | AKD5LGHT500 | | K4W1G1646E-HC11 |
| 0x2(0010) | 900MHz 512MB(64M*16) Hynix | AKD5LZWTW02 | | H5TQ1G63DFR-11C |
| 0x6(0110) | 900MHz 1GB(128M*16) Hynix | AKD5MGWTW00 | | H5TQ2G63BFR-11C |
| 0x7(0111) | 900MHz 1GB(128M*16) Samsung | AKD5MGWT500 | | K4W2G1646C-HC11 |

ROM_SI Strap Bit for RAM Mapping

| | PU | PD |
|---|---|---|
| 5K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 25K | 1100 | 0100 |
| 30K | 1101 | 0101 |
| 35K | 1110 | 0110 |
| 45K | 1111 | 0111 |




STRAP2 ROM_SCLK

| | | | |
|---|---|---|---|
| N12P-GE (AJ0N12P0T02) | PD 30K | PU 15K | 0xDF5 |
| N12P-GT (AJ0N12P0T03) | PD 35K | PU 15K | 0xDF6 |
| N11P-GS | PD 5K | PU 15K | 0xDF0 |




## GPIO ASSIGNMENTS

| GPIO | I/O | ACTIVE | USAGE |
|---|---|---|---|
| 0 | N/A | N/A | |
| 1 | IN | N/A | Hot plug detect for IFP link C |
| 2 | OUT | HIGH | PANEL BACKLIGHT PWM |
| 3 | OUT | HIGH | PANEL POWER ENABLE |
| 4 | OUT | HIGH | PANEL BACKLIGHT ENABLE |
| 5 | OUT | N/A | NVVDD VID0 |
| 6 | OUT | N/A | NVVDD VID1 |
| 7 | OUT | N/A | NVVDD VID2 |
| 8 | I/O | LOW | OVERT |
| 9 | I/O | LOW | ALERT |
| 10 | OUT | N/A | FBVREF SELECT |
| 11 | OUT | N/A | SLI Raster Sync |
| 12 | IN | N/A | AC PWR Detect Input |
| 13 | OUT | N/A | Power Supply Control |
| 14 | OUT | N/A | Power Supply Control |
| 15 | OUT | N/A | Hot plug detect for IFP link E |
| 16 | OUT | N/A | Programmable Fan Control |
| 17 | OUT | N/A | Reserved |
| 19 | OUT | N/A | Reserved |
| 20 | OUT | N/A | Hot plug detect for IFP link D |
| 21 | OUT | N/A | Reserved |
| 22 | OUT | N/A | Hot plug detect for IFP link F |
| 23 | OUT | N/A | SLI Swap Ready single |
| 23 | OUT | N/A | |

NB5

PROJECT : TWH
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | DGPU 4/5 (MIO/GPIO) | 1A |
| Date: Friday, August 27, 2010 | Sheet 18 of 57 | |

31.56A

0802

+VCC_GFX_CORE

U26F

[GPU VDD]

| | | | |
|---|---|---|---|
| AB11 | VDD_001 | VDD_057 | P21 |
| AB13 | VDD_002 | VDD_058 | P23 |
| AB15 | VDD_003 | VDD_059 | P25 |
| AB17 | VDD_004 | VDD_060 | R11 |
| AB19 | VDD_005 | VDD_061 | R12 |
| AB21 | VDD_006 | VDD_062 | R13 |
| AB23 | VDD_007 | VDD_063 | R14 |
| AB25 | VDD_008 | VDD_064 | R15 |
| AC11 | VDD_009 | VDD_065 | R16 |
| AC12 | VDD_010 | VDD_066 | R17 |
| AC13 | VDD_011 | VDD_067 | R18 |
| AC14 | VDD_012 | VDD_068 | R19 |
| AC15 | VDD_013 | VDD_069 | R20 |
| AC16 | VDD_014 | VDD_070 | R21 |
| AC17 | VDD_015 | VDD_071 | R22 |
| AC18 | VDD_016 | VDD_072 | R23 |
| AC19 | VDD_017 | VDD_073 | R24 |
| AC20 | VDD_018 | VDD_074 | R25 |
| AC21 | VDD_019 | VDD_075 | T12 |
| AC22 | VDD_020 | VDD_076 | T14 |
| AC23 | VDD_021 | VDD_077 | T16 |
| AC24 | VDD_022 | VDD_078 | T18 |
| AC25 | VDD_023 | VDD_079 | T20 |
| AD12 | VDD_024 | VDD_080 | T22 |
| AD14 | VDD_025 | VDD_081 | T24 |
| AD16 | VDD_026 | VDD_082 | V11 |
| AD18 | VDD_027 | VDD_083 | V13 |
| AD22 | VDD_028 | VDD_084 | V15 |
| AD24 | VDD_029 | VDD_085 | V17 |
| L11 | VDD_030 | VDD_086 | V19 |
| L12 | VDD_031 | VDD_087 | V21 |
| L13 | VDD_032 | VDD_088 | V23 |
| L14 | VDD_033 | VDD_089 | V25 |
| L15 | VDD_034 | VDD_090 | W11 |
| L16 | VDD_035 | VDD_091 | W12 |
| L17 | VDD_036 | VDD_092 | W13 |
| L18 | VDD_037 | VDD_093 | W14 |
| L19 | VDD_038 | VDD_094 | W15 |
| L20 | VDD_039 | VDD_095 | W16 |
| L21 | VDD_040 | VDD_096 | W17 |
| L22 | VDD_041 | VDD_097 | W18 |
| L23 | VDD_042 | VDD_098 | W19 |
| L24 | VDD_043 | VDD_099 | W20 |
| L25 | VDD_044 | VDD_100 | W21 |
| M12 | VDD_045 | VDD_101 | W22 |
| M14 | VDD_046 | VDD_102 | W23 |
| M16 | VDD_047 | VDD_103 | W24 |
| M18 | VDD_048 | VDD_104 | W25 |
| M20 | VDD_049 | VDD_105 | Y12 |
| M22 | VDD_050 | VDD_106 | Y14 |
| M24 | VDD_051 | VDD_107 | Y16 |
| P11 | VDD_052 | VDD_108 | Y18 |
| P13 | VDD_053 | VDD_109 | Y20 |
| P15 | VDD_054 | VDD_110 | Y22 |
| P17 | VDD_055 | VDD_111 | Y24 |
| P19 | VDD_056 | | |

N12x_GSD

+VCC_GFX_CORE

U26G

[GPU GND]

| | | | |
|---|---|---|---|
| AA2 | GND_1 | GND_97 | E9 |
| AA5 | GND_2 | GND_98 | E12 |
| AA11 | GND_3 | GND_99 | E15 |
| AA12 | GND_4 | GND_100 | E18 |
| AA13 | GND_5 | GND_101 | E24 |
| AA14 | GND_6 | GND_102 | E27 |
| AA15 | GND_7 | GND_103 | E30 |
| AA16 | GND_8 | GND_104 | F2 |
| AA17 | GND_9 | GND_105 | F5 |
| AA18 | GND_10 | GND_106 | F31 |
| AA19 | GND_11 | GND_107 | F34 |
| AA20 | GND_12 | GND_108 | J2 |
| AA21 | GND_13 | GND_109 | J5 |
| AA22 | GND_14 | GND_110 | J31 |
| AA23 | GND_15 | GND_111 | J34 |
| AA24 | GND_16 | GND_112 | L9 |
| AA25 | GND_17 | GND_113 | M2 |
| AA34 | GND_18 | GND_114 | M5 |
| AB12 | GND_19 | GND_115 | M11 |
| AB14 | GND_20 | GND_116 | M13 |
| AB16 | GND_21 | GND_117 | M15 |
| AB18 | GND_22 | GND_118 | M17 |
| AB20 | GND_23 | GND_119 | M19 |
| AB22 | GND_24 | GND_120 | M21 |
| AB24 | GND_25 | GND_121 | M23 |
| AC9 | GND_26 | GND_122 | M25 |
| AD11 | GND_27 | GND_123 | M31 |
| AD13 | GND_28 | GND_124 | M34 |
| AD15 | GND_29 | GND_125 | N11 |
| AD17 | GND_30 | GND_126 | N12 |
| AD2 | GND_31 | GND_127 | N13 |
| AD5 | GND_32 | GND_128 | N14 |
| AD21 | GND_33 | GND_129 | N15 |
| AD23 | GND_34 | GND_130 | N16 |
| AD25 | GND_35 | GND_131 | N17 |
| AD31 | GND_36 | GND_132 | N18 |
| AD34 | GND_37 | GND_133 | N19 |
| AE11 | GND_38 | GND_134 | N20 |
| AE12 | GND_39 | GND_135 | N21 |
| AE13 | GND_40 | GND_136 | N22 |
| AE14 | GND_41 | GND_137 | N23 |
| AE15 | GND_42 | GND_138 | N24 |
| AE16 | GND_43 | GND_139 | N25 |
| AE17 | GND_44 | GND_140 | P12 |
| AE18 | GND_45 | GND_141 | P14 |
| AE19 | GND_46 | GND_142 | P16 |
| AE20 | GND_47 | GND_143 | P18 |
| AE21 | GND_48 | GND_144 | P20 |
| AE22 | GND_49 | GND_145 | P22 |
| AE23 | GND_50 | GND_146 | P24 |
| AE24 | GND_51 | GND_147 | R2 |
| AE25 | GND_52 | GND_148 | R5 |
| AG2 | GND_53 | GND_149 | R31 |
| AG31 | GND_54 | GND_150 | R34 |
| AG34 | GND_55 | GND_151 | T11 |
| AK2 | GND_56 | GND_152 | T13 |
| AG5 | GND_57 | GND_153 | T15 |
| AK31 | GND_58 | GND_154 | T17 |
| AK34 | GND_59 | GND_155 | T19 |
| AK5 | GND_60 | GND_156 | T21 |
| AK14 | GND_61 | GND_157 | T23 |
| AL6 | GND_62 | GND_158 | T25 |
| AL9 | GND_63 | GND_159 | U11 |
| AL12 | GND_64 | GND_160 | U12 |
| AL15 | GND_65 | GND_161 | U13 |
| AL18 | GND_66 | GND_162 | U14 |
| AL21 | GND_67 | GND_163 | U15 |
| AL24 | GND_68 | GND_164 | U16 |
| AL27 | GND_69 | GND_165 | U17 |
| AL30 | GND_70 | GND_166 | U18 |
| AN2 | GND_71 | GND_167 | U19 |
| AN34 | GND_72 | GND_168 | U20 |
| AP3 | GND_73 | GND_169 | U21 |
| AP6 | GND_74 | GND_170 | U22 |
| AP9 | GND_75 | GND_171 | U23 |
| AP12 | GND_76 | GND_172 | U24 |
| AP15 | GND_77 | GND_173 | U25 |
| AP18 | GND_78 | GND_174 | V2 |
| AP21 | GND_79 | GND_175 | V5 |
| AP24 | GND_80 | GND_176 | V9 |
| AP27 | GND_81 | GND_177 | V12 |
| AP30 | GND_82 | GND_178 | V14 |
| AP33 | GND_83 | GND_179 | V16 |
| B3 | GND_84 | GND_180 | V18 |
| B6 | GND_85 | GND_181 | V20 |
| B9 | GND_86 | GND_182 | V22 |
| B12 | GND_87 | GND_183 | V24 |
| B15 | GND_88 | GND_184 | V31 |
| B21 | GND_89 | GND_185 | Y11 |
| B24 | GND_90 | GND_186 | Y13 |
| B27 | GND_91 | GND_187 | Y15 |
| B30 | GND_92 | GND_188 | Y17 |
| B33 | GND_93 | GND_189 | Y19 |
| C2 | GND_94 | GND_190 | Y21 |
| C34 | GND_95 | GND_191 | Y23 |
| E6 | GND_96 | GND_192 | Y25 |

N12x_GSD

PLACE UNDER BALLS

+VCC_GFX_CORE

NVVDD
DA-05206_V04:Page 20
Scott-0710

0809

| | |
|---|---|
| C250 | 0.01u/25V/X7R_GSD |
| C247 | 0.01u/25V/X7R_GSD |
| C243 | 0.01u/25V/X7R_GSD |
| C265 | 0.01u/25V/X7R_GSD |
| C284 | 0.01u/25V/X7R_GSD |
| C311 | 0.01u/25V/X7R_GSD |
| C289 | 0.01u/25V/X7R_GSD |
| C257 | 0.01u/25V/X7R_GSD |
| C253 | 0.022U/16V/X7R_GSD |
| C277 | 0.022U/16V/X7R_GSD |
| C267 | 0.022U/16V/X7R_GSD |
| C248 | 0.047U/16V/X7R_GSD |
| C271 | 0.047U/16V/X7R_GSD |
| C239 | 0.047U/16V/X7R_GSD |
| C301 | 0.1u/16V/X7R_GSD |
| C299 | 0.1u/16V/X7R_GSD |
| C258 | 0.22u/6.3V/X5R_GSD |
| C295 | 0.22u/6.3V/X5R_GSD |
| C297 | 0.22u/6.3V/X5R_GSD |
| C276 | 1U/6.3V/X5R_GSD |

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PLACE NEAR BALLS

+VCC_GFX_CORE

| | |
|---|---|
| C294 | 4.7U/6.3V/X5R_6_GSD |
| C270 | 10U/6.3V/X5R_8_GSD |
| C308 | 10U/6.3V/X5R_8_GSD |
| C317 | 10U/6.3V/X5R_8_GSD |
| C318 | 10U/6.3V/X5R_8_GSD |

0717

0817

NB5

PROJECT : TWH
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| A3 | DGPU 5/5 (Power/Ground) | 1A |

Date: Friday, August 27, 2010 Sheet 19 of 57

# CHANNEL A: 256MB/512MB DDR3

(16) VMA_DQ[63..0]
(16) VMA_DM[7..0]
(16) VMA_WDQS[7..0]
(16) VMA_RDQS[7..0]

VRAM3 / VRAM7 / VRAM4 / VRAM8 — 96-BALL SDRAM DDR3 — VRAM_DDR3_GSD

Should be 240 Ohms +-1%

R333 240/F_GSD
R636 240/F_GSD
R349 240/F_GSD
R623 240/F_GSD

+1.5V_GFX

FBCLK Termination
DA-05093-001_V02:Page 96
R=160/F
Scott-0710

Placement has to be close to VRAM

VMA_CLK0 — R347 162/F_GSD — VMA_CLK0#
VMA_CLK1 — R351 162/F_GSD — VMA_CLK1#

R638 1.33K/F_GSD — VREFC_VMA1 — R637 1.33K/F_GSD — C355 0.01u/25V/X7R_N12P
R345 1.33K/F_GSD — VREFD_VMA1 — R346 1.33K/F_GSD — C394 0.01u/25V/X7R_N12P
R344 1.33K/F_GSD — VREFC_VMA3 — R343 1.33K/F_GSD — C391 0.01u/25V/X7R_N12P
R634 1.33K/F_GSD — VREFD_VMA3 — R633 1.33K/F_GSD — C645 0.01u/25V/X7R_N12P

(16) FBA_CMD17 — TP17
(16) FBA_CMD1 — TP18

C569 *4.7U/6.3V/X5R_6_NC

C327 1U/6.3V/X5R_GSD
C359 1U/6.3V/X5R_GSD
C649 1U/6.3V/X5R_GSD
C390 1U/6.3V/X5R_GSD

C179 10U/6.3V/X5R_8_GSD
C627 0.1U/16V/X7R_GSD
C639 0.1U/16V/X7R_GSD
C642 *0.1U/16V/X7R_GSD_NC
C641 *0.1U/16V/X7R_GSD_NC
C397 0.1U/16V/X7R_GSD

C637 10U/6.3V/X5R_8_GSD
C398 0.1U/16V/X7R_GSD
C352 0.1U/16V/X7R_GSD
C615 0.1U/16V/X7R_GSD
C568 *0.1U/16V/X7R_GSD_NC
C361 0.1U/16V/X7R_GSD
C392 0.1U/16V/X7R_GSD
C389 0.1U/16V/X7R_GSD

C377 10U/6.3V/X5R_8_GSD
C638 10U/6.3V/X5R_8_GSD
C379 0.1U/16V/X7R_GSD
C567 *0.1U/16V/X7R_GSD_NC
C353 *0.1U/16V/X7R_GSD_NC
C363 0.1U/16V/X7R_GSD
C323 0.1U/16V/X7R_GSD

C386 10U/6.3V/X5R_8_GSD
C180 10U/6.3V/X5R_8_GSD
C630 *0.1U/16V/X7R_GSD_NC
C578 0.1U/16V/X7R_GSD
C640 0.1U/16V/X7R_GSD

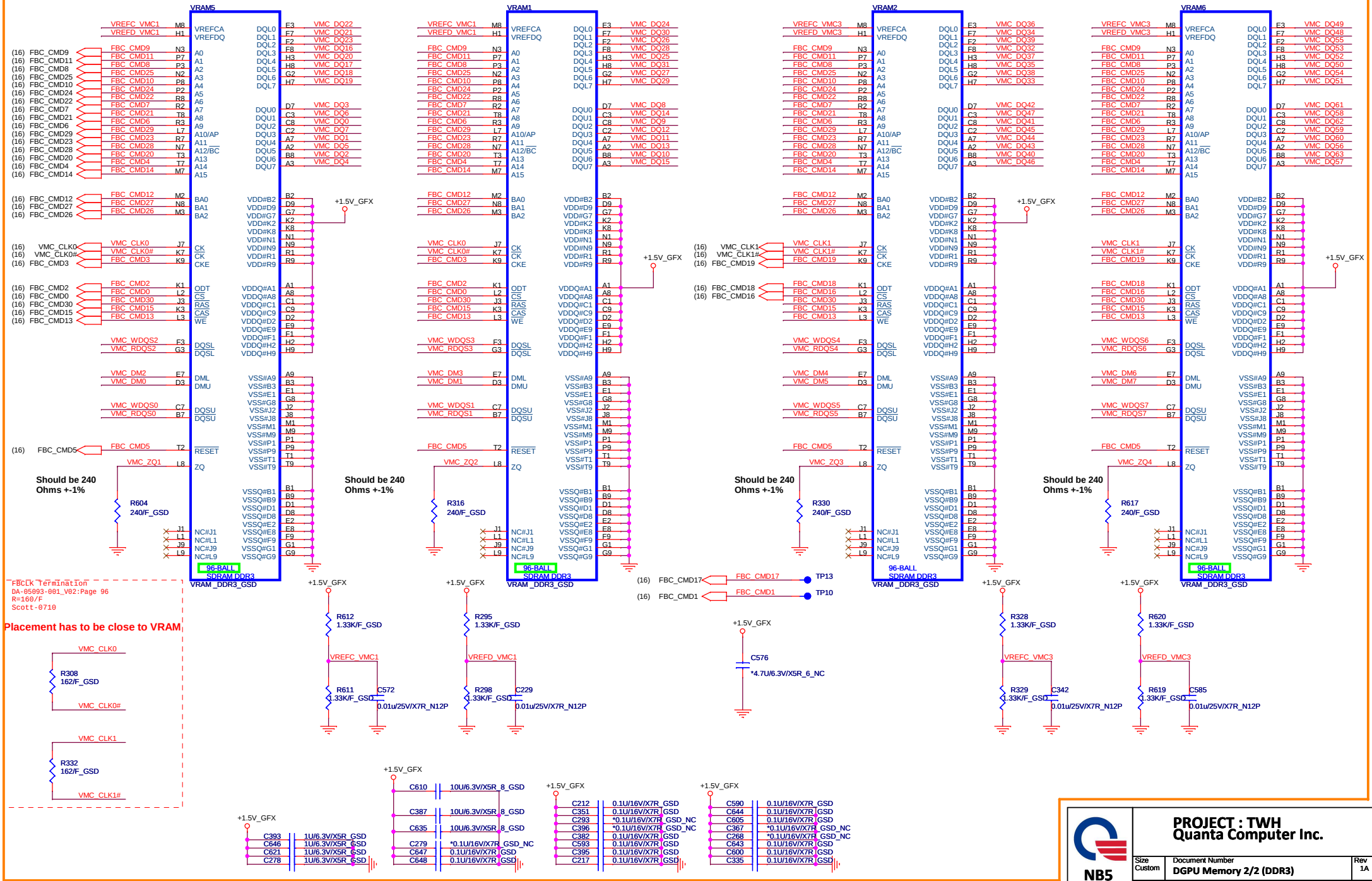
NB5

PROJECT : TWH
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | DGPU Memory 1/2 (DDR3) | 1A |
| Date: Friday, August 27, 2010 | Sheet 20 of 57 | |

# CHANNEL B: 256MB/512MB DDR3

(16) VMC_DQ[63..0]
(16) VMC_DM[7..0]
(16) VMC_WDQS[7..0]
(16) VMC_RDQS[7..0]

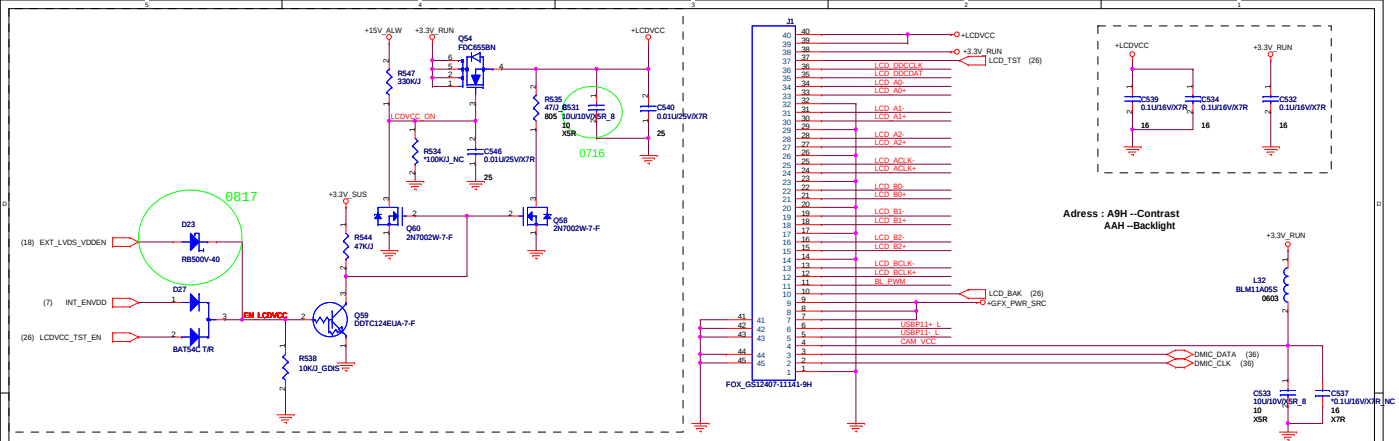


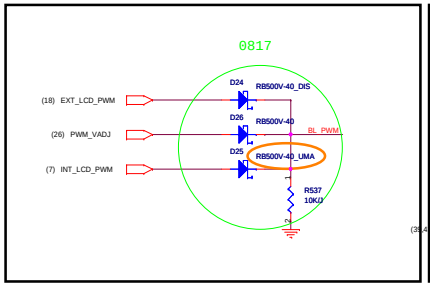

NB5

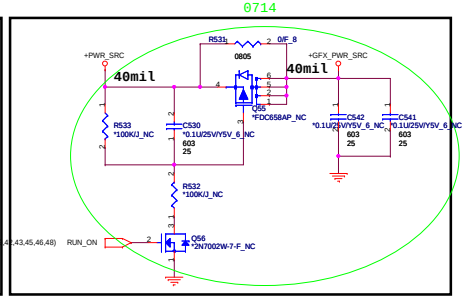
PROJECT : TWH
Quanta Computer Inc.

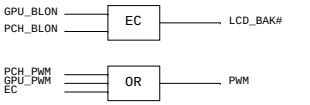
| Size | Document Number | Rev |
|---|---|---|
| Custom | DGPU Memory 2/2 (DDR3) | 1A |

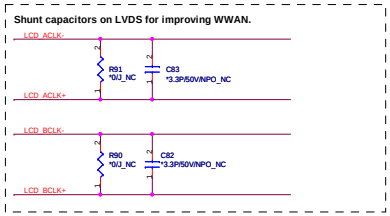
Date: Friday, August 27, 2010 Sheet 21 of 57

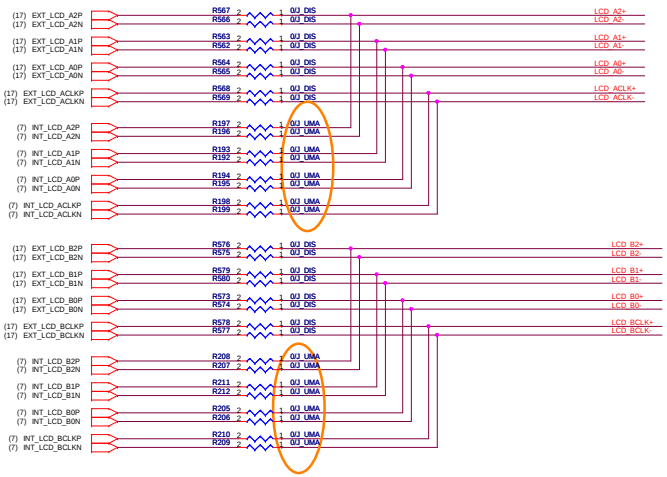


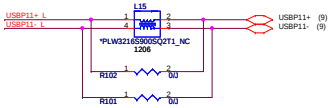



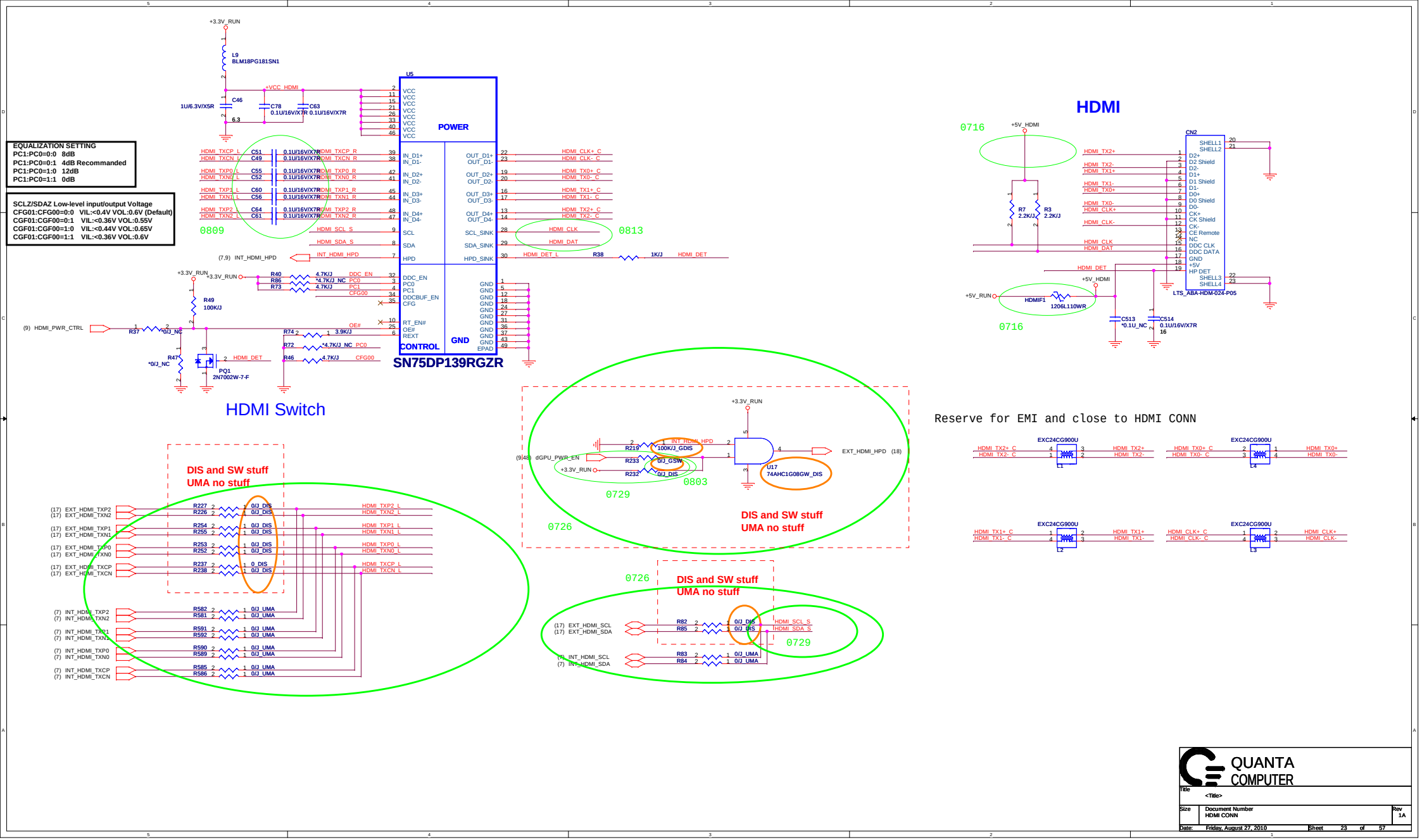





Quanta Computer Inc.
PROJECT : GM6C MLK DIS

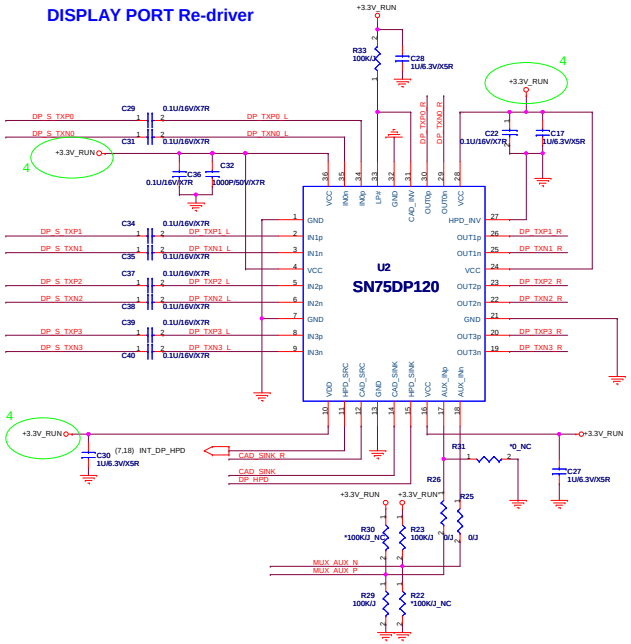
| Size | Document Number | Rev |
|---|---|---|
| | LCD CONN | 1A |

Date: Friday, August 27, 2010 Sheet 22 of 57

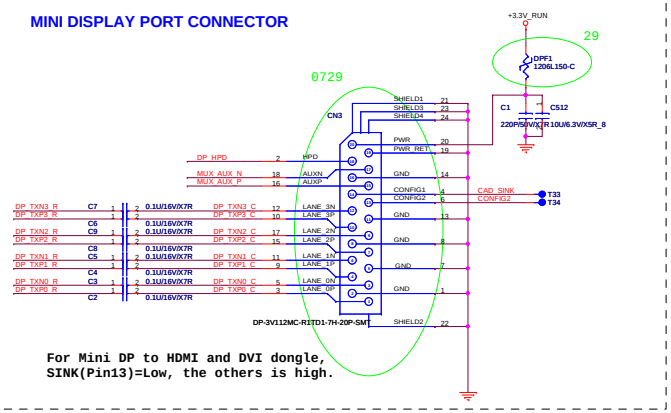



| | | | |
|---|---|---|---|
| QUANTA COMPUTER | | | |
| Title | <Title> | | |
| Size | Document Number HDMI CONN | | Rev 1A |
| Date: Friday, August 27, 2010 | Sheet 23 of 57 | | |

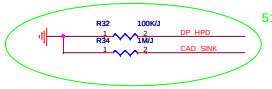
## DISPLAY PORT Re-driver

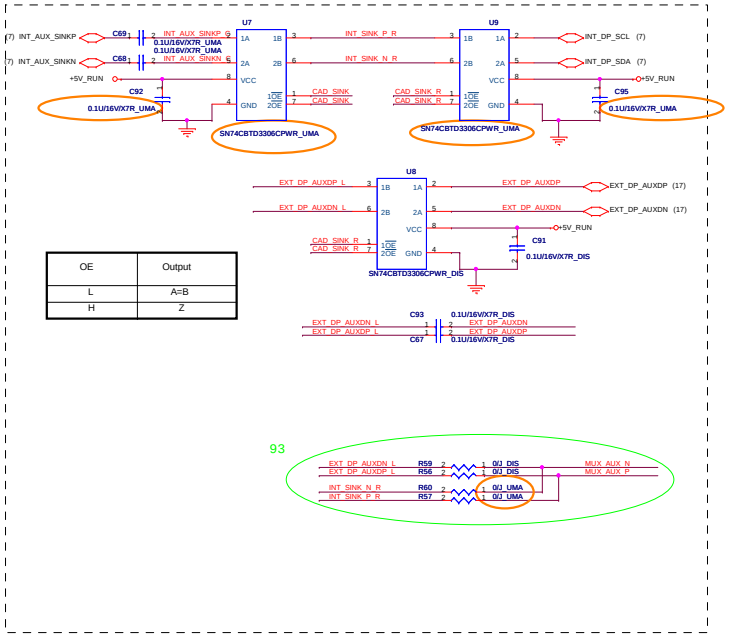



## MINI DISPLAY PORT CONNECTOR

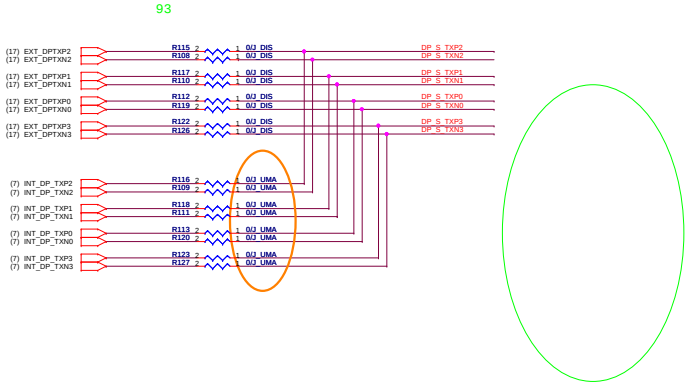



**For Mini DP to HDMI and DVI dongle, SINK(Pin13)=Low, the others is high.**




| OE | Output |
|---|---|
| L | A=B |
| H | Z |

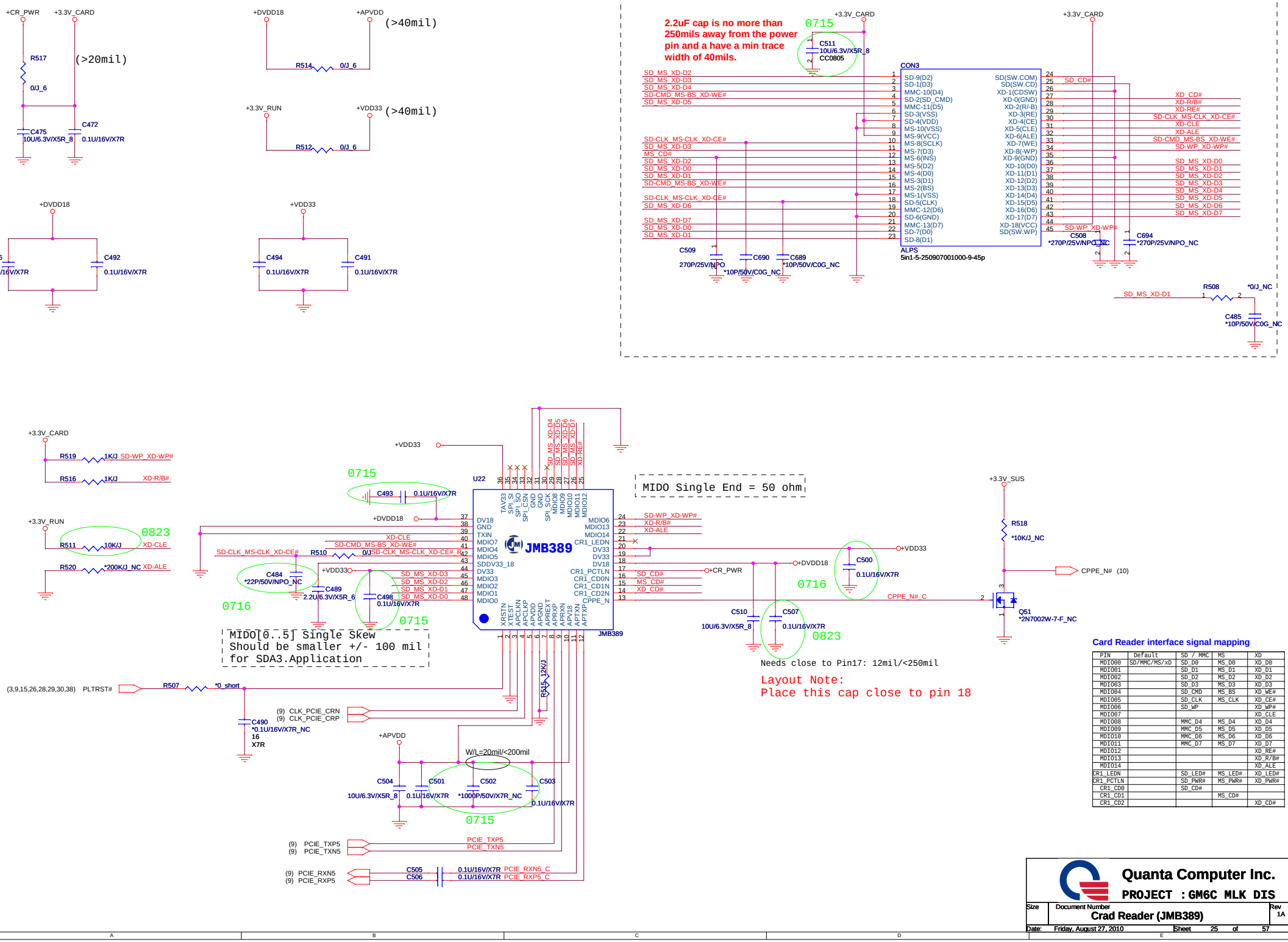









| | | |
|---|---|---|
| QUANTA COMPUTER | | |
| Title | <Title> | |
| Size | Document Number: MINI DP CONN | Rev: 1A |
| Date: Friday, August 27, 2010 | Sheet 24 of 57 | |




**Card Reader interface signal mapping**

| PIN | Default | SD / MMC | MS | XD |
|---|---|---|---|---|
| MDIO00 | SD/MMC/MS/xD | SD_D0 | MS_D0 | XD_D0 |
| MDIO01 | | SD_D1 | MS_D1 | XD_D1 |
| MDIO02 | | SD_D2 | MS_D2 | XD_D2 |
| MDIO03 | | SD_D3 | MS_D3 | XD_D3 |
| MDIO04 | | SD_CMD | MS_BS | XD_WE# |
| MDIO05 | | SD_CLK | MS_CLK | XD_CE# |
| MDIO06 | | SD_WP | | XD_WP# |
| MDIO07 | | | | XD_CLE |
| MDIO08 | | MMC_D4 | MS_D4 | XD_D4 |
| MDIO09 | | MMC_D5 | MS_D5 | XD_D5 |
| MDIO10 | | MMC_D6 | MS_D6 | XD_D6 |
| MDIO11 | | MMC_D7 | MS_D7 | XD_D7 |
| MDIO12 | | | | XD_RE# |
| MDIO13 | | | | XD_R/B# |
| MDIO14 | | | | XD_ALE |
| CR1_LEDN | | SD_LED# | MS_LED# | XD_LED# |
| CR1_PCTLN | | SD_PWR# | MS_PWR# | XD_PWR# |
| CR1_CD0 | | SD_CD# | | |
| CR1_CD1 | | | MS_CD# | |
| CR1_CD2 | | | | XD_CD# |

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | Crad Reader (JMB389) | 1A |
| Date: Friday, August 27, 2010 | Sheet 25 of 57 | |

BX1 leakage issue workaround circuit
R96,C104 no stuff,R100 stuff
BX2 will close it.
R96,C104 stuff,R100 no stuff

Layout Note: Place these caps close to ITE8502

Layout Note: Place PC169 close to ITE8502

# IT8518E/BX1

U11

LPC
CIR
GPIO
SM BUS
PS/2
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK

prochot pin level shift

Board ID Straps

| Config_0 | Config_1 | GM6/GM6C |
|---|---|---|
| 0 | 0 | UMA |
| 0 | 1 | Studio Optimum |
| 1 | 0 | Studio Discrete |

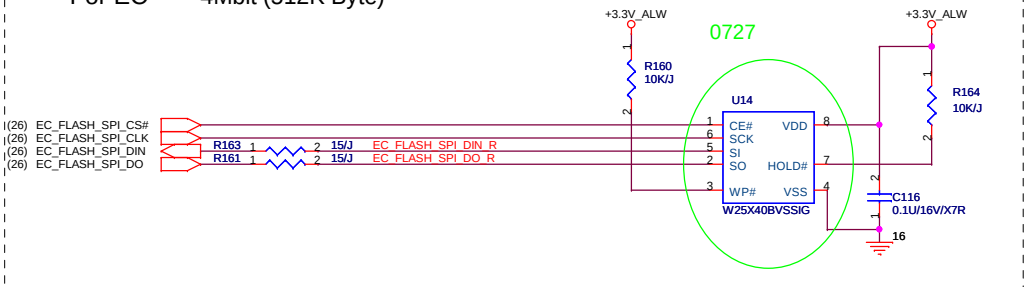
| USB_BACK_EN# | BID1 | GM6/GM6C |
|---|---|---|
| 0 | 0 | SSI (X00) |
| 0 | 1 | PT (X01) |
| 1 | 0 | ST (X02) |
| 1 | 1 | OT (A00) |
| 0 | 0 | (A01) |

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

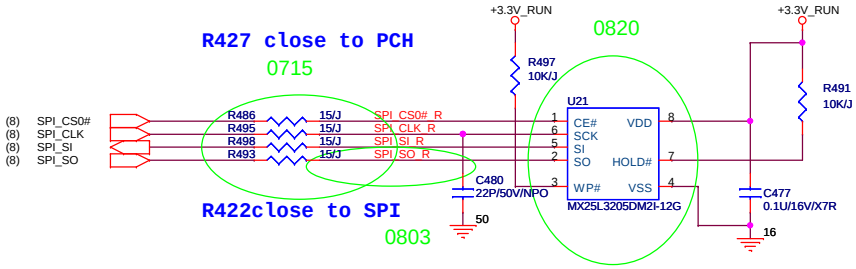
| Size | Document Number | Rev |
|---|---|---|
| | SIO (ITE8518) | 1A |

Date: Friday, August 27, 2010 Sheet 26 of 57

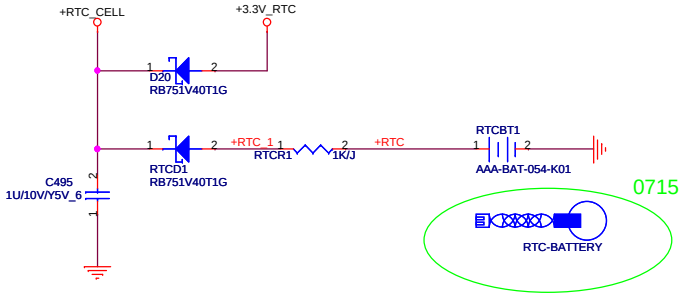
## For EC 4Mbit (512K Byte)



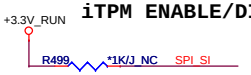

## For PCH 32Mbit (4M Byte)




## RTC BATTERY




## iTPM ENABLE/DISABLE




| TPM Function | R428 |
|---|---|
| Enable | Mount |
| Disable | NC (Default) |

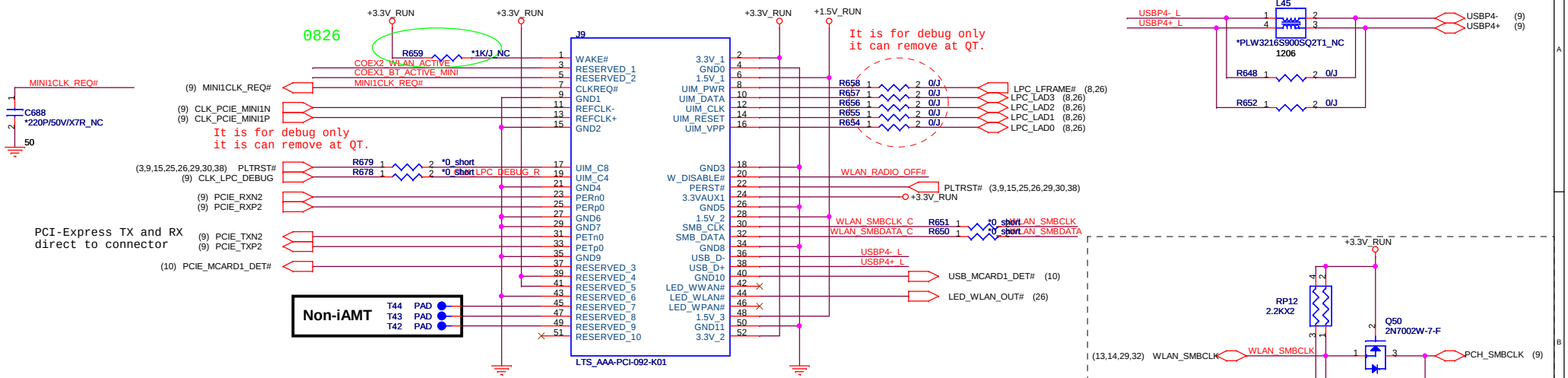
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | FLASH/RTC | 1A |

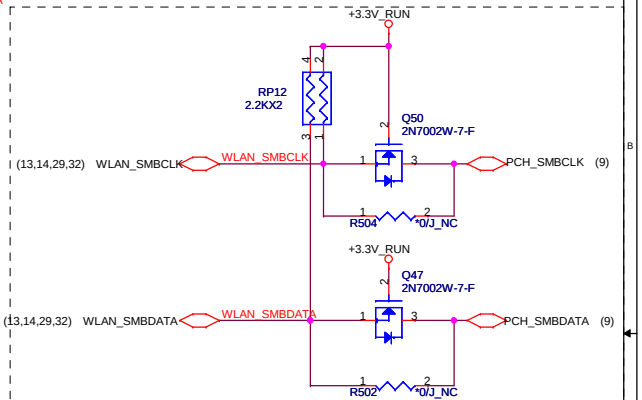
Date: Friday, August 27, 2010 Sheet 27 of 57

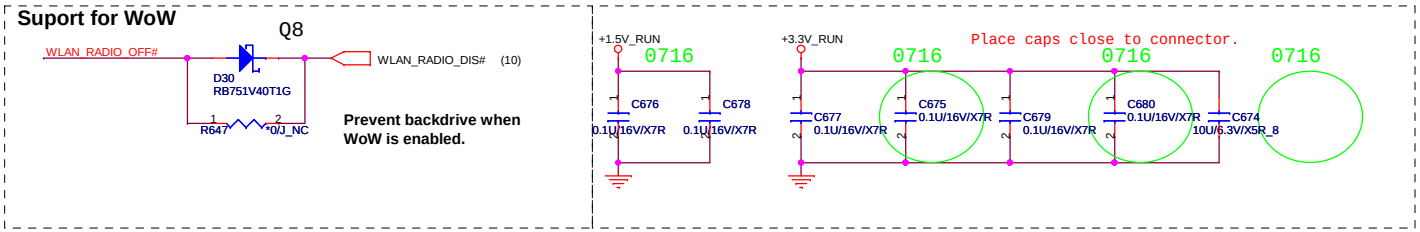
# MiniCard WLAN connector



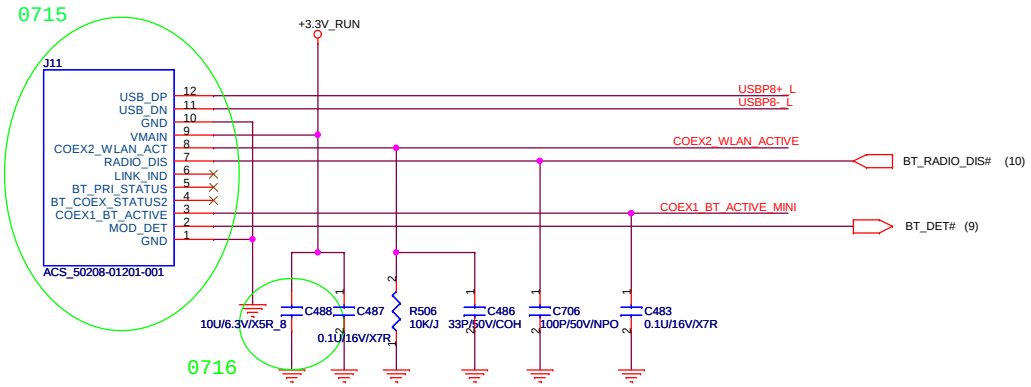


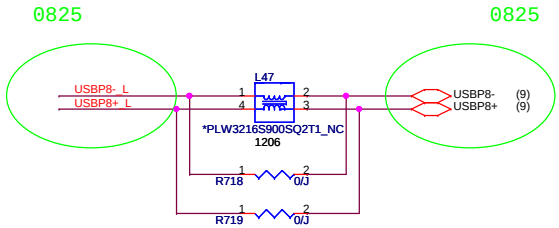





## Support Dell BT375 (Little Stone) module (XPS) W TO B

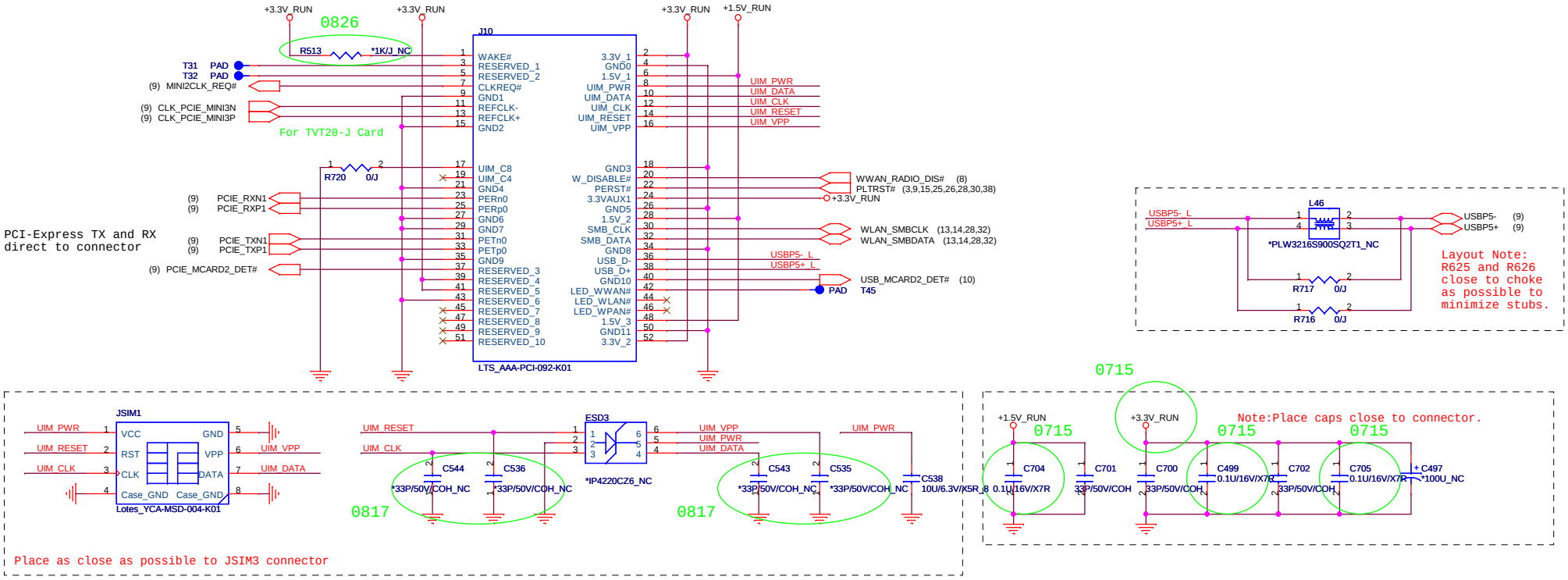



Quanta Computer Inc.
PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | MINI-Card (WLAN/WPAN) | 1A |
| Date: Friday, August 27, 2010 | Sheet 28 of 57 | |

# MiniCard WWAN connector











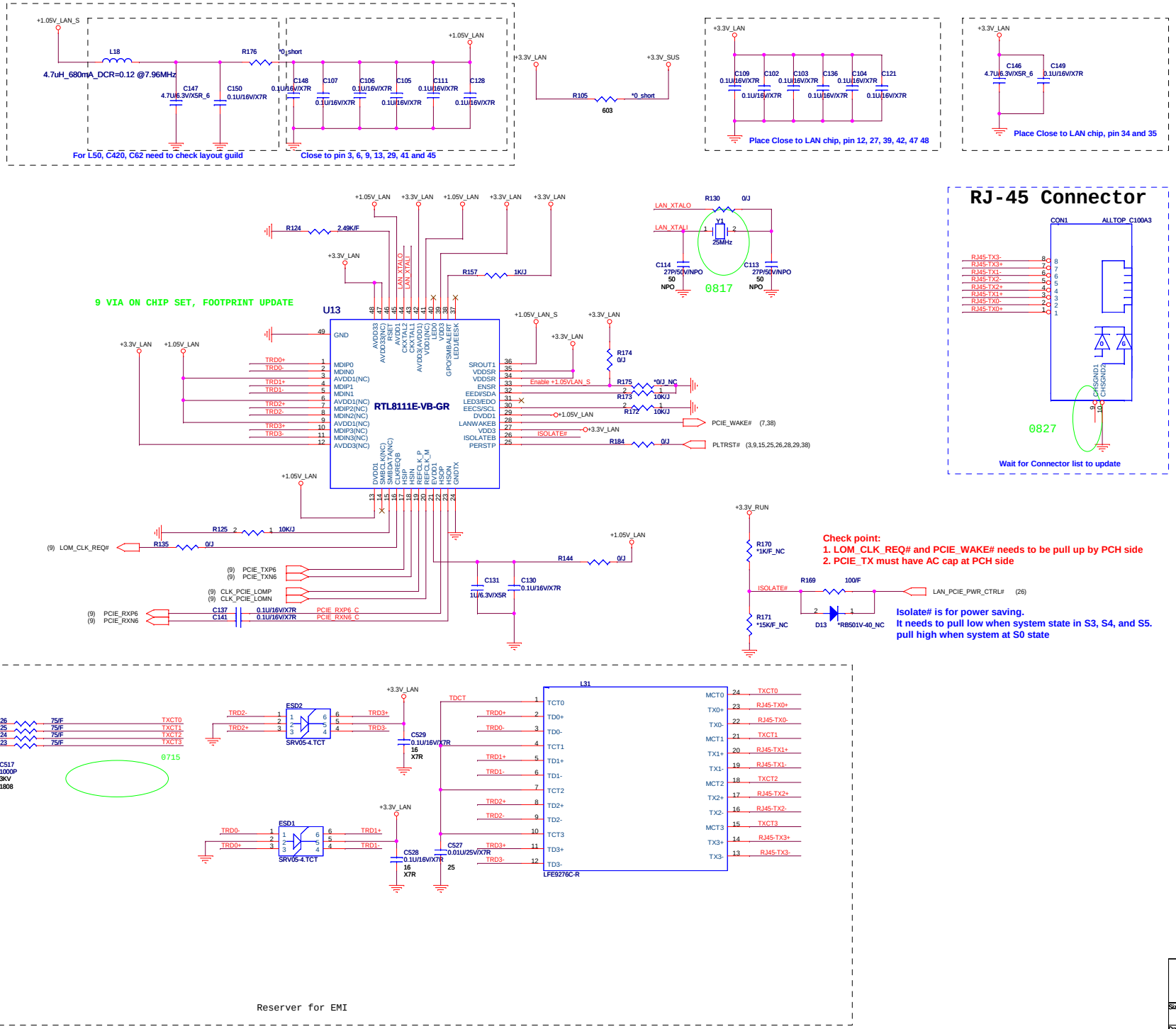


Quanta Computer Inc.

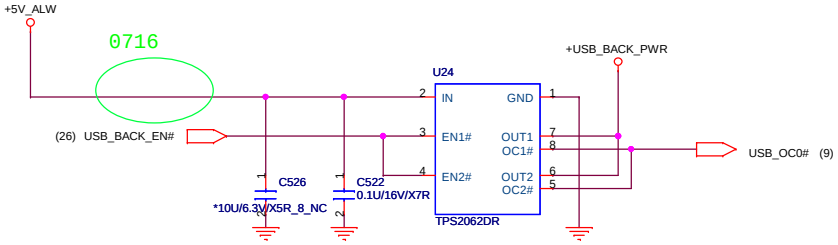
PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | MINI-Card (WWAN) | 1A |

Date: Friday, August 27, 2010 Sheet 29 of 57

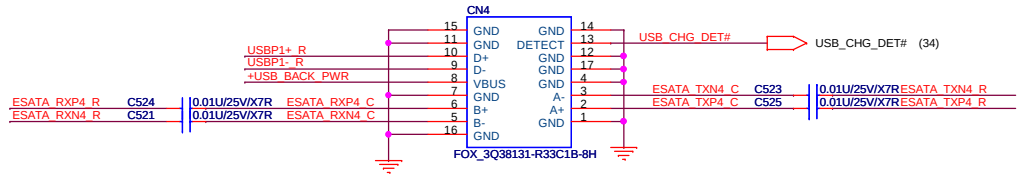

+1.05V_LAN_S
L18
4.7uH_680mA_DCR=0.12 @7.96MHz
R176
*0_short
C147
4.7U/6.3V/X5R_6
C150
0.1U/16V/X7R
+1.05V_LAN
C148
C107
C106
C105
C111
C128
0.1U/16V/X7R
For L50, C420, C62 need to check layout guild
Close to pin 3, 6, 9, 13, 29, 41 and 45
+3.3V_LAN
R105
603
*0_short
+3.3V_SUS
+3.3V_LAN
C109
C102
C103
C136
C104
C121
0.1U/16V/X7R
Place Close to LAN chip, pin 12, 27, 39, 42, 47 48
+3.3V_LAN
C146
4.7U/6.3V/X5R_6
C149
0.1U/16V/X7R
Place Close to LAN chip, pin 34 and 35
9 VIA ON CHIP SET, FOOTPRINT UPDATE
U13
RTL8111E-VB-GR
R124
2.49K/F
R157
1K/J
R130
0/J
LAN_XTALO
LAN_XTALI
Y1
25MHz
C114
27P/50V/NPO
C113
27P/50V/NPO
0817
R174
0/J
R175
*0/J_NC
R172
10K/J
R173
10K/J
R184
0/J
Enable +1.05VLAN_S
ISOLATE#
PCIE_WAKE# (7,38)
PLTRST# (3,9,15,25,26,28,29,38)
RJ-45 Connector
CON1
ALLTOP_C100A3
RJ45-TX3-
RJ45-TX3+
RJ45-TX1-
RJ45-TX2-
RJ45-TX2+
RJ45-TX1+
RJ45-TX0-
RJ45-TX0+
CHSGND1
CHSGND2
0827
Wait for Connector list to update
R125
10K/J
R135
0/J
(9) LOM_CLK_REQ#
R144
0/J
(9) PCIE_TXP6
(9) PCIE_TXN6
(9) CLK_PCIE_LOMP
(9) CLK_PCIE_LOMN
(9) PCIE_RXP6
(9) PCIE_RXN6
C137
C141
0.1U/16V/X7R
PCIE_RXP6_C
PCIE_RXN6_C
C131
1U/6.3V/X5R
C130
0.1U/16V/X7R
+3.3V_RUN
R170
*1K/F_NC
R171
*15K/F_NC
R169
100/F
D13
*RB501V-40_NC
LAN_PCIE_PWR_CTRL# (26)
Check point:
1. LOM_CLK_REQ# and PCIE_WAKE# needs to be pull up by PCH side
2. PCIE_TX must have AC cap at PCH side
Isolate# is for power saving.
It needs to pull low when system state in S3, S4, and S5.
pull high when system at S0 state
R526
R525
R524
R523
75/F
TXCT0
TXCT1
TXCT2
TXCT3
0715
C517
1000P
3KV
1808
ESD2
SRV05-4.TCT
ESD1
SRV05-4.TCT
C529
C528
0.1U/16V/X7R
C527
0.01U/25V/X7R
L31
LFE9276C-R
Reserver for EMI
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size
Document Number
LAN (RTL8111EL/RJ45)
Rev
1A
Date: Friday, August 27, 2010
Sheet 30 of 57

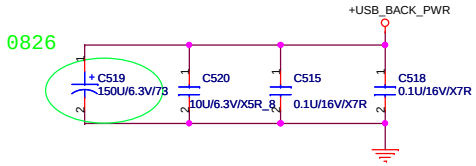
# ESATA + USB Conn + Power Share

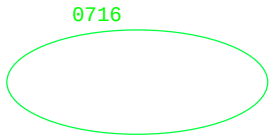


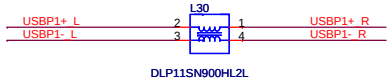

USB_BACK_EN# needs to be low when system S3 and S5 for USB charge

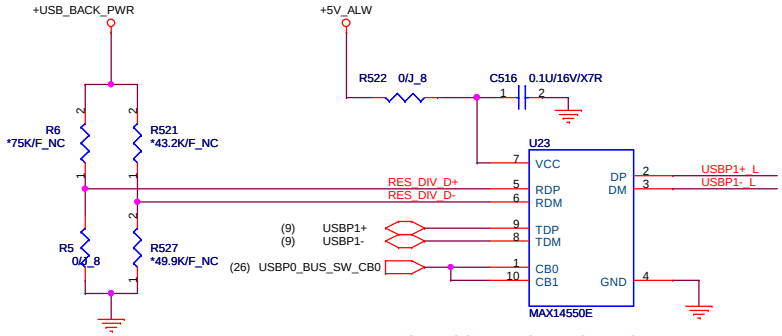
This pin connects to 3VALW ON POWER LOGIC




EC needs to drive CB0/CB1 pins to low
when system S3/S5 and dirve high when system S0.

U49 PN and Footprint needs to double check

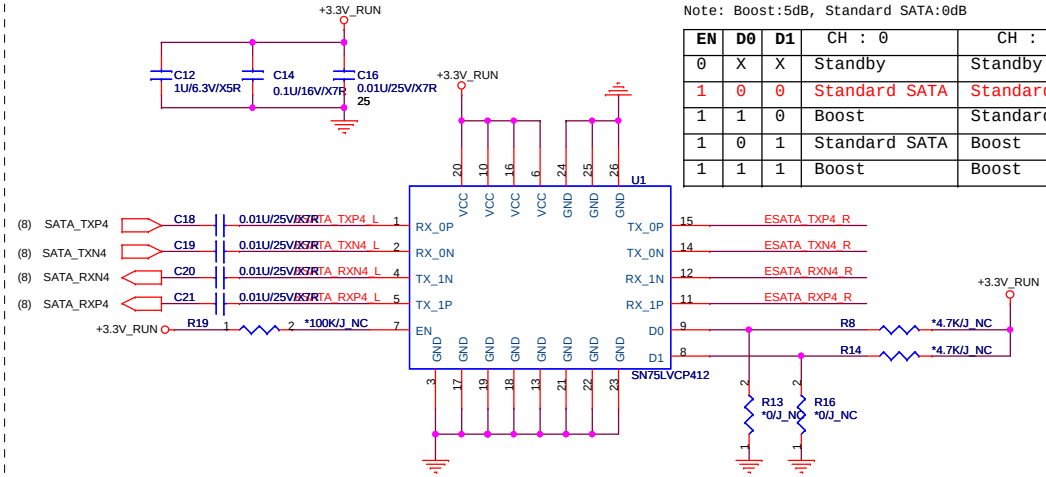
R15 needs to be 49.9K_F if we use external resisters.

| CB0 | CB1 | Function |
|---|---|---|
| 0 | 0 | Auto Detection active |
| 1 | 1 | USB Function only |

(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

## E-SATA Re-driver

Layout Note: Please put those on the same side of MB PCB



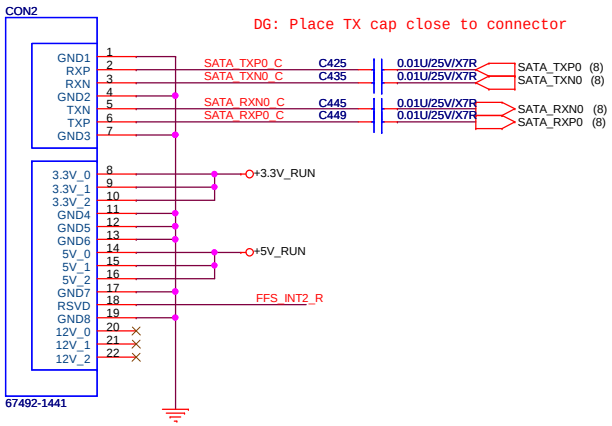

Note: Boost:5dB, Standard SATA:0dB

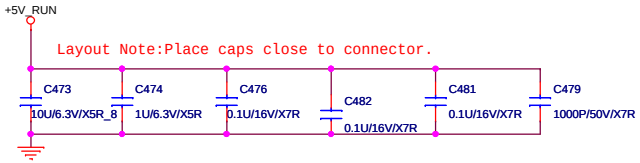
| EN | D0 | D1 | CH : 0 | CH : 1 |
|---|---|---|---|---|
| 0 | X | X | Standby | Standby |
| 1 | 0 | 0 | Standard SATA | Standard SATA |
| 1 | 1 | 0 | Boost | Standard SATA |
| 1 | 0 | 1 | Standard SATA | Boost |
| 1 | 1 | 1 | Boost | Boost |

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

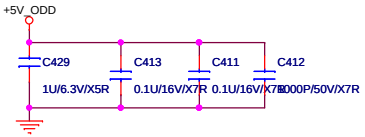
| Size | Document Number | Rev |
|---|---|---|
| | Righ PUSB/ESATA | 1A |
| Date: Friday, August 27, 2010 | Sheet 31 of 57 | |

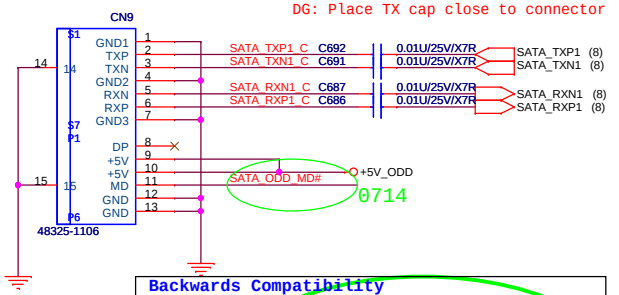
## SATA Connector.

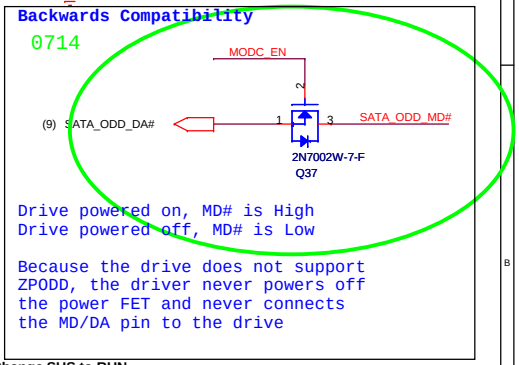


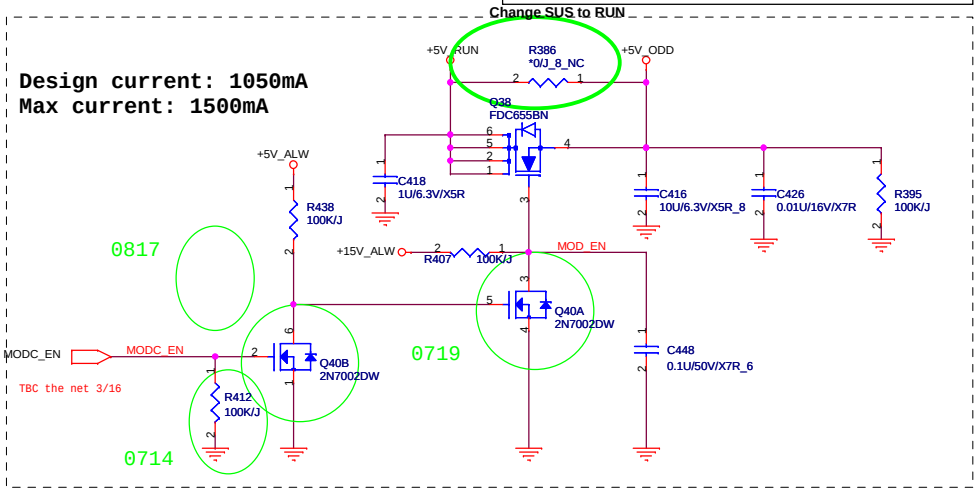



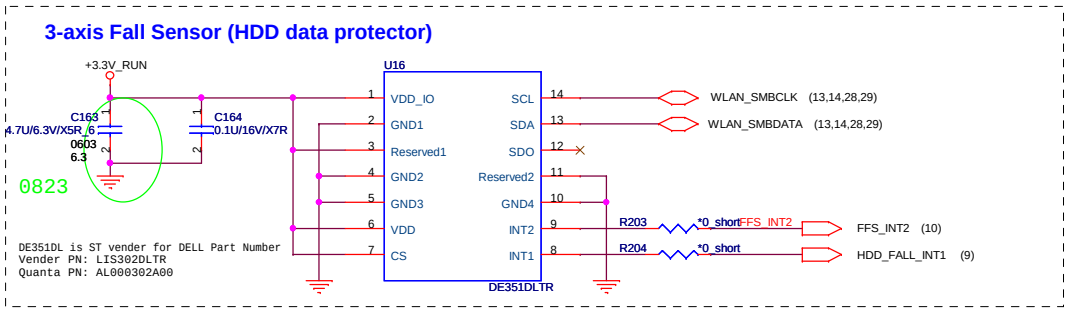

## ODD Connector

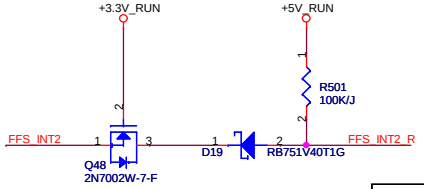



Quanta Computer Inc.
PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | SATA (HDD&ODD) | 1A |
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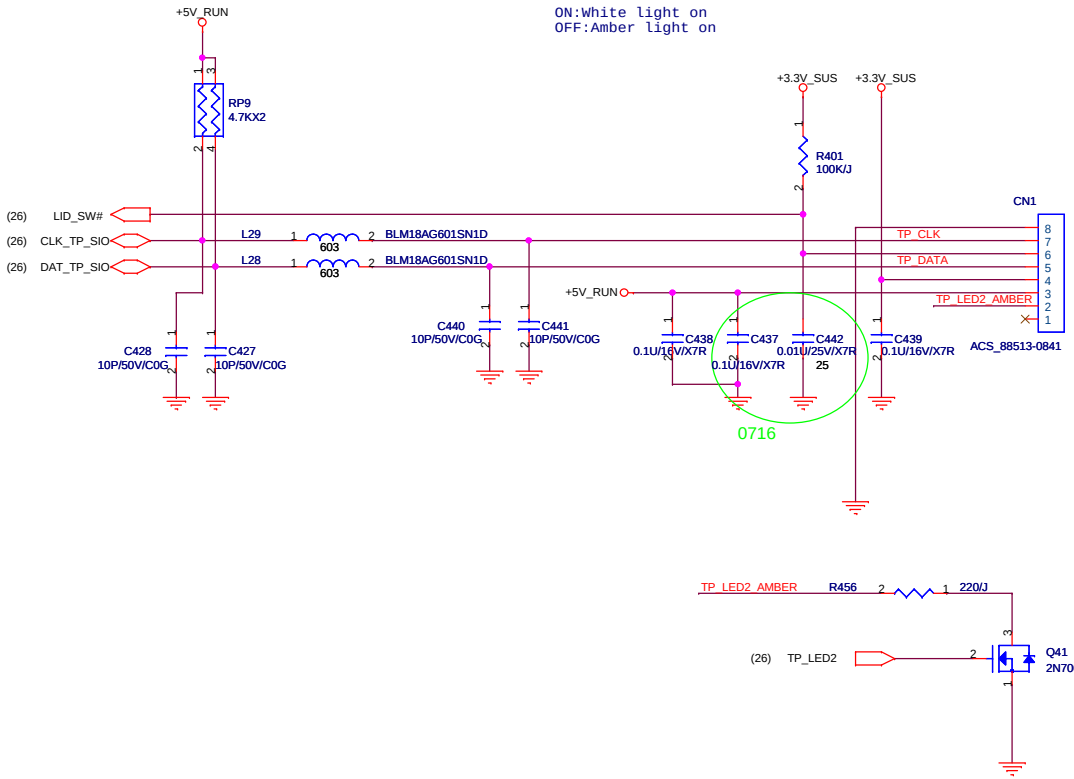
## Touch Pad

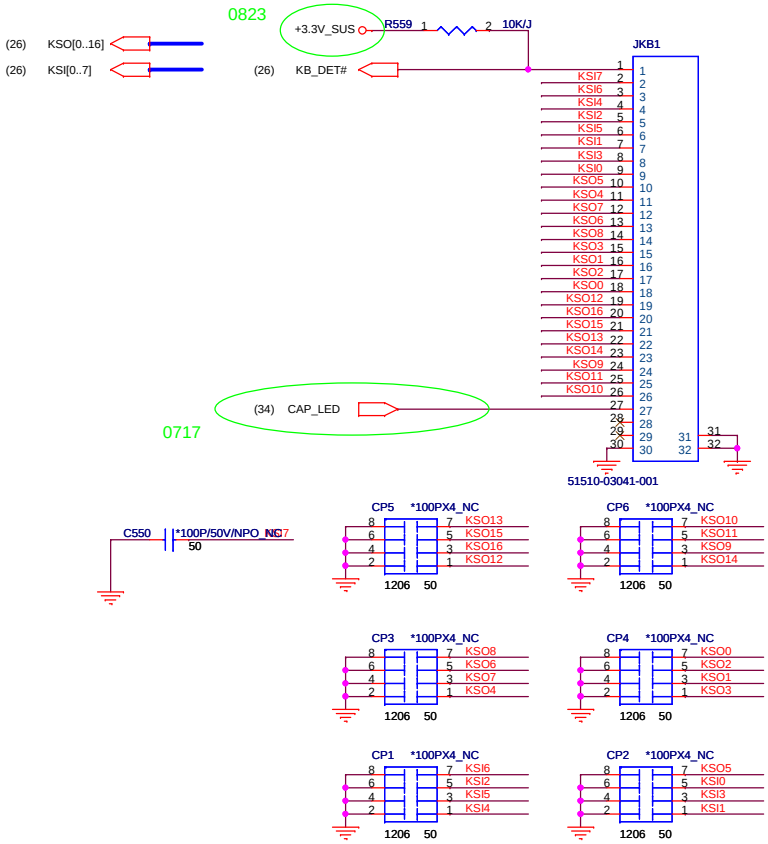
ON:White light on
OFF:Amber light on







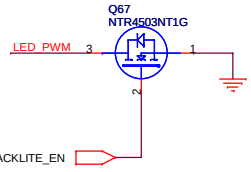
## KEYBOARD CONNECTOR

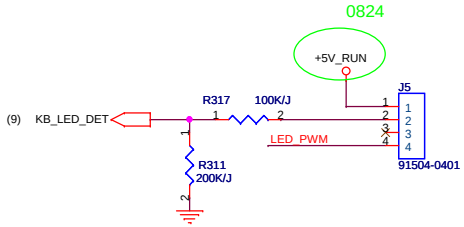


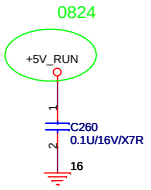

Layout Note: 100P CAPS CLOSE TO JKB3

## Key board illumination

+KB_LED power trace width >10 mil

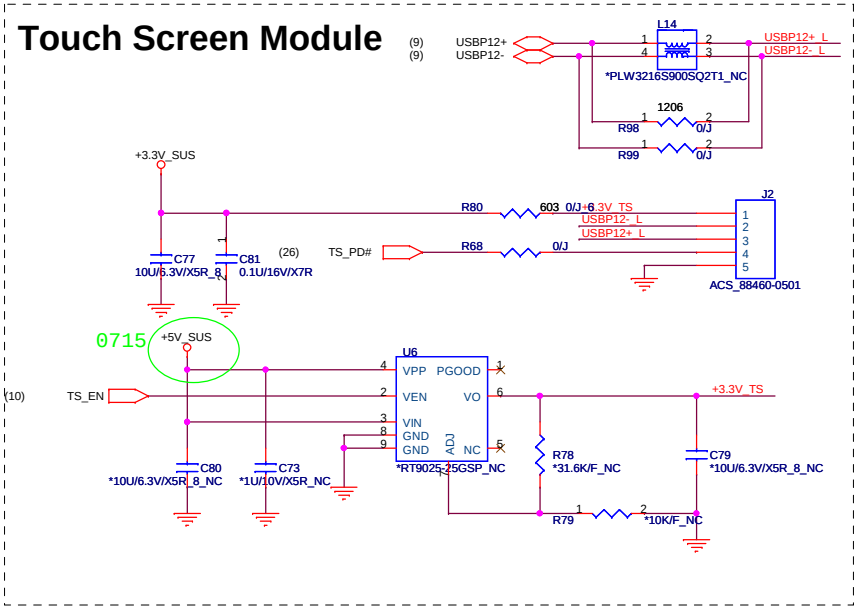


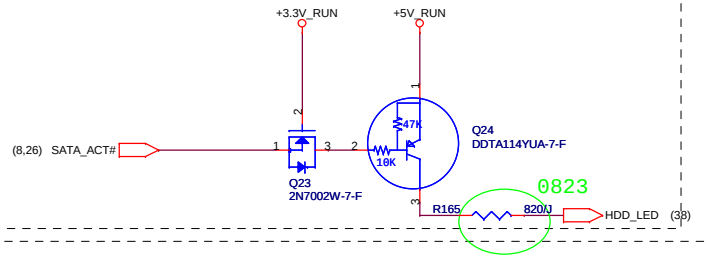




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : GM6C MLK DIS | | |
| Size | Document Number: TP/KB | Rev: 1A |
| Date: Friday, August 27, 2010 | Sheet 33 of 57 | |

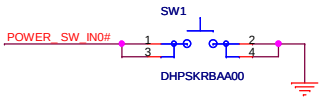
# Touch Screen Module



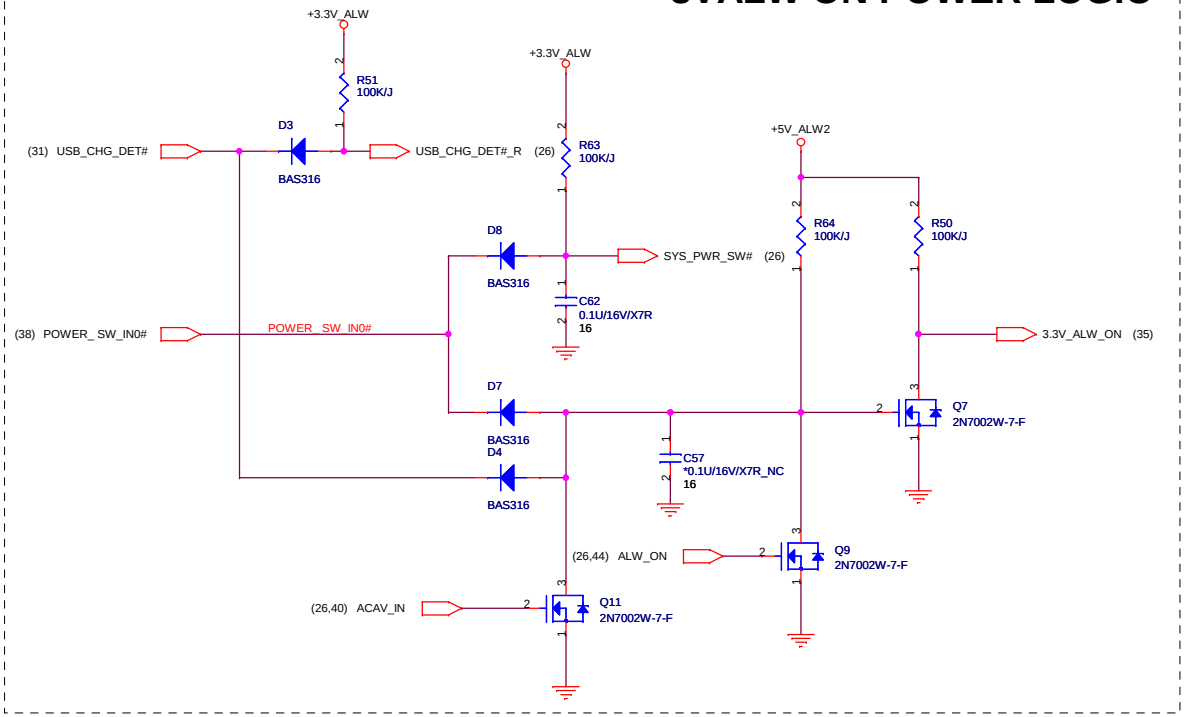

## HDD activity LED.



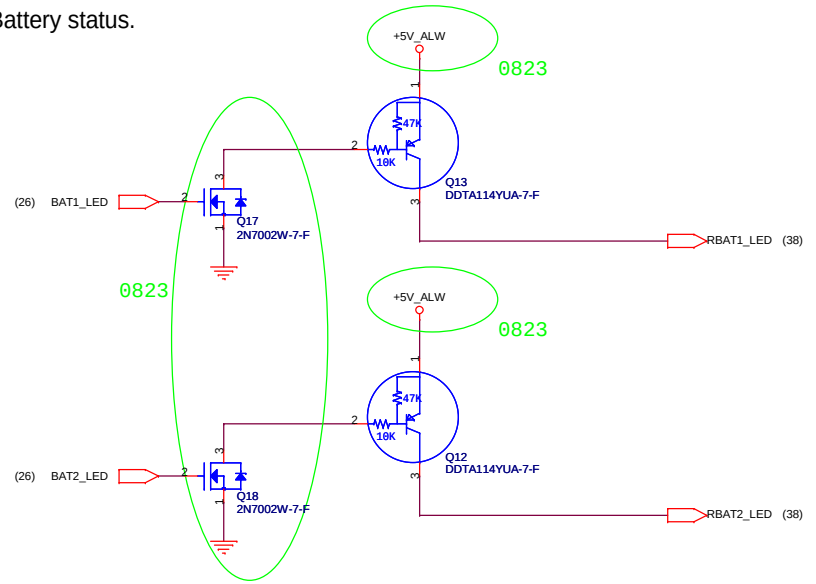

## Power button for Engineer

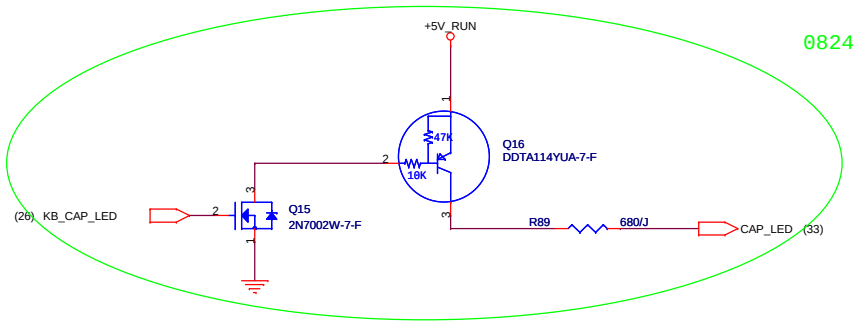


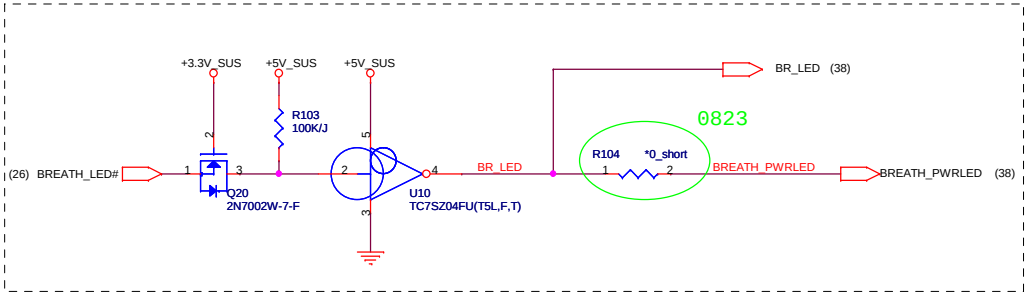

# 3VALW ON POWER LOGIC




## Battery status.




Quanta Computer Inc.
PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | SWITCH/LED/T-Screen | 1A |
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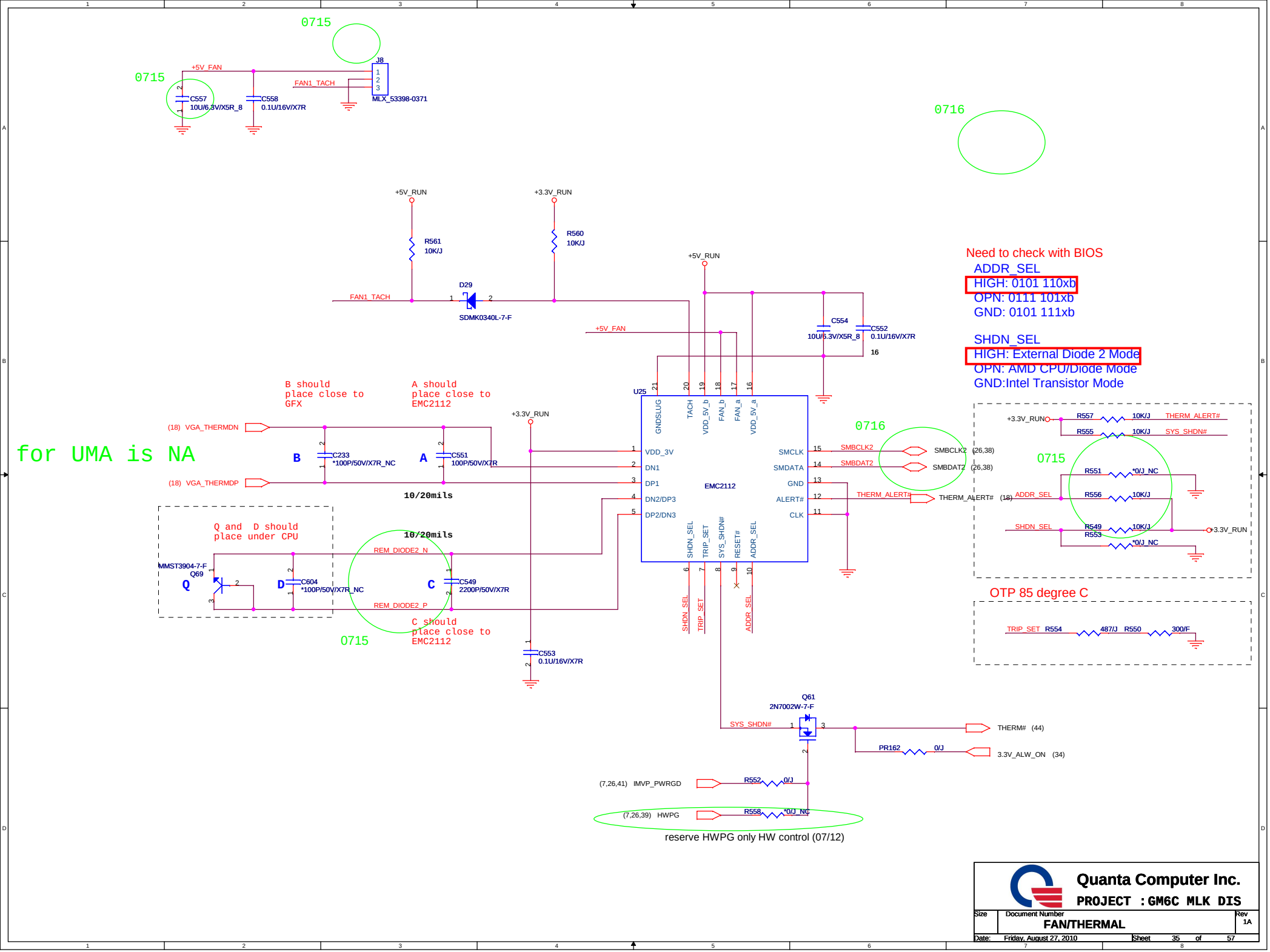
0715
+5V_FAN
FAN1_TACH
J8
MLX_53398-0371
C557
10U/6.3V/X5R_8
C558
0.1U/16V/X7R
0716
+5V_RUN
+3.3V_RUN
R561
10K/J
R560
10K/J
D29
SDMK0340L-7-F
C554
10U/6.3V/X5R_8
C552
0.1U/16V/X7R
16
Need to check with BIOS
ADDR_SEL
HIGH: 0101 110xb
OPN: 0111 101xb
GND: 0101 111xb
SHDN_SEL
HIGH: External Diode 2 Mode
OPN: AMD CPU/Diode Mode
GND:Intel Transistor Mode
B should place close to GFX
A should place close to EMC2112
for UMA is NA
(18) VGA_THERMDN
(18) VGA_THERMDP
B
C233
*100P/50V/X7R_NC
A
C551
100P/50V/X7R
10/20mils
U25
GNDSLUG
TACH
VDD_5V_b
FAN_b
FAN_a
VDD_5V_a
VDD_3V
DN1
DP1
DN2/DP3
DP2/DN3
EMC2112
SMCLK
SMDATA
GND
ALERT#
CLK
SMBCLK2
SMBDAT2
THERM_ALERT#
SHDN_SEL
TRIP_SET
SYS_SHDN#
RESET#
ADDR_SEL
Q and D should place under CPU
MMST3904-7-F
Q69
Q
D
C604
*100P/50V/X7R_NC
C
C549
2200P/50V/X7R
REM_DIODE2_N
REM_DIODE2_P
C should place close to EMC2112
C553
0.1U/16V/X7R
R557
10K/J
THERM_ALERT#
R555
10K/J
SYS_SHDN#
R551
*0/J_NC
R556
10K/J
R549
10K/J
R553
*0/J_NC
OTP 85 degree C
TRIP_SET
R554
487/J
R550
300/F
Q61
2N7002W-7-F
THERM# (44)
PR162
0/J
3.3V_ALW_ON (34)
(7,26,41) IMVP_PWRGD
R552
0/J
(7,26,39) HWPG
R558
*0/J_NC
reserve HWPG only HW control (07/12)
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size
Document Number
FAN/THERMAL
Rev
1A
Date: Friday, August 27, 2010
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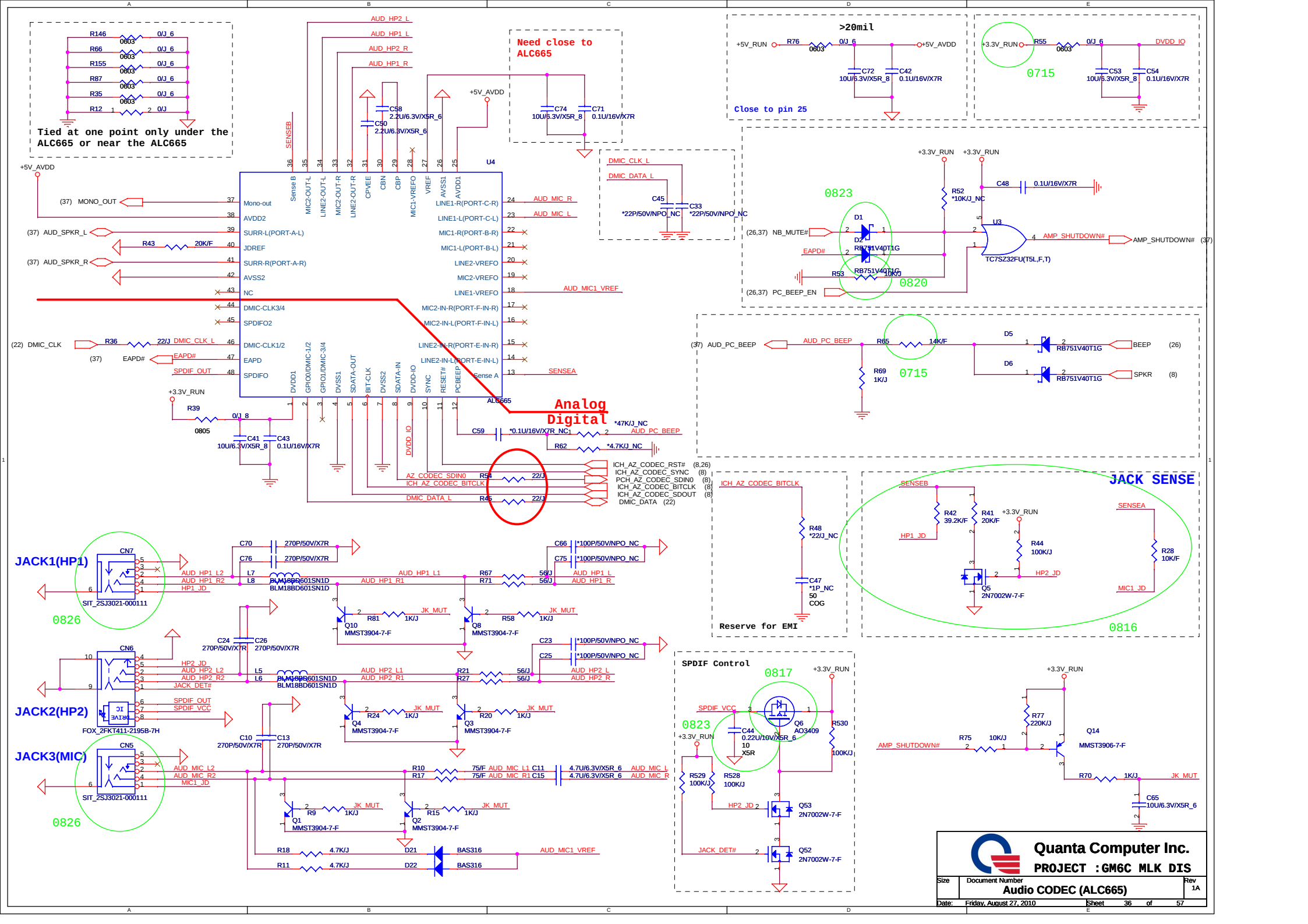
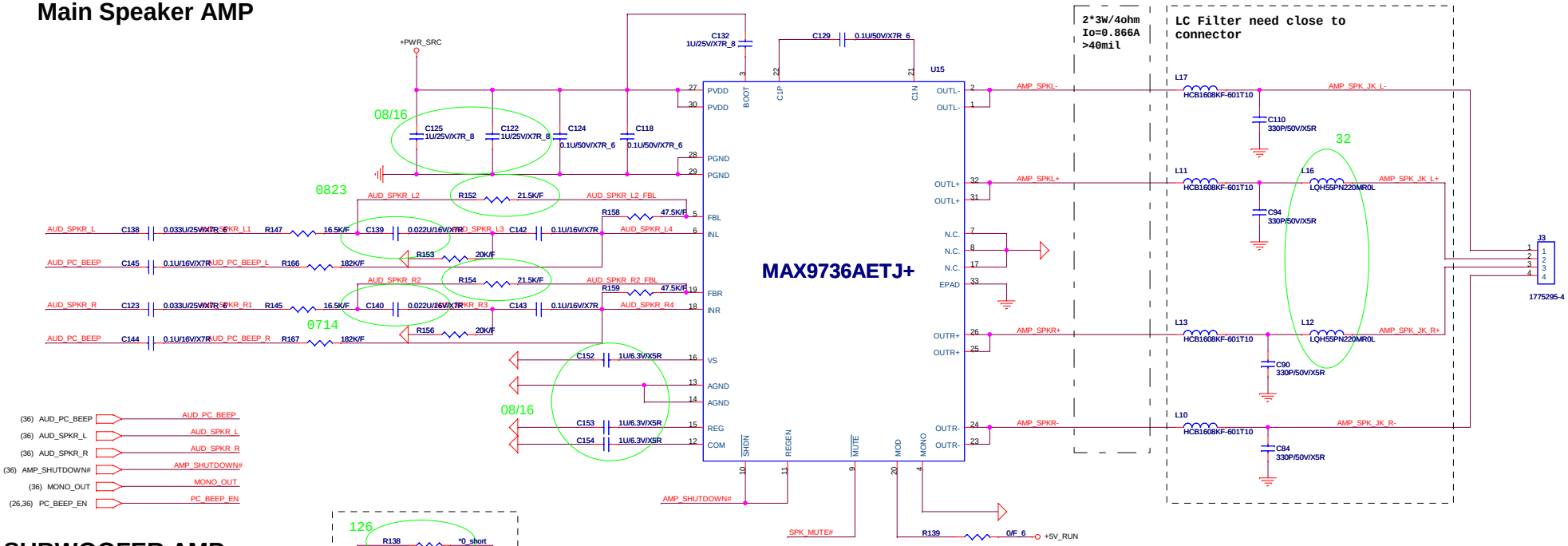
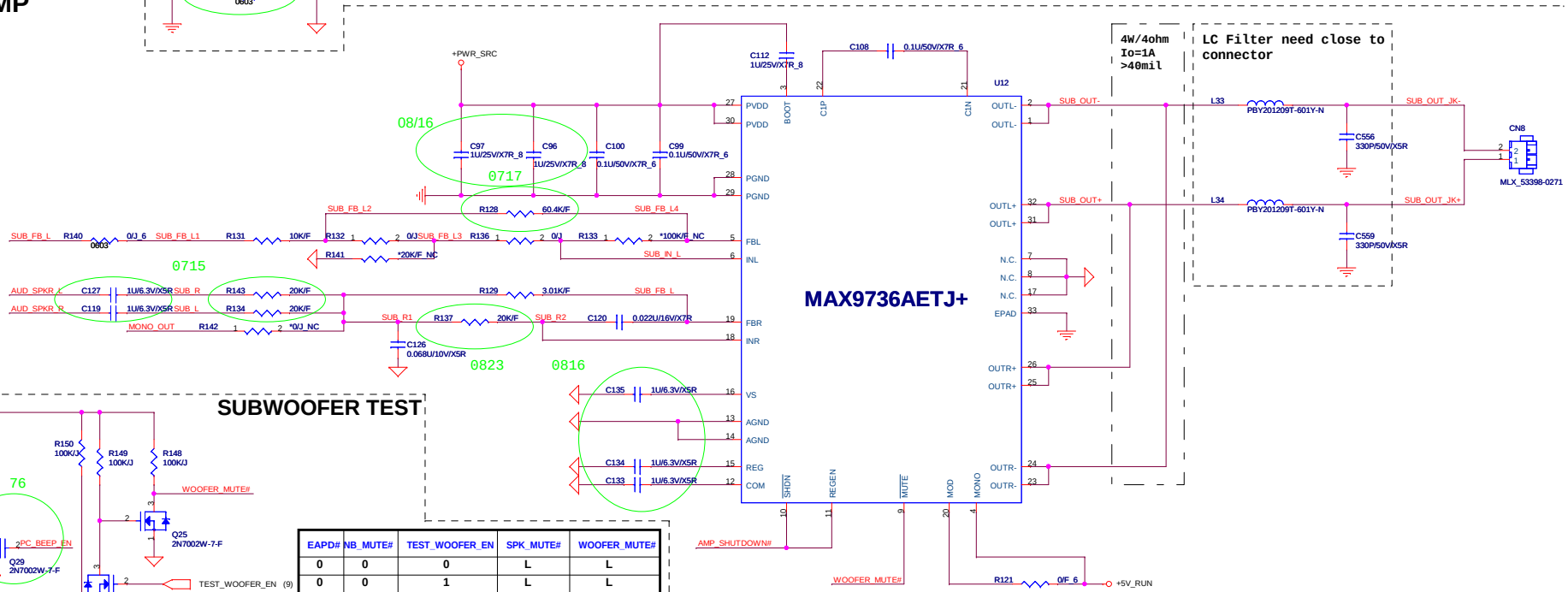

Tied at one point only under the ALC665 or near the ALC665
Need close to ALC665
>20mil
Close to pin 25
U4
ALC665
Analog
Digital
JACK1(HP1)
JACK2(HP2)
JACK3(MIC)
JACK SENSE
SPDIF Control
Reserve for EMI
0826
0823
0817
0715
0820
0816
Quanta Computer Inc.
PROJECT :GM6C MLK DIS
Audio CODEC (ALC665)
Rev 1A
Date: Friday, August 27, 2010
Sheet 36 of 57

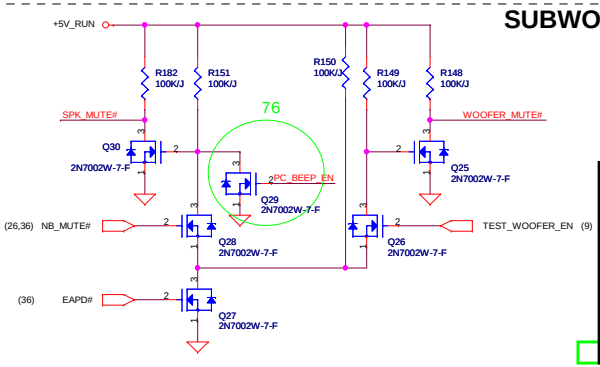
# Main Speaker AMP




# SUBWOOFER AMP




# SUBWOOFER TEST

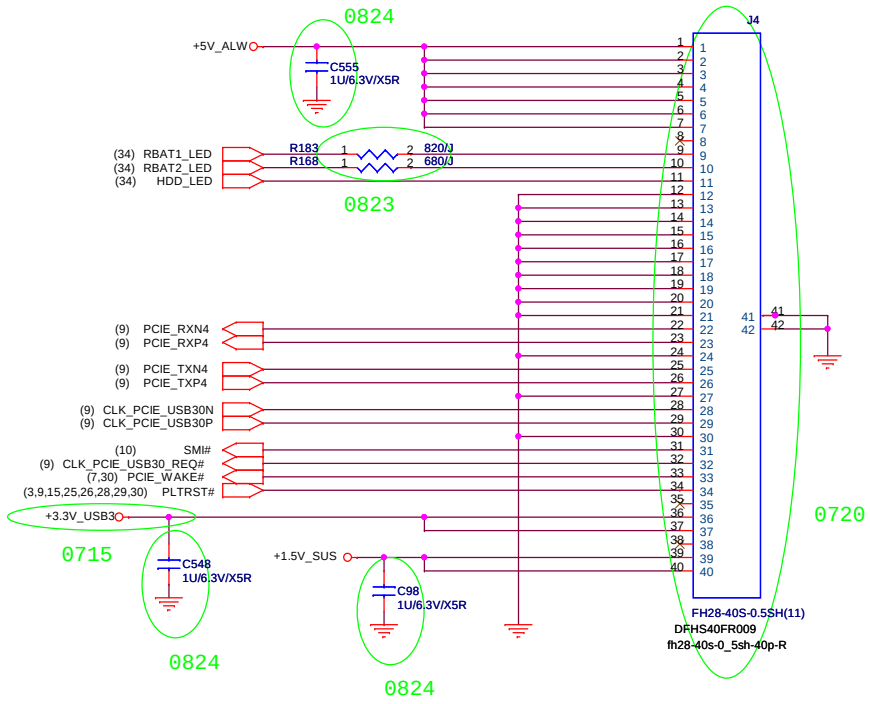


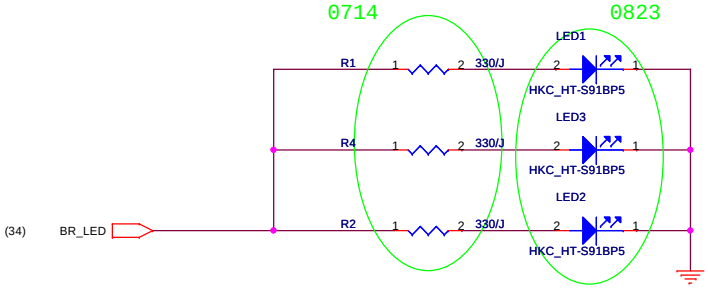

| EAPD# | NB_MUTE# | TEST_WOOFER_EN | SPK_MUTE# | WOOFER_MUTE# |
|---|---|---|---|---|
| 0 | 0 | 0 | L | L |
| 0 | 0 | 1 | L | L |
| 0 | 1 | 0 | L | L |
| 0 | 1 | 1 | L | L |
| 1 | 0 | 0 | L | L |
| 1 | 0 | 1 | L(Disable SPK) | H(Test Woofer) |
| 1 | 1 | 0 | H(Test SPK) | L(Disable Woofer) |
| 1 | 1 | 1 | H | H |

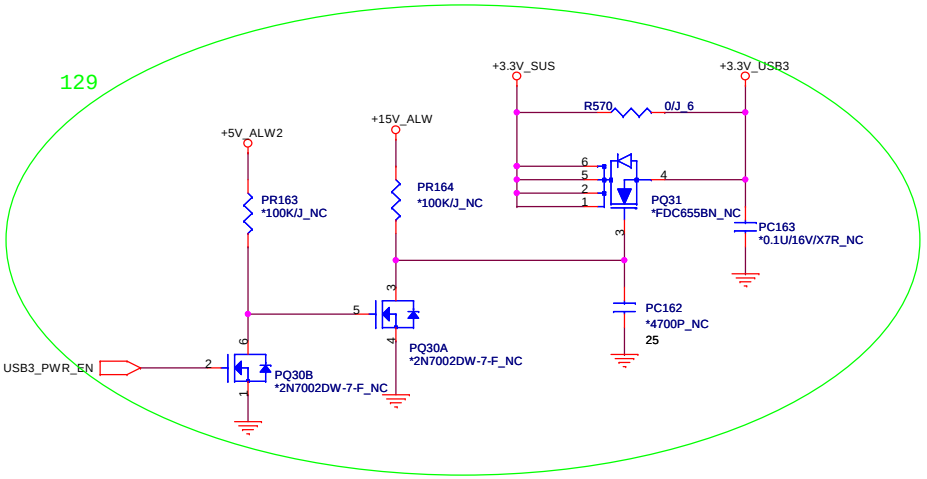
Quanta Computer Inc.

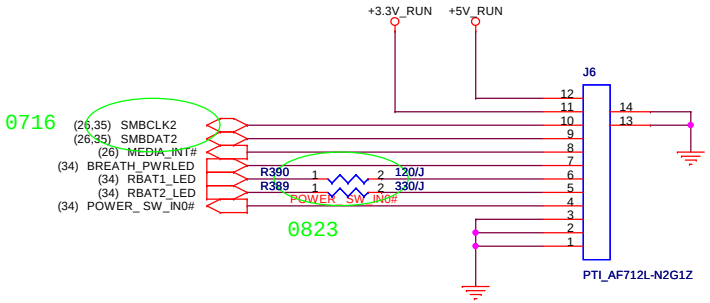
PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | Audio AMP (MAX9736A) | 1A |
| Date: Friday, August 27, 2010 | Sheet 37 of 57 | |




Quanta Computer Inc.

PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | Left USB/MMB CONN | 1A |

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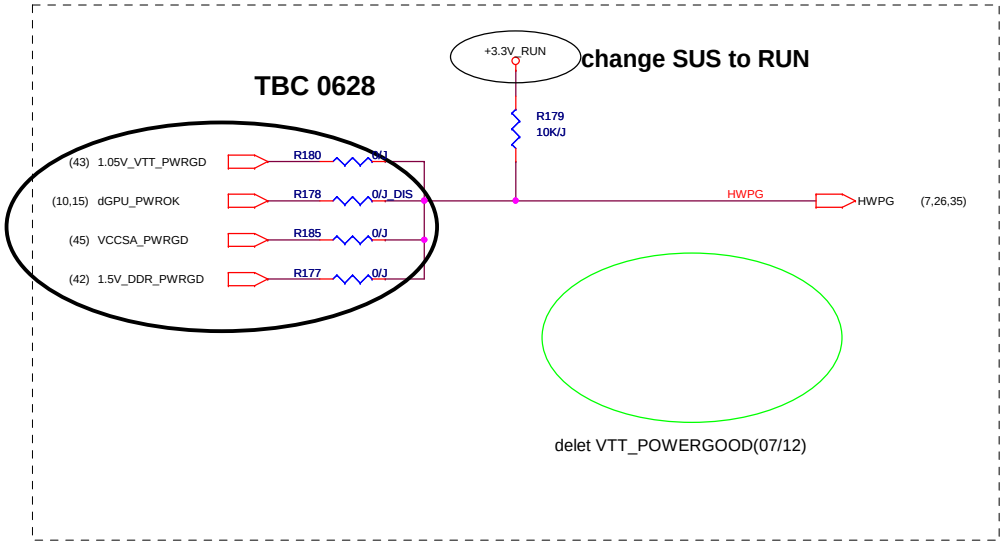
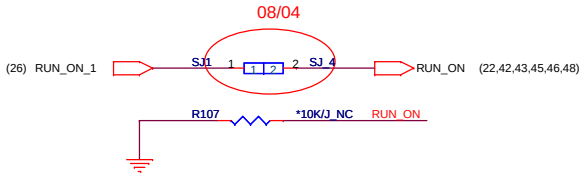
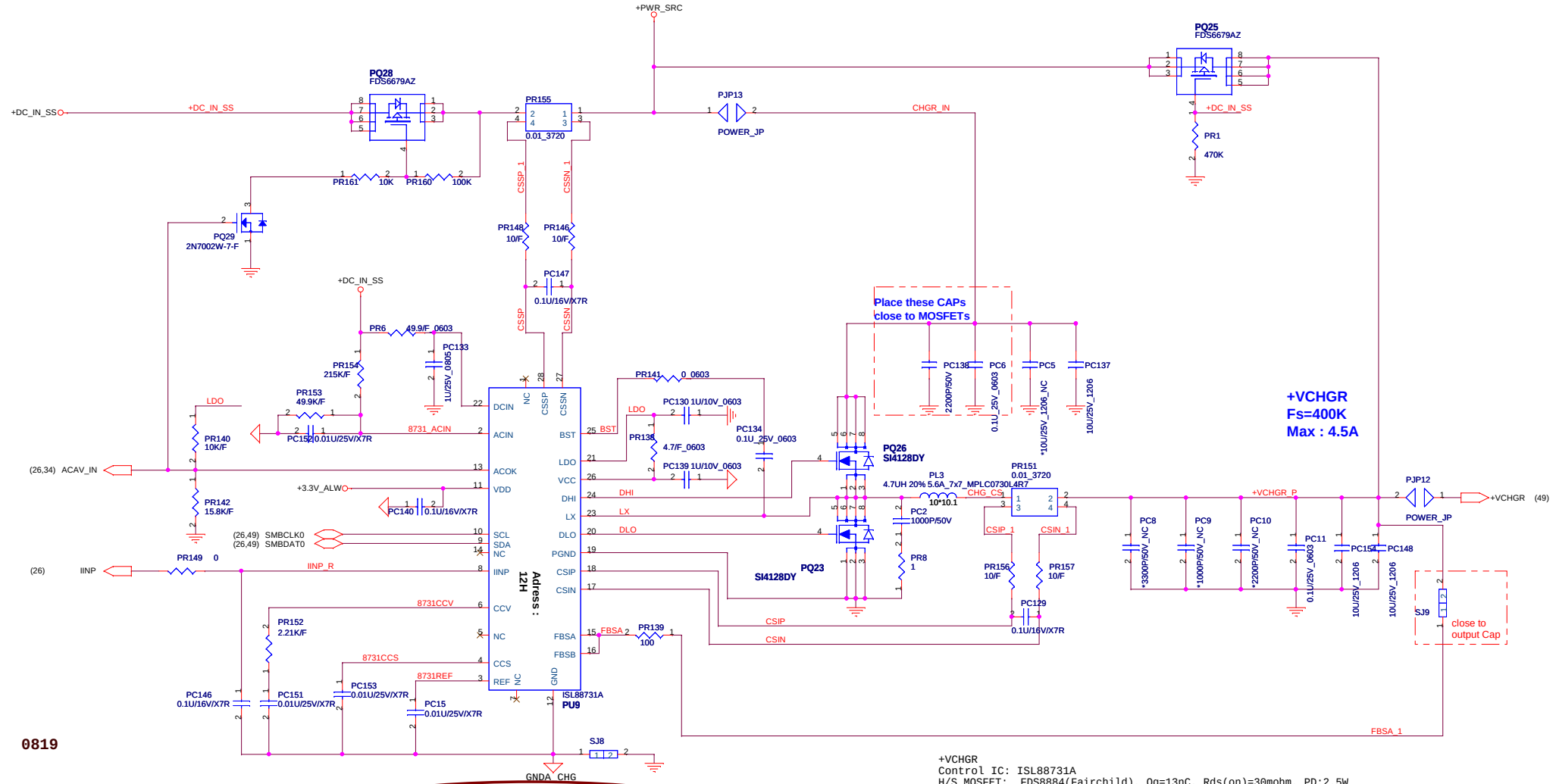



| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : GM6C MLK DIS | | |
| Size | Document Number: System Reset Circuit | Rev: 1A |
| Date: Friday, August 27, 2010 | Sheet 39 of 57 | |

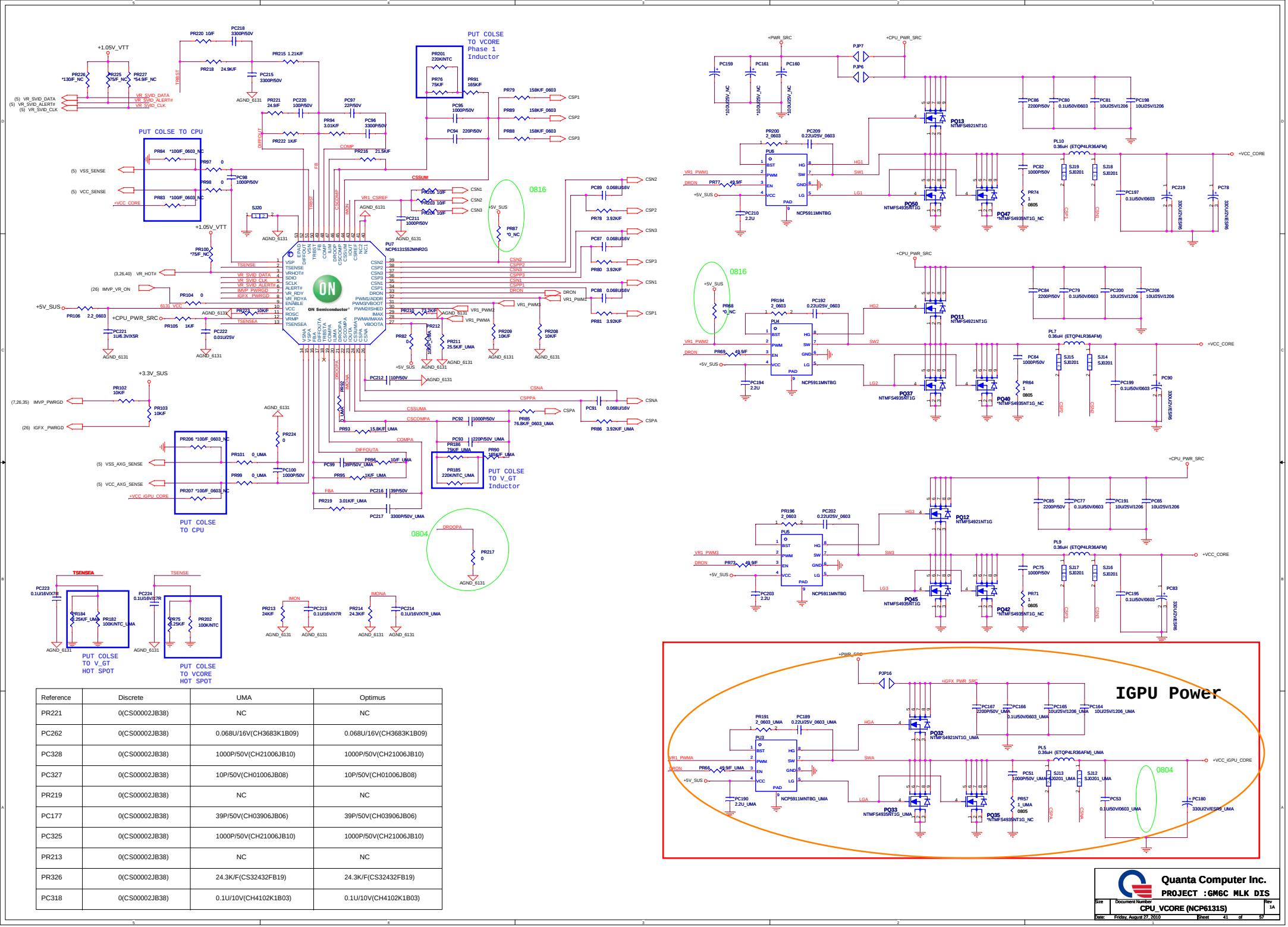



| Adapter type | 90W | 130W |
|---|---|---|
| ADAPT_TRIP_SET | 0 | 1 |

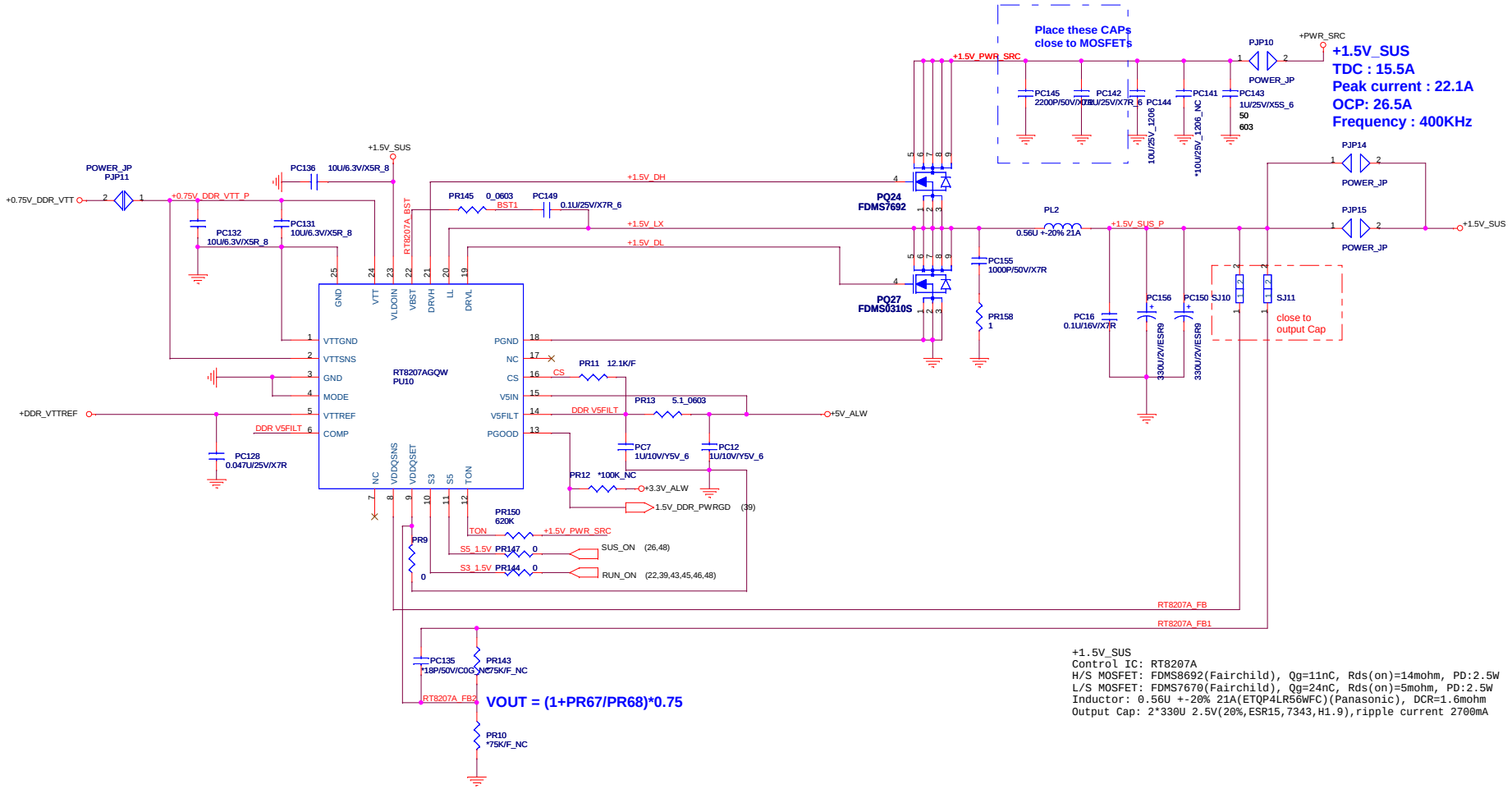
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | Charger (ISL88731) | 1A |
| Date: Friday, August 27, 2010 | Sheet 40 of 57 | |




| Reference | Discrete | UMA | Optimus |
|---|---|---|---|
| PR221 | 0(CS00002JB38) | NC | NC |
| PC262 | 0(CS00002JB38) | 0.068U/16V(CH3683K1B09) | 0.068U/16V(CH3683K1B09) |
| PC328 | 0(CS00002JB38) | 1000P/50V(CH21006JB10) | 1000P/50V(CH21006JB10) |
| PC327 | 0(CS00002JB38) | 10P/50V(CH01006JB08) | 10P/50V(CH01006JB08) |
| PR219 | 0(CS00002JB38) | NC | NC |
| PC177 | 0(CS00002JB38) | 39P/50V(CH03906JB06) | 39P/50V(CH03906JB06) |
| PC325 | 0(CS00002JB38) | 1000P/50V(CH21006JB10) | 1000P/50V(CH21006JB10) |
| PR213 | 0(CS00002JB38) | NC | NC |
| PR326 | 0(CS00002JB38) | 24.3K/F(CS32432FB19) | 24.3K/F(CS32432FB19) |
| PC318 | 0(CS00002JB38) | 0.1U/10V(CH4102K1B03) | 0.1U/10V(CH4102K1B03) |




+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.56U +-20% 21A(ETQP4LR56WFC)(Panasonic), DCR=1.6mohm
Output Cap: 2*330U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

**VDDQ and VTT discharge control**

| MODE pin | Discharge mode |
|---|---|
| V5IN | No discharge |
| VDDQ | Tracking discharge |
| S4/GND | Non-tracking discharge |

**VDDQ output voltage selection**

| VDDQSET | VDDQ(V) | VTTREF and VTT | NOTE |
|---|---|---|---|
| GND | 1.5V | VDDQSNS/2 | DDR3 |
| V5IN | 1.8V | VDDQSNS/2 | DDR2 |
| FB Resistors | Adjusting | VDDQSNS/2 | 1.5V < VVDDQ < 3V |

**Outputs Management by S3, S5 control**

| State | S3 | S5 | VDDQ | VTTREF | VTT |
|---|---|---|---|---|---|
| S0 | HI | HI | On | On | On |
| S3 | LO | HI | On | On | Off (Hi-Z) |
| S4/S5 | LO | LO | On (discharge) | Off (discharge) | Off (discharge) |

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | 1.5V_SUS & 0.75_DDR_VTT (RT8207) | 1A |

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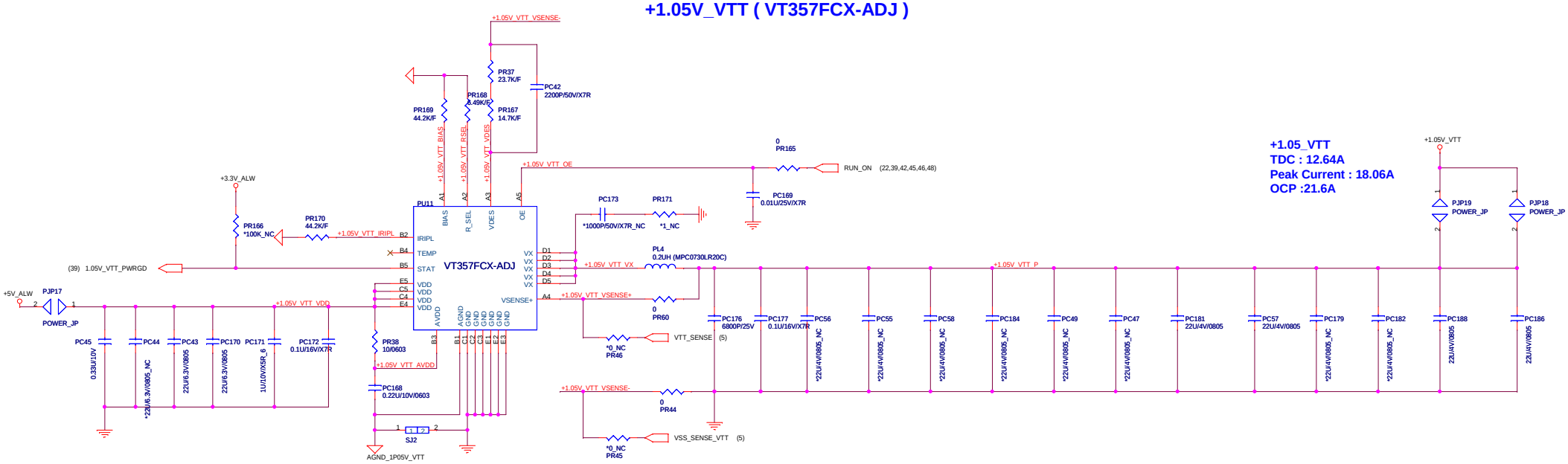
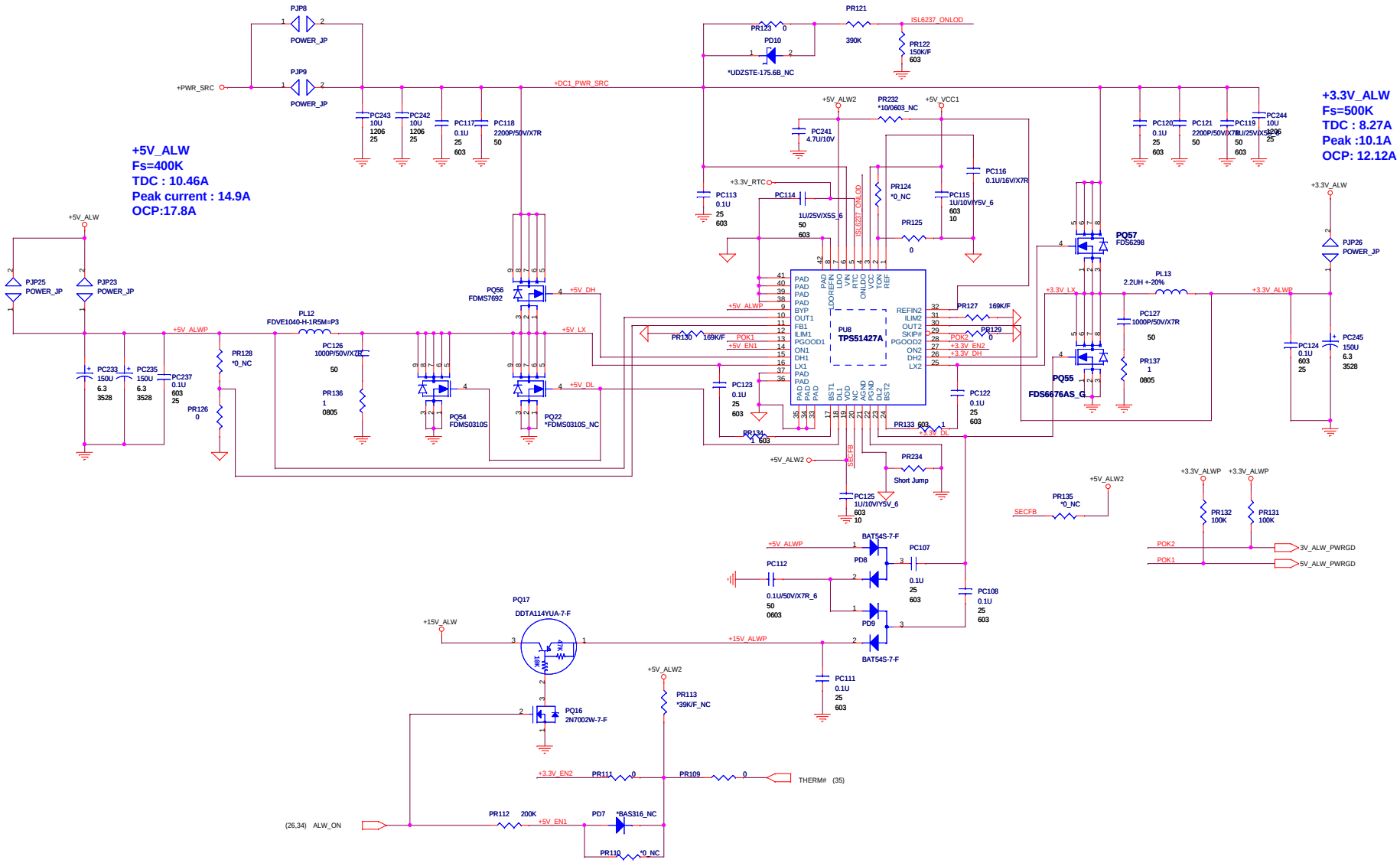
# +1.05V_VTT ( VT357FCX-ADJ )



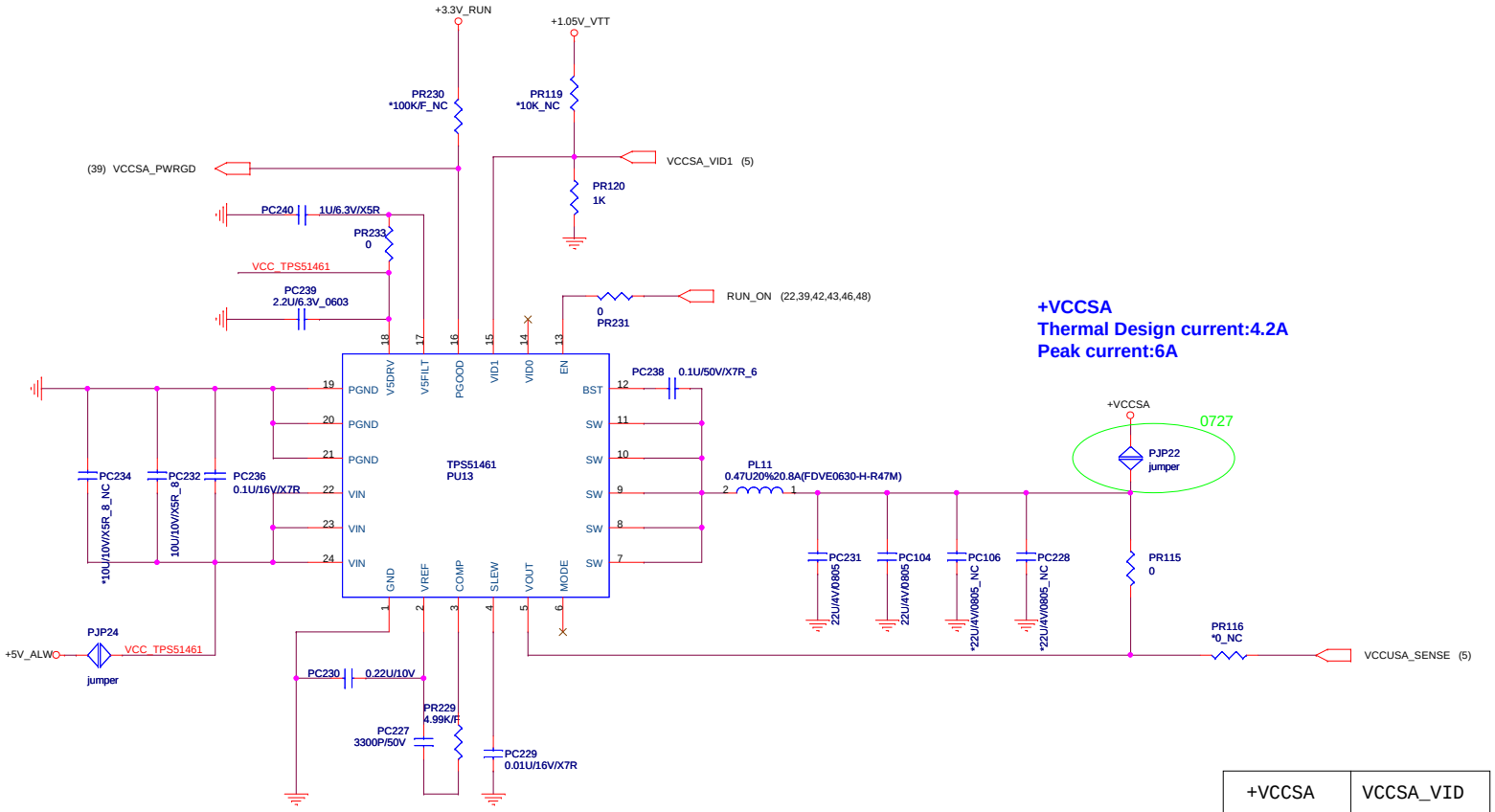

**+1.05_VTT**
**TDC : 12.64A**
**Peak Current : 18.06A**
**OCP :21.6A**

Route +1.05V_VTT_VSENSE+ and +1.05V_VTT_VSENSE- as differential pair

| | | | |
|---|---|---|---|
| Quanta Computer Inc. | | | |
| PROJECT : GM6C MLK DIS | | | |
| Size | Document Number | | Rev |
| | 1.05V_VTT | | 1A |
| Date: Friday, August 27, 2010 | | Sheet 43 of 57 | |




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : GM6C MLK DIS | | |
| Size | Document Number: 3.3V_ALW / 5V_ALW(TPS51427A) | Rev: 1A |
| Date: Friday, August 27, 2010 | Sheet 44 of 57 | |




| +VCCSA | VCCSA_VID |
|---|---|
| 0.8V | High |
| 0.9V | Low |

Quanta Computer Inc.
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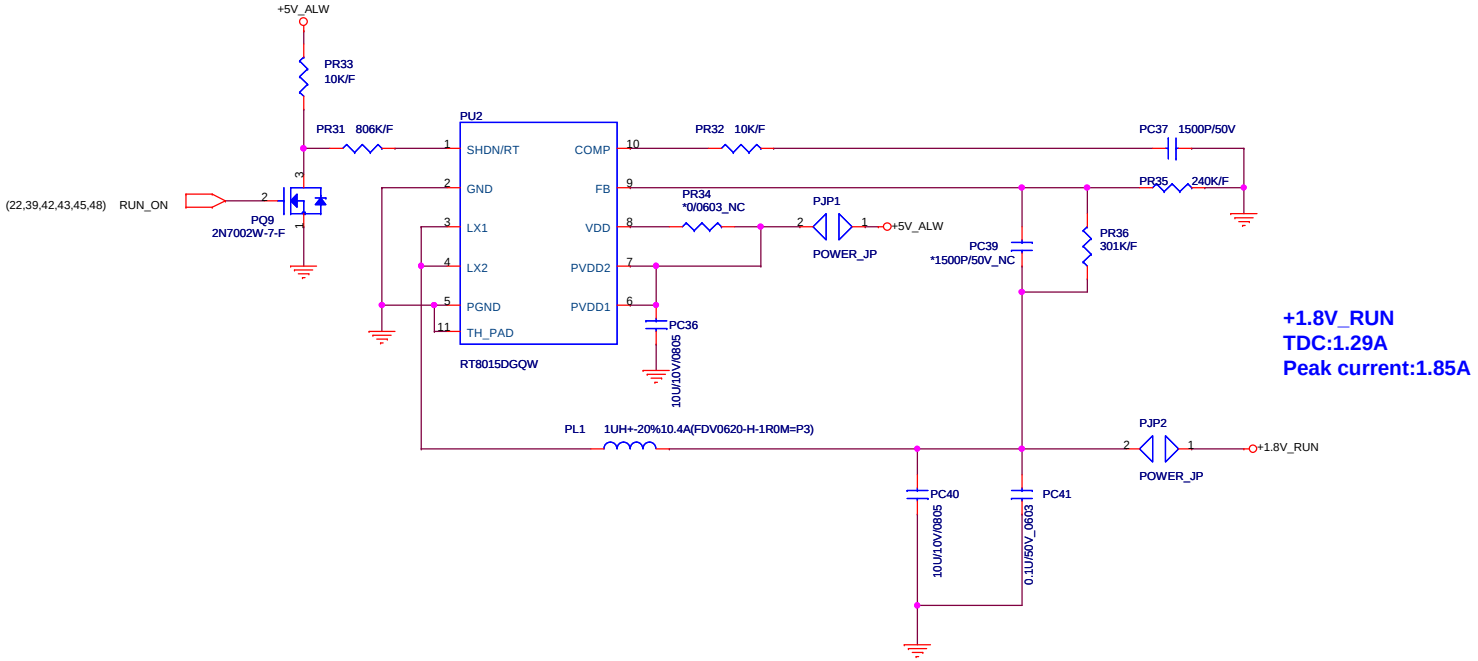
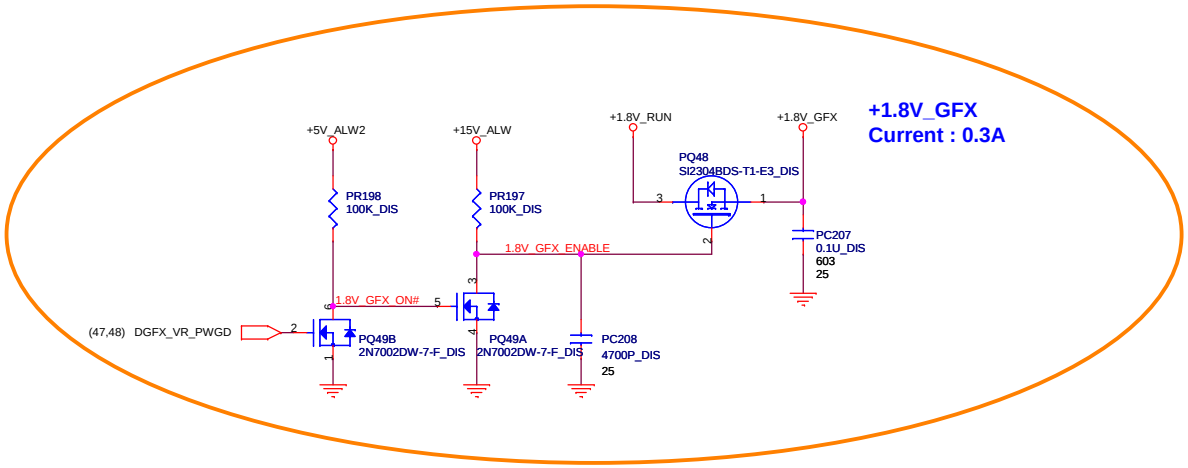
| Size | Document Number | Rev |
|---|---|---|
| | VCCSA (TPS51461) | 1A |
| Date: Friday, August 27, 2010 | Sheet 45 of 57 | |




**+1.8V_RUN**
**TDC:1.29A**
**Peak current:1.85A**




**+1.8V_GFX**
**Current : 0.3A**

**Quanta Computer Inc.**
**PROJECT : GM6C MLK DIS**

| Size | Document Number | Rev |
|---|---|---|
| | 1.8V_RUN & 1.8V_RUN_GFX | 1A |
| Date: Friday, August 27, 2010 | Sheet 46 of 57 | |

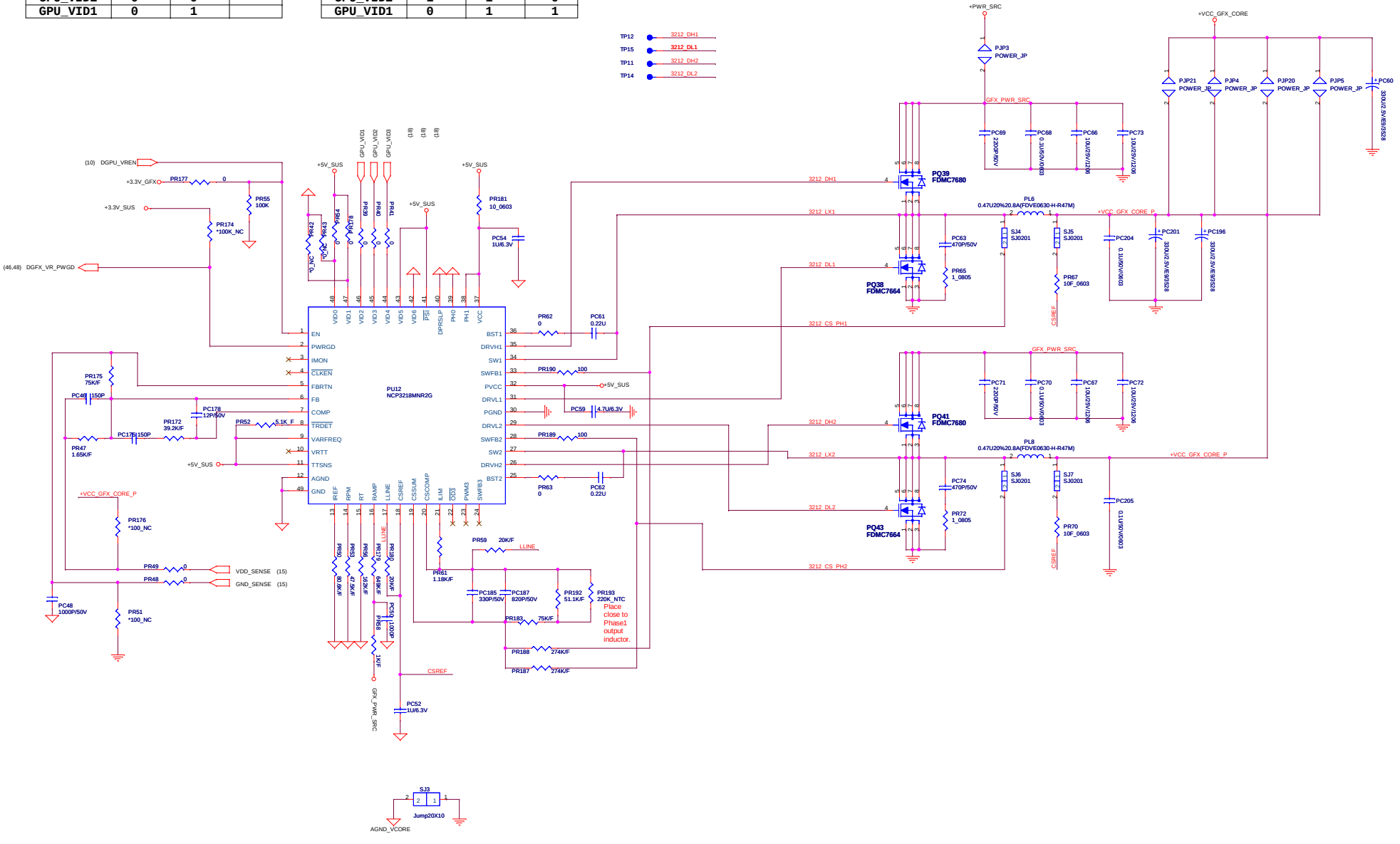
**N12P-GT:**

| | 1.075V | 0.825V | |
|---|---|---|---|
| GPU_VID3 | 0 | 1 | |
| GPU_VID2 | 0 | 0 | |
| GPU_VID1 | 0 | 1 | |

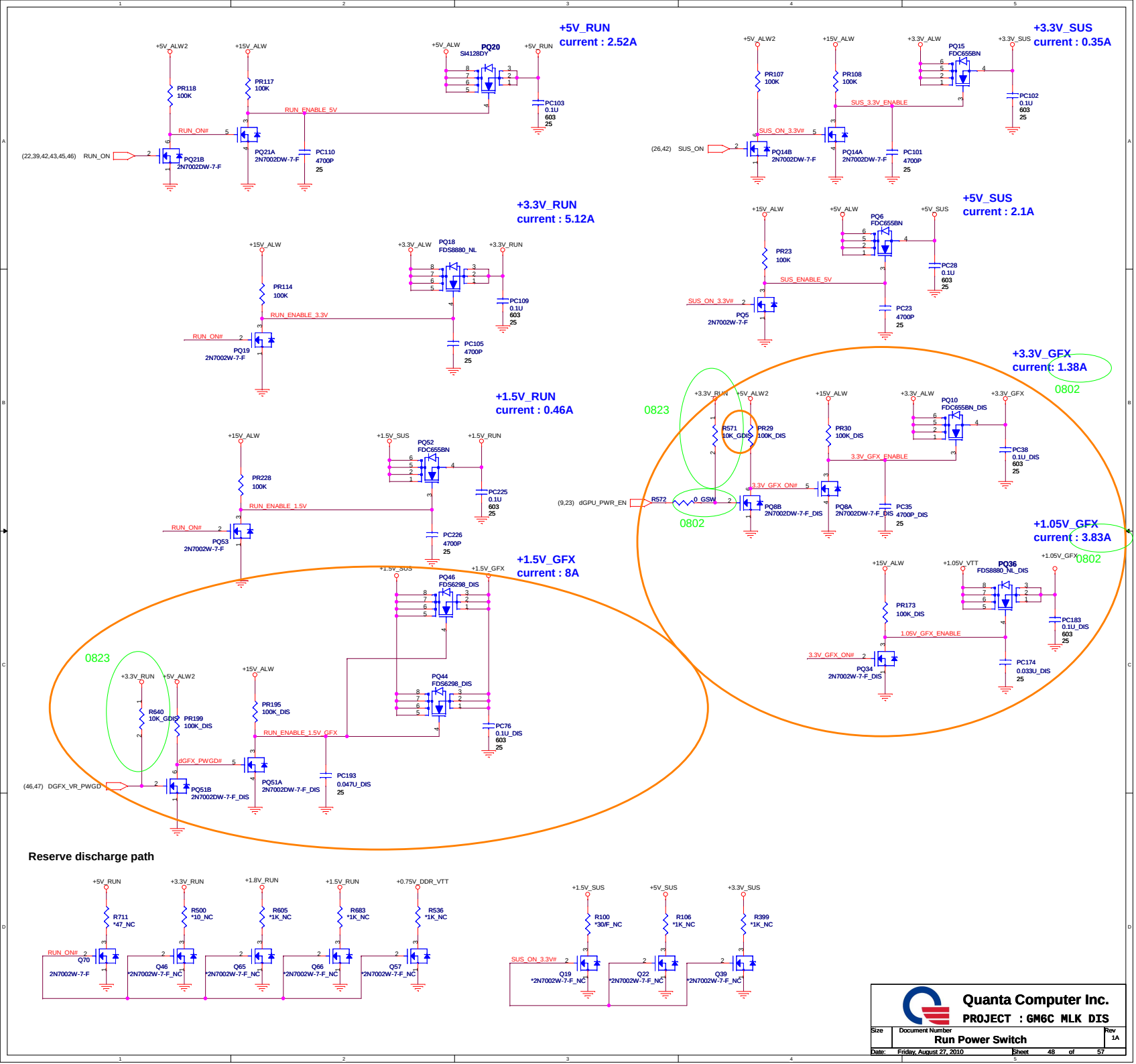
**N12P-GE:**

| | 0.975V | 0.95V | 0.85V |
|---|---|---|---|
| GPU_VID3 | 0 | 0 | 1 |
| GPU_VID2 | 1 | 1 | 0 |
| GPU_VID1 | 0 | 1 | 1 |

**+VCC_GFX_CORE**
**Fs=300K**
**Current:37.84A**
**OCP:45.4A**



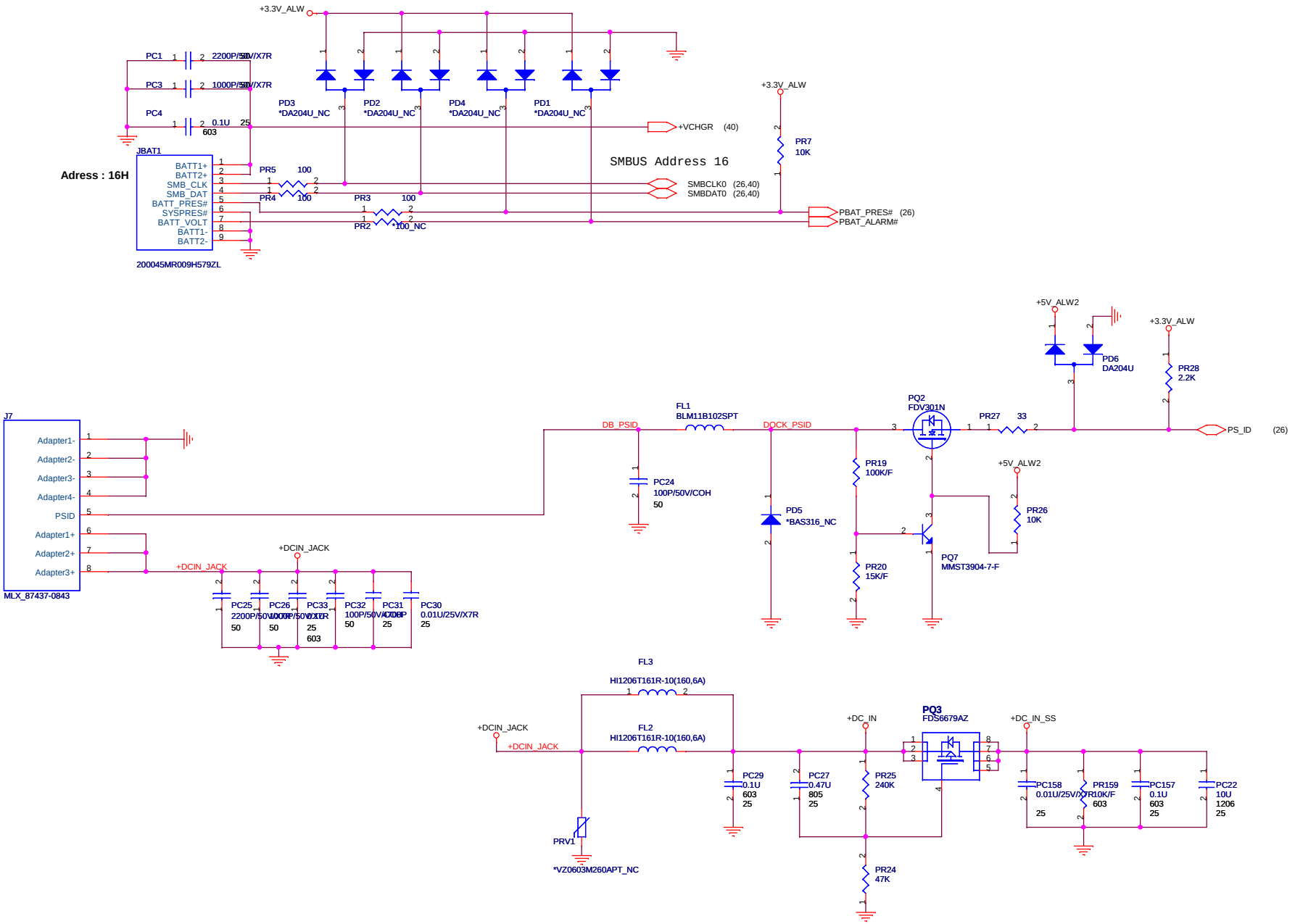

| | |
|---|---|
| Quanta Computer Inc. | |
| PROJECT : GM6C MLK DIS | |
| Size | Document Number: VGA_N11P-dGFX (NCP3218MNR2G) Rev: 1A |
| Date: Friday, August 27, 2010 | Sheet 47 of 57 |




Quanta Computer Inc.

PROJECT : GM6C MLK DIS

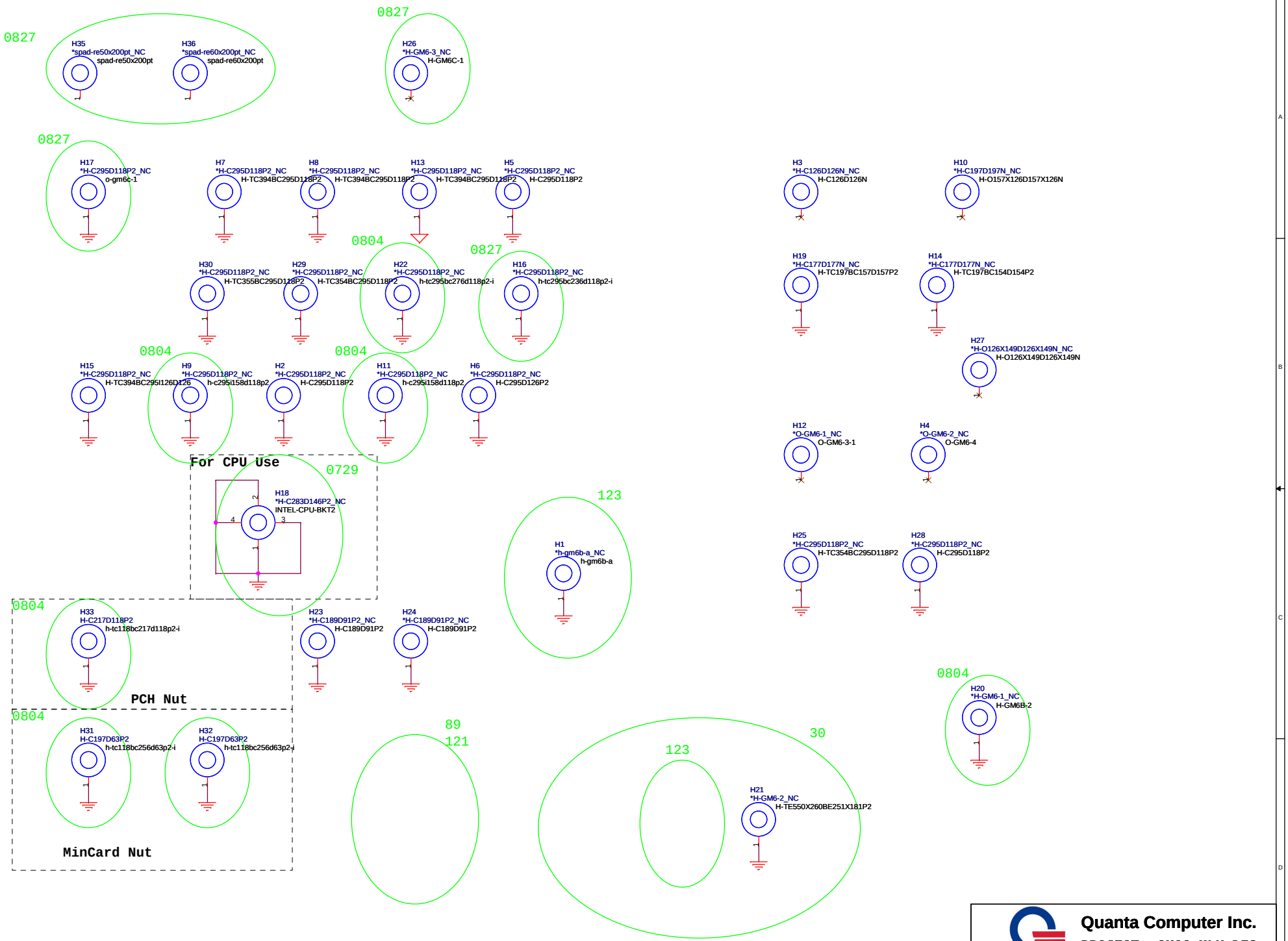
| Size | Document Number | Rev |
|---|---|---|
| | Run Power Switch | 1A |
| Date: Friday, August 27, 2010 | Sheet 48 of 57 | |




Quanta Computer Inc.

PROJECT : GM6C MLK DIS

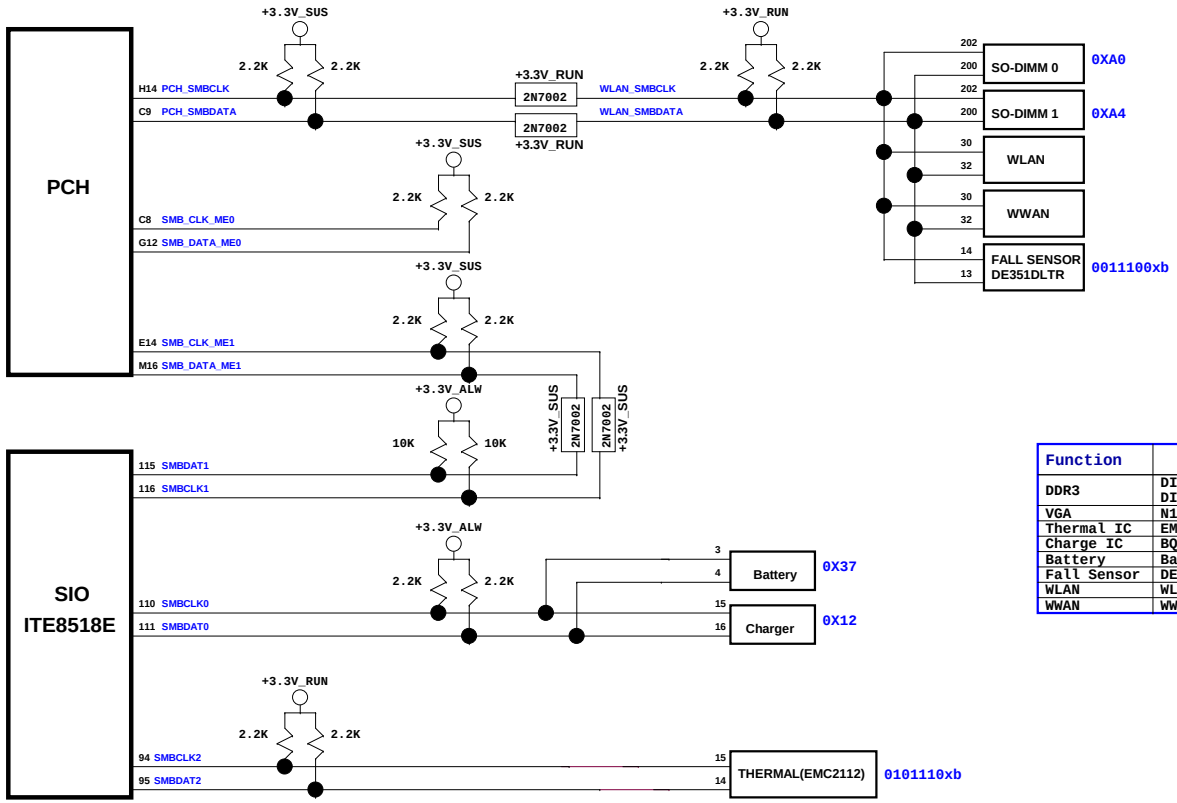
| Size | Document Number | Rev |
|---|---|---|
| | DCIN&BATT | 1A |
| Date: Friday, August 27, 2010 | Sheet 49 of 57 | |




Quanta Computer Inc.

PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | PAD & SCREW | 1A |
| Date: Friday, August 27, 2010 | Sheet 50 of 57 | |




| Function | IC | SMBus Address |
|---|---|---|
| DDR3 | DIMM0<br>DIMM1 | A0<br>A4 |
| VGA | N11P | 9E |
| Thermal IC | EMC2112 | 0011100xb |
| Charge IC | BQ24765RUVR | 0x12 |
| Battery | Battery | 0X37 |
| Fall Sensor | DE351DLTR | 0101110xb |
| WLAN | WLAN Module | X |
| WWAN | WWAN Module | X |

Quanta Computer Inc.
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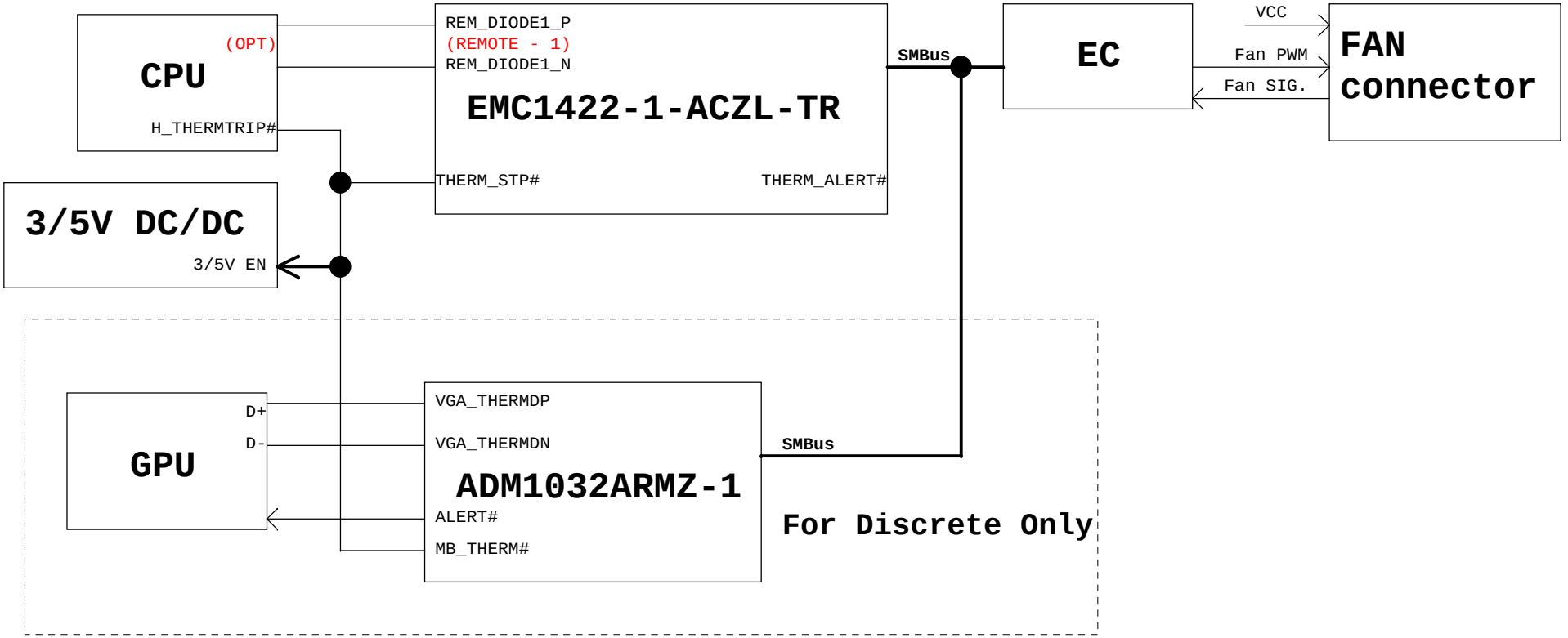
Size | Document Number: SMBUS | Rev 1A
Date: Friday, August 27, 2010 | Sheet 51 of 57




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : GM6C MLK DIS | | |
| Size | Document Number: THERMAL MAP | Rev: 1A |
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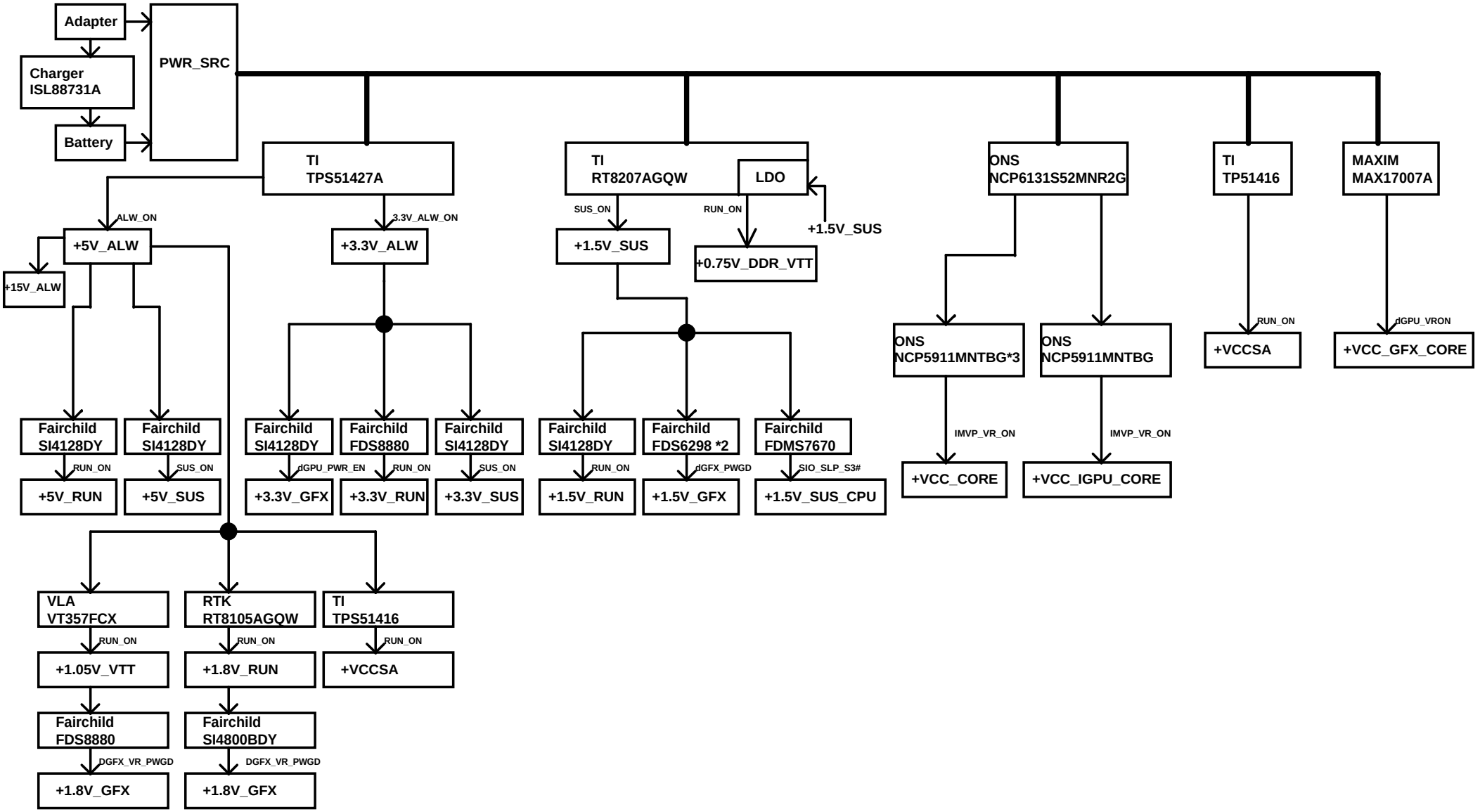
VER : 1A




Quanta Computer Inc.

PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | Power Block Diagram | 1A |

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# UM6C-MLK Power Design Block Diagram

**OPTIMUS UMA DIS**

| | | | |
|---|---|---|---|
| (1) | (1) | (1) | AC : DC_IN -> DC_IN_SS -> +PWR_SRC<br>Bat : +VCHGR -> +PWR_SRC,+5V_ALW2, |
| (2) | (2) | (2) | SYS_PWR_SW# |
| (3) | (3) | (3) | 3.3V_ALW_ON |
| (4) | (4) | (4) | 3.3V_ALW |
| (5) | (5) | (5) | ALW_ON |
| (6) | (6) | (6) | +5V_ALW,+15V_ALW |
| (7) | (7) | (7) | SUS_ON |
| (8) | (8) | (8) | +5V_SUS,+3V_SUS |
| (9) | (9) | (9) | +1.5V_SUS |
| (10) | (10) | (10) | 1.5V_DDR_PWRGD |
| (11) | (11) | (11) | RSMRST# |
| (12) | (12) | (12) | AC_PRESENT |
| (13) | (13) | (13) | SIO_PWRBTN# |
| (14) | (14) | (14) | SIO_SLP_S5# |
| (15) | (15) | (15) | SIO_SLP_S3# |
| (16) | (16) | (16) | +1.5V_SUS_CPU |
| (17) | (17) | (17) | RUN_ON |
| (18) | (18) | (18) | +0.75V_DDR_VTT,+5V_RUN,+3.3V_RUN,+1.5V_RUN |
| (19) | (19) | (19) | +1.8V_RUN |
| (20) | (20) | (20) | +1.05V_VTT,+1.05V_VTT_PWRGD |
| (21) | (21) | (21) | +VCCSA,VCCSA_PWRGD |
| (22) | | (22) | dGPU_PWR_EN |
| (23) | | (23) | +3.3V_GFX, +1.05V_GFX |
| (24) | | (24) | +VCC_GFX_CORE |
| (25) | | (25) | DGFX_VR_PWGD |
| (26) | | (26) | +1.8V_GFX, +1.5V_GFX |
| (27) | (20) | (27) | dGPU_PWROK |
| (28) | | (28) | HWPG |
| (29) | (22) | (29) | IMVP_VR_ON |
| (30) | (23) | (30) | +VCC_CORE, +VCC_iGPU_CORE |
| (31) | (24) | (31) | EC_PWROK |
| (32) | (25) | (32) | SYS_PWROK |
| (33) | (26) | (33) | PM_DRAM_PWRGD |
| (34) | (27) | (34) | CLK_CPU_BCLKN, CLK_CPU_BCLKP |
| (35) | (28) | (35) | H_PWRGOOD |
| (36) | (29) | (36) | PLTRST#(PCI_PLTRST#) |

Power Jack
Adapter input
+DC_IN_SS
FDS6679
+PWR_SRC
Charger
ISL88731
Page 40
+VCHGR
Battery
FDS6679
+PWR_SRC

+5V_VCC1 (from +5V_ALW2 for Max so;ution) for TI solution, IC can supply 5V by itself.
SYSTEM POWER
TPS51427A
Page 44
LDO
VR
+5V_ALW2
+3.3V_ALW
+5V_ALW
+3.3V_ALW_ON(From 3V_ALW ON POWER LOGIC)
ALW_ON(For +5V_ALW and turn on +15V_ALW)
3V_ALW_PWRGD
5V_ALW_PWRGD

VRAM DDR3 POWER
RT8207AGQW
Page 42
+5V_ALW
SUS_ON
RUN_ON
VR
LDO
+1.5V_SUS
1.5V_DDR_PWRGD
+0.75V_DDR_VTT

Diode & Cap
Page 44
+5V_ALW
+15V_ALW
ALW_ON

SI4128DY
Page 48
+5V_ALW
+5V_SUS
SUS_ON

SI4128DY
Page 48
+3.3V_ALW
+3.3V_SUS
SUS_ON

FDMS7670
Page 48
+1.5V_SUS
+1.5V_SUS_CPU
SIO_SLP_S3#

VCCPLL POWER
RT8105AGQW
Page 46
+5V_ALW
RUN_ON
VR
+1.8V_RUN

CPU Memory Control & I/O Power
VT357
Page 43
+5V_ALW
RUN_ON
VR
+1.05V_VTT
+1.05V_VTT_PWRGD

VccSA POWER
TPS51416
Page 45
+5V_ALW
RUN_ON
VR
+VCCSA
VCCSA_PWRGD

SI4128DY
Page 48
+5V_ALW
+5V_RUN
RUN_ON

FDS8880
Page 48
+3.3V_ALW
+3.3V_RUN
RUN_ON

SI4128DY
Page 48
+1.5V_SUS
+1.5V_RUN
RUN_ON

SI4128DY
Page 48
+3.3V_ALW
+3.3V_GFX
dGPU_PWR_EN

FDS6298 x 2
Page 48
+1.5V_SUS
+1.5V_GFX
dGFX_PWGD

FDS8880
Page 48
+1.05V_VTT
+1.05V_GFX
dGPU_PWR_EN

SI4800BDY
Page 46
+1.8V_RUN
+1.8V_GFX
DGFX_VR_PWGD

GRAPHY CORE POWER
MAX17007A
Page 47
+5V_SUS
+3.3V_GFX
VR
+VCC_GFX_CORE

NCP5911MNTBG
Page 41
IMVP_VR_ON
VR
+VCC_CORE

NCP5911MNTBG
Page 41
IMVP_VR_ON
VR
+VCC_iGPU_CORE

SYS_PWR_SW#

EC
IT8512
Page 26
ALW_ON
SUS_ON
RSMRST#
AC_PRESENT
SIO_PWRBTN#
SIO_SLP_S5#
SIO_SLP_S3#
HWPG
RUN_ON_1
IMVP_VR_ON
EC_PWROK

PCH
Page 7~12
DGFX_VR_PWGD
SYS_PWROK
dGPU_PWROK
PM_DRAM_PWRGD
CLK_CPU_BCLKN
CLK_CPU_BCLKP
H_PWRGOOD
PLTRST#(PCI_PLTRST#)

CPU
Page 3~6

25MHz(x'tal)

Reset Circuit
Page 39
Inverter
short jump
Wire AND
Page 39
RUN_ON_1
RUN_ON
1.05V_VTT_PWRGD
DGFX_VR_PWGD
VCCSA_PWRGD
1.5V_DDR_PWRGD
HWPG

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size
Document Number
Power sequence Block
Rev 1A
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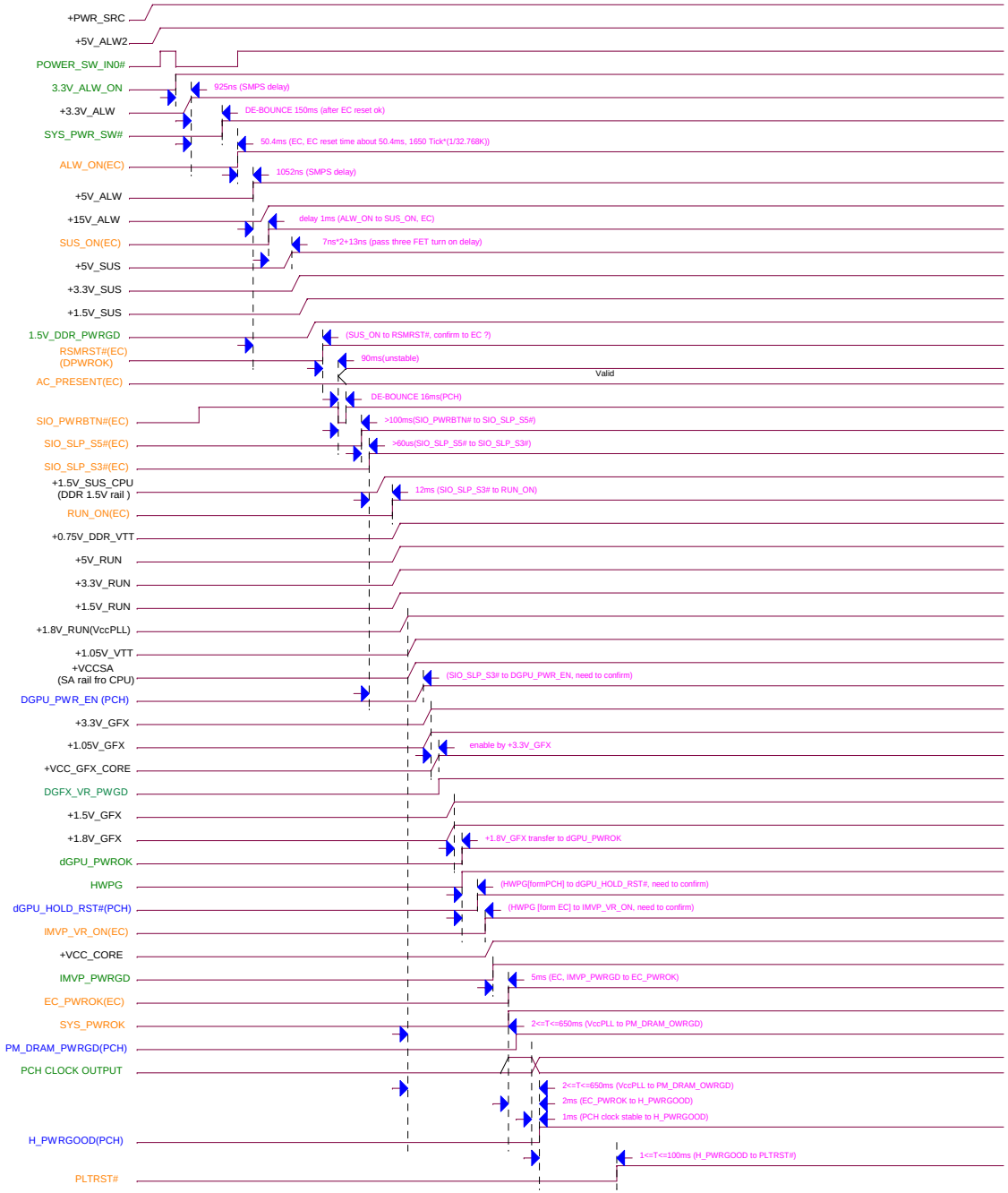
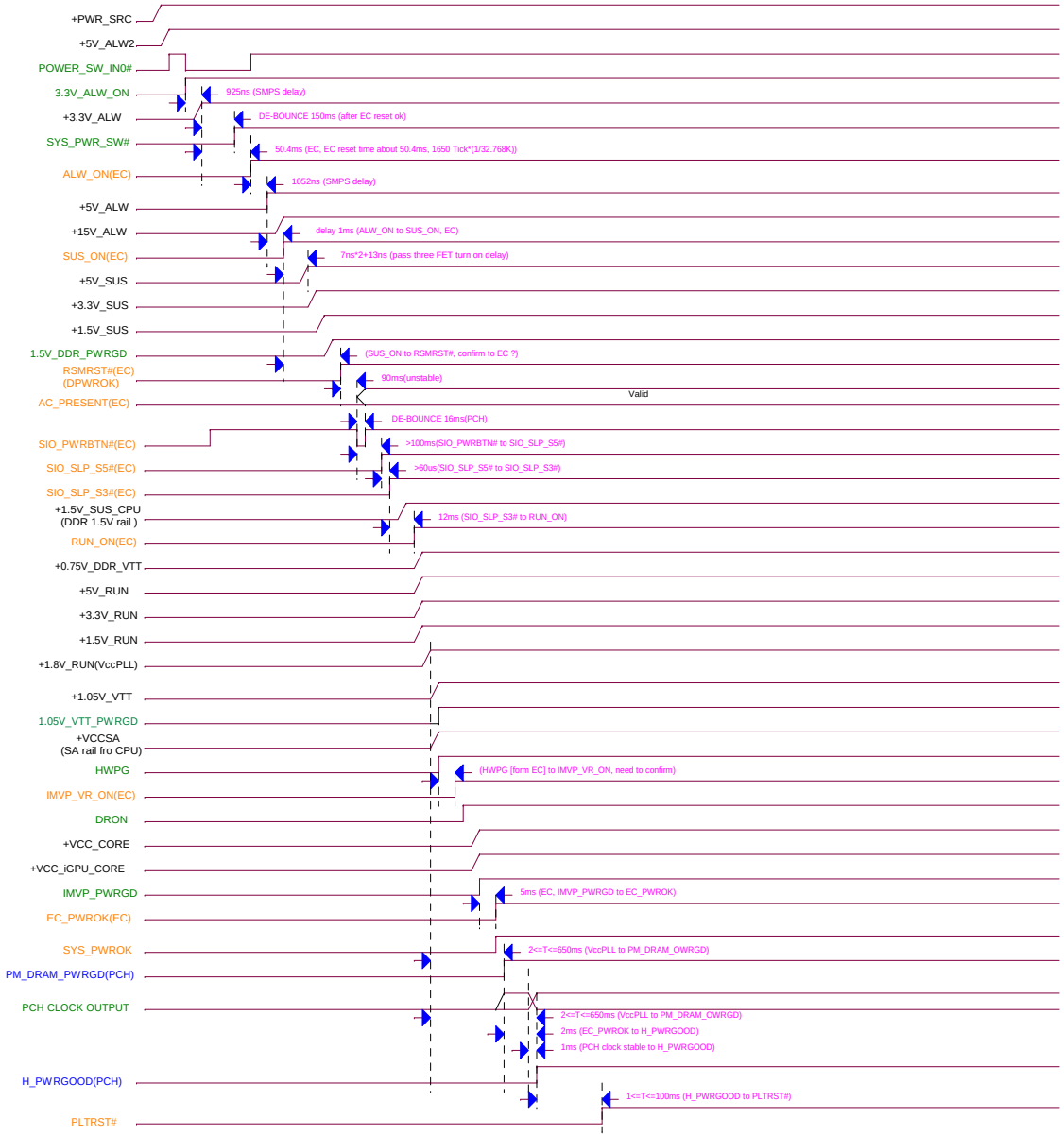
# UM6B_MLK_DIS Power on Timing(BATTERY MODE)



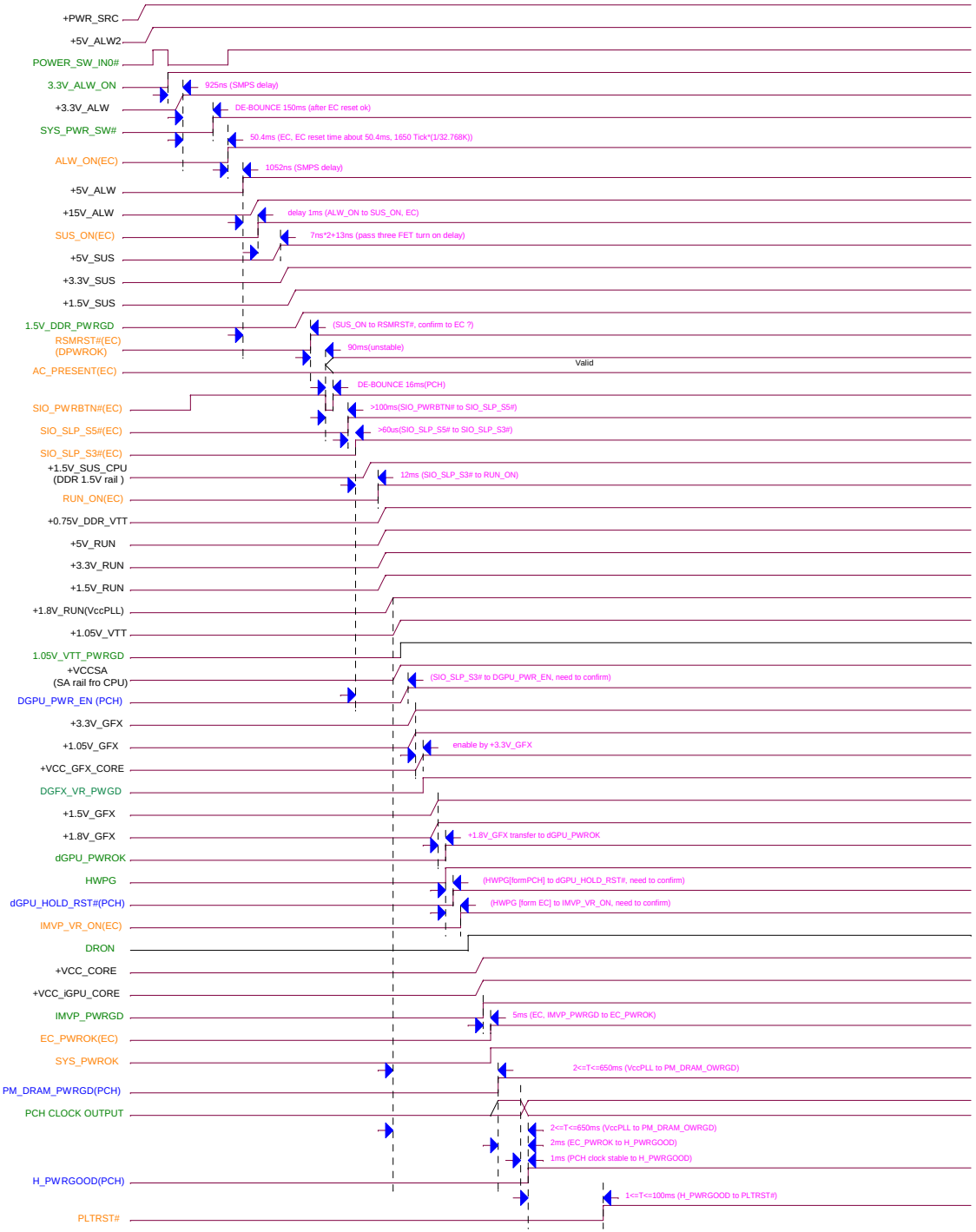

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : GM6C MLK DIS | | |
| Size | Document Number: POWER SEQUENCE | Rev: 1A |
| Date: Friday, August 27, 2010 | Sheet 55 of 57 | |

# UM6B_MLK_UMA Power on Timing(BATTERY MODE)




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : GM6C MLK DIS | | |
| Size | Document Number: POWER SEQUENCE | Rev 1A |
| Date: Friday, August 27, 2010 | Sheet 56 of 57 | |

# UM6B_MLK_OPTIMUS Power on Timing(BATTERY MODE)




Quanta Computer Inc.
PROJECT : GM6C MLK DIS

| Size | Document Number | Rev |
|---|---|---|
| | POWER SEQUENCE | 1A |

Date: Friday, August 27, 2010 Sheet 57 of 57