CASPER Memo 13: XAUI Transmission Error Rates on the BEE2

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1 Introduction

The goal of the Center for Astronomy Signal Processing and Electronics Research (CASPER) group at the University of California, Berkeley, is to develop general-purpose hardware and signal processing algorithms to meet the growing demand for processing power in the astronomy community. To this end, CASPER relies on general-purpose Field-Programmable Gate Array (FPGA)-based processing boards connected by common interfaces using industry-standard protocols.

Interboard communication within the CASPER framework relies largely on the X Attachment Unit Interface (XAUI) protocol as defined by the IEEE 802.3ae 10GbE specification. This protocol is used both as a lightweight point-to-point transmission interface, and as the physical layer for 10 Gigabit Ethernet packetized communication. It is vital, therefore, to quantify the error rate of these communication links between the boards that are used by CASPER for data processing.

Currently, CASPER has at its disposal two processing boards which tie CX4 connectors (capable of transmitting the XAUI protocol) to FPGAs. The first of these, the Internet BreakOut Board (IBOB) attaches two CX4 connectors to one Xilinx Virtex 2 Pro 50 FPGA. Currently, this board is configured to transmit XAUI over its ports using a preemphasis setting of 3 and a swing of 800, as defined by Xilinx Memos DS083 [2] and UG024 [1]. These parameters are designed to compensate for cable loss and filtering on the transmission side to achieve a reliable waveform on the receive side. The other board currently used in CASPER systems is the Berkeley Emulation Engine 2 (BEE2) board, which attaches four CX4 connectors to each of four Xilinx Virtex 2 Pro 70 FPGAs on the board, and two CX4 connectors to the final fifth FPGA. This system is also configured to use a premphasis of 3 and swing of 800, but because this board has longer traces between the FPGA and its CX4 connectors, this board is expected to have a different performance than the IBOB board.

Anecdotally, IBOB to BEE2 communication and BEE2 to BEE2 communication have been shown to be reliable with low error rates. However, IBOB to IBOB communication has been less reliable. An explanation for this is that the preemphasis and swing values (which are set to the maximum) may be overdriving the signal for the shorter its shorter traces from FPGA to CX4. This theory remains to be tested.

2 Test Setup

This test was performed on a BEE2 board, revision 2.1, connecting ports 0 through 3 of FPGA 2 to 0 through 3 of FPGA 3 via 3 meter CX4 cables. Ports 0 and 1 used the black Fujitsu cables, and ports 2 and 3 used the blue Gore cables. Transmission in each direction occurred at the full line rate of 10 Gb/s (3.125 GHz $\times$ 4 lanes) Transmission data for a cable was generated using a Linear Feedback Shift Register (LFSR) Core provided by Xilinx. An identical LFSR was used on the receive side to check the validity of the transmission. An out-of-band signal was used to synchronize the two LFSRs. To verify that errors would be accurately identified, we inserted a run-time programmable bit-flip between the LFSR and the XAUI transmission module, and verified that each bit-flip we inserted was detected as an error on the receive side.

3 Results

Over a period of 16 hours, 573,123 Gb of data were transmitted and received on each data link. During this time, no errors were detected. This produces an estimated bit-error rate of:

$$R = \frac{1}{(8\ links) \times 5.7 \cdot 10^{14}} = 2.2 \cdot 10^{-16} \frac{errors}{s}$$

References

[1] RocketIO Tranceiver User Guide (UG024 V2.5). Xilinx user guide, http://www.xilinx.com, December 2004.

[2] Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (DS083-2 V4.5). Xilinx data sheet, http://www.xilinx.com, October 2005.