

# Characterization of 5Gsp/s ADC Demux 1:2 Board

Homin Jiang<sup>a</sup>, Howard Liu<sup>a</sup>, Kim Guzzino<sup>a</sup>, Derek Kubo<sup>a</sup>, CT Li<sup>a</sup>, Kevin Lo<sup>a</sup>, Ray Chang<sup>a</sup>, Arthur Tsai<sup>b</sup>

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## I. INTRODUCTION

ASIAA, the Academia Sinica Institute of Astronomy and Astrophysics, has developed a 5 Giga sample per second (5Gsp/s) Analog to Digital (ADC) Printed Circuit Board (PCB) for the CASPER[1] community by employing an e2v's EV8AQ160 ADC chip[1]. Analog data from the sky, passes thru the balun filters, and is digitalized by the chip, then the ADC board outputs the digitized data to the ROACH1 or ROACH2[1] board via the Z-DOK connector, that is the standard process using the CASPER toolflow.

At the time of ADC board development, only ROACH 1 was available. The maximum allowed global clock frequency of ROACH 1 is 450MHz, which is the limitation of ROACH board. With the 450MHz limitation, the ADC clock can be driven to 1.8GHz only. To break thru the limitation, we made the other version of PCB which is called Demux 1:2 ADC board. This board sacrifices the lower 4 bit of each sample. The disadvantage of the Demux 1:2 board is, it has only 4 bits because it is limited by the number of pins of the ZDOK connector. On the other hand, the output data of the Demux 1:2 board is demultiplexed by 8. This allows the use of all of the ZDOK pins at half the Demux 1:1 rate. Therefore the clock rate of Demux 1:2 board is half of Demux 1:1 board. The system clock of ROACH board usually aligns the clock signal of the ADC board to minimize the spurious harmonics. While the Demux 1:2

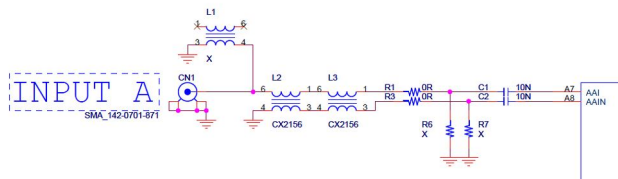


Fig.1. Input schematic of ADC board. There are 3 baluns on the schematic, L1, L2 and L3 for limiting the input signal in the range of 2.5GHz. Input signal goes thru those baluns, crosses zero ohm resistor, R1 and R3, then passes thru the capacitors of 10n value, C1 and C2, enter the input pins of ADC chip, A7 and A8. Two termination resistors R6 and R7 on this schematic are not populated.

<sup>a</sup>: The authors are with the Academia Sinica Institute of Astronomy and Astrophysics, P.O. Box 23-141, Taipei, 106, Taiwan. (phone: 886-2-23665347; fax: 886-2-23677849; e-mail: [homin@asiaa.sinica.edu.tw](mailto:homin@asiaa.sinica.edu.tw)).

ADC board is driven up to 2.5GHz, With the de-multiplexing factor of 8, the system clock is only 312.5MHz, which is within the operating range of the ROACH1 board.

In this article, mainly the Demux 1:2 version of the 5Gsp/s ADC board was under test for the characterization. The Demux 1:1 board was examined only for the impedance of the clock traces. Passive and active tests were carried out to have more information about the board. Passive tests tell the impedance of the PCB traces, insertion and reflection loss of the input path and the connected passive components. Active measurements tell the typical ADC characterization, such as Effective Number Of Bits (ENOB), Signal to Noise and Distortion (SINAD) and Spurious Free Dynamic Range (SFDR) [3].

## II. PASSIVE MEASUREMENT OF INPUT BALUNS

During S21 transmission test, two pigtail UT-047 wires with two SMA connectors were soldered to pin A7 and pin A8 individually. The SMA connector to A7 was connected to an Agilent PNA-X N5245A Network Analyzer. The SMA connector at A8 was terminated with a 50 ohm load. Physical setup is depicted in Fig.2. The blue line in Fig.3 shows the transmission loss of the 2 balun configuration and red line shows the transmission loss of the 3 balun configuration. The baluns, CX-2156[4] by Pulse, used in the input port contributed 0.4dB transmission loss each, for the 2 balun configuration, there is 0.8 dB transmission loss in total. From the plot, it can be easily distinguished that the 2 baluns configuration has better transmission performance.

A 100 ohms termination resistor is placed between pin A7

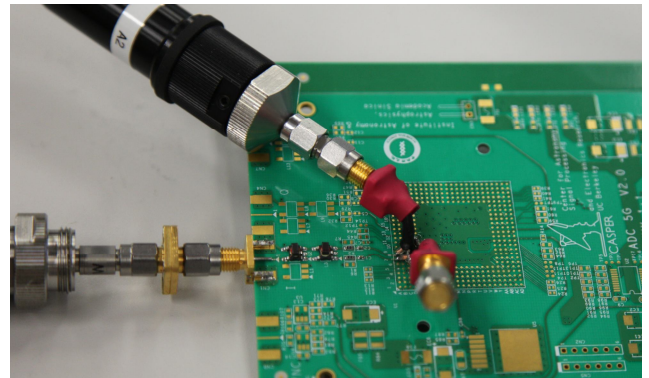


Fig. 2. Bare board with a two balun input configuration under test for transmission performance.

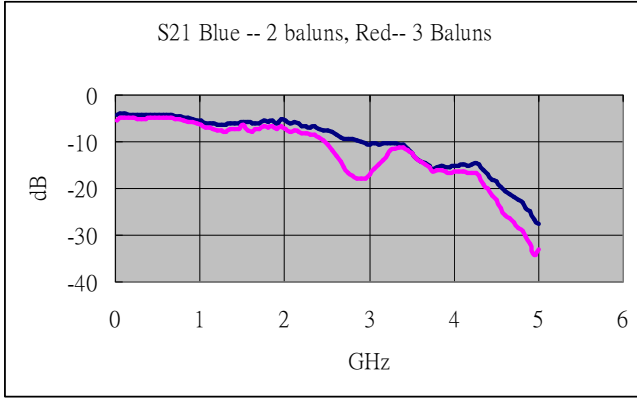


Fig 3. Transmission of signal input with 2 baluns and 3 baluns configuration.

and A8 instead of pigtail SMA connectors while the test of return loss was performed. The result is depicted as Fig. 4.

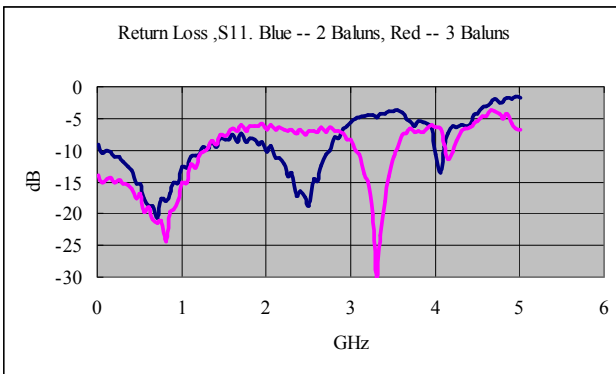


Fig. 4. Return losses of 2 baluns and 3 baluns configurations.

From the plot, the 2 baluns configuration has lower return loss than the 3 baluns configuration and was chosen as the best balun configuration.

From the measurements of insertion loss, S21, and return

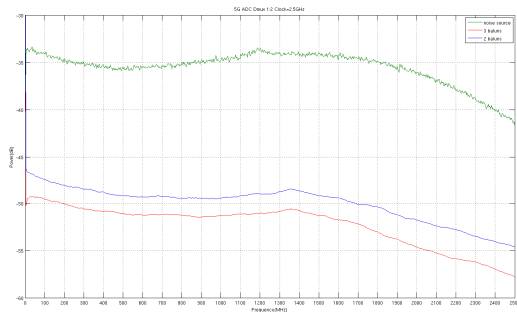


Fig. 5. Applied the noise source to the ADC board and took the data from ROACH, FFT performed in MATLAB. The green curve on the top is the spectrum of noise source by spectrum analyzer. The blue curve is the spectrum of 3 balun configuration and the red curve 2 balun configuration. From the plot, 2 baluns has better flatness performance than 3 baluns'.

loss, S11, for 2 balun and 3 balun configuration, we can conclude that 2 baluns configuration is better for our application. ASIAA's key projects are focused on the broadband and high frequency. 3 baluns has better performance in low frequency zone where will be our guard band area, the data will not be used in our application. Thus, only the 2 balun configuration of ADC board is under test in the following characterizations.

### III. IMPEDANCE MEASUREMENT OF CLOCK TRACES

At the time of this work, the Demux 1:1 ADC board was reported had problem to output clock signal to Roach 2 board. Concern has been drawn to the layout of clock traces. Consequently, impedance measurements of clock traces have been carried out by employing the Time Domain Reflectometer (TDR).

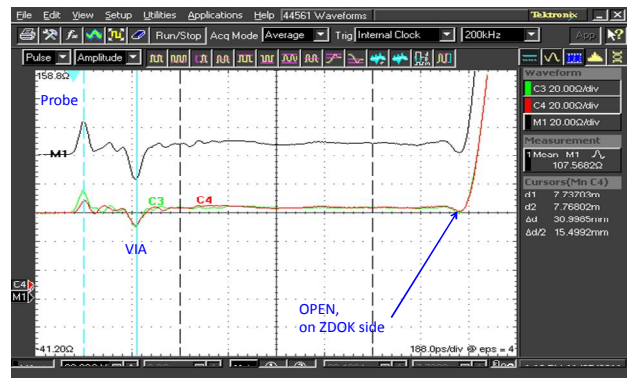


Fig. 6. Impedance of Demux 1:1 board without ZDOK installed. The red and black lines show the impedance of the pair of differential traces. The green line is the average impedance of the pair. First peak from the left is where the probe touched, the valley is caused by the thru hole. There is little bumpy curve between the peak and valley, that is the impedance of the clock trace. Compare to the valley, the bumpy impedance caused by the long clock trace is negligible.

A Tektronix DSA8200 by was used for this measurement. Measurement proceeded straightforwardly by probing the SMA connector. The ADC board had no ADC chip installed. The results are as showed in Fig. 5 to Fig.8. The red and black curves show the impedance of the pair of differential traces. The green curve is the average impedance of that pair. The first peak from the left labeled "PROBE" is caused by the test probe, the valley labeled as "VIA" is caused by the thru hole. There is little bumpy curve between the peak and valley, that is the impedance of the clock trace. The scale of Y axis is 20 ohms, the ideal green line is on the middle of the plot which is 100 ohms.

Fig. 6 shows the impedance of Demux 1:1 board without ZDOK connector on it. The impedance variance of the clock

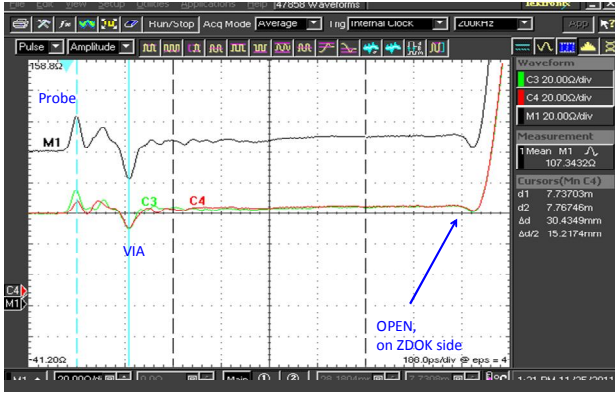


Fig. 7. Impedance of Demux 1:2 board without ZDOK.

traces of Demux 1:1 board, is smaller than that of the Demux 1:2 board. The measurement results do not reveal the problem that was reported concerning the Demux 1:1 board.

Fig. 7 shows the impedance of Demux 1:2 board without ZDOK connector on it. The peak between the peak of “Probe” and the valley of “VIA” is caused by the pair of serpentine paths, which is to equalize the path lengths between the A and C clock pairs. The magnitude of abrupt impedance by the serpentine clock traces is almost the same as the impedance valley caused by the thru hole.

Fig. 8 and Fig. 9 show the impedance of the Demux 1:1 and the Demux 1:2 board with ZDOK connectors installed individually. The impedance mismatch by the ZDOK and the thru hole are more severe than the clock traces.

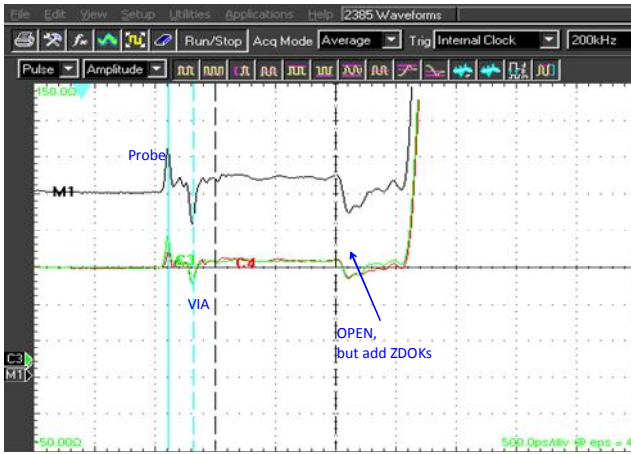


Fig. 8. Impedance of Dmux 1:1 board with ZDOK.

#### IV. SFDR MEASUREMENT

The input frequency of Continuous Wave (CW) signal was properly chosen to have the pure monotonic signal right on the center of spectral bin. To avoid artifacts of the quantization noise correlation[4], or the effect of Differential

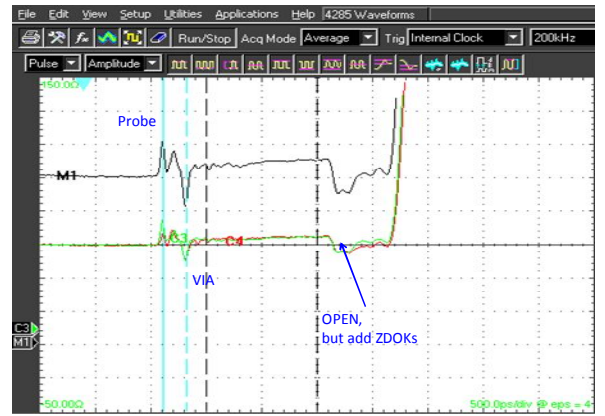


Fig. 9. Dmux 1:2 board with ZDOK installed. Black and red line both represent the resistance of the pair of differential line respectively. The green line is the average resistance of the pair of differential line. The scale of Y axis is 20 ohm per grid, the ideal resistance is at the center of Y axis, i.e. 100 ohm

Nonlinearity (DNL), a low power noise was added to the carrier. A 2 GHz bandwidth noise source was attenuated by 30dB to the carrier, passed thru a low pass filter, and then combined with the CW carrier by a combiner. At the end, the dithered carrier was sent to the 5Gbps ADC board which was the device under test.

The clock frequency was fixed at 2500MHz by employing an Agilent 83630 synthesizer at 0dBm. The CW signal was provided by another Agilent 83630 synthesizer, at -5dBm, the value was selected to avoid saturation of ADC level.

To have the spectrum for analysis, the Fast Fourier Transform (FFT) was performed in Matlab. The number of sample points is 16384, that leads to the process gain of 39.13 dB as equation (1) shows:

$$ProcessGain = 10\log\left(\frac{M}{2}\right) \quad (1)$$

Where M is the number of samples.

Setup of the active measurement such as SFDR, SINAD and ENOB is that a 5Gbps Demux 1:2 ADC board was plugged in the ZDOK 0 connector of a ROACH 1 board. Inside the ROACH board, a simple model file was running. The model had a snap block capturing the digitized data from the ADC board, then saved it in the Block RAM (BRAM).[6][7] A Python program was running in the Personal Computer (PC) pipelined the data in the BRAM to the PC and saved the data to the hard drive. The test conductor retrieved the data files and analyzed with Matlab.

Because the Demux 1:2 was specifically designed to meet the limitation of ZDOK's pins by discarding the 4 least significant bits, there is no information of those 4 bits from the board. The full scale of 4 bits input can't be converted to the full scale input of the ADC chip which is  $\pm 0.5V$  directly. To avoid the ambiguity, the parameters in the rest of this

article are all respect to the carrier only.

As illustrated by Fig. 10, the SFDR is the power of carrier to the power of the strongest harmonic. Fig. 11 depicts that the SFDR of Demux 1:2 in the input range of 100MHz to 2400MHz. The SFDR values are around 35dB at low frequency region, and the values are down to 25 dB at high frequency region.

## V. SINAD MEASUREMENT

SINAD as its name, comprises two components, signal to noise (SNR) and signal to distortion (THD). The typical method to calculate these two values is by getting information from the spectrum. SNR is calculated by subtracting the noise floor and the process gain from the power of carrier as Fig. 10 demonstrates.

The top 5 harmonic tones were picked and summed as the power of Distortion (D). Subtracting the power of top five harmonics from the carrier (S) power, the Total Harmonic Distortion (THD) can be derived. Combine the SNR and THD, the SINAD parameter can be derived as the equation (2) shows:

$$\begin{aligned} SNR &= 10\log\left(\frac{S}{N}\right) \\ THD &= 10\log\left(\frac{S}{D}\right) \\ SINAD &= 10\log\left(\frac{S}{N+D}\right) \end{aligned} \quad (2)$$

Where N is the power of noises.

To avoid saturation, the input power was selected around 1 bit under the full scale. The ENOB has to be compensated due to the loss of the input power by equation (4). We input the amplitude around the half of the full scale. The ratio is 15/8, 15 is the full scale of 4 bits.

Another more straightforward method to derive the SINAD is by using software tools, such as Matlab, in this work. The process is as follows, search the entire spectrum, locate the bin of carrier, sum the power of carrier with nearby spectral bins as the power of signal. Also sum all the power of every spectral bin as the total power of the spectrum. Subtract the total power of spectrum to the power of carrier, leaves the power of noise and distortion. Divide the power of signal by the power of noise and distortion as equation (2) shows.

Because all the harmonics are taken into account, the SINAD obtained by software method is a little bit worse than it is obtained from the plot.

## VI. ENOB BY 3 METHODS

Once there is SINAD value, the ENOB can be derived directly using equation (3):

$$ENOB = \frac{SINAD - 1.76dB + 20\log_{10}\left(\frac{Fullscale\_Amplitude}{Input\_Amplitude}\right)}{6.02} \quad (3)$$

With two values of SINAD from previous section, we can derive two ENOB correspondingly. Another approach to characterize the ENOB of ADC board is performed by sine wave curve fitting.[3] Curve fitting tool called “cftool” by Matlab [8] is employed to perform this characterization.

“cftool” fitted the data set according to the sine wave as equation (4) shows. In the ideal case, the CW input signals are pure sine waves without offset. Thus, 4 parameters of fitting the curve as equation (4) shows, is used to fit the amplitude, phase, frequency and offset:

$$F(x) = a1 * \sin(b1 * x + c1) + d1 \quad (4)$$

After fitting, it generates measures of the goodness of fit. The key parameter is the Sum of Squares Due to Error. This statistic measures the total deviation of the response values from the fit to the response values. It is also called the summed square of residuals and is usually labeled as SSE. A value closer to 0 indicates that the model has a smaller random error component, and that the fit will be more useful for prediction. The SSE measure includes errors due to

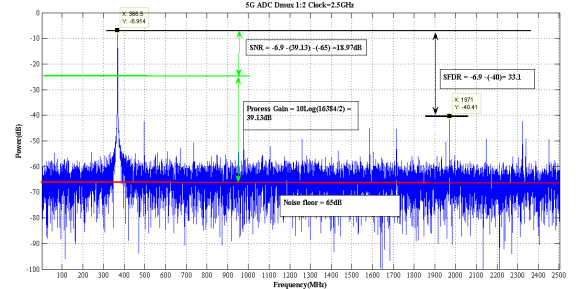


Fig. 10. Typical SFDR, SINAD measurement.

Integral Non-Linearity (INL), DNL, missing codes, jitter and noises. Note that the curve fitting method is performed in time domain, consequently no spectral information can be

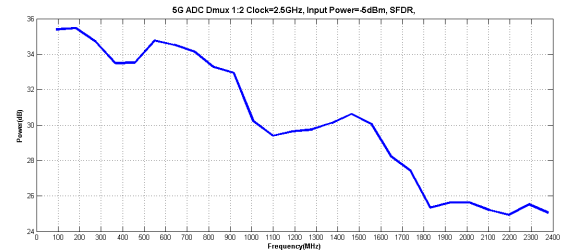


Fig. 11. SFDR of input frequency from 100MHz to 2400MHz..



generated such as THD and SINAD.

In ideal case, there is square error of every sample. In the assumption of one bit least significant bit(LSB), that is 1/12. Compare the SSE by the curve fitting with the ideal square error of whole spectrum, the ENOB can be obtained by following equation (5):

$$ENOB = N - \log_2 \left( \frac{Q_A}{Q_T} \right)$$

$$Q_T = \sqrt{\frac{16384}{12}}$$

$$Q_A = \sqrt{SSE}$$
(5)

Where 16384 is the number of samples in the work, N is the number of ADC bits.  $Q_T$  is the theoretical N-bit RMS quantization error.  $Q_A$  is the actual RMS error from best fit sine wave.

The ENOB by curve fitting of this work is around 3.6 to 3.9 bits as the dark blue curve illustrated in Fig. 13. It considers the purity of the sine wave only, without taking the input power level into consideration. The ENOB by the curve fitting method has better numbers than the ones by the previous two methods.

## VII. SUMMARY

The passive measurements in Section II and III have shown that the layout of the Demux 1:2 PCB board is promising. The 2 balun configuration has been adopted by ASIAA to have better performance in high frequency end. The major interesting ADC characterization parameter, ENOB, has been approached by 3 methods. The typical method by the spectrum plot has the ENOB in between. Reading the noise floor visually from the spectrum plot, could lead to worse flatness across the whole band. The ENOB by the software program has the worst ENOB due to taking all the harmonics into account. In the other hand, because no human error is involved, it has the better flatness all over the band. The ENOB by curve fitting has the best ENOB, but considers the purity of sine wave without regard to spectral characteristics.

The typical method is also the most popular way for ADC characterization, the ENOB by the typical method is most valuable for comparison. The worst ENOB is around 2.5 bits at the high frequency end, and the best ENOB is around 3.9 bits at the lower part of the band.

The other two key parameters of ADC characterization, SFDR and SINAD are also obtained by the typical methods.

The board under test can digitalized input signals up to 2.5GHz, the SFDR, SINAD and ENOB are reasonable for a 4 bit test but worsen as the input frequency increases.

## VIII. FUTURE WORK

As the Roach2 becomes available at the end of 2011, we would like to keep characterizing the other version of 5Gbps ADC board, i.e. Demux 1:1 board (full speed 8 bit) which is not possible using the Roach 1 board.

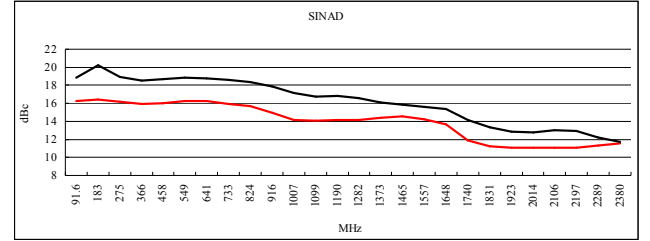


Fig. 12. Black represents the SINAD by typical method. Red line represents the SINAD calculated by Matlab program.

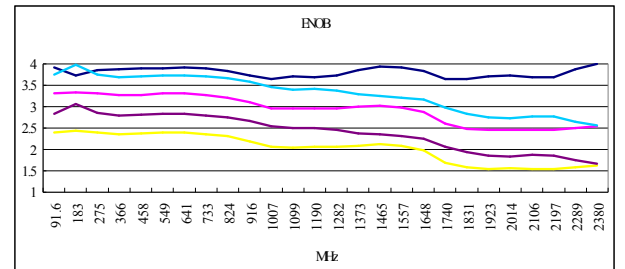


Fig. 13. Effective Number of Bits by 3 methods. Dark blue line represents the ENOB by curve fitting. Light Blue line represents the ENOB by typical method with compensation. The pink line represents the ENOB calculated by Matlab program with compensation. Brown line represents the ENOB by typical method without compensation. The yellow line represents the ENOB which is calculated by Matlab program without compensation.

## REFERENCES

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- [2] [Data Sheet: EV8AQ160](#), e2V
- [3] [Walt Kester, "Data Conversion Handbook, Analog Devices", ISBN: 0-7506-7841-0](#)
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- [6] Walt Kester, "Taking the Mystery out of the Infamous Formula, SNR = 6.02N + 1.76dB, and Why You Should Care", MT-001, Tutorial, Analog Devices.
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- [8] [Matlab](#)