Background & History of CASPER Hardware

CASPER History (1)

- SERENDIP5 Board (~2003-2004)
  - Designed by Aaron, revised by Henry
  - 1x Virtex2 2V1000, 1X Virtex2 2V6000, Integrated 100MHz ADCs, CompactPCI backplane
  - GALFA Spectrometer
  - Astronomy Signal Processor (ASP)
  - SERENDIP5 SETI Spectrometer (superseded)
  - ATA-4 Fboard
  - Australia CSIRO

CASPER History (2)

- BEE2
  - 5x Virtex-II Pro 2VP70s, 18x CX4
  - Architecture by Chen Chang (Ph.D), implementation by Pierre-Yvez Droz (M.S.)
  - Successor to BEE1 (20 Virtex FPGAs)
    - ASIC architecture, implementation **emulation**
  - Solution looking for a problem

CASPER History (3)

- IBOB
  - Virtex-II Pro 2VP50, 2x CX4, 2x Z-DOK+
  - Designed in SSL collaboration
  - Schematics by BWRC, layout to VDI
  - Solves BEE2 data input problem
- ADC
  - Dual 1GS/s ADCs
  - Schematics by BWRC, layout to VDI

Board Design Notes

- BEE2, IBOB, ADC designed using “BEE_DB” text-based netlist language; schematics auto-generated (illegible)
- Cadence ConceptHDL schematics + Cadence Allegro layout
- Layout .brd files readable using Allegro Free Physical Viewer; probe net connections

Board Architecture Notes (1)

- System Clock (sys_clk) vs. User Clock (usr_clk)
  - BEE2, IBOB: sys_clk is fixed 100MHz on-board oscillator; used for PowerPC, buses
  - BEE2s: programmable clock generator for usr_clk; both sys_clk & usr_clk can mux in external input

Board Architecture Notes (2)

- BEE2 & IBOB designed to support both 10GbE & InfiniBand
- Both protocols are built on top of XAUI (**X** **A**ttachment **U**nit **I**nterface)
- XAUI uses 8b/10b encoding
  - InfiniBand: 8Gb/s (2.5Gb/s per lane) using 125.00MHz reference
  - 10GbE: 10Gb/s using (3.125Gb/s per lane) using 156.25MHz reference
  - BEE2 takes both clocks in, uses Xilinx built-in clock mux; IBOB uses external jumpers to select

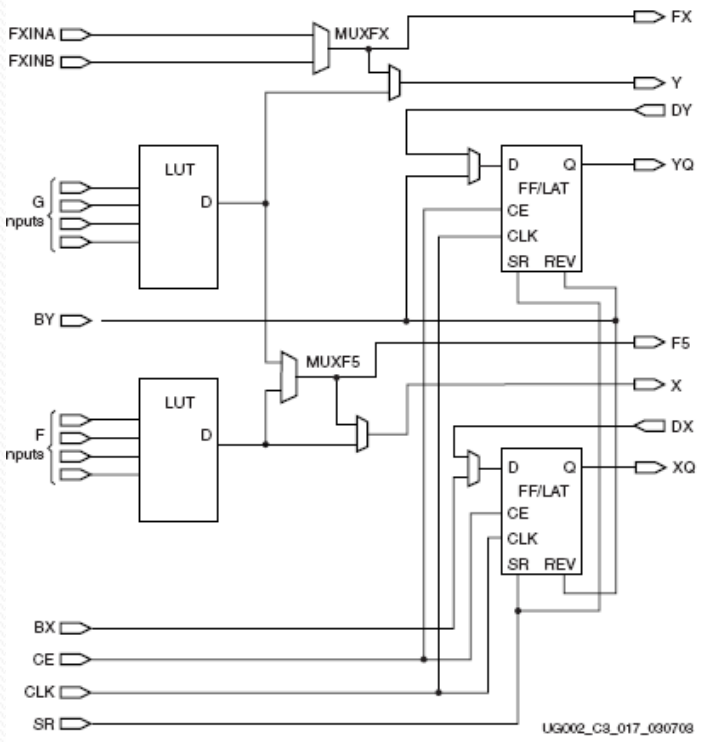
Xilinx Architecture (1)

- Read datasheets, user guides from Xilinx website (UG012, DS083, UG190, DS202)

- SRAM-based configuration
- Hierarchical routing fabric
- Logic fabric with “hard” elements (BlockRAM, multipliers, PowerPC)

Xilinx Architecture (2)

- Basic “logic element”: 4-input lookup table (4LUT) + flip-flop/Latch
- 2 LUTs & 2 FFs per SLICE
- 4 SLICEs per Configurable Logic Block (CLB)
- Each LUT can be used as an SRL16



Xilinx Architecture (3)

- Hierarchical routing fabric
- Low-skew global lines connected to global buffers/MUXs (BUFG/BUFGMs)
- BUFGs have associated IOBs
- Digital Clock Managers (DCM) with DLLs to do clock cleaning, phase shifting, frequency synthesis