Xilinx EDK in a Giant Nutshell

References

- Xilinx Platform Format Specification Reference Manual
  - 7.1
  - 10.1
  - 11.1
- EDK Tutorial

- Xilinx FPGA Design Flow Overview
  - http://www.xilinx.com/itp/xilinx10/isehelp/ise_c_fpga_design_flow_overview.htm

Background

- Target market: programmable system on chip (PSoC) embedded systems
  - Subdivision into “IP cores”
- EDK: **E**mbedded **D**evelopment **K**it
  - Primary tool: Xilinx Platform Studio (XPS)
  - Handles embedded processor and associated peripherals
  - Generates files for ISE
- ISE: Integrated Software Environment
  - Primary interface: Project Navigator
  - Suite of tools for to go from HDL to bitstream

EDK Project Files

- .xmp – XPS Microprocessor Project
  - Main project file
  - Target architecture
  - Project paths & included files
- .mhs – Microprocessor Hardware Specification
  - Top-level wrapper
  - IP core instantiation and interconnection
  - Top-level ports
- .mss – Microprocessor Software Specification
  - Defines drivers for instantiated cores

EDK PCores

- Modular, reusable design subcomponents
- Built-in EDK pcores in $XILINX_EDK\hw

- Naming convention: *bus*_name_v*X*_*YZ*_*n*
  - *I.e.,* opb_adccontroller_v1_00_a

- Can use Create/Import Peripheral Wizard

EDK PCores Structure

- \data – Pcore information
  - *.mpd*: **M**icroprocessor **P**eripheral **D**efinition
    defines connectivity and parameters
  - *.pao*: **P**eriperal **A**nalyze **O**rder
    defines list of HDL files used by core
  - *.bbd*: **B**lack-**B**ox **D**efinition
    defines list of black-box files used by core
- \hdl – HDL source
  - Separate \verilog and \vhdl directories
- \netlist – Black-box netlist
- \doc – Associated documentation

ISE Project Files

- .ucf – User Constraints File
  - Defines physical, hardware-specific constraints
  - I/O pin locations, user-defined placement & routing
  - Timing constraints