MKID ADC Test Report
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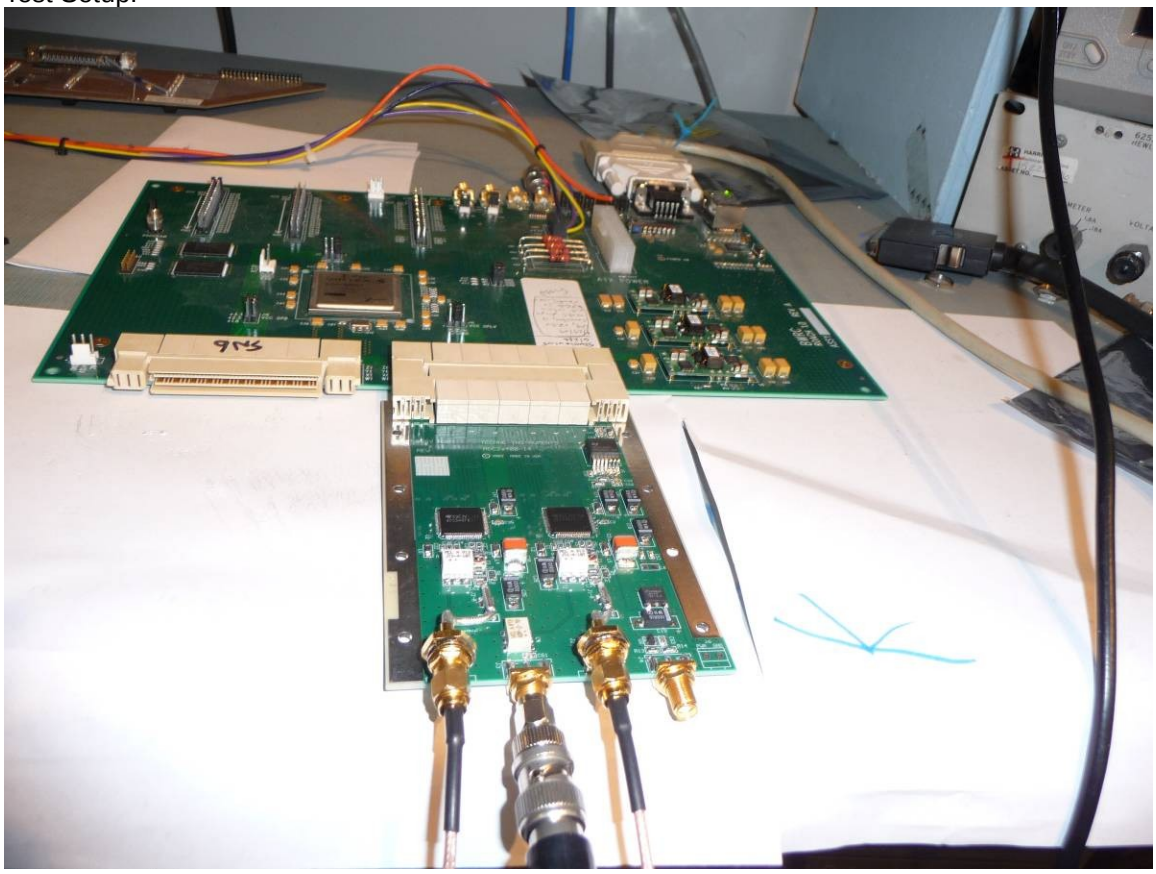
July 28, 2009

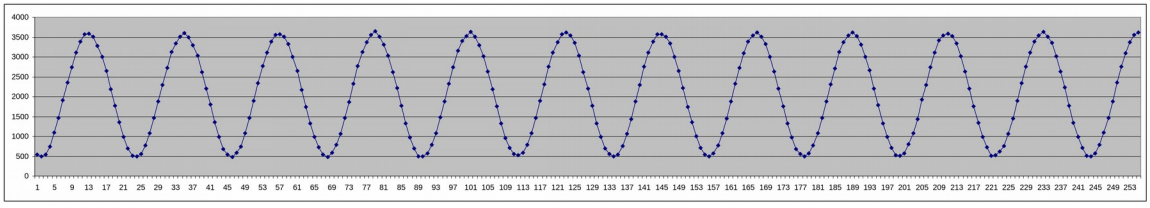
Test Setup:



I tested the first-article MKID_ADC (also known as ADC2x550-12. The label silk-screened on the PCB says “ADC2x14-400”, referring to the other ADC chip that this board can accept, the TI ADS5474. This board was populated with two ADS54RF63I’s). The ADC board was plugged into a “miniROACH” FPGA board.
I drove the clock input with a 550MHz +6dBm sinewave from a Fluke 6062A synthesizer, and the ADC inputs from a PTS3200 synthesizer, via a power splitter and equal-length cables.

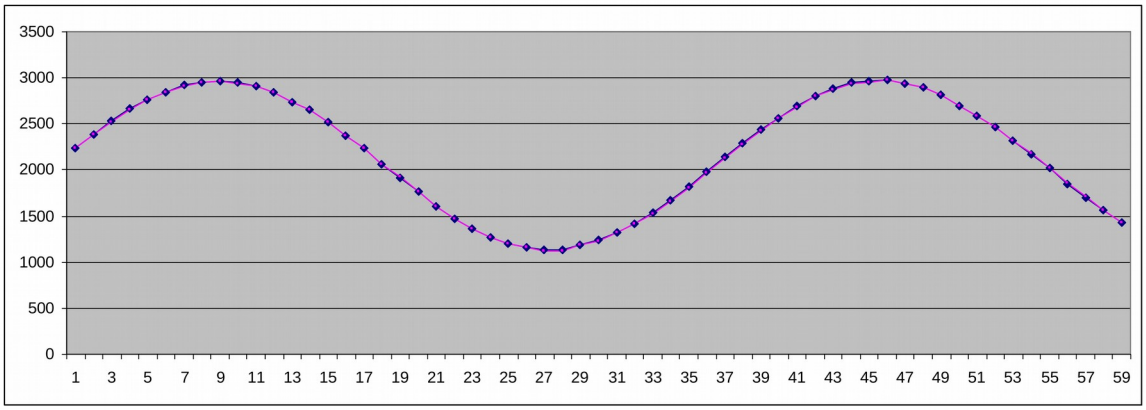
I wrote firmware to read a series of 1024 simultaneous samples from each of the two ADC channels into a FIFO buffer, then trickle the samples out through a serial port. Software on the PC provided quick-look waveforms, and stored the data in a file for further analysis using Excel.

Some waveforms

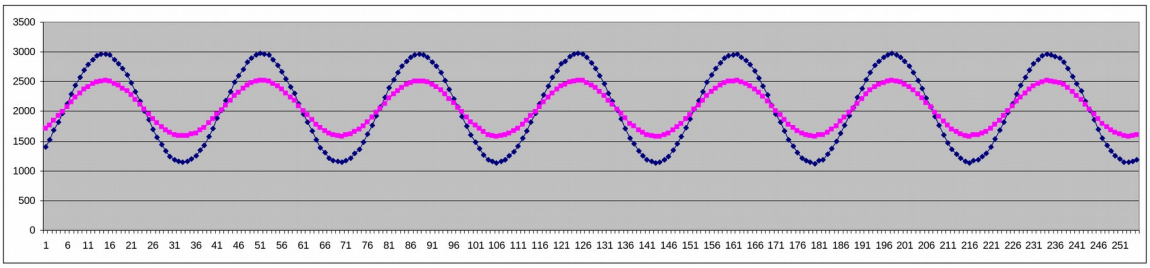


A) 15MHz large amplitude sampled at 550MHz, 1 channel driven

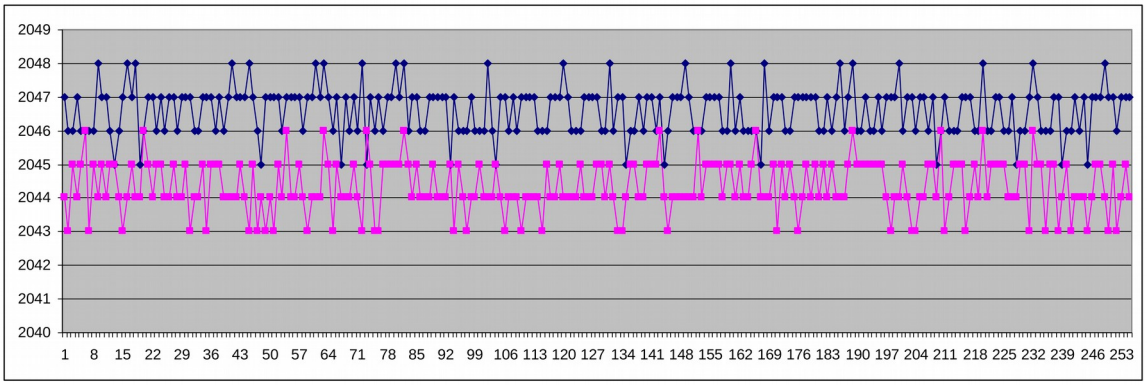
This is the maximum amplitude available from the synthesizer, 341mV rms as measured on my oscilloscope, or 964mV pp. Displayed amplitude is 3085 LSB's pp, so full scale range is 1.28vpp.



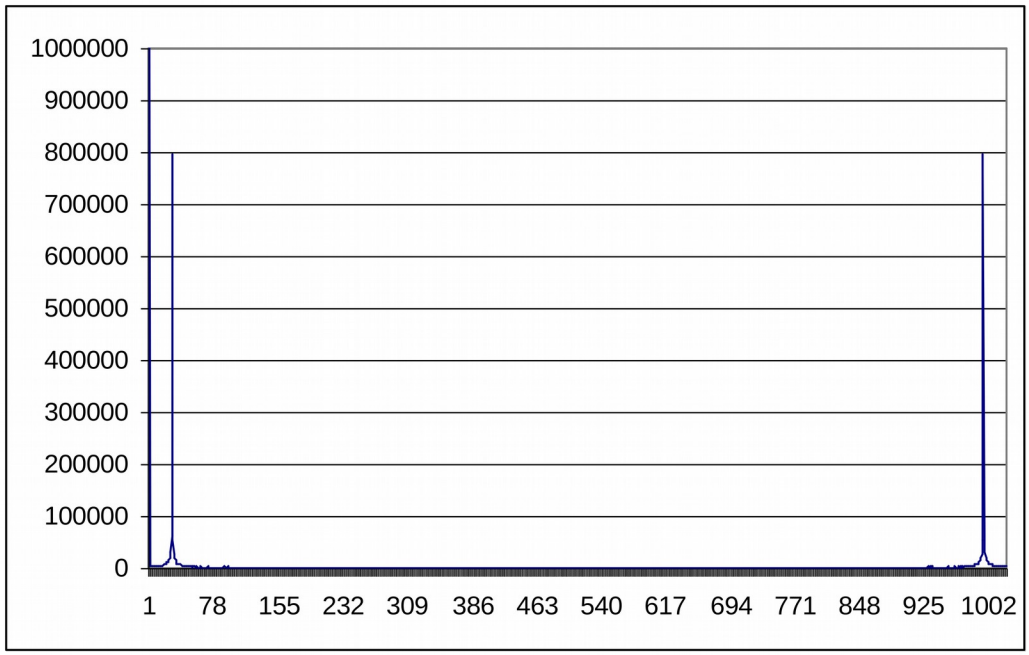
B) Both channels driven. The two waveforms are nearly identical.



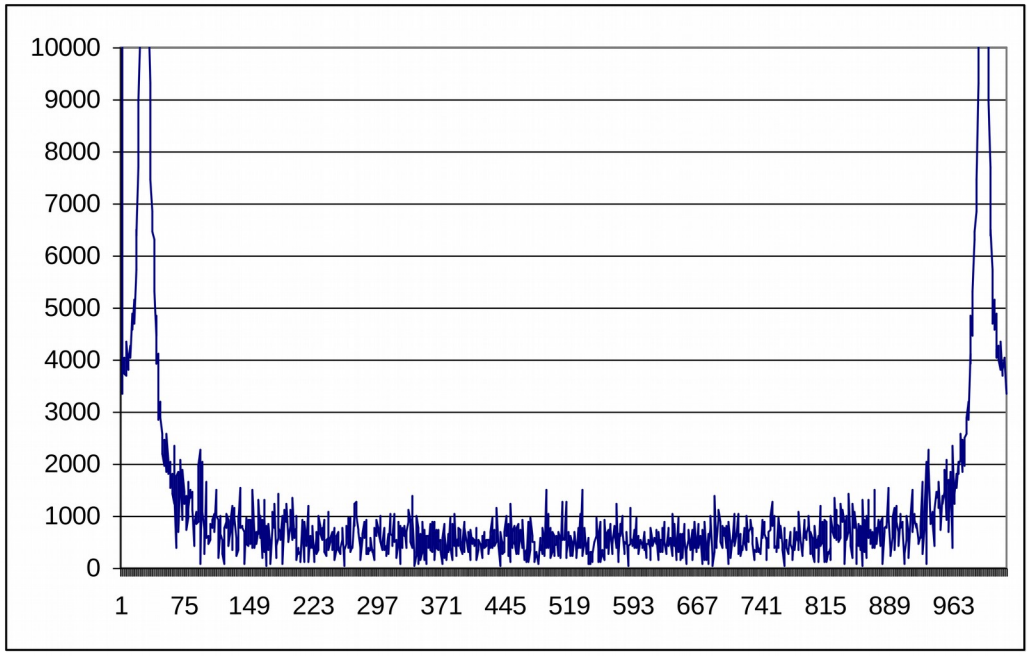
C) Both channels driven, 6dB attenuator in Q.



D) Both channels undriven, a couple LSBs difference in offset between channels. Rms noise level about 0.7LSBs, each channel.

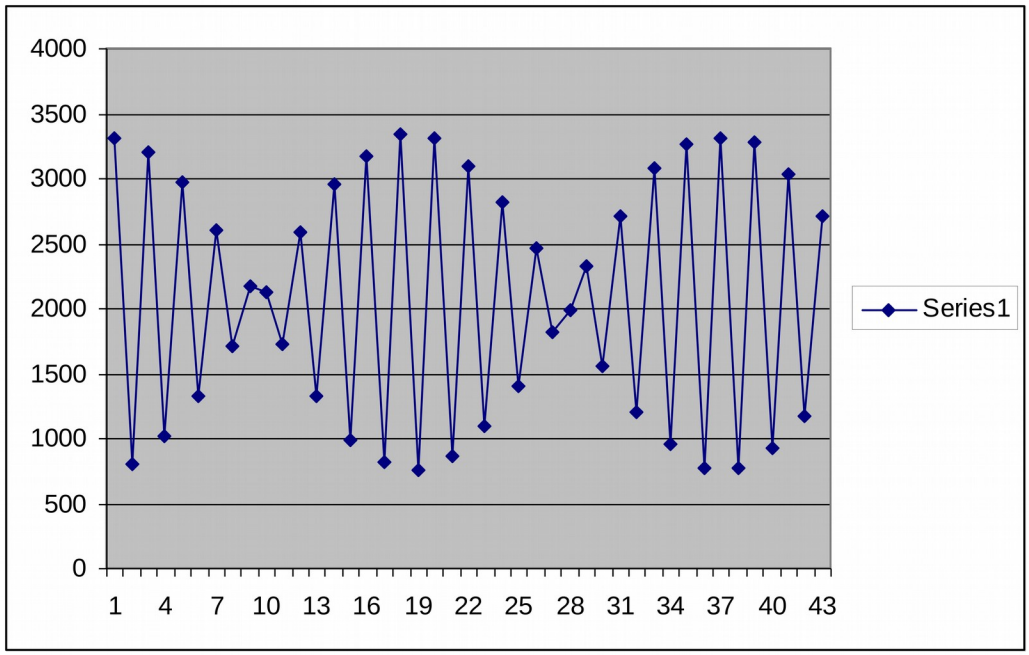


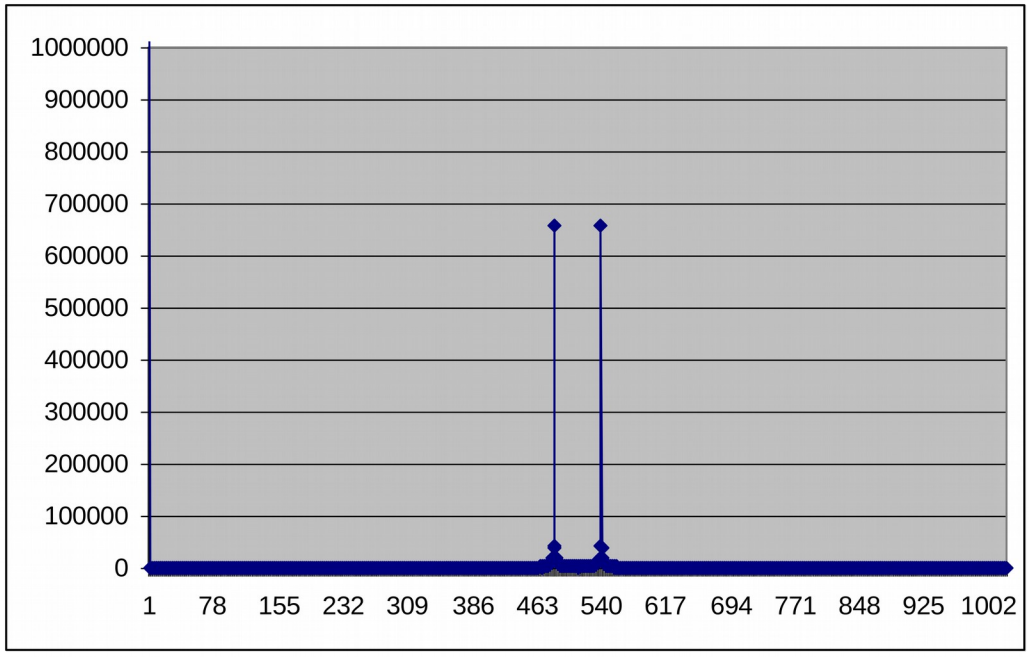
E) 1024-point FFT of waveform as in A). No windowing applied.



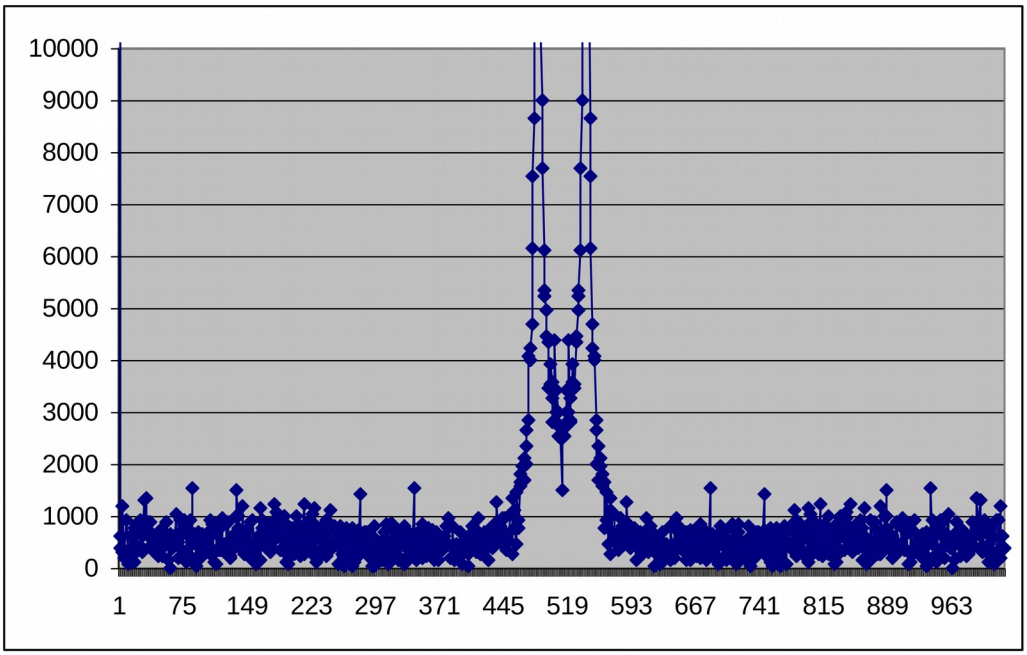
Same as E), zoomed vertically x100.

F) 260MHz signal, 550MHz sampling.


4000
3500
3000
2500
2000
1500
1000
500
0
1 4 7 10 13 16 19 22 25 28 31 34 37 40 43
Series1


1000000
900000
800000
700000
600000
500000
400000
300000
200000
100000
0
1 78 155 232 309 386 463 540 617 694 771 848 925 1002

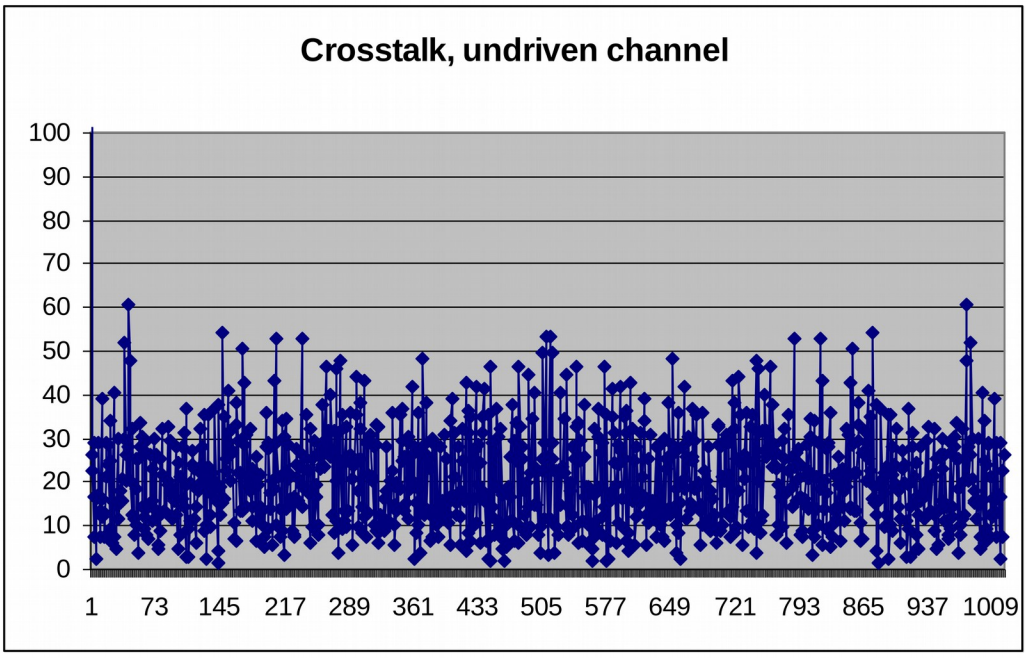
G) FFT of F)



G), zoomed x100 in gain.

Crosstalk

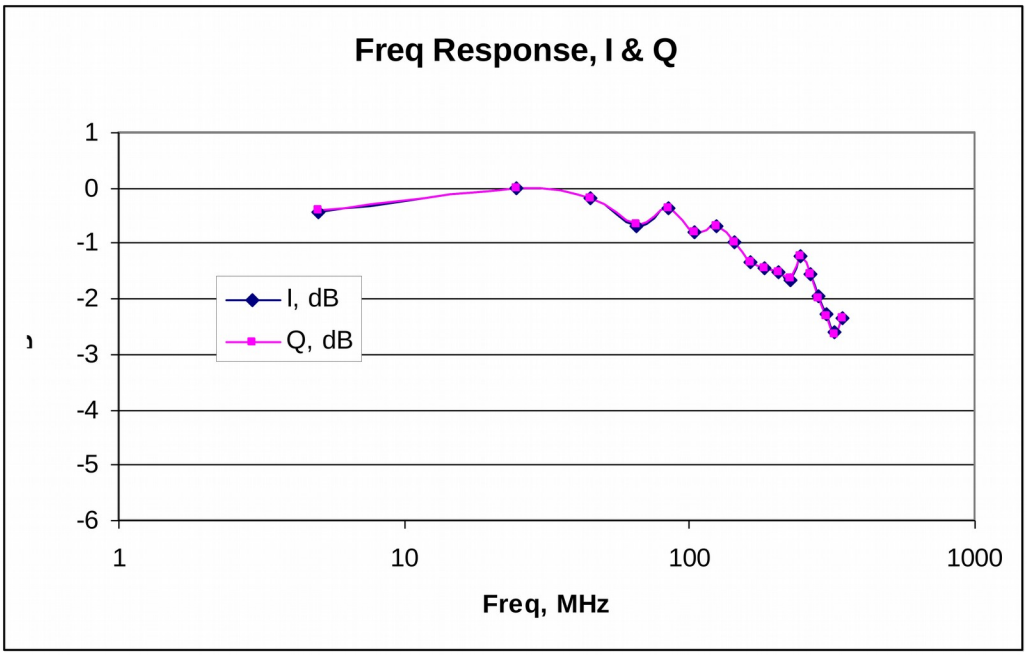
I drove one input with a 1vpp 260MHz sinewave and looked at the other channel's output, then took the FFT:



Can't see any crosstalk

Frequency Response

I stepped the frequency through 20MHz increments to generate the following plots.



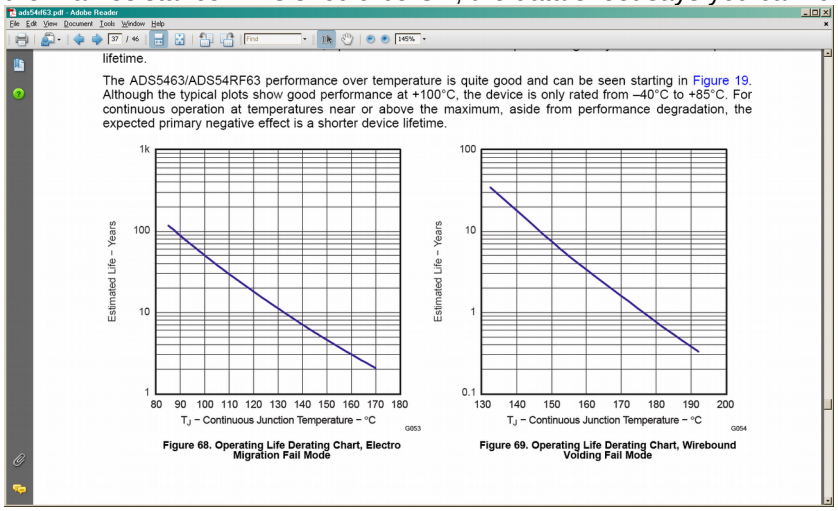
Gain flatness is within 2dB to beyond the first Nyquist zone. The two channels match very well.

Data synchronism

In the waveforms above, it's clear that where two waveforms are plotted, the samples are in sync. But I did catch it once where there was a 1-cycle delay between I & Q. There are no phase adjustments available inside the ADC chips, but there may be more robust clock phasing possible in the FPGA code. I'll know more when I've tested a bunch of units.

Power/Thermal

The ADC chips dissipate 2.2W each and get hot; I measured a case temperature of 50C on the bench. This implies a junction temperature of about 100C, based on 24C/W junction-case thermal resistance. This should be OK; the data sheet says you can run them at 100C for years:



But if they will be in a hot environment, some airflow should be provided.