6 Gsps ADC Interleave Test

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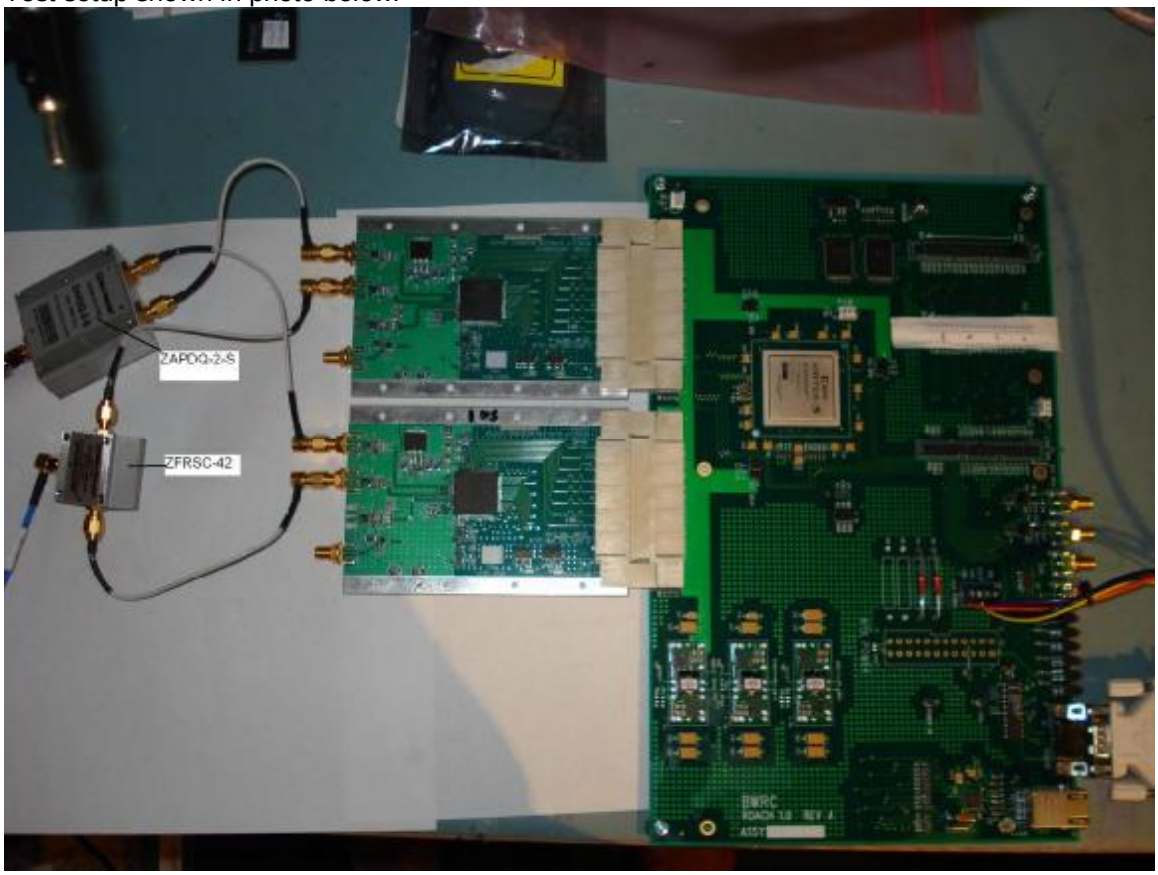
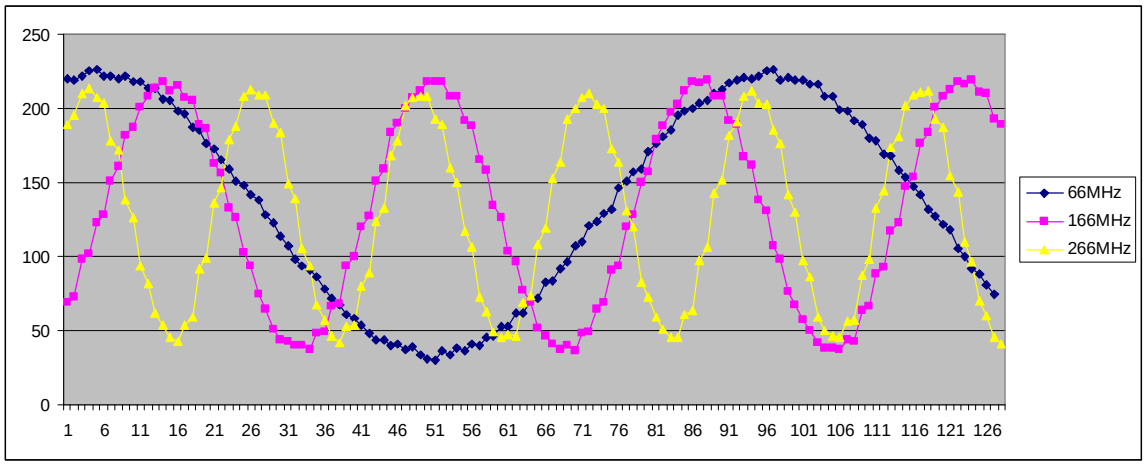
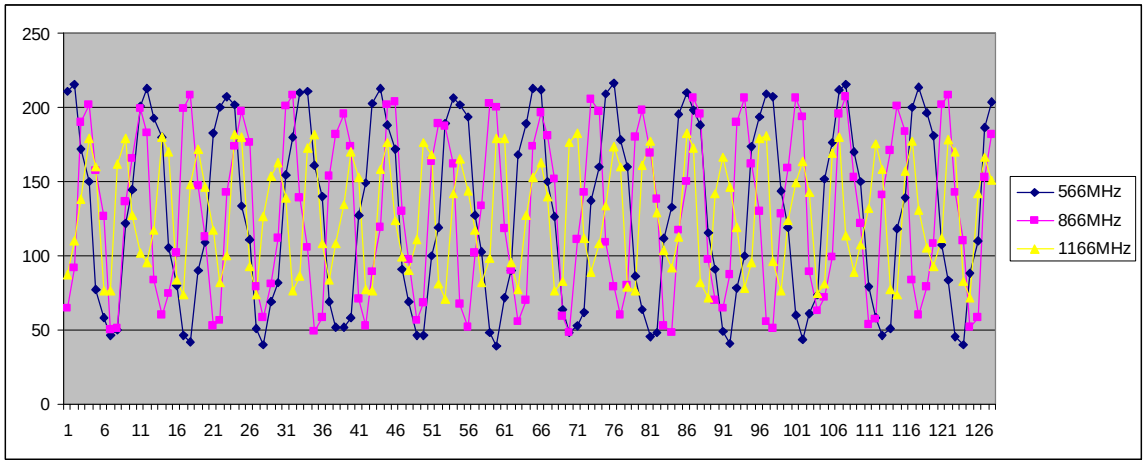
The purpose of this test was to interleave two ADC083000 boards and measure the ADC board frequency response. Each ADC board sampled at 3 Gsps, for an effective sample rate of 6 Gsps. The two ADC boards (Assembly R271, revA), were plugged into a Virtex 5 board ("Roach 1.0", revA), with FPGA type XC5VSX50TFF1136 installed.

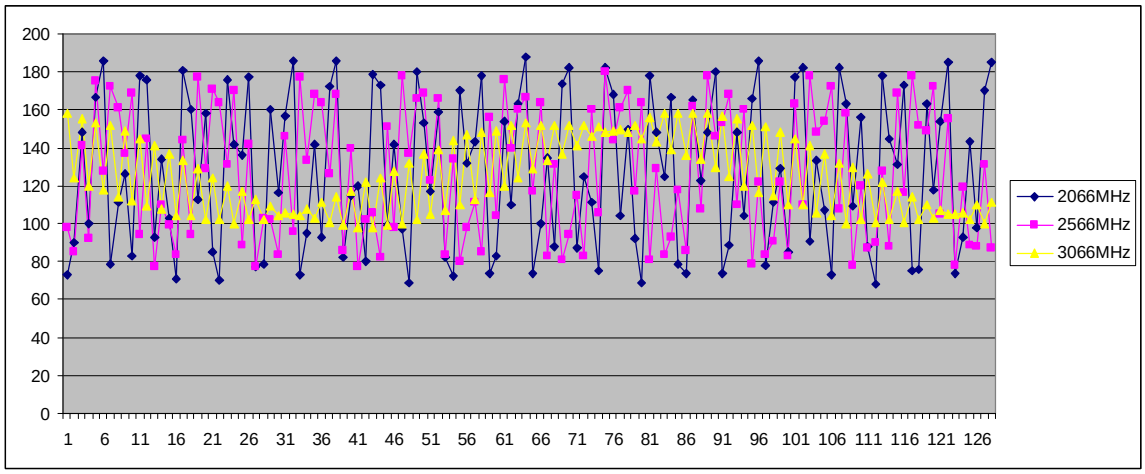
I drove the two ADC clock inputs with 1.5GHz through a ZAPDQ-2-S quadrature splitter (so one is delayed ¼ cycle at 1.5GHz, thus ½ cycle at 3GHz). I drove the two ADC inputs through a ZFRSC-42-S+ resistive splitter. I carefully matched cable lengths, and used all SMA connections. Clock frequency of the ADC interface is 375MHz, for a 750MHz DDR data rate. Test setup shown in photo below.



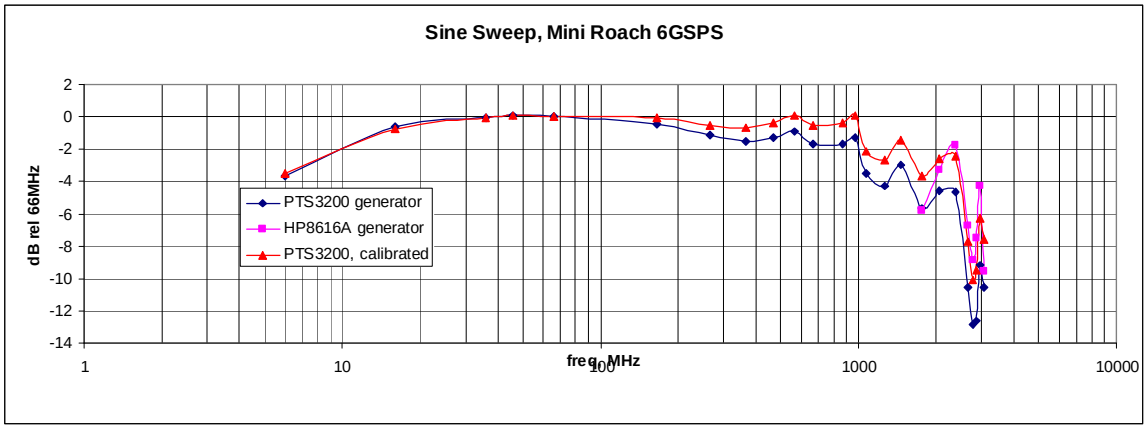
First I acquired 128 sample records and plotted them at various input frequencies:







Next I acquired 1024 sample records and computed rms amplitude vs frequency. I used two different RF generators for the input, an HP8616A (only goes 1.8GHz and up) and a PTS3200 (1MHz to 3.2GHz). I calibrated the PTS3200 output using an HP432A RF power meter. The red plot below shows the calibrated data.



Conclusions:

From the 266MHz plot it's clear that the differential sampling phase is off by something like 50ps. This will distort the waveforms, especially at higher frequencies, but shouldn't affect the rms values.

Analog bandwidth falls off rapidly above 2.5GHz, probably due to the ADC083000 response itself (National warned us that the 3GHz specified in the data sheet was not actually achieved).

Between 1GHz and 2.5GHz response is bumpy, maybe due to balun or PCB issues.