Table 154. Error calculation for programmed baud rates at f_{PCLK} = 30 MHz or f_{PCLK} = 60 MHz, oversampling by $8^{(1)}$ (continued)

| Oversampling by 8 (OVER8=1) | | | | | | | | | | | |
|-----------------------------|-------------|----------------------------|---|---|---------------------------|---|------------|--|--|--|--|
| Baud rate | | f _{PCLK} = 30 MHz | | | f _{PCLK} =60 MHz | | | | | | |
| S.No | Desired | Actual | Value programmed in the baud rate register | % Error = (Calculated - Desired)B.Rate /Desired B.Rate | Actual | Value programmed in the baud rate register | % Error | | | | |
| 7 | 460.8 KBps | 461.538 KBps | 8.1250 | 0.16% | 461.538 KBps | 16.2500 | 0.16% | | | | |
| 8 | 896 KBps | 909.091 KBps | 4.1250 | 1.46% | 895.522 KBps | 8.3750 | 0.05% | | | | |
| 9 | 921.6 KBps | 909.091 KBps | 4.1250 | 1.36% | 923.077 KBps | 8.1250 | 0.16% | | | | |
| 10 | 1.792 MBps | 1.7647 MBps | 2.1250 | 1.52% | 1.8182 MBps | 4.1250 | 1.46% | | | | |
| 11 | 1.8432 MBps | 1.8750 MBps | 2.0000 | 1.73% | 1.8182 MBps | 4.1250 | 1.36% | | | | |
| 12 | 3.584 MBps | 3.7500 MBps | 1.0000 | 4.63% | 3.5294 MBps | 2.1250 | 1.52% | | | | |
| 13 | 3.6864 MBps | 3.7500 MBps | 1.0000 | 1.73% | 3.7500 MBps | 2.0000 | 1.73% | | | | |
| 14 | 7.168 MBps | NA | NA | NA | 7.5000 MBps | 1.0000 | 4.63% | | | | |
| 15 | 7.3728 MBps | NA | NA | NA | 7.5000 MBps | 1.0000 | 1.73% | | | | |

^{1.} The lower the CPU clock the lower the accuracy for a particular baud rate. The upper limit of the achievable baud rate can be fixed with these data

Table 155. Error calculation for programmed baud rates at f_{PCLK} = 42 MHz or f_{PCLK} = 84 Hz, oversampling by $16^{(1)(2)}$

| Oversampling by 16 (OVER8=0) | | | | | | | | | | | |
|------------------------------|------------|----------------------------|---|---|----------------------------|---|------------|--|--|--|--|
| Baud rate | | f _{PCLK} = 42 MHz | | | f _{PCLK} = 84 MHz | | | | | | |
| S.No | Desired | Actual | Value programmed in the baud rate register | % Error = (Calculated - Desired)B.Rate /Desired B.Rate | Actual | Value programmed in the baud rate register | % Error | | | | |
| 1 | 1.2 KBps | 1.2 KBps | 2187.5 | 0 | 1.2 KBps | NA | 0 | | | | |
| 2 | 2.4 KBps | 2.4 KBps | 1093.75 | 0 | 2.4 KBps | 2187.5 | 0 | | | | |
| 3 | 9.6 KBps | 9.6 KBps | 273.4375 | 0 | 9.6 KBps | 546.875 | 0 | | | | |
| 4 | 19.2 KBps | 19.195 KBps | 136.75 | 0.02 | 19.2 KBps | 273.4375 | 0 | | | | |
| 5 | 38.4 KBps | 38.391 KBps | 68.375 | 0.02 | 38.391 KBps | 136.75 | 0.02 | | | | |
| 6 | 57.6 KBps | 57.613 KBps | 45.5625 | 0.02 | 57.613 KBps | 91.125 | 0.02 | | | | |
| 7 | 115.2 KBps | 115.068 KBps | 22.8125 | 0.11 | 115.226 KBps | 45.5625 | 0.02 | | | | |
| 8 | 230.4 KBps | 230.769 KBps | 11.375 | 0.16 | 230.137 KBps | 22.8125 | 0.11 | | | | |
| 9 | 460.8 KBps | 461.538 KBps | 5.6875 | 0.16 | 461.538 KBps | 11.375 | 0.16 | | | | |



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Only USART1 and USART6 are clocked with PCLK2. Other USARTs are clocked with PCLK1. Refer to the device datasheets for the maximum values for PCLK1 and PCLK2.