FRANK **SEELMANN**

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BS student studying Computer Engineering at SUNY New Paltz. Experienced with ARM Microcontrollers in C and FPGA devices in Verilog. Interested in computer architecture, computer hardware, and embedded systems.

EDUCATION

MAY 2022

Bachelor of Science in Computer Engineering, State University of New York at New Paltz

GPA 3.93

EMPLOYMENT AND VOLUNTEERING

JULY 2017 – PRESENT

Dietary Aide, Woodland Pond at New Paltz

Responsible for preparation & handling of foodstuffs, and ensuring residents receive food appropriate for their dietary restrictions.

FALL 2015 – SPRING 2019

Documentation Manager, St. Charles Borromeo School of Religion

Digital recordkeeping.

PROGRAMMING LANGUAGES AND HDLS

- C, C++, Java, ARM Assembly, MIPS Assembly, Python, JavaScript, Vue.js
- Verilog, System Verilog, VHDL

SOFTWARE

- PSpice, LTSpice, Electric VLSI, Quartus Prime, ModelSim, QuestaSim, Keil uVision5, Visual Studio Code, Unreal Engine 4, Git, Microsoft Office (Word, PowerPoint, Visio, Excel, Project Professional)

COURSE PROJECTS

Senior Design, Spring 2022 & Fall 2021

Creating a proof-of-concept project for generating solar power via the thermal expansion of a fluid. Working with a group of interdisciplinary engineers (Electrical, Mechanical, and Computer) and a faculty advisor.

Design and Verification of System on Chip, Fall 2021

Designed and synthesized a DDS (Direct Digital Synthesis) device capable of outputting a variable frequency sinusoidal or triangle waveform via LUT ROM modules. Made in Verilog using Quartus Prime on an FPGA board and verified using the SignalTap Logic Analyzer.

Embedded Systems, Spring 2021

Designed a pseudo car on an ARM-based microcontroller in C. Drives a motor based on the position of a potentiometer to simulate a gas pedal, and outputs information to an LCD to simulate a dashboard. Also capable of cruise control such that if the speed of the motor is changed the car will attempt to return to the set speed.

VLSI Design, Spring 2021

Design and synthesis of a 4-bit Ripple-Carry Adder with CMOS technology. Used Electric VLSI for design and LTSpice for simulation. The design started at the PMOS and NMOS network level to construct a 1-bit Adder, then used abstraction to build up from there. Made use of various Electric VLSI error detection tools: DRC (design rule check), NCC (network consistency check), and ERC (electrical rule check).

Introduction to Computer Architecture, Spring 2021

Paper design of an ARM LEGv8 processor. Project included creating a 5-stage datapath, control logic, and ALU such that the processor could support 9 operations.

Microcontrollers, Fall 2020

Created a traffic light controller on an ARM-based microcontroller in C. Capable of switching modes of operation (rural vs urban) and pedestrian crosswalk.

Electronics 1, Fall 2020

Design, tested, and compared three types of voltage rectifiers: Full-wave, Zener diode, and fixed voltage (7805 IC). Verification in PSpice, ElectricVLab, and CircuitLab.

Digital Systems Design, Fall 2020

Design and synthesis of a finite-state machine in Verilog using Quartus Prime on an FPGA board. This design took the form of a traffic light controller.

Software Engineering, Spring 2020

Started the design of an interactive circuit simulation software using Unreal Engine 4. Assisted a group who continued the project in Fall 2021.

Some projects have demo videos on my YouTube channel, Frank Seelmann
https://www.youtube.com/channel/UC64ecUkYQauZPHafvRddrTA/featured

LEADERSHIP & TEAMWORK

- Member of a team of 5 interdisciplinary engineers for the Senior Design project.
- Led a group of 4 for the Software Engineering Project.
- Co-founded High School Chess Club, Coding Club, and Science Club.