COMPUTER ARCHITECTURE SPRING 2013

MIDTERM EXAM

Time: 60 minutes

Total Points: 100%

Instructions:

1. Sign your name, student ID and solutions on your answer sheet.
2. Show all work. If you cannot finish a problem, your written work will help us to give you partial credit. (NOTE: You don't need to write pages of explanation; just be clear.)
3. Write legibly and clearly.
4. Work alone.
5. Read each question carefully before answering it. Try to solve the problems that seem easy before attacking the harder ones.

Problem 1: Performance and CPI. (20%)

1. Assume a typical program has the following instruction type:

30% loads

15% stores

50% adds

4% multiplies

1% divides

Assume the current-generation processor has the following instruction latencies:

loads: 2 cycles

stores: 6 cycles

adds: 1 cycles

multiplies: 14 cycles

divides: 50 cycles

What is the average CPI?

Solution:

$$CPI = \sum Freq_i * CPI_i = 30\% \times 2 + 15\% \times 6 + 50\% \times 1 + 4\% \times 14 + 1\% \times 15 = 3.06$$

Problem 2: Amdahl's Law (2*10% = 20%)

Speedup-overall = $\frac{1}{1-C+\frac{C}{\text{Speedup-enhanced}}}$

2. Suppose you have a machine which executes a program consisting of 50% floating point multiply, 20% floating point divide, and the remaining 30% are from other instructions.

(1) Management wants the machine to run 4 times faster. You can make the divide run at most 3 times faster and the multiply run at most 8 times faster. Can you meet management's goal by making only one improvement, and which one?

Solution: Amdahl's Law states: $speedup_{overall} = 1/((1-F)+F/speedup_{enhanced})$.

Speedup after improvement with Divide is:

$speedup_{divide} = \frac{1}{(1-20\%)+20\%/3} = 15/13 < 4$, The management's goal cannot be met by making the improvement with Divide alone.

Speedup after improvement with Divide is:

$speedup_{Multiply} = \frac{1}{(1-50\%)+50\%/8} = 16/9 < 4$, The management's goal cannot be met by making the improvement with Multiply alone either.

(2) If you make both the multiply and divide improvements, what is the speed of the improved machine?

Solution: $speedup_{overall} = \frac{1}{30\%+20\%/3+50\%/8} = 2.33$, we can see that The management's goal cannot be met. Actually, the speedup cannot exceed 1/30%=3.33.

Problem 3: pipeline speedup (2*10% =20%)

3. In this problem, we will explore how deepening the pipeline affects performance in two ways: faster clock cycle and increased stalls due to data and control hazards. Assume that the original machine is a 5-stage pipeline with a 1 ns clock cycle. The second machine is a 12-stage pipeline with a 0.6 ns clock cycle. The 5-stage pipeline experiences 2 stall due to data hazard every **7** instructions, whereas the 12-stage pipeline experiences **5** stalls every **9** instructions. In addition, branches constitute 20% of the instructions, and the misprediction rate for both machines is 5%.

(1) What is the speedup of the 12-stage pipeline over the 5-stage pipeline, taking into account only data hazards?

Solution: Let I be the number of instructions, Execution Time = I ×CPI ×Cycle Speedup = (I ×9/7×1)/(I ×14/9 ×0.6) = 1.38.

(2) If the branch mispredict penalty for the first machine is 2 cycles but the second machine is 5 cycles, what are the CPIs of each, taking into account the stalls due to

branch mispredictions?

Solution: the CPI of 5-stage is $CPI_{5-stage} = 9/7 + 0.20 \times 5\% \times 2 = 1.31$. the CPI of 12-stage is $CPI_{12-stage} = 14/9 + 0.20 \times 5\% \times 5 = 1.61$.

Problem 4: pipeline hazards (4*10%=40%)

4. Consider the following code, answer the questions:

```
.text
1: Loop:    MOV R3, R7      ;   move R7 to R3
2:          LD R8, 0(R3)
3:          DADDI R3, R3, 4
4:          LD R9, 0(R3)
5:          BNE R8, R9, Loop
6: end:     halt
```

(1) What is the difference between a dependence and hazard?

Solution: Dependencies are properties of programs. Whether a given dependency results in an actual hazard being detected and whether that hazard actually causes a stall are properties of the pipeline organization.

(2) What is the difference between a name dependence and a true dependence?

Solution: Name dependence occurs when two instructions use the same register or memory location, but there is no flow of data between these two instructions. A true (data) dependence occurs between two instruction (i, j) when instruction i produces as result that may be used by instruction j.

(3) Which of WAW, RAW, WAR are true dependencies and which are name dependencies?

Solution: RAW: true dependence; WAW, WAR: name dependence.

(4) List all of the dependencies in each loop above by describing where the dependencies occur, on which registers, and the kind of dependency.

Solution: The dependencies list as follow:

order	Dependency pair	register	kind
A	1 vs. 2	R3	RAW
B	1 vs. 3	R3	RAW

C	2 vs. 5	R8	RAW
D	3 vs. 4	R3	RAW
E	4 vs. 5	R9	RAW
F	1 vs. 3	R3	WAW
G	2 vs. 3	R3	WAR