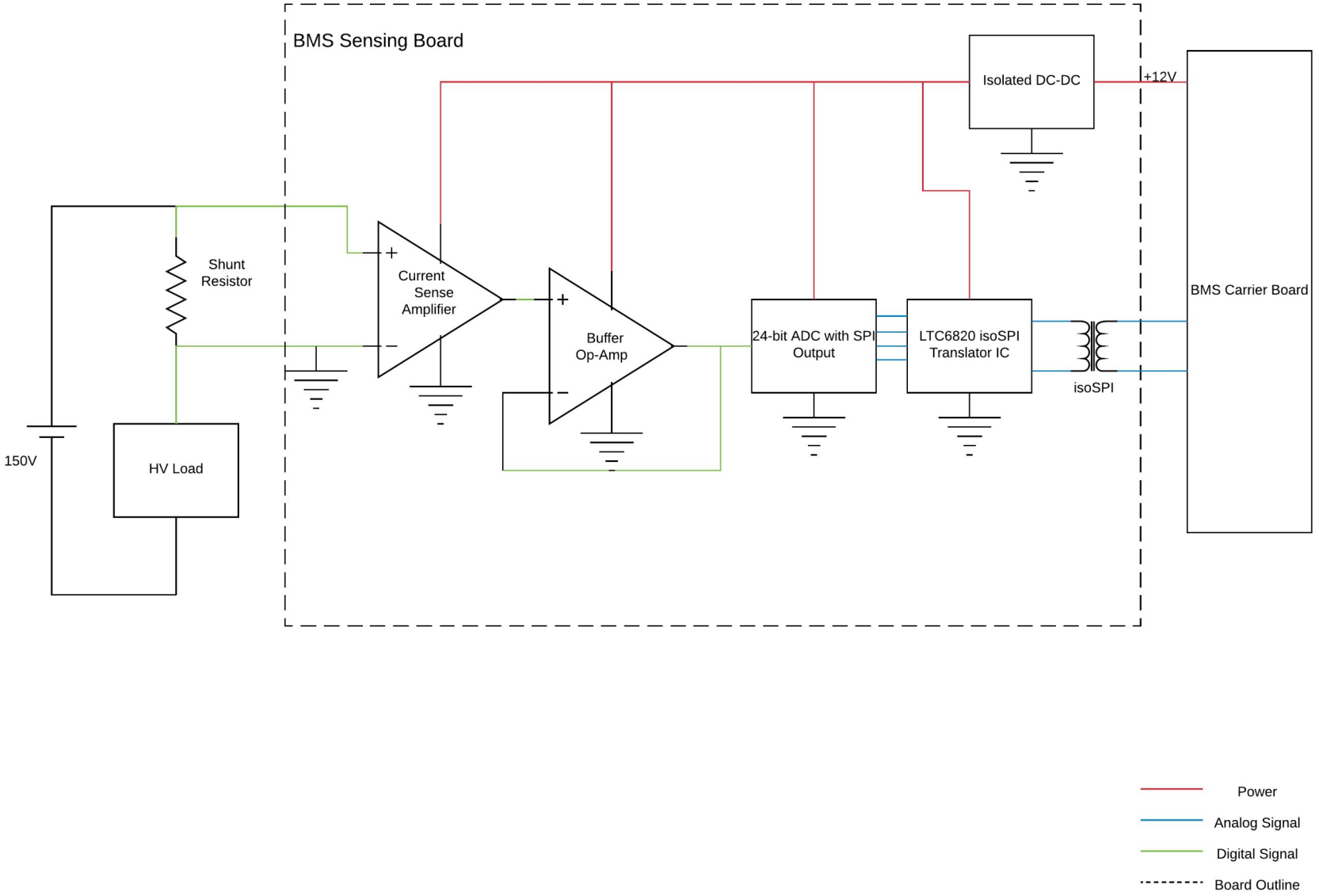
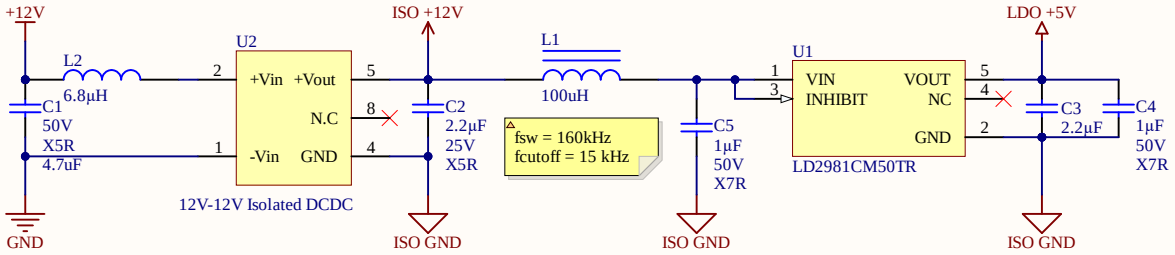
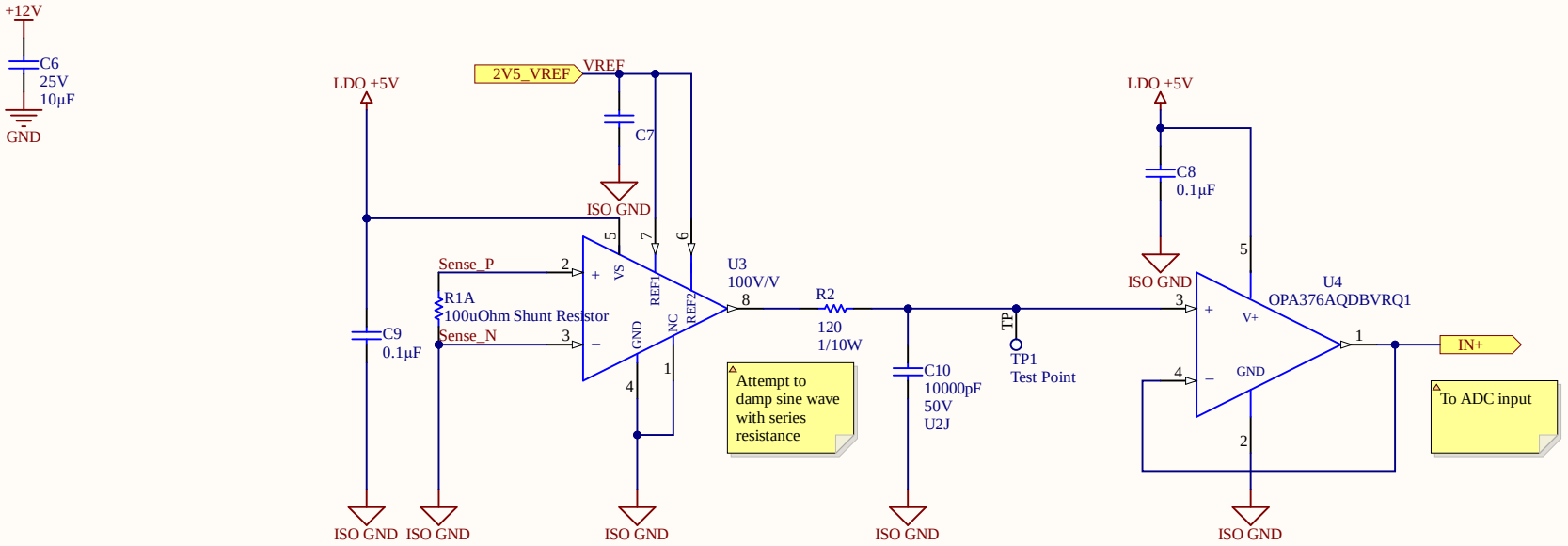


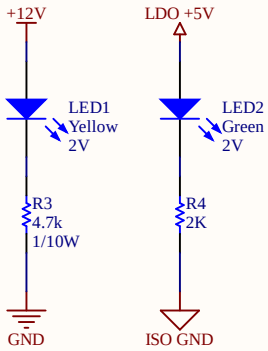
Last Updated: Oct 29, 2017

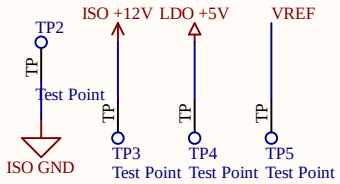
Project: ***BMS_Current_Sense.PrjPcb***		MIDNIGHT SUN
Title: **BMS Current Sense Block Diagram**		
Project Lead: Liam Hawkins		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.1	
Date: 2019-11-30	Sheet 1 of 3	Website: www.uwmidsun.com





Using the internal resistor divider (Fig 29 of INA240 Datasheet, Oct 2016) to get the mid voltage point of the 4.096V reference. Isense = 0 when Vout = Vref/2





Project:	***BMS_Current_Sense.PrjPcb***	
Title:	**BMS Current Sense Board**	
Project Lead:	Liam Hawkins	
Size:	Letter	Revision: 1.1
Date:	2019-11-30	Sheet 2 of 3

MIDNIGHT SUN

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Waterloo, ON, Canada
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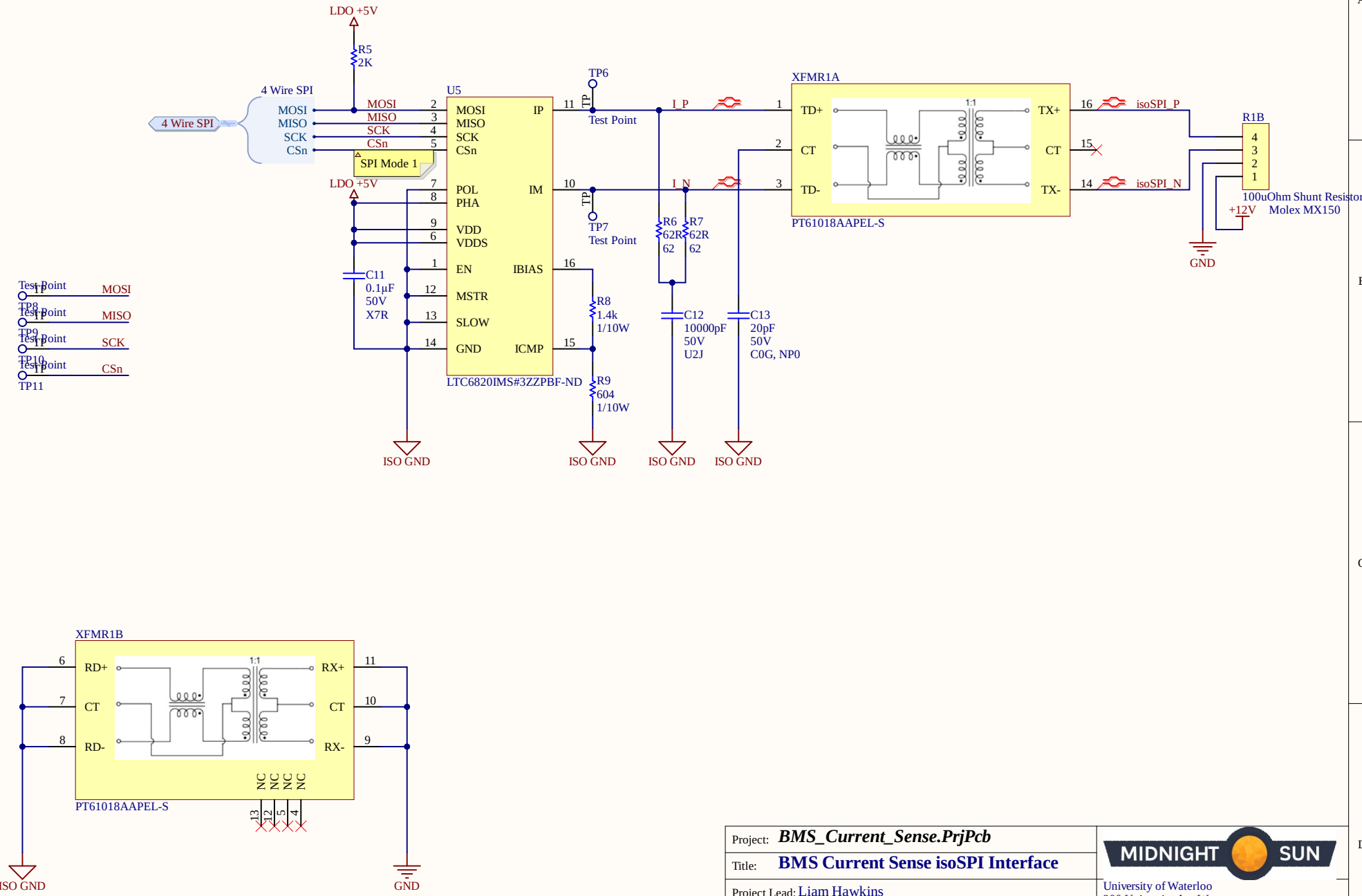
Website: www.uwmidsun.com



Project: *BMS_Current_Sense.PrjPcb*		MIDNIGHT SUN
Title: **BMS Current Sense isoSPI Interface**		
Project Lead: Liam Hawkins		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.1	
Date: 2019-11-30	Sheet 3 of 3	Website: www.uwmidsun.com

RESET/PWDN Pin

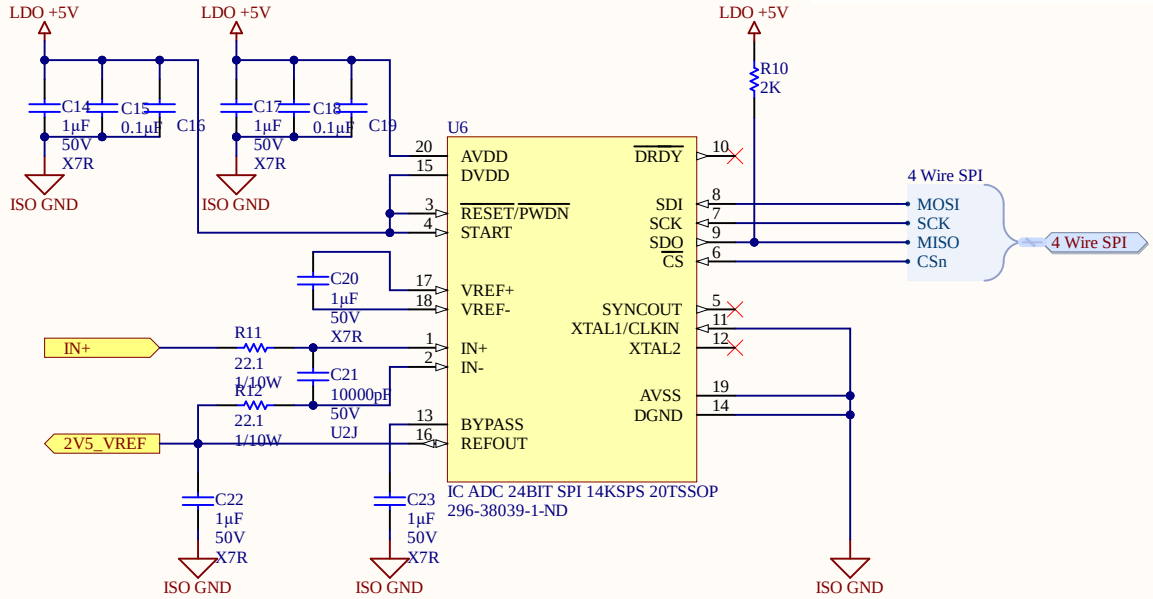
This pin must be high in normal operation. If it is desired to completely power down the device, or to have a hardware reset control, then connect this pin to a controller. If these functions are not needed, tie the pin high. (Note that the device can both be reset and SLEEP mode engaged by commands.)

START Pin

If it is desired to control conversions by pin, connect this line to the controller. Otherwise, this line can be tied high to free-run conversions. The conversions can also be controlled by software commands. In this case, tie the START pin low.

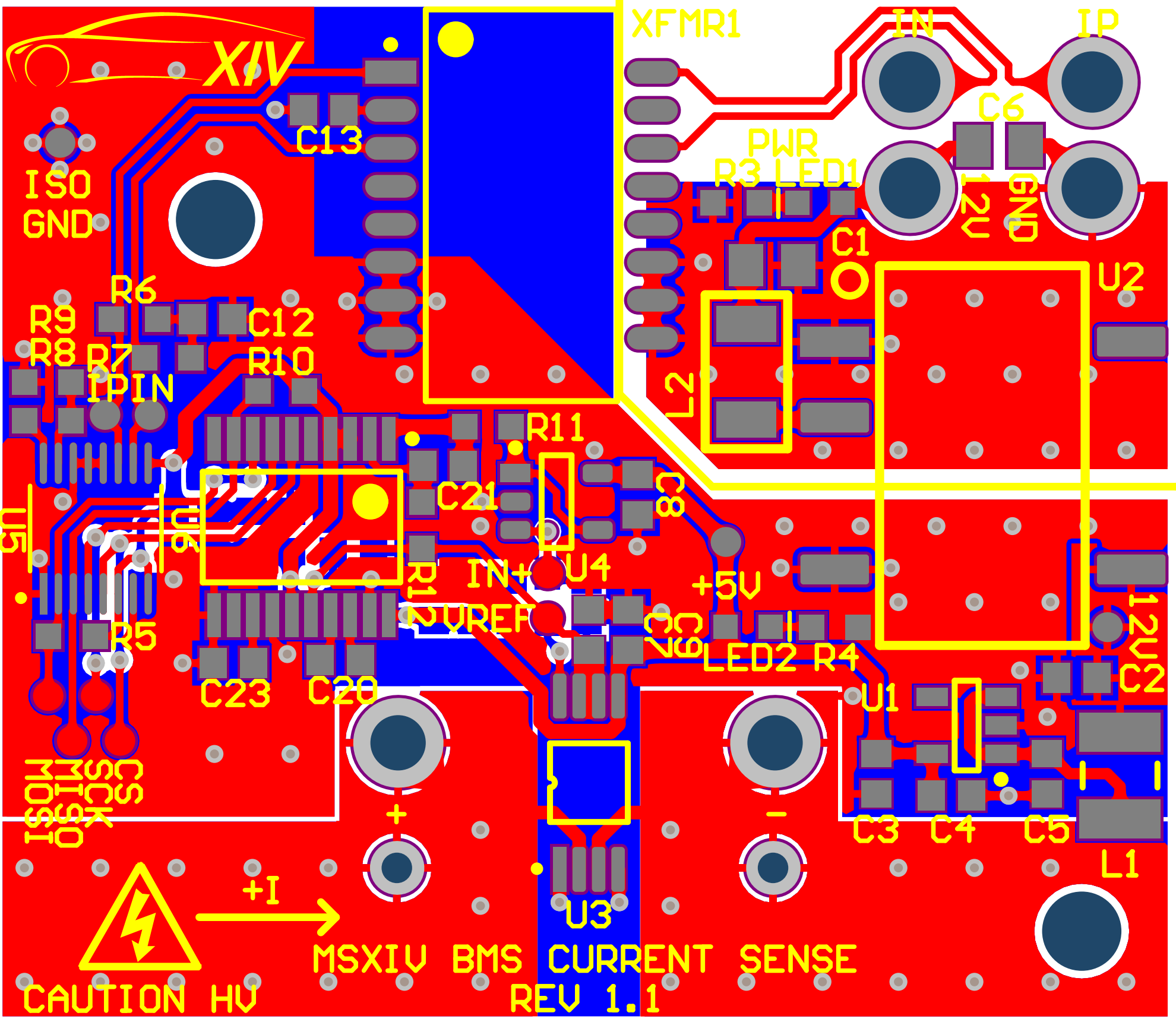
DRDY Pin

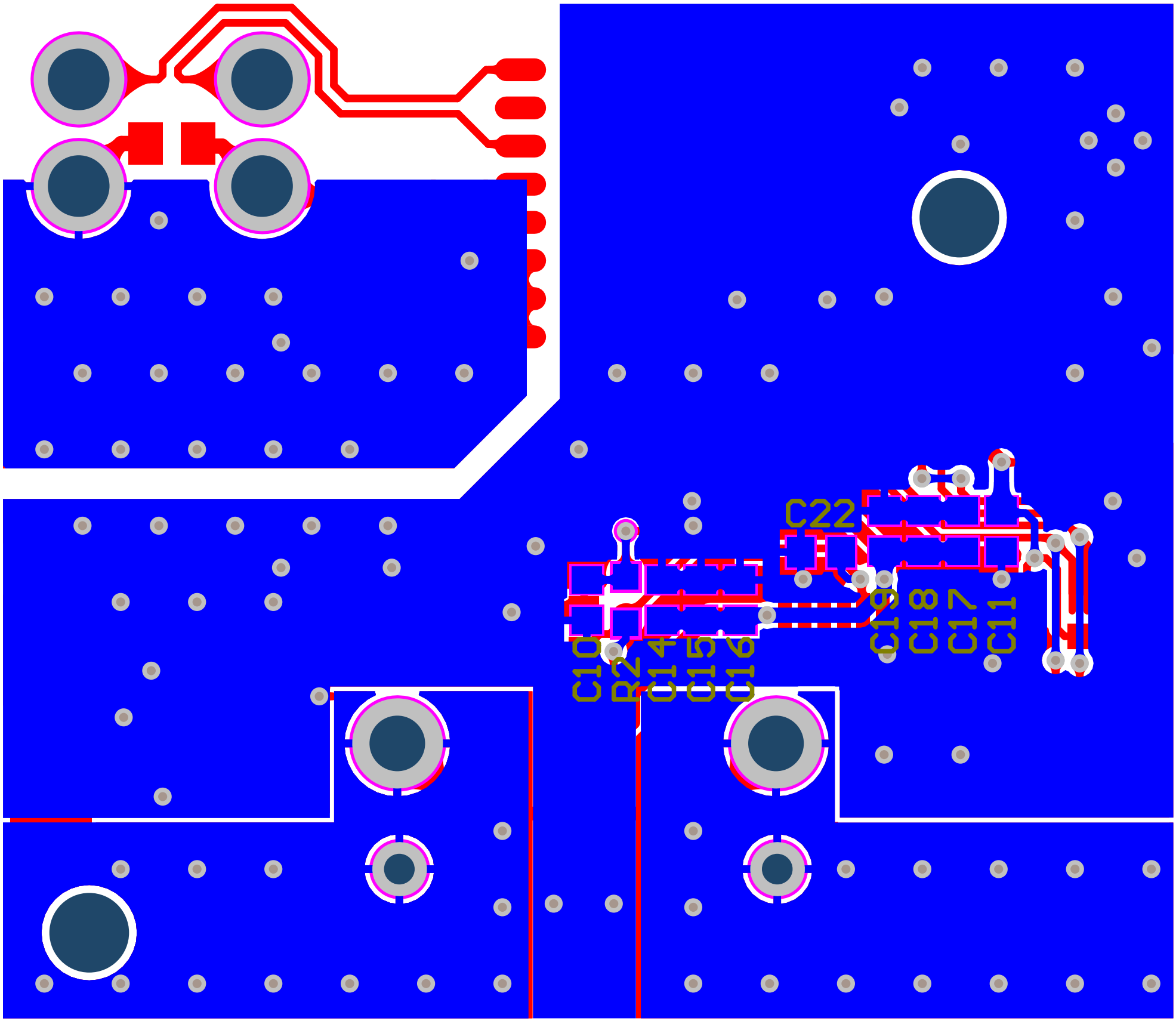
DRDY is an output that indicates when data are ready for readback. Note that the DOUT pin (and also the DRDY register bit) indicates when data are ready as well, so DRDY connection to a controller is optional.

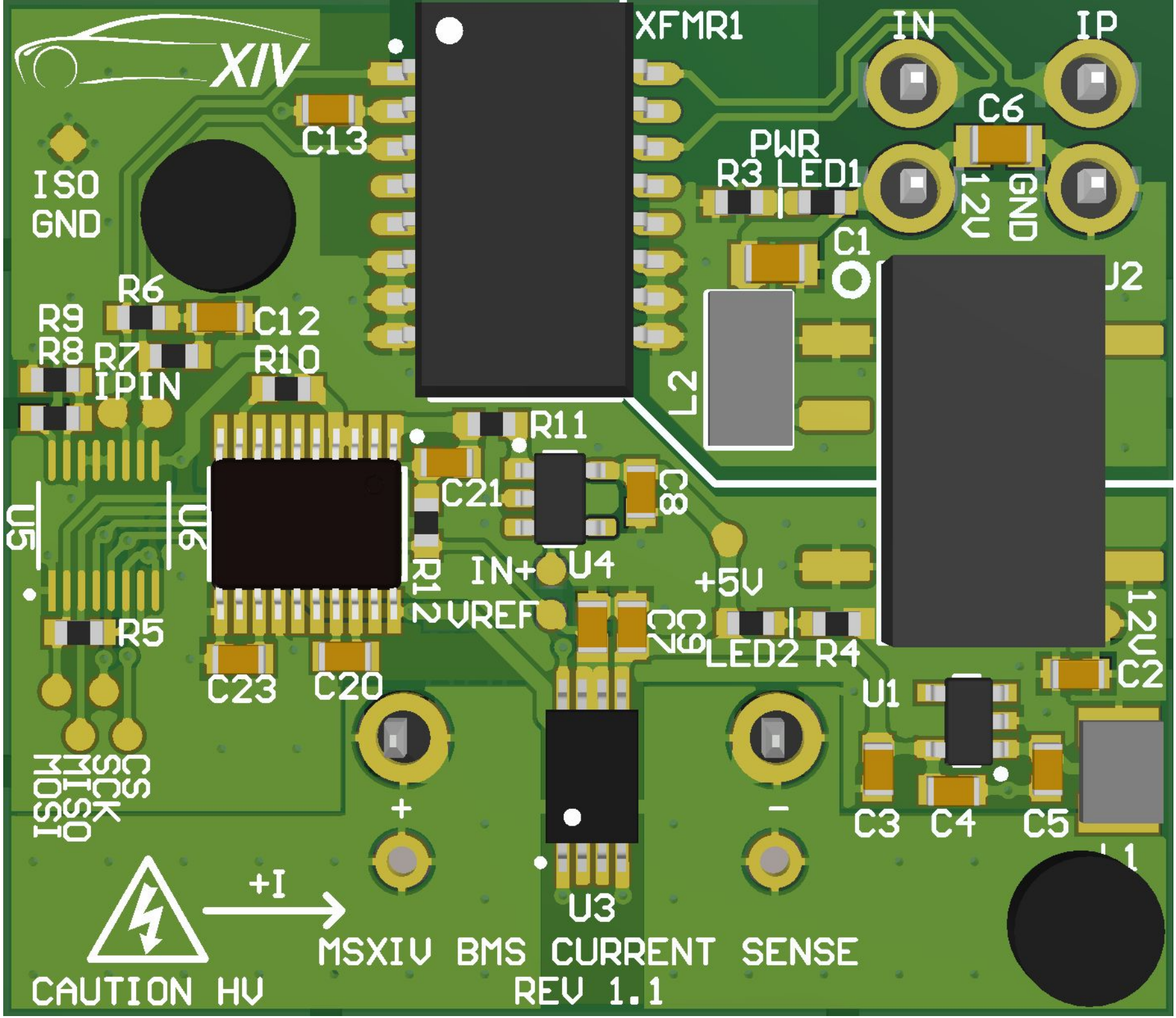


Title		
Size: A	Number	Revision
Date: 11-30-2019		Sheet of
File: C:\Users\..\ADC_Circuit.SchDoc		Drawn By:

Comment	Description	Designator	Footprint	LibRef	Quantity
CAP CER 4.7UF 50V 10% X5R 0805	4.7µF ±20% 50V Ceramic Capacitor X5R 0805 (2012 Metric)	C1	CAP, 0805	CAP CER 4.7UF 50V 10% X5R 0805	1
CAP CER 2.2UF 25V 10% X5R 0603	2.2µF ±10% 25V Ceramic Capacitor X5R 0603 (1608 Metric)	C2	CAP, 0603	CAP CER 2.2UF 25V 10% X5R 0603	1
CAP CER 2.2UF 25V 10% X5R 0603	2.2µF ±10% 25V Ceramic Capacitor X5R 0603 (1608 Metric)	C3	CAP, 0603	CAP CER 2.2UF 25V 10% X5R 0603	1
CAP CER 1UF 50V 10% X7R 0603	1µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C4	CAP, 0603	CAP CER 1UF 50V 10% X7R 0603	1
CAP CER 1UF 50V 10% X7R 0603	1µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C5	CAP, 0603	CAP CER 1UF 50V 10% X7R 0603	1
CAP CER 10uF 25V 10% X5R 0805	10µF ±10% 25V Ceramic Capacitor X5R 0805 (2012 Metric)	C6	CAP, 0805	CAP CER 10uF 25V 10% X5R 0805	1
CAP CER 0.022UF 50V 10% X7R 0603	0.022µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C7	CAP, 0603	CAP CER 0.022UF 50V 10% X7R 0603	1
CAP CER 0.1UF 50V 10% X7R 0603	0.1µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C8	CAP, 0603	CAP CER 0.1UF 50V 10% X7R 0603	1
CAP CER 0.1UF 50V 10% X7R 0603	0.1µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C9	CAP, 0603	CAP CER 0.1UF 50V 10% X7R 0603	1
CAP CER 10nF 50V 5% X7R 0603	10000pF ±5% 50V Ceramic Capacitor (Z) 0603 (1608 Metric)	C10	CAP, 0603	CAP CER 10nF 50V 5% X7R 0603	1
CAP CER 0.1UF 50V 10% X7R 0603	0.1µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C11	CAP, 0603	CAP CER 0.1UF 50V 10% X7R 0603	1
CAP CER 10nF 50V 5% X7R 0603	10000pF ±5% 50V Ceramic Capacitor (Z) 0603 (1608 Metric)	C12	CAP, 0603	CAP CER 10nF 50V 5% X7R 0603	1
CAP CER 20PF 50V ±5% C0G/NP0 0603	20pF ±5% 50V Ceramic Capacitor C0G, NP0 0603 (1608 Metric)	C13	CAP, 0603	CAP CER 20PF 50V ±5% C0G/NP0 0603	1
CAP CER 1UF 50V 10% X7R 0603	1µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C14	CAP, 0603	CAP CER 1UF 50V 10% X7R 0603	1
CAP CER 0.1UF 50V 10% X7R 0603	0.1µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C15	CAP, 0603	CAP CER 0.1UF 50V 10% X7R 0603	1
CAP CER 0.022UF 50V 10% X7R 0603	0.022µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C16	CAP, 0603	CAP CER 0.022UF 50V 10% X7R 0603	1
CAP CER 1UF 50V 10% X7R 0603	1µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C17	CAP, 0603	CAP CER 1UF 50V 10% X7R 0603	1
CAP CER 0.1UF 50V 10% X7R 0603	0.1µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C18	CAP, 0603	CAP CER 0.1UF 50V 10% X7R 0603	1
CAP CER 0.022UF 50V 10% X7R 0603	0.022µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C19	CAP, 0603	CAP CER 0.022UF 50V 10% X7R 0603	1
CAP CER 1UF 50V 10% X7R 0603	1µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C20	CAP, 0603	CAP CER 1UF 50V 10% X7R 0603	1
CAP CER 10nF 50V 5% X7R 0603	10000pF ±5% 50V Ceramic Capacitor (Z) 0603 (1608 Metric)	C21	CAP, 0603	CAP CER 10nF 50V 5% X7R 0603	1
CAP CER 1UF 50V 10% X7R 0603	1µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C22	CAP, 0603	CAP CER 1UF 50V 10% X7R 0603	1
CAP CER 1UF 50V 10% X7R 0603	1µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C23	CAP, 0603	CAP CER 1UF 50V 10% X7R 0603	1
IND 100uH 60mA 5% 1210	100µH Unshielded Wirewound Inductor 60mA 11 Ohm Max 1210 (3225 Metric)	L1	1210	IND 100uH 60mA 5% 1210	1
IND 6.8uH 260mA 20% 1210	6.8µH Shielded Wirewound Inductor 260mA 204 mOhm Max 1210 (3225 Metric)	L2	NLFV32T-6R8M-EF/IND 6.8uH	IND 6.8uH 260mA 20% 1210	1
LED YELLOW CLEAR 2.1V 0603	Yellow 590nm LED Indication - Discrete 2V 0603 (1608 Metric)	LED1	LED_0603	LED YELLOW CLEAR 2.1V 0603	1
LED GREEN CLEAR 2V 0603	Green 572nm LED Indication - Discrete 2V 0603 (1608 Metric)	LED2	LED_0603	LED GREEN CLEAR 2V 0603	1
100uOhm Shunt Resistor	100 µOhms ±5% 36W Shunt, Battery Specialized Resistor Metal Element ±175ppm/°C Shunt Fixture, 60mm Pitch	R1	RES SHUNT 100UOHM 60MM	RES SHUNT 100UOHM 5% 36W 60MM	1
RES 120 OHM 1% 1/10W 0603	RES SMD 120 OHM 1% 1/10W 0603	R2	RES, 0603	RES 120 OHM 1% 1/10W 0603	1
RES 4.7K OHM 1% 1/10W 0603	4.7k Ohm ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	R3	RES, 0603	RES 4.7K OHM 1% 1/10W 0603	1
2K	2k Ohm ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	R4	RES, 0603	RES 2K OHM 1% 1/10W 0603	1
2K	2k Ohm ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	R5	RES, 0603	RES 2K OHM 1% 1/10W 0603	1
62R	62 Ohms ±0.1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thin Film	R6	RES, 0603	RES 62 OHM 0.1% 1/10W 0603	1
62R	62 Ohms ±0.1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thin Film	R7	RES, 0603	RES 62 OHM 0.1% 1/10W 0603	1
RES 1.4k OHM 1% 1/10W 0603	RES SMD 1.4K OHM 1% 1/10W 0603	R8	RES, 0603	RES 1.4k OHM 1% 1/10W 0603	1
RES 604 OHM 1% 1/10W 0603	RES SMD 604 OHM 1% 1/10W 0603	R9	RES, 0603	RES 604 OHM 1% 1/10W 0603	1
2K	2k Ohm ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	R10	RES, 0603	RES 2K OHM 1% 1/10W 0603	1
RES 22.1 OHM 1% 1/10W 0603	22.1 Ohm ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	R11	RES, 0603	RES 22.1 OHM 1% 1/10W 0603	1
RES 22.1 OHM 1% 1/10W 0603	22.1 Ohm ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	R12	RES, 0603	RES 22.1 OHM 1% 1/10W 0603	1
IC REG LDO 5V 0.1A SOT23-5	Linear Voltage Regulator IC Positive, Fixed Output 5V 105mA SOT-23-5	U1	SOT95P280X145-5N	IC REG LDO 5V 0.1A SOT23-5	1
IC DCDC ISOLATED 12V 1W 8-SMD 5-LEAD	Isolated Module DC DC Converter 1 Output 12V 84mA 10.8V - 13.2V Input	U2	IC, Isolated DCDC	IC DCDC ISOLATED 12V 1W 8-SMD 5-LEAD	1
100V IV	Current Sense Amplifier 1 Circuit 8-TSSOP	U3	IC CURRENT AMPLIFIER INA240 TSSOP-8	IC CURRENT AMPLIFIER INA240 8-TSSOP	1
IC OP AMP GEN PURPOSE RR 5.5MHZ SOT-23-5	General Purpose Amplifier 1 Circuit Rail-to-Rail SOT-23-5	U4	IC OP AMP GP RR 10MHZ SOT-23-5	IC OP AMP GEN PURPOSE RR 5.5MHZ SOT-23-5	1
IC ISOSPI COMM INTERFACE 1.7036520/MSK3229SF	Isolated Communications Interface Interface 16-MSOP	U5	IC isoSPI Interface 1.7036520 MSOP	IC ISOSPI COMM INTERFACE 1.7036520/MSK3229SF	1
IC ADC 24BIT SPI 14KSPS 20TSSOP	24 Bit Analog to Digital Converter 1 Input 1 Sigma-Delta 20-TSSOP	U6	TSSOP65P640X120-20N	IC ADC 24BIT SPI 14KSPS 20TSSOP	1
IC PULSE XFMR 1CT:1CT 350UH SMD	PULSE XFMR 1CT:1CT 350UH SMD	XFMR1	IC, PULSE XFMR 1CT:1CT 350UH SMD	IC PULSE XFMR 1CT:1CT 350UH SMD	1


XIV
XFMR1
IN
IP
C6
PWR
R3 LED1
12V
GND
C13
ISO
GND
C1
U2
R6
R9
R8
R7
IPIN
C12
R10
L2
R11
C21
C8
U5
U6
R12
IN+
U4
+5V
VREF
C7
C9
LED2 R4
12V
C2
R5
C23
C20
U1
MOSI
MISO
SCK
CS
+
-
C3
C4
C5
L1
+I
U3
MSXIV BMS CURRENT SENSE
REV 1.1
CAUTION HV


C22
C10
R2
C14
C15
C16
C19
C18
C17
C11


XIV
XFMR1
IN
IP
C6
C13
PWR
R3 LED1
12V
GND
ISO
GND
C1
U2
R6
R9
C12
R8
R7
R10
IPIN
L2
R11
C21
C8
U5
U6
R12
IN+
U4
+5V
VREF
C7
C9
LED2
R4
12V
R5
C23
C20
C2
U1
MOSI
MISO
SCK
CS
+
-
C3
C4
C5
+I
U3
MSXIV BMS CURRENT SENSE
REV 1.1
CAUTION HV

Electrical Rules Check Report

Class	Document	Message
Warning	ADC_Circuit.SchDoc	Net CSn has no driving source (Pin TP11-TP, Pin U5-5, Pin U6-6)
Warning	ADC_Circuit.SchDoc	Net MOSI has no driving source (Pin R5-2, Pin TP8-TP, Pin U5-2, Pin U6-8)
Warning	BMS_Current_Sense.SchDoc	Net NetC10_1 has no driving source (Pin C10-1, Pin R2-2, Pin TP1-TP, Pin U4-3)
Warning	ADC_Circuit.SchDoc	Net NetC20_1 has no driving source (Pin C20-1, Pin U6-17)
Warning	ADC_Circuit.SchDoc	Net NetC20_2 has no driving source (Pin C20-2, Pin U6-18)
Warning	ADC_Circuit.SchDoc	Net NetC21_1 has no driving source (Pin C21-1, Pin R11-2, Pin U6-1)
Warning	ADC_Circuit.SchDoc	Net NetC21_2 has no driving source (Pin C21-2, Pin R12-2, Pin U6-2)
Warning	ADC_Circuit.SchDoc	Net SCK has no driving source (Pin TP10-TP, Pin U5-4, Pin U6-7)
Warning	BMS_Current_Sense.SchDoc	Net Sense_2_P has no driving source (Pin R1-5, Pin U3-2)
Warning	ADC_Circuit.SchDoc	NetC22_1 contains IO Pin and Output Port objects (Pin U6-16, Port 2V5_VREF).
Warning	BMS_Current_Sense.SchDoc	Nets Wire Sense_N has multiple names (Net Label Sense_N, Power Object ISO GND, Power Object ISO GND, Power Object ISO GND

Design Rules Verification Report

Filename : C:\Users\Midnight Sun\Documents\Midnight Sun\hardware\MSXIV_BMS_Curre

Warnings 0
Rule Violations 231

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Clearance Constraint (Gap=0.254mm) (InComponent('R1')),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=1.27mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	2
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	72
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	132
Silk to Silk (Clearance=0.254mm) (All),(All)	25
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	231

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (2.65mm > 2.54mm) Pad R1-0(36.353mm,3.133mm) on Multi-Layer Actual Hole Size = 2.65mm
Hole Size Constraint: (2.65mm > 2.54mm) Pad R1-0(7.403mm,26.933mm) on Multi-Layer Actual Hole Size = 2.65mm

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C10-1(19.8mm,14.875mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C10-2(19.8mm,13.525mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C11-1(6mm,17.175mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C11-2(6mm,15.825mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad C12-1(6.625mm,23.6mm) on Top Layer And Pad R6-2(5.475mm,23.6mm)
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C12-1(6.625mm,23.6mm) on Top Layer And Pad R7-2(6.575mm,22.3mm)
Minimum Solder Mask Sliver Constraint: (0.21mm < 0.254mm) Between Pad C13-1(11.7mm,30.6mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.076mm < 0.254mm) Between Pad C13-1(11.7mm,30.6mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C14-1(17.3mm,13.525mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad C14-1(17.3mm,13.525mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C14-2(17.3mm,14.875mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad C14-2(17.3mm,14.875mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C15-1(16mm,13.525mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C15-2(16mm,14.875mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C17-1(7.3mm,15.825mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C17-2(7.3mm,17.175mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C18-1(8.6mm,15.825mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C18-2(8.6mm,17.175mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.137mm < 0.254mm) Between Pad C20-1(10.9mm,12.2mm) on Top Layer And Pad U6-15(9.95mm,13.7mm)
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad C20-1(10.9mm,12.2mm) on Top Layer And Pad U6-16(10.6mm,13.7mm)
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad C20-1(10.9mm,12.2mm) on Top Layer And Pad U6-17(11.25mm,13.7mm)
Minimum Solder Mask Sliver Constraint: (0.176mm < 0.254mm) Between Pad C20-1(10.9mm,12.2mm) on Top Layer And Pad U6-18(11.9mm,13.7mm)
Minimum Solder Mask Sliver Constraint: (0.176mm < 0.254mm) Between Pad C20-2(12.25mm,12.2mm) on Top Layer And Pad U6-17(11.25mm,13.7mm)
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad C20-2(12.25mm,12.2mm) on Top Layer And Pad U6-18(11.9mm,13.7mm)
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad C20-2(12.25mm,12.2mm) on Top Layer And Pad U6-19(12.55mm,13.7mm)
Minimum Solder Mask Sliver Constraint: (0.137mm < 0.254mm) Between Pad C20-2(12.25mm,12.2mm) on Top Layer And Pad U6-20(13.2mm,13.7mm)
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C21-1(15.675mm,18.7mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.254mm) Between Pad C21-2(14.325mm,18.7mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C23-1(8.675mm,12.1mm) on Top Layer And Pad U6-12(8mm,13.7mm) on
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C23-1(8.675mm,12.1mm) on Top Layer And Pad U6-13(8.65mm,13.7mm)
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C23-1(8.675mm,12.1mm) on Top Layer And Pad U6-14(9.3mm,13.7mm)
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C23-2(7.325mm,12.1mm) on Top Layer And Pad U6-11(7.35mm,13.7mm)
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C23-2(7.325mm,12.1mm) on Top Layer And Pad U6-12(8mm,13.7mm) on
Minimum Solder Mask Sliver Constraint: (0.067mm < 0.254mm) Between Pad C6-2(34.475mm,29.4mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.159mm < 0.254mm) Between Pad C7-1(19.888mm,12.525mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.242mm < 0.254mm) Between Pad C7-1(19.888mm,12.525mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad C7-1(19.888mm,12.525mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad C7-1(19.888mm,12.525mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.251mm < 0.254mm) Between Pad C7-1(19.888mm,12.525mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.159mm < 0.254mm) Between Pad C7-2(19.888mm,13.875mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.21mm < 0.254mm) Between Pad C7-2(19.888mm,13.875mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad C8-1(21.5mm,18.4mm) on Top Layer And Pad U4-5(20.175mm,18.45mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad C8-2(21.5mm,17.05mm) on Top Layer And Pad U4-4(20.175mm,16.55mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad C9-1(21.2mm,12.525mm) on Top Layer And Pad U3-5(20.856mm,11mm)
Minimum Solder Mask Sliver Constraint: (0.227mm < 0.254mm) Between Pad IP-TP(3.7mm,20.4mm) on Top Layer And Pad R9-1(2.575mm,21.5mm) on
Minimum Solder Mask Sliver Constraint: (0.15mm < 0.254mm) Between Pad LED1-1(28.35mm,27.49mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad LED1-2(26.85mm,27.49mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.254mm) Between Pad R10-1(10.375mm,21.2mm) on Top Layer And Pad U6-4(11.25mm,19.6mm)
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-1(10.375mm,21.2mm) on Top Layer And Pad U6-5(10.6mm,19.6mm)
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-1(10.375mm,21.2mm) on Top Layer And Pad U6-6(9.95mm,19.6mm)
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-2(8.825mm,21.2mm) on Top Layer And Pad U6-7(9.3mm,19.6mm) on
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-2(8.825mm,21.2mm) on Top Layer And Pad U6-8(8.65mm,19.6mm)

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-2(8.825mm,21.2mm) on Top Layer And Pad U6-9(8mm,19.6mm) on
Minimum Solder Mask Sliver Constraint: (0.254mm < 0.254mm) Between Pad R5-1(3.375mm,13mm) on Top Layer And Pad U5-3(2.649mm,14.416mm)
Minimum Solder Mask Sliver Constraint: (0.196mm < 0.254mm) Between Pad R5-1(3.375mm,13mm) on Top Layer And Pad U5-4(3.15mm,14.416mm) on
Minimum Solder Mask Sliver Constraint: (0.196mm < 0.254mm) Between Pad R5-1(3.375mm,13mm) on Top Layer And Pad U5-5(3.65mm,14.416mm) on
Minimum Solder Mask Sliver Constraint: (0.196mm < 0.254mm) Between Pad R5-2(1.825mm,13mm) on Top Layer And Pad U5-1(1.649mm,14.416mm)
Minimum Solder Mask Sliver Constraint: (0.196mm < 0.254mm) Between Pad R5-2(1.825mm,13mm) on Top Layer And Pad U5-2(2.149mm,14.416mm)
Minimum Solder Mask Sliver Constraint: (0.251mm < 0.254mm) Between Pad R6-1(3.925mm,23.6mm) on Top Layer And Pad R7-1(5.025mm,22.3mm)
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R6-2(5.475mm,23.6mm) on Top Layer And Pad R7-1(5.025mm,22.3mm)
Minimum Solder Mask Sliver Constraint: (0.251mm < 0.254mm) Between Pad R6-2(5.475mm,23.6mm) on Top Layer And Pad R7-2(6.575mm,22.3mm)
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R8-1(1.025mm,20.2mm) on Top Layer And Pad R9-2(1.025mm,21.5mm)
Minimum Solder Mask Sliver Constraint: (0.211mm < 0.254mm) Between Pad R8-1(1.025mm,20.2mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R8-2(2.575mm,20.2mm) on Top Layer And Pad R9-1(2.575mm,21.5mm)
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm) Between Pad R8-2(2.575mm,20.2mm) on Top Layer And Pad U5-13(3.15mm,18.784mm)
Minimum Solder Mask Sliver Constraint: (0.196mm < 0.254mm) Between Pad R8-2(2.575mm,20.2mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.196mm < 0.254mm) Between Pad R8-2(2.575mm,20.2mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U1-1(33.655mm,9.06mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U1-2(33.655mm,10.01mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U4-1(17.425mm,18.45mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U4-2(17.425mm,17.5mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.079mm < 0.254mm) Between Pad U4-3(17.425mm,16.55mm) on Top Layer And Via (18.5mm,16.5mm) from

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Arc (13.975mm,19.6mm) on Top Overlay And Pad C21-2(14.325mm,18.7mm)
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.254mm) Between Arc (17.425mm,19.3mm) on Top Overlay And Pad R11-1(17.275mm,20mm)
Silk To Solder Mask Clearance Constraint: (0.101mm < 0.254mm) Between Pad C10-2(19.8mm,13.525mm) on Bottom Layer And Text "C10"
Silk To Solder Mask Clearance Constraint: (0.132mm < 0.254mm) Between Pad C1-1(25.125mm,25.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.132mm < 0.254mm) Between Pad C1-2(26.875mm,25.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.132mm < 0.254mm) Between Pad C1-2(26.875mm,25.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad C12-2(7.975mm,23.6mm) on Top Layer And Text "C12" (8.6mm,23.1mm)
Silk To Solder Mask Clearance Constraint: (0.056mm < 0.254mm) Between Pad C13-1(11.7mm,30.6mm) on Top Layer And Text "C13"
Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C13-2(10.35mm,30.6mm) on Top Layer And Text "C13"
Silk To Solder Mask Clearance Constraint: (0.101mm < 0.254mm) Between Pad C14-1(17.3mm,13.525mm) on Bottom Layer And Text "C14"
Silk To Solder Mask Clearance Constraint: (0.101mm < 0.254mm) Between Pad C15-1(16mm,13.525mm) on Bottom Layer And Text "C15"
Silk To Solder Mask Clearance Constraint: (0.101mm < 0.254mm) Between Pad C16-1(14.7mm,13.525mm) on Bottom Layer And Text "C16"
Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C20-1(10.9mm,12.2mm) on Top Layer And Text "C20"
Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C20-2(12.25mm,12.2mm) on Top Layer And Text "C20"
Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C21-1(15.675mm,18.7mm) on Top Layer And Text "C21"
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad C21-2(14.325mm,18.7mm) on Top Layer And Text "C21"
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C21-2(14.325mm,18.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C21-2(14.325mm,18.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C23-1(8.675mm,12.1mm) on Top Layer And Text "C23" (7mm,10.7mm)
Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C23-2(7.325mm,12.1mm) on Top Layer And Text "C23" (7mm,10.7mm)
Silk To Solder Mask Clearance Constraint: (0.243mm < 0.254mm) Between Pad C3-2(29.489mm,7.725mm) on Top Layer And Text "C3"
Silk To Solder Mask Clearance Constraint: (0.132mm < 0.254mm) Between Pad C4-1(31.329mm,7.663mm) on Top Layer And Text "C4"
Silk To Solder Mask Clearance Constraint: (0.132mm < 0.254mm) Between Pad C4-2(32.679mm,7.663mm) on Top Layer And Text "C4"
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad C4-2(32.679mm,7.663mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad C4-2(32.679mm,7.663mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.243mm < 0.254mm) Between Pad C5-2(35.179mm,7.725mm) on Top Layer And Text "C5"
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad C6-1(32.725mm,29.4mm) on Top Layer And Text "12V"
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad C6-1(32.725mm,29.4mm) on Top Layer And Text "C6" (33mm,30.3mm)
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad C6-2(34.475mm,29.4mm) on Top Layer And Text "C6" (33mm,30.3mm)
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad C6-2(34.475mm,29.4mm) on Top Layer And Text "GND"
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad C8-1(21.5mm,18.4mm) on Top Layer And Text "C8" (22.2mm,18.4mm)
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad C8-2(21.5mm,17.05mm) on Top Layer And Text "C8" (22.2mm,18.4mm)
Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C9-1(21.2mm,12.525mm) on Top Layer And Text "C7"
Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C9-2(21.2mm,13.875mm) on Top Layer And Text "C7"
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad CS-TP(4.2mm,9.5mm) on Top Layer And Text "CS" (4.1mm,8.8mm) on
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad CS-TP(4.2mm,9.5mm) on Top Layer And Text "SCK" (3.1mm,8.8mm) on
Silk To Solder Mask Clearance Constraint: (0.205mm < 0.254mm) Between Pad IN+-TP(18.5mm,15.1mm) on Top Layer And Text "IN+"
Silk To Solder Mask Clearance Constraint: (0.182mm < 0.254mm) Between Pad IN+-TP(18.5mm,15.1mm) on Top Layer And Text "U4"
Silk To Solder Mask Clearance Constraint: (0.253mm < 0.254mm) Between Pad IN+-TP(18.5mm,15.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.031mm < 0.254mm) Between Pad IN-TP(5.2mm,20.4mm) on Top Layer And Text "IN" (4.7mm,20.9mm) on
Silk To Solder Mask Clearance Constraint: (0.031mm < 0.254mm) Between Pad IP-TP(3.7mm,20.4mm) on Top Layer And Text "IP" (3.2mm,20.9mm) on
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad L2-1(25.146mm,23.436mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad L2-1(25.146mm,23.436mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad L2-1(25.146mm,23.436mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad L2-2(25.146mm,20.236mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.218mm < 0.254mm) Between Pad L2-2(25.146mm,20.236mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad L2-2(25.146mm,20.236mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.135mm < 0.254mm) Between Pad LED1-1(28.35mm,27.49mm) on Top Layer And Text "LED1"
Silk To Solder Mask Clearance Constraint: (0.135mm < 0.254mm) Between Pad LED1-2(26.85mm,27.49mm) on Top Layer And Text "LED1"
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED1-2(26.85mm,27.49mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.135mm < 0.254mm) Between Pad LED2-1(24.45mm,13.31mm) on Top Layer And Text "LED2"
Silk To Solder Mask Clearance Constraint: (0.135mm < 0.254mm) Between Pad LED2-2(25.95mm,13.31mm) on Top Layer And Text "LED2"

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED2-2(25.95mm,13.31mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.194mm < 0.254mm) Between Pad MISO-TP(2.6mm,9.5mm) on Top Layer And Text "MISO"
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R10-1(10.375mm,21.2mm) on Top Layer And Text "R10" (8.6mm,21.8mm)
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R10-2(8.825mm,21.2mm) on Top Layer And Text "R10" (8.6mm,21.8mm)
Silk To Solder Mask Clearance Constraint: (0.246mm < 0.254mm) Between Pad R1-1(30.603mm,27.983mm) on Multi-Layer And Text "12V"
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.254mm) Between Pad R1-1(30.603mm,27.983mm) on Multi-Layer And Text "LED1"
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad R11-1(17.275mm,20mm) on Top Layer And Text "R11"
Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad R12-1(14.3mm,15.925mm) on Top Layer And Text "R12"
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R12-1(14.3mm,15.925mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R12-2(14.3mm,17.475mm) on Top Layer And Text "C21"
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R12-2(14.3mm,17.475mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.254mm) Between Pad R1-3(30.603mm,31.533mm) on Multi-Layer And Text "IN"
Silk To Solder Mask Clearance Constraint: (0.134mm < 0.254mm) Between Pad R1-4(36.703mm,31.533mm) on Multi-Layer And Text "IP"
Silk To Solder Mask Clearance Constraint: (0.164mm < 0.254mm) Between Pad R1-5(13.503mm,9.433mm) on Multi-Layer And Text "C16"
Silk To Solder Mask Clearance Constraint: (0.185mm < 0.254mm) Between Pad R1-5(13.503mm,9.433mm) on Multi-Layer And Text "C20"
Silk To Solder Mask Clearance Constraint: (0.191mm < 0.254mm) Between Pad R3-1(25.575mm,27.5mm) on Top Layer And Text "LED1"
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R3-1(25.575mm,27.5mm) on Top Layer And Text "R3"
Silk To Solder Mask Clearance Constraint: (0.135mm < 0.254mm) Between Pad R3-1(25.575mm,27.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R3-2(24.025mm,27.5mm) on Top Layer And Text "R3"
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R4-1(27.325mm,13.3mm) on Top Layer And Text "R4" (27.5mm,11.9mm)
Silk To Solder Mask Clearance Constraint: (0.235mm < 0.254mm) Between Pad R4-1(27.325mm,13.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R4-2(28.875mm,13.3mm) on Top Layer And Text "R4" (27.5mm,11.9mm)
Silk To Solder Mask Clearance Constraint: (0.144mm < 0.254mm) Between Pad R4-2(28.875mm,13.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.197mm < 0.254mm) Between Pad R4-2(28.875mm,13.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad R5-1(3.375mm,13mm) on Top Layer And Text "R5" (4mm,12.6mm) on
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R6-1(3.925mm,23.6mm) on Top Layer And Text "R6" (4mm,24.2mm) on
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R6-2(5.475mm,23.6mm) on Top Layer And Text "R6" (4mm,24.2mm) on
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R7-1(5.025mm,22.3mm) on Top Layer And Text "IN" (4.7mm,20.9mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R7-1(5.025mm,22.3mm) on Top Layer And Text "R7" (3.2mm,21.9mm)
Silk To Solder Mask Clearance Constraint: (0.231mm < 0.254mm) Between Pad R7-2(6.575mm,22.3mm) on Top Layer And Text "IN" (4.7mm,20.9mm)
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad R9-1(2.575mm,21.5mm) on Top Layer And Text "IP" (3.2mm,20.9mm)
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad R9-1(2.575mm,21.5mm) on Top Layer And Text "R7" (3.2mm,21.9mm)
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R9-1(2.575mm,21.5mm) on Top Layer And Text "R8" (1.3mm,22.1mm) on
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R9-2(1.025mm,21.5mm) on Top Layer And Text "R8" (1.3mm,22.1mm) on
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad TP3-TP(37.206mm,13.3mm) on Top Layer And Text "12V"
Silk To Solder Mask Clearance Constraint: (0.234mm < 0.254mm) Between Pad TP3-TP(37.206mm,13.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad U1-1(33.655mm,9.06mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad U1-1(33.655mm,9.06mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad U1-2(33.655mm,10.01mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad U1-3(33.655mm,10.96mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad U1-3(33.655mm,10.96mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad U1-4(31.355mm,10.96mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad U1-4(31.355mm,10.96mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad U1-5(31.355mm,9.06mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad U1-5(31.355mm,9.06mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.203mm < 0.254mm) Between Pad U2-1(28.096mm,22.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad U2-2(28.096mm,20.31mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad U2-4(28.096mm,15.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.243mm < 0.254mm) Between Pad U2-5(38.006mm,15.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.243mm < 0.254mm) Between Pad U2-8(38.006mm,22.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.222mm < 0.254mm) Between Pad U4-1(17.425mm,18.45mm) on Top Layer And Text "C21"
Silk To Solder Mask Clearance Constraint: (0.136mm < 0.254mm) Between Pad U4-2(17.425mm,17.5mm) on Top Layer And Text "C21"

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U5-6(4.151mm,14.416mm) on Top Layer And Text "R5" (4mm,12.6mm)
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U5-8(5.151mm,14.416mm) on Top Layer And Text "R5" (4mm,12.6mm)
Silk To Solder Mask Clearance Constraint: (0.063mm < 0.254mm) Between Pad VREF-TP(18.5mm,13.6mm) on Top Layer And Text "VREF"
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad XFMR1-1(13.254mm,31.854mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-10(22.004mm,24.234mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-10(22.004mm,24.234mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-11(22.004mm,25.504mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-11(22.004mm,25.504mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-12(22.004mm,26.774mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-12(22.004mm,26.774mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-13(22.004mm,28.044mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-13(22.004mm,28.044mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-14(22.004mm,29.314mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-14(22.004mm,29.314mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-15(22.004mm,30.584mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-15(22.004mm,30.584mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-16(22.004mm,31.854mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-16(22.004mm,31.854mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad XFMR1-2(13.254mm,30.584mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.241mm < 0.254mm) Between Pad XFMR1-3(13.254mm,29.314mm) on Top Layer And Text "C13"
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad XFMR1-3(13.254mm,29.314mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad XFMR1-4(13.254mm,28.044mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad XFMR1-5(13.254mm,26.774mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad XFMR1-6(13.254mm,25.504mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad XFMR1-7(13.254mm,24.234mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad XFMR1-8(13.254mm,22.964mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-9(22.004mm,22.964mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-9(22.004mm,22.964mm) on Top Layer And Track

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.237mm < 0.254mm) Between Arc (17.425mm,19.3mm) on Top Overlay And Text "R11" (17.9mm,19.6mm) on Top
Silk To Silk Clearance Constraint: (0.203mm < 0.254mm) Between Arc (28.596mm,24.89mm) on Top Overlay And Text "C1" (28.1mm,25.8mm) on Top
Silk To Silk Clearance Constraint: (0.176mm < 0.254mm) Between Text "12V" (37.846mm,14.648mm) on Top Overlay And Text "C2"
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "C14" (16.9mm,10.9mm) on Bottom Overlay And Text "R2" (18.1mm,10.9mm) on
Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "C7" (21.8mm,13.7mm) on Top Overlay And Text "C9" (22.8mm,13.7mm) on Top
Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "C9" (22.8mm,13.7mm) on Top Overlay And Text "LED2" (23.8mm,11.9mm) on
Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "CS" (4.1mm,8.8mm) on Top Overlay And Text "SCK" (3.1mm,8.8mm) on Top
Silk To Silk Clearance Constraint: (0.179mm < 0.254mm) Between Text "IN" (4.7mm,20.9mm) on Top Overlay And Text "IP" (3.2mm,20.9mm) on Top
Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "IP" (3.2mm,20.9mm) on Top Overlay And Text "R7" (3.2mm,21.9mm) on Top
Silk To Silk Clearance Constraint: (0.239mm < 0.254mm) Between Text "L2" (23.3mm,20.4mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "LED1" (26.2mm,28.1mm) on Top Overlay And Text "PWR" (25.3mm,29.1mm) on
Silk To Silk Clearance Constraint: (0.02mm < 0.254mm) Between Text "LED1" (26.2mm,28.1mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.02mm < 0.254mm) Between Text "LED2" (23.8mm,11.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "MISO" (2.1mm,8.8mm) on Top Overlay And Text "MOSI" (1.1mm,8.8mm) on Top
Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "MISO" (2.1mm,8.8mm) on Top Overlay And Text "SCK" (3.1mm,8.8mm) on Top
Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "PWR" (25.3mm,29.1mm) on Top Overlay And Text "R3" (24.175mm,28.1mm) on
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "R12" (13.9mm,15.4mm) on Top Overlay And Text "VREF" (15.1mm,13.2mm) on
Silk To Silk Clearance Constraint: (0.15mm < 0.254mm) Between Text "R12" (13.9mm,15.4mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.157mm < 0.254mm) Between Text "R12" (13.9mm,15.4mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.15mm < 0.254mm) Between Text "R8" (1.3mm,22.1mm) on Top Overlay And Text "R9" (1.3mm,23.2mm) on Top
Silk To Silk Clearance Constraint: (0.075mm < 0.254mm) Between Text "U4" (19.2mm,14.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.095mm < 0.254mm) Between Text "U4" (19.2mm,14.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.052mm < 0.254mm) Between Text "U5" (0.2mm,17.2mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.252mm < 0.254mm) Between Text "U6" (6mm,17.2mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0mm < 0.254mm) Between Text "U6" (6mm,17.2mm) on Top Overlay And Track