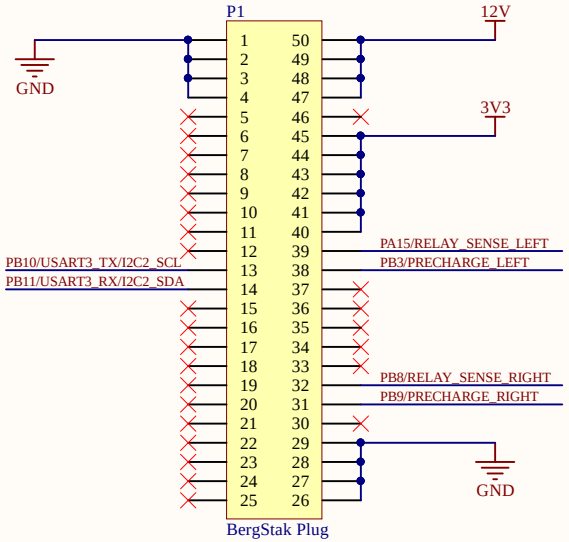
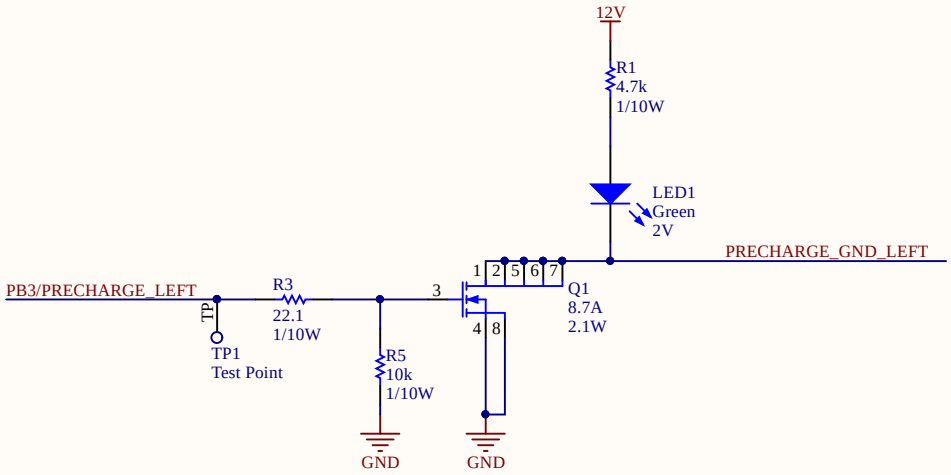
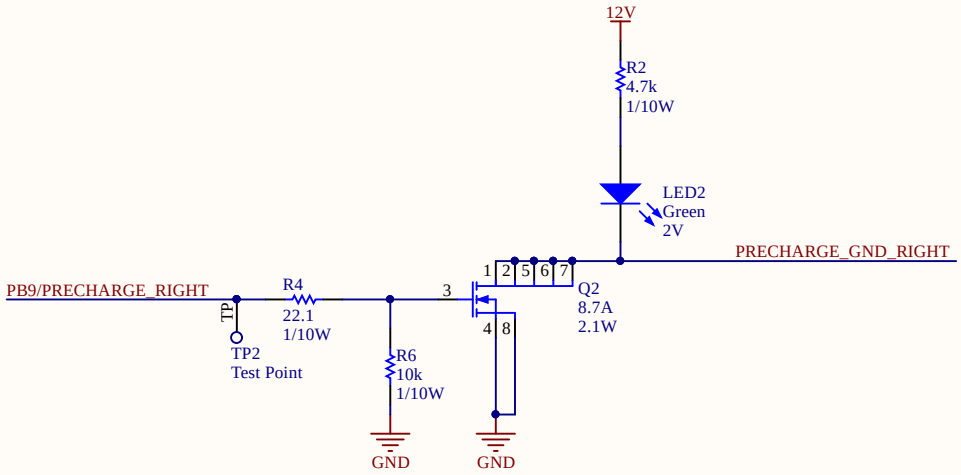


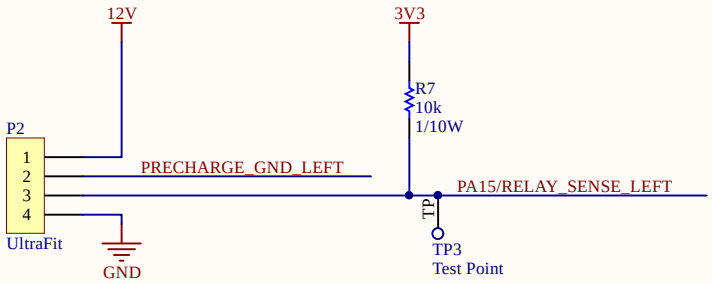
Project: *MSXII_MotorControllerInterface.PrjPcb*		MIDNIGHT SUN
Title: **Controller Board Interface**		
Project Author: Peiliang Guo		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.6	
Date: 2018-05-21	Sheet 1 of 3	Website: www.uwmidsun.com

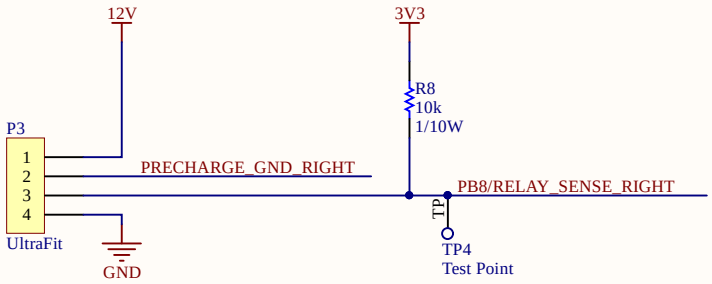
Precharge Control





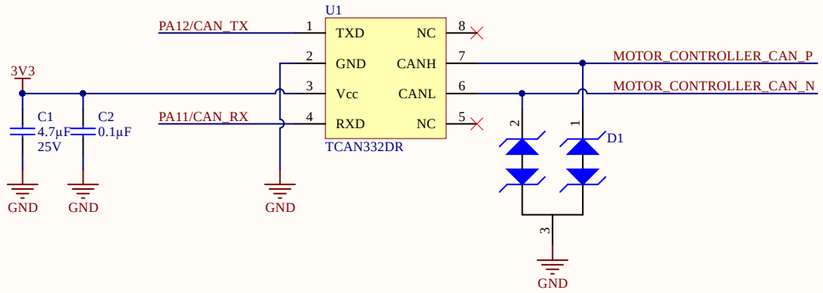
Relay Connectors



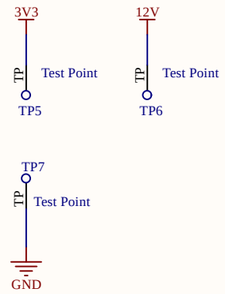


Project: *MSXII_MotorControllerInterface.PrjPcb*		MIDNIGHT SUN
Title: **PreCharge Interface**		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Author: Peiliang Guo		
Size: Letter	Revision: 1.6	
Date: 2018-05-21	Sheet 2 of 3	Website: www.uwmidsun.com

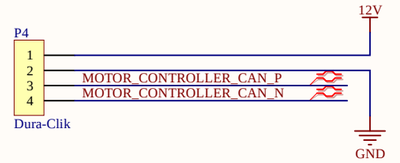
CAN

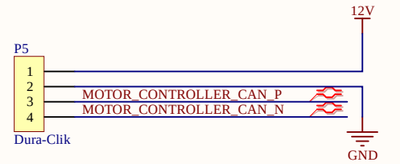


Power Test Points

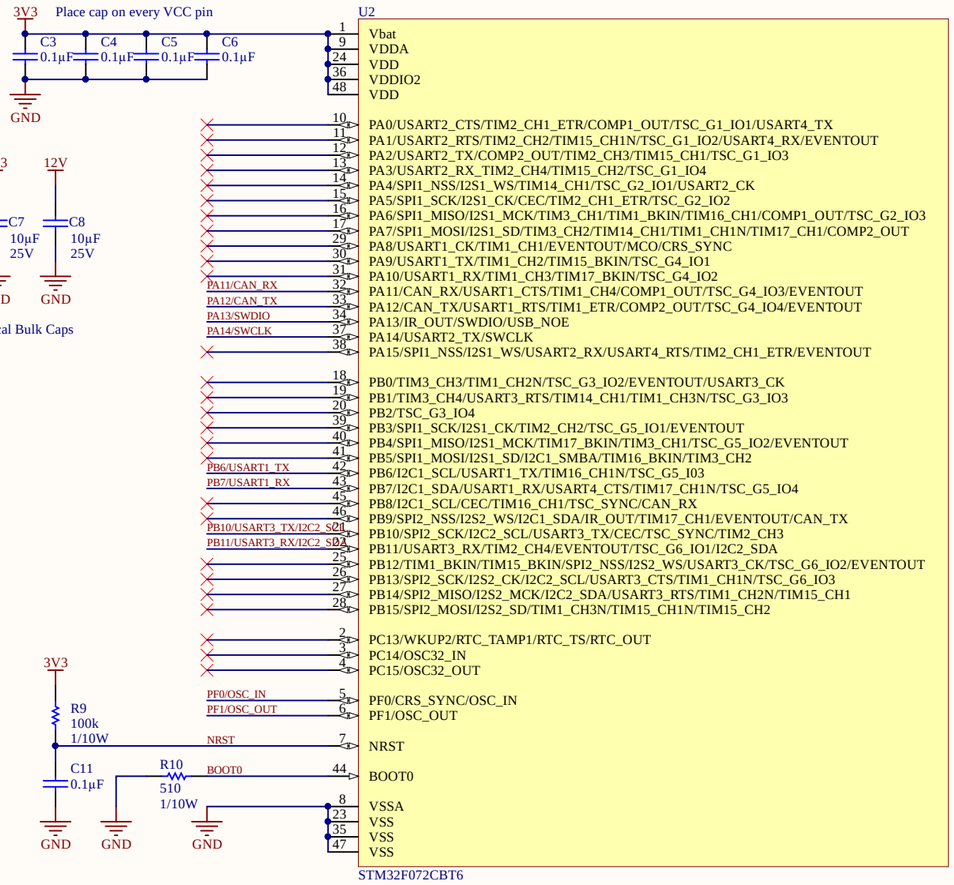


Connectors

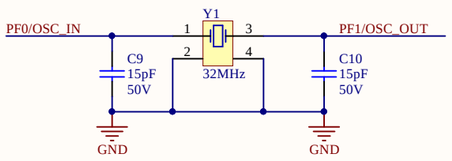


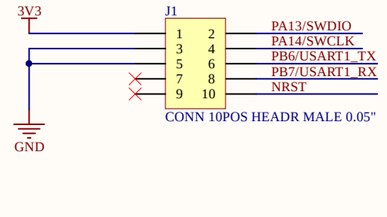


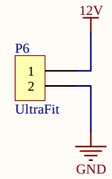
MCU + Peripherals



Clocking





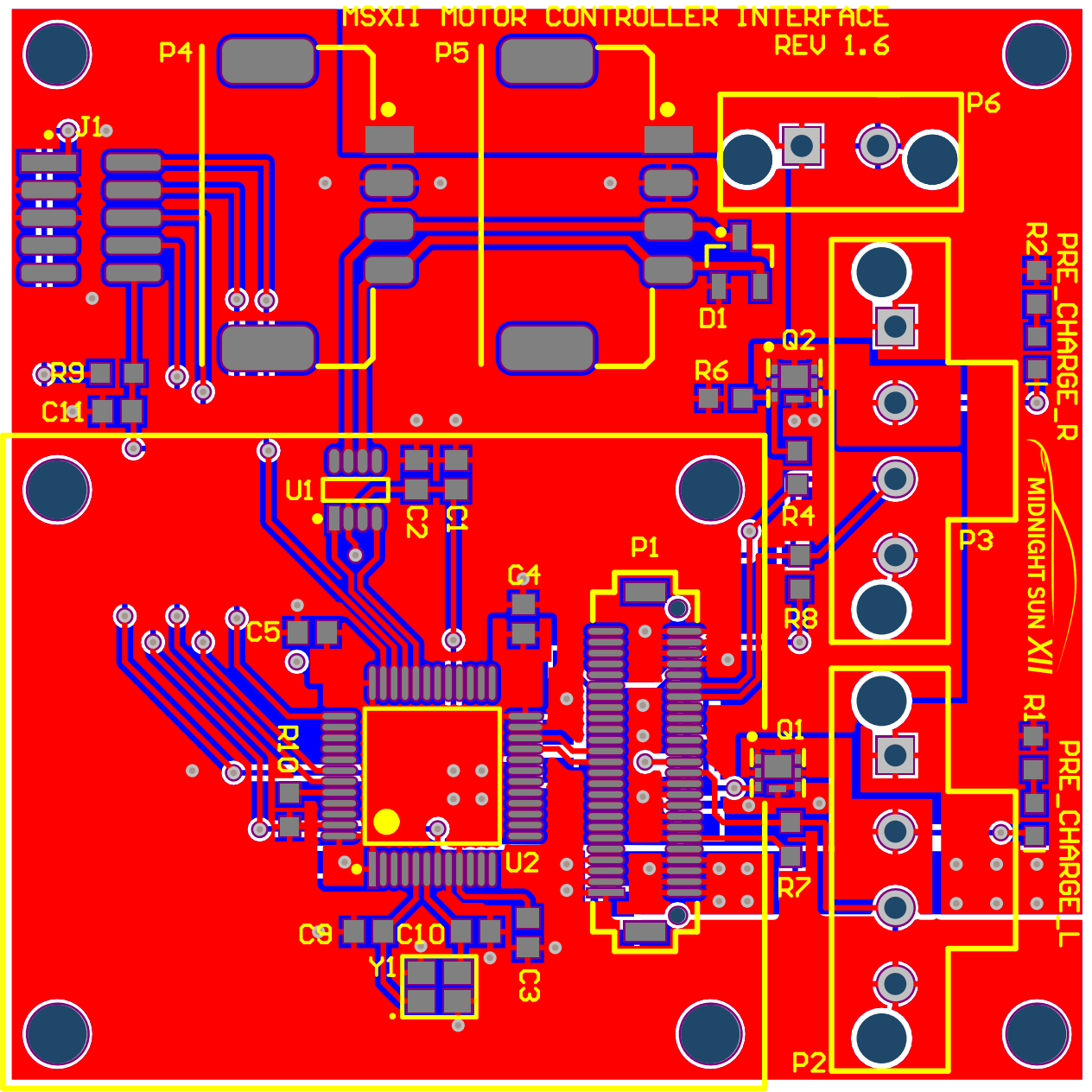


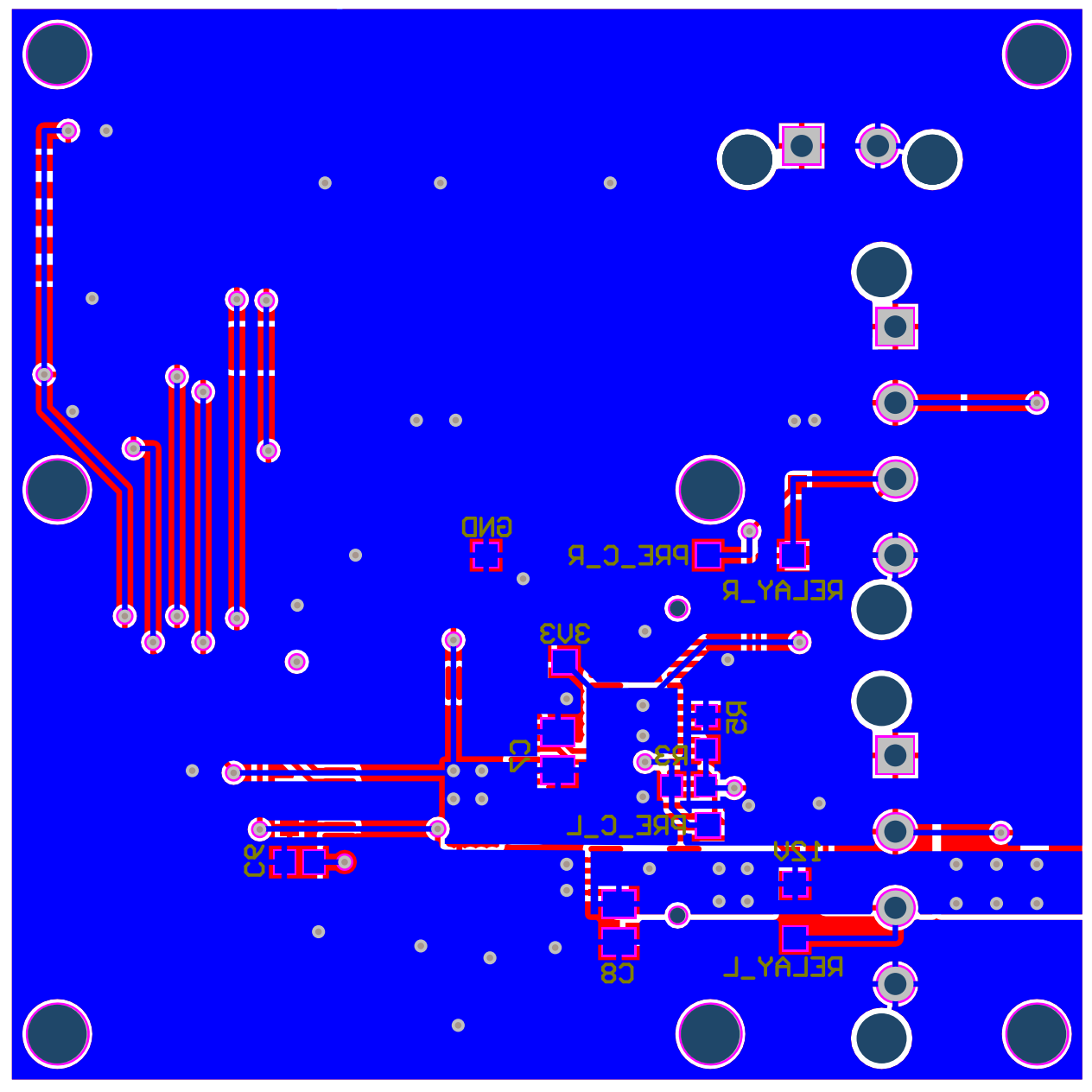
Project: *MSXII_MotorControllerInterface.PrjPcb*		MIDNIGHT SUN
Title: **Slave Controller**		
Project Lead: Peiliang Guo		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.6	
Date: 2018-05-21	Sheet 3 of 3	Website: www.uwmidsun.com

Bill of Materials

Project:	MSXII_MotorControllerInterface.PrjPcb
Revision:	1.6
Project Lead:	Peiliang Guo
Generated On:	2018-05-21 9:28:46 PM
Production Quantity:	1
Currency	CAD
Total Parts Count:	39

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Supplier Order Qty 1	Supplier Subtotal 1
CAP CER 4.7UF 25V 10% X5R 0603	C1	Murata	GRM188R61E475KE11D	Digi-Key	490-7203-1-ND	0.53	1	$ 0.53
CAP CER 0.1UF 50V 10% X7R 0603	C2	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.2	1	$ 0.20
CAP CER 0.1UF 50V 10% X7R 0603	C3	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.2	1	$ 0.20
CAP CER 0.1UF 50V 10% X7R 0603	C4	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.2	1	$ 0.20
CAP CER 0.1UF 50V 10% X7R 0603	C5	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.2	1	$ 0.20
CAP CER 0.1UF 50V 10% X7R 0603	C6	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.2	1	$ 0.20
CAP CER 10uF 25V 10% X5R 0805	C7	Murata	GRM21BR61E106KA73L	Digi-Key	490-5523-1-ND	0.31	1	$ 0.31
CAP CER 10uF 25V 10% X5R 0805	C8	Murata	GRM21BR61E106KA73L	Digi-Key	490-5523-1-ND	0.31	1	$ 0.31
CAP CER 15PF 50V ±5% NPO 0603	C9	Yageo	CC0603JRNPO9BN150	Digi-Key	311-1060-1-ND	0.13	1	$ 0.13
CAP CER 15PF 50V ±5% NPO 0603	C10	Yageo	CC0603JRNPO9BN150	Digi-Key	311-1060-1-ND	0.13	1	$ 0.13
CAP CER 0.1UF 50V 10% X7R 0603	C11	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.2	1	$ 0.20
DIODE TVS 24VWM 70VC SOT23	D1	Nexperia	PESD1CAN,215	Digi-Key	1727-3817-1-ND	0.63	1	$ 0.63
CONN 10POS HEADR MALE 0.05"	J1	Amphenol FCI	20021121-00010C4LF	Digi-Key	609-3695-1-ND	1.08	1	$ 1.08
LED GREEN CLEAR 2V 0603	LED1	Wurth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.18	1	$ 0.18
LED GREEN CLEAR 2V 0603	LED2	Wurth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.18	1	$ 0.18
CONN 50POS Bergstak Plug 0.02"	P1	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND	1.79	1	$ 1.79
CONN 4POS ULTRA-FIT 0.138"	P2	Molex	1722871104	Digi-Key	WM11703-ND	1.15	1	$ 1.15
CONN 4POS ULTRA-FIT 0.138"	P3	Molex	1722871104	Digi-Key	WM11703-ND	1.15	1	$ 1.15
CONN 4POS DURA-CLIK 0.079"	P4	Molex	560020-0420	Digi-Key	WM10864CT-ND	2.02	1	$ 2.02
CONN 4POS DURA-CLIK 0.079"	P5	Molex	560020-0420	Digi-Key	WM10864CT-ND	2.02	1	$ 2.02
CONN 2POS ULTRA-FIT 0.138"	P6	Molex	1722861302	Digi-Key	WM11673-ND	1.77	1	$ 1.77
MOSFET N-CH 30V 8.7A 2.1W 6-PQFN (2x2)	Q1	Infineon	IRLHS6342TRPBF	Digi-Key	IRLHS6342TRPBFCT-ND	0.9	1	$ 0.90
MOSFET N-CH 30V 8.7A 2.1W 6-PQFN (2x2)	Q2	Infineon	IRLHS6342TRPBF	Digi-Key	IRLHS6342TRPBFCT-ND	0.9	1	$ 0.90
RES 4.7K OHM 1% 1/10W 0603	R1	Yageo	RC0603FR-074K7L	Digi-Key	311-4.70KHRCT-ND	0.13	1	$ 0.13
RES 4.7K OHM 1% 1/10W 0603	R2	Yageo	RC0603FR-074K7L	Digi-Key	311-4.70KHRCT-ND	0.13	1	$ 0.13
RES 22.1 OHM 1% 1/10W 0603	R3	Yageo	RC0603FR-0722R1L	Digi-Key	311-22.1HRCT-ND	0.13	1	$ 0.13
RES 22.1 OHM 1% 1/10W 0603	R4	Yageo	RC0603FR-0722R1L	Digi-Key	311-22.1HRCT-ND	0.13	1	$ 0.13
RES 10K OHM 1% 1/10W 0603	R5	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 10K OHM 1% 1/10W 0603	R6	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 10K OHM 1% 1/10W 0603	R7	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 10K OHM 1% 1/10W 0603	R8	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 100K OHM 5% 1/8W 0603	R9	Yageo	RC0603JR-07100KL	Digi-Key	311-100KGRCT-ND	0.13	1	$ 0.13
RES 510 OHM 5% 1/10W 0603	R10	Yageo	RC0603JR-07510RL	Digi-Key	311-510GRCT-ND	0.13	1	$ 0.13
Test Point	TP5							
Test Point	TP6							
Test Point	TP7							
IC CAN Tranceiver TCAN332DR	U1	Texas Instruments	TCAN332DR	Digi-Key	296-43711-1-ND	2.65	1	$ 2.65
IC MCU 32BIT 128KB FLASH 48LQFP	U2	STMicroelectronics	STM32F072CBT6	Digi-Key	497-14645-ND	4.56	1	$ 4.56
CRYSTAL 32 MHz 8pF 4-SMD	Y1	Kyocera AVX	CX2520DB32000D0GPSC1	Digi-Key	1253-1730-1-ND	0.92	1	$ 0.92
							Total:	$ 25.81


MSXII MOTOR CONTROLLER INTERFACE
REV 1.6
P4
P5
P6
J1
D1
Q2
R6
R9
C11
R2
PRE_CHARGE_R
U1
C2
C1
R4
P1
C4
P3
MIDNIGHT SUN XII
C5
R8
R10
Q1
R1
PRE_CHARGE_L
U2
R7
C9
C10
Y1
C3
P2


GND
PRE_C_R
RELAY_R
3V3
R5
R3
C4
PRE_C_L
C3
12V
C8
RELAY_L

MSXII MOTOR CONTROLLER IN
P4
P5
P6
J1
D1
Q2
R6
R9
C11
R2
PRE_CHARGE_R
R4
R8
P3
NIGHT SUN XII
R1
Q1
PRE_CHARGE_L
R7
P2
U1
C2
C1
P1
C4
C5
R10
U2

Electrical Rules Check Report

Class	Document	Message
Warning	Slave_Controller.SchDoc	Net BOOT0 has no driving source (Pin R10-2,Pin U2-44)

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII_MotorControllerInterfa

Warnings 0
Rule Violations 92

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=2.54mm) (Preferred=0.254mm) (All)	0
Width Constraint (Min=0.381mm) (Max=0.381mm) (Preferred=0.381mm) (InNet('12V'))	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.15mm) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)	46
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	36
Silk to Silk (Clearance=0.254mm) (OnLayer('Bottom Overlay')),(OnLayer('Bottom Overlay'))	0
Silk to Silk (Clearance=0.254mm) (OnLayer('Top Overlay')),(OnLayer('Top Overlay'))	5
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	5
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	92

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C10-1(22.375mm,7.2mm) on Top Layer And Pad C10-2(21.025mm,7.2mm) on
Minimum Solder Mask Sliver Constraint: (0.222mm < 0.3mm) Between Pad C10-1(22.375mm,7.2mm) on Top Layer And Via (22.375mm,6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C1-1(20.809mm,28.875mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C11-1(4.579mm,31.1mm) on Top Layer And Pad C11-2(5.929mm,31.1mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C2-1(19.004mm,28.875mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C3-1(24.104mm,6.471mm) on Top Layer And Pad C3-2(24.104mm,7.821mm)
Minimum Solder Mask Sliver Constraint: (0.293mm < 0.3mm) Between Pad C3-1(24.104mm,6.471mm) on Top Layer And Via (25.375mm,6.471mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C4-1(23.9mm,22.229mm) on Top Layer And Pad C4-2(23.9mm,20.879mm) on
Minimum Solder Mask Sliver Constraint: (0.259mm < 0.3mm) Between Pad C4-1(23.9mm,22.229mm) on Top Layer And Via (23.9mm,23.416mm) from Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C5-1(13.525mm,20.954mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.268mm < 0.3mm) Between Pad C5-1(13.525mm,20.954mm) on Top Layer And Via (13.525mm,22.2mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C6-1(12.925mm,10.4mm) on Bottom Layer And Pad C6-2(14.275mm,10.4mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C9-1(16.125mm,7.2mm) on Top Layer And Pad C9-2(17.475mm,7.2mm) on
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(29.5mm,22.8mm) on Top Layer And Pad P1-(31mm,22.05mm) on
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(29.5mm,7.2mm) on Top Layer And Pad P1-(31mm,7.95mm) on Multi-Layer
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-1(34.675mm,15.15mm) on Top Layer And Pad Q1-2(34.675mm,14.5mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-2(34.675mm,14.5mm) on Top Layer And Pad Q1-3(34.675mm,13.85mm) on
Minimum Solder Mask Sliver Constraint: (0.275mm < 0.3mm) Between Pad Q1-2(34.675mm,14.5mm) on Top Layer And Pad Q1-8(35.6mm,13.76mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-3(34.675mm,13.85mm) on Top Layer And Pad Q1-7(35.6mm,14.8mm) on
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.3mm) Between Pad Q1-3(34.675mm,13.85mm) on Top Layer And Pad Q1-8(35.6mm,13.76mm) on
Minimum Solder Mask Sliver Constraint: (0.178mm < 0.3mm) Between Pad Q1-3(34.675mm,13.85mm) on Top Layer And Via (34.261mm,13mm) from Top
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-4(36.525mm,13.85mm) on Top Layer And Pad Q1-5(36.525mm,14.5mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-4(36.525mm,13.85mm) on Top Layer And Pad Q1-7(35.6mm,14.8mm) on
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.3mm) Between Pad Q1-4(36.525mm,13.85mm) on Top Layer And Pad Q1-8(35.6mm,13.76mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-5(36.525mm,14.5mm) on Top Layer And Pad Q1-6(36.525mm,15.15mm) on
Minimum Solder Mask Sliver Constraint: (0.275mm < 0.3mm) Between Pad Q1-5(36.525mm,14.5mm) on Top Layer And Pad Q1-8(35.6mm,13.76mm) on
Minimum Solder Mask Sliver Constraint: (0.187mm < 0.3mm) Between Pad Q1-7(35.6mm,14.8mm) on Top Layer And Pad Q1-8(35.6mm,13.76mm) on Top
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q2-1(35.439mm,33.05mm) on Top Layer And Pad Q2-2(35.439mm,32.4mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q2-2(35.439mm,32.4mm) on Top Layer And Pad Q2-3(35.439mm,31.75mm) on
Minimum Solder Mask Sliver Constraint: (0.275mm < 0.3mm) Between Pad Q2-2(35.439mm,32.4mm) on Top Layer And Pad Q2-8(36.364mm,31.66mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q2-3(35.439mm,31.75mm) on Top Layer And Pad Q2-7(36.364mm,32.7mm) on
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.3mm) Between Pad Q2-3(35.439mm,31.75mm) on Top Layer And Pad Q2-8(36.364mm,31.66mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q2-4(37.289mm,31.75mm) on Top Layer And Pad Q2-5(37.289mm,32.4mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q2-4(37.289mm,31.75mm) on Top Layer And Pad Q2-7(36.364mm,32.7mm) on
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.3mm) Between Pad Q2-4(37.289mm,31.75mm) on Top Layer And Pad Q2-8(36.364mm,31.66mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q2-5(37.289mm,32.4mm) on Top Layer And Pad Q2-6(37.289mm,33.05mm) on
Minimum Solder Mask Sliver Constraint: (0.275mm < 0.3mm) Between Pad Q2-5(37.289mm,32.4mm) on Top Layer And Pad Q2-8(36.364mm,31.66mm) on
Minimum Solder Mask Sliver Constraint: (0.187mm < 0.3mm) Between Pad Q2-7(36.364mm,32.7mm) on Top Layer And Pad Q2-8(36.364mm,31.66mm) on
Minimum Solder Mask Sliver Constraint: (0.297mm < 0.3mm) Between Pad Y1-1(19.2mm,4.021mm) on Top Layer And Pad Y1-2(20.9mm,4.021mm) on
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad Y1-1(19.2mm,4.021mm) on Top Layer And Pad Y1-4(19.2mm,5.321mm) on
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad Y1-2(20.9mm,4.021mm) on Top Layer And Pad Y1-3(20.9mm,5.321mm) on
Minimum Solder Mask Sliver Constraint: (0.118mm < 0.3mm) Between Pad Y1-2(20.9mm,4.021mm) on Top Layer And Via (20.916mm,2.9mm) from Top
Minimum Solder Mask Sliver Constraint: (0.297mm < 0.3mm) Between Pad Y1-3(20.9mm,5.321mm) on Top Layer And Pad Y1-4(19.2mm,5.321mm) on
Minimum Solder Mask Sliver Constraint: (0.222mm < 0.3mm) Between Pad Y1-4(19.2mm,5.321mm) on Top Layer And Via (19.2mm,6.546mm) from Top
Minimum Solder Mask Sliver Constraint: (0.234mm < 0.3mm) Between Via (33.6mm,13.8mm) from Top Layer to Bottom Layer And Via (34.261mm,13mm)
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.3mm) Between Via (36.364mm,30.666mm) from Top Layer to Bottom Layer And Via

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.155mm < 0.178mm) Between Pad P4-7(12.17mm,34mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.17mm < 0.178mm) Between Pad P4-7(12.17mm,47.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.155mm < 0.178mm) Between Pad P5-7(25mm,34mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.17mm < 0.178mm) Between Pad P5-7(25mm,47.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q1-1(34.675mm,15.15mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q1-2(34.675mm,14.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q1-2(34.675mm,14.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q1-3(34.675mm,13.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q1-4(36.525mm,13.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q1-5(36.525mm,14.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q1-5(36.525mm,14.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q1-6(36.525mm,15.15mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q2-1(35.439mm,33.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q2-2(35.439mm,32.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q2-2(35.439mm,32.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q2-3(35.439mm,31.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q2-4(37.289mm,31.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q2-5(37.289mm,32.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q2-5(37.289mm,32.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q2-6(37.289mm,33.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U1-1(15.225mm,26.175mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U1-2(15.875mm,26.175mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U1-3(16.525mm,26.175mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U1-4(17.175mm,26.175mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U1-5(17.175mm,28.825mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U1-6(16.525mm,28.825mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U1-7(15.875mm,28.825mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U1-8(15.225mm,28.825mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad Y1-1(19.2mm,4.021mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad Y1-1(19.2mm,4.021mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad Y1-2(20.9mm,4.021mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad Y1-2(20.9mm,4.021mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad Y1-3(20.9mm,5.321mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad Y1-3(20.9mm,5.321mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad Y1-4(19.2mm,5.321mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad Y1-4(19.2mm,5.321mm) on Top Layer And Track

Silk to Silk (Clearance=0.254mm) (OnLayer('Top Overlay')),(OnLayer('Top Overlay'))
Silk To Silk Clearance Constraint: (0.151mm < 0.254mm) Between Text "P2" (36.384mm,0.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.151mm < 0.254mm) Between Text "P2" (36.384mm,0.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.168mm < 0.254mm) Between Text "P6" (44.4mm,44.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.168mm < 0.254mm) Between Text "P6" (44.4mm,44.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.209mm < 0.254mm) Between Text "Y1" (16.9mm,5.2mm) on Top Overlay And Track

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (0.181mm < 0.406mm) Between Board Edge And Text "MSXII MOTOR CONTROLLER INTERFACE

REV 1.6" (14.1mm,47.4mm) on Top Overlay

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,0mm)(0mm,30mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,0mm)(35mm,0mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,30mm)(35mm,30mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (35mm,0mm)(35mm,13.1mm) on Top Overlay