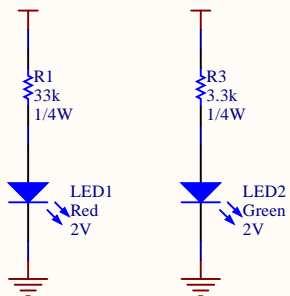

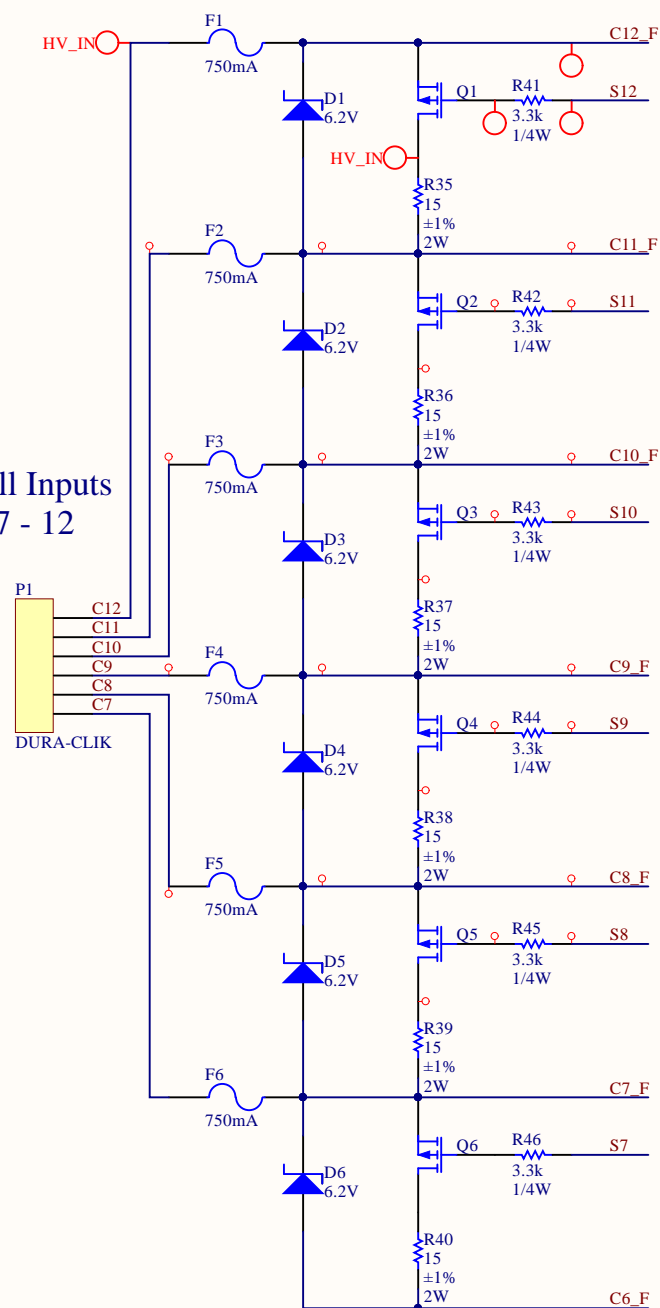


▲ 5V Rail Current Consumption:
 LTC6804 IREG = IREG (LTC6804 CORE) + IREG (isoSPI)
 Thermistor Buffer Op Amp
 Thermistor X12

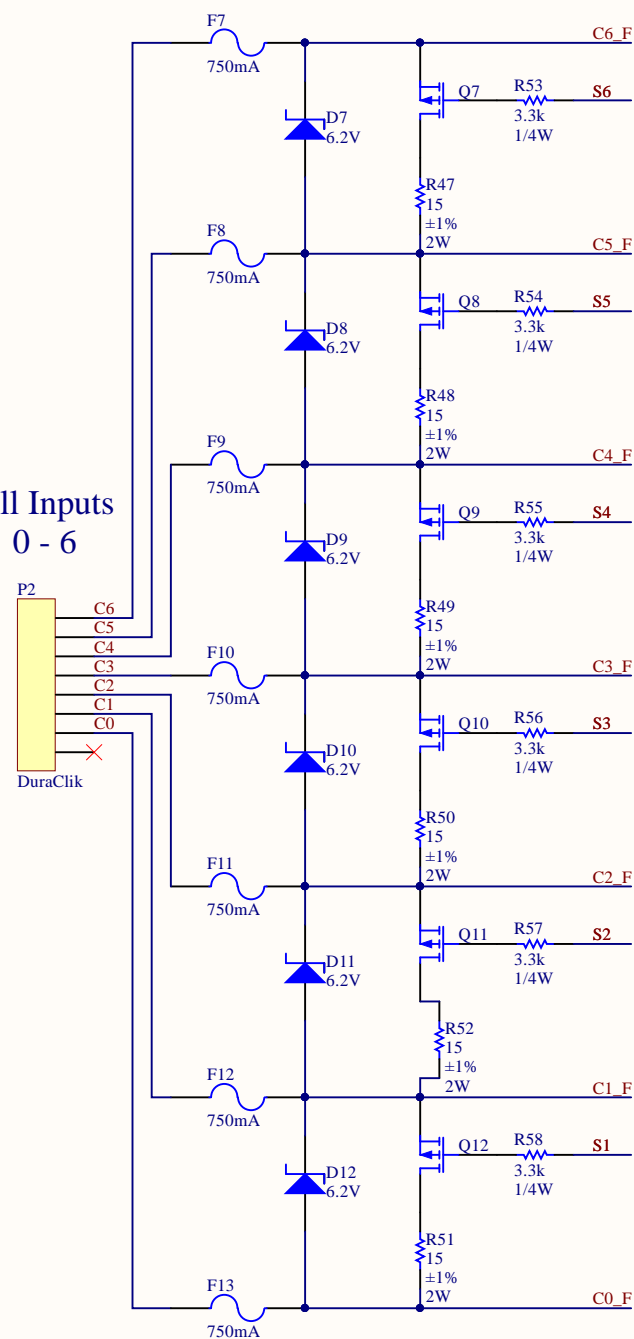


Project: BMS_AFE.PrjPcb		<div><div>MIDNIGHT</div><div></div><div>SUN</div></div>
Title: Power Supplies		
Project Lead: Kevin Chen, Taiping Li		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 3.1	
Date: 2018-10-19	Sheet2 of 6	
		Website: www.uwmidson.com

Cell Inputs
7 - 12



Cell Inputs
0 - 6



Cell+Bal_Interface

C12_F	→	C12_F
S12	→	S12
C11_F	→	C11_F
S11	→	S11
C10_F	→	C10_F
S10	→	S10
C9_F	→	C9_F
S9	→	S9
C8_F	→	C8_F
S8	→	S8
C7_F	→	C7_F
S7	→	S7
C6_F	→	C6_F
S6	→	S6
C5_F	→	C5_F
S5	→	S5
C4_F	→	C4_F
S4	→	S4
C3_F	→	C3_F
S3	→	S3
C2_F	→	C2_F
S2	→	S2
C1_F	→	C1_F
S1	→	S1
C0_F	→	C0_F

Project: **BMS_AFE.PrjPcb**

Title: **Cell+Balancing Interface**

Project Lead: Kevin Chen, Taiping Li

Size: Letter

Revision: 3.1

Date: 2018-10-19

Sheet4 of 6

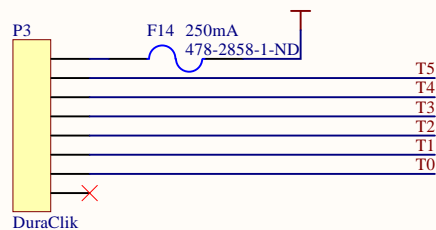


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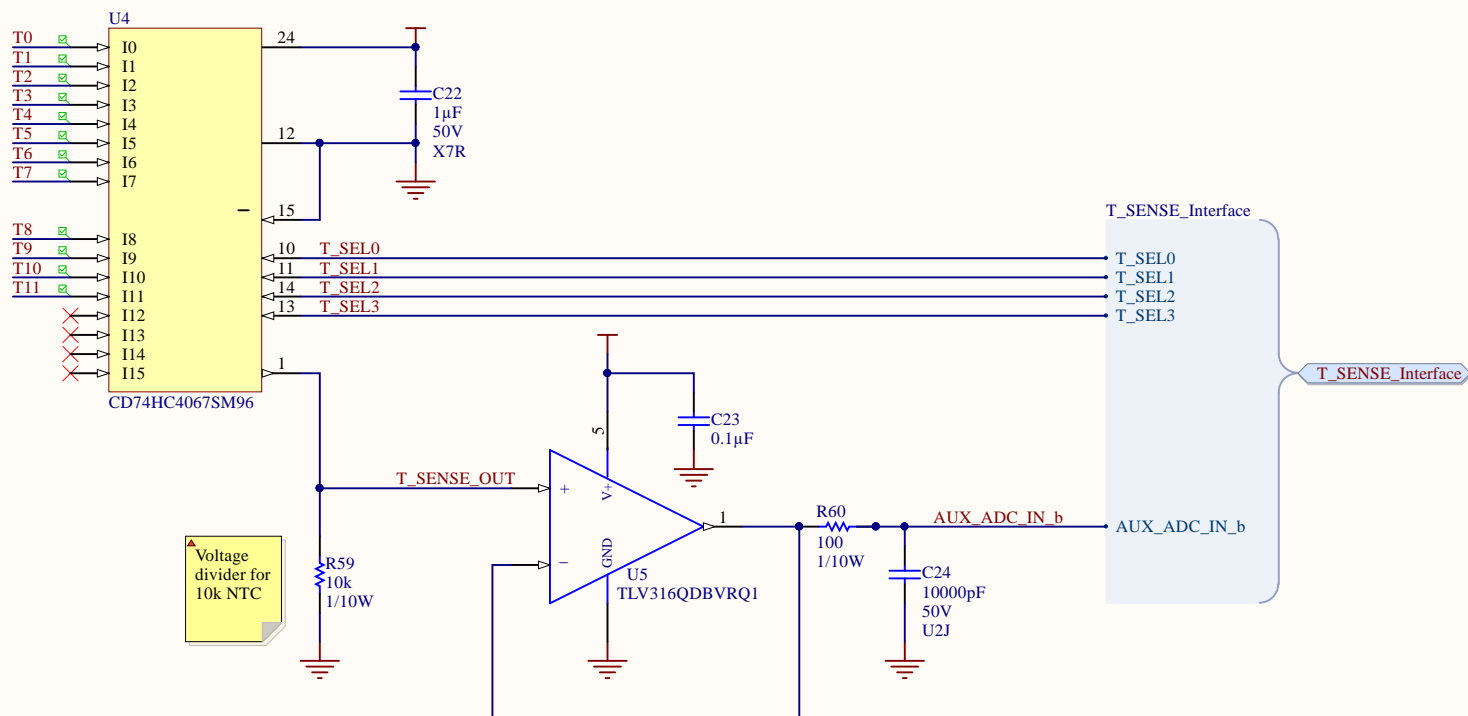
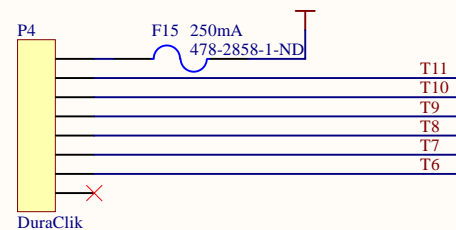
Thermistor Inputs

0 - 5



Thermistor Inputs

6 - 11



Project: **BMS_AFE.PrjPcb**

Title: **Thermistor Interface**

Project Lead: Kevin Chen, Taiping Li

Size: Letter

Date: 2018-10-19

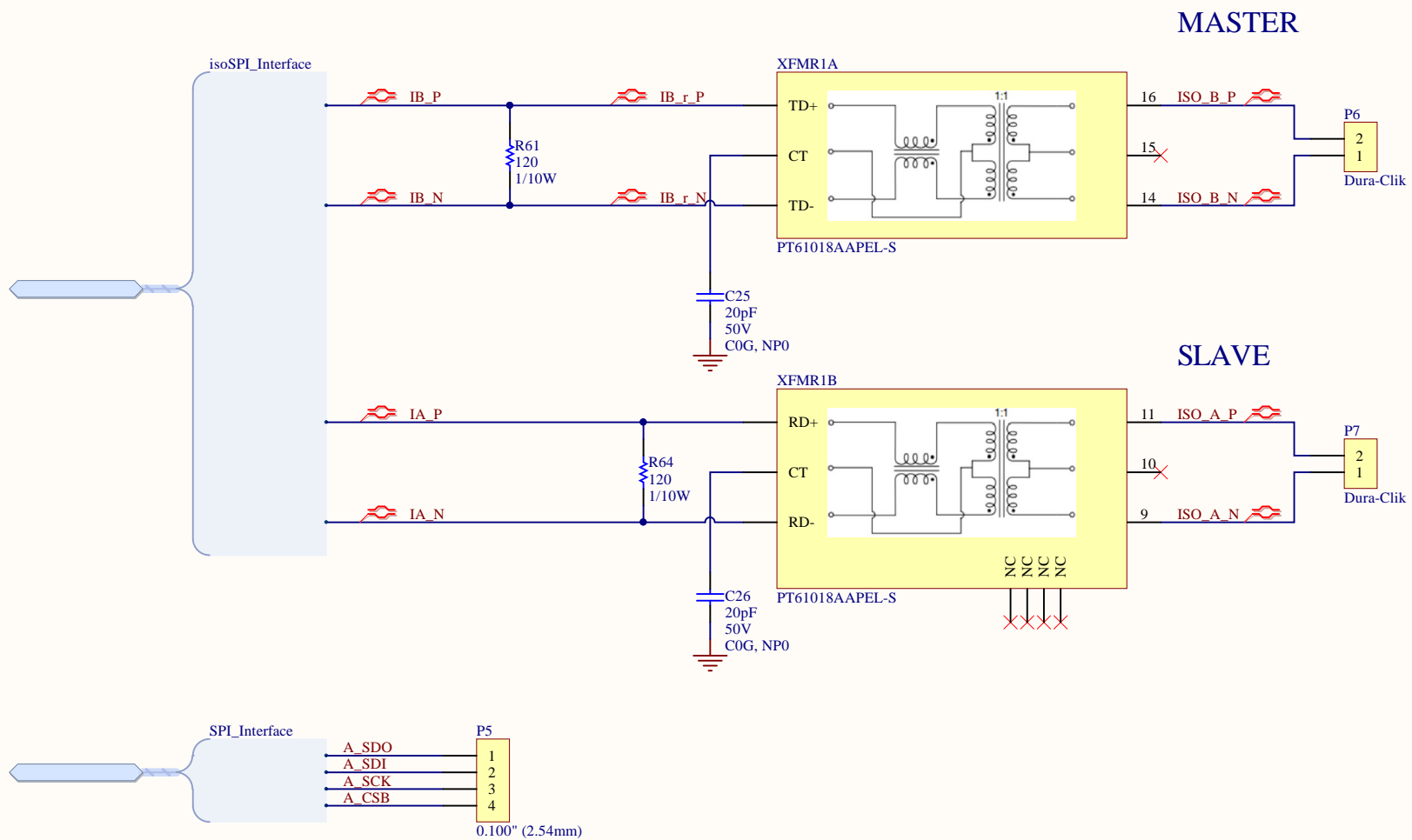
Revision: 3.1


Sheet5 of 6

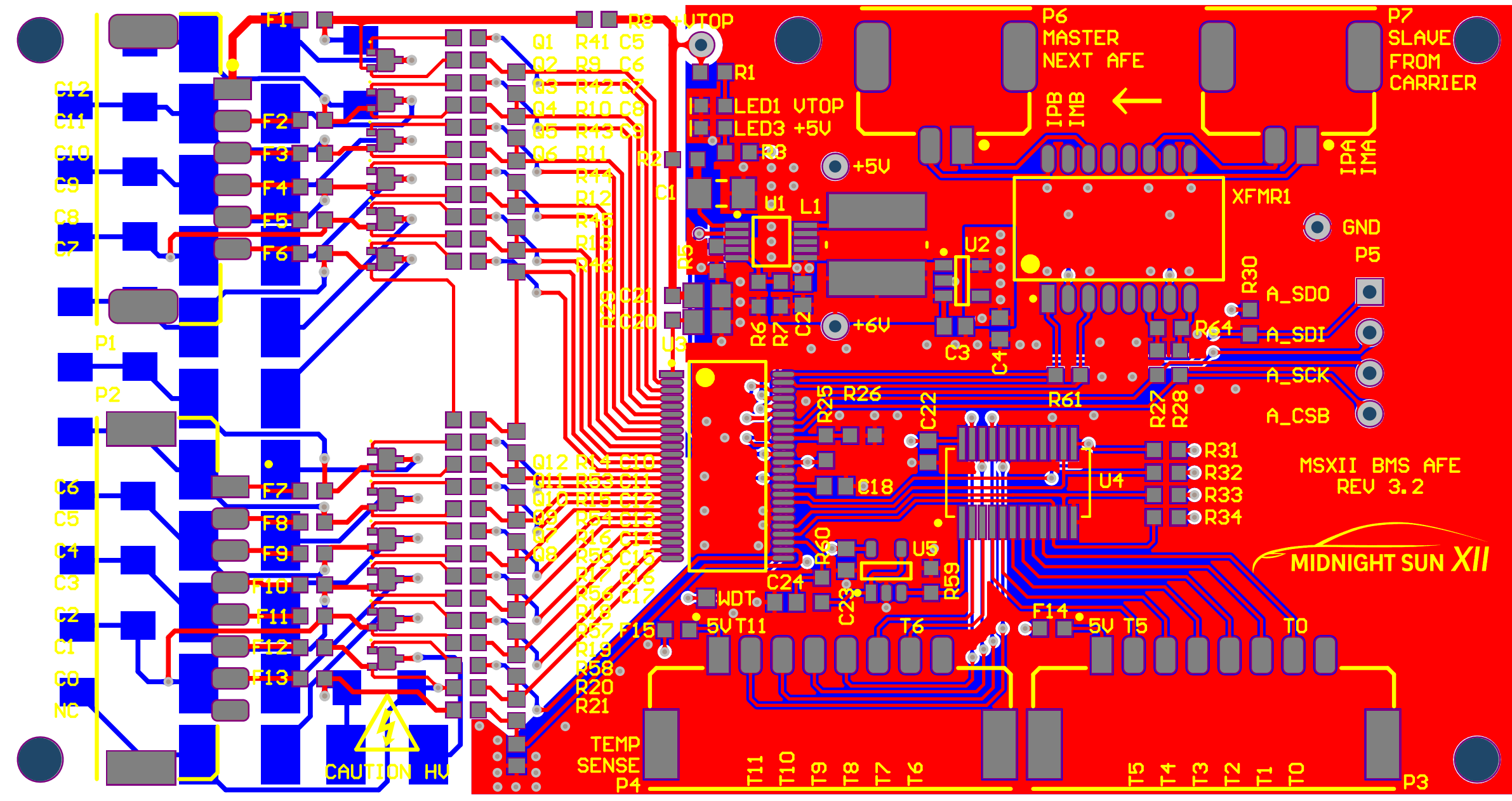


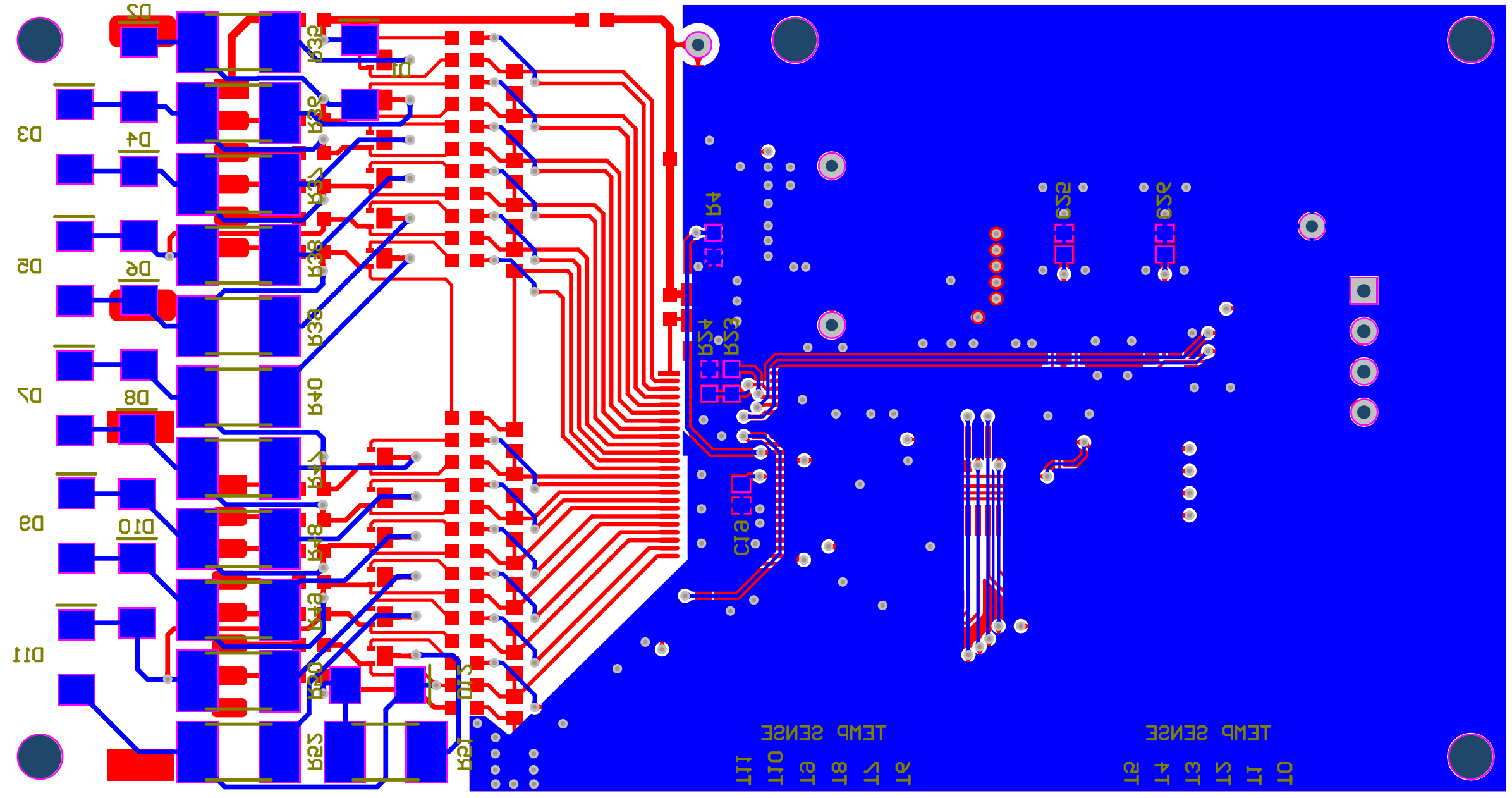
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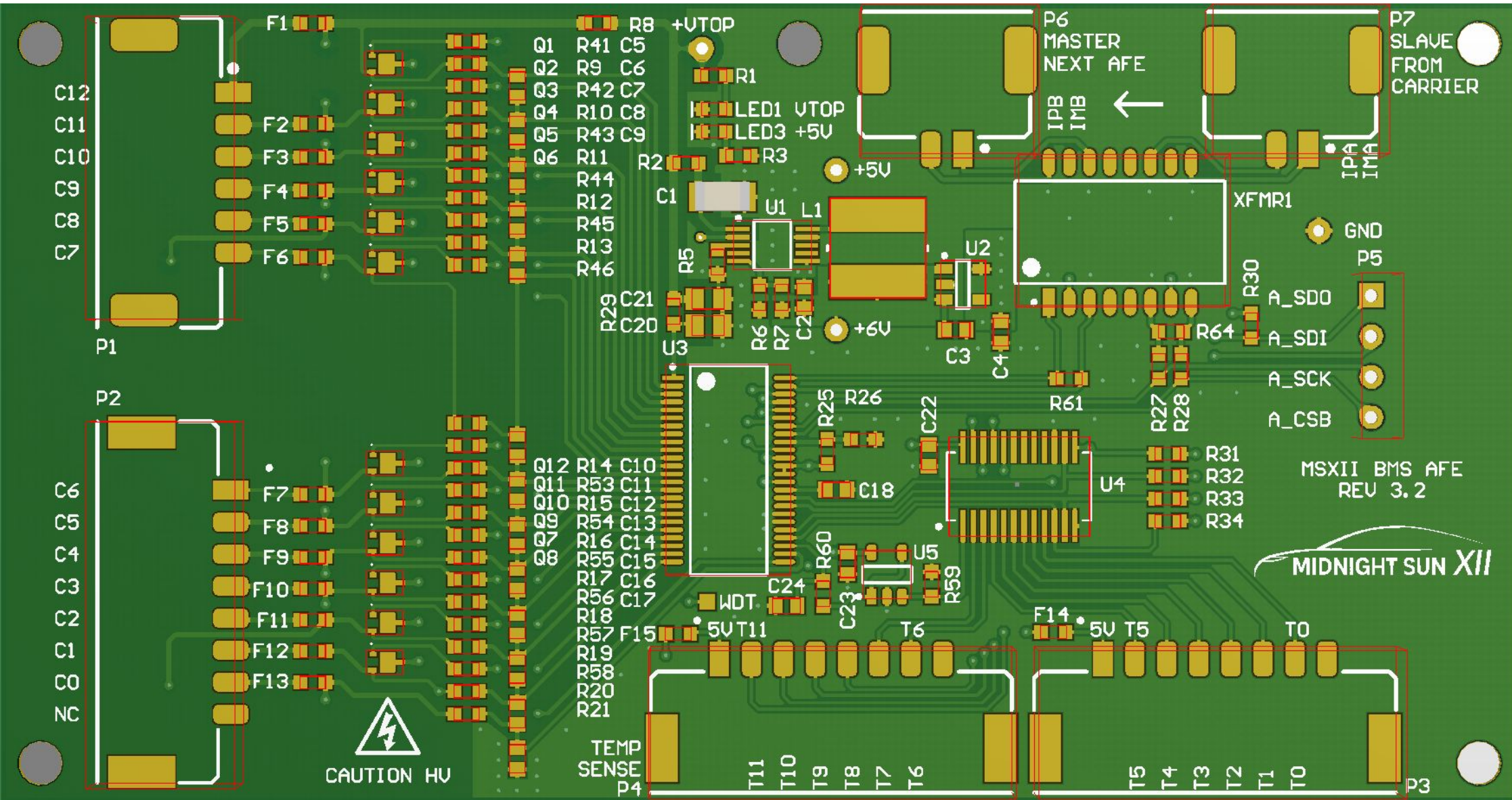
Website: www.uwmidson.com



Project: BMS_AFE.PrjPcb		
Title: isoSPI Interface		
Project Lead: Kevin Chen, Taiping Li		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 3.1	
Date: 2018-10-19	Sheet6 of 6	
		Website: www.uwmidsun.com







Electrical Rules Check Report

Class	Document	Message
Warning	AFE.SchDoc	Nets Wire IB_N has multiple names (Net Label IB_N,Net Label IB_N,Net Label IB_N,Net Label IB_r_N)
Warning	isoSPI_Interface.SchDoc	Nets Wire IB_N has multiple names (Net Label IB_N,Net Label IB_r_N)
Warning	AFE.SchDoc	Nets Wire IB_P has multiple names (Net Label IB_P,Net Label IB_P,Net Label IB_P,Net Label IB_r_P)
Warning	isoSPI_Interface.SchDoc	Nets Wire IB_P has multiple names (Net Label IB_P,Net Label IB_r_P)

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII_BMS_AFE\AFE.PcbDc
c

Warnings 0
Rule Violations 1

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.6mm) (InNetClass('HV_IN'),(InNet('GND'))	0
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Clearance Constraint (Gap=0.6mm) (InNetClass('HV_IN'),(InNet('+5V'))	0
Clearance Constraint (Gap=0.6mm) (InNetClass('HV_IN'),(InNet('+6V'))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=2.54mm) (Preferred=0.305mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.152mm)	0
Hole Size Constraint (Min=0.025mm) (Max=100mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	1
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	1

Board Clearance Constraint (Gap=0mm) (All)	
Board Outline Clearance(Outline Edge): (0.15mm < 0.295mm) Between Text "D2" (9.4mm,48.9mm) on Bottom Overlay And Board Edge	