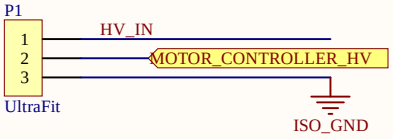
Pre-Charge

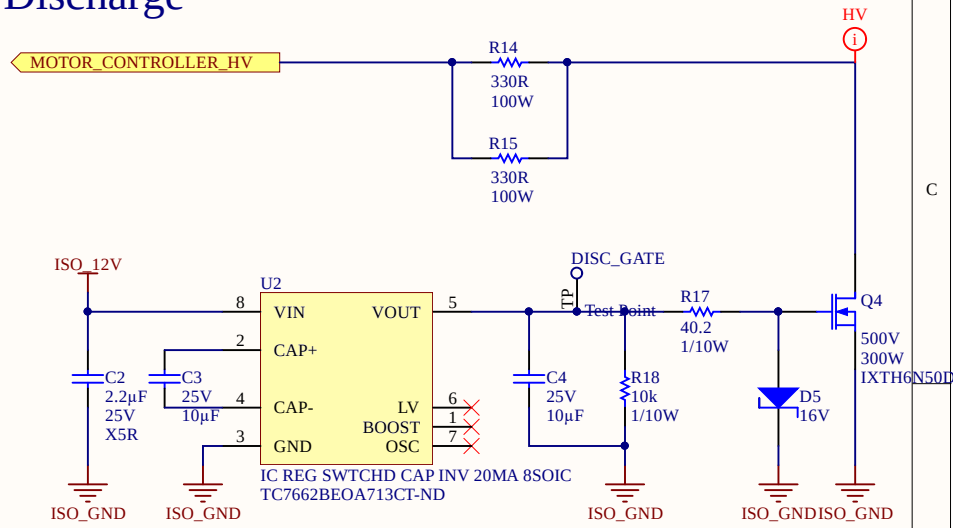
HEATSINK 2xTO-247_1
345-1573-ND

HEATSINK 4xTO-247
345-1574-ND

HV Connector

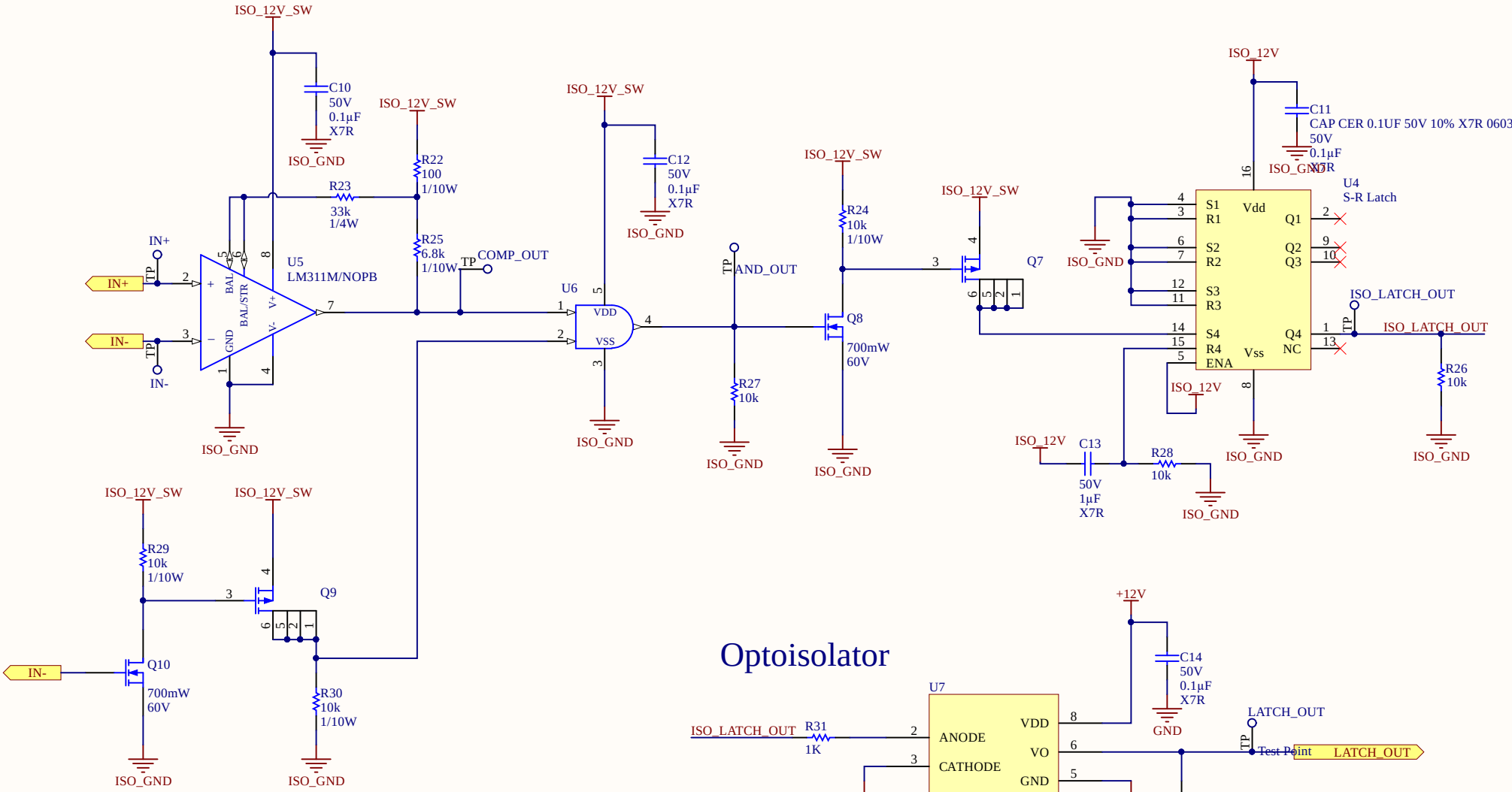


Discharge



Project: ***PreCharge.PrjPcb***		MIDNIGHT SUN
Title: *		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Author: Hanna Muratovic		
Size: Letter	Revision: 3.0	
Date: 2018-06-22	Sheet * of *	Website: www.uwmidsun.com

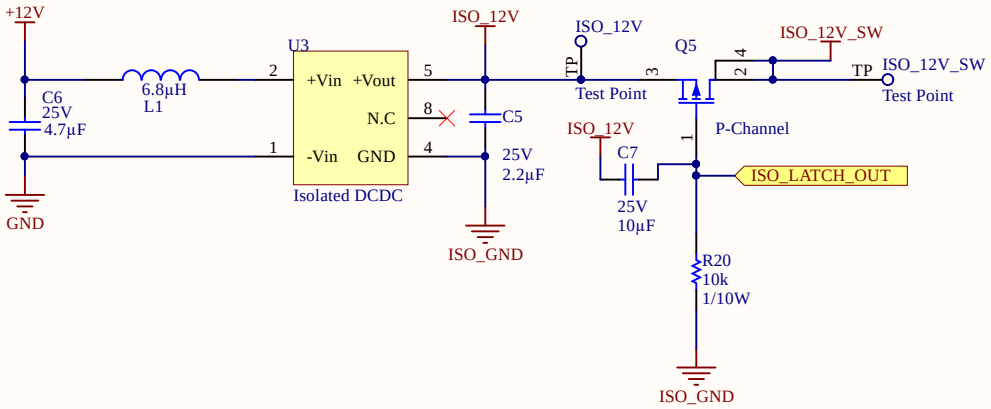
Logic



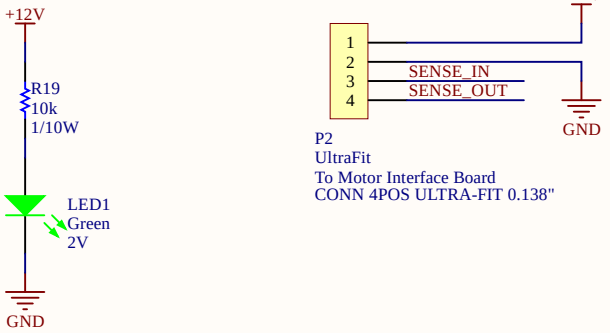
Optoisolator

Project: ***PreCharge.PrjPcb***		MIDNIGHT SUN
Title: *		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Author: Hanna Muratovic		
Size: Letter	Revision: 3.0	
Date: 2018-06-22	Sheet* of *	Website: www.uwmidsun.com

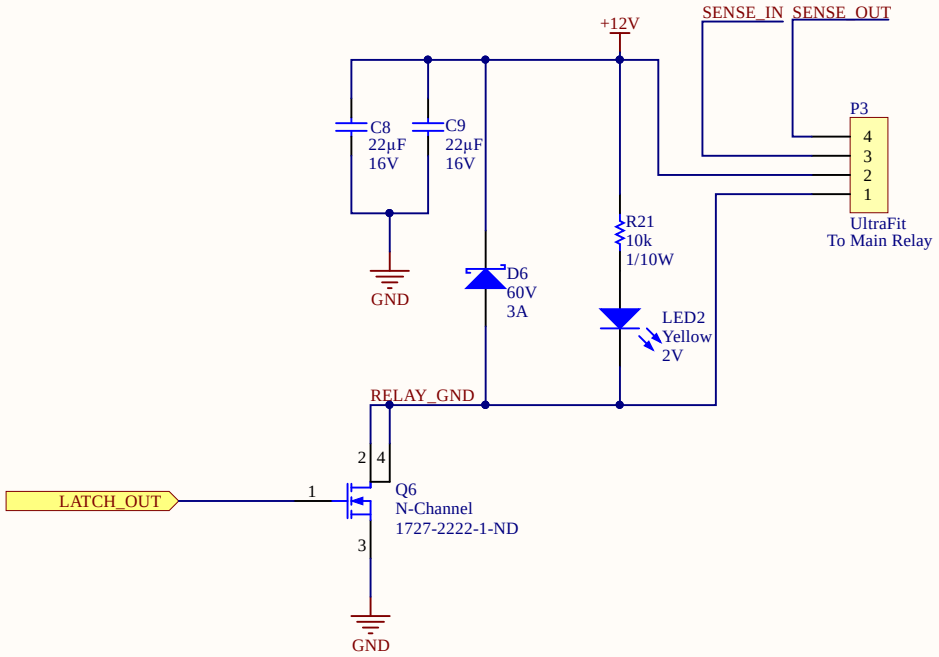
Isolated DC/DC



Connection to Motor Interface Board



Relay



Project: ***PreCharge.PrjPcb***		MIDNIGHT SUN
Title: *		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Author: Hanna Muratovic		
Size: Letter	Revision: 3.0	
Date: 2018-06-22	Sheet * of *	Website: www.uwmidsun.com

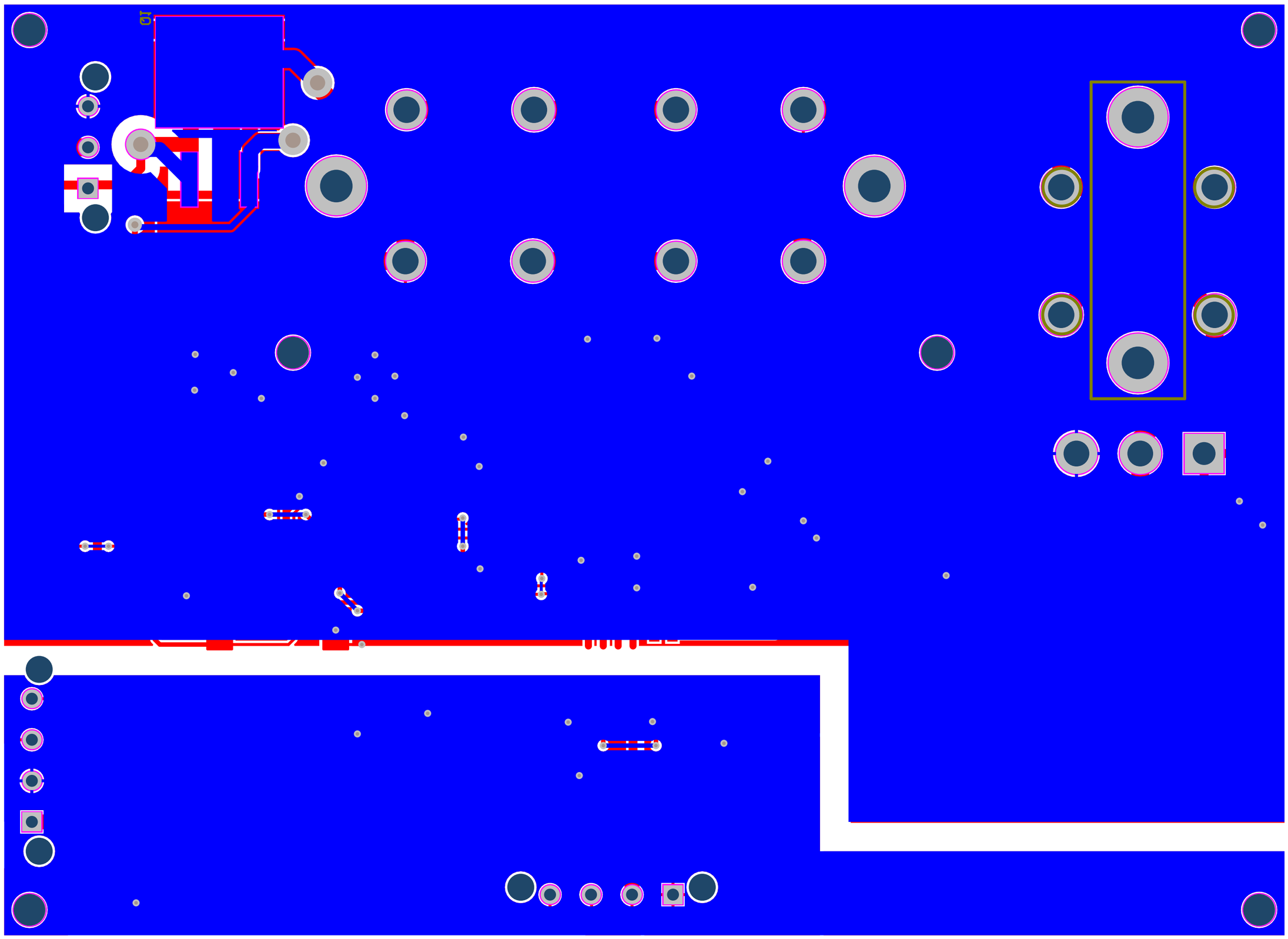
Bill of Materials

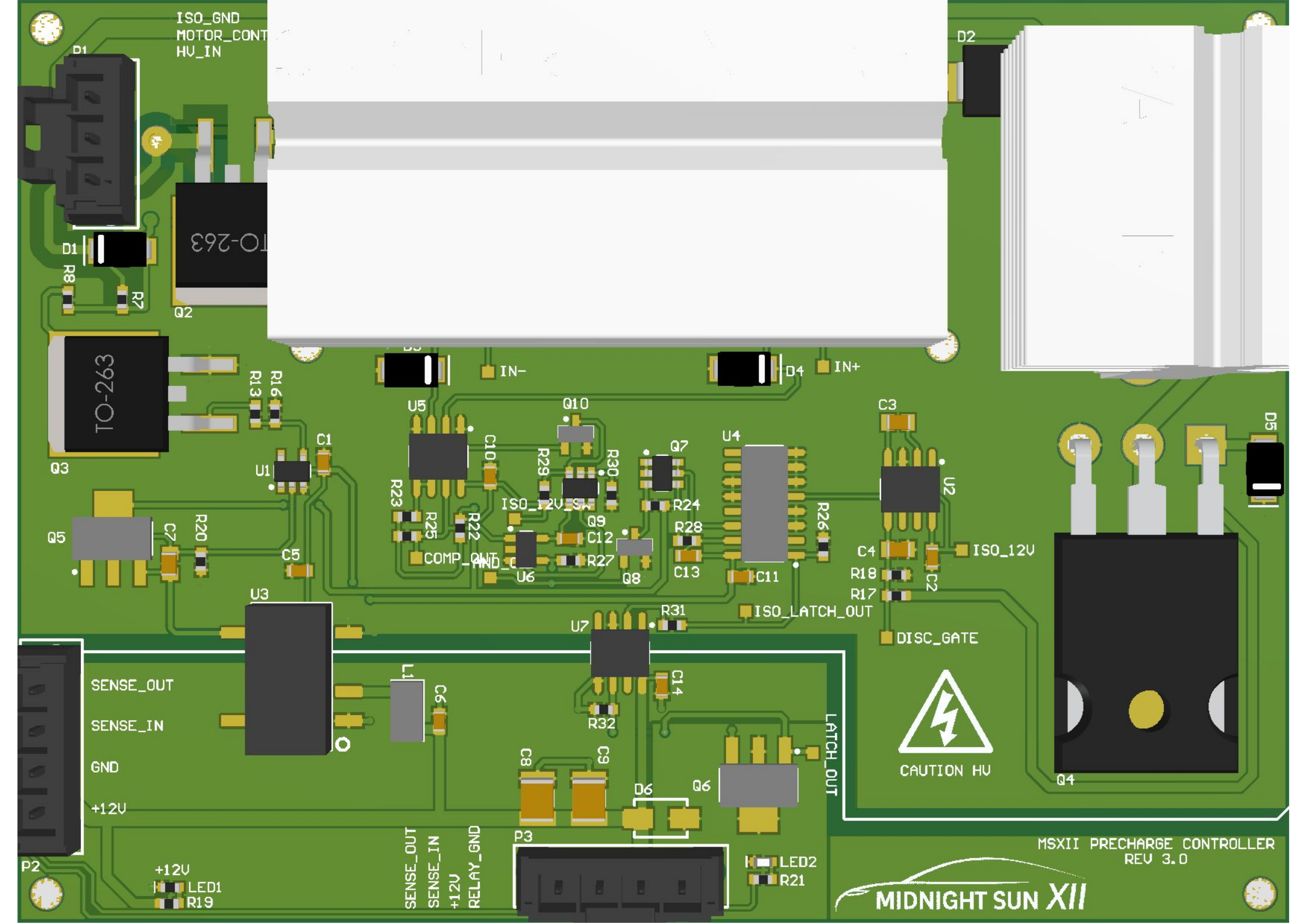
Project:	PreCharge.PrjPcb
Revision:	3.0
Project Lead:	Hanna Muratovic
Generated On:	2018-06-22 1:53:08 AM
Production Quantity:	1
Currency	CAD
Total Parts Count:	77

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Supplier Order Qty 1	Supplier Subtotal 1
HEATSINK 4xTO-247		Wakefield	OMNI-UNI-30-50-D	Digi-Key	345-1574-ND	5.44	1	$ 5.44
HEATSINK 2xTO-247_1		Wakefield	OMNI-UNI-30-25-D	Digi-Key	345-1573-ND	3.72	1	$ 3.72
CAP CER 0.1UF 50V 10% X7R 0603	C1	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.21	1	$ 0.21
CAP CER 2.2UF 25V 10% X5R 0603	C2	Murata	GRM188R61E225KA12D	Digi-Key	490-10731-1-ND	0.24	1	$ 0.24
CAP CER 10uF 25V 10% X5R 0805	C3	Murata	GRM21BR61E106KA73L	Digi-Key	490-5523-1-ND	0.71	1	$ 0.71
CAP CER 10uF 25V 10% X5R 0805	C4	Murata	GRM21BR61E106KA73L	Digi-Key	490-5523-1-ND	0.71	1	$ 0.71
CAP CER 2.2UF 25V 10% X5R 0603	C5	Murata	GRM188R61E225KA12D	Digi-Key	490-10731-1-ND	0.24	1	$ 0.24
CAP CER 4.7UF 25V 10% X5R 0603	C6	Murata	GRM188R61E475KE11D	Digi-Key	490-7203-1-ND	0.61	1	$ 0.61
CAP CER 10uF 25V 10% X5R 0805	C7	Murata	GRM21BR61E106KA73L	Digi-Key	490-5523-1-ND	0.71	1	$ 0.71
CAP CER 22UF 16V ±20% X5R 1210	C8	Murata	GRM32ER61C226ME20L	Digi-Key	490-1881-1-ND	2.45	1	$ 2.45
CAP CER 22UF 16V ±20% X5R 1210	C9	Murata	GRM32ER61C226ME20L	Digi-Key	490-1881-1-ND	2.45	1	$ 2.45
CAP CER 0.1UF 50V 10% X7R 0603	C10	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.21	1	$ 0.21
CAP CER 0.1UF 50V 10% X7R 0603	C11	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.21	1	$ 0.21
CAP CER 0.1UF 50V 10% X7R 0603	C12	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.21	1	$ 0.21
CAP CER 1UF 50V 10% X7R 0603	C13	Taiyo Yuden	UMK107AB7105KA-T	Digi-Key	587-3247-1-ND	0.39	1	$ 0.39
CAP CER 0.1UF 50V 10% X7R 0603	C14	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.21	1	$ 0.21
DIODE ZENER 16V 5W DO-214AA (SMB)	D1	MCC	SMBJ5353B-TP	Digi-Key	SMBJ5353B-TPMSCT-ND	0.9	1	$ 0.90
DIODE GEN PURP 800V 8A SMC	D2	Diodes	S8KC-13	Digi-Key	S8KCDICT-ND	0.9	1	$ 0.90
DIODE ZENER 16V 5W DO-214AA (SMB)	D3	MCC	SMBJ5353B-TP	Digi-Key	SMBJ5353B-TPMSCT-ND	0.9	1	$ 0.90
DIODE ZENER 16V 5W DO-214AA (SMB)	D4	MCC	SMBJ5353B-TP	Digi-Key	SMBJ5353B-TPMSCT-ND	0.9	1	$ 0.90
DIODE ZENER 16V 5W DO-214AA (SMB)	D5	MCC	SMBJ5353B-TP	Digi-Key	SMBJ5353B-TPMSCT-ND	0.9	1	$ 0.90
DIODE SCHOTTKY 60V 3A SMA	D6	Diodes	B360A-13-F	Digi-Key	B360A-FDICT-ND	0.64	1	$ 0.64
IND 6.8uH 260mA 20% 1210	L1	TDK	NLFV32T-6R8M-EF	Digi-Key	445-15776-1-ND	0.59	1	$ 0.59
LED GREEN CLEAR 2V 0603	LED1	Wurth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.19	1	$ 0.19
LED YELLOW CLEAR 2.1V 0603	LED2	Wurth Electronics	150060YS75000	Digi-Key	732-4981-1-ND	0.19	1	$ 0.19
CONN 3POS ULTRA-FIT 0.138"	P1	Molex	1722871103	Digi-Key	WM11702-ND	1.09	1	$ 1.09
CONN 4POS ULTRA-FIT 0.138"	P2	Molex	1722871104	Digi-Key	WM11703-ND	1.2	1	$ 1.20
CONN 4POS ULTRA-FIT 0.138"	P3	Molex	1722871104	Digi-Key	WM11703-ND	1.2	1	$ 1.20
MOSFET P-CH 500V 10A 300W TO-263	Q1	IXYS	IXTA10P50P	Digi-Key	IXTA10P50P-ND	7.93	1	$ 7.93
MOSFET P-CH 500V 10A 300W TO-263	Q2	IXYS	IXTA10P50P	Digi-Key	IXTA10P50P-ND	7.93	1	$ 7.93
MOSFET N-CH 650V 8A X2 TO-263	Q3	IXYS	IXTA8N65X2	Digi-Key	IXTA8N65X2-ND	3.79	1	$ 3.79
MOSFET DEPLETION N-CH 500V 6A TO247	Q4	IXYS	IXTH6N50D2	Digi-Key	IXTH6N50D2-ND	9.64	1	$ 9.64
MOSFET P-CH 60V 3A SOT223	Q5	Diodes	ZXMP6A17GQTA	Digi-Key	ZXMP6A17GQTADIDKR-ND	1.2	1	$ 1.20
MOSFET N-CH 55V 7A SOT223	Q6	Nexperia	BUK7880-55A/CUX	Digi-Key	1727-2222-1-ND	0.82	1	$ 0.82
MOSFET P-CH 30V 4A 1.6W SOT-23-6	Q7	STMicroelectronics	STT4P3LLH6	Digi-Key	497-15521-1-ND	0.9	1	$ 0.90
MOSFET N-CH 60V 310MA SOT23	Q8	Diodes	DMN65D8L-7	Digi-Key	DMN65D8L-7DICT-ND	0.27	1	$ 0.27
MOSFET P-CH 30V 4A 1.6W SOT-23-6	Q9	STMicroelectronics	STT4P3LLH6	Digi-Key	497-15521-1-ND	0.9	1	$ 0.90
MOSFET N-CH 60V 310MA SOT23	Q10	Diodes	DMN65D8L-7	Digi-Key	DMN65D8L-7DICT-ND	0.27	1	$ 0.27
RES 18 OHM 100W 5% TO-247	R1			Digi-Key	AP101 18R J-ND			
RES 18 OHM 100W 5% TO-247	R2			Digi-Key	AP101 18R J-ND			
RES 18 OHM 100W 5% TO-247	R3			Digi-Key	AP101 18R J-ND			
RES 18 OHM 100W 5% TO-247	R4			Digi-Key	AP101 18R J-ND			
RES SMD 470K OHM 0.1% 1/4W 1206	R5	Susumu	RG3216P-4703-B-T1	Digi-Key	RG32P470KBDKR-ND	0.88	1	$ 0.88
RES SMD 470K OHM 0.1% 1/4W 1206	R6	Susumu	RG3216P-4703-B-T1	Digi-Key	RG32P470KBDKR-ND	0.88	1	$ 0.88
RES 29.4K OHM 1% 1/10W 0603	R7	Yageo	RC0603FR-0729K4L	Digi-Key	311-29.4KHRCT-ND	0.13	1	$ 0.13
RES 470K OHM 1% 1/4W 0603	R8	Panasonic	ERJPA3F4703V	Digi-Key	P470KBYCT-ND	0.21	1	$ 0.21
RES SMD 29.4K OHM 1% 1/4W 1206	R9	Panasonic	ERJ-8ENF2942V	Digi-Key	P29.4KFCT-ND	0.15	1	$ 0.15
RES SMD 33K OHM 0.1% 1/4W 1206	R10	Yageo	RT1206BRD0733KL	Digi-Key	YAG2038CT-ND	0.9	1	$ 0.90
RES SMD 2K OHM 0.1% 1/4W 1206	R11	Panasonic	ERA-8AEB202V	Digi-Key	P2.0KBCCT-ND	0.88	1	$ 0.88
RES SMD 0 OHM JUMPER 1/4W 1206	R12	Vishay	CRCW12060000Z0EA	Digi-Key	541-0.0ECT-ND	0.13	1	$ 0.13
RES 22.1 OHM 1% 1/10W 0603	R13	Yageo	RC0603FR-0722R1L	Digi-Key	311-22.1HRCT-ND	0.13	1	$ 0.13
RES 330 OHM 100W 5% TO-247	R14			Digi-Key	AP101 330R J-ND			
RES 330 OHM 100W 5% TO-247	R15			Digi-Key	AP101 330R J-ND			
RES 10K OHM 1% 1/10W 0603	R16	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 40.2 OHM 0.5% 1/10W 0603	R17	Yageo	RT0603DRE0740R2L	Digi-Key	311-2576-1-ND	0.16	1	$ 0.16
RES 10K OHM 1% 1/10W 0603	R18	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 10K OHM 1% 1/10W 0603	R19	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 10K OHM 1% 1/10W 0603	R20	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 10K OHM 1% 1/10W 0603	R21	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 100 OHM 1% 1/10W 0603	R22	Yageo	RC0603FR-07100RL	Digi-Key	311-100HRCT-ND	0.13	1	$ 0.13
RES 33K OHM 1% 1/4W 0603	R23	Panasonic	ERJPA3F3302V	Digi-Key	P33KBYCT-ND	0.21	1	$ 0.21
RES 10K OHM 1% 1/10W 0603	R24	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 6.8k OHM 1% 1/10W 0603	R25	Stackpole Electronics	RMCF0603FT6K80	Digi-Key	RMCF0603FT6K80CT-ND	0.13	1	$ 0.13
RES 10K OHM 1% 1/10W 0603	R26	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 10K OHM 1% 1/10W 0603	R27	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 10K OHM 1% 1/10W 0603	R28	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 10K OHM 1% 1/10W 0603	R29	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 10K OHM 1% 1/10W 0603	R30	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 1K OHM 5% 1/10W 0603	R31	Yageo	RC0603JR-071KL	Digi-Key	311-1.0KGRCT-ND	0.13	1	$ 0.13
RES 10K OHM 1% 1/10W 0603	R32	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
IC INVERTER SCHMITT 1CH 5SSOP	U1	Rohm	BU4S584G2-TR	Digi-Key	BU4S584G2DKR-ND	0.9	1	$ 0.90
IC REG SWTCHD CAP INV 20MA 8SOIC	U2	Microchip	TC7662BEOA713	Digi-Key	TC7662BEOA713CT-ND	3.05	1	$ 3.05
IC DCDC ISOLATED 12V 1W 8-SMD 5-LEAD	U3	XP Power	ISE1212A	Digi-Key	1470-2950-1-ND	5.65	1	$ 5.65
IC SR LATCH 4CH 16SOIC	U4	Texas Instruments	CD4043BDR	Digi-Key	296-31496-1-ND	0.64	1	$ 0.64
IC COMPARATOR 8-SOIC	U5	TI National Semiconductor	LM311M/NOPB	Digi-Key	LM311MNS/NOPB-ND	1.16	1	$ 1.16
IC AND GATE 1CH 5-SSOP	U6	Rohm	BU4S81G2-TR	Digi-Key	BU4S81G2CT-ND	1	1	$ 1.00
IC DIGITAL ISO SI8715BC-A-IS	U7	Silicon Labs	SI8715BC-A-IS	Digi-Key	336-3027-ND	1.33	1	$ 1.33
							Total:	$ 82.31

ISO_GND

ISO_GND
MOTOR_CONTROLLER
HV_IN
P1
D2
R3
R4
R15
D1
R8
R7
Q2
R1
R2
R5
R9
R11
R12
R10
R6
D3
D4
IN-
IN+
R13
R14
U5
Q10
C3
D5
C1
U1
C10
R29
R30
Q7
U4
U2
Q3
R23
R25
R22
ISO_12V_SW
Q9
R24
R28
R26
C12
Q5
C7
R20
C5
COMP_OUT
GND_OUT
U6
R27
Q8
C13
C11
C4
ISO_12V
R18
R17
C2
U3
R31
ISO_LATCH_OUT
U7
DISC_GATE
SENSE_OUT
SENSE_IN
GND
+12V
L1
C6
C14
R32
C8
C9
D6
Q6
LATCH_OUT
CAUTION HV
Q4
P2
P3
+12V
LED1
R19
SENSE_OUT
SENSE_IN
+12V
RELAY_GND
LED2
R21
MSXII PRECHARGE CONTROLLER
REV 3.0
MIDNIGHT SUN XII




ISO_GND
MOTOR_CONT
HV_IN
P1
D1
R8
R7
Q2
TO-263
D2
TO-263
Q3
R13
R16
U1
C1
U5
C10
R23
R25
R22
COMP_OUT
IN-
D3
D4
IN+
Q10
R29
R30
Q7
ISO_12V_SW
Q9
C12
R27
U6
Q8
R24
R28
C13
U4
C11
R26
C3
U2
D5
C4
R18
R17
C2
ISO_12V
ISO_LATCH_OUT
DISC_GATE
Q5
C7
R20
C5
U3
L1
C6
U7
R31
C14
R32
C8
C9
D6
Q6
LATCH_OUT
CAUTION HV
Q4
SENSE_OUT
SENSE_IN
GND
+12V
P2
P3
+12V
LED1
R19
SENSE_OUT
SENSE_IN
+12V
RELAY_GND
LED2
R21
MSXII PRECHARGE CONTROLLER
REV 3.0
MIDNIGHT SUN XII

Electrical Rules Check Report

Class	Document	Message
Error	High Voltage Section.SchDoc	Duplicate Component Designators * at 4070.224mil,7606.662mil and 5212.293mil,7562.396mil
Error	High Voltage Section.SchDoc	Duplicate Component Designators * at 5212.293mil,7562.396mil and 4070.224mil,7606.662mil
Warning	Logic.SchDoc	Net NetQ9_1 has no driving source (Pin Q9-1,Pin Q9-2,Pin Q9-5,Pin Q9-6,Pin R30-1,Pin U6-2)
Warning	High Voltage Section.SchDoc	Off grid at 3760.97mil,8006.662mil
Warning	High Voltage Section.SchDoc	Off grid at 4903.039mil,7962.396mil

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII_PreChargeControlle

Warnings 0

Rule Violations 164

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (All),(All)	1
Clearance Constraint (Gap=0.8mm) (InPolygon and InNet('ISO_GND')),(InNet('TO DISCHARGE RESISTOR') or	0
Clearance Constraint (Gap=1.25mm) (InNet('HV_IN')),(All)	53
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.2mm) (Max=2.54mm) (Preferred=0.35mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	10
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)	23
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	59
Silk to Silk (Clearance=0.254mm) (All),(All)	18
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=100mm) (Prefered=12.7mm) (All)	0
Total	164

Clearance Constraint (Gap=0.2mm) (All),(All)
Clearance Constraint: (0.171mm < 0.2mm) Between Pad Q1-4(18.7mm,73.9mm) on Bottom Layer And Via (25mm,68.1mm) from Component Side to

Clearance Constraint (Gap=1.25mm) (InNet('HV_IN')),(All)
Clearance Constraint: (1.08mm < 1.25mm) Between Pad D1-2(7.036mm,58.2mm) on Component Side And Pad P1-(8.13mm,61.5mm) on Multi-Layer
Clearance Constraint: (Collision < 1.25mm) Between Pad D1-2(7.036mm,58.2mm) on Component Side And Track (3.2mm,58.3mm)(7.6mm,58.3mm) on
Clearance Constraint: (Collision < 1.25mm) Between Pad D1-2(7.036mm,58.2mm) on Component Side And Track (7.25mm,57.75mm)(9.1mm,55.9mm) on
Clearance Constraint: (Collision < 1.25mm) Between Pad D1-2(7.036mm,58.2mm) on Component Side And Track (7.6mm,58.3mm)(7.8mm,58.3mm) on
Clearance Constraint: (1.047mm < 1.25mm) Between Pad P1-(8.13mm,61.5mm) on Multi-Layer And Track (7.5mm,64mm)(7.5mm,64.281mm) on
Clearance Constraint: (1.047mm < 1.25mm) Between Pad P1-(8.13mm,61.5mm) on Multi-Layer And Track (7.5mm,64mm)(7.8mm,64.3mm) on Component
Clearance Constraint: (Collision < 1.25mm) Between Pad P1-1(7.5mm,64mm) on Multi-Layer And Track (3.881mm,64.281mm)(7.5mm,64.281mm) on
Clearance Constraint: (Collision < 1.25mm) Between Pad P1-1(7.5mm,64mm) on Multi-Layer And Track (7.5mm,64mm)(7.5mm,64.281mm) on Component
Clearance Constraint: (Collision < 1.25mm) Between Pad P1-1(7.5mm,64mm) on Multi-Layer And Track (7.5mm,64mm)(7.8mm,64.3mm) on Component
Clearance Constraint: (Collision < 1.25mm) Between Pad P1-1(7.5mm,64mm) on Multi-Layer And Track (7.8mm,64.3mm)(10.6mm,64.3mm) on Component
Clearance Constraint: (Collision < 1.25mm) Between Pad Q1-3(16.16mm,64.75mm) on Bottom Layer And Track
Clearance Constraint: (0.697mm < 1.25mm) Between Pad Q1-4(18.7mm,73.9mm) on Bottom Layer And Via (12mm,67.75mm) from Component Side to
Clearance Constraint: (Collision < 1.25mm) Between Pad Q2-3(16.26mm,67.35mm) on Component Side And Track (12mm,67.75mm)(16.05mm,67.75mm)
Clearance Constraint: (Collision < 1.25mm) Between Pad Q2-3(16.26mm,67.35mm) on Component Side And Track (16.05mm,67.75mm)(16.3mm,68mm)
Clearance Constraint: (0.934mm < 1.25mm) Between Pad R7-2(9.1mm,54.75mm) on Component Side And Track (4.4mm,53.2mm)(9.1mm,53.2mm) on
Clearance Constraint: (0.535mm < 1.25mm) Between Pad R7-2(9.1mm,54.75mm) on Component Side And Track (7.25mm,57.75mm)(9.1mm,55.9mm) on
Clearance Constraint: (0.934mm < 1.25mm) Between Pad R7-2(9.1mm,54.75mm) on Component Side And Track (9.1mm,53.2mm)(11mm,53.2mm) on
Clearance Constraint: (Collision < 1.25mm) Between Pad R7-2(9.1mm,54.75mm) on Component Side And Track (9.1mm,55.066mm)(9.1mm,55.9mm) on
Clearance Constraint: (Collision < 1.25mm) Between Track (10.6mm,64.3mm)(12mm,65.7mm) on Component Side And Track
Clearance Constraint: (1.034mm < 1.25mm) Between Track (10.6mm,64.3mm)(12mm,65.7mm) on Component Side And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (10.6mm,64.3mm)(12mm,65.7mm) on Component Side And Track
Clearance Constraint: (0.419mm < 1.25mm) Between Track (10.6mm,64.3mm)(12mm,65.7mm) on Component Side And Via (12mm,67.75mm) from
Clearance Constraint: (Collision < 1.25mm) Between Track (12.084mm,67.75mm)(12.519mm,67.315mm) on Bottom Layer And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (12.084mm,67.75mm)(12.519mm,67.315mm) on Bottom Layer And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (12.084mm,67.75mm)(12.519mm,67.315mm) on Bottom Layer And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (12.084mm,67.75mm)(12.519mm,67.315mm) on Bottom Layer And Via (12mm,67.75mm) from
Clearance Constraint: (Collision < 1.25mm) Between Track (12.519mm,67.315mm)(13.595mm,67.315mm) on Bottom Layer And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (12.519mm,67.315mm)(13.595mm,67.315mm) on Bottom Layer And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (12.519mm,67.315mm)(13.595mm,67.315mm) on Bottom Layer And Via (12mm,67.75mm) from
Clearance Constraint: (Collision < 1.25mm) Between Track (12mm,65.7mm)(12mm,67.75mm) on Component Side And Track
Clearance Constraint: (1.218mm < 1.25mm) Between Track (12mm,65.7mm)(12mm,67.75mm) on Component Side And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (12mm,65.7mm)(12mm,67.75mm) on Component Side And Via (12mm,67.75mm) from
Clearance Constraint: (0.302mm < 1.25mm) Between Track (12mm,67.75mm)(12.084mm,67.75mm) on Bottom Layer And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (12mm,67.75mm)(12.084mm,67.75mm) on Bottom Layer And Via (12mm,67.75mm) from
Clearance Constraint: (Collision < 1.25mm) Between Track (12mm,67.75mm)(16.05mm,67.75mm) on Component Side And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (12mm,67.75mm)(16.05mm,67.75mm) on Component Side And Via (12mm,67.75mm) from
Clearance Constraint: (Collision < 1.25mm) Between Track (13.595mm,67.315mm)(16.16mm,64.75mm) on Bottom Layer And Via (12mm,67.75mm) from
Clearance Constraint: (Collision < 1.25mm) Between Track (2.7mm,58.8mm)(2.7mm,63.1mm) on Component Side And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (2.7mm,58.8mm)(2.7mm,63.1mm) on Component Side And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (2.7mm,58.8mm)(2.7mm,63.1mm) on Component Side And Track
Clearance Constraint: (0.908mm < 1.25mm) Between Track (2.7mm,58.8mm)(2.7mm,63.1mm) on Component Side And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (2.7mm,58.8mm)(3.2mm,58.3mm) on Component Side And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (2.7mm,63.1mm)(3.881mm,64.281mm) on Component Side And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (3.2mm,58.3mm)(7.6mm,58.3mm) on Component Side And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (3.2mm,58.3mm)(7.6mm,58.3mm) on Component Side And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (3.881mm,64.281mm)(7.5mm,64.281mm) on Component Side And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (3.881mm,64.281mm)(7.5mm,64.281mm) on Component Side And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (3.881mm,64.281mm)(7.5mm,64.281mm) on Component Side And Track
Clearance Constraint: (0.271mm < 1.25mm) Between Track (7.25mm,57.75mm)(9.1mm,55.9mm) on Component Side And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (7.25mm,57.75mm)(9.1mm,55.9mm) on Component Side And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (7.5mm,64mm)(7.5mm,64.281mm) on Component Side And Track
Clearance Constraint: (Collision < 1.25mm) Between Track (7.5mm,64mm)(7.5mm,64.281mm) on Component Side And Track

Clearance Constraint (Gap=1.25mm) (InNet('HV_IN')),(All)
Clearance Constraint: (Collision < 1.25mm) Between Track (7.5mm,64mm)(7.8mm,64.3mm) on Component Side And Track

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (2.775mm > 2.54mm) Pad *-6(74.64mm,64.2mm) on Multi-Layer Actual Hole Size = 2.775mm
Hole Size Constraint: (2.775mm > 2.54mm) Pad *-6(97.15mm,70.07mm) on Multi-Layer Actual Hole Size = 2.775mm
Hole Size Constraint: (2.775mm > 2.54mm) Pad *-7(28.7mm,64.2mm) on Multi-Layer Actual Hole Size = 2.775mm
Hole Size Constraint: (2.775mm > 2.54mm) Pad *-7(97.15mm,49.13mm) on Multi-Layer Actual Hole Size = 2.775mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(107.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(107.5mm,77.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,77.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(25mm,50mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(80mm,50mm) on Multi-Layer Actual Hole Size = 2.7mm

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C10-1(40.9mm,39.35mm) on Component Side And Pad C10-2(40.9mm,38mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C1-1(26.5mm,39.2mm) on Component Side And Pad C1-2(26.5mm,40.55mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C11-1(63.25mm,30mm) on Component Side And Pad C11-2(61.9mm,30mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C12-1(48.45mm,33.3mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C13-1(57.35mm,31.8mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.3mm) Between Pad C13-1(57.35mm,31.8mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.3mm) Between Pad C13-2(58.7mm,31.8mm) on Component Side And Pad R28-2(58.7mm,33.1mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C14-1(55.75mm,21.225mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C2-1(79.11mm,31mm) on Component Side And Pad C2-2(79.11mm,32.35mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C5-1(23.725mm,30.5mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C6-1(36.5mm,18.15mm) on Component Side And Pad C6-2(36.5mm,16.8mm)
Minimum Solder Mask Sliver Constraint: (0.198mm < 0.3mm) Between Pad Q7-1(54.4mm,39.9mm) on Component Side And Pad Q7-2(54.4mm,38.95mm)
Minimum Solder Mask Sliver Constraint: (0.198mm < 0.3mm) Between Pad Q7-2(54.4mm,38.95mm) on Component Side And Pad Q7-3(54.4mm,38mm) on
Minimum Solder Mask Sliver Constraint: (0.198mm < 0.3mm) Between Pad Q7-4(57.13mm,38mm) on Component Side And Pad Q7-5(57.13mm,38.95mm)
Minimum Solder Mask Sliver Constraint: (0.198mm < 0.3mm) Between Pad Q7-5(57.13mm,38.95mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.198mm < 0.3mm) Between Pad Q9-1(49.65mm,39mm) on Component Side And Pad Q9-2(48.7mm,39mm) on
Minimum Solder Mask Sliver Constraint: (0.198mm < 0.3mm) Between Pad Q9-2(48.7mm,39mm) on Component Side And Pad Q9-3(47.75mm,39mm) on
Minimum Solder Mask Sliver Constraint: (0.198mm < 0.3mm) Between Pad Q9-4(47.75mm,36.27mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.198mm < 0.3mm) Between Pad Q9-5(48.7mm,36.27mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U1-1(22.82mm,37.75mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U1-2(23.77mm,37.75mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U6-1(42.65mm,33.3mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U6-2(42.65mm,32.35mm) on Component Side And Pad

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Arc (103.65mm,53.19mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Arc (103.65mm,64.07mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Arc (34.64mm,57.7mm) on Top Overlay And Pad R1-1(34.6mm,57.8mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Arc (34.64mm,70.7mm) on Top Overlay And Pad R3-1(34.7mm,70.7mm) on
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Arc (42.65mm,34.15mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Arc (45.52mm,57.7mm) on Top Overlay And Pad R1-2(45.48mm,57.8mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Arc (45.52mm,70.7mm) on Top Overlay And Pad R3-2(45.58mm,70.7mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Arc (57.76mm,57.7mm) on Top Overlay And Pad R2-1(57.7mm,57.8mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Arc (57.76mm,70.7mm) on Top Overlay And Pad R4-1(57.7mm,70.7mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Arc (68.64mm,57.7mm) on Top Overlay And Pad R2-2(68.58mm,57.8mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Arc (68.64mm,70.7mm) on Top Overlay And Pad R4-2(68.58mm,70.7mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Arc (90.65mm,53.22mm) on Bottom Overlay And Pad R14-2(90.6mm,53.22mm)
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Arc (90.65mm,64.1mm) on Bottom Overlay And Pad R14-1(90.6mm,64.1mm) on
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad C11-1(63.25mm,30mm) on Component Side And Text "C11"
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad COMP_OUT-TP(34.5mm,31.6mm) on Component Side And Text
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D1-2(7.036mm,58.2mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D3-2(36.1mm,47.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D4-2(64.8mm,48mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D5-2(107.8mm,37.336mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D6-1(57.7mm,9.05mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D6-1(57.7mm,9.05mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D6-2(53.7mm,9.05mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D6-2(53.7mm,9.05mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.253mm < 0.254mm) Between Pad L1-1(33.75mm,16.8mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.253mm < 0.254mm) Between Pad L1-1(33.75mm,16.8mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.253mm < 0.254mm) Between Pad L1-1(33.75mm,16.8mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.253mm < 0.254mm) Between Pad L1-2(33.75mm,20mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.243mm < 0.254mm) Between Pad L1-2(33.75mm,20mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.253mm < 0.254mm) Between Pad L1-2(33.75mm,20mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED1-2(12.5mm,3.1mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED2-2(63.75mm,5.29mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad Q2-4(18.8mm,58.2mm) on Component Side And Text "Q2"
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad Q5-1(6mm,30.4mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad Q5-2(8.3mm,30.4mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad Q5-3(10.6mm,30.4mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad Q5-4(8.3mm,36.2mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad Q6-1(66.4mm,14.85mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad Q6-2(64.1mm,14.85mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad Q6-3(61.8mm,14.85mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad Q6-4(64.1mm,9.05mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.006mm < 0.254mm) Between Pad Q9-4(47.75mm,36.27mm) on Component Side And Text "ISO_12V_SW"
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad Q9-5(48.7mm,36.27mm) on Component Side And Text "ISO_12V_SW"
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad Q9-6(49.65mm,36.27mm) on Component Side And Text "ISO_12V_SW"
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R10-1(65.725mm,52.8mm) on Component Side And Text "R10"
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R10-2(63.075mm,52.8mm) on Component Side And Text "R10"
Silk To Solder Mask Clearance Constraint: (0.039mm < 0.254mm) Between Pad R1-1(34.6mm,57.8mm) on Multi-Layer And Text "R1"
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R12-1(58.725mm,52.8mm) on Component Side And Text "R12"
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R12-2(56.075mm,52.8mm) on Component Side And Text "R12"
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R14-1(90.6mm,64.1mm) on Multi-Layer And Text "R14"
Silk To Solder Mask Clearance Constraint: (0.049mm < 0.254mm) Between Pad R2-1(57.7mm,57.8mm) on Multi-Layer And Text "R2"
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad R27-1(48.65mm,31.4mm) on Component Side And Text "R27"
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R29-1(45.6mm,36.27mm) on Component Side And Text "ISO_12V_SW"

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R6-1(72.325mm,52.8mm) on Component Side And Text "R6"
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R6-2(69.675mm,52.8mm) on Component Side And Text "R6"
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad U3-1(28.65mm,17.5mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad U3-2(28.65mm,20.04mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad U3-4(28.65mm,25.12mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad U6-3(42.65mm,31.4mm) on Component Side And Text "AND_OUT"
Silk To Solder Mask Clearance Constraint: (0.053mm < 0.254mm) Between Pad U6-4(45.4mm,31.4mm) on Component Side And Text "AND_OUT"

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Arc (34.64mm,57.7mm) on Top Overlay And Text "R1" (31.922mm,57.386mm) on Top
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Arc (57.76mm,57.7mm) on Top Overlay And Text "R2" (59.329mm,57.504mm) on Top
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "AND_OUT" (39.5mm,30.8mm) on Top Overlay And Text "COMP_OUT"
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "AND_OUT" (39.5mm,30.8mm) on Top Overlay And Text "U6" (43.3mm,29.6mm) on
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "AND_OUT" (39.5mm,30.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "AND_OUT" (39.5mm,30.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "AND_OUT" (39.5mm,30.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.062mm < 0.254mm) Between Text "L1" (33.4mm,22.3mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.099mm < 0.254mm) Between Text "P1" (4.9mm,75.1mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "P1" (4.9mm,75.1mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.197mm < 0.254mm) Between Text "P3" (43.1mm,7.1mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.168mm < 0.254mm) Between Text "P3" (43.1mm,7.1mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "R10" (63.4mm,53.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "R12" (56.4mm,53.65mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "R6" (70.4mm,53.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.238mm < 0.254mm) Between Text "U3" (20.3mm,28.1mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "U6" (43.3mm,29.6mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.24mm < 0.254mm) Between Text "U6" (43.3mm,29.6mm) on Top Overlay And Track