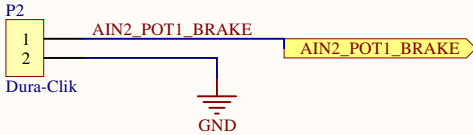
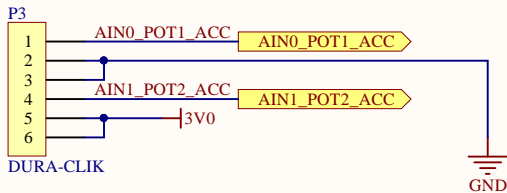


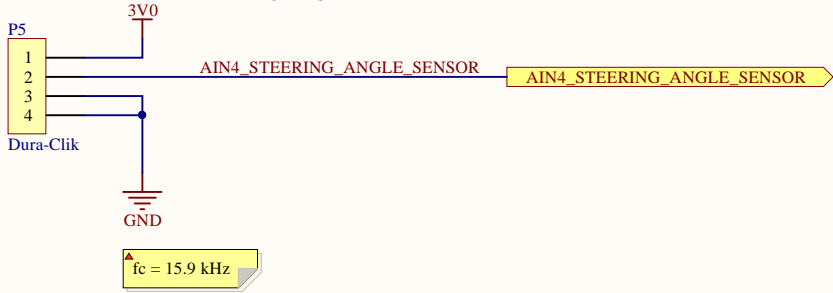
Brake Pedal Connector



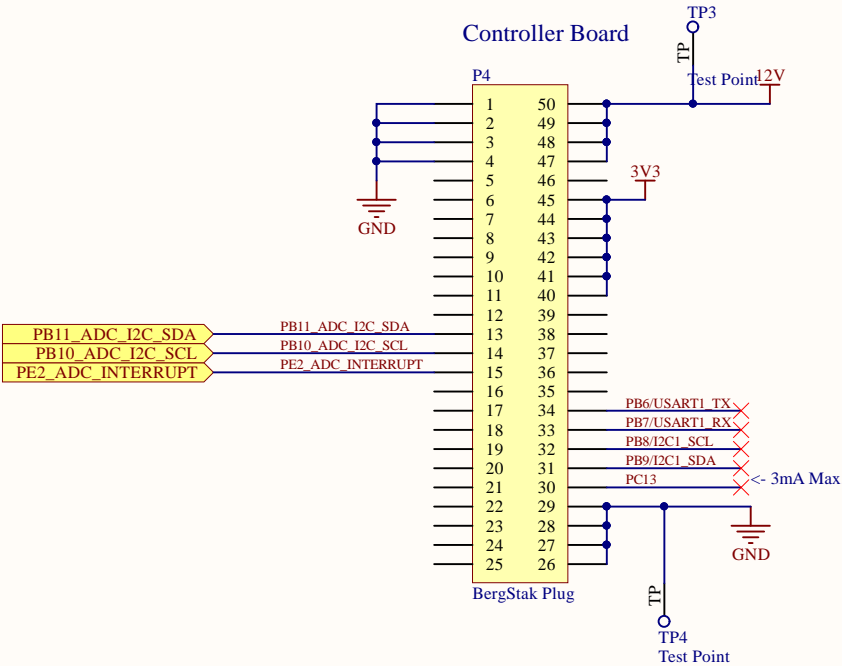
Accelerator Pedal Connector



Steering Angle Sensor



Controller Board



PROJECT	MSXII_PedalBoard.PrjPcb		
DOCUMENT	Title		
PART NUMBER	VARIANT	[No Variations]	
DRAWN BY	REVISION	2.1	
LAST MODIFIED	2019-01-18	SHEET	* OF *

MIDNIGHT

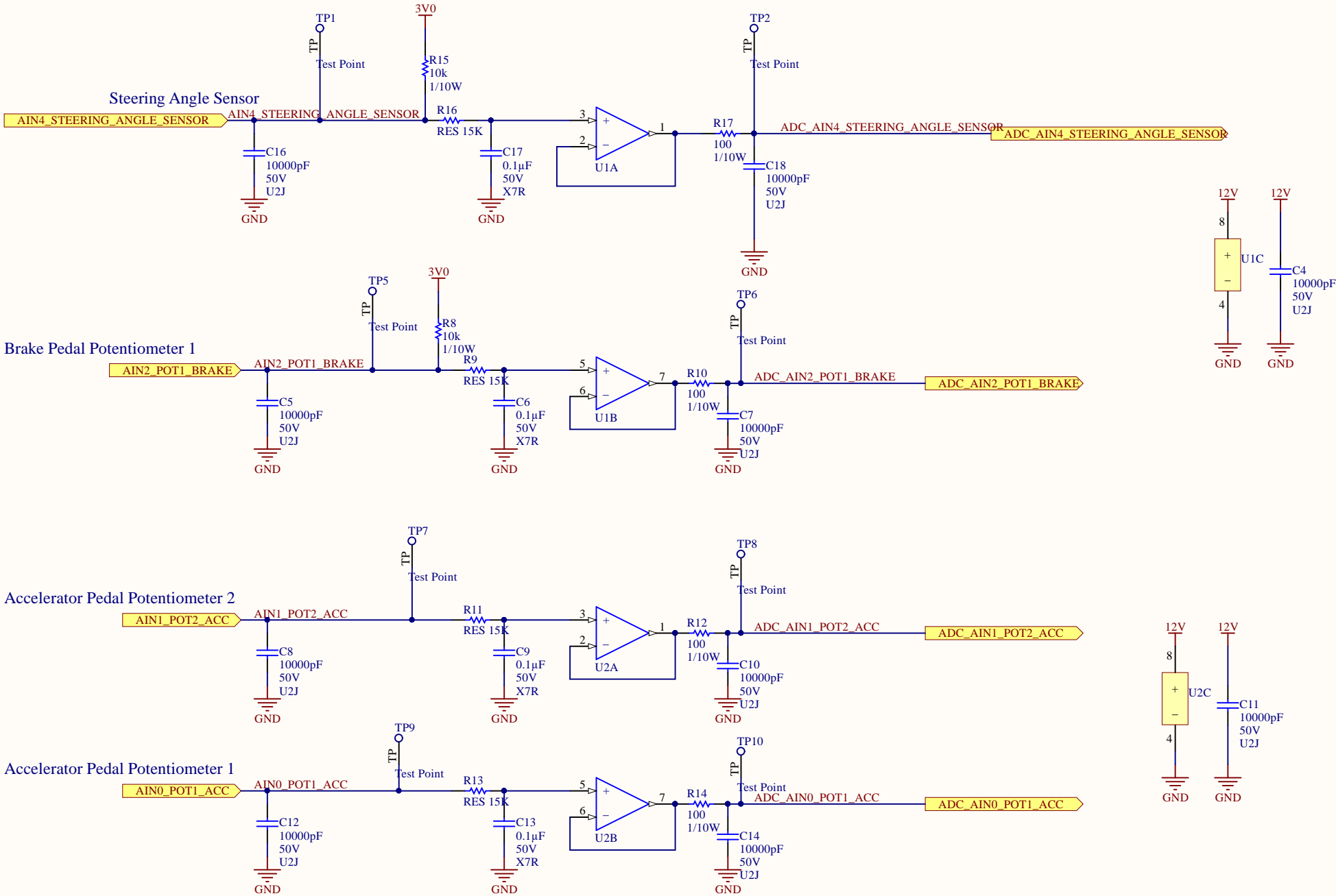
SUN

Engineering 5 - 1002
University of Waterloo
(519) 888-4567 x32978
hardware@uwmidsun.com

fc = 116.17[Hz]

RC Low Pass Filter

fc = 159154.94[Hz]



PROJECT		MSXII_PedalBoard.PrjPcb	
DOCUMENT		Title	
PART NUMBER		VARIANT	[No Variations]
DRAWN BY		REVISION	2.1
LAST MODIFIED		SHEET	* OF *
		2019-01-18	

MIDNIGHT

SUN

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P2

P3

BRAKE

ACCEL

P5

TP15

TP5

R9

U1

C6

C8

TP7

C12

C9

TP9

C16

C21

U5

C20

C4

+1dd

R15

C13

R11

U2

TP10

C17

R16

TP1

TP2

C18

R10

C20

R12

TP6

TP8

R14

STEERING ANGLE

P1

GND

TP4

TP3

ILED1

R1

12V

POWER

PEDAL BOARD

REV 3.0

P4

TP2

C18

R10

C20

R12

TP6

TP8

R14

TP2

C18

R10

C20

R12

TP6

TP8

R14

TP2

C18

R10

C20

R12

TP6

TP8

R14

TP2

C18

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TP2

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R10

C20

R12

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R10

C20

R12

TP6

TP8

R14

TP2

C18

R10

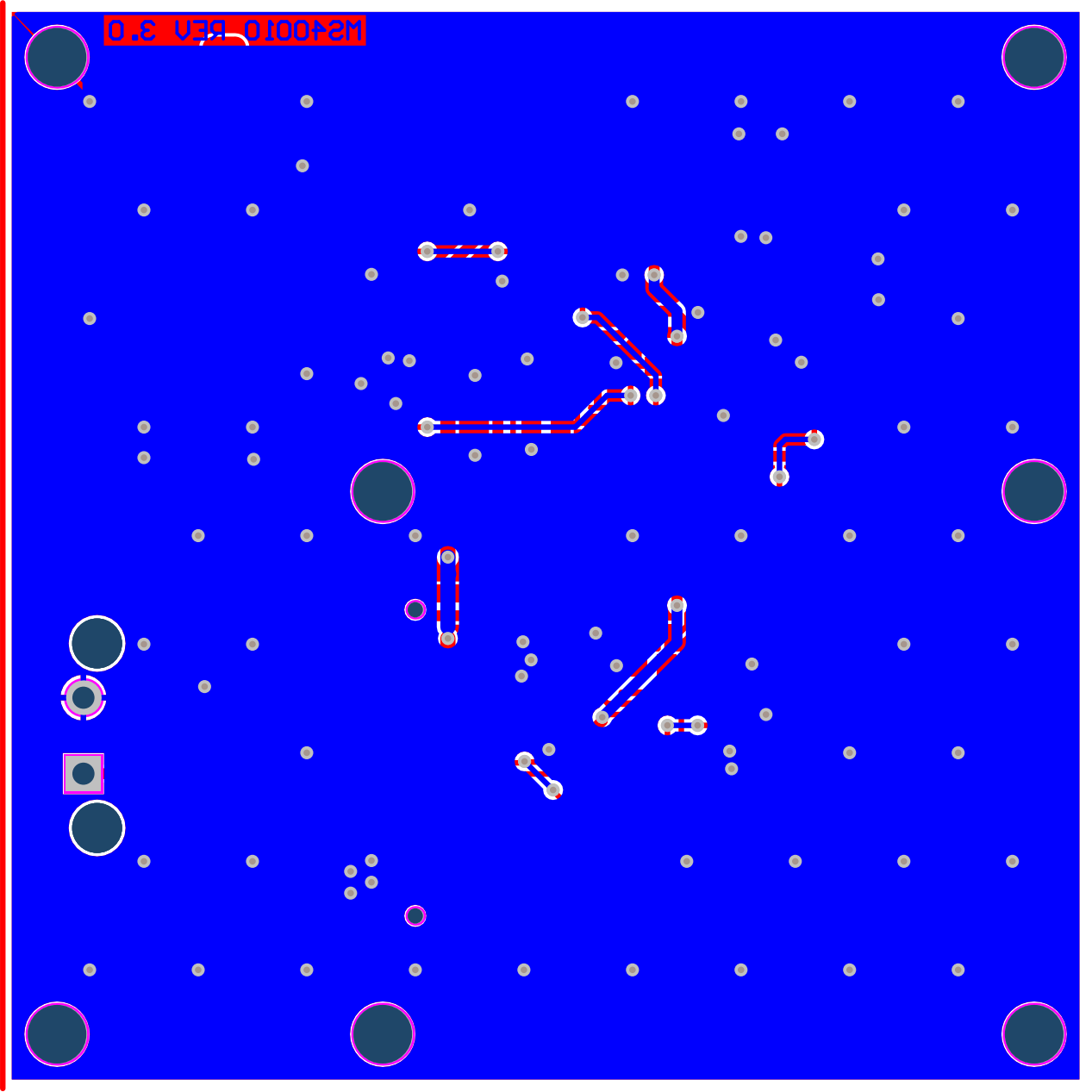
C20

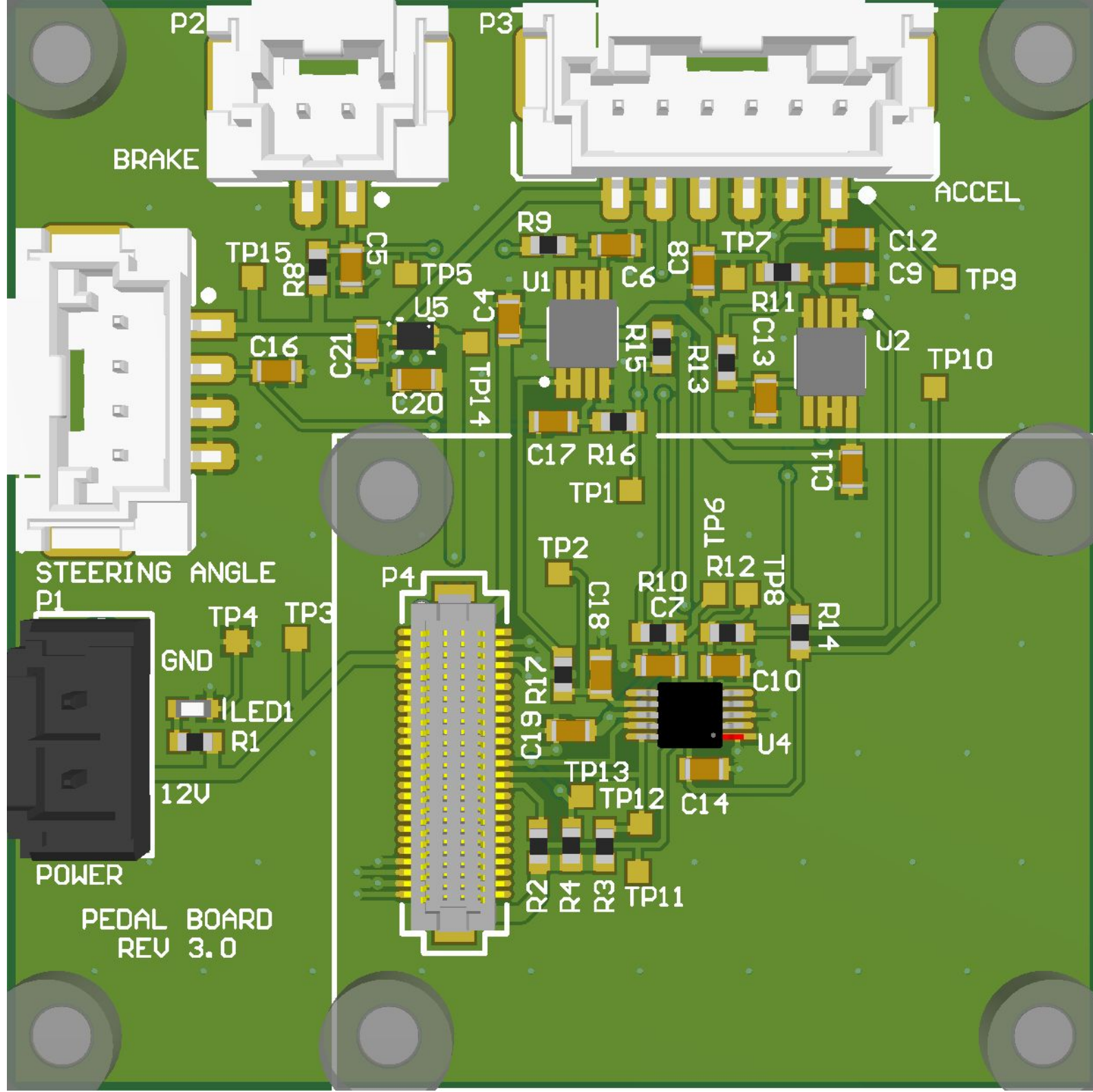
R12

TP6

TP8

R14





Electrical Rules Check Report

Class	Document	Message
Warning	PedalBoardAnalogInputs.SchDoc	Net NetC6_1 has no driving source (Pin C6-1,Pin R9-1,Pin U1-5)
Warning	PedalBoardAnalogInputs.SchDoc	Net NetC9_1 has no driving source (Pin C9-1,Pin R11-1,Pin U2-3)
Warning	PedalBoardAnalogInputs.SchDoc	Net NetC13_1 has no driving source (Pin C13-1,Pin R13-1,Pin U2-5)
Warning	PedalBoardAnalogInputs.SchDoc	Net NetC17_1 has no driving source (Pin C17-1,Pin R16-1,Pin U1-3)

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII_PedalBoard\Pedal Bc

Warnings 0

Rule Violations 46

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=2.54mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.05mm) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.1mm) (All),(All)	4
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	26
Silk to Silk (Clearance=0.254mm) (All),(All)	10
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	6
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	46

Minimum Solder Mask Sliver (Gap=0.1mm) (All),(All)	
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.1mm) Between Pad U5-1(18.01mm,34.871mm) on Top Layer And Pad U5-5(18.725mm,34.571mm)	
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.1mm) Between Pad U5-2(18.01mm,34.271mm) on Top Layer And Pad U5-5(18.725mm,34.571mm)	
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.1mm) Between Pad U5-3(19.45mm,34.271mm) on Top Layer And Pad U5-5(18.725mm,34.571mm)	
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.1mm) Between Pad U5-4(19.45mm,34.871mm) on Top Layer And Pad U5-5(18.725mm,34.571mm)	

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C10-2(33.564mm,19.475mm) on Top Layer And Text "C10"
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C16-1(11.7mm,32.95mm) on Top Layer And Text "C16"
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C16-2(13.05mm,32.95mm) on Top Layer And Text "C16"
Silk To Solder Mask Clearance Constraint: (0.096mm < 0.178mm) Between Pad C20-1(19.45mm,32.571mm) on Top Layer And Text "C20"
Silk To Solder Mask Clearance Constraint: (0.096mm < 0.178mm) Between Pad C20-2(18.1mm,32.571mm) on Top Layer And Text "C20"
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C4-2(23mm,36mm) on Top Layer And Text "C4" (22.25mm,35.325mm) on
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C5-1(15.8mm,38.357mm) on Top Layer And Text "C5"
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C8-1(31.9mm,38.207mm) on Top Layer And Text "C8" (31.15mm,37.5mm)
Silk To Solder Mask Clearance Constraint: (0.135mm < 0.178mm) Between Pad P2-3(19.4mm,46.35mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.155mm < 0.178mm) Between Pad P5-7(3.714mm,25.457mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.17mm < 0.178mm) Between Pad P5-7(3.714mm,38.657mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.131mm < 0.178mm) Between Pad TP11-TP(28.915mm,10.005mm) on Top Layer And Text "TP11"
Silk To Solder Mask Clearance Constraint: (0.145mm < 0.178mm) Between Pad TP13-TP(26.342mm,13.5mm) on Top Layer And Text "TP13"
Silk To Solder Mask Clearance Constraint: (0.138mm < 0.178mm) Between Pad TP15-TP(11.25mm,37.298mm) on Top Layer And Text "TP15"
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.178mm) Between Pad TP4-TP(10.525mm,20.575mm) on Top Layer And Text "TP4"
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U4-1(33.476mm,16.225mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U4-10(29.076mm,16.225mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U4-2(33.476mm,16.725mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U4-3(33.476mm,17.225mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U4-4(33.476mm,17.725mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.157mm < 0.178mm) Between Pad U4-5(33.476mm,18.225mm) on Top Layer And Text "C10"
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U4-5(33.476mm,18.225mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U4-6(29.076mm,18.225mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U4-7(29.076mm,17.725mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U4-8(29.076mm,17.225mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U4-9(29.076mm,16.725mm) on Top Layer And Track

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "C7" (29.6mm,21.75mm) on Top Overlay And Text "R10" (29.039mm,22.925mm)
Silk To Silk Clearance Constraint: (0.231mm < 0.254mm) Between Text "LED1" (10.359mm,16.98mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.049mm < 0.254mm) Between Text "P1" (1.464mm,22.05mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.018mm < 0.254mm) Between Text "P1" (1.464mm,22.05mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.131mm < 0.254mm) Between Text "P3" (21.75mm,48.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.131mm < 0.254mm) Between Text "P4" (17.275mm,23.133mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.254mm < 0.254mm) Between Text "POWER" (1.464mm,9.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.068mm < 0.254mm) Between Text "R8" (13.55mm,36.5mm) on Top Overlay And Text "TP15" (10.094mm,38.012mm)
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "TP3" (12.8mm,21.5mm) on Top Overlay And Track (15mm,0mm)(15mm,30mm) on
Silk To Silk Clearance Constraint: (0.046mm < 0.254mm) Between Text "U5" (18.775mm,35.5mm) on Top Overlay And Track

Board Clearance Constraint (Gap=0mm) (All)

Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,0mm)(0mm,50mm) on Top Layer
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (15mm,0mm)(15mm,30mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (15mm,0mm)(50mm,0mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.353mm < 0.406mm) Between Board Edge And Track (23.2mm,49.52mm)(42.55mm,49.52mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (29.854mm,30mm)(50mm,30mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (50mm,0mm)(50mm,30mm) on Top Overlay