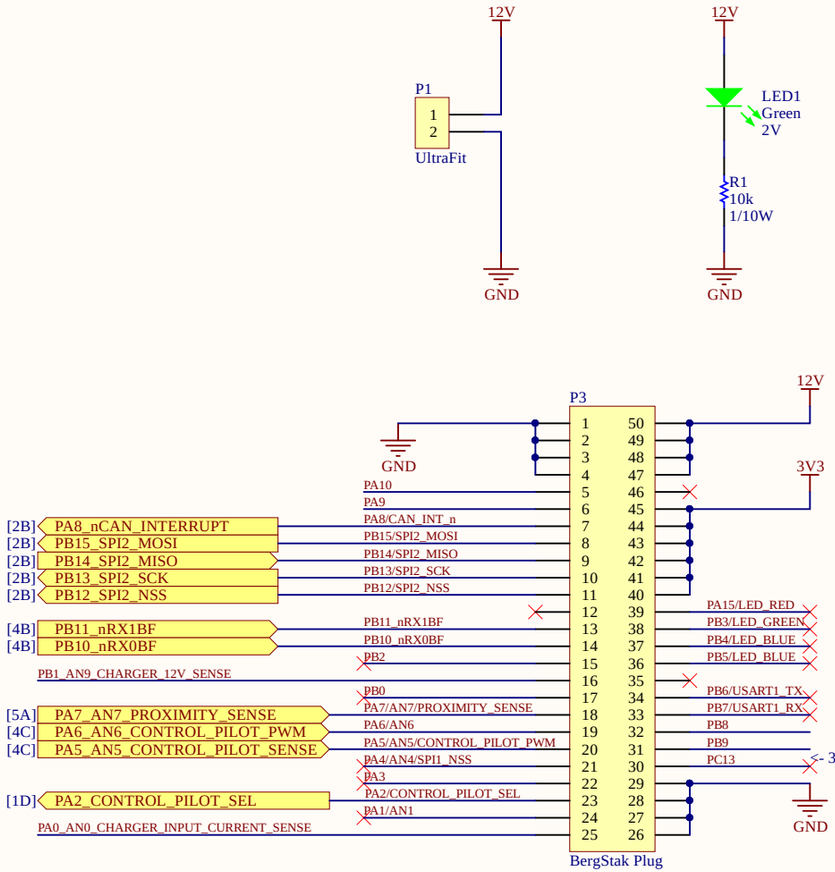
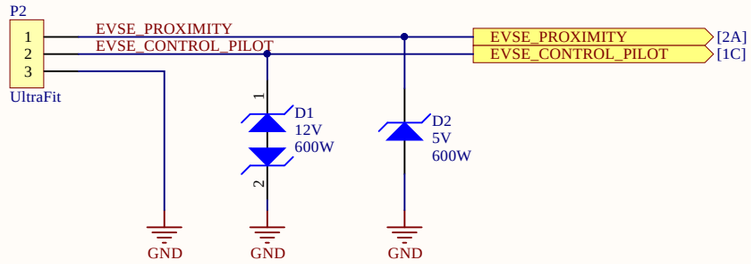
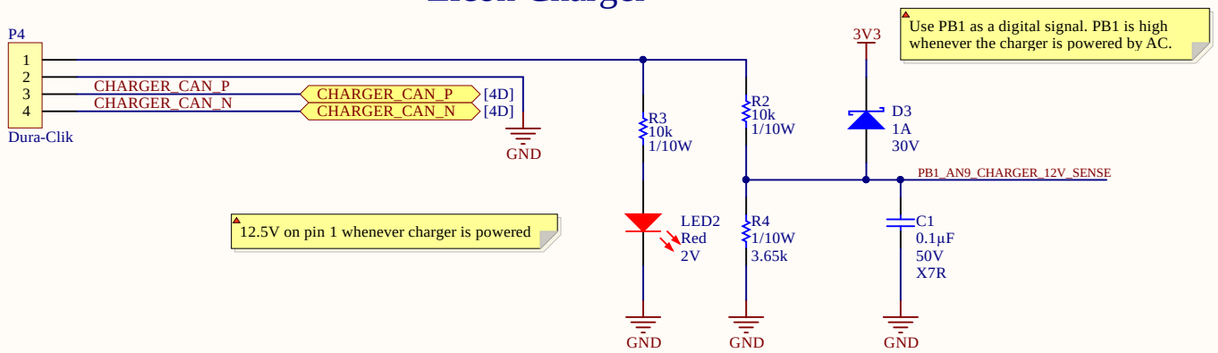


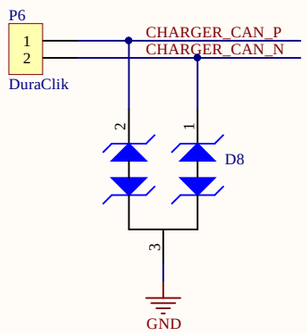
Vehicle Inlet

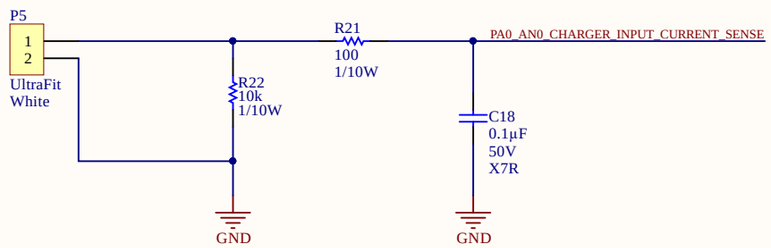


Elcon Charger



CAN Diag



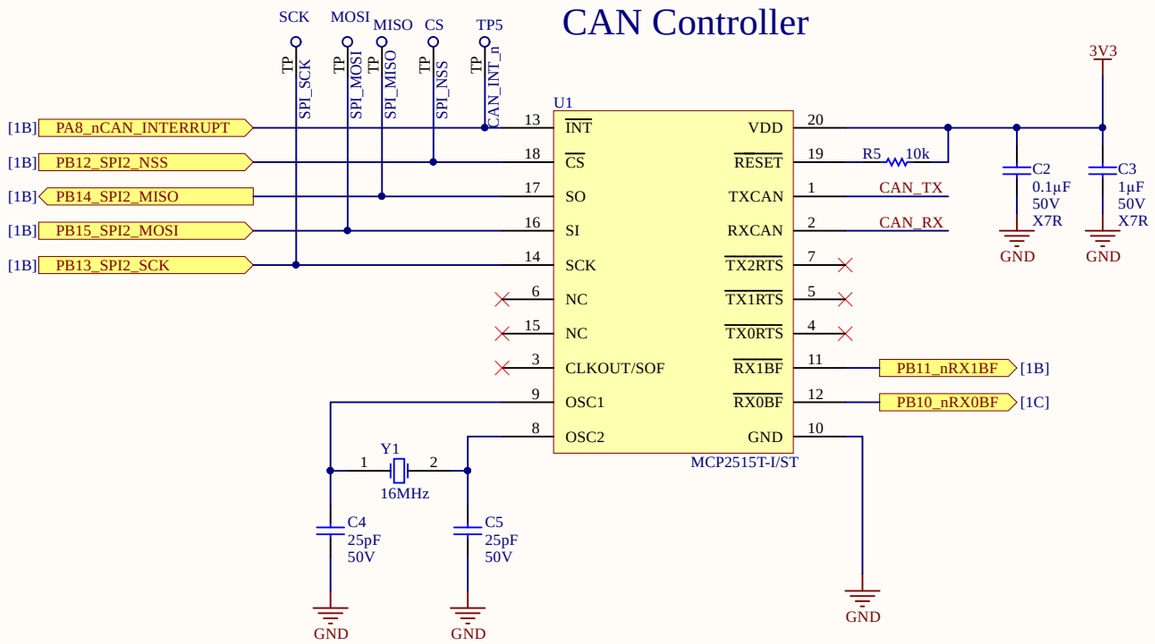


PROJECT	MSXII_ChargerInterface.PrjPcb
DOCUMENT	Charger Interface - Connectors
PART NUMBER	MS-ELE0009
VARIANT	[No Variations]
DRAWN BY	Taiping Li, Peiliang Guo
REVISION	3.0
LAST MODIFIED	3/18/2019
SHEET	1 OF 3

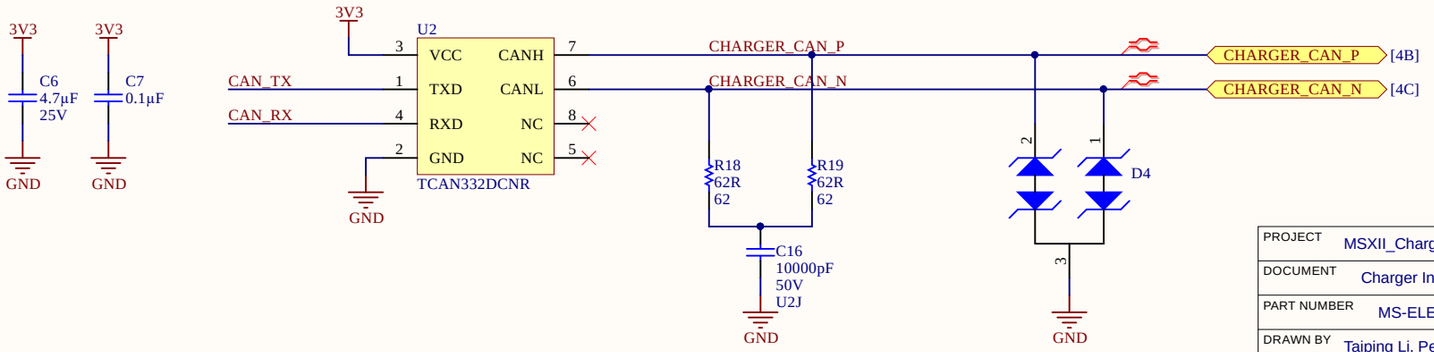
MIDNIGHT SUN

Engineering 5 - 1002
University of Waterloo
(519) 888-4567 x32978
hardware@uwmidsun.com

CAN Controller



CAN Transceiver



PROJECT	MSXII_ChargerInterface.PrjPcb		
DOCUMENT	Charger Interface - CAN		
PART NUMBER	MS-ELE0009	VARIANT	[No Variations]
DRAWN BY	Taiping Li, Peiliang Guo	REVISION	3.0
LAST MODIFIED	3/18/2019	SHEET	2 OF 3

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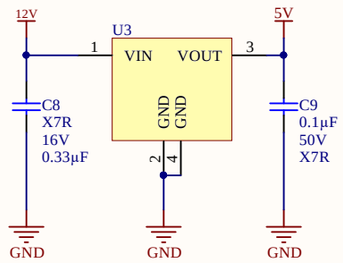
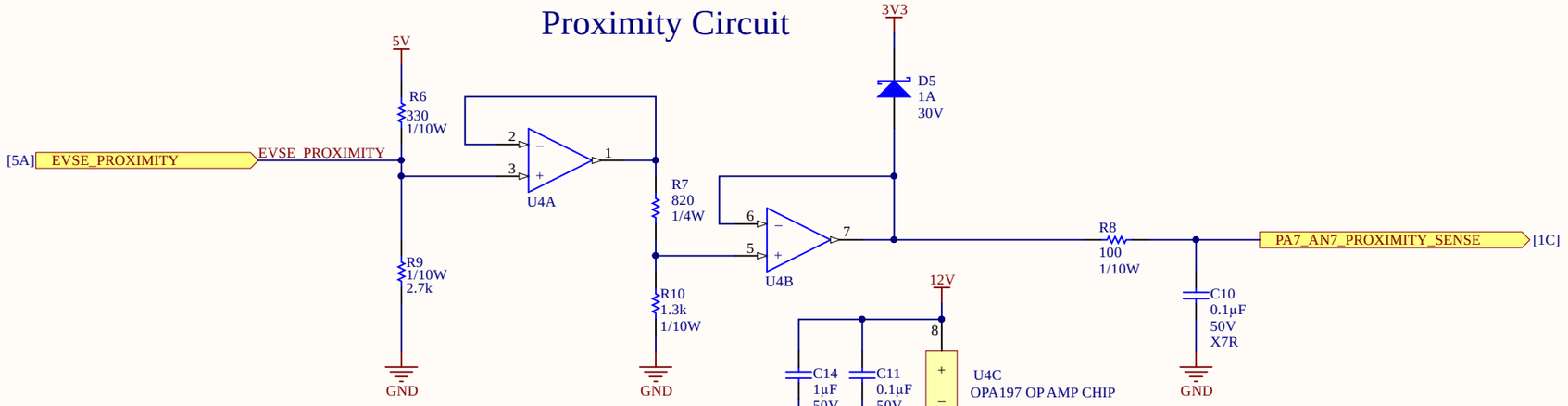
hardware@uwmidsun.com

5V Power Supply



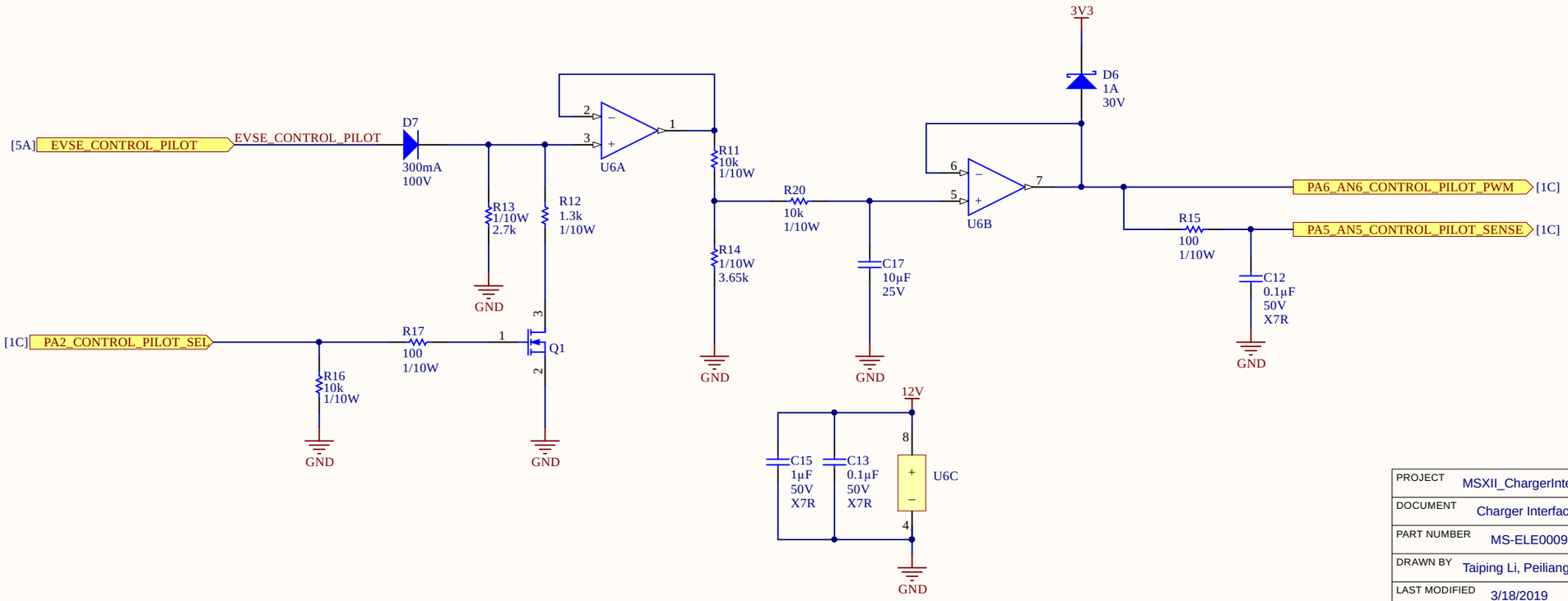
Proximity Circuit



PA7/AN7/PROXIMITY_SENSE Expected Voltages

Description	Min Voltage	Nominal Voltage	Max Voltage	Min ADC Reading	Nominal ADC Reading	Max ADC Reading
EVSE Not Connected	4.13	4.46	4.78	2.533	2.735	2.931
EVSE Connector plugged in, button is peleased	1.23	1.53	1.82	0.754	0.938	1.116
EVSE Connector is plugged In, button is pressed	2.38	2.77	3.16	1.459	1.699	1.938

Control Pilot Circuit



PROJECT	MSXII_ChargerInterface.PrjPcb		
DOCUMENT	Charger Interface - J1772 Interface		
PART NUMBER	MS-ELE0009	VARIANT	[No Variations]
DRAWN BY	Taiping Li, Peiliang Guo	REVISION	3.0
LAST MODIFIED	3/18/2019	SHEET	3 OF 3

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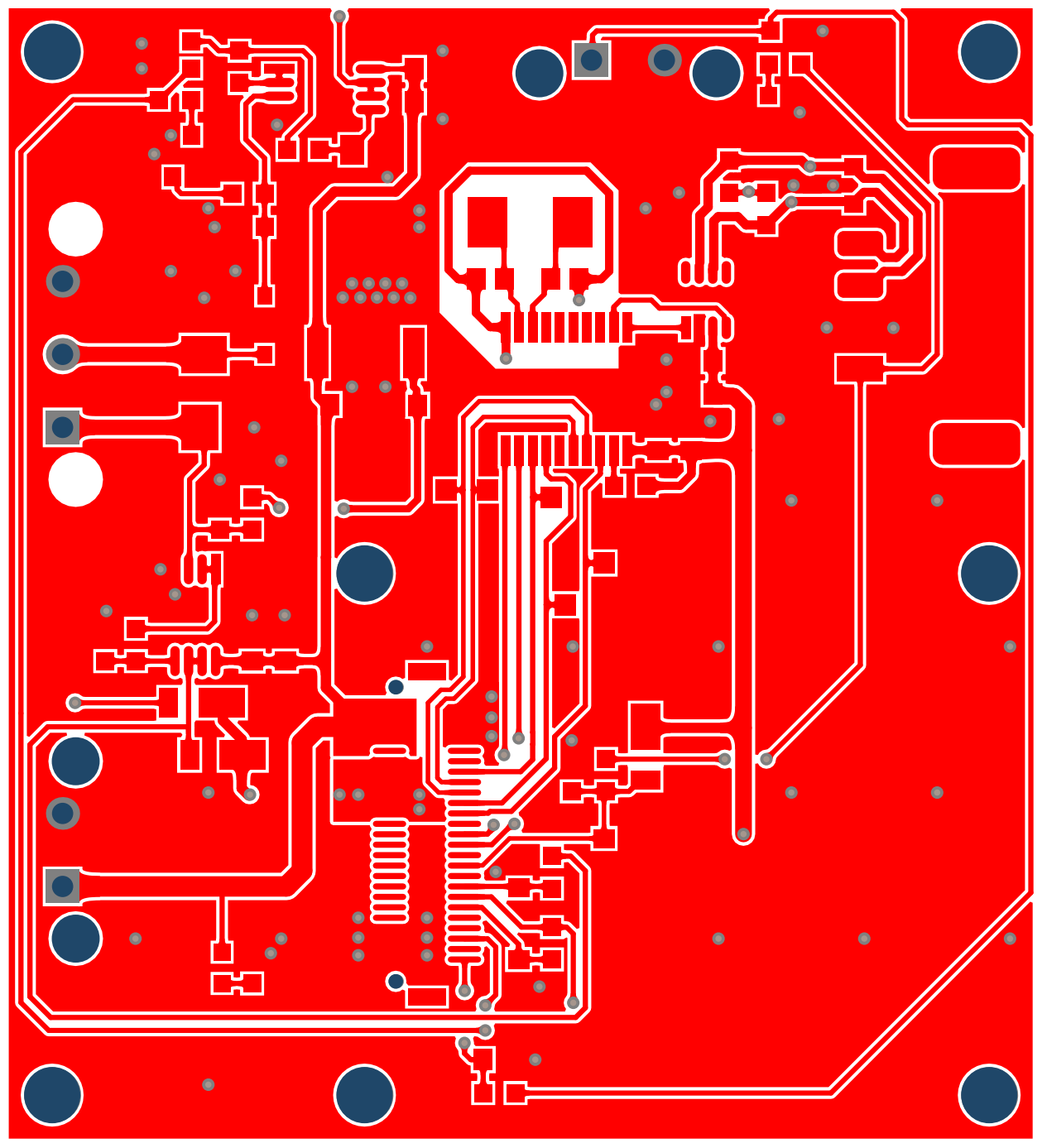

MS-ELE0009
REV 3.0
19/03

Design Rules Verification Repor

Filename : \\Mac\Home\Documents\midsun\hardware\MSXII_ChargerInterface\Charger In

Warnings 0
Rule Violations 11(

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All	0
Short-Circuit Constraint (Allowed=No) (All),(All	0
Un-Routed Net Constraint ((All)	0
Modified Polygon (Allow modified: No), (Allow shelved: Nc	0
Width Constraint (Min=0.152mm) (Max=2.54mm) (Preferred=0.25mm) (Al	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mr	0
Minimum Annular Ring (Minimum=0.15mm) (All	0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All	0
Hole To Hole Clearance (Gap=0.254mm) (All),(Al	0
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All	36
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(Al	24
Silk to Silk (Clearance=0.254mm) (OnLayer('Bottom Overlay')),(OnLayer('Bottom Overlay	0
Silk to Silk (Clearance=0.254mm) (OnLayer('Top Overlay')),(OnLayer('Top Overlay	29
Net Antennae (Tolerance=0mm) (All	0
Board Clearance Constraint (Gap=0mm) (All	21
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (Al	0
Total	110

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C10-1(24.925mm,12.425mm) on Top Layer A
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C1-1(29mm,14.8mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C11-1(12.1mm,23.3mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C12-1(24.9mm,9mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C13-1(19.9mm,51.7mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C14-1(13.7mm,23.3mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C15-1(19.9mm,50.1mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C16-1(34.825mm,45.75mm) on Bottom Layer A
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C18-1(23.2mm,4.2mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C2-1(31.6mm,33.4mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C3-1(33.2mm,33.4mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.3mm) Between Pad C3-2(33.2mm,34.75mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.3mm) Between Pad C3-2(33.2mm,34.75mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C4-1(24.2mm,41.6mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C5-1(26.45mm,41.6mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C6-1(32.888mm,36.1mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C7-1(32.888mm,37.7mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C8-1(15.85mm,35.6mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C9-1(20.05mm,35.562mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad D8-3(37.4mm,36mm) on Bottom Layer And '
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P3-(19mm,22.05mm) on Multi-Layer And P
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P3-(19mm,7.95mm) on Multi-Layer And P
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.3mm) Between Pad R14-1(9.175mm,53mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.3mm) Between Pad R14-2(7.625mm,53mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.06mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region (0 hole(
Minimum Solder Mask Sliver Constraint: (0.117mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region
Minimum Solder Mask Sliver Constraint: (0.282mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region
Minimum Solder Mask Sliver Constraint: (0.282mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region
Minimum Solder Mask Sliver Constraint: (0.286mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region
Minimum Solder Mask Sliver Constraint: (0.287mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region
Minimum Solder Mask Sliver Constraint: (0.287mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region
Minimum Solder Mask Sliver Constraint: (0.294mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region
Minimum Solder Mask Sliver Constraint: (0.296mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region
Minimum Solder Mask Sliver Constraint: (0.299mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region
Minimum Solder Mask Sliver Constraint: (0.007mm < 0.3mm) Between Via (16.452mm,40.725mm) from Top Layer to Bott
Minimum Solder Mask Sliver Constraint: (0.044mm < 0.3mm) Between Via (16.452mm,40.725mm) from Top Layer to Bott

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(Al
Silk To Solder Mask Clearance Constraint: (0.09mm < 0.178mm) Between Arc (41mm,44.25mm) on Top Overlay And F
Silk To Solder Mask Clearance Constraint: (0.092mm < 0.178mm) Between Pad C11-2(12.1mm,24.65mm) on Top Layer A
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C1-2(29mm,13.45mm) on Top Layer A
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad C12-2(24.9mm,7.65mm) on Top Layer A
Silk To Solder Mask Clearance Constraint: (0.076mm < 0.178mm) Between Pad C14-2(13.7mm,24.65mm) on Top Layer A
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.178mm) Between Pad C5-2(27.8mm,41.6mm) on Top Layer A
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad P3-1(22.3mm,21mm) on Top Layer And Tr
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad P3-25(22.3mm,9mm) on Top Layer And Tr
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad P3-26(18.7mm,9mm) on Top Layer A
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad P3-50(18.7mm,21mm) on Top Layer A
Silk To Solder Mask Clearance Constraint: (0.119mm < 0.178mm) Between Pad P4-7(46.889mm,33.71mm) on Top Layer A
Silk To Solder Mask Clearance Constraint: (0.16mm < 0.178mm) Between Pad P4-7(46.889mm,46.91mm) on Top Layer A
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q1-1(9.2mm,48.5mm) on Top Layer A
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q1-2(7.4mm,48.5mm) on Top Layer A
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad R18-1(36.8mm,44.2mm) on Top Layer A
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-1(32.925mm,39.275mm) on Top La
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U2-2(33.575mm,39.275mm) on Top La
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U2-3(34.225mm,39.275mm) on Top La
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U2-4(34.875mm,39.275mm) on Top La
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-5(34.875mm,41.925mm) on Top La
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-6(34.225mm,41.925mm) on Top La
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-7(33.575mm,41.925mm) on Top La
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-8(32.925mm,41.925mm) on Top La
Silk To Solder Mask Clearance Constraint: (0.162mm < 0.178mm) Between Pad U3-4(17.55mm,43.868mm) on Top Layer A

Silk to Silk (Clearance=0.254mm) (OnLayer('Top Overlay')),(OnLayer('Top Overlay
Silk To Silk Clearance Constraint: (0.234mm < 0.254mm) Between Arc (30.9mm,39.3mm) on Top Overlay And Text "
Silk To Silk Clearance Constraint: (0.243mm < 0.254mm) Between Arc (32.15mm,39.275mm) on Top Overlay And Text "
Silk To Silk Clearance Constraint: (0.119mm < 0.254mm) Between Text "C10" (27.45mm,14mm) on Top Overlay And
Silk To Silk Clearance Constraint: (0.204mm < 0.254mm) Between Text "C13" (22.25mm,51.265mm) on Top Overlay A
Silk To Silk Clearance Constraint: (0.204mm < 0.254mm) Between Text "C15" (22.25mm,49.75mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "C2" (34.4mm,35.25mm) on Top Overlay And Text "
Silk To Silk Clearance Constraint: (0.168mm < 0.254mm) Between Text "CP" (6.3mm,38.7mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.148mm < 0.254mm) Between Text "CS" (30mm,27.5mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "CURRENT SENSE" (25.1mm,48mm) on Top Ove
Silk To Silk Clearance Constraint: (0.168mm < 0.254mm) Between Text "CURRENT SENSE" (25.1mm,48mm) on Top Ove
Silk To Silk Clearance Constraint: (0.125mm < 0.254mm) Between Text "D1" (9.4mm,43.6mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.215mm < 0.254mm) Between Text "D3" (30.5mm,23.5mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.229mm < 0.254mm) Between Text "J17

INLET" (1.4mm,28mm) on Top Overlay And Track (0.38mm,30.7mm)(5.93mm,30.7mm) on To

Silk to Silk (Clearance=0.254mm) (OnLayer('Top Overlay')),(OnLayer('Top Overlay
Silk To Silk Clearance Constraint: (0.175mm < 0.254mm) Between Text "MOSI" (22.75mm,35.25mm) on Top Overlay A
Silk To Silk Clearance Constraint: (0.22mm < 0.254mm) Between Text "MOSI" (22.75mm,35.25mm) on Top Overlay A
Silk To Silk Clearance Constraint: (0.169mm < 0.254mm) Between Text "P1" (0.6mm,20.2mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.168mm < 0.254mm) Between Text "P1" (0.6mm,20.2mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.108mm < 0.254mm) Between Text "P2" (0.3mm,45.6mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "P2" (0.3mm,45.6mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.21mm < 0.254mm) Between Text "P3" (19.8mm,24.2mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.254mm < 0.254mm) Between Text "POWER" (1.5mm,7.5mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.168mm < 0.254mm) Between Text "PROX" (6.3mm,36mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "Q1" (5.63mm,46.7mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "Q1" (5.63mm,46.7mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.15mm < 0.254mm) Between Text "R10" (2.3mm,25.2mm) on Top Overlay And Text "
Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "TP5" (26mm,29.5mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.086mm < 0.254mm) Between Text "U2" (30.9mm,41.3mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.086mm < 0.254mm) Between Text "U2" (30.9mm,41.3mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.175mm < 0.254mm) Between Text "U6" (15mm,52.6mm) on Top Overlay And Tr

Board Clearance Constraint (Gap=0mm) (All
Board Outline Clearance(Outline Edge): (0.145mm < 0.406mm) Between Board Edge And Text "ELCON CHARGE
Board Outline Clearance(Outline Edge): (0.15mm < 0.406mm) Between Board Edge And Text "P2" (0.3mm,45.6mm) on T
Board Outline Clearance(Outline Edge): (0.25mm < 0.406mm) Between Board Edge And Text "P5" (22.8mm,53.8mm) on T
Board Outline Clearance(Outline Edge): (0.253mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.253mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.253mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.253mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.253mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (15mm,0mm)(15mm,14.4m
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (15mm,30mm)(50mm,30m
Board Outline Clearance(Outline Edge): (0.403mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.403mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.403mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.403mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.375mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (43.5mm,0mm)(50mm,0m
Board Outline Clearance(Outline Edge): (0.375mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.153mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.375mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (50mm,0mm)(50mm,30m

Electrical Rules Check Repor

Class	Document	Message
Warning	Charger Interface - J1772 Interface.SchDoc	Net NetC17_1 has no driving source (Pin C17-1,Pin R20-2,Pin U6-5
Warning	Charger Interface - J1772 Interface.SchDoc	Net NetD7_2 has no driving source (Pin D7-2,Pin R12-1,Pin R13-1,Pi U6-3)
Warning	Charger Interface - J1772 Interface.SchDoc	Net NetR7_2 has no driving source (Pin R7-2,Pin R10-1,Pin U4-5
Error	Charger Interface - CAN.SchDoc	Net PA9 has only one pin (Pin P3-6
Error	Charger Interface - CAN.SchDoc	Net PA10 has only one pin (Pin P3-5
Error	Charger Interface - CAN.SchDoc	Net PB8 has only one pin (Pin P3-32
Error	Charger Interface - CAN.SchDoc	Net PB9 has only one pin (Pin P3-31
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PA2/CONTROL_PILOT_SEL has multiple names (Net Lab PA2/CONTROL_PILOT_SEL,Port PA2_CONTROL_PILOT_SEL)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PA2/CONTROL_PILOT_SEL has multiple names (Net Lab PA2/CONTROL_PILOT_SEL,Port PA2_CONTROL_PILOT_SEL,Port PA2_CONTROL_PILOT_SEL)
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PA5/AN5/CONTROL_PILOT_PWM has multiple names (N Label PA5/AN5/CONTROL_PILOT_PWM,Port PA5_AN5_CONTROL_PILOT_SENSE)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PA5/AN5/CONTROL_PILOT_PWM has multiple names (N Label PA5/AN5/CONTROL_PILOT_PWM,Port PA5_AN5_CONTROL_PILOT_SENSE,Port PA5_AN5_CONTROL_PILOT_SENSE)
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PA6/AN6 has multiple names (Net Label PA6/AN6,Pc PA6_AN6_CONTROL_PILOT_PWM)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PA6/AN6 has multiple names (Net Label PA6/AN6,Pc PA6_AN6_CONTROL_PILOT_PWM,Port PA6_AN6_CONTROL_PILOT_PWM)
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PA7/AN7/PROXIMITY_SENSE has multiple names (Net Lab PA7/AN7/PROXIMITY_SENSE,Port PA7_AN7_PROXIMITY_SENSE)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PA7/AN7/PROXIMITY_SENSE has multiple names (Net Lab PA7/AN7/PROXIMITY_SENSE,Port PA7_AN7_PROXIMITY_SENSE,Pc PA7_AN7_PROXIMITY_SENSE)
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PA8/CAN_INT_n has multiple names (Net Lab PA8/CAN_INT_n,Port PA8_nCAN_INTERRUPT)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PA8/CAN_INT_n has multiple names (Net Lab PA8/CAN_INT_n,Port PA8_nCAN_INTERRUPT,Port PA8_nCAN_INTERRUPT)
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PB12/SPI2_NSS has multiple names (Net Labe PB12/SPI2_NSS,Port PB12_SPI2_NSS)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PB12/SPI2_NSS has multiple names (Net Label PB12/SPI2_NSS,Port PB12_SPI2_NSS,Port PB12_SPI2_NSS
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PB13/SPI2_SCK has multiple names (Net Labe PB13/SPI2_SCK,Port PB13_SPI2_SCK)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PB13/SPI2_SCK has multiple names (Net Label PB13/SPI2_SCK,Port PB13_SPI2_SCK,Port PB13_SPI2_SCK
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PB14/SPI2_MISO has multiple names (Net Labe PB14/SPI2_MISO,Port PB14_SPI2_MISO)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PB14/SPI2_MISO has multiple names (Net Label PB14/SPI2_MISO,Port PB14_SPI2_MISO,Port PB14_SPI2_MISC
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PB15/SPI2_MOSI has multiple names (Net Labe PB15/SPI2_MOSI,Port PB15_SPI2_MOSI)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PB15/SPI2_MOSI has multiple names (Net Label PB15/SPI2_MOSI,Port PB15_SPI2_MOSI,Port PB15_SPI2_MOS
Warning	Charger Interface - Connectors.SchDoc	Off grid Net Label PA2/CONTROL_PILOT_SEL at 3006.571mil,3800n