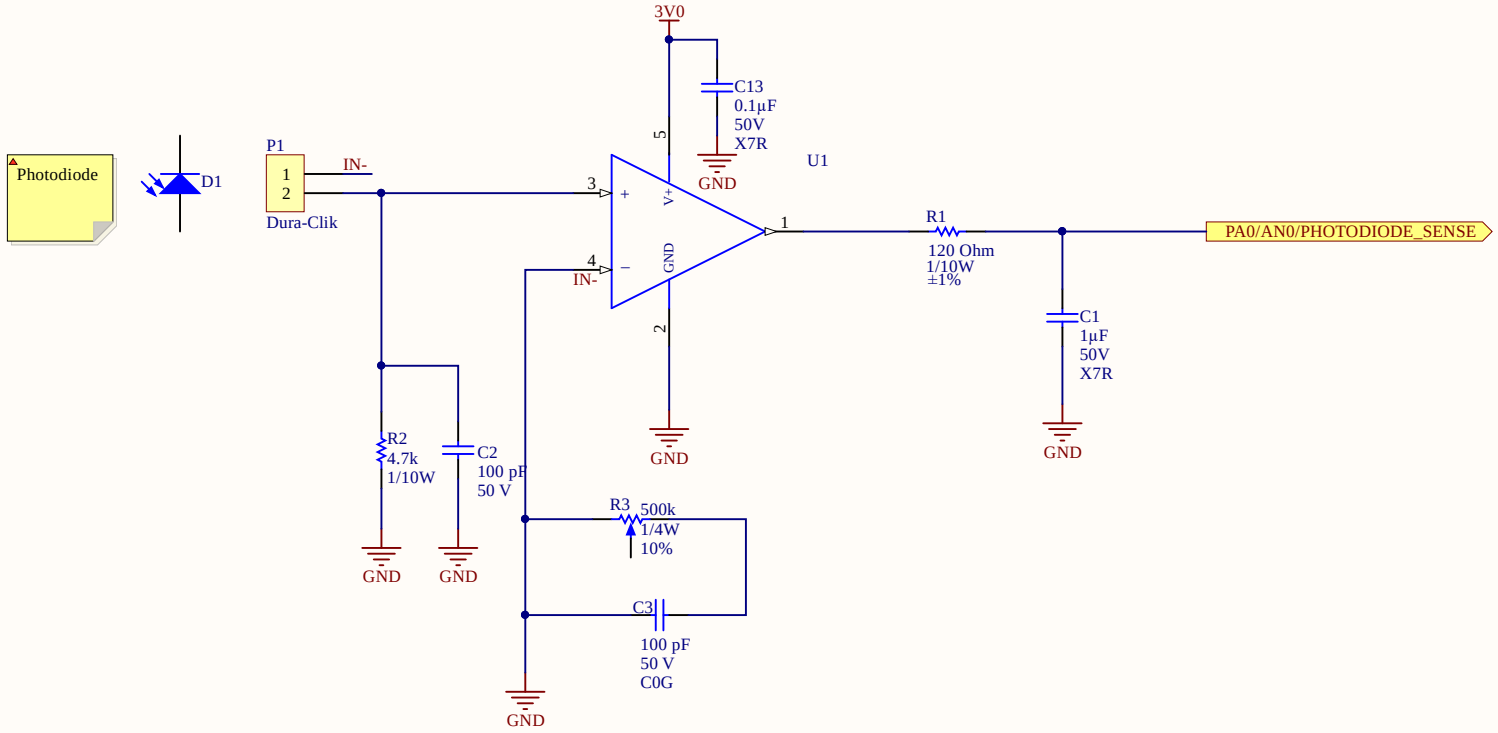
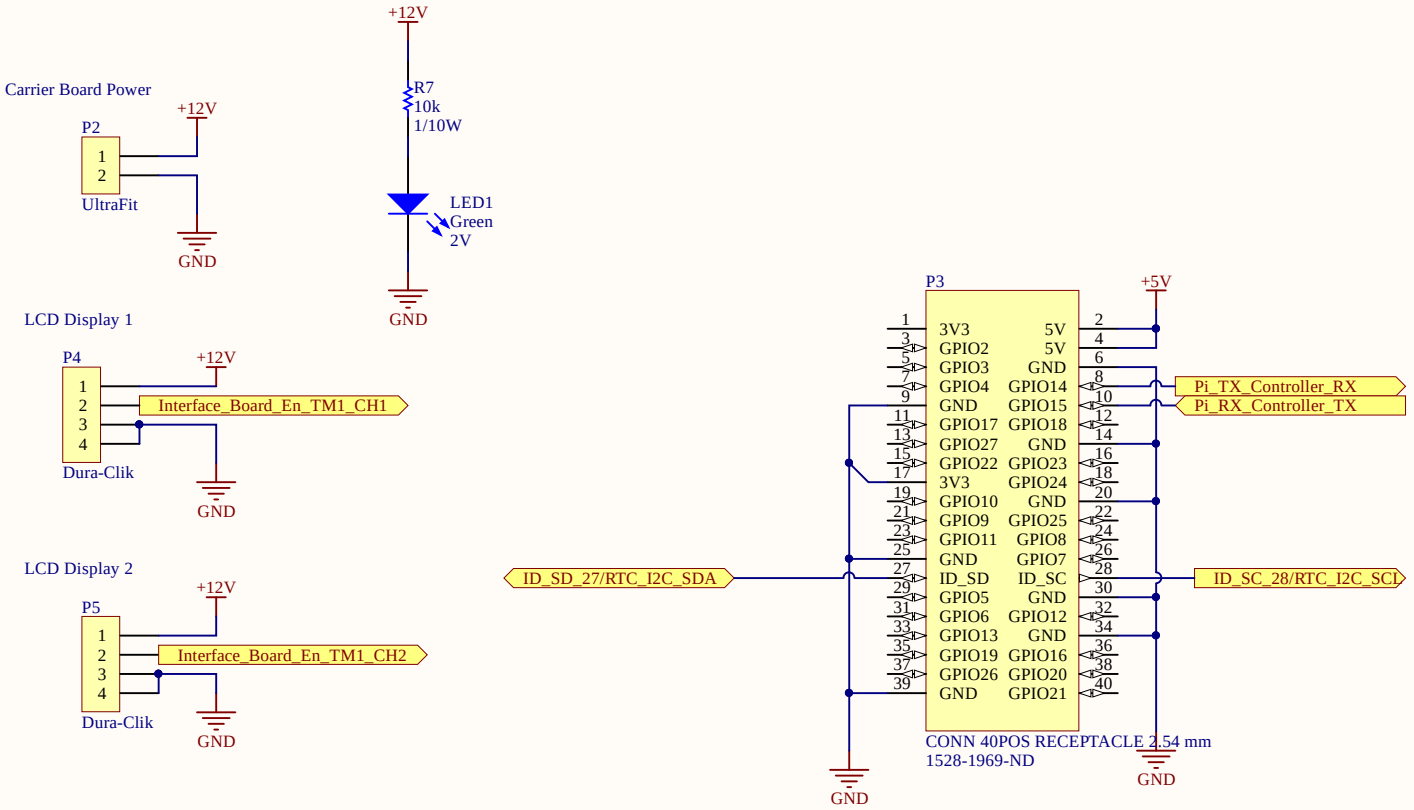
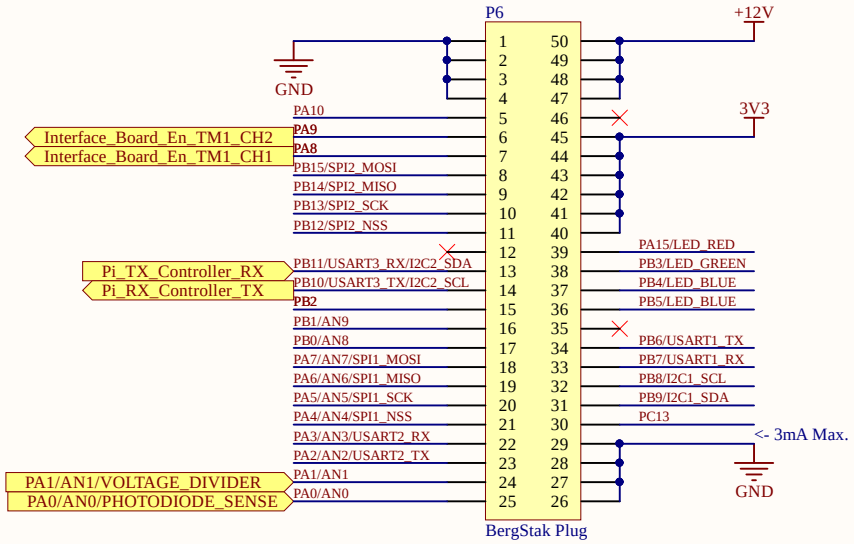


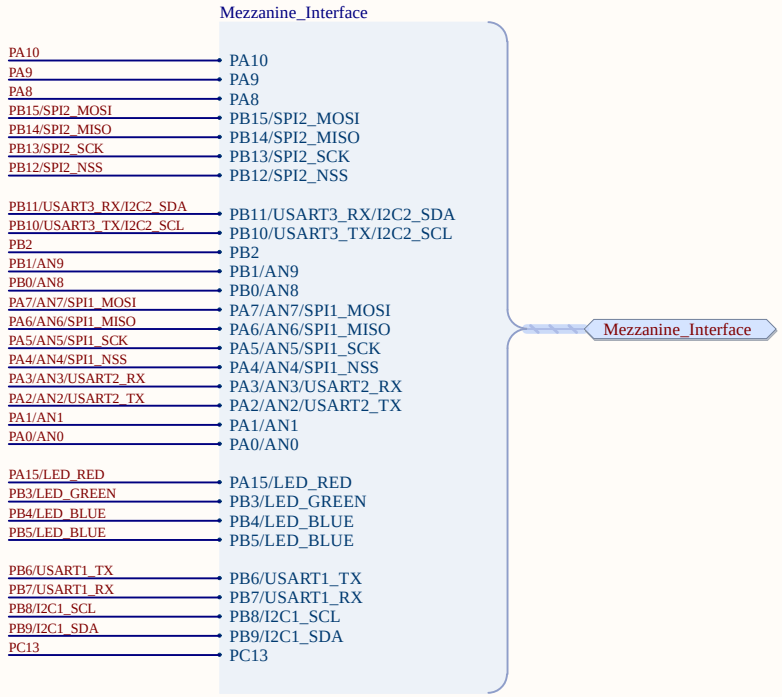
Project: ***Driver_Display.PrjPcb***		MIDNIGHT SUN
Title: *		
Project Lead: Kelly Tang		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.0	
Date: 2018-06-22	Sheet * of *	Website: www.uwmidsun.com



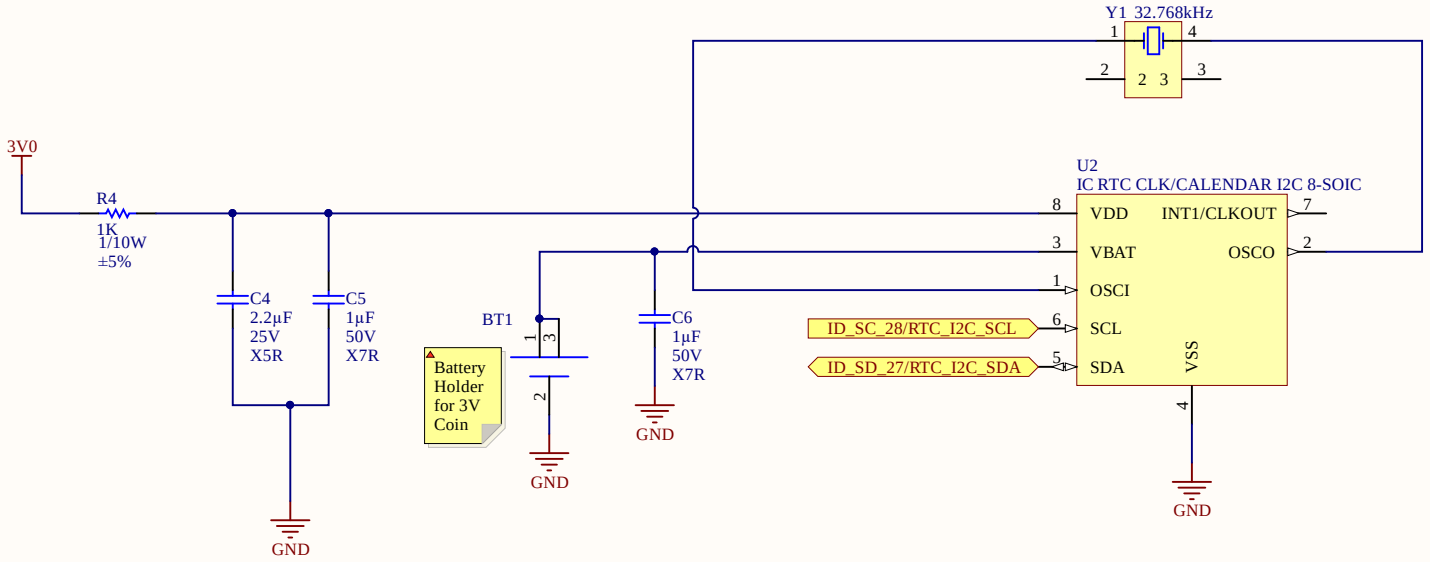
Project: ***Driver_Display.PrjPcb***		MIDNIGHT SUN
Title: *		
Project Lead: Kelly Tang		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.0	
Date: 2018-06-22	Sheet* of *	Website:

Text
Text
Text



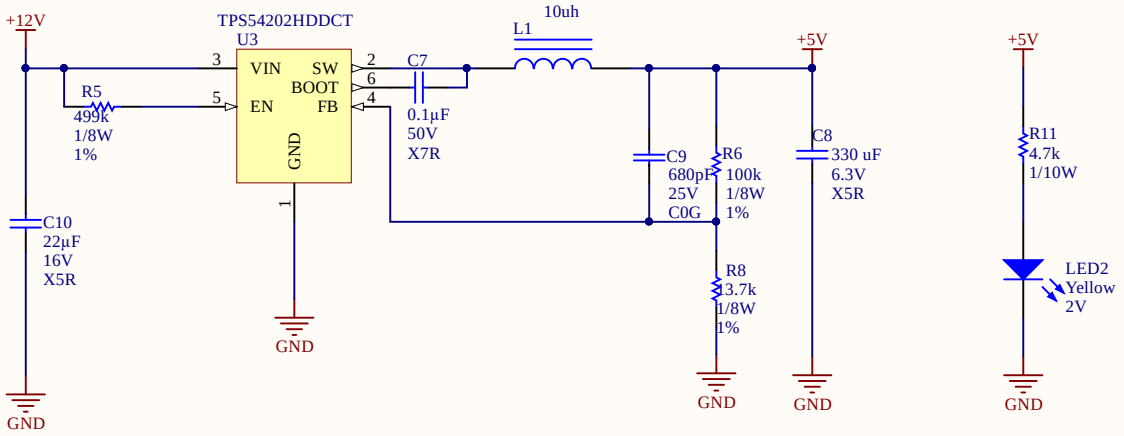


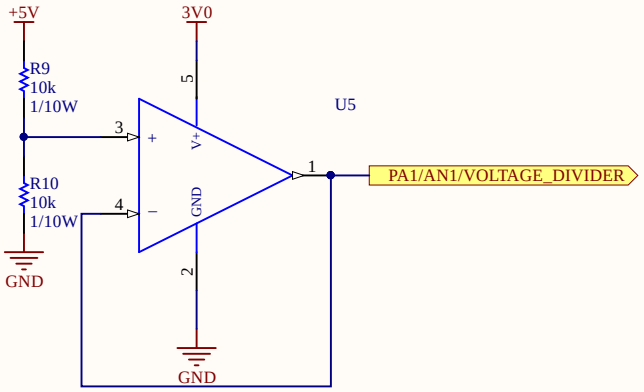
Project: ***Driver_Display.PrjPcb***		MIDNIGHT SUN
Title: *		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Lead: Kelly Tang		
Size: Letter	Revision: 1.0	
Date: 2018-06-22	Sheet * of *	Website: www.uwmidsun.com

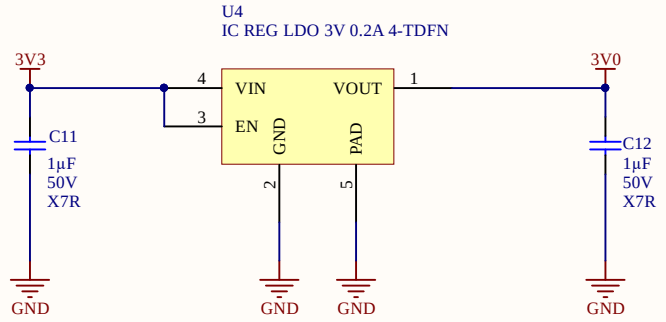


Project: ***Driver_Display.PrjPcb***		MIDNIGHT SUN
Title: *		
Project Lead: Kelly Tang		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.0	
Date: 2018-06-22	Sheet* of *	Website: www.uwmidsun.com

Part	Manufacturer	Part Number	Quantity	Price	Attributes
Cbst	TDK	C2012X5R2A104	1	$0.04	Cap=100nF, ESR=0.021Ohm, Total Derated Cap=1.0E-7F
Cin	TDK	C4532X5R1E226	1	$0.54	Cap=22uF, ESR=2.434mOhm, Total Derated Cap=1.1E-5F
Cout	Panasonic	EEHZC1E331P	1	$1.30	Cap=330uF, ESR=0.02Ohm, Total Derated Cap=3.3E-4F
L1	Bourns	SRN6045-100M	1	$0.18	L=10uH, DCR=0.059Ohm, IDC=2.5A
Ren	Panasonic	ERJ-6ENF4993V	1	$0.01	Resistance=499kOhm, Tolerance=1%, Power=0.125W
Rfbb	Panasonic	ERJ-6ENF1372V	1	$0.01	Resistance=13.7kOhm, Tolerance=1%, Power=0.125W
Rfbt	Panasonic	ERJ-6ENF1003V	1	$0.01	Resistance=100kOhm, Tolerance=1%, Power=0.125W
U1	Texas Instruments	TPS54202HDDC	1	$0.65	
Cff	MuRata	GRM033R71E68	1	$0.01	Cap=680pF, ESR=1mOhm, Total Derated Cap=6.8E-10F





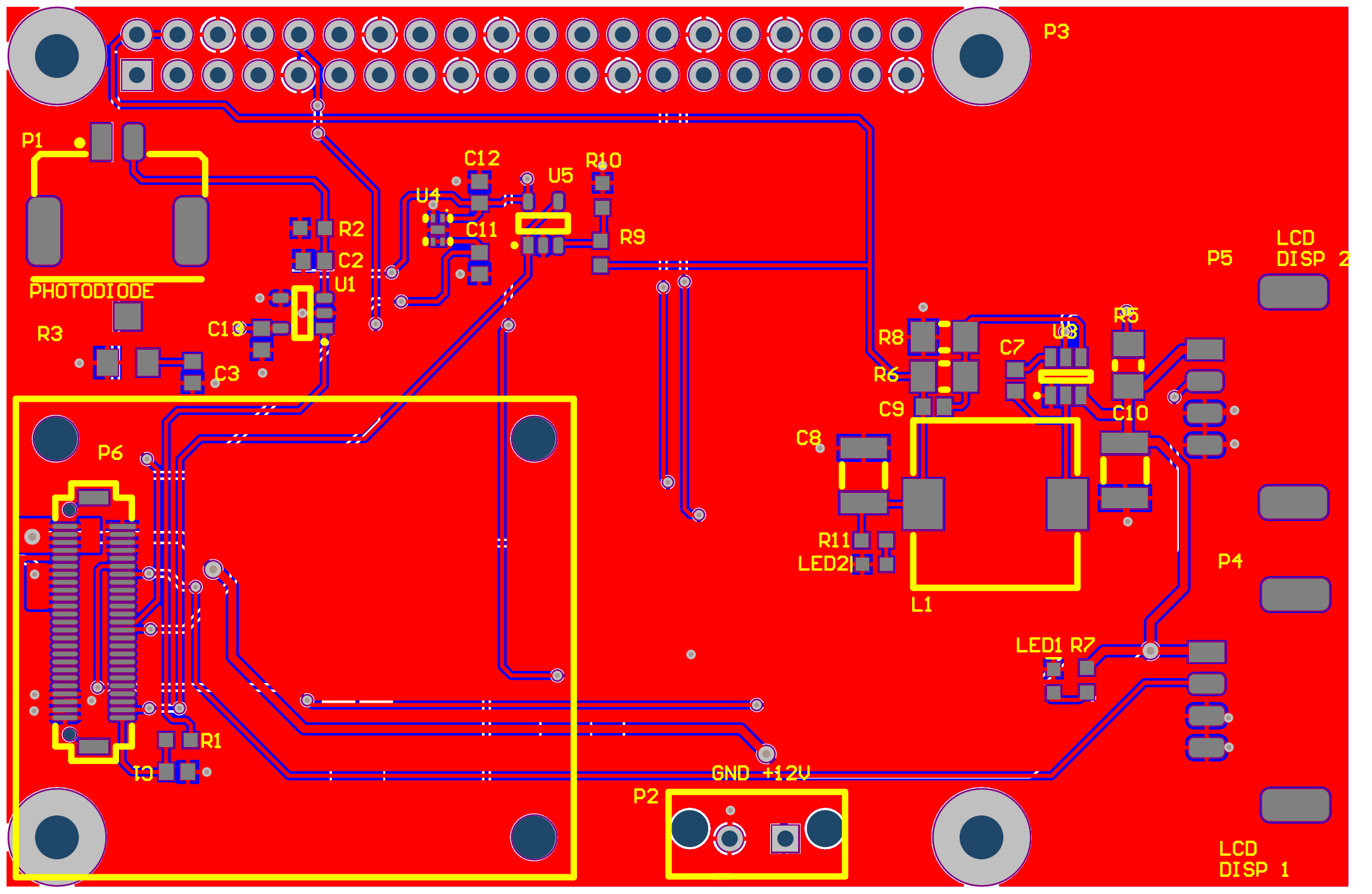


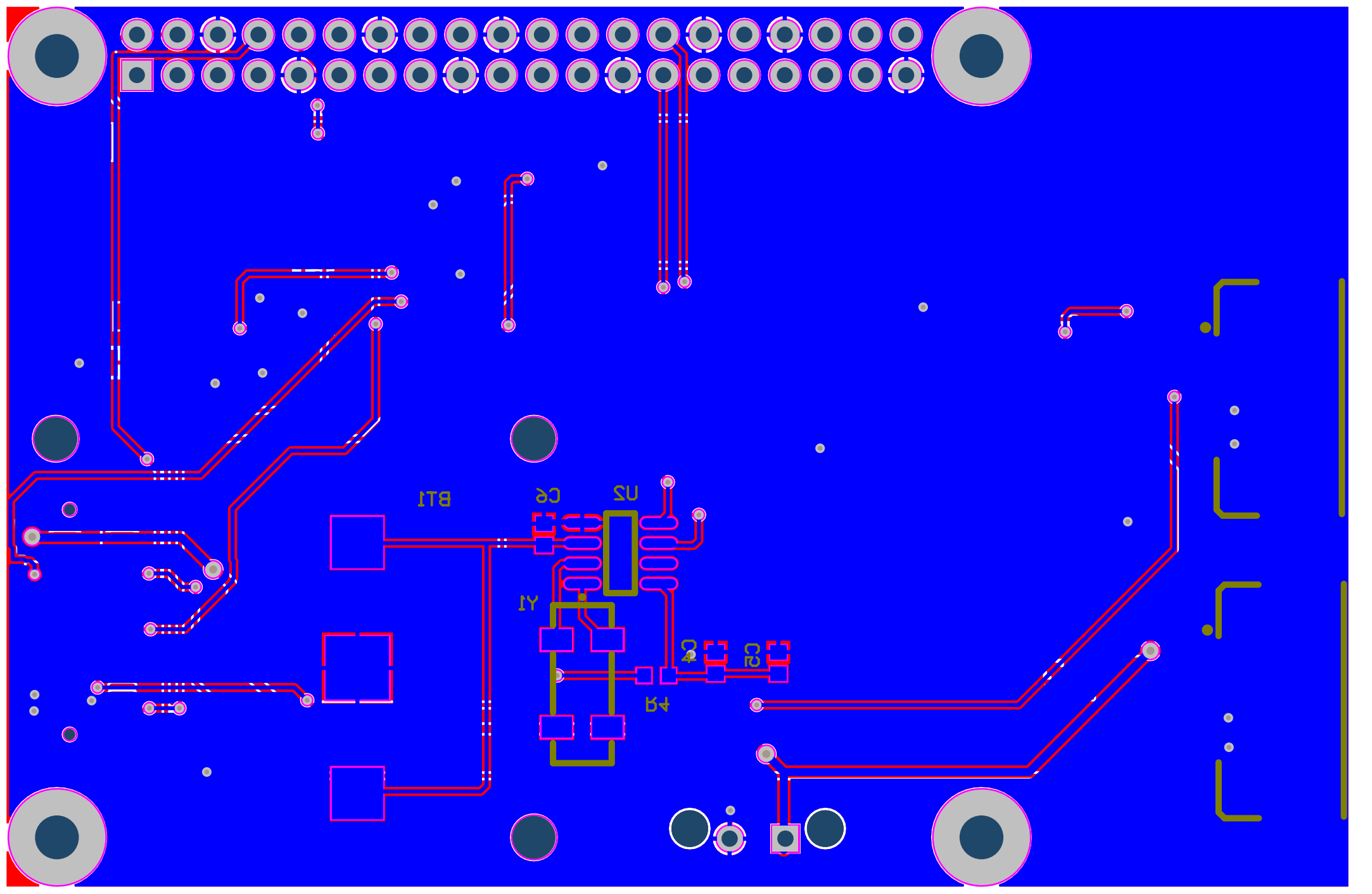
Project: *Driver_Display.PrjPcb*		MIDNIGHT SUN
Title: *		
Project Lead: Kelly Tang		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.0	
Date: 2018-06-22	Sheet * of *	Website: www.uwmidsun.com

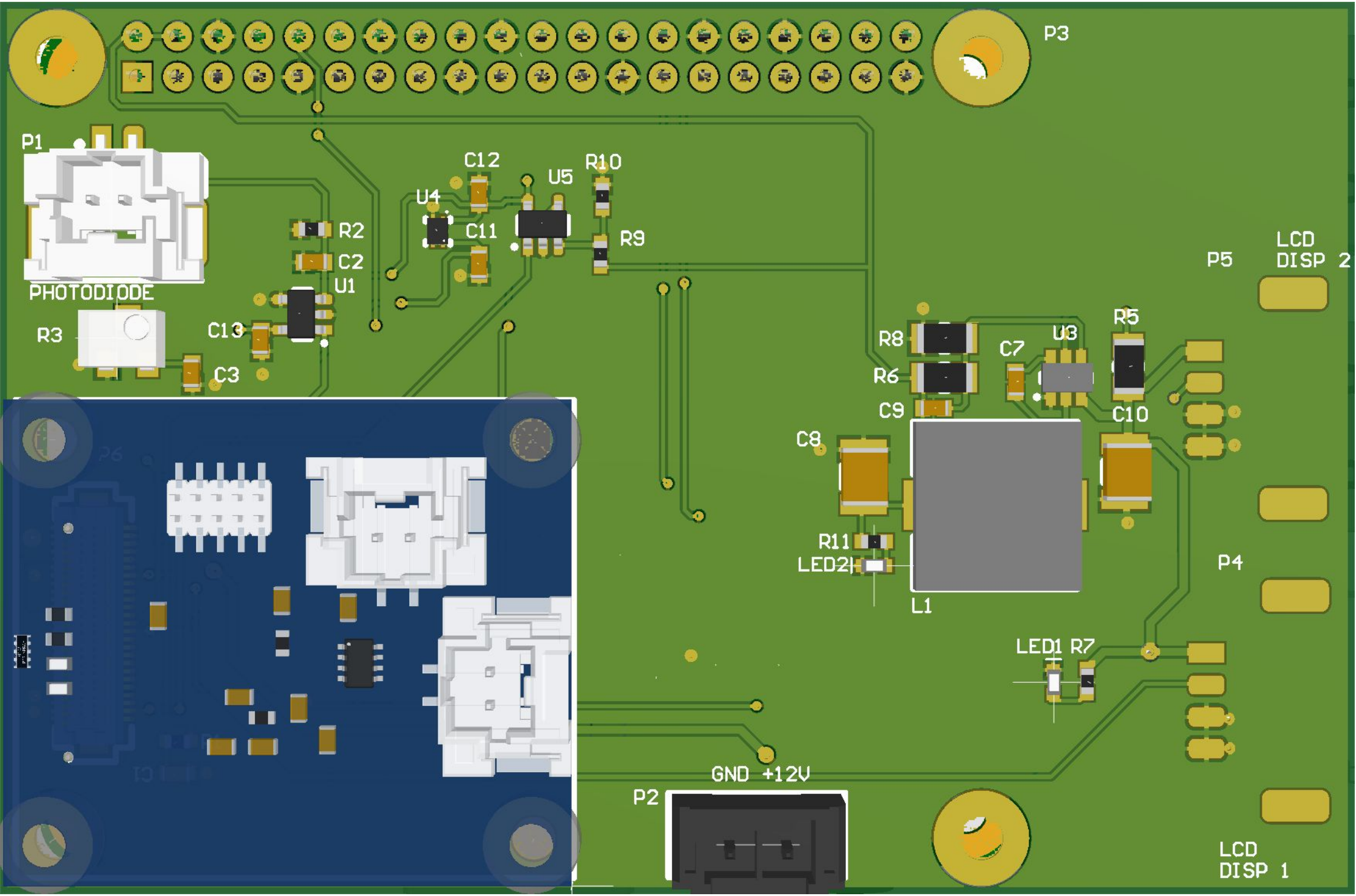
Bill of Materials

Project:	Driver_Display.PrjPcb
Revision:	1.0
Project Lead:	Kelly Tang
Generated On:	2018-06-22 3:59:10 AM
Production Quantity:	1
Currency	CAD
Total Parts Count:	40

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Supplier Order Qty 1	Supplier Subtotal 1
HOLDER BATTERY COIN 12MM DIA	BT1	Keystone Electronics	3000	Digi-Key	36-3000-ND	0.77	1	$ 0.77
CAP CER 1UF 50V 10% X7R 0603	C1, C5, C6, C11, C12	Taiyo Yuden	UMK107AB7105KA-T	Digi-Key	587-3247-1-ND	0.39	5	$ 1.93
CAP CER 100PF 50V C0G/NP0 0603	C2, C3	Kyocera AVX	06035A101FAT2A	Digi-Key	478-6202-1-ND	0.32	2	$ 0.64
CAP CER 2.2UF 25V 10% X5R 0603	C4	Murata	GRM188R61E225KA12D	Digi-Key	490-10731-1-ND	0.24	1	$ 0.24
CAP CER 0.1UF 50V 10% X7R 0603	C7, C13	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.21	2	$ 0.43
CAP CER 330UF 6.3V X5R 1210	C8	Taiyo Yuden	JMK325ABJ337MM-P	Digi-Key	587-5449-1-ND	7.41	1	$ 7.41
CAP CER 680PF 25V C0G 0201	C9	Murata	GRM0335C1E681JA01D	Digi-Key	490-14330-1-ND	0.13	1	$ 0.13
CAP CER 22UF 16V ±20% X5R 1210	C10	Murata	GRM32ER61C226ME20L	Digi-Key	490-1881-1-ND	2.45	1	$ 2.45
IND 10UH 2.8A 59 MOHM SMD	L1	Sumida	CDRH103RNP-100NC-B	Digi-Key	308-1910-1-ND	2.04	1	$ 2.04
LED GREEN CLEAR 2V 0603	LED1	Wurth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.19	1	$ 0.19
LED YELLOW CLEAR 2.1V 0603	LED2	Wurth Electronics	150060YS75000	Digi-Key	732-4981-1-ND	0.19	1	$ 0.19
CONN 2POS DURA-CLIK 0.079" VERT	P1	Molex	560020-0220	Digi-Key	WM10862CT-ND	1.09	1	$ 1.09
CONN 2POS ULTRA-FIT 0.138"	P2	Molex	1722861302	Digi-Key	WM11673-ND	1.84	1	$ 1.84
CONN 40POS RECEPTACLE 2.54 mm	P3	Adafruit Industries	1992	Digi-Key	1528-1969-ND	3.92	1	$ 3.92
CONN 4POS DURA-CLIK 0.079"	P4, P5	Molex	560020-0420	Digi-Key	WM10864CT-ND	2.1	2	$ 4.20
CONN 50POS Bergstak Plug 0.02"	P6	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND	1.86	1	$ 1.86
RES 120 OHM 1% 1/10W 0603	R1	Yageo	RC0603FR-07120RL	Digi-Key	311-120HRCT-ND	0.13	1	$ 0.13
RES 4.7K OHM 1% 1/10W 0603	R2, R11	Yageo	RC0603FR-074K7L	Digi-Key	311-4.70KHRCT-ND	0.13	2	$ 0.27
POT 500K OHM 0.25W SMD	R3	Nidec Copal	SM-42TW504	Digi-Key	SM-42TW504CT-ND	4.52	1	$ 4.52
RES 1K OHM 5% 1/10W 0603	R4	Yageo	RC0603JR-071KL	Digi-Key	311-1.0KGRCT-ND	0.13	1	$ 0.13
RES 499K OHM 1% 1/4W 1206	R5	Stackpole Electronics	RMCF1206FT499K	Digi-Key	RMCF1206FT499KCT-ND	0.13	1	$ 0.13
RES 100K OHM 1% 1/4W 1206	R6	Yageo	RC1206FR-07100KL	Digi-Key	311-100KFRCT-ND	0.13	1	$ 0.13
RES 10K OHM 1% 1/10W 0603	R7, R9, R10	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.03	10	$ 0.32
RES 13.7K OHM 1% 1/4W 1206	R8	Yageo	RC1206FR-0713K7L	Digi-Key	311-13.7KFRCT-ND	0.13	1	$ 0.13
IC OP AMP GEN PURPOSE RR 10MHZ SOT-23-5	U1, U5	Texas Instruments	TLV316QDBVRQ1	Digi-Key	296-45323-1-ND	1.13	2	$ 2.26
IC RTC CLK/CALENDAR I2C 8-SOIC	U2	NXP Semiconductors	PCF8523T/1,118	Digi-Key	568-5306-1-ND	1.73	1	$ 1.73
IC REG BUCK ADJ 2A SYNC 6SOT	U3	Texas Instruments	TPS54202HDDCT	Digi-Key	296-44497-1-ND	2.66	1	$ 2.66
IC REG LDO 3V 0.2A 4-TDFN	U4	Microchip	MIC94310-PYMT-TR	Digi-Key	576-4761-1-ND	0.39	1	$ 0.39
CRYSTAL 32.7680KHZ 12.5PF SMD	Y1	ECS International	ECS-.327-12.5-17X-TR	Digi-Key	XC1195CT-ND	0.74	1	$ 0.74
							Total:	$ 42.87


P3
P1
C12
U5
R10
U4
C11
R9
R2
C2
U1
PHOTODIODE
R3
C1
C3
P5
LCD
DISP 2
R8
C7
U3
R5
R6
C9
C10
C8
P6
R11
LED2
L1
P4
LED1 R7
R1
IC
GND +12V
P2
LCD
DISP 1


BT1
C6
U2
Y1
C4
C5
R4


P3
P1
PHOTODIODE
C12
U5
R10
U4
C11
R9
R2
C2
U1
C13
R3
C3
P5
LCD
DISP 2
R8
R6
C9
C7
U3
R5
C10
C8
R11
LED2
L1
P4
LED1 R7
GND +12V
P2
LCD
DISP 1

Electrical Rules Check Report

Class	Document	Message
Warning	Ambient Light Sensor.SchDoc	Floating Net Label IN- at (425,570)
Error	Ambient Light Sensor.SchDoc	Net IN- has only one pin (Pin P1-1)
Warning	Ambient Light Sensor.SchDoc	Net NetC2_1 has no driving source (Pin C2-1,Pin P1-2,Pin R2-2,Pin U1-3)
Warning	Voltage Regulator.SchDoc	Net NetC9_2 has no driving source (Pin C9-2,Pin R6-2,Pin R8-1,Pin U3-4)
Warning	Voltage Regulator.SchDoc	Net NetR5_1 has no driving source (Pin R5-1,Pin U3-5)
Warning	Voltage Regulator.SchDoc	Net NetR9_2 has no driving source (Pin R9-2,Pin R10-1,Pin U5-3)
Warning	RTC.SchDoc	Net NetU2_1 has no driving source (Pin U2-1,Pin Y1-1)
Warning	Connectors.SchDoc	NetP3_8 contains IO Pin and Output Port objects (Port Pi_TX_Controller_RX)
Warning	Connectors.SchDoc	NetP3_10 contains IO Pin and Input Port objects (Port Pi_RX_Controller_TX)
Error	Ambient Light Sensor.SchDoc	Net PA2/AN2/USART2_TX has only one pin (Pin P6-23)
Error	Ambient Light Sensor.SchDoc	Net PA3/AN3/USART2_RX has only one pin (Pin P6-22)
Error	Ambient Light Sensor.SchDoc	Net PA4/AN4/SPI1_NSS has only one pin (Pin P6-21)
Error	Ambient Light Sensor.SchDoc	Net PA5/AN5/SPI1_SCK has only one pin (Pin P6-20)
Error	Ambient Light Sensor.SchDoc	Net PA6/AN6/SPI1_MISO has only one pin (Pin P6-19)
Error	Ambient Light Sensor.SchDoc	Net PA7/AN7/SPI1_MOSI has only one pin (Pin P6-18)
Warning	Connectors.SchDoc	Net PA8 has no driving source (Pin P4-2,Pin P6-7)
Warning	Connectors.SchDoc	Net PA9 has no driving source (Pin P5-2,Pin P6-6)
Error	Ambient Light Sensor.SchDoc	Net PA10 has only one pin (Pin P6-5)
Error	Ambient Light Sensor.SchDoc	Net PA15/LED_RED has only one pin (Pin P6-39)
Error	Ambient Light Sensor.SchDoc	Net PB0/AN8 has only one pin (Pin P6-17)
Error	Ambient Light Sensor.SchDoc	Net PB1/AN9 has only one pin (Pin P6-16)
Error	Ambient Light Sensor.SchDoc	Net PB2 has only one pin (Pin P6-15)
Error	Ambient Light Sensor.SchDoc	Net PB3/LED_GREEN has only one pin (Pin P6-38)
Error	Ambient Light Sensor.SchDoc	Net PB4/LED_BLUE has only one pin (Pin P6-37)
Error	Ambient Light Sensor.SchDoc	Net PB5/LED_BLUE has only one pin (Pin P6-36)
Error	Ambient Light Sensor.SchDoc	Net PB6/USART1_TX has only one pin (Pin P6-34)
Error	Ambient Light Sensor.SchDoc	Net PB7/USART1_RX has only one pin (Pin P6-33)
Error	Ambient Light Sensor.SchDoc	Net PB8/I2C1_SCL has only one pin (Pin P6-32)
Error	Ambient Light Sensor.SchDoc	Net PB9/I2C1_SDA has only one pin (Pin P6-31)
Error	Ambient Light Sensor.SchDoc	Net PB12/SPI2_NSS has only one pin (Pin P6-11)
Error	Ambient Light Sensor.SchDoc	Net PB13/SPI2_SCK has only one pin (Pin P6-10)
Error	Ambient Light Sensor.SchDoc	Net PB14/SPI2_MISO has only one pin (Pin P6-9)
Error	Ambient Light Sensor.SchDoc	Net PB15/SPI2_MOSI has only one pin (Pin P6-8)
Error	Ambient Light Sensor.SchDoc	Net PC13 has only one pin (Pin P6-30)

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII_DriverDisplay\Drive

Warnings 0

Rule Violations 140

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=2.54mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.152mm) (All)	48
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	1
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)	42
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	44
Silk to Silk (Clearance=0.254mm) (All),(All)	4
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	1
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	140

Minimum Annular Ring (Minimum=0.152mm) (All)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (-1.436mm,7.925mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (-1.4mm,16.495mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (1.4mm,29.738mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (-1.4mm,8.95mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (11.475mm,31.923mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (12.725mm,33.823mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (12.9mm,29.125mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (15.4mm,32.873mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (15.7mm,8.6mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (16.35mm,45.9mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (16.375mm,44.15mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (2.175mm,8.575mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (2.55mm,9.4mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (20mm,32.2mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (21.6mm,33.6mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (21mm,35.419mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (23.6mm,39.675mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (25.05mm,41.15mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (25.3mm,35.325mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (28.325mm,32.125mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (29.5mm,41.3mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (31.388mm,10.15mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (34.225mm,42.125mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (38.04mm,34.5mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (38.325mm,22.275mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (39.375mm,34.85mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (39.781mm,11.469mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (40.275mm,20.225mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (42.25mm,1.688mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (43.9mm,8.3mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (47.875mm,24.4mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (5.65mm,23.725mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (5.771mm,16.55mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (5.875mm,13.05mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (5.8mm,8.1mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (54.341mm,33.25mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (63.25mm,31.7mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (67.175mm,19.8mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (67.1mm,33mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (7.685mm,8.1mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (70.1mm,27.619mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (73.49mm,7.498mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (73.525mm,5.65mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (73.875mm,24.675mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (73.875mm,26.774mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (8.7mm,15.7mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (9.4mm,4.1mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (9.925mm,28.475mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)

Hole To Hole Clearance (Gap=0.254mm) (All),(All)
Hole To Hole Clearance Constraint: (Collision < 0.254mm) Between Pad Free-(-0.075mm,0mm) on Multi-Layer And Pad Free-1(0mm,0mm) on Multi-Layer

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C1-1(6.875mm,4.1mm) on Top Layer And Pad C1-2(8.225mm,4.1mm) on Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C11-1(26.5mm,36.675mm) on Top Layer And Pad C11-2(26.5mm,35.325mm)
Minimum Solder Mask Sliver Constraint: (0.222mm < 0.3mm) Between Pad C11-2(26.5mm,35.325mm) on Top Layer And Via (25.3mm,35.325mm) from
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.3mm) Between Pad C1-2(8.225mm,4.1mm) on Top Layer And Via (9.4mm,4.1mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C12-1(26.5mm,39.775mm) on Top Layer And Pad C12-2(26.5mm,41.125mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C13-1(12.825mm,31.923mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.3mm) Between Pad C13-1(12.825mm,31.923mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C2-1(16.8mm,36.15mm) on Top Layer And Pad C2-2(15.45mm,36.15mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C3-1(8.5mm,28.498mm) on Top Layer And Pad C3-2(8.5mm,29.848mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C4-1(41.325mm,10.275mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C5-1(45.25mm,10.275mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C6-1(30.55mm,18.318mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C7-1(60.124mm,29.325mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C9-1(54.325mm,27mm) on Top Layer And Pad C9-2(55.675mm,27mm) on Top
Minimum Solder Mask Sliver Constraint: (0.297mm < 0.3mm) Between Pad C9-1(54.325mm,27mm) on Top Layer And Pad R6-1(54.344mm,28.9mm) on
Minimum Solder Mask Sliver Constraint: (0.297mm < 0.3mm) Between Pad C9-2(55.675mm,27mm) on Top Layer And Pad R6-1(54.344mm,28.9mm) on
Minimum Solder Mask Sliver Constraint: (0.297mm < 0.3mm) Between Pad C9-2(55.675mm,27mm) on Top Layer And Pad R6-2(56.994mm,28.9mm) on
Minimum Solder Mask Sliver Constraint: (0.272mm < 0.3mm) Between Pad P5-3(72mm,26.6mm) on Top Layer And Via (73.875mm,26.774mm) from Top
Minimum Solder Mask Sliver Constraint: (0.272mm < 0.3mm) Between Pad P5-4(72mm,24.6mm) on Top Layer And Via (73.875mm,24.675mm) from Top
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P6-(0.8mm,20.55mm) on Multi-Layer And Pad P6-(2.3mm,21.3mm) on Top
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P6-(0.8mm,6.45mm) on Multi-Layer And Pad P6-(2.3mm,5.7mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.252mm < 0.3mm) Between Pad P6-21(4.1mm,9.5mm) on Top Layer And Via (2.55mm,9.4mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.153mm < 0.3mm) Between Pad R10-2(34.225mm,41.044mm) on Top Layer And Via (34.225mm,42.125mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U1-1(16.775mm,31.923mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U1-2(16.775mm,32.873mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.297mm < 0.3mm) Between Pad U1-4(14.025mm,33.823mm) on Top Layer And Via (12.725mm,33.823mm) from
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U3-1(62.35mm,27.7mm) on Top Layer And Pad U3-2(63.3mm,27.7mm) on Top
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U3-2(63.3mm,27.7mm) on Top Layer And Pad U3-3(64.25mm,27.7mm) on Top
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U3-4(64.25mm,30.1mm) on Top Layer And Pad U3-5(63.3mm,30.1mm) on Top
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U3-5(63.3mm,30.1mm) on Top Layer And Pad U3-6(62.35mm,30.1mm) on Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U4-1(24.2mm,38.809mm) on Top Layer And Pad U4-2(23.6mm,38.809mm) on
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.3mm) Between Pad U4-1(24.2mm,38.809mm) on Top Layer And Pad U4-5(23.9mm,38.094mm) on
Minimum Solder Mask Sliver Constraint: (0.234mm < 0.3mm) Between Pad U4-1(24.2mm,38.809mm) on Top Layer And Via (23.6mm,39.675mm) from Top
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.3mm) Between Pad U4-2(23.6mm,38.809mm) on Top Layer And Pad U4-5(23.9mm,38.094mm) on
Minimum Solder Mask Sliver Constraint: (0.113mm < 0.3mm) Between Pad U4-2(23.6mm,38.809mm) on Top Layer And Via (23.6mm,39.675mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U4-3(23.6mm,37.369mm) on Top Layer And Pad U4-4(24.2mm,37.369mm) on
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.3mm) Between Pad U4-3(23.6mm,37.369mm) on Top Layer And Pad U4-5(23.9mm,38.094mm) on
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.3mm) Between Pad U4-4(24.2mm,37.369mm) on Top Layer And Pad U4-5(23.9mm,38.094mm) on
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U5-1(29.55mm,37.125mm) on Top Layer And Pad U5-2(30.5mm,37.125mm) on
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U5-2(30.5mm,37.125mm) on Top Layer And Pad U5-3(31.45mm,37.125mm) on
Minimum Solder Mask Sliver Constraint: (0.222mm < 0.3mm) Between Via (-1.436mm,7.925mm) from Top Layer to Bottom Layer And Via
Minimum Solder Mask Sliver Constraint: (0.103mm < 0.3mm) Between Via (2.175mm,8.575mm) from Top Layer to Bottom Layer And Via (2.55mm,9.4mm)

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad C9-1(54.325mm,27mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad C9-2(55.675mm,27mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad Free-1(0mm,0mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad Free-1(0mm,0mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.14mm < 0.178mm) Between Pad P1-3(-0.8mm,38.02mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.163mm < 0.178mm) Between Pad P1-3(8.4mm,38.02mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad P6-1(4.1mm,19.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad P6-25(4.1mm,7.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad P6-26(0.5mm,7.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad P6-50(0.5mm,19.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad R5-1(67.2mm,30.925mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad R5-1(67.2mm,30.925mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad R5-2(67.2mm,28.275mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad R5-2(67.2mm,28.275mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad R6-1(54.344mm,28.9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad R6-1(54.344mm,28.9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad R6-2(56.994mm,28.9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad R6-2(56.994mm,28.9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad R8-1(56.994mm,31.374mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad R8-1(56.994mm,31.374mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad R8-2(54.344mm,31.374mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad R8-2(54.344mm,31.374mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U1-1(16.775mm,31.923mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U1-2(16.775mm,32.873mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U1-3(16.775mm,33.823mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U1-4(14.025mm,33.823mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U1-5(14.025mm,31.923mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad U4-1(24.2mm,38.809mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U4-2(23.6mm,38.809mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad U4-3(23.6mm,37.369mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad U4-4(24.2mm,37.369mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U5-1(29.55mm,37.125mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U5-2(30.5mm,37.125mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U5-3(31.45mm,37.125mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U5-4(31.45mm,39.875mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U5-5(29.55mm,39.875mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.039mm < 0.178mm) Between Pad Y1-1(34.55mm,12.4mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.039mm < 0.178mm) Between Pad Y1-1(34.55mm,12.4mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.178mm) Between Pad Y1-2(34.55mm,6.9mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.078mm < 0.178mm) Between Pad Y1-2(34.55mm,6.9mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.178mm) Between Pad Y1-3(31.35mm,6.9mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.078mm < 0.178mm) Between Pad Y1-3(31.35mm,6.9mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.039mm < 0.178mm) Between Pad Y1-4(31.35mm,12.4mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.039mm < 0.178mm) Between Pad Y1-4(31.35mm,12.4mm) on Bottom Layer And Track

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.13mm < 0.254mm) Between Text "LED2" (46.625mm,16.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.2mm < 0.254mm) Between Text "P1" (-2.075mm,43.325mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.2mm < 0.254mm) Between Text "P1" (-2.075mm,43.325mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "PHOTODIODE" (-1.75mm,33.725mm) on Top Overlay And Track

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Text "LCD

DISP 2" (76.5mm,35.75mm) on Top Overlay