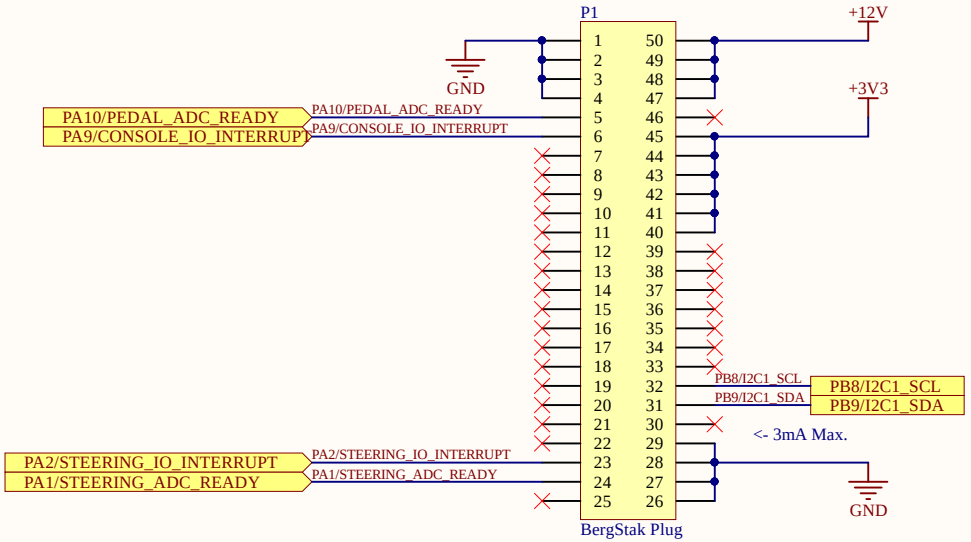
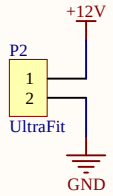
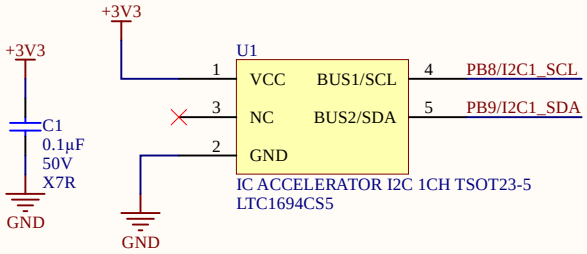
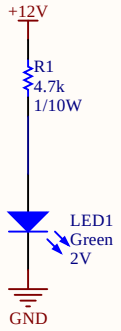
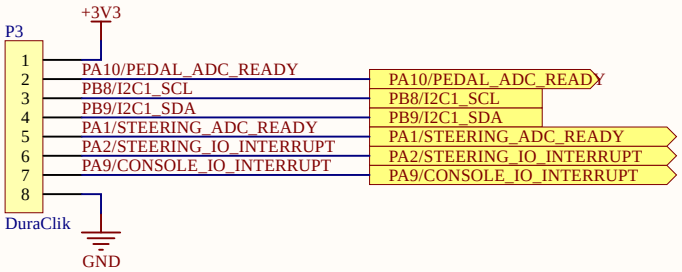


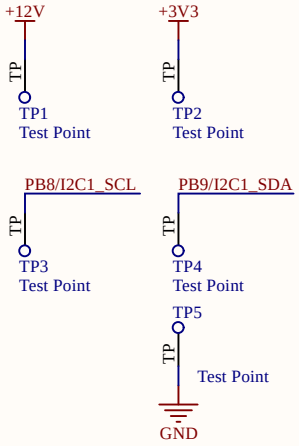
Project: *MSXII_DriverControlsCarrierBoard.PrjPcb*		MIDNIGHT SUN
Title: **Controller Board Interface**		
Project Author: Mena Labib		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 2.1	
Date: 2018-05-21	Sheet 1 of 2	Website: www.uwmidsun.com









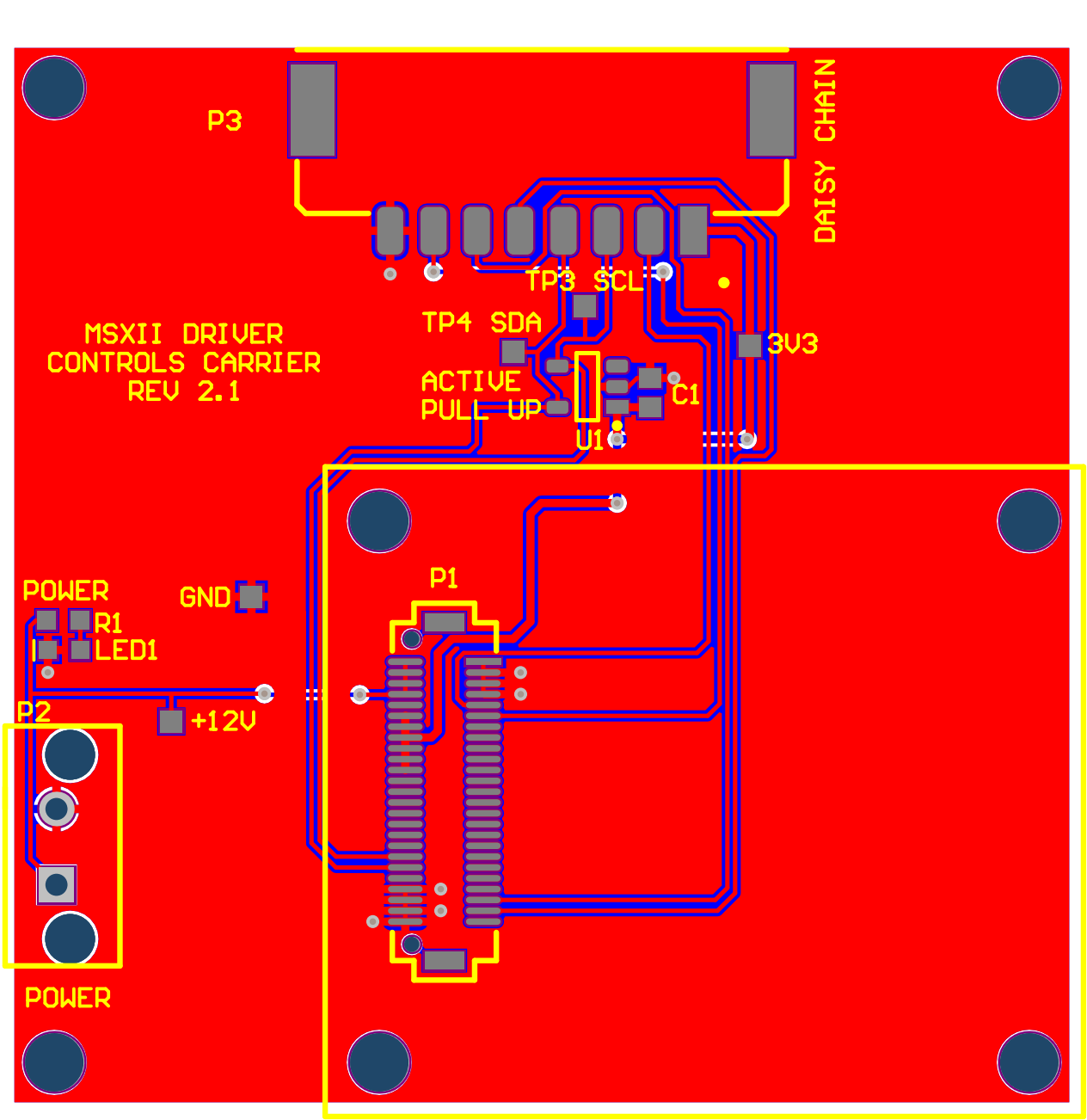


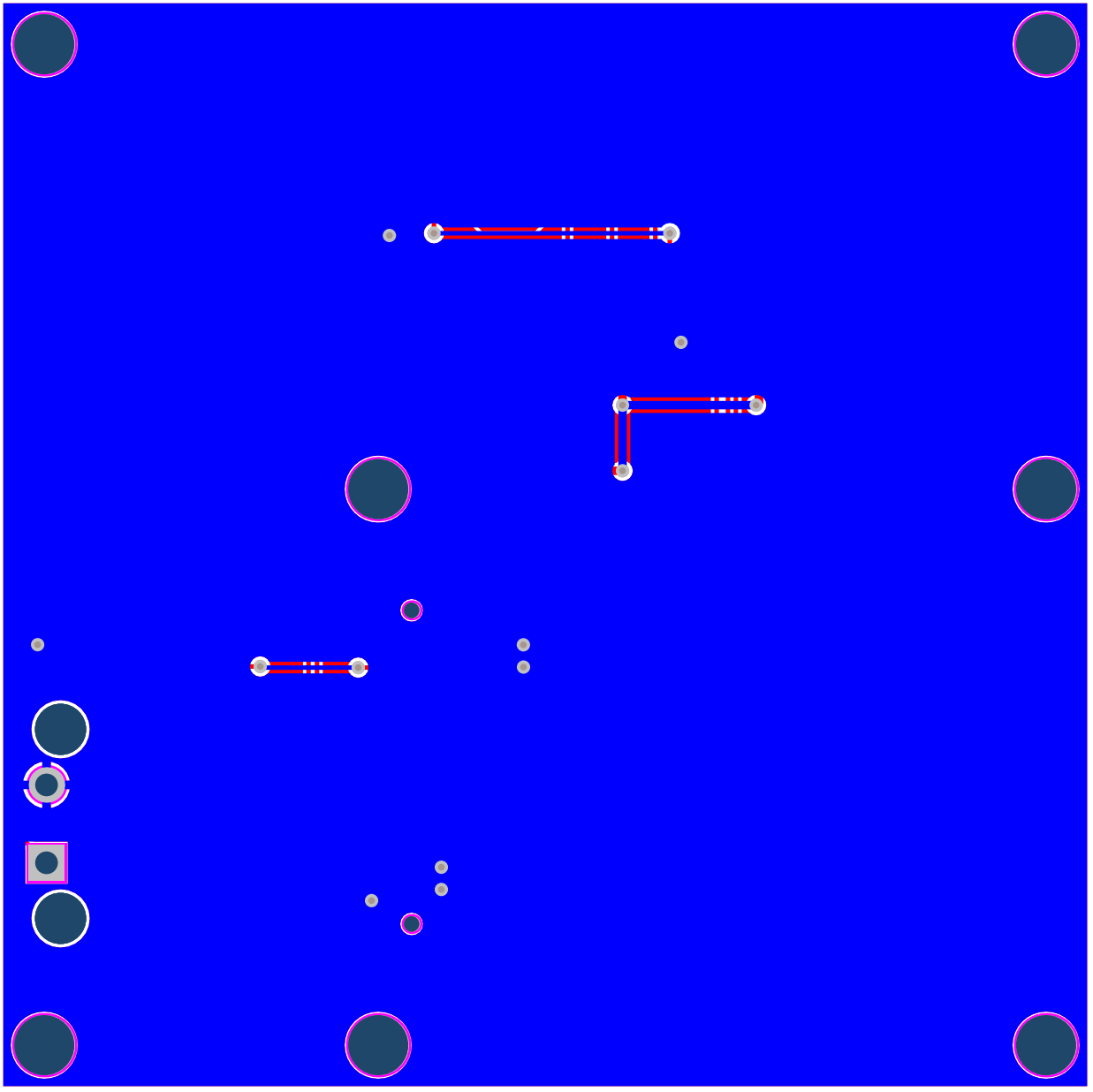
Project: *MSXII_DriverControlsCarrierBoard.PrjPcb*		MIDNIGHT SUN
Title: **Driver Controls Carrier**		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Author: Mena Labib		
Size: Letter	Revision: 2.1	
Date: 2018-05-21	Sheet 2 of 2	Website: www.uwmidsun.com

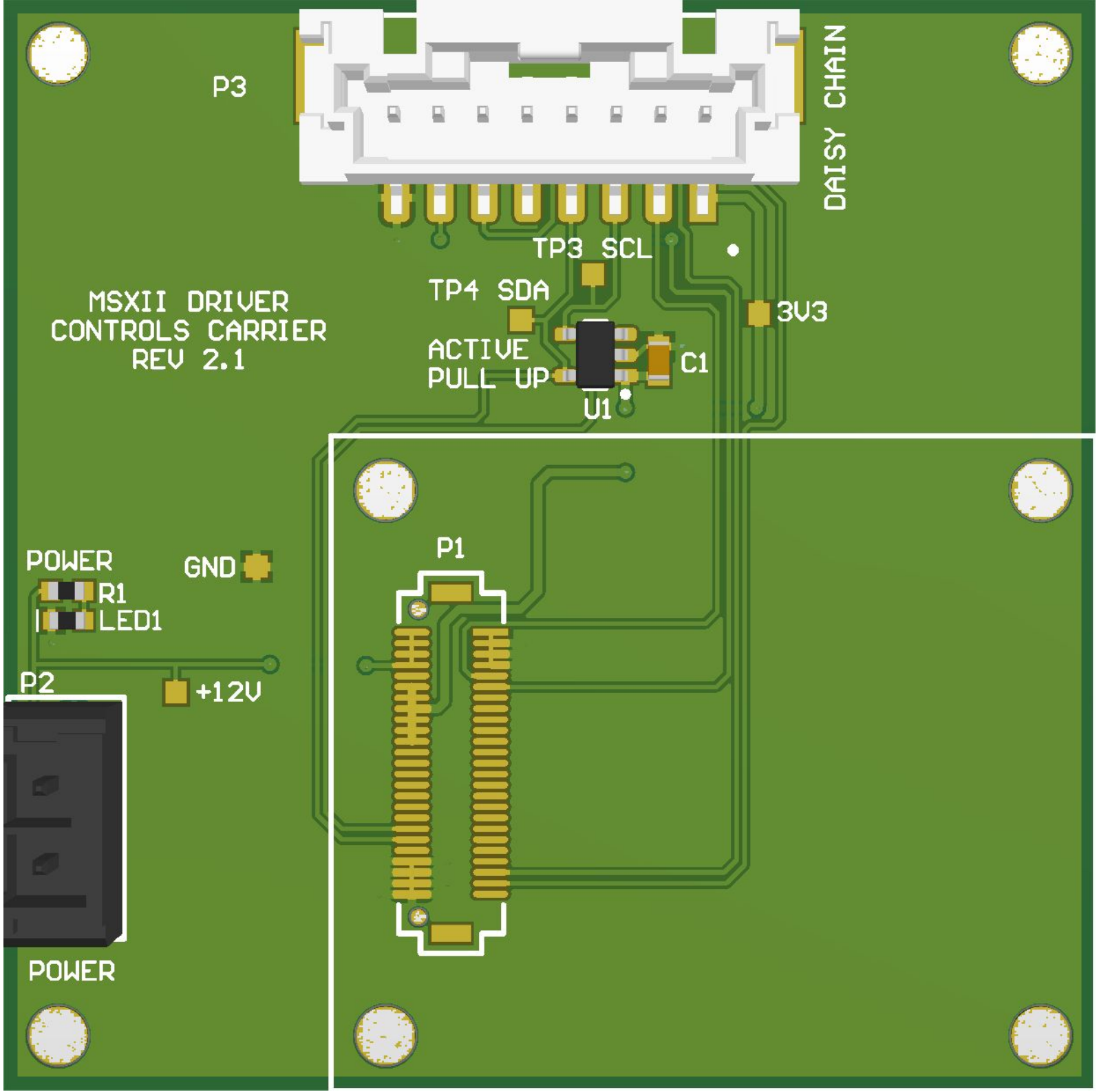
Bill of Materials

Project:	MSXII_DriverControlsCarrierBoard.PrjPcb
Revision:	2.1
Project Lead:	Mena Labib
Generated On:	2018-05-21 8:53:10 PM
Production Quantity:	1
Currency	CAD
Total Parts Count:	12

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Supplier Order Qty 1	Supplier Subtotal 1
CAP CER 0.1UF 50V 10% X7R 0603	C1	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.2	1	$ 0.20
LED GREEN CLEAR 2V 0603	LED1	Wurth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.18	1	$ 0.18
CONN 50POS Bergstak Plug 0.02"	P1	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND	1.79	1	$ 1.79
CONN 2POS ULTRA-FIT 0.138"	P2	Molex	1722861302	Digi-Key	WM11673-ND	1.77	1	$ 1.77
CONN 8POS DURA-CLIK 0.079"	P3	Molex	560020-0820	Digi-Key	WM10868CT-ND	1.84	1	$ 1.84
RES 4.7K OHM 1% 1/10W 0603	R1	Yageo	RC0603FR-074K7L	Digi-Key	311-4.70KHRCT-ND	0.13	1	$ 0.13
Test Point	TP1							
Test Point	TP2							
Test Point	TP3							
Test Point	TP4							
Test Point	TP5							
IC ACCELERATOR I2C 1CH TSOT23-5	U1	Analog Devices / Linear Technology	LTC1694CS5#TRMPBF	Digi-Key	LTC1694CS5#TRMPBFCT-ND	4.15	1	$ 4.15
							Total:	$ 10.06


P3
DAISY CHAIN
TP3 SCL
TP4 SDA
3V3
MSXII DRIVER
CONTROLS CARRIER
REV 2.1
ACTIVE
PULL UP
C1
U1
P1
POWER
GND
R1
LED1
P2
+12V
POWER




P3
DAISY CHAIN
TP3 SCL
TP4 SDA
3V3
MSXII DRIVER
CONTROLS CARRIER
REV 2.1
ACTIVE
PULL UP
C1
U1
P1
POWER
GND
R1
LED1
P2
+12V
POWER

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for MSXII_DriverControlsCarrierBoard.PrjPcb

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII_DriverControlsCarrie

Warnings 0
Rule Violations 11

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.203mm) (Max=2.54mm) (Preferred=0.203mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	7
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	4
Silk To Solder Mask (Clearance=0.254mm) (Disabled)(IsPad),(All)	0
Silk to Silk (Clearance=0.254mm) (Disabled)(All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	11

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(17.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(17.5mm,27.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,47.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(47.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(47.5mm,27.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(47.5mm,47.5mm) on Multi-Layer Actual Hole Size = 2.7mm

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad ACTIVE PULL UP-1(28.475mm,32.75mm) on Top Layer And Pad ACTIVE
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad ACTIVE PULL UP-2(28.475mm,33.7mm) on Top Layer And Pad ACTIVE
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(19mm,22.05mm) on Multi-Layer And Pad P1-(20.5mm,22.8mm) on Top
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(19mm,7.95mm) on Multi-Layer And Pad P1-(20.5mm,7.2mm) on Top