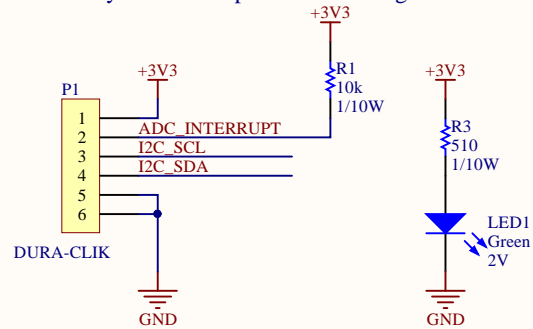
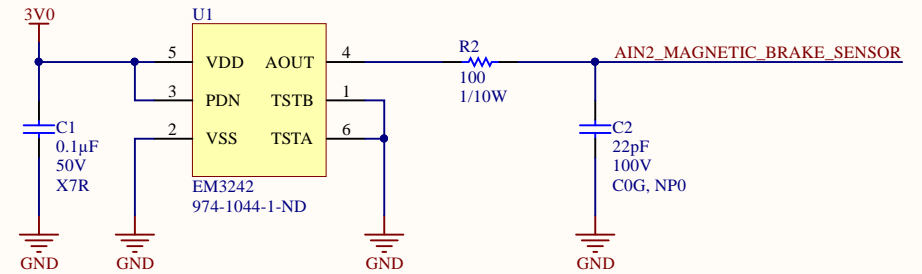


Daisy-Chained Input from Steering Wheel Interface Board

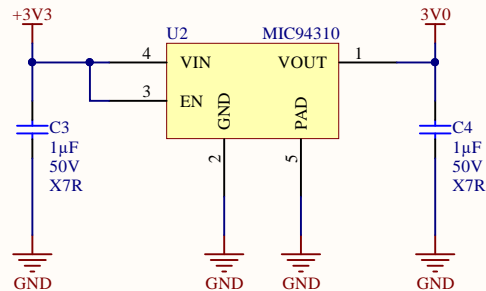


Brake Pedal Magnetic Sensor

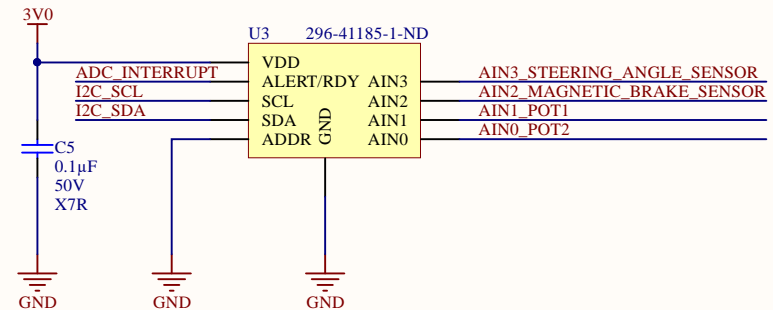


Max Output Capacitance = 200 pF

Power Supply

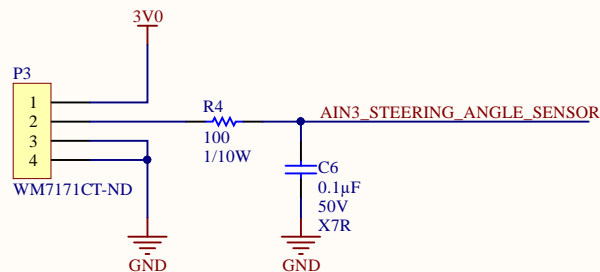


ADC



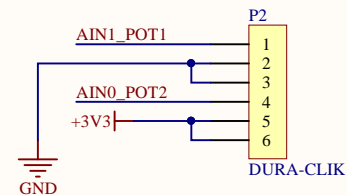
I2C Address:
1001000 (0x48)

Steering Angle Sensor



fc = 15.9 kHz

Accelerator Pedal Connector



Project: **MSXII_PedalBoard.PrjPcb**

Title: **Pedal Interface Board**

Project Lead: Taiping Li

Size: Letter

Date: 2018-05-21

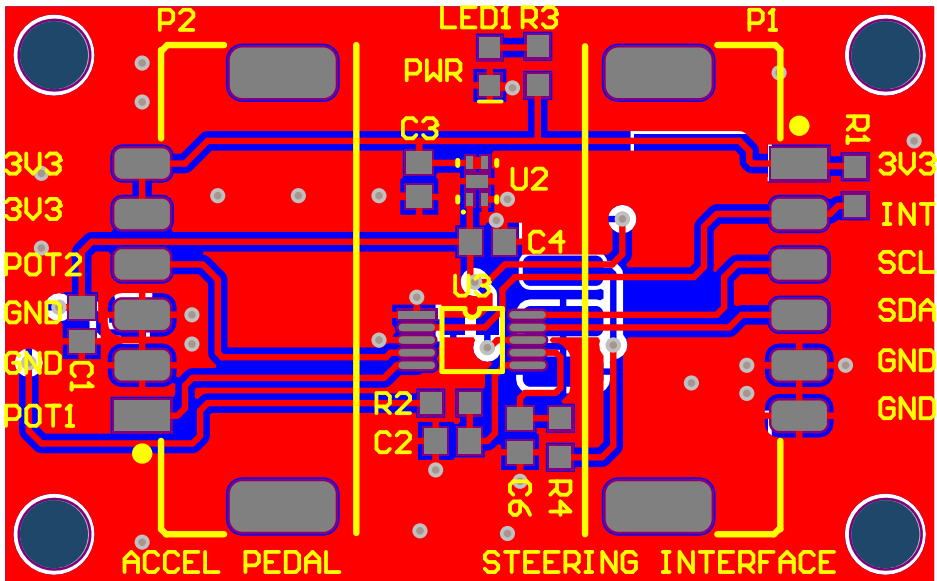
Revision: 2.0

Sheet1 of 1

MIDNIGHT SUN

University of Waterloo
200 University Ave W
Waterloo, ON, Canada
N2L 3E9

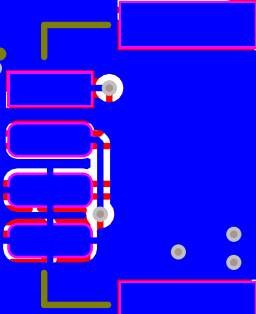
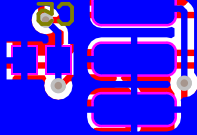
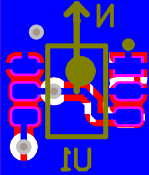
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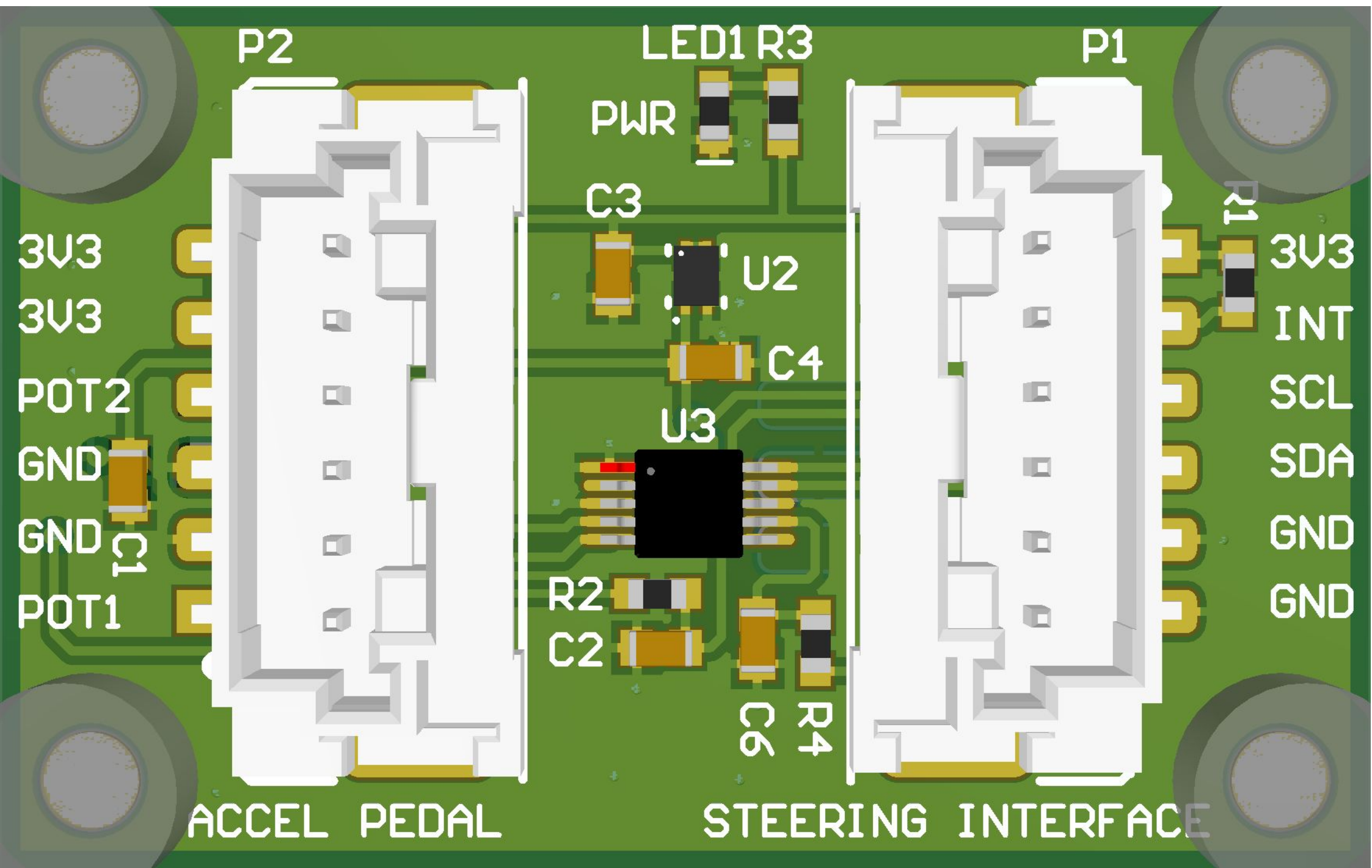


MSXII DRIVER CONTROLS
PEDAL BOARD
REV 2.1

3V0
SENSE
END
END

STEERING ANGLE SENSOR





Electrical Rules Check Report

Class	Document	Message
		Successful Compile for MSXII_PedalBoard.PrjPcb

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII_PedalBoard\PedalBc

Warnings 0
Rule Violations 36

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.254mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	4
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	10
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	22
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	36

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,21.5mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(35.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(35.5mm,21.5mm) on Multi-Layer Actual Hole Size = 2.7mm	

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-1(5.65mm,12.5mm) on Bottom Layer And Pad U1-2(5.65mm,11.5mm) on	
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-2(5.65mm,11.5mm) on Bottom Layer And Pad U1-3(5.65mm,10.5mm) on	
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-4(1.55mm,10.5mm) on Bottom Layer And Pad U1-5(1.55mm,11.5mm) on	
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-5(1.55mm,11.5mm) on Bottom Layer And Pad U1-6(1.55mm,12.5mm) on	
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U2-1(19mm,15.785mm) on Top Layer And Pad U2-2(19.6mm,15.785mm) on	
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.254mm) Between Pad U2-1(19mm,15.785mm) on Top Layer And Pad U2-5(19.3mm,16.5mm) on	
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.254mm) Between Pad U2-2(19.6mm,15.785mm) on Top Layer And Pad U2-5(19.3mm,16.5mm) on	
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U2-3(19.6mm,17.225mm) on Top Layer And Pad U2-4(19mm,17.225mm) on	
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.254mm) Between Pad U2-3(19.6mm,17.225mm) on Top Layer And Pad U2-5(19.3mm,16.5mm) on	
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.254mm) Between Pad U2-4(19mm,17.225mm) on Top Layer And Pad U2-5(19.3mm,16.5mm) on	

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.188mm < 0.254mm) Between Arc (18.746mm,15.277mm) on Top Overlay And Pad U2-1(19mm,15.785mm)
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED1-2(19.8mm,20.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad P3-(28.188mm,6.4mm) on Bottom Layer And Text "STEERING ANGLE"
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad R3-2(21.7mm,21.85mm) on Top Layer And Text "R3" (21.1mm,22.6mm) on
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U2-1(19mm,15.785mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U2-2(19.6mm,15.785mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U2-3(19.6mm,17.225mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U2-4(19mm,17.225mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad U3-1(16.9mm,11.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad U3-1(16.9mm,11.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U3-10(21.3mm,11.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad U3-10(21.3mm,11.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad U3-2(16.9mm,10.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad U3-3(16.9mm,10.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad U3-4(16.9mm,9.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad U3-5(16.9mm,9.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U3-5(16.9mm,9.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U3-6(21.3mm,9.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad U3-6(21.3mm,9.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad U3-7(21.3mm,9.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad U3-8(21.3mm,10.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad U3-9(21.3mm,10.7mm) on Top Layer And Track