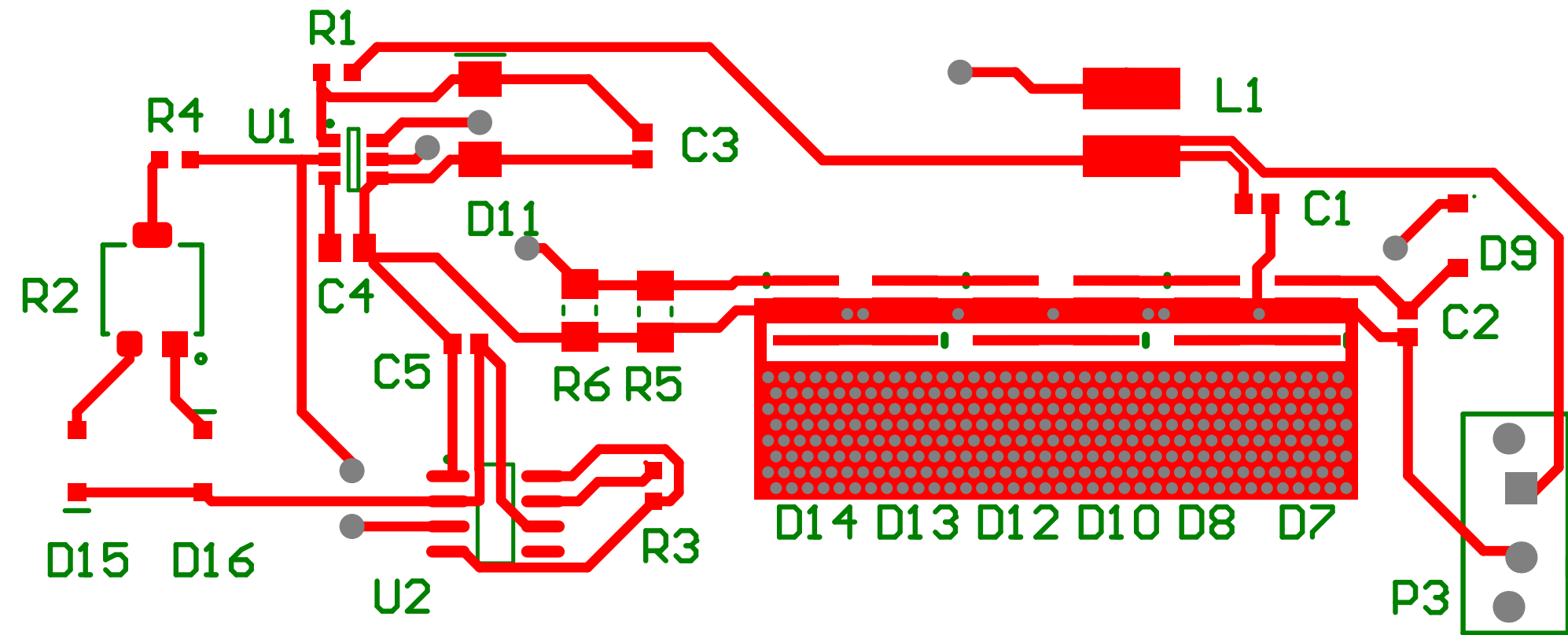
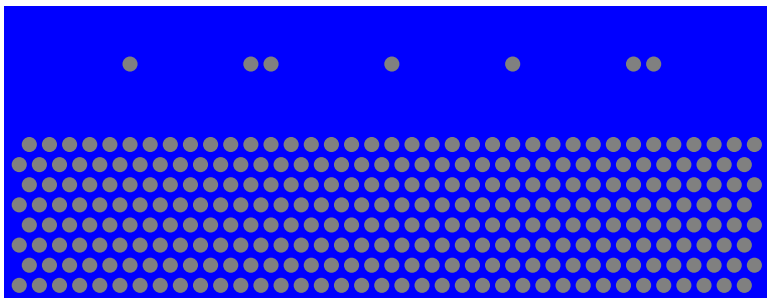
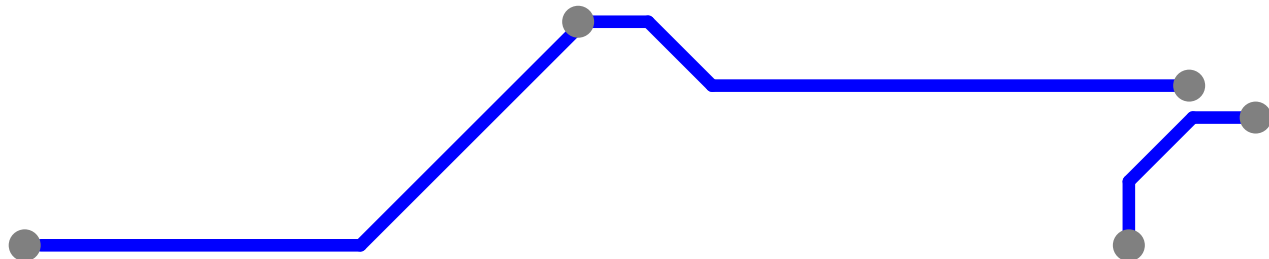


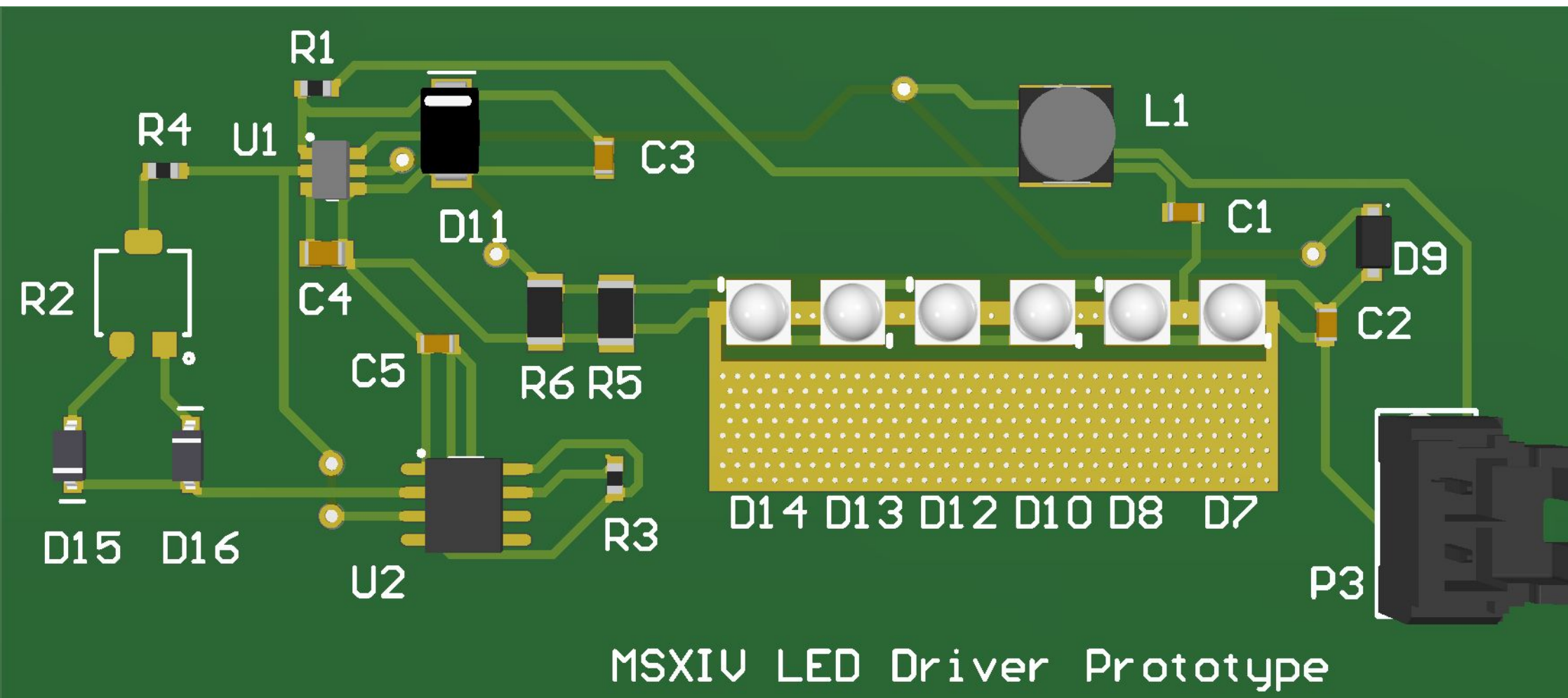
Bill of Materials	
Project:	TailLightsPrototype.PrjPCB
Revision:	1.0
Project Lead:	<Parameter ProjectAuthor not found>
Generated On:	2019-09-14 11:58 AM
Production Quantity:	1
Currency	USD
Total Parts Count:	25

[illegible]



MSXIV LED Driver Prototype





Design Rules Verification Report

Filename : C:\Users\Liam\Documents\UWaterloo\Midnight Sun\Hardware Repository\ha

Warnings 0
Rule Violations 500

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Clearance Constraint (Gap=0.1mm) (IsStitchingVia and InNet('GND')),(IsVia and (Not IsStitchingVia)) Or IsPad)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.5mm) (Max=0.5mm) (Preferred=0.5mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	492
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	8
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	500

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)

[illegible]

[illegible]

[illegible]

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)

[illegible]

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Arc (74.47mm,26.74mm) on Top Overlay And Pad D9-1(73.66mm,26.4mm)
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D10-3(55.88mm,19.48mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D11-2(24.23mm,32.664mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D12-3(50.8mm,22.48mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D13-3(45.72mm,19.48mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D14-3(40.718mm,22.48mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D7-3(66.04mm,19.48mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D8-3(60.96mm,22.48mm) on Top Layer And Track