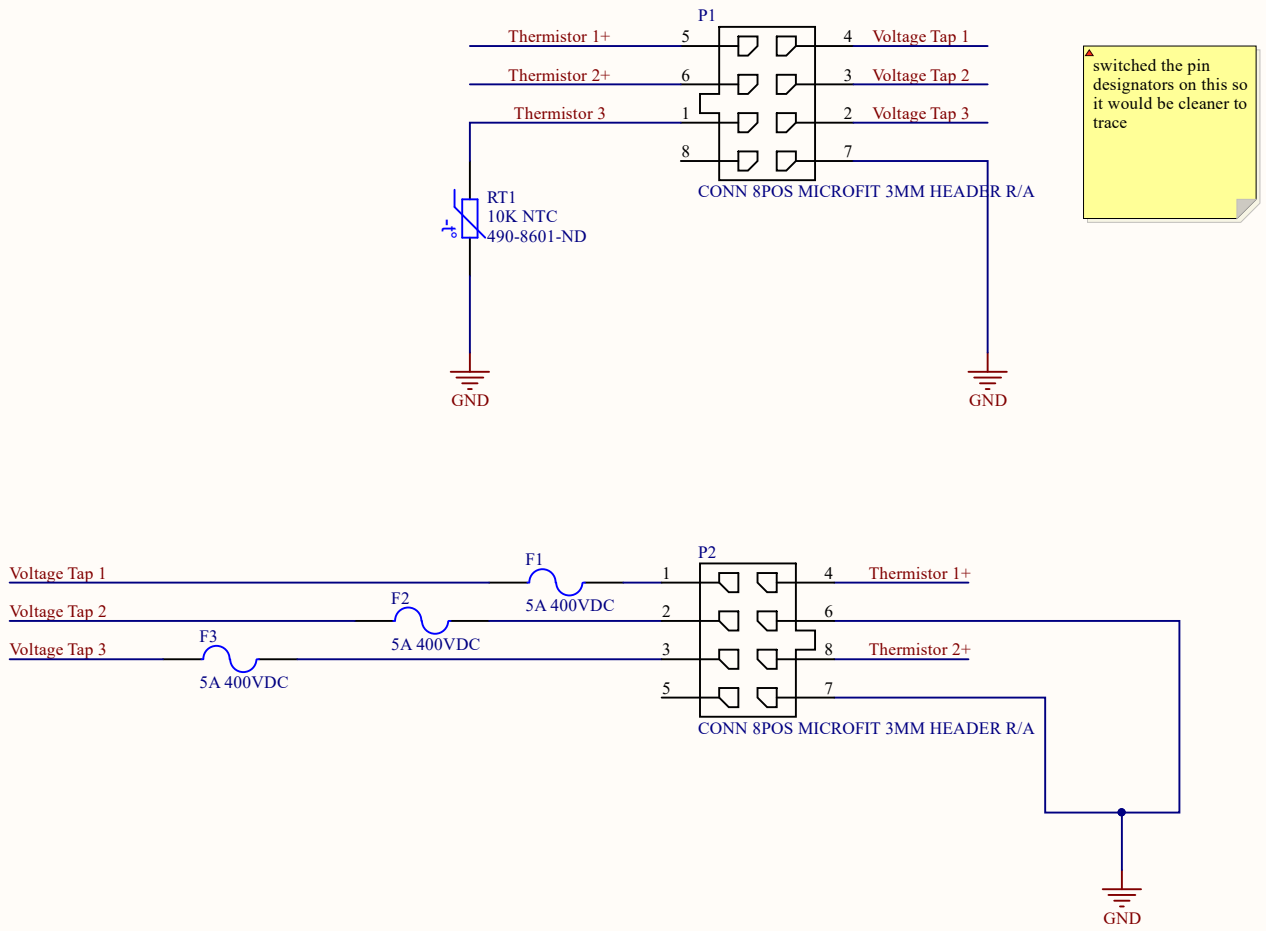
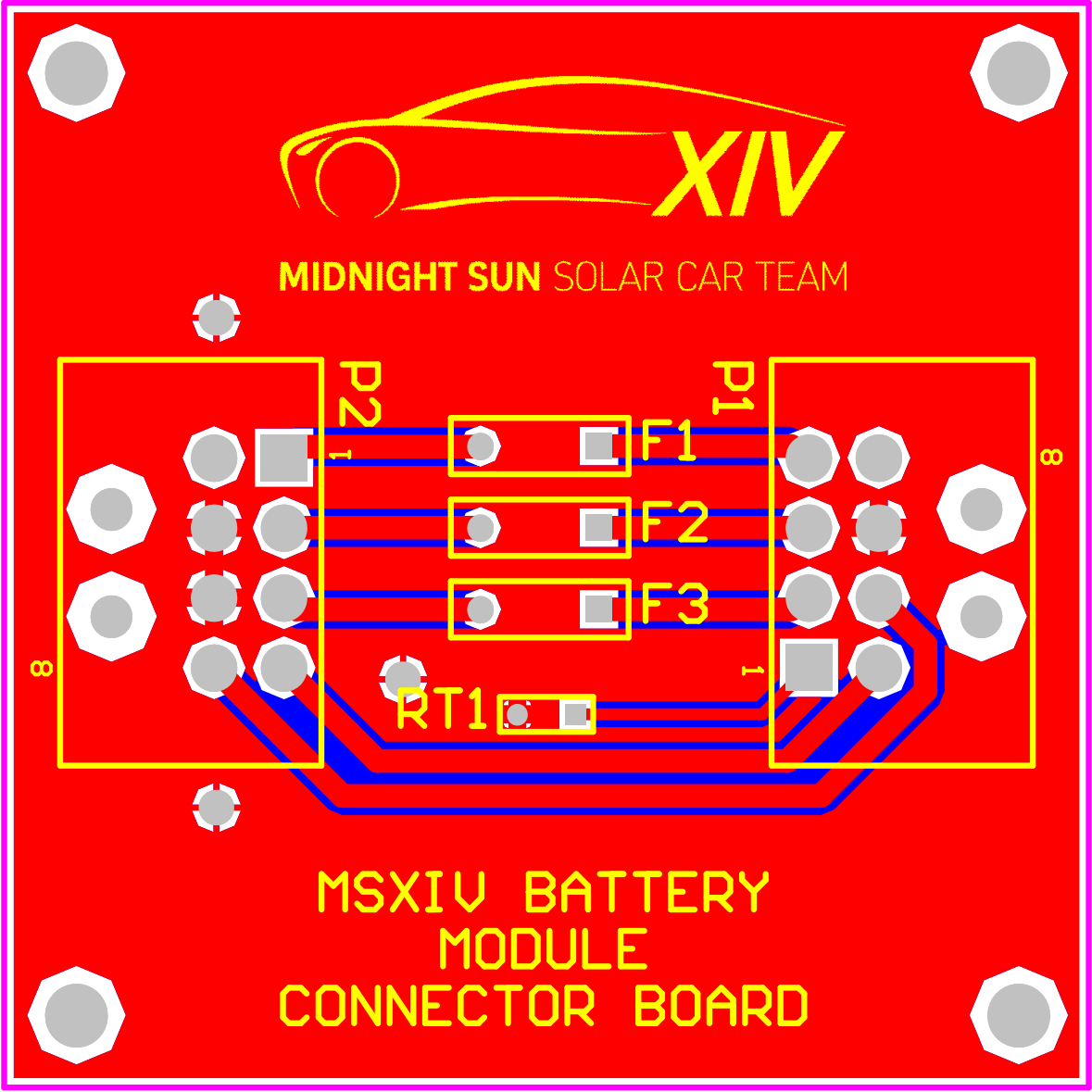


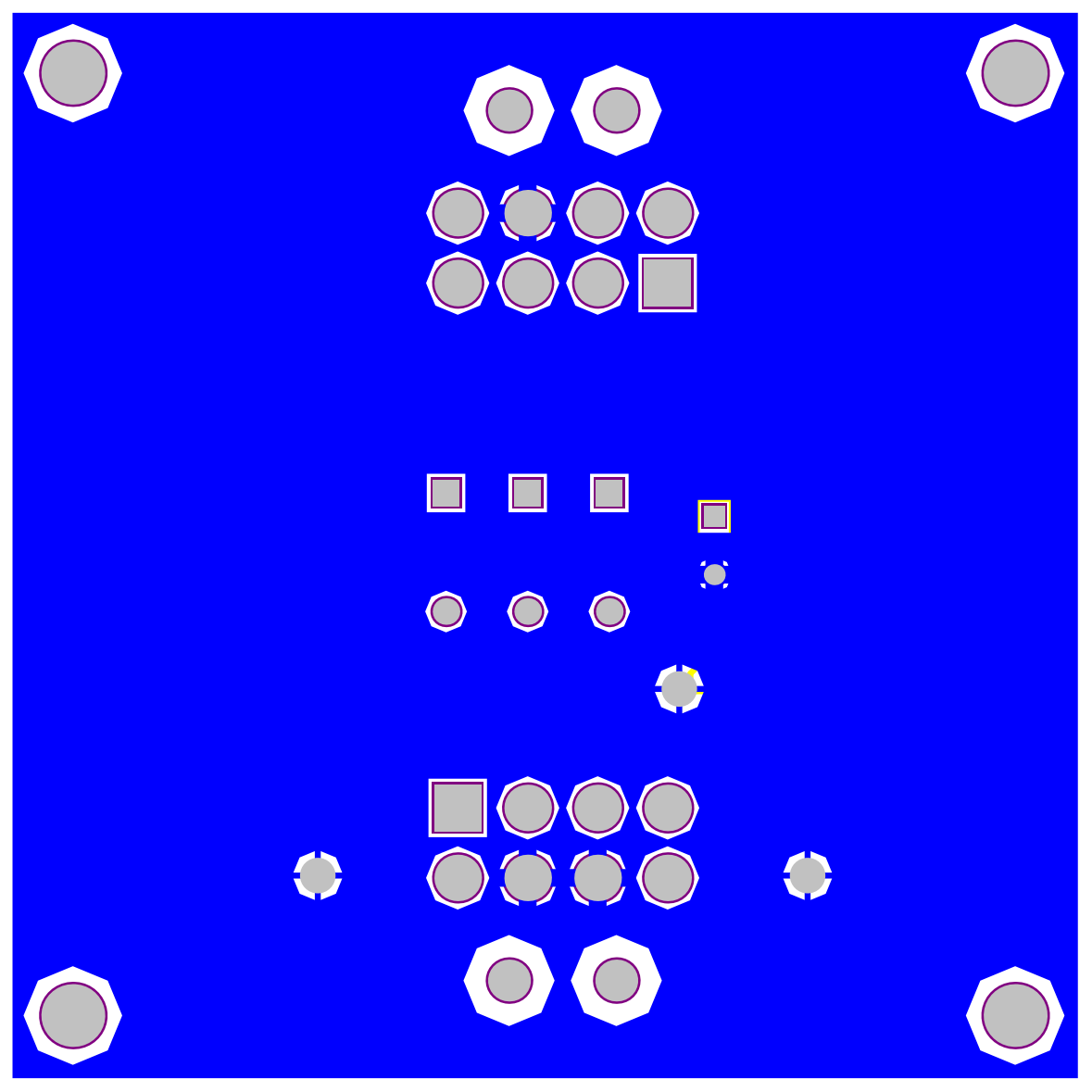
Project: MSXIV_BatteryModuleConnectorBoard.PrjPcb		MIDNIGHT SUN
Title: *		
Project Author: Aashmika Mali		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.0	
Date: 2019-09-15	Sheet* of *	Website: uwmidsun.com

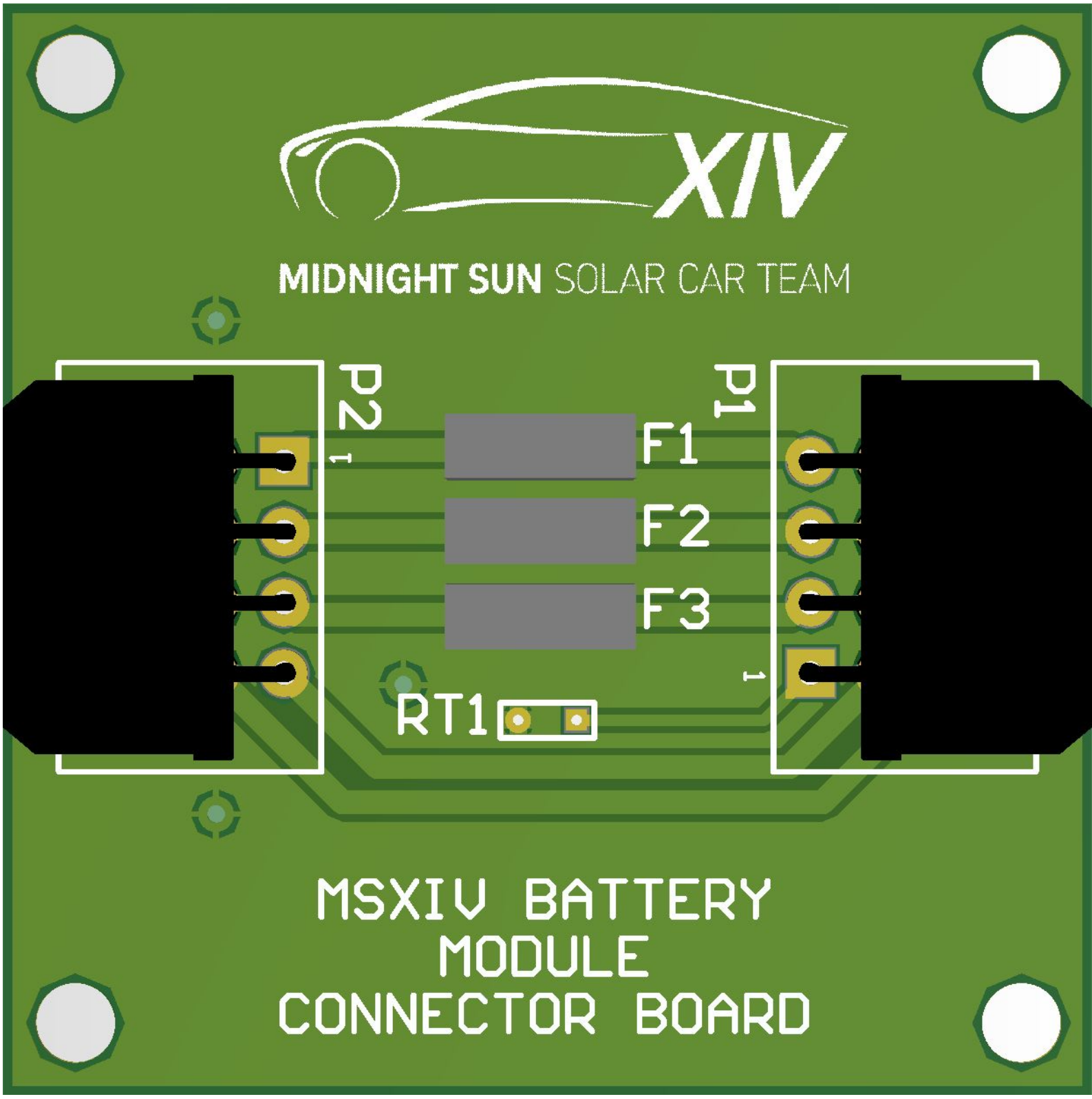
Bill of Materials

Project:	0V_BatteryModuleConnectorBoard.PrjPcb
Revision:	1.0
Project Lead:	Aashmika Mali
Generated On:	2019-09-15 2:47 PM
Production Quantity:	1
Currency:	USD
Total Parts Count:	6

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Pric
FUSE 5A 125VAC/400VDC RADIAL	F1, F2, F3			Digi-Key	283-2770-ND	
CONN 8POS MICROFIT 3MM HEADER R/ A	P1, P2	Molex	0430450800	Digi-Key	WM1816-ND	
NTC THERMISTOR 10K 1% BEAD	RT1			Digi-Key	490-8601-ND	


XIV
MIDNIGHT SUN SOLAR CAR TEAM
P2
1
8
P1
1
8
F1
F2
F3
RT1
MSXIV BATTERY
MODULE
CONNECTOR BOARD




XIV
MIDNIGHT SUN SOLAR CAR TEAM
J2
1
J1
F1
F2
F3
RT1
1
MSXIV BATTERY
MODULE
CONNECTOR BOARD

Electrical Rules Check Report

Class	Document	Message
Warning	MSXIV_BatteryModuleConnectorBoard.SchDoc	Off grid Net Label Thermistor 1+ at 5980.115mil,4500mil
Warning	MSXIV_BatteryModuleConnectorBoard.SchDoc	Off grid Net Label Thermistor 2+ at 5980.115mil,4100mil
Warning	MSXIV_BatteryModuleConnectorBoard.SchDoc	Off grid Net Label Thermistor 3 at 4131.041mil,6900mil

Design Rules Verification Report

Filename : C:\Users\Aashmika Mali\Documents\First Year\Midnight Sun\hardware\MSXIV_BatteryModuleConnectorBoard\MSXIV_BatteryModu

Warnings 0
Rule Violations 18

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=100mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	8
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	6
Silk to Silk (Clearance=10mil) (All),(All)	4
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	18

Hole Size Constraint (Min=1mil) (Max=100mil) (All)
Hole Size Constraint: (133.858mil > 100mil) Pad Free-(0mil,0mil) on Multi-Layer Actual Hole Size = 133.858mil
Hole Size Constraint: (133.858mil > 100mil) Pad Free-(0mil,1590.551mil) on Multi-Layer Actual Hole Size = 133.858mil
Hole Size Constraint: (133.858mil > 100mil) Pad Free-(1590.551mil,0mil) on Multi-Layer Actual Hole Size = 133.858mil
Hole Size Constraint: (133.858mil > 100mil) Pad Free-(1590.551mil,1590.551mil) on Multi-Layer Actual Hole Size = 133.858mil
Hole Size Constraint: (122.047mil > 100mil) Pad P1-(736.221mil,1527.559mil) on Multi-Layer Actual Hole Size = 122.047mil
Hole Size Constraint: (122.047mil > 100mil) Pad P1-(917.323mil,1527.559mil) on Multi-Layer Actual Hole Size = 122.047mil
Hole Size Constraint: (122.047mil > 100mil) Pad P2-(736.221mil,59.055mil) on Multi-Layer Actual Hole Size = 122.047mil
Hole Size Constraint: (122.047mil > 100mil) Pad P2-(917.323mil,59.055mil) on Multi-Layer Actual Hole Size = 122.047mil

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1082.677mil,842.52mil) on Multi-Layer And Track (1053.15mil,714.567mil)(1053.15mil,872.047mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1082.677mil,842.52mil) on Multi-Layer And Track (1053.15mil,872.047mil)(1112.205mil,872.047mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1082.677mil,842.52mil) on Multi-Layer And Track (1112.205mil,714.567mil)(1112.205mil,872.047mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.941mil < 10mil) Between Pad RT1-2(1082.677mil,744.095mil) on Multi-Layer And Track (1053.15mil,714.567mil)(1053.15mil,872.047mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (8.833mil < 10mil) Between Pad RT1-2(1082.677mil,744.095mil) on Multi-Layer And Track (1053.15mil,714.567mil)(1112.205mil,714.567mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.941mil < 10mil) Between Pad RT1-2(1082.677mil,744.095mil) on Multi-Layer And Track (1112.205mil,714.567mil)(1112.205mil,872.047mil) on Top Overlay [Top Overlay] to [Top

Silk to Silk (Clearance=10mil) (All),(All)
Silk To Silk Clearance Constraint: (7.806mil < 10mil) Between Text "1" (1003.937mil,1125.984mil) on Top Overlay And Track (484.252mil,1173.228mil)(1169.291mil,1173.228mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (7.806mil < 10mil) Between Text "1" (649.606mil,460.63mil) on Top Overlay And Track (484.252mil,413.386mil)(1169.291mil,413.386mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "8" (1015.748mil,-43.307mil) on Top Overlay And Track (484.252mil,-27.559mil)(1169.291mil,-27.559mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "8" (637.795mil,1629.921mil) on Top Overlay And Track (484.252mil,1614.173mil)(1169.291mil,1614.173mil) on Top Overlay Silk Text to Silk Clearance