
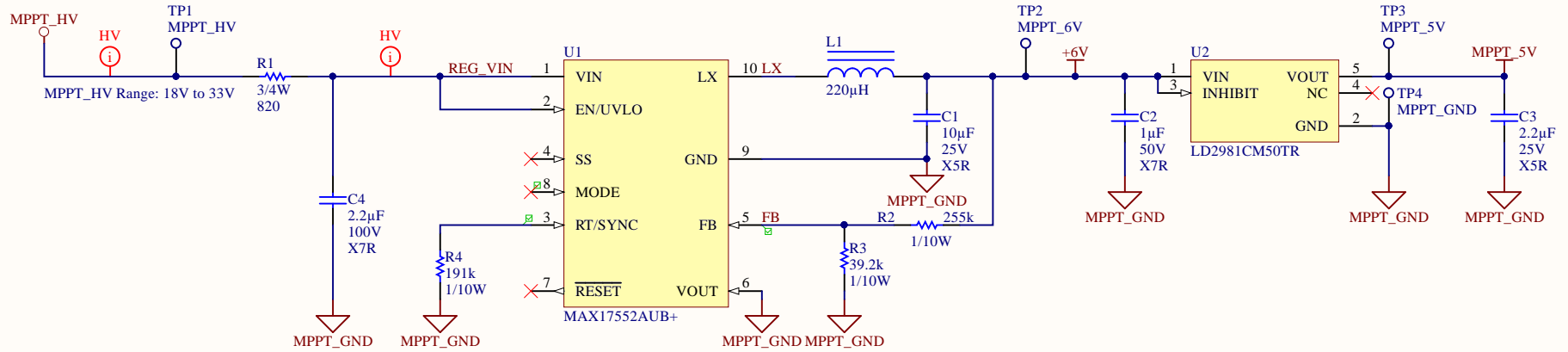
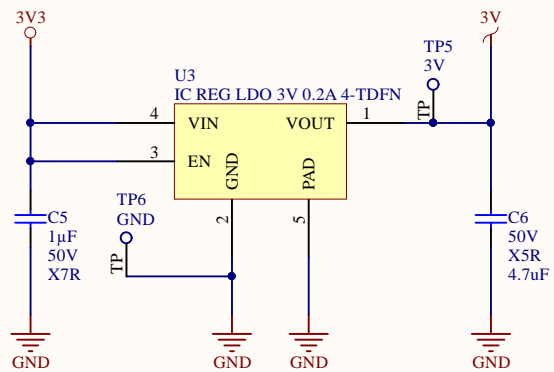


Project: <i><b>MSXII_SolarSenseSlave.PrjPcb</b></i>		
Title: <b>Controller Board Interface</b>		
Project Lead: <b>Peiliang Guo</b>		University of Waterloo 200 University Ave W Waterloo, ON, Canada <b>N2L 3E9</b>
Size: <b>Letter</b>	Revision: <b>1.13</b>	
Date: <b>2018-02-27</b>	Sheet <b>2</b> of <b>4</b>	Website: <b><a href="http://www.uwmidsun.com">www.uwmidsun.com</a></b>

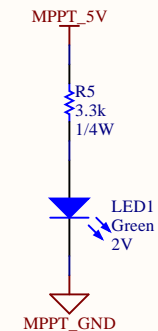
# Voltage Sense Power Supply




# Isolated Side Power Supply

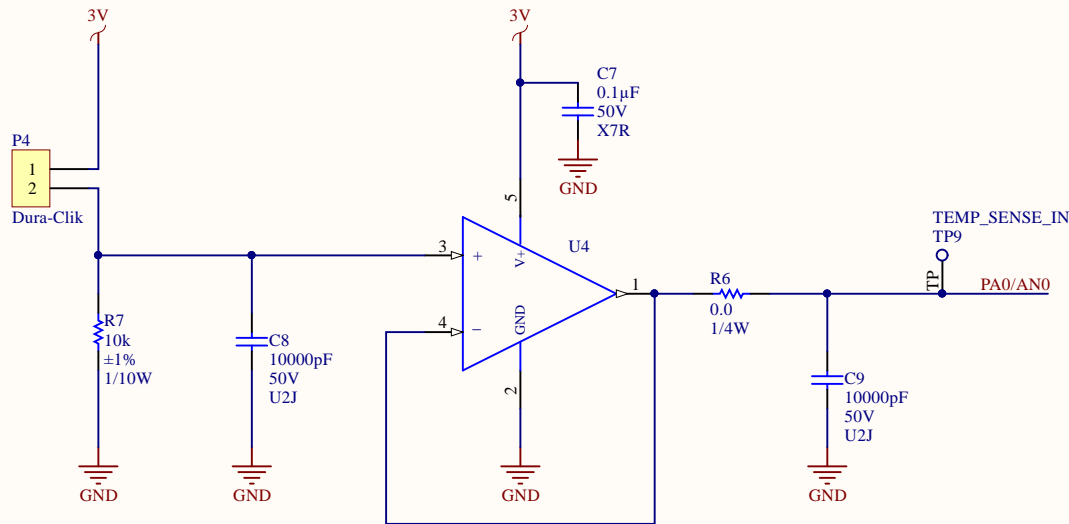


# Power Indicator LED

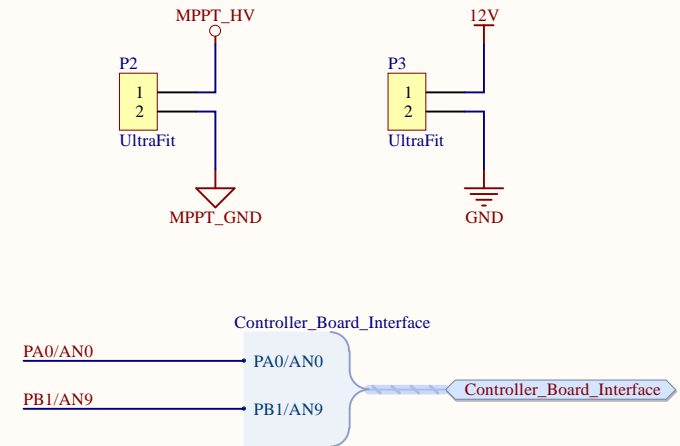


Project: <i>MSXII_SolarSenseSlave.PrjPcb</i>		
Title: <b>Power Supplies</b>		
Project Lead: Peiliang Guo		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.13	
Date: 2018-02-27	Sheet3 of 4	
		Website: <a href="http://www.uwmidsun.com">www.uwmidsun.com</a>

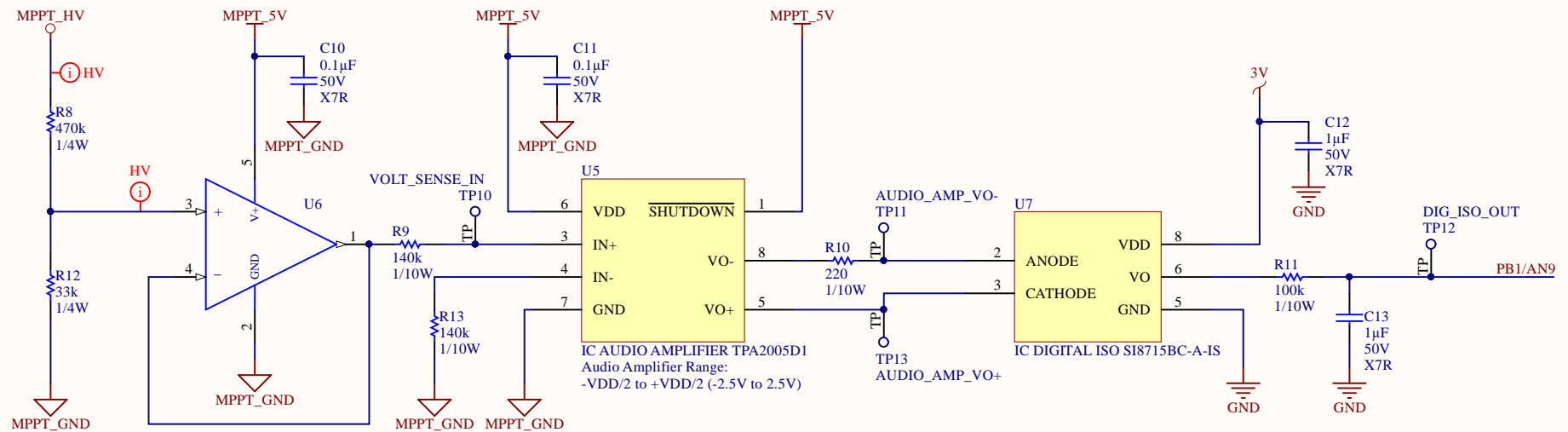
## Temperature Sense




## Connectors



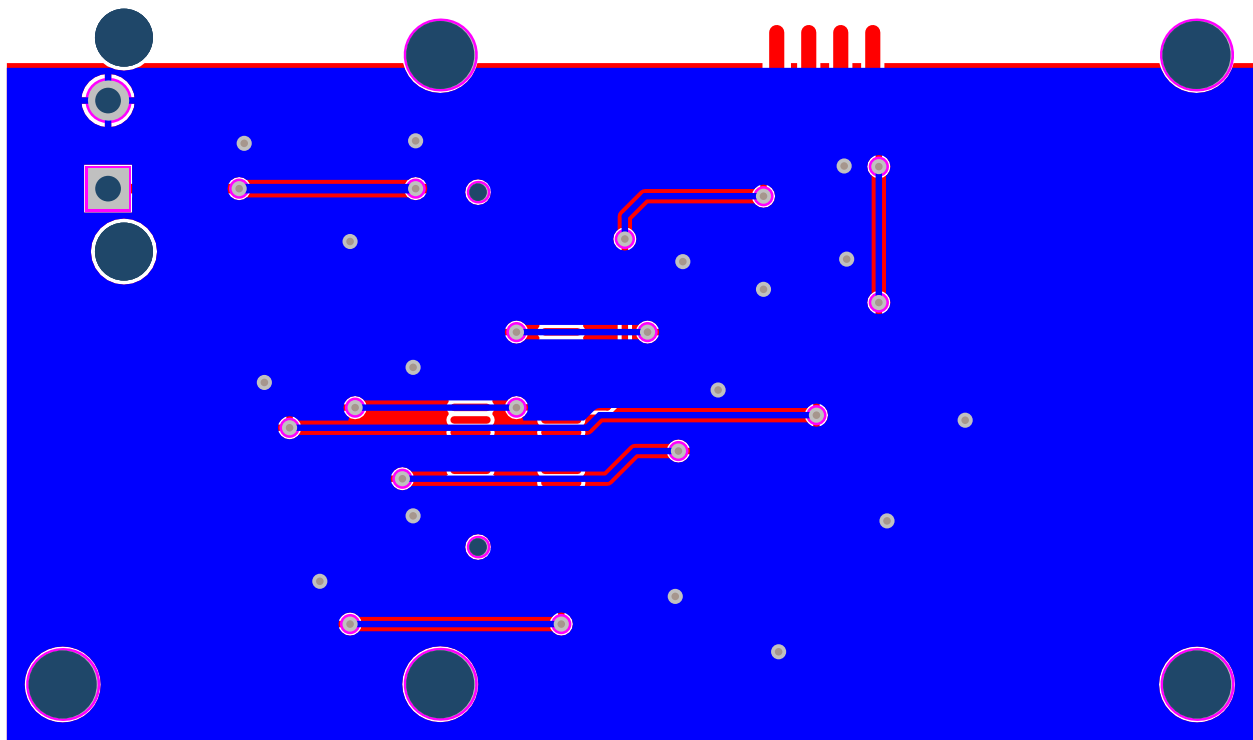
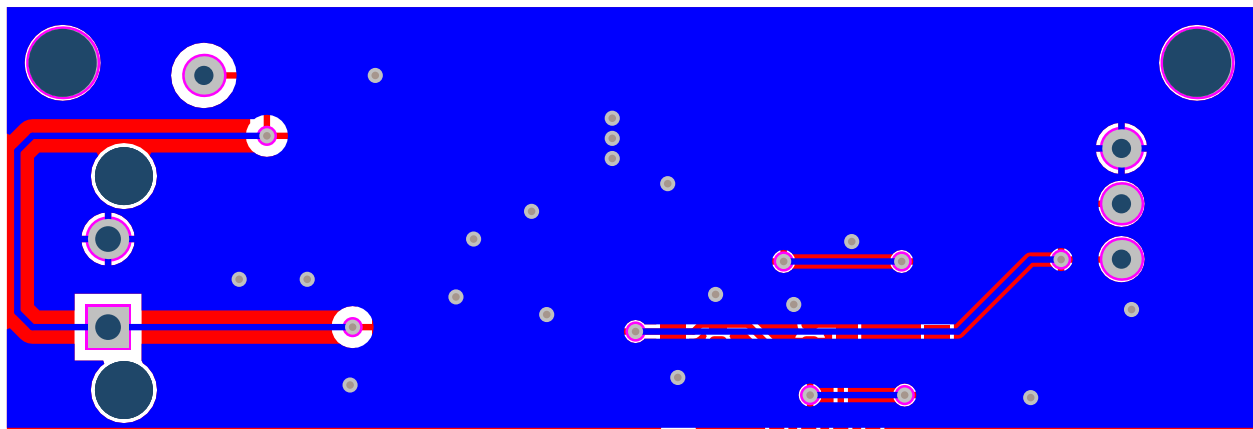
## Voltage Sense

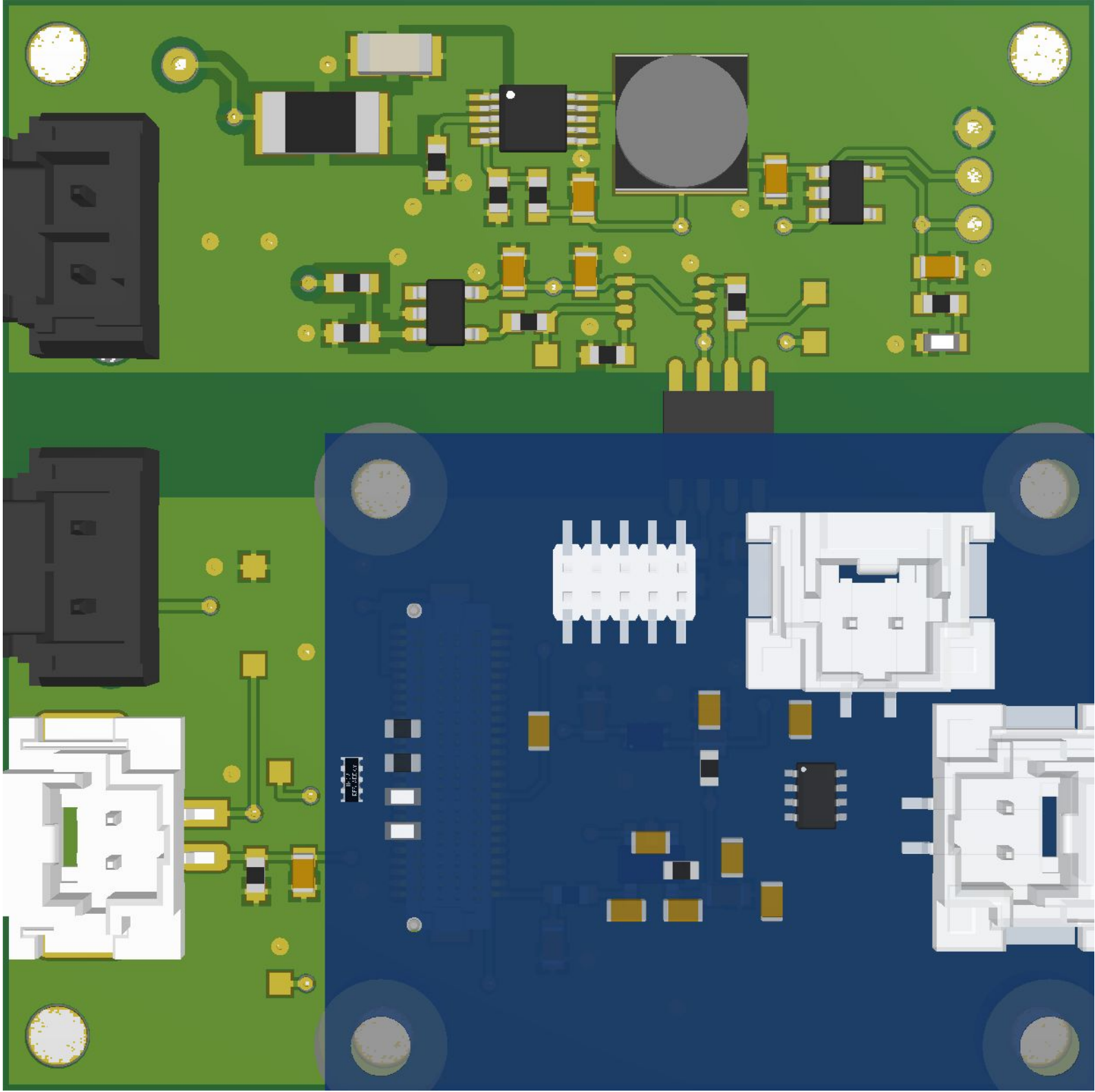


Project: <i>MSXII_SolarSenseSlave.PrjPcb</i>		 MIDNIGHT SUN
Title: <b>Solar Sense Slave</b>		
Project Lead: Peiliang Guo		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.13	
Date: 2018-02-27	Sheet4 of 4	
		Website: <a href="http://www.uwmidsun.com">www.uwmidsun.com</a>











## Electrical Rules Check Report

Class	Document	Message
Warning	SolarSenseBoard.SchDoc	Net NetC8_1 has no driving source (Pin C8-1,Pin P4-2,Pin R7-1,Pin U4-3)
Warning	SolarSenseBoard.SchDoc	Net NetR8_2 has no driving source (Pin R8-2,Pin R12-1,Pin U6-3)

## Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII\_SolarSenseSlave\SolarSenseSlave.sch Warnings 0  
Rule Violations 6

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=20.866mil) (InNetClass('HV')), (InNet('MPPT_GND'))	0
Clearance Constraint (Gap=6mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( (All) )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=6mil) (Max=100mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect )(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Minimum Annular Ring (Minimum=5.906mil) (All)	0
Hole Size Constraint (Min=11.811mil) (Max=248.031mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=11.811mil) (Disabled)(All),(All)	0
Silk To Solder Mask (Clearance=7mil) (IsPad),(All)	6
Silk to Silk (Clearance=10mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Total	6

Silk To Solder Mask (Clearance=7mil) (IsPad),(All)	
Silk To Solder Mask Clearance Constraint: (6.688mil < 7mil) Between Pad P4-3(142.52mil,641.732mil) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (4.921mil < 7mil) Between Pad U2-1(1474.409mil,1655.512mil) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (4.921mil < 7mil) Between Pad U2-2(1474.409mil,1618.11mil) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (4.921mil < 7mil) Between Pad U2-3(1474.409mil,1580.709mil) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (4.921mil < 7mil) Between Pad U2-4(1564.961mil,1580.709mil) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (4.921mil < 7mil) Between Pad U2-5(1564.961mil,1655.512mil) on Top Layer And Track	