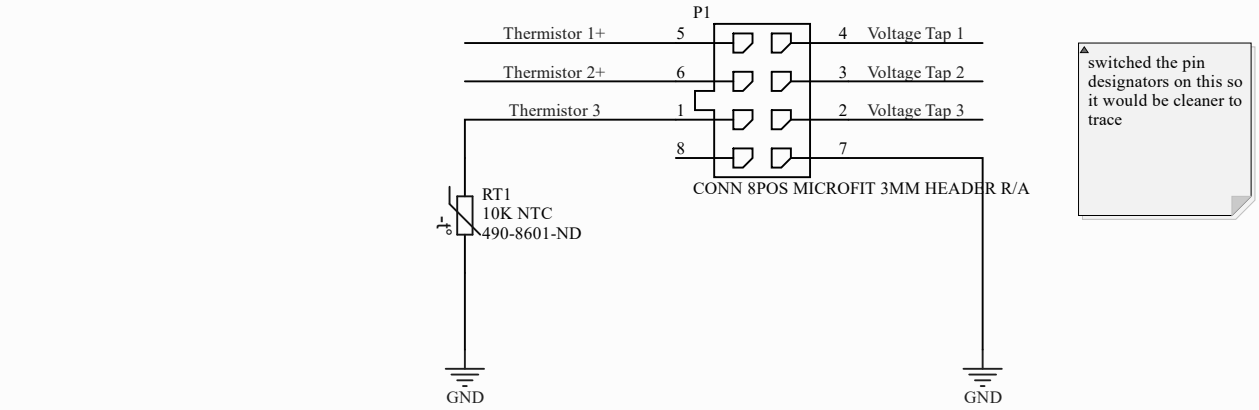
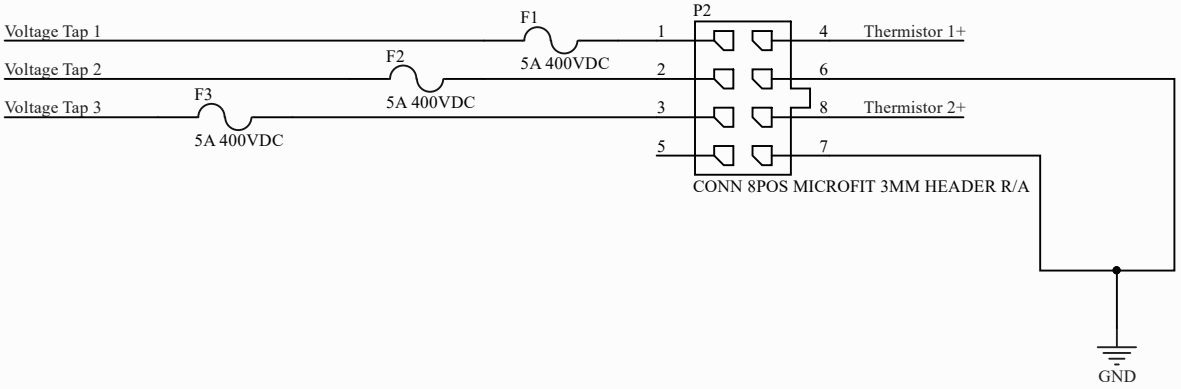
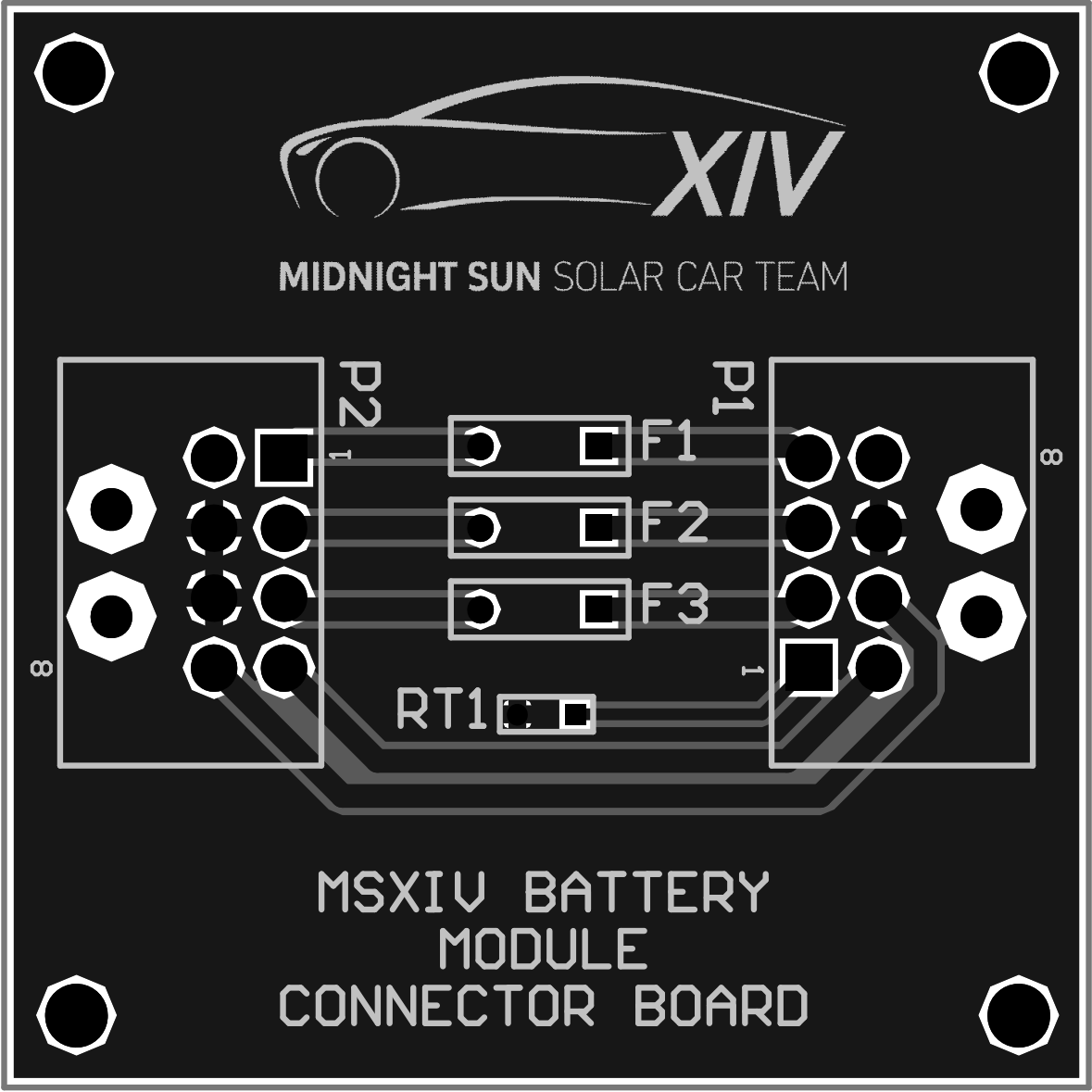
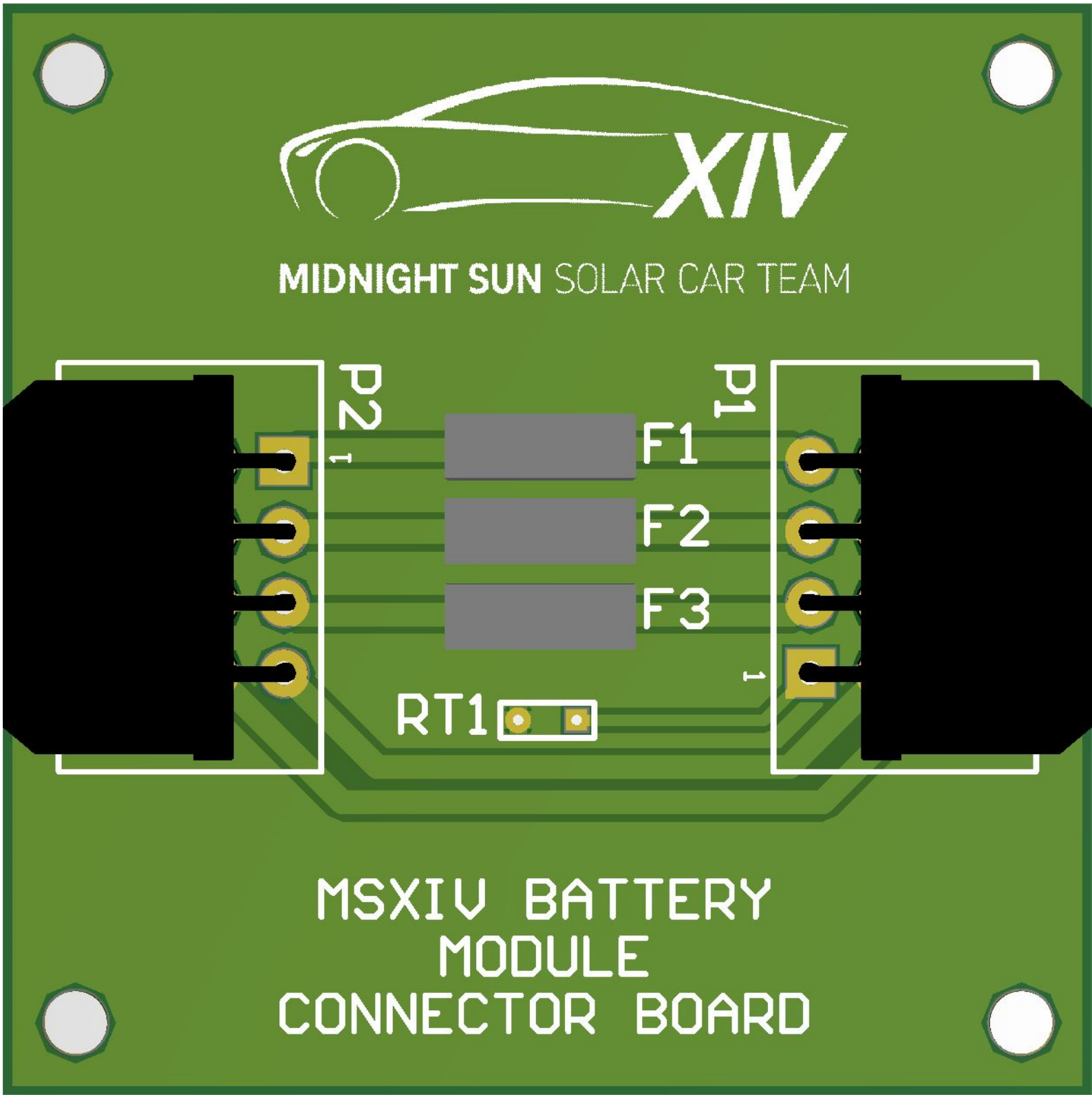




Project: MSXIV_BatteryModuleConnectorBoard.PrjPcb		MIDNIGHT SUN
Title: *		
Project Author: Aashmika Mali		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.0	
Date: 2019-09-15	Sheet* of *	Website: uwmidsun.com

Comment	Description	Designator	Footprint	LibRef	Qu
5A 400VDC	FUSE BOARD MNT 5A	F1, F2, F3	FUSE 5A 400VDC RAI	FUSE 5A 125VAC/400	
CONN 8POS MICROFI	Connector Header Thr	P1, P2	CONN, 8POS R/A MIC	CONN 8POS MICROFI	
10K NTC	NTC Thermistor 10k B	RT1	NTC THERMISTOR BE	NTC THERMISTOR 10	


XIV
MIDNIGHT SUN SOLAR CAR TEAM
P2
P1
F1
F2
F3
RT1
1
8
8
1
MSXIV BATTERY
MODULE
CONNECTOR BOARD


XIV
MIDNIGHT SUN SOLAR CAR TEAM
J2
1
J1
F1
F2
F3
RT1
1
MSXIV BATTERY
MODULE
CONNECTOR BOARD

Electrical Rules Check Report

Class	Document	Message
Warning	MSXIV_BatteryModuleConnectorBoard.SchDoc	Off grid Net Label Thermistor 1+ at 5980.115mil,4500mil
Warning	MSXIV_BatteryModuleConnectorBoard.SchDoc	Off grid Net Label Thermistor 2+ at 5980.115mil,4100mil
Warning	MSXIV_BatteryModuleConnectorBoard.SchDoc	Off grid Net Label Thermistor 3 at 4131.041mil,6900mil

Design Rules Verification Report

Filename : C:\Users\Aashmika Mali\Documents\First Year\Midnight Sun\hardware\MSXIV_BatteryModuleConnectorBoard\MSXIV_BatteryModu

Warnings 0
Rule Violations 18

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=100mil) (Preferred=10mil) (All)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	8
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	6
Silk to Silk (Clearance=10mil) (All),(All)	4
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	18

Hole Size Constraint (Min=1mil) (Max=100mil) (All)
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(0mil,0mil) on Multi-Layer Actual Hole Size = 106.299mil
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(0mil,1594.488mil) on Multi-Layer Actual Hole Size = 106.299mil
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(1590.551mil,1594.488mil) on Multi-Layer Actual Hole Size = 106.299mil
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(1590.551mil,3.937mil) on Multi-Layer Actual Hole Size = 106.299mil
Hole Size Constraint: (122.047mil > 100mil) Pad P1-(736.221mil,1531.496mil) on Multi-Layer Actual Hole Size = 122.047mil
Hole Size Constraint: (122.047mil > 100mil) Pad P1-(917.323mil,1531.496mil) on Multi-Layer Actual Hole Size = 122.047mil
Hole Size Constraint: (122.047mil > 100mil) Pad P2-(736.221mil,62.992mil) on Multi-Layer Actual Hole Size = 122.047mil
Hole Size Constraint: (122.047mil > 100mil) Pad P2-(917.323mil,62.992mil) on Multi-Layer Actual Hole Size = 122.047mil

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1082.677mil,846.457mil) on Multi-Layer And Track (1053.15mil,718.504mil)(1053.15mil,875.984mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1082.677mil,846.457mil) on Multi-Layer And Track (1053.15mil,875.984mil)(1112.205mil,875.984mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1082.677mil,846.457mil) on Multi-Layer And Track (1112.205mil,718.504mil)(1112.205mil,875.984mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.941mil < 10mil) Between Pad RT1-2(1082.677mil,748.032mil) on Multi-Layer And Track (1053.15mil,718.504mil)(1053.15mil,875.984mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (8.833mil < 10mil) Between Pad RT1-2(1082.677mil,748.032mil) on Multi-Layer And Track (1053.15mil,718.504mil)(1112.205mil,718.504mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.941mil < 10mil) Between Pad RT1-2(1082.677mil,748.032mil) on Multi-Layer And Track (1112.205mil,718.504mil)(1112.205mil,875.984mil) on Top Overlay [Top Overlay] to [Top

Silk to Silk (Clearance=10mil) (All),(All)
Silk To Silk Clearance Constraint: (7.806mil < 10mil) Between Text "1" (1003.937mil,1129.921mil) on Top Overlay And Track (484.252mil,1177.165mil)(1169.291mil,1177.165mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (7.806mil < 10mil) Between Text "1" (649.606mil,464.567mil) on Top Overlay And Track (484.252mil,417.323mil)(1169.291mil,417.323mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "8" (1015.748mil,-39.37mil) on Top Overlay And Track (484.252mil,-23.622mil)(1169.291mil,-23.622mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "8" (637.795mil,1633.858mil) on Top Overlay And Track (484.252mil,1618.11mil)(1169.291mil,1618.11mil) on Top Overlay Silk Text to Silk Clearance