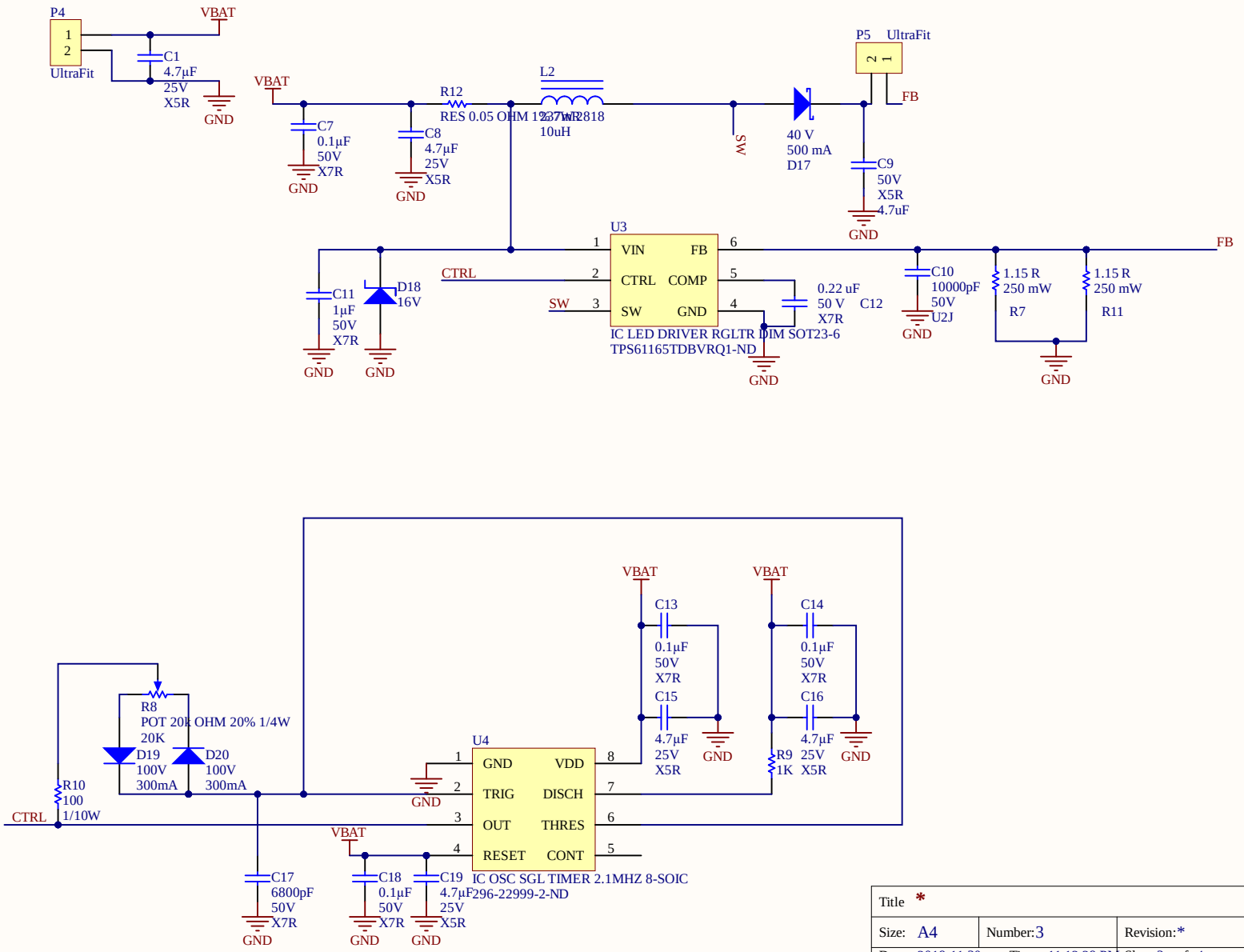

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Size: A4	Number: 3	Revision: *	
Date: 2019-11-30	Time: 11:12:29 PM	Sheet 3 of 4	
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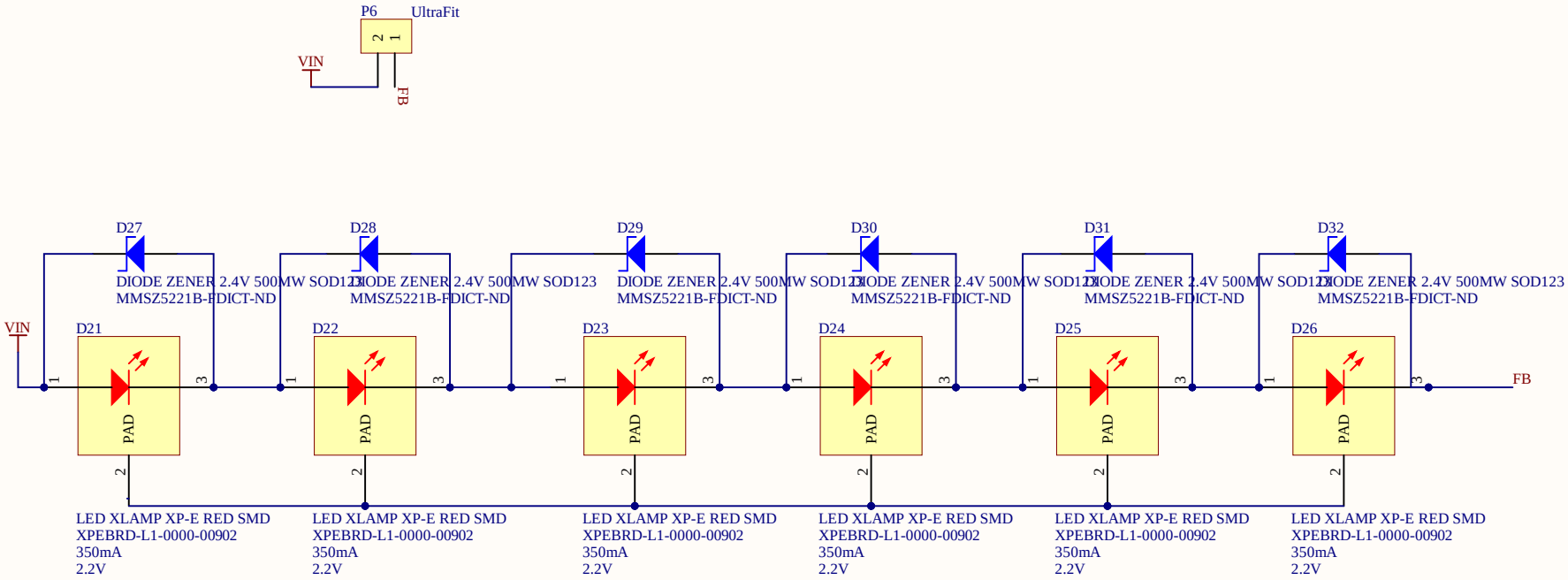

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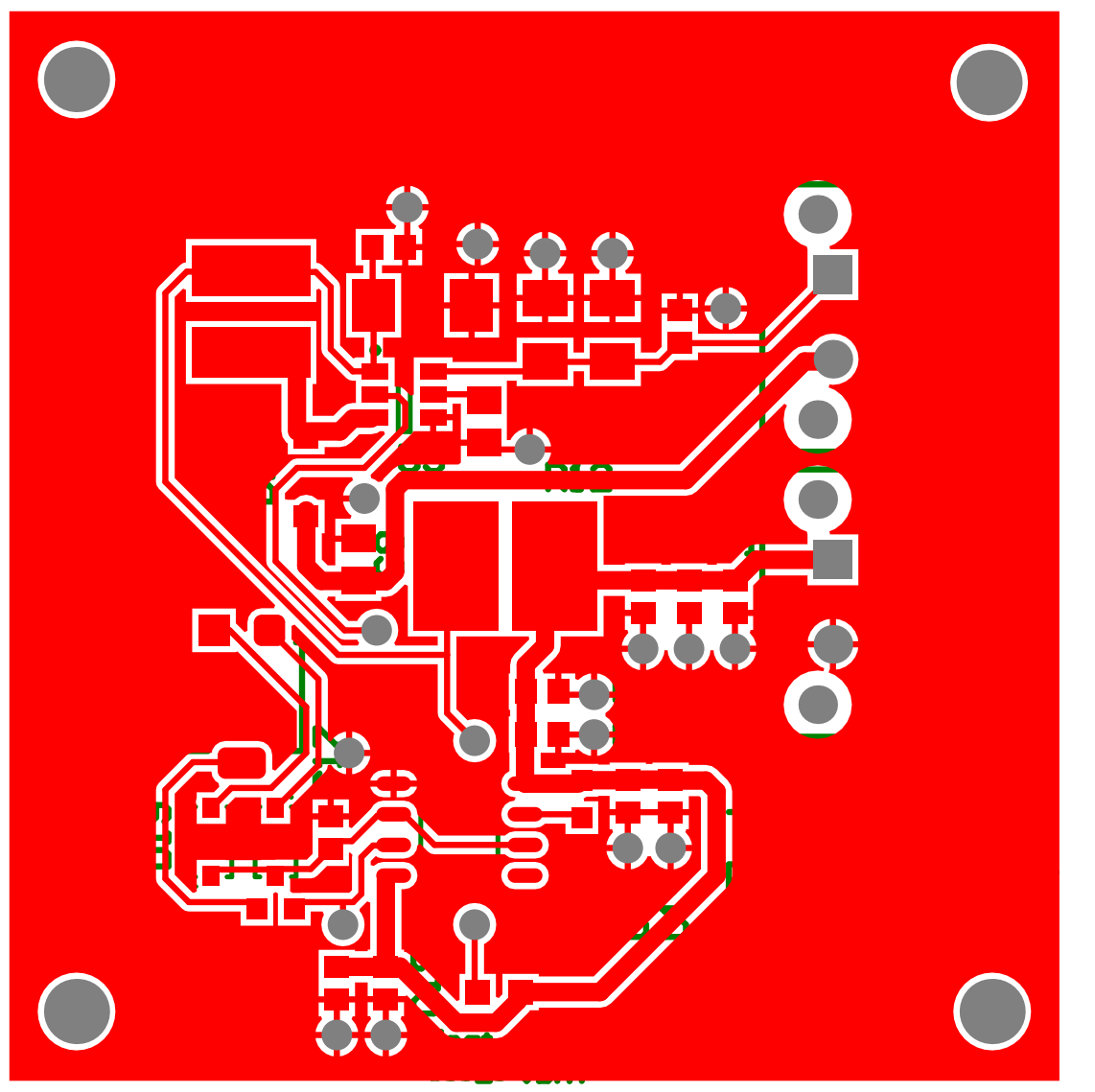
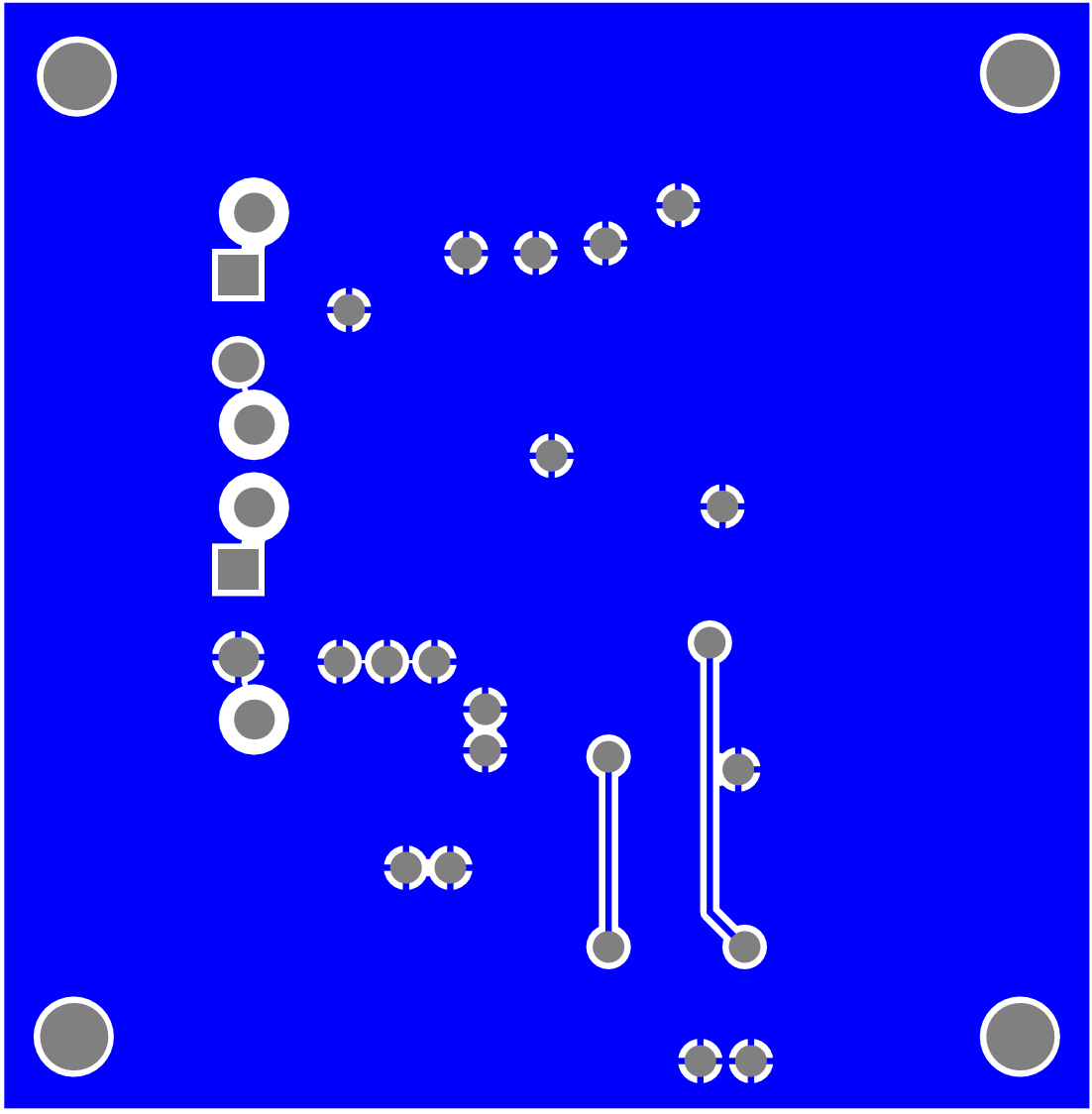
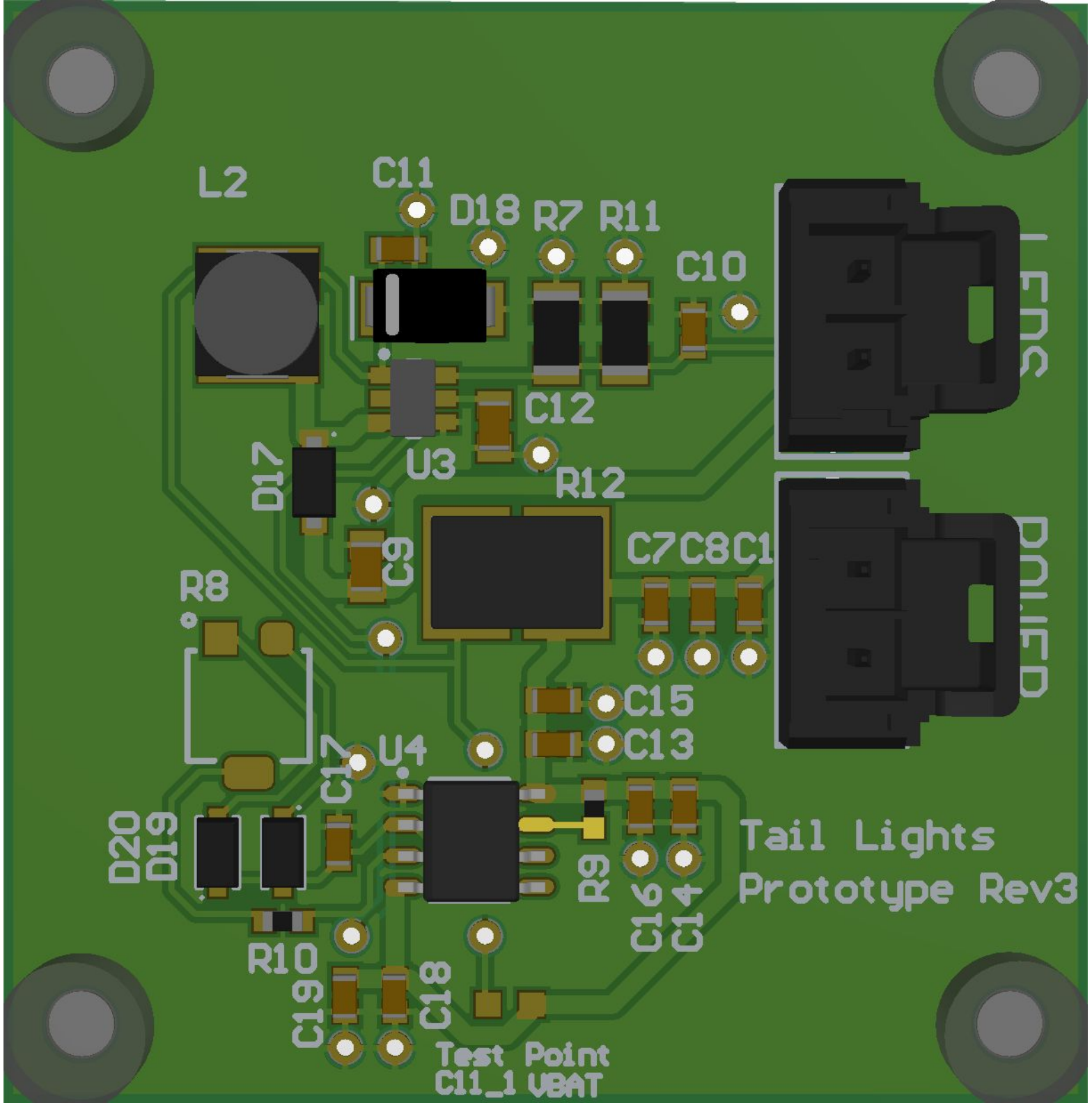
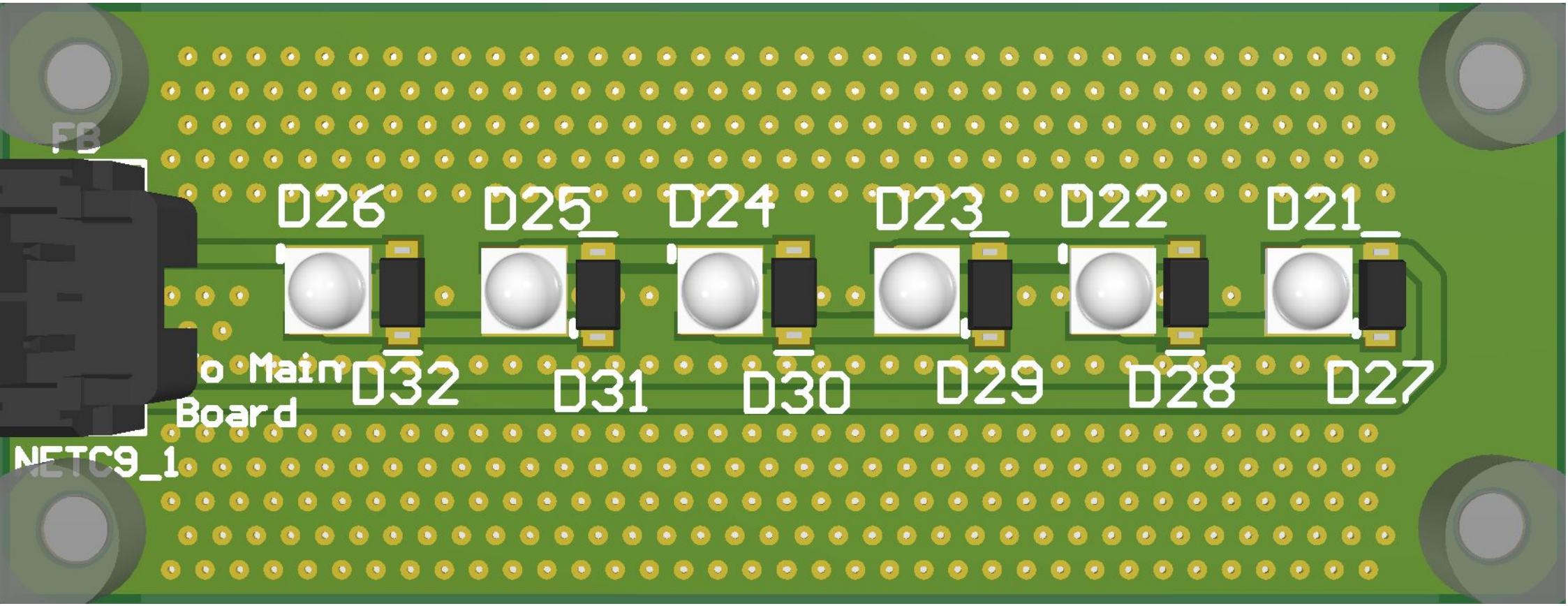
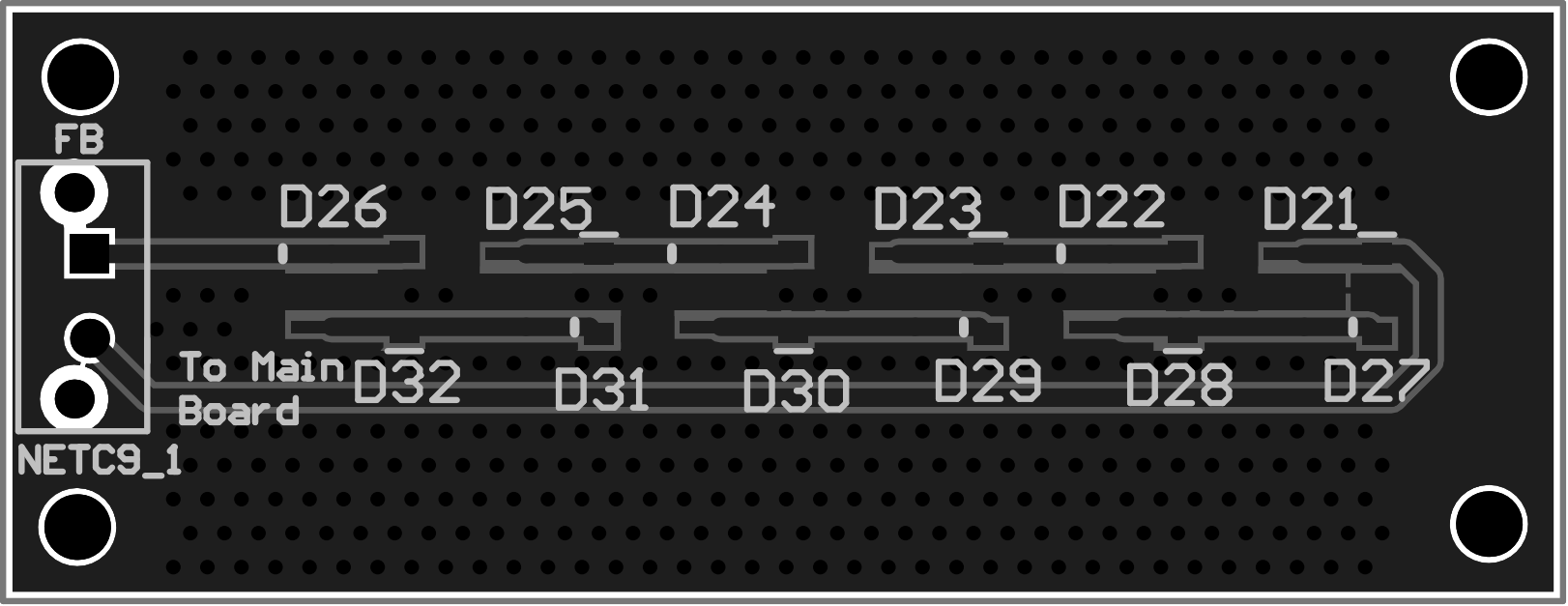
Date: 11-30-2019	Sheet of	
File: C:\Users\..\TailLightPrototypeRev3LEDs.SchDoc	Drawn By:	






L2
C11
D18
R7
R11
C10
LEDS
C12
U3
D17
R12
C9
C7
C8
C1
R8
POWER
C15
C13
U4
C17
D20
D19
R9
C16
C14
Tail Lights
Prototype Rev3
R10
C19
C18
Test Point
C11_1
VBAT


FB
D26
D25_
D24
D23_
D22
D21_
o Main
Board
D32
D31
D30
D29
D28
D27
NETC9_1


FB
D26
D25_
D24
D23_
D22
D21_
To Main
Board
D32
D31
D30
D29
D28
D27
NETC9_1

Comment	Description	Designator	Footprint	LibRef	Quantity
CAP CER 4.7UF 25V 10% X5R 0603	4.7µF ±10% 25V Ceramic Capacitor X5R 0603 (1608 Metric)	C1, C8, C15, C16, C19	CAP, 0603	CAP CER 4.7UF 25V 10% X5R 0603	5
CAP CER 0.1UF 50V 10% X7R 0603	0.10µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C7, C13, C14, C18	CAP, 0603	CAP CER 0.1UF 50V 10% X7R 0603	4
CAP CER 4.7UF 50V 10% X5R 0805	4.7µF ±20% 50V Ceramic Capacitor X5R 0805 (2012 Metric)	C9	CAP, 0805	CAP CER 4.7UF 50V 10% X5R 0805	1
CAP CER 10nF 50V 5% X7R 0603	10000pF ±5% 50V Ceramic Capacitor U2J 0603 (1608 Metric)	C10	CAP, 0603	CAP CER 10nF 50V 5% X7R 0603	1
CAP CER 1UF 50V 10% X7R 0603	1µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C11	CAP, 0603	CAP CER 1UF 50V 10% X7R 0603	1
CAP CER 0.22UF 50V X7R 0805		C12	CAP, 0805	CAP CER 0.22UF 50V X7R 0805	1
CAP CER 6800pF 50V 10% X7R 0603	6800pF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C17	CAP, 0603	CAP CER 6800pF 50V 10% X7R 0603	1
DIODE SCHOTTKY 40V 500MA SOD123	Diode Schottky 40V 500mA Surface Mount SOD-123	D17	SOD123	DIODE SCHOTTKY 40V 500MA SOD123	1
DIODE ZENER 16V 5W DO-214AA (SMB)	Zener Diode 16V 5W ±5% Surface Mount DO-214AA (SMB)	D18	DO-214AA Diode	DIODE ZENER 16V 5W DO-214AA (SMB)	1
DIODE GEN PURP 100V 300MA SOD123	Diode Standard 100V 300mA (DC) Surface Mount SOD-123	D19, D20	DIODE GEN PURP 100V 300MA SOD123	DIODE GEN PURP 100V 300MA SOD123	2
LED XLAMP XP-E RED SMD	LED Lighting Color XLamp® XP-E2 Red 623nm (620nm ~ 625nm) 1414 (3535 Metric)	D21, D22, D23, D24, D25, D26	LED CREE XP-E2 1414 2-SMD	LED XLAMP XP-E RED SMD	6
DIODE ZENER 2.4V 500MW SOD123	Zener Diode 2.4V 500mW ±5% Surface Mount SOD-123	D27, D28, D29, D30, D31, D32	DIODE SOD123	DIODE ZENER 2.4V 500MW SOD123	6
FIXED IND 10UH 1.13A 237 MOHM	10µH Shielded Wirewound Inductor 1.13A 237mOhm Max Nonstandard	L2	INDP5050X20N	FIXED IND 10UH 1.13A 237 MOHM	1
CONN 2POS ULTRA-FIT 0.138"	Connector Header Through Hole 2 position 0.138" (3.50mm), 2 Positions Header, Shrouded Connector 0.138" (3.50mm) Through Hole Gold	P4, P5, P6	CONN, 2POS ULTRA-FIT	CONN 2POS ULTRA-FIT 0.138"	3
RES SMD 1.15 OHM 1% 1/4W 1206		R7, R11	RES 1206	RES SMD 1.15 OHM 1% 1/4W 1206	2
POT 20k OHM 20% 1/4W	20k Ohm 0.25W, 1/4W Gull Wing Surface Mount Trimmer Potentiometer	R8	20K POT	POT 20k OHM 20% 1/4W	1
1K	1k Ohm ±5% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric)	R9	RES, 0603	RES 1K OHM 5% 1/10W 0603	1
RES 100 OHM 1% 1/10W 0603	100 Ohm ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	R10	RES, 0603	RES 100 OHM 1% 1/10W 0603	1
RES 0.05 OHM 1% 7W 2818	50 mOhms ±1% 7W Chip Resistor Nonstandard Automotive AEC-Q200, Current Sense, Moisture Resistant, Pulse Withstanding Metal Element	R12	RES 2818	RES 0.05 OHM 1% 7W 2818	1
IC LED DRIVER RGLTR DIM SOT23-6	LED Driver IC 1 Output DC DC Regulator Step-Up (Boost) PWM Dimming 1.2A (Switch) SOT-23-6	U3	SOT23-6_N	IC LED DRIVER RGLTR DIM SOT23-6	1
IC OSC SGL TIMER 2.1MHZ 8-SOIC	555 Type, Timer/Oscillator (Single) IC 2.1MHz 8-SOIC	U4	SOIC8	IC OSC SGL TIMER 2.1MHZ 8-SOIC	1

Design Rules Verification Report

Filename : C:\Users\Midnight Sun\Documents\Midnight Sun\hardware\MSXIV_TailLights

Warnings 0
Rule Violations 38

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=30mil) (Preferred=10mil) (All)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	4
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	15
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	14
Silk to Silk (Clearance=10mil) (All),(All)	5
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	38

Hole Size Constraint (Min=1mil) (Max=100mil) (All)
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(125mil,138.329mil) on Multi-Layer Actual Hole Size = 106.299mil
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(125mil,1658.329mil) on Multi-Layer Actual Hole Size = 106.299mil
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(1615mil,1653.329mil) on Multi-Layer Actual Hole Size = 106.299mil
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(1620mil,138.329mil) on Multi-Layer Actual Hole Size = 106.299mil

Minimum Solder Mask Sliver (Gap=10mil) (All),(All)
Minimum Solder Mask Sliver Constraint: (8.709mil < 10mil) Between Pad C1-2(1200mil,788.425mil) on Top Layer And Via (1200mil,730mil) from Top
Minimum Solder Mask Sliver Constraint: (8.709mil < 10mil) Between Pad C13-1(911.575mil,590mil) on Top Layer And Via (970mil,590mil) from Top
Minimum Solder Mask Sliver Constraint: (8.709mil < 10mil) Between Pad C14-1(1095mil,463.425mil) on Top Layer And Via (1095mil,405mil) from
Minimum Solder Mask Sliver Constraint: (8.709mil < 10mil) Between Pad C15-1(911.575mil,660mil) on Top Layer And Via (970mil,655mil) from Top
Minimum Solder Mask Sliver Constraint: (8.709mil < 10mil) Between Pad C16-1(1025mil,463.425mil) on Top Layer And Via (1025mil,405mil) from
Minimum Solder Mask Sliver Constraint: (8.709mil < 10mil) Between Pad C18-2(630mil,158.425mil) on Top Layer And Via (630mil,100mil) from Top
Minimum Solder Mask Sliver Constraint: (8.354mil < 10mil) Between Pad C19-2(550mil,158.071mil) on Top Layer And Via (550mil,100mil) from Top
Minimum Solder Mask Sliver Constraint: (8.709mil < 10mil) Between Pad C7-2(1050mil,788.425mil) on Top Layer And Via (1050mil,730mil) from Top
Minimum Solder Mask Sliver Constraint: (8.709mil < 10mil) Between Pad C8-2(1125mil,788.425mil) on Top Layer And Via (1125mil,730mil) from Top
Minimum Solder Mask Sliver Constraint: (9.913mil < 10mil) Between Pad C9-2(585mil,909.449mil) on Top Layer And Via (595mil,975mil) from Top
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U3-1(612.756mil,1182.402mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U3-2(612.756mil,1145mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U3-4(707.244mil,1107.599mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U3-5(707.244mil,1145mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (7mil < 10mil) Between Via (970mil,590mil) from Top Layer to Bottom Layer And Via (970mil,655mil) from

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (8.037mil < 10mil) Between Arc (319.409mil,342.165mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (8.037mil < 10mil) Between Arc (475.591mil,487.835mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Arc (531.89mil,1087.756mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad C9-1(585mil,840.551mil) on Top Layer And Text "C9" (655mil,850mil) on
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad C9-2(585mil,909.449mil) on Top Layer And Text "C9" (655mil,850mil) on
Silk To Solder Mask Clearance Constraint: (9.724mil < 10mil) Between Pad D18-2(610mil,1290mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad D19-1(450mil,470.118mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad D19-1(450mil,470.118mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad D19-2(450mil,359.882mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad D19-2(450mil,359.882mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad D20-1(345mil,359.882mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad D20-1(345mil,359.882mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad D20-2(345mil,470.118mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad D20-2(345mil,470.118mil) on Top Layer And Track

Silk to Silk (Clearance=10mil) (All),(All)
Silk To Silk Clearance Constraint: (6.021mil < 10mil) Between Arc (642.716mil,543.465mil) on Top Overlay And Text "U4" (610mil,560mil) on Top
Silk To Silk Clearance Constraint: (8.355mil < 10mil) Between Text "C1" (1180mil,885mil) on Top Overlay And Text "C8" (1095mil,885mil) on Top
Silk To Silk Clearance Constraint: (1.33mil < 10mil) Between Text "C1" (1180mil,885mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (5.01mil < 10mil) Between Text "C11_1" (700mil,30mil) on Top Overlay And Text "Test Point" (700mil,75mil) on
Silk To Silk Clearance Constraint: (8.355mil < 10mil) Between Text "C7" (1010mil,885mil) on Top Overlay And Text "C8" (1095mil,885mil) on Top

Design Rules Verification Report

Filename : C:\Users\Midnight Sun\Documents\Midnight Sun\hardware\MSXIV_TailLights

Warnings 0
Rule Violations 25

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.762mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	4
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	1
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	15
Silk to Silk (Clearance=0.254mm) (All),(All)	5
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	25

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(3.048mm,3.048mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(3.175mm,21.59mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(61.087mm,21.59mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(61.087mm,3.175mm) on Multi-Layer Actual Hole Size = 2.7mm

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D25-2(21.5mm,12.8mm) on Top Layer And Via (23.8mm,12.6mm)

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D21-3(53.5mm,11.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D22-3(45.5mm,14.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D23-3(37.5mm,11.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D24-3(29.5mm,14.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D25-3(21.5mm,11.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D26-3(13.5mm,14.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.218mm < 0.254mm) Between Pad D27-1(56.5mm,14.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.19mm < 0.254mm) Between Pad D27-2(56.5mm,11.02mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.218mm < 0.254mm) Between Pad D28-1(48.5mm,11.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.218mm < 0.254mm) Between Pad D29-1(40.5mm,14.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.19mm < 0.254mm) Between Pad D29-2(40.5mm,11.02mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.218mm < 0.254mm) Between Pad D30-1(32.5mm,11.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.218mm < 0.254mm) Between Pad D31-1(24.5mm,14.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.19mm < 0.254mm) Between Pad D31-2(24.5mm,11.02mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.218mm < 0.254mm) Between Pad D32-1(16.5mm,11.1mm) on Top Layer And Track

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.151mm < 0.254mm) Between Text "D21" (51.994mm,15.418mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.064mm < 0.254mm) Between Text "D23" (35.992mm,15.418mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.064mm < 0.254mm) Between Text "D25" (19.99mm,15.418mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.238mm < 0.254mm) Between Text "D32" (14.595mm,8.284mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.216mm < 0.254mm) Between Text "FB" (2.286mm,18.542mm) on Top Overlay And Track