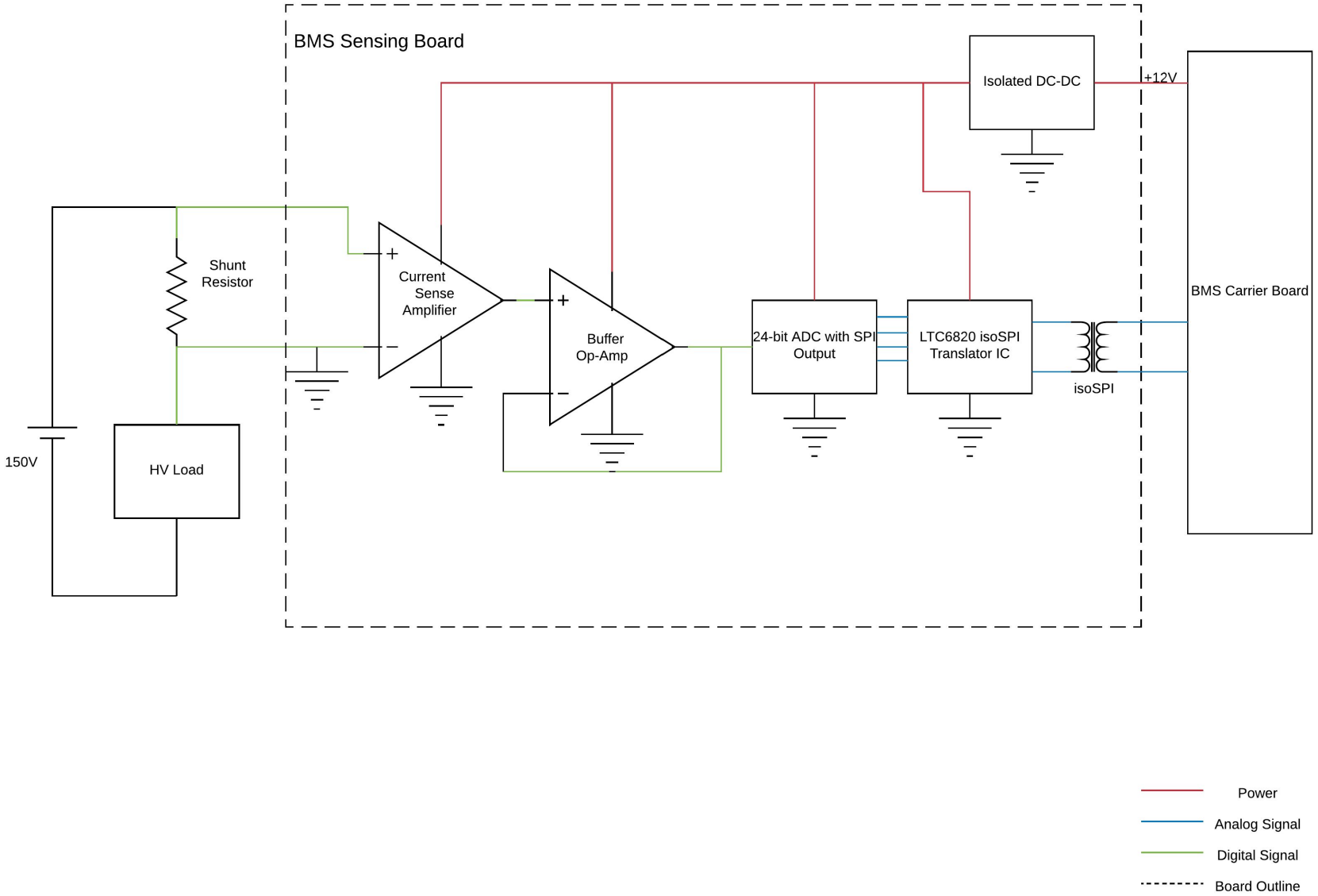
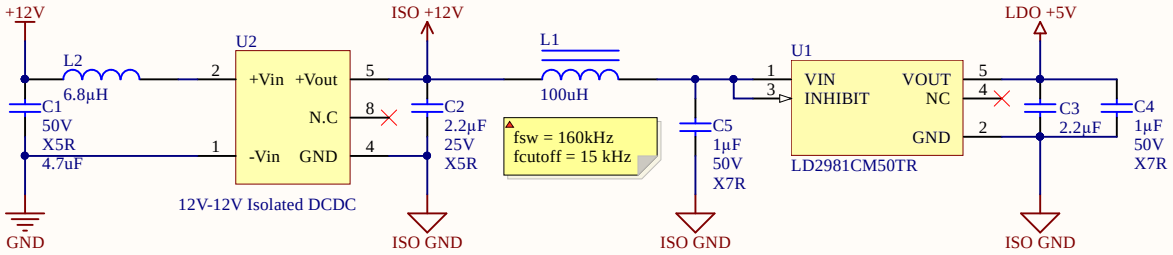
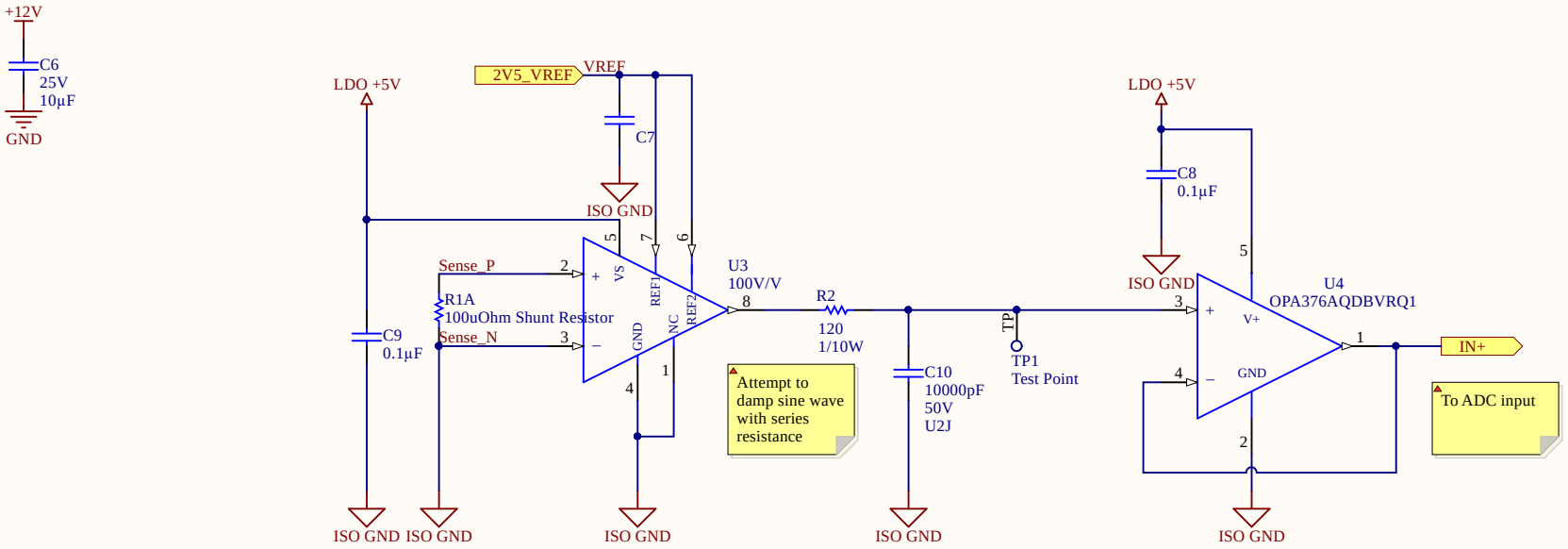


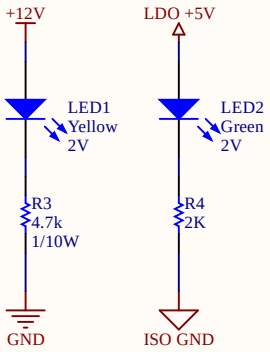

Last Updated: Oct 29, 2017

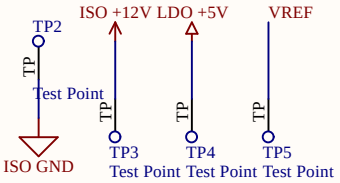
| | | |
|---|---|---|
| Project: ***BMS_Current_Sense.PrjPcb*** | | MIDNIGHT SUN |
| Title: **BMS Current Sense Block Diagram** | | |
| Project Lead: Liam Hawkins | | University of Waterloo<br>200 University Ave W<br>Waterloo, ON, Canada<br>N2L 3E9 |
| Size: Letter | Revision: 1.0 | |
| Date: 2019-09-14 | Sheet 1 of 3 | Website: www.uwmidsun.com |



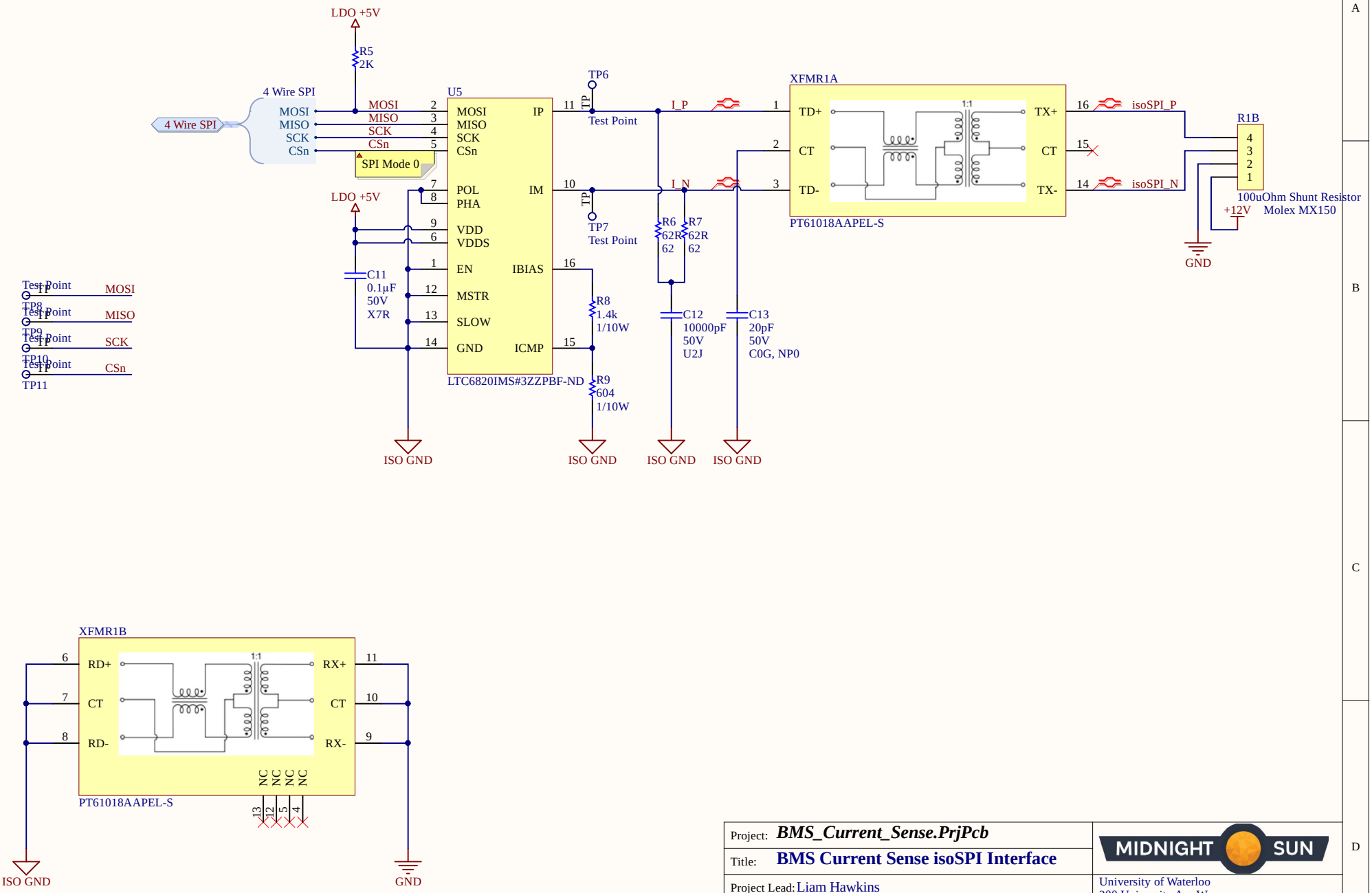




Using the internal resistor divider (Fig 29 of INA240 Datasheet, Oct 2016) to get the mid voltage point of the 4.096V reference. Isense = 0 when Vout = Vref/2




| | | |
|---|---|---|
| Project: ***BMS_Current_Sense.PrjPcb*** | | MIDNIGHT SUN |
| Title: **BMS Current Sense Board** | | |
| Project Lead: Liam Hawkins | | University of Waterloo<br>200 University Ave W<br>Waterloo, ON, Canada<br>N2L 3E9 |
| Size: Letter | Revision: 1.0 | |
| Date: 2019-09-14 | Sheet 2 of 3 | Website: www.uwmidsun.com |




| | | |
|---|---|---|
| Project: ***BMS_Current_Sense.PrjPcb*** | | MIDNIGHT SUN |
| Title: **BMS Current Sense isoSPI Interface** | | |
| Project Lead: Liam Hawkins | | University of Waterloo<br>200 University Ave W<br>Waterloo, ON, Canada<br>N2L 3E9 |
| Size: Letter | Revision: 1.0 | |
| Date: 2019-09-14 | Sheet 3 of 3 | Website: www.uwmidsun.com |

**RESET/PWDN Pin**

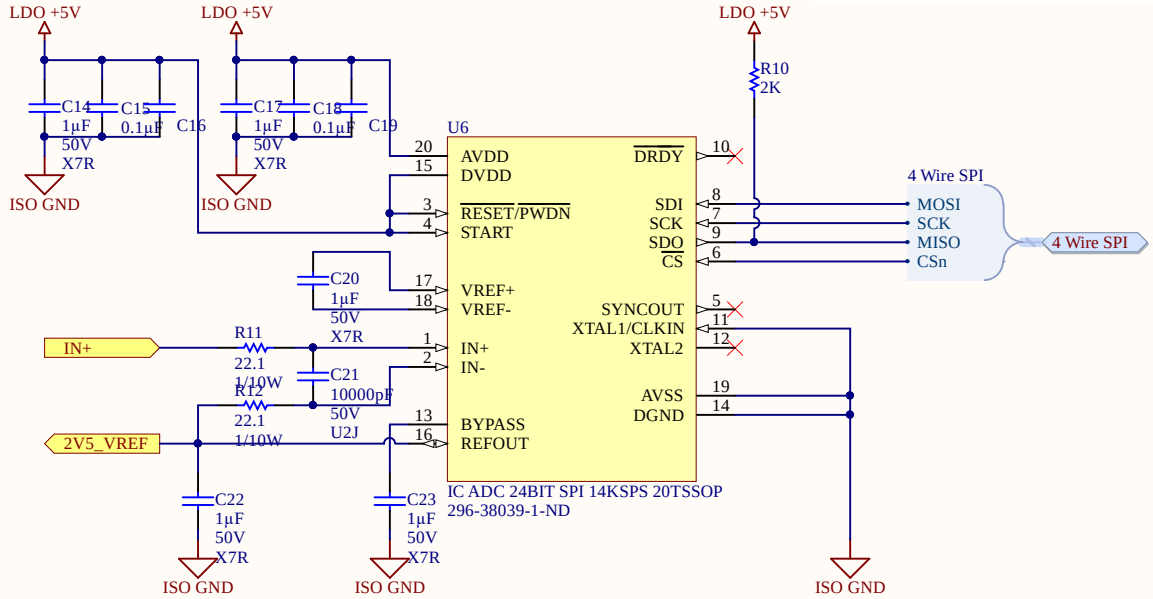
This pin must be high in normal operation. If it is desired to completely power down the device, or to have a hardware reset control, then connect this pin to a controller. If these functions are not needed, tie the pin high. (Note that the device can both be reset and SLEEP mode engaged by commands.)

**START Pin**

If it is desired to control conversions by pin, connect this line to the controller. Otherwise, this line can be tied high to free-run conversions. The conversions can also be controlled by software commands. In this case, tie the START pin low.

**DRDY Pin**

DRDY is an output that indicates when data are ready for readback. Note that the DOUT pin (and also the DRDY register bit) indicates when data are ready as well, so DRDY connection to a controller is optional.

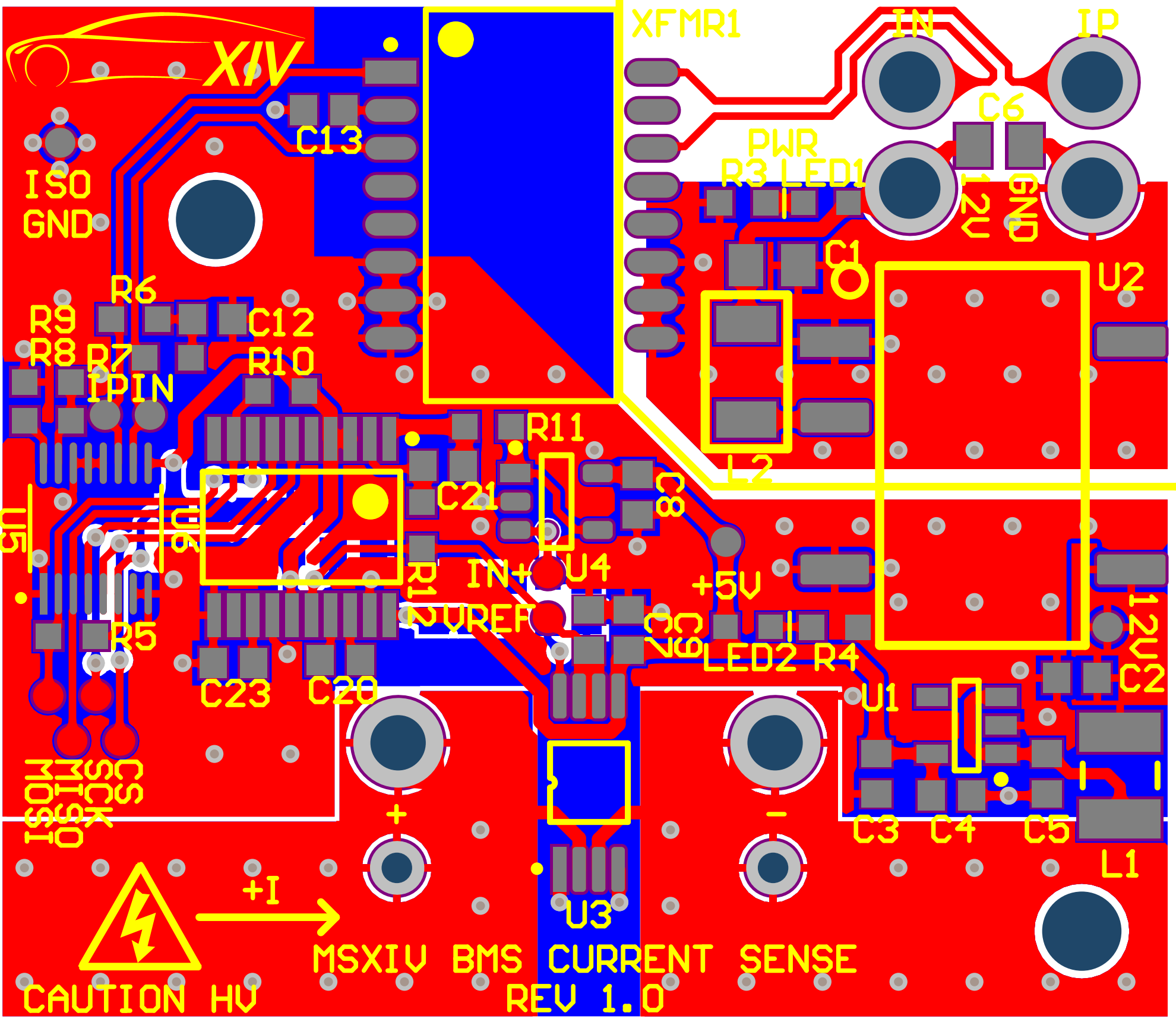


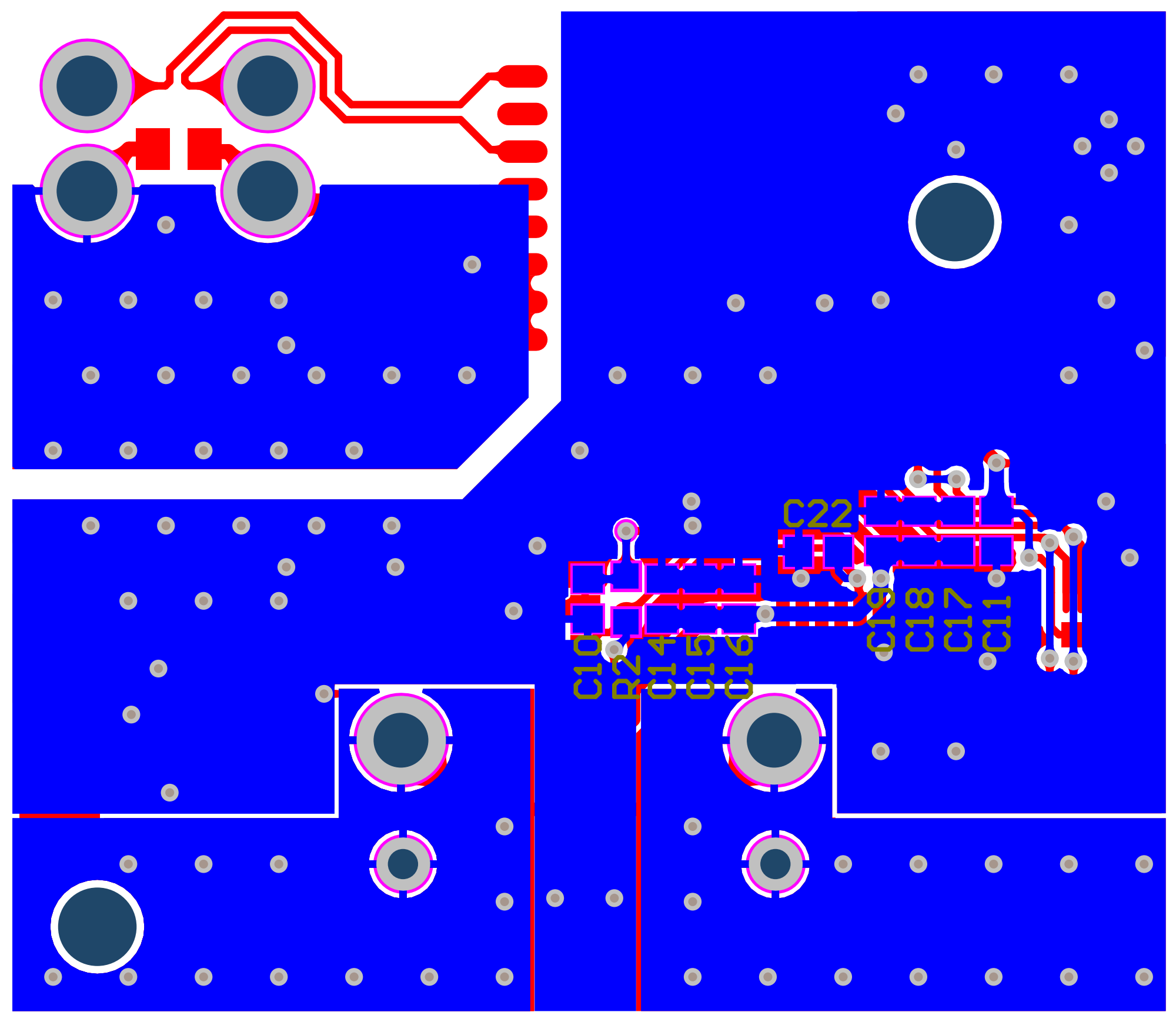

| | | |
|---|---|---|
| Title | | |
| Size: A | Number: | Revision: |
| Date: 2019-09-14 | | Sheet of |
| File: C:\Users\..\ADC_Circuit.SchDoc | | Drawn By: |

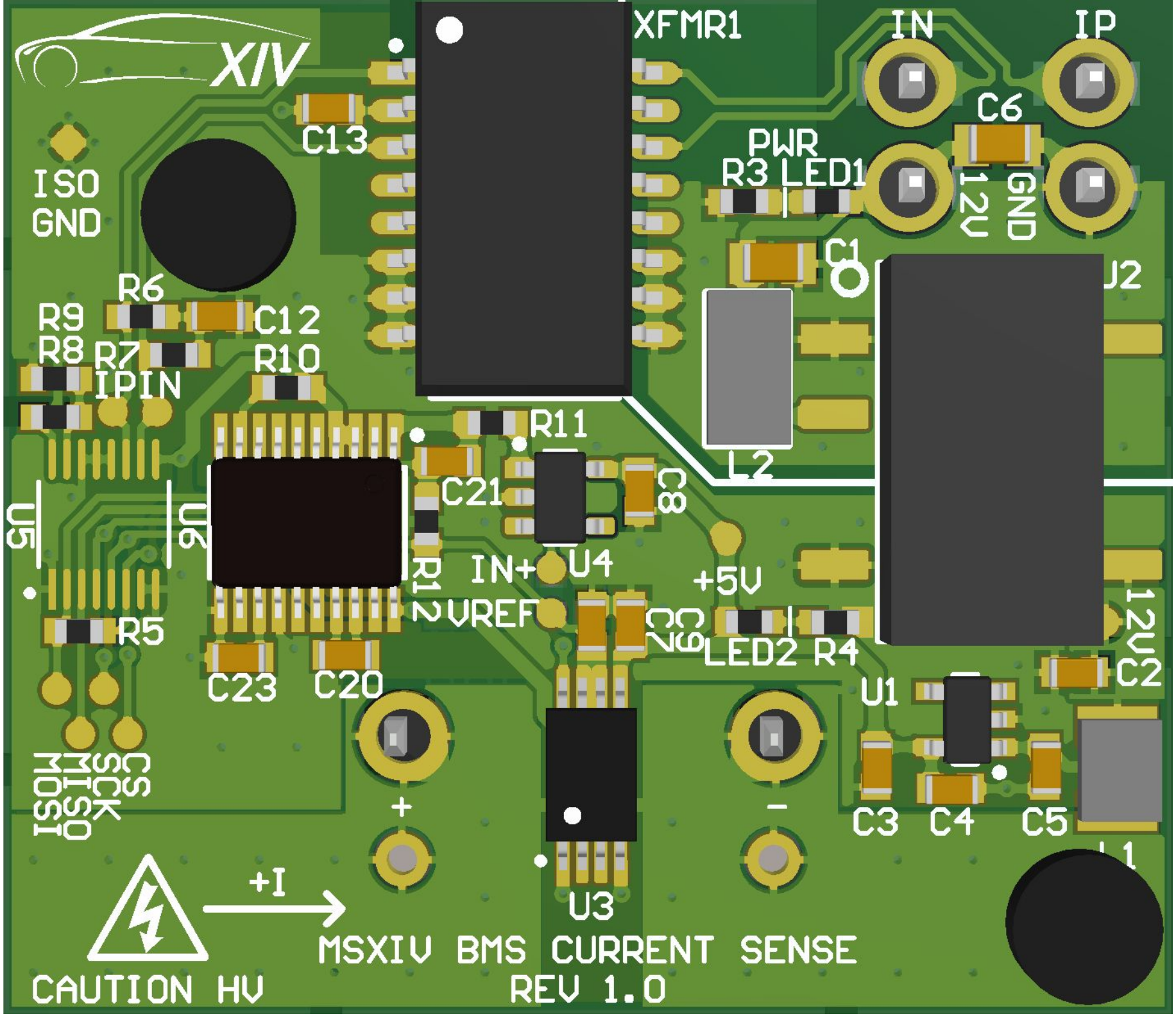
# Bill of Materials

| | |
|---|---|
| Project: | BMS_Current_Sense.PrjPcb |
| Revision: | 1.0 |
| Project Lead: | Liam Hawkins |
| Generated On: | 2019-09-14 12:21 PM |
| Production Quantity: | 1 |
| Currency | CAD |
| Total Parts Count: | 46 |

| LibRef | Designator | Manufacturer 1 | Manufacturer Part Number 1 | Supplier 1 | Supplier Part Number 1 | Supplier Unit Price 1 | Quantity | Supplier Subtotal 1 |
|---|---|---|---|---|---|---|---|---|
| CAP CER 4.7UF 50V 10% X5R 0805 | C1 | Murata | GRT21BR61H475ME13L | Digi-Key | 490-12395-1-ND | 0.58385 | 1 | $ 0.58 |
| CAP CER 2.2UF 25V 10% X5R 0603 | C2 | Murata | GRM188R61E225KA12D | Digi-Key | 490-10731-1-ND | 0.22558 | 1 | $ 0.23 |
| CAP CER 2.2UF 25V 10% X5R 0603 | C3 | Murata | GRM188R61E225KA12D | Digi-Key | 490-10731-1-ND | 0.22558 | 1 | $ 0.23 |
| CAP CER 1UF 50V 10% X7R 0603 | C4 | Taiyo Yuden | UMK107AB7105KA-T | Digi-Key | 587-3247-1-ND | 0.33173 | 1 | $ 0.33 |
| CAP CER 1UF 50V 10% X7R 0603 | C5 | Taiyo Yuden | UMK107AB7105KA-T | Digi-Key | 587-3247-1-ND | 0.33173 | 1 | $ 0.33 |
| CAP CER 10uF 25V 10% X5R 0805 | C6 | Murata | GRM21BR61E106KA73L | Digi-Key | 490-5523-1-ND | 0.57058 | 1 | $ 0.57 |
| CAP CER 0.022UF 50V 10% X7R 0603 | C7 | Murata | GRM188R71H223KA01D | Digi-Key | 490-1517-1-ND | | 1 | |
| CAP CER 0.1UF 50V 10% X7R 0603 | C8 | Kyocera AVX | 06035C104KAT2A | Digi-Key | 478-5052-1-ND | 0.19904 | 1 | $ 0.20 |
| CAP CER 0.1UF 50V 10% X7R 0603 | C9 | Kyocera AVX | 06035C104KAT2A | Digi-Key | 478-5052-1-ND | 0.19904 | 1 | $ 0.20 |
| CAP CER 10nF 50V 5% X7R 0603 | C10 | KEMET | C0603C103J5JACTU | Digi-Key | 399-13384-1-ND | 0.43789 | 1 | $ 0.44 |
| CAP CER 0.1UF 50V 10% X7R 0603 | C11 | Kyocera AVX | 06035C104KAT2A | Digi-Key | 478-5052-1-ND | 0.19904 | 1 | $ 0.20 |
| CAP CER 10nF 50V 5% X7R 0603 | C12 | KEMET | C0603C103J5JACTU | Digi-Key | 399-13384-1-ND | 0.43789 | 1 | $ 0.44 |
| CAP CER 20PF 50V ±5% C0G/NP0 0603 | C13 | Murata | GRM1885C1H200JA01D | Digi-Key | 490-1410-1-ND | 0.13269 | 1 | $ 0.13 |
| CAP CER 1UF 50V 10% X7R 0603 | C14 | Taiyo Yuden | UMK107AB7105KA-T | Digi-Key | 587-3247-1-ND | 0.33173 | 1 | $ 0.33 |
| CAP CER 0.1UF 50V 10% X7R 0603 | C15 | Kyocera AVX | 06035C104KAT2A | Digi-Key | 478-5052-1-ND | 0.19904 | 1 | $ 0.20 |
| CAP CER 0.022UF 50V 10% X7R 0603 | C16 | Murata | GRM188R71H223KA01D | Digi-Key | 490-1517-1-ND | | 1 | |
| CAP CER 1UF 50V 10% X7R 0603 | C17 | Taiyo Yuden | UMK107AB7105KA-T | Digi-Key | 587-3247-1-ND | 0.33173 | 1 | $ 0.33 |
| CAP CER 0.1UF 50V 10% X7R 0603 | C18 | Kyocera AVX | 06035C104KAT2A | Digi-Key | 478-5052-1-ND | 0.19904 | 1 | $ 0.20 |
| CAP CER 0.022UF 50V 10% X7R 0603 | C19 | Murata | GRM188R71H223KA01D | Digi-Key | 490-1517-1-ND | | 1 | |
| CAP CER 1UF 50V 10% X7R 0603 | C20 | Taiyo Yuden | UMK107AB7105KA-T | Digi-Key | 587-3247-1-ND | 0.33173 | 1 | $ 0.33 |
| CAP CER 10nF 50V 5% X7R 0603 | C21 | KEMET | C0603C103J5JACTU | Digi-Key | 399-13384-1-ND | 0.43789 | 1 | $ 0.44 |
| CAP CER 1UF 50V 10% X7R 0603 | C22 | Taiyo Yuden | UMK107AB7105KA-T | Digi-Key | 587-3247-1-ND | 0.33173 | 1 | $ 0.33 |
| CAP CER 1UF 50V 10% X7R 0603 | C23 | Taiyo Yuden | UMK107AB7105KA-T | Digi-Key | 587-3247-1-ND | 0.33173 | 1 | $ 0.33 |
| IND 100uH 60mA 5% 1210 | L1 | TDK EPCOS | B82422T1104J000 | Digi-Key | 495-5646-1-ND | 0.79616 | 1 | $ 0.80 |
| IND 6.8uH 260mA 20% 1210 | L2 | TDK | NLFV32T-6R8M-EF | Digi-Key | 445-15776-1-ND | 0.58385 | 1 | $ 0.58 |
| LED YELLOW CLEAR 2.1V 0603 | LED1 | Wurth Electronics | 150060YS75000 | Digi-Key | 732-4981-1-ND | 0.18577 | 1 | $ 0.19 |
| LED GREEN CLEAR 2V 0603 | LED2 | Wurth Electronics | 150060VS75000 | Digi-Key | 732-4980-1-ND | 0.18577 | 1 | $ 0.19 |
| RES SHUNT 100UOHM 5% 3W 60MM | R1 | Vishay Dale | WSBM8518L1000JK | Digi-Key | 541-1906-ND | 38.39 | 1 | $ 38.39 |
| RES 120 OHM 1% 1/10W 0603 | R2 | Yageo | RC0603FR-07120RL | Digi-Key | 311-120HRCT-ND | 0.13269 | 1 | $ 0.13 |
| RES 4.7K OHM 1% 1/10W 0603 | R3 | Yageo Phycomp | RC0603FR-074K7L | Digi-Key | 311-4.70KHRCT-ND | 0.13269 | 1 | $ 0.13 |
| RES 2K OHM 1% 1/10W 0603 | R4 | Yageo | RC0603FR-072KL | Digi-Key | 311-2.00KHRCT-ND | 0.13269 | 1 | $ 0.13 |
| RES 2K OHM 1% 1/10W 0603 | R5 | Yageo | RC0603FR-072KL | Digi-Key | 311-2.00KHRCT-ND | 0.13269 | 1 | $ 0.13 |
| RES 62 OHM 0.1% 1/10W 0603 | R6 | Panasonic | ERA3AEB620V | Digi-Key | P62DBCT-ND | 0.46443 | 1 | $ 0.46 |
| RES 62 OHM 0.1% 1/10W 0603 | R7 | Panasonic | ERA3AEB620V | Digi-Key | P62DBCT-ND | 0.46443 | 1 | $ 0.46 |
| RES 1.4k OHM 1% 1/10W 0603 | R8 | Yageo | RC0603FR-071K4L | Digi-Key | 311-1.40KHRCT-ND | 0.13269 | 1 | $ 0.13 |
| RES 604 OHM 1% 1/10W 0603 | R9 | Yageo | RC0603FR-07604RL | Digi-Key | 311-604HRCT-ND | 0.13269 | 1 | $ 0.13 |
| RES 2K OHM 1% 1/10W 0603 | R10 | Yageo | RC0603FR-072KL | Digi-Key | 311-2.00KHRCT-ND | 0.13269 | 1 | $ 0.13 |
| RES 22.1 OHM 1% 1/10W 0603 | R11 | Yageo | RC0603FR-0722R1L | Digi-Key | 311-22.1HRCT-ND | 0.13269 | 1 | $ 0.13 |
| RES 22.1 OHM 1% 1/10W 0603 | R12 | Yageo | RC0603FR-0722R1L | Digi-Key | 311-22.1HRCT-ND | 0.13269 | 1 | $ 0.13 |
| IC REG LDO 5V 0.1A SOT23-5 | U1 | STMicroelectronics | LD2981CM50TR | Digi-Key | 497-7787-1-ND | 0.8625 | 1 | $ 0.86 |
| IC DCDC ISOLATED 12V 1W 8-SMD 5-LEAD | U2 | XP Power | ISE1212A-TR | Digi-Key | 1470-2950-1-ND | 5.64 | 1 | $ 5.64 |
| IC CURRENT AMP LIFIER INA240 8-TSSOP | U3 | Texas Instruments | INA240A3PWR | Digi-Key | 296-45090-1-ND | 3.52 | 1 | $ 3.52 |
| C OP AMP GEN PURPOSE RR 5.5MHZ SOT-23-5 | U4 | Texas Instruments | OPA376AQDBVRQ1 | Digi-Key | 296-36701-1-ND | 2.84 | 1 | $ 2.84 |
| ISOSPI COMM INTERFACE LTC6820IMS#3ZZP | U5 | Analog Devices / Linear | LTC6820IMS#3ZZPBF | Digi-Key | LTC6820IMS#3ZZPBF-ND | 8.01 | 1 | $ 8.01 |
| IC ADC 24BIT SPI 14KSPS 20TSSOP | U6 | Texas Instruments | ADS1259QPWRQ1 | Digi-Key | 296-38039-1-ND | 16.69 | 1 | $ 16.69 |
| IC PULSE XFMR 1CT:1CT 350UH SMD | XFMR1 | Bourns | PT61018AAPEL-S | Digi-Key | PT61018AAPEL-SCT-ND | 5.08 | 1 | $ 5.08 |
| | | | | | | | Total: | $ 91.28 |


XIV
XFMR1
IN
IP
C6
PWR
R3 LED1
12V
GND
C13
ISO
GND
C1
U2
R6
R9
R8
R7
IPIN
C12
R10
R11
L2
C21
C8
U5
U6
R12
IN+
U4
+5V
VREF
C7
C9
LED2 R4
12V
C2
R5
C23
C20
U1
MOSI
MISO
SCK
CS
+
-
C3
C4
C5
L1
+I
U3
MSXIV BMS CURRENT SENSE
REV 1.0
CAUTION HV


C22
C10
R2
C14
C15
C16
C19
C18
C17
C11


XIV
XFMR1
IN
IP
C6
C13
PWR
R3 LED1
12V
GND
ISO
GND
C1
U2
R6
R9
C12
R8
R7
R10
IPIN
R11
L2
C21
C8
U5
U6
R12
IN+
U4
+5V
VREF
C7
C9
LED2
R4
12V
R5
C23
C20
U1
C2
MOSI
MISO
SCK
CS
+
-
C3
C4
C5
L1
+I
U3
MSXIV BMS CURRENT SENSE
REV 1.0
CAUTION HV

# Electrical Rules Check Report

| Class | Document | Message |
|---|---|---|
| Warning | ADC_Circuit.SchDoc | NetC22_1 contains IO Pin and Output Port objects (Pin U6-16,Port 2V5_VREF) |
| Warning | BMS_Current_Sense.SchDoc | Net NetC10_1 has no driving source (Pin C10-1,Pin R2-2,Pin TP1-TP,Pin U4-3) |
| Warning | ADC_Circuit.SchDoc | Net NetC20_1 has no driving source (Pin C20-1,Pin U6-17) |
| Warning | ADC_Circuit.SchDoc | Net NetC20_2 has no driving source (Pin C20-2,Pin U6-18) |
| Warning | ADC_Circuit.SchDoc | Net NetC21_1 has no driving source (Pin C21-1,Pin R11-2,Pin U6-1) |
| Warning | ADC_Circuit.SchDoc | Net NetC21_2 has no driving source (Pin C21-2,Pin R12-2,Pin U6-2) |
| Warning | BMS_Current_Sense.SchDoc | Net Sense_2_P has no driving source (Pin R1-5,Pin U3-2) |
| Warning | BMS_Current_Sense.SchDoc | Nets Wire Sense_N has multiple names (Net Label Sense_N,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object |
| Warning | ADC_Circuit.SchDoc | Nets Wire Sense_N has multiple names (Net Label Sense_N,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND

# Design Rules Verification Report

Filename : C:\Users\Liam\Documents\UWaterloo\Midnight Sun\Hardware Repository\hardw

Warnings 0
Rule Violations 231

| Warnings | |
|---|---|
| Total | 0 |

| Rule Violations | |
|---|---|
| Clearance Constraint (Gap=0.152mm) (All),(All) | 0 |
| Clearance Constraint (Gap=0.254mm) (InComponent('R1')),(All) | 0 |
| Short-Circuit Constraint (Allowed=No) (All),(All) | 0 |
| Un-Routed Net Constraint ( (All) ) | 0 |
| Modified Polygon (Allow modified: No), (Allow shelved: No) | 0 |
| Width Constraint (Min=0.152mm) (Max=1.27mm) (Preferred=0.254mm) (All) | 0 |
| Power Plane Connect Rule(Relief Connect )(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm) | 0 |
| Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All) | 2 |
| Hole To Hole Clearance (Gap=0.254mm) (All),(All) | 0 |
| Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All) | 71 |
| Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All) | 132 |
| Silk to Silk (Clearance=0.254mm) (All),(All) | 26 |
| Net Antennae (Tolerance=0mm) (All) | 0 |
| Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All) | 0 |
| Total | 231 |

| Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All) |
|---|
| Hole Size Constraint: (2.65mm > 2.54mm) Pad R1-0(36.353mm,3.133mm) on Multi-Layer Actual Hole Size = 2.65mm |
| Hole Size Constraint: (2.65mm > 2.54mm) Pad R1-0(7.403mm,26.933mm) on Multi-Layer Actual Hole Size = 2.65mm |

| Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All) |
| --- |
| Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C10-1(19.8mm,14.875mm) on Bottom Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C10-2(19.8mm,13.525mm) on Bottom Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C11-1(6mm,17.175mm) on Bottom Layer And Pad C17-2(7.3mm,17.175mm) |
| Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C11-2(6mm,15.825mm) on Bottom Layer And Pad C17-1(7.3mm,15.825mm) |
| Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad C12-1(6.625mm,23.6mm) on Top Layer And Pad R6-2(5.475mm,23.6mm) on |
| Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C12-1(6.625mm,23.6mm) on Top Layer And Pad R7-2(6.575mm,22.3mm) on |
| Minimum Solder Mask Sliver Constraint: (0.21mm < 0.254mm) Between Pad C13-1(11.7mm,30.6mm) on Top Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.076mm < 0.254mm) Between Pad C13-1(11.7mm,30.6mm) on Top Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C14-1(17.3mm,13.525mm) on Bottom Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad C14-1(17.3mm,13.525mm) on Bottom Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C14-2(17.3mm,14.875mm) on Bottom Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad C14-2(17.3mm,14.875mm) on Bottom Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C15-1(16mm,13.525mm) on Bottom Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C15-2(16mm,14.875mm) on Bottom Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C17-1(7.3mm,15.825mm) on Bottom Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C17-2(7.3mm,17.175mm) on Bottom Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C18-1(8.6mm,15.825mm) on Bottom Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.148mm < 0.254mm) Between Pad C18-2(8.6mm,17.175mm) on Bottom Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.137mm < 0.254mm) Between Pad C20-1(10.9mm,12.2mm) on Top Layer And Pad U6-15(9.95mm,13.7mm) on |
| Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad C20-1(10.9mm,12.2mm) on Top Layer And Pad U6-16(10.6mm,13.7mm) on |
| Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad C20-1(10.9mm,12.2mm) on Top Layer And Pad U6-17(11.25mm,13.7mm) on |
| Minimum Solder Mask Sliver Constraint: (0.176mm < 0.254mm) Between Pad C20-1(10.9mm,12.2mm) on Top Layer And Pad U6-18(11.9mm,13.7mm) on |
| Minimum Solder Mask Sliver Constraint: (0.176mm < 0.254mm) Between Pad C20-2(12.25mm,12.2mm) on Top Layer And Pad U6-17(11.25mm,13.7mm) |
| Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad C20-2(12.25mm,12.2mm) on Top Layer And Pad U6-18(11.9mm,13.7mm) on |
| Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad C20-2(12.25mm,12.2mm) on Top Layer And Pad U6-19(12.55mm,13.7mm) |
| Minimum Solder Mask Sliver Constraint: (0.137mm < 0.254mm) Between Pad C20-2(12.25mm,12.2mm) on Top Layer And Pad U6-20(13.2mm,13.7mm) on |
| Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C21-1(15.675mm,18.7mm) on Top Layer And Pad R11-2(15.725mm,20mm) |
| Minimum Solder Mask Sliver Constraint: (0.122mm < 0.254mm) Between Pad C21-2(14.325mm,18.7mm) on Top Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C23-1(8.675mm,12.1mm) on Top Layer And Pad U6-12(8mm,13.7mm) on |
| Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C23-1(8.675mm,12.1mm) on Top Layer And Pad U6-13(8.65mm,13.7mm) on |
| Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C23-1(8.675mm,12.1mm) on Top Layer And Pad U6-14(9.3mm,13.7mm) on |
| Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C23-2(7.325mm,12.1mm) on Top Layer And Pad U6-11(7.35mm,13.7mm) on |
| Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad C23-2(7.325mm,12.1mm) on Top Layer And Pad U6-12(8mm,13.7mm) on |
| Minimum Solder Mask Sliver Constraint: (0.067mm < 0.254mm) Between Pad C6-2(34.475mm,29.4mm) on Top Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.159mm < 0.254mm) Between Pad C7-1(19.888mm,12.525mm) on Top Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.242mm < 0.254mm) Between Pad C7-1(19.888mm,12.525mm) on Top Layer And Pad U3-5(20.856mm,11mm) |
| Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad C7-1(19.888mm,12.525mm) on Top Layer And Pad U3-6(20.206mm,11mm) |
| Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad C7-1(19.888mm,12.525mm) on Top Layer And Pad U3-7(19.556mm,11mm) |
| Minimum Solder Mask Sliver Constraint: (0.251mm < 0.254mm) Between Pad C7-1(19.888mm,12.525mm) on Top Layer And Pad U3-8(18.906mm,11mm) |
| Minimum Solder Mask Sliver Constraint: (0.159mm < 0.254mm) Between Pad C7-2(19.888mm,13.875mm) on Top Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.21mm < 0.254mm) Between Pad C7-2(19.888mm,13.875mm) on Top Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad C8-1(21.5mm,18.4mm) on Top Layer And Pad U4-5(20.175mm,18.45mm) on |
| Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad C8-2(21.5mm,17.05mm) on Top Layer And Pad U4-4(20.175mm,16.55mm) |
| Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad C9-1(21.2mm,12.525mm) on Top Layer And Pad U3-5(20.856mm,11mm) on |
| Minimum Solder Mask Sliver Constraint: (0.227mm < 0.254mm) Between Pad IP-TP(3.7mm,20.4mm) on Top Layer And Pad R9-1(2.575mm,21.5mm) on |
| Minimum Solder Mask Sliver Constraint: (0.222mm < 0.254mm) Between Pad LED1-2(27.05mm,27.49mm) on Top Layer And Pad R3-1(25.8mm,27.5mm) |
| Minimum Solder Mask Sliver Constraint: (0.248mm < 0.254mm) Between Pad R10-1(10.375mm,21.2mm) on Top Layer And Pad U6-4(11.25mm,19.6mm) |
| Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-1(10.375mm,21.2mm) on Top Layer And Pad U6-5(10.6mm,19.6mm) on |
| Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-1(10.375mm,21.2mm) on Top Layer And Pad U6-6(9.95mm,19.6mm) on |
| Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-2(8.825mm,21.2mm) on Top Layer And Pad U6-7(9.3mm,19.6mm) on |
| Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-2(8.825mm,21.2mm) on Top Layer And Pad U6-8(8.65mm,19.6mm) on |
| Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-2(8.825mm,21.2mm) on Top Layer And Pad U6-9(8mm,19.6mm) on Top |

| Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All) |
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| Minimum Solder Mask Sliver Constraint: (0.254mm < 0.254mm) Between Pad R5-1(3.375mm,13mm) on Top Layer And Pad U5-3(2.649mm,14.416mm) on |
| Minimum Solder Mask Sliver Constraint: (0.196mm < 0.254mm) Between Pad R5-1(3.375mm,13mm) on Top Layer And Pad U5-4(3.15mm,14.416mm) on |
| Minimum Solder Mask Sliver Constraint: (0.196mm < 0.254mm) Between Pad R5-1(3.375mm,13mm) on Top Layer And Pad U5-5(3.65mm,14.416mm) on |
| Minimum Solder Mask Sliver Constraint: (0.196mm < 0.254mm) Between Pad R5-2(1.825mm,13mm) on Top Layer And Pad U5-1(1.649mm,14.416mm) on |
| Minimum Solder Mask Sliver Constraint: (0.196mm < 0.254mm) Between Pad R5-2(1.825mm,13mm) on Top Layer And Pad U5-2(2.149mm,14.416mm) on |
| Minimum Solder Mask Sliver Constraint: (0.251mm < 0.254mm) Between Pad R6-1(3.925mm,23.6mm) on Top Layer And Pad R7-1(5.025mm,22.3mm) on |
| Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R6-2(5.475mm,23.6mm) on Top Layer And Pad R7-1(5.025mm,22.3mm) on |
| Minimum Solder Mask Sliver Constraint: (0.251mm < 0.254mm) Between Pad R6-2(5.475mm,23.6mm) on Top Layer And Pad R7-2(6.575mm,22.3mm) on |
| Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R8-1(1.025mm,20.2mm) on Top Layer And Pad R9-2(1.025mm,21.5mm) on |
| Minimum Solder Mask Sliver Constraint: (0.211mm < 0.254mm) Between Pad R8-1(1.025mm,20.2mm) on Top Layer And Pad U5-16(1.649mm,18.784mm) |
| Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R8-2(2.575mm,20.2mm) on Top Layer And Pad R9-1(2.575mm,21.5mm) on |
| Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm) Between Pad R8-2(2.575mm,20.2mm) on Top Layer And Pad U5-13(3.15mm,18.784mm) on |
| Minimum Solder Mask Sliver Constraint: (0.196mm < 0.254mm) Between Pad R8-2(2.575mm,20.2mm) on Top Layer And Pad U5-14(2.649mm,18.784mm) |
| Minimum Solder Mask Sliver Constraint: (0.196mm < 0.254mm) Between Pad R8-2(2.575mm,20.2mm) on Top Layer And Pad U5-15(2.149mm,18.784mm) |
| Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U1-1(33.655mm,9.06mm) on Top Layer And Pad U1-2(33.655mm,10.01mm) |
| Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U1-2(33.655mm,10.01mm) on Top Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U4-1(17.425mm,18.45mm) on Top Layer And Pad U4-2(17.425mm,17.5mm) |
| Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U4-2(17.425mm,17.5mm) on Top Layer And Pad U4-3(17.425mm,16.55mm) |
| Minimum Solder Mask Sliver Constraint: (0.079mm < 0.254mm) Between Pad U4-3(17.425mm,16.55mm) on Top Layer And Via (18.5mm,16.5mm) from |

| Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All) |
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| Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Arc (13.975mm,19.6mm) on Top Overlay And Pad C21-2(14.325mm,18.7mm) |
| Silk To Solder Mask Clearance Constraint: (0.139mm < 0.254mm) Between Arc (17.425mm,19.3mm) on Top Overlay And Pad R11-1(17.275mm,20mm) on |
| Silk To Solder Mask Clearance Constraint: (0.101mm < 0.254mm) Between Pad C10-2(19.8mm,13.525mm) on Bottom Layer And Text "C10" |
| Silk To Solder Mask Clearance Constraint: (0.132mm < 0.254mm) Between Pad C1-1(25.125mm,25.4mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.132mm < 0.254mm) Between Pad C1-2(26.875mm,25.4mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.132mm < 0.254mm) Between Pad C1-2(26.875mm,25.4mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad C12-2(7.975mm,23.6mm) on Top Layer And Text "C12" (8.6mm,23.1mm) on |
| Silk To Solder Mask Clearance Constraint: (0.056mm < 0.254mm) Between Pad C13-1(11.7mm,30.6mm) on Top Layer And Text "C13" (10.2mm,29.2mm) |
| Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C13-2(10.35mm,30.6mm) on Top Layer And Text "C13" (10.2mm,29.2mm) |
| Silk To Solder Mask Clearance Constraint: (0.101mm < 0.254mm) Between Pad C14-1(17.3mm,13.525mm) on Bottom Layer And Text "C14" |
| Silk To Solder Mask Clearance Constraint: (0.101mm < 0.254mm) Between Pad C15-1(16mm,13.525mm) on Bottom Layer And Text "C15" |
| Silk To Solder Mask Clearance Constraint: (0.101mm < 0.254mm) Between Pad C16-1(14.7mm,13.525mm) on Bottom Layer And Text "C16" |
| Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C20-1(10.9mm,12.2mm) on Top Layer And Text "C20" (10.6mm,10.8mm) |
| Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C20-2(12.25mm,12.2mm) on Top Layer And Text "C20" (10.6mm,10.8mm) |
| Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C21-1(15.675mm,18.7mm) on Top Layer And Text "C21" |
| Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad C21-2(14.325mm,18.7mm) on Top Layer And Text "C21" |
| Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C21-2(14.325mm,18.7mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C21-2(14.325mm,18.7mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C23-1(8.675mm,12.1mm) on Top Layer And Text "C23" (7mm,10.7mm) on |
| Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C23-2(7.325mm,12.1mm) on Top Layer And Text "C23" (7mm,10.7mm) on |
| Silk To Solder Mask Clearance Constraint: (0.243mm < 0.254mm) Between Pad C3-2(29.489mm,7.725mm) on Top Layer And Text "C3" |
| Silk To Solder Mask Clearance Constraint: (0.132mm < 0.254mm) Between Pad C4-1(31.329mm,7.663mm) on Top Layer And Text "C4" |
| Silk To Solder Mask Clearance Constraint: (0.132mm < 0.254mm) Between Pad C4-2(32.679mm,7.663mm) on Top Layer And Text "C4" |
| Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad C4-2(32.679mm,7.663mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad C4-2(32.679mm,7.663mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.243mm < 0.254mm) Between Pad C5-2(35.179mm,7.725mm) on Top Layer And Text "C5" |
| Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad C6-1(32.725mm,29.4mm) on Top Layer And Text "12V" (32.4mm,28.4mm) |
| Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad C6-1(32.725mm,29.4mm) on Top Layer And Text "C6" (33mm,30.3mm) on |
| Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad C6-2(34.475mm,29.4mm) on Top Layer And Text "C6" (33mm,30.3mm) on |
| Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad C6-2(34.475mm,29.4mm) on Top Layer And Text "GND" (34mm,28.4mm) |
| Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad C8-1(21.5mm,18.4mm) on Top Layer And Text "C8" (22.2mm,18.4mm) on |
| Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad C8-2(21.5mm,17.05mm) on Top Layer And Text "C8" (22.2mm,18.4mm) |
| Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C9-1(21.2mm,12.525mm) on Top Layer And Text "C7" (21.8mm,13.7mm) |
| Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad C9-2(21.2mm,13.875mm) on Top Layer And Text "C7" (21.8mm,13.7mm) |
| Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad CS-TP(4.2mm,9.5mm) on Top Layer And Text "CS" (4.1mm,8.8mm) on |
| Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad CS-TP(4.2mm,9.5mm) on Top Layer And Text "SCK" (3.1mm,8.8mm) on |
| Silk To Solder Mask Clearance Constraint: (0.205mm < 0.254mm) Between Pad IN+-TP(18.5mm,15.1mm) on Top Layer And Text "IN+" (15.9mm,14.7mm) |
| Silk To Solder Mask Clearance Constraint: (0.182mm < 0.254mm) Between Pad IN+-TP(18.5mm,15.1mm) on Top Layer And Text "U4" (19.2mm,14.9mm) |
| Silk To Solder Mask Clearance Constraint: (0.253mm < 0.254mm) Between Pad IN+-TP(18.5mm,15.1mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.031mm < 0.254mm) Between Pad IN-TP(5.2mm,20.4mm) on Top Layer And Text "IN" (4.7mm,20.9mm) on |
| Silk To Solder Mask Clearance Constraint: (0.031mm < 0.254mm) Between Pad IP-TP(3.7mm,20.4mm) on Top Layer And Text "IP" (3.2mm,20.9mm) on |
| Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad L2-1(25.146mm,23.436mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad L2-1(25.146mm,23.436mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad L2-1(25.146mm,23.436mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad L2-2(25.146mm,20.236mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.218mm < 0.254mm) Between Pad L2-2(25.146mm,20.236mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad L2-2(25.146mm,20.236mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.135mm < 0.254mm) Between Pad LED1-1(28.55mm,27.49mm) on Top Layer And Text "LED1" |
| Silk To Solder Mask Clearance Constraint: (0.135mm < 0.254mm) Between Pad LED1-2(27.05mm,27.49mm) on Top Layer And Text "LED1" |
| Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED1-2(27.05mm,27.49mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.135mm < 0.254mm) Between Pad LED2-1(24.45mm,13.31mm) on Top Layer And Text "LED2" |
| Silk To Solder Mask Clearance Constraint: (0.135mm < 0.254mm) Between Pad LED2-2(25.95mm,13.31mm) on Top Layer And Text "LED2" |

| Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All) |
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| Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED2-2(25.95mm,13.31mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.194mm < 0.254mm) Between Pad MISO-TP(2.6mm,9.5mm) on Top Layer And Text "MISO" (2.1mm,8.8mm) |
| Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R10-1(10.375mm,21.2mm) on Top Layer And Text "R10" (8.6mm,21.8mm) |
| Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R10-2(8.825mm,21.2mm) on Top Layer And Text "R10" (8.6mm,21.8mm) on |
| Silk To Solder Mask Clearance Constraint: (0.246mm < 0.254mm) Between Pad R1-1(30.603mm,27.983mm) on Multi-Layer And Text "12V" |
| Silk To Solder Mask Clearance Constraint: (0.094mm < 0.254mm) Between Pad R1-1(30.603mm,27.983mm) on Multi-Layer And Text "LED1" |
| Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad R11-1(17.275mm,20mm) on Top Layer And Text "R11" (17.9mm,19.6mm) |
| Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad R12-1(14.3mm,15.925mm) on Top Layer And Text "R12" |
| Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R12-1(14.3mm,15.925mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R12-2(14.3mm,17.475mm) on Top Layer And Text "C21" (14.9mm,17.3mm) |
| Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R12-2(14.3mm,17.475mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.139mm < 0.254mm) Between Pad R1-3(30.603mm,31.533mm) on Multi-Layer And Text "IN" |
| Silk To Solder Mask Clearance Constraint: (0.134mm < 0.254mm) Between Pad R1-4(36.703mm,31.533mm) on Multi-Layer And Text "IP" |
| Silk To Solder Mask Clearance Constraint: (0.164mm < 0.254mm) Between Pad R1-5(13.503mm,9.433mm) on Multi-Layer And Text "C16" |
| Silk To Solder Mask Clearance Constraint: (0.185mm < 0.254mm) Between Pad R1-5(13.503mm,9.433mm) on Multi-Layer And Text "C20" |
| Silk To Solder Mask Clearance Constraint: (0.172mm < 0.254mm) Between Pad R3-1(25.8mm,27.5mm) on Top Layer And Text "LED1" (26.4mm,28.1mm) |
| Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R3-1(25.8mm,27.5mm) on Top Layer And Text "R3" (24.4mm,28.1mm) on |
| Silk To Solder Mask Clearance Constraint: (0.11mm < 0.254mm) Between Pad R3-1(25.8mm,27.5mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R3-2(24.25mm,27.5mm) on Top Layer And Text "R3" (24.4mm,28.1mm) on |
| Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R4-1(27.325mm,13.3mm) on Top Layer And Text "R4" (27.5mm,11.9mm) on |
| Silk To Solder Mask Clearance Constraint: (0.235mm < 0.254mm) Between Pad R4-1(27.325mm,13.3mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R4-2(28.875mm,13.3mm) on Top Layer And Text "R4" (27.5mm,11.9mm) on |
| Silk To Solder Mask Clearance Constraint: (0.144mm < 0.254mm) Between Pad R4-2(28.875mm,13.3mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.197mm < 0.254mm) Between Pad R4-2(28.875mm,13.3mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad R5-1(3.375mm,13mm) on Top Layer And Text "R5" (4mm,12.6mm) on Top |
| Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R6-1(3.925mm,23.6mm) on Top Layer And Text "R6" (4mm,24.2mm) on Top |
| Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R6-2(5.475mm,23.6mm) on Top Layer And Text "R6" (4mm,24.2mm) on Top |
| Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R7-1(5.025mm,22.3mm) on Top Layer And Text "IN" (4.7mm,20.9mm) on |
| Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R7-1(5.025mm,22.3mm) on Top Layer And Text "R7" (3.2mm,21.9mm) on |
| Silk To Solder Mask Clearance Constraint: (0.231mm < 0.254mm) Between Pad R7-2(6.575mm,22.3mm) on Top Layer And Text "IN" (4.7mm,20.9mm) on |
| Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad R9-1(2.575mm,21.5mm) on Top Layer And Text "IP" (3.2mm,20.9mm) on |
| Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad R9-1(2.575mm,21.5mm) on Top Layer And Text "R7" (3.2mm,21.9mm) on |
| Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R9-1(2.575mm,21.5mm) on Top Layer And Text "R8" (1.3mm,22.1mm) on |
| Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad R9-2(1.025mm,21.5mm) on Top Layer And Text "R8" (1.3mm,22.1mm) on |
| Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad TP3-TP(37.206mm,13.3mm) on Top Layer And Text "12V" |
| Silk To Solder Mask Clearance Constraint: (0.234mm < 0.254mm) Between Pad TP3-TP(37.206mm,13.3mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad U1-1(33.655mm,9.06mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad U1-1(33.655mm,9.06mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad U1-2(33.655mm,10.01mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad U1-3(33.655mm,10.96mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad U1-3(33.655mm,10.96mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad U1-4(31.355mm,10.96mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad U1-4(31.355mm,10.96mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad U1-5(31.355mm,9.06mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad U1-5(31.355mm,9.06mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.203mm < 0.254mm) Between Pad U2-1(28.096mm,22.85mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad U2-2(28.096mm,20.31mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad U2-4(28.096mm,15.23mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.243mm < 0.254mm) Between Pad U2-5(38.006mm,15.23mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.243mm < 0.254mm) Between Pad U2-8(38.006mm,22.85mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.222mm < 0.254mm) Between Pad U4-1(17.425mm,18.45mm) on Top Layer And Text "C21" |
| Silk To Solder Mask Clearance Constraint: (0.136mm < 0.254mm) Between Pad U4-2(17.425mm,17.5mm) on Top Layer And Text "C21" (14.9mm,17.3mm) |

| Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All) |
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| Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U5-6(4.151mm,14.416mm) on Top Layer And Text "R5" (4mm,12.6mm) on |
| Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U5-8(5.151mm,14.416mm) on Top Layer And Text "R5" (4mm,12.6mm) on |
| Silk To Solder Mask Clearance Constraint: (0.063mm < 0.254mm) Between Pad VREF-TP(18.5mm,13.6mm) on Top Layer And Text "VREF" |
| Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad XFMR1-1(13.254mm,31.854mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-10(22.004mm,24.234mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-10(22.004mm,24.234mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-11(22.004mm,25.504mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-11(22.004mm,25.504mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-12(22.004mm,26.774mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-12(22.004mm,26.774mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-13(22.004mm,28.044mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-13(22.004mm,28.044mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-14(22.004mm,29.314mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-14(22.004mm,29.314mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-15(22.004mm,30.584mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-15(22.004mm,30.584mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-16(22.004mm,31.854mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-16(22.004mm,31.854mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad XFMR1-2(13.254mm,30.584mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.241mm < 0.254mm) Between Pad XFMR1-3(13.254mm,29.314mm) on Top Layer And Text "C13" |
| Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad XFMR1-3(13.254mm,29.314mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad XFMR1-4(13.254mm,28.044mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad XFMR1-5(13.254mm,26.774mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad XFMR1-6(13.254mm,25.504mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad XFMR1-7(13.254mm,24.234mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad XFMR1-8(13.254mm,22.964mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.226mm < 0.254mm) Between Pad XFMR1-9(22.004mm,22.964mm) on Top Layer And Track |
| Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad XFMR1-9(22.004mm,22.964mm) on Top Layer And Track |

| Silk to Silk (Clearance=0.254mm) (All),(All) |
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| Silk To Silk Clearance Constraint: (0.237mm < 0.254mm) Between Arc (17.425mm,19.3mm) on Top Overlay And Text "R11" (17.9mm,19.6mm) on Top |
| Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Arc (28.596mm,24.89mm) on Top Overlay And Text "C1" (27.871mm,25.376mm) on Top |
| Silk To Silk Clearance Constraint: (0.176mm < 0.254mm) Between Text "12V" (37.846mm,14.648mm) on Top Overlay And Text "C2" (37.706mm,11.2mm) |
| Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "C14" (16.9mm,10.9mm) on Bottom Overlay And Text "R2" (18.1mm,10.9mm) on |
| Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "C7" (21.8mm,13.7mm) on Top Overlay And Text "C9" (22.8mm,13.7mm) on Top |
| Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "C9" (22.8mm,13.7mm) on Top Overlay And Text "LED2" (23.8mm,11.9mm) on Top |
| Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "CS" (4.1mm,8.8mm) on Top Overlay And Text "SCK" (3.1mm,8.8mm) on Top |
| Silk To Silk Clearance Constraint: (0.179mm < 0.254mm) Between Text "IN" (4.7mm,20.9mm) on Top Overlay And Text "IP" (3.2mm,20.9mm) on Top |
| Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "IP" (3.2mm,20.9mm) on Top Overlay And Text "R7" (3.2mm,21.9mm) on Top |
| Silk To Silk Clearance Constraint: (0.039mm < 0.254mm) Between Text "L2" (24.6mm,18.2mm) on Top Overlay And Track |
| Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "L2" (24.6mm,18.2mm) on Top Overlay And Track (24mm,18mm)(39.5mm,18mm) |
| Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "LED1" (26.4mm,28.1mm) on Top Overlay And Text "PWR" (25.3mm,29.1mm) on |
| Silk To Silk Clearance Constraint: (0.02mm < 0.254mm) Between Text "LED1" (26.4mm,28.1mm) on Top Overlay And Track |
| Silk To Silk Clearance Constraint: (0.02mm < 0.254mm) Between Text "LED2" (23.8mm,11.9mm) on Top Overlay And Track |
| Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "MISO" (2.1mm,8.8mm) on Top Overlay And Text "MOSI" (1.1mm,8.8mm) on Top |
| Silk To Silk Clearance Constraint: (0.05mm < 0.254mm) Between Text "MISO" (2.1mm,8.8mm) on Top Overlay And Text "SCK" (3.1mm,8.8mm) on Top |
| Silk To Silk Clearance Constraint: (0.053mm < 0.254mm) Between Text "PWR" (25.3mm,29.1mm) on Top Overlay And Text "R3" (24.4mm,28.1mm) on Top |
| Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "R12" (13.9mm,15.4mm) on Top Overlay And Text "VREF" (15.1mm,13.2mm) on |
| Silk To Silk Clearance Constraint: (0.15mm < 0.254mm) Between Text "R12" (13.9mm,15.4mm) on Top Overlay And Track |
| Silk To Silk Clearance Constraint: (0.157mm < 0.254mm) Between Text "R12" (13.9mm,15.4mm) on Top Overlay And Track |
| Silk To Silk Clearance Constraint: (0.15mm < 0.254mm) Between Text "R8" (1.3mm,22.1mm) on Top Overlay And Text "R9" (1.3mm,23.2mm) on Top |
| Silk To Silk Clearance Constraint: (0.075mm < 0.254mm) Between Text "U4" (19.2mm,14.9mm) on Top Overlay And Track |
| Silk To Silk Clearance Constraint: (0.095mm < 0.254mm) Between Text "U4" (19.2mm,14.9mm) on Top Overlay And Track |
| Silk To Silk Clearance Constraint: (0.052mm < 0.254mm) Between Text "U5" (0.2mm,17.2mm) on Top Overlay And Track |
| Silk To Silk Clearance Constraint: (0.252mm < 0.254mm) Between Text "U6" (6mm,17.2mm) on Top Overlay And Track |
| Silk To Silk Clearance Constraint: (0mm < 0.254mm) Between Text "U6" (6mm,17.2mm) on Top Overlay And Track (6.975mm,14.8mm)(6.975mm,18.5mm) |