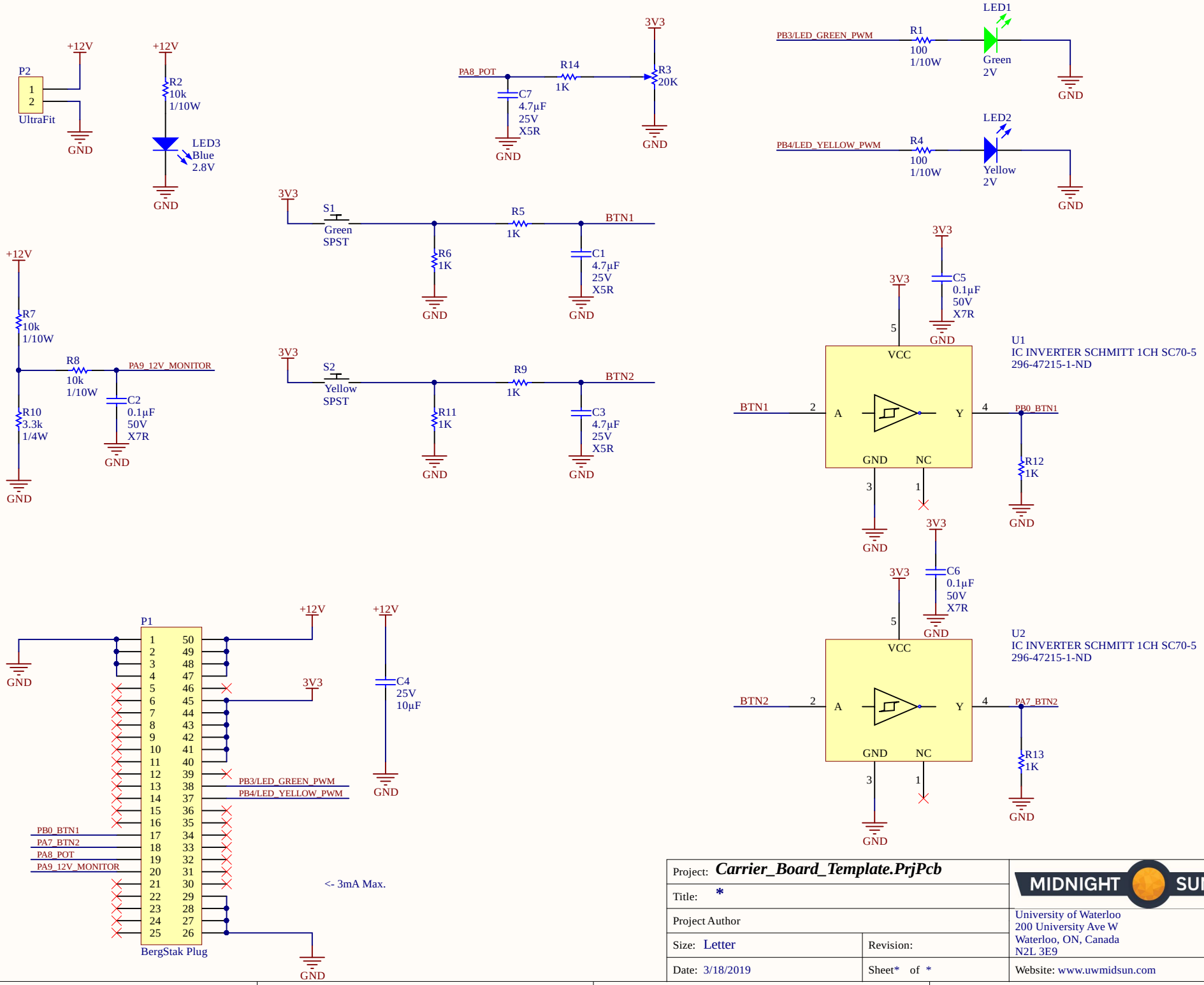
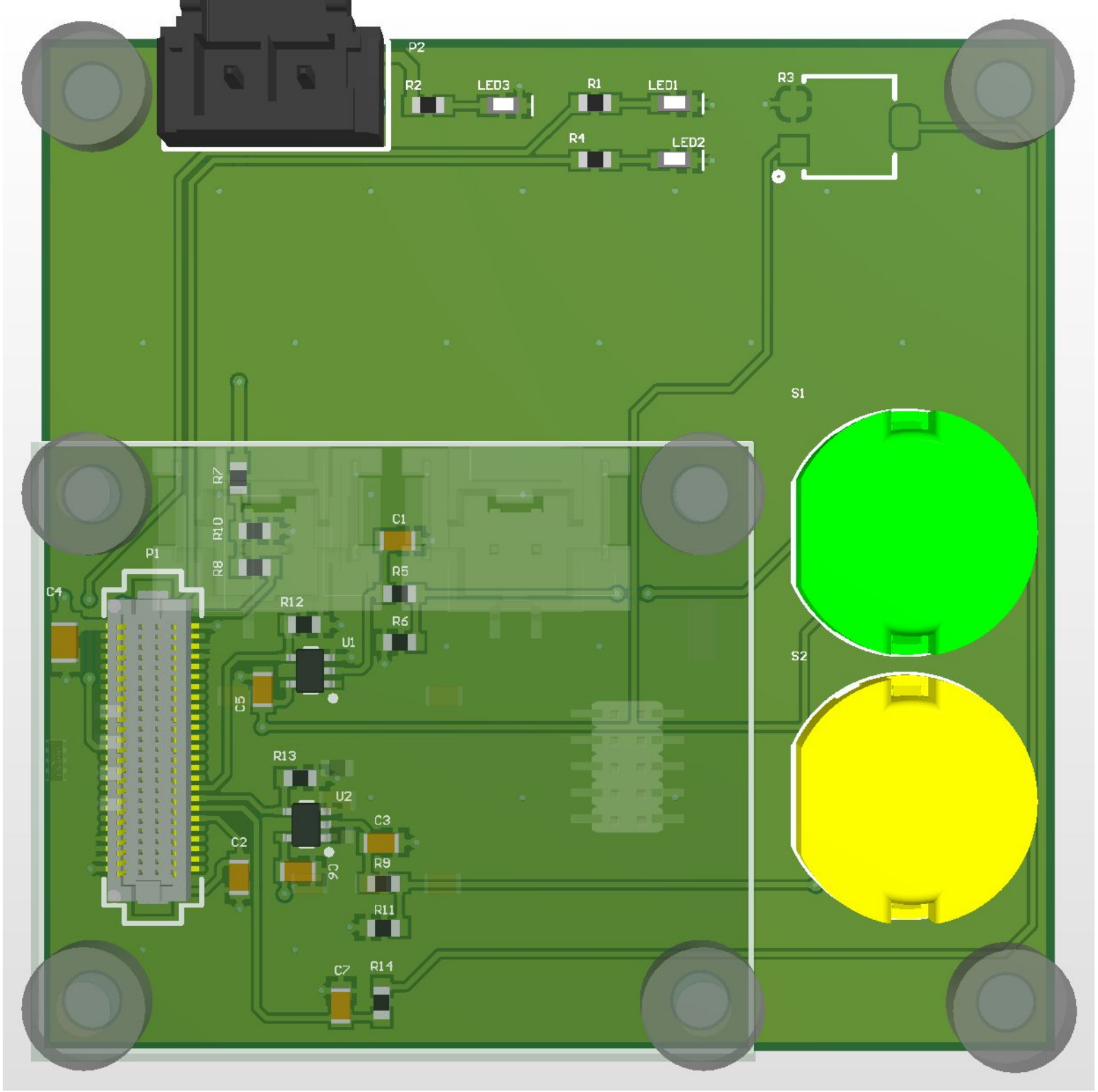
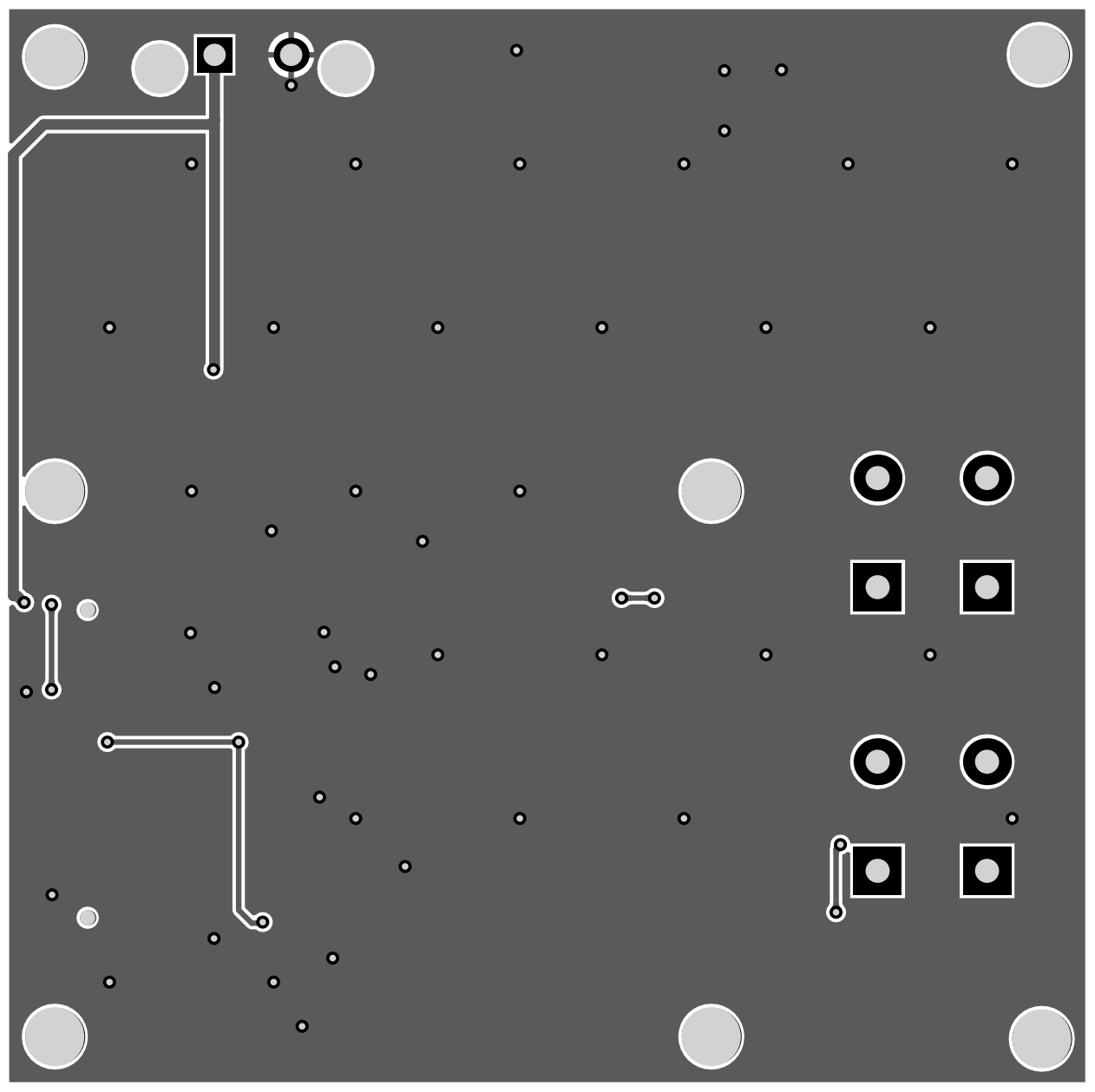

P2
1
2
UltraFit
+12V
GND
+12V
R2
10k
1/10W
LED3
Blue
2.8V
GND
PA8_POT
R14
1K
C7
4.7µF
25V
X5R
GND
3V3
R3
20K
GND
PB3/LED_GREEN_PWM
R1
100
1/10W
LED1
Green
2V
GND
PB4/LED_YELLOW_PWM
R4
100
1/10W
LED2
Yellow
2V
GND
3V3
S1
Green
SPST
R5
1K
BTN1
R6
1K
C1
4.7µF
25V
X5R
GND
GND
+12V
R7
10k
1/10W
R8
10k
1/10W
PA9_12V_MONITOR
C2
0.1µF
50V
X7R
R10
3.3k
1/4W
GND
GND
3V3
S2
Yellow
SPST
R9
1K
BTN2
R11
1K
C3
4.7µF
25V
X5R
GND
GND
3V3
C5
0.1µF
50V
X7R
GND
5
VCC
U1
IC INVERTER SCHMITT 1CH SC70-5
296-47215-1-ND
BTN1
2
A
Y
4
PB0_BTN1
GND
NC
3
1
R12
1K
GND
GND
3V3
C6
0.1µF
50V
X7R
GND
3V3
5
VCC
U2
IC INVERTER SCHMITT 1CH SC70-5
296-47215-1-ND
BTN2
2
A
Y
4
PA7_BTN2
GND
NC
3
1
R13
1K
GND
GND
P1
1 50
2 49
3 48
4 47
5 46
6 45
7 44
8 43
9 42
10 41
11 40
12 39
13 38
14 37
15 36
16 35
17 34
18 33
19 32
20 31
21 30
22 29
23 28
24 27
25 26
BergStak Plug
+12V
3V3
GND
PB3/LED_GREEN_PWM
PB4/LED_YELLOW_PWM
PB0_BTN1
PA7_BTN2
PA8_POT
PA9_12V_MONITOR
+12V
C4
25V
10µF
GND
<- 3mA Max.
GND
Project: Carrier_Board_Template.PrjPcb
Title: *
Project Author
Size: Letter
Revision:
Date: 3/18/2019
Sheet* of *
MIDNIGHT SUN
University of Waterloo
200 University Ave W
Waterloo, ON, Canada
N2L 3E9
Website: www.uwmidsun.com


P2
R2
LED3
R1
LED1
R3
R4
LED2
S1
S2
P1
C4
R7
R10
R8
C1
R5
R12
R6
U1
C5
R13
U2
C3
C2
C6
R9
R11
C7
R14



Electrical Rules Check Repor

Class	Document	Message
Warning	hw_tutorial.SchDoc	Extra Pin R3-2 (Inferred) in Alternate 1 of part R
Warning	hw_tutorial.SchDoc	Extra Pin R3-2 in Normal of part R?
Warning	hw_tutorial.SchDoc	Extra Pin R3-3 (Inferred) in Alternate 1 of part R
Warning	hw_tutorial.SchDoc	Extra Pin R3-3 in Normal of part R?

Design Rules Verification Repor

Filename : \\Mac\Home\Documents\midsun\hardware\MSXII_HW_Tutorial\hw_tutorial.Pcb

Warnings 0
Rule Violations 115

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All	0
Short-Circuit Constraint (Allowed=No) (All),(All	0
Un-Routed Net Constraint ((All)	0
Modified Polygon (Allow modified: No), (Allow shelved: Nc	0
Width Constraint (Min=0.152mm) (Max=2.54mm) (Preferred=0.254mm) (Al	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mr	0
Minimum Annular Ring (Minimum=0.152mm) (Al	55
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All	0
Hole To Hole Clearance (Gap=0.254mm) (All),(Al	0
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All	45
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(Al	0
Silk to Silk (Clearance=0.254mm) (All),(All	2
Net Antennae (Tolerance=0mm) (Al	0
Board Clearance Constraint (Gap=0mm) (All	13
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (Al	0
Total	115

Minimum Annular Ring (Minimum=0.152mm) (Al
Minimum Annular Ring: (0.15mm < 0.152mm) Via (1.1mm,22.4mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (1.2mm,18.3mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (10.9mm,16mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (12.4mm,25.68mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (12.5mm,35mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (12.5mm,5mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (12mm,7.75mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (13.3mm,46.1mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (13.8mm,2.975mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (14.6mm,13.475mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (14.8mm,21.037mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (15.2mm,6.1mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (15.3mm,19.45mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (16.25mm,12.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (16.25mm,27.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (16.25mm,42.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (16.933mm,19.1mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (18.508mm,10.3mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (19.3mm,25.2mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (2.35mm,18.405mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (2.35mm,22.3mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (2.375mm,9mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (20mm,20mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (20mm,35mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (23.6mm,47.7mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (23.75mm,12.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (23.75mm,27.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (23.75mm,42.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (27.5mm,20mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (27.5mm,35mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (28.4mm,22.6mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (29.904mm,22.6mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (31.25mm,12.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (31.25mm,42.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (33.1mm,44.012mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (33.1mm,46.77mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (35.708mm,46.802mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (35mm,20mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (35mm,35mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (38.2mm,8.2mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (38.4mm,11.3mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (38.75mm,42.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (4.9mm,16mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (42.5mm,20mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (42.5mm,35mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (46.25mm,12.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (46.25mm,42.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (5mm,35mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (5mm,5mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (8.75mm,27.5mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (8.75mm,42.5mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (8.7mm,21mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)

Minimum Annular Ring (Minimum=0.152mm) (Al
Minimum Annular Ring: (0.15mm < 0.152mm) Via (9.75mm,33.069mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (9.775mm,7mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (9.8mm,18.5mm) from Top Layer to Bottom Layer (Annular Ring=0.15m

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C1-1(16.933mm,25.2mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.089mm < 0.3mm) Between Pad C1-2(18.283mm,25.2mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C2-1(9.8mm,9.3mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.3mm) Between Pad C2-2(9.8mm,7.95mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C3-1(16.125mm,10.3mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad C3-2(17.475mm,10.3mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.3mm) Between Pad C4-1(1.2mm,21.075mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.3mm) Between Pad C4-1(1.2mm,21.075mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.023mm < 0.3mm) Between Pad C4-2(1.2mm,19.325mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C5-1(10.95mm,17.2mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.208mm < 0.3mm) Between Pad C5-1(10.95mm,17.2mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.272mm < 0.3mm) Between Pad C5-1(10.95mm,17.2mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.176mm < 0.3mm) Between Pad C5-2(10.95mm,18.55mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad C5-2(10.95mm,18.55mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.172mm < 0.3mm) Between Pad C5-2(10.95mm,18.55mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C6-1(12.025mm,8.9mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.172mm < 0.3mm) Between Pad C6-1(12.025mm,8.9mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C7-1(14.8mm,1.625mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.3mm) Between Pad C7-2(14.8mm,2.975mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.258mm < 0.3mm) Between Pad LED1-2(31.939mm,46.805mm) on Top Layer A
Minimum Solder Mask Sliver Constraint: (0.258mm < 0.3mm) Between Pad LED2-2(31.939mm,44.012mm) on Top Layer A
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad LED3-2(23.55mm,46.7mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(4mm,22.05mm) on Multi-Layer And P
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(4mm,7.95mm) on Multi-Layer And P
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P1-1(7.3mm,21mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.3mm) Between Pad P1-2(7.3mm,20.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.3mm) Between Pad P1-26(3.7mm,9mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.187mm < 0.3mm) Between Pad P1-27(3.7mm,9.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.09mm < 0.3mm) Between Pad P1-39(3.7mm,15.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.09mm < 0.3mm) Between Pad P1-41(3.7mm,16.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.156mm < 0.3mm) Between Pad P1-44(3.7mm,18mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.053mm < 0.3mm) Between Pad P1-45(3.7mm,18.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.265mm < 0.3mm) Between Pad P1-46(3.7mm,19mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.092mm < 0.3mm) Between Pad P2-2(13.3mm,47.495mm) on Multi-Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad R10-2(11.325mm,25.7mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad R12-1(13.775mm,21.075mm) on Top Layer A
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad R13-1(13.575mm,13.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.239mm < 0.3mm) Between Pad R3-3(37.1mm,46.8mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.172mm < 0.3mm) Between Pad R6-1(16.933mm,20.2mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad S2-1(40.1mm,10.1mm) on Multi-Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U1-1(14.4mm,18.15mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U1-2(14.4mm,18.8mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.126mm < 0.3mm) Between Pad U1-2(14.4mm,18.8mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U2-1(14.2mm,10.55mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U2-2(14.2mm,11.2mm) on Top Layer And F

Silk to Silk (Clearance=0.254mm) (All),(All
Silk To Silk Clearance Constraint: (0.137mm < 0.254mm) Between Text "C4" (0.302mm,22.496mm) on Top Overlay And Tr
Silk To Silk Clearance Constraint: (0.132mm < 0.254mm) Between Text "LED2" (31.189mm,44.7mm) on Top Overlay /

Board Clearance Constraint (Gap=0mm) (All
Board Outline Clearance(Outline Edge): (0.227mm < 0.406mm) Between Board Edge And Text "C4" (0.302mm,22.496mm)
Board Outline Clearance(Outline Edge): (0.125mm < 0.406mm) Between Board Edge And Text "P2" (18.2mm,49.4mm)
Board Outline Clearance(Outline Edge): (0.356mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.356mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.356mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,0mm)(0mm,30mm)
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,0mm)(35mm,0mm)
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,30mm)(35mm,30m
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (35mm,0mm)(35mm,30m
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Tra