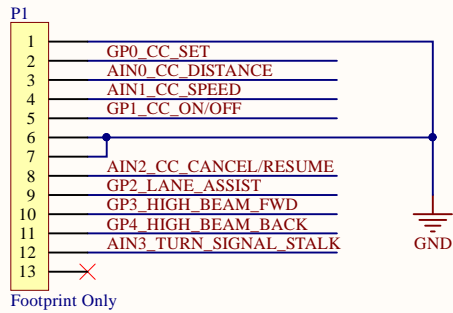
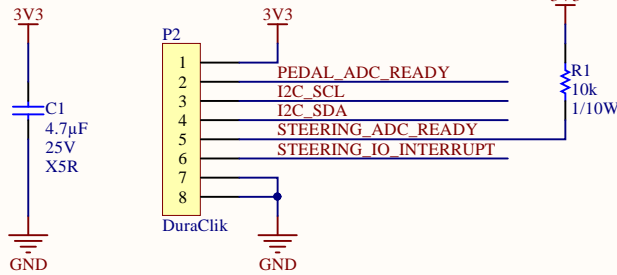


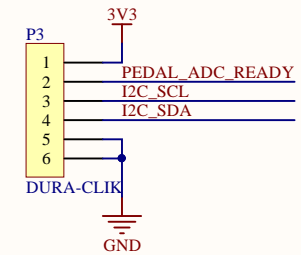
Steering Stalk Connector



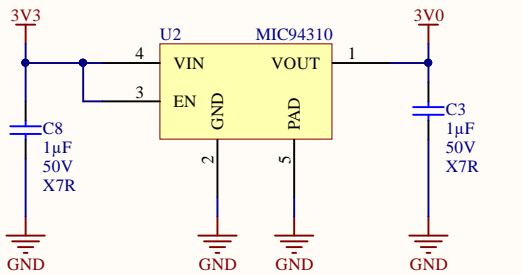
From Center Console Board



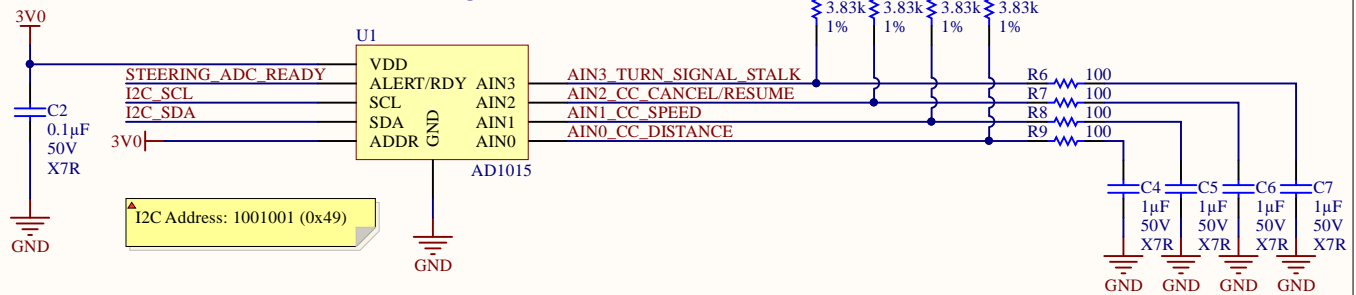
To Pedal Interface Board



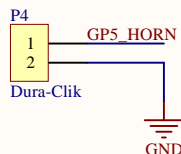
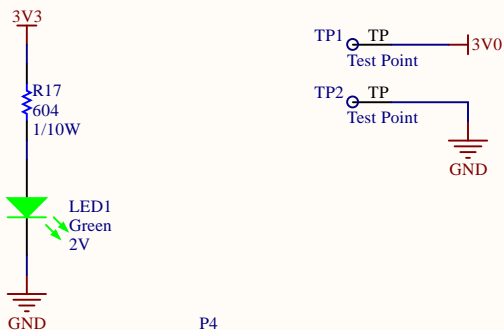
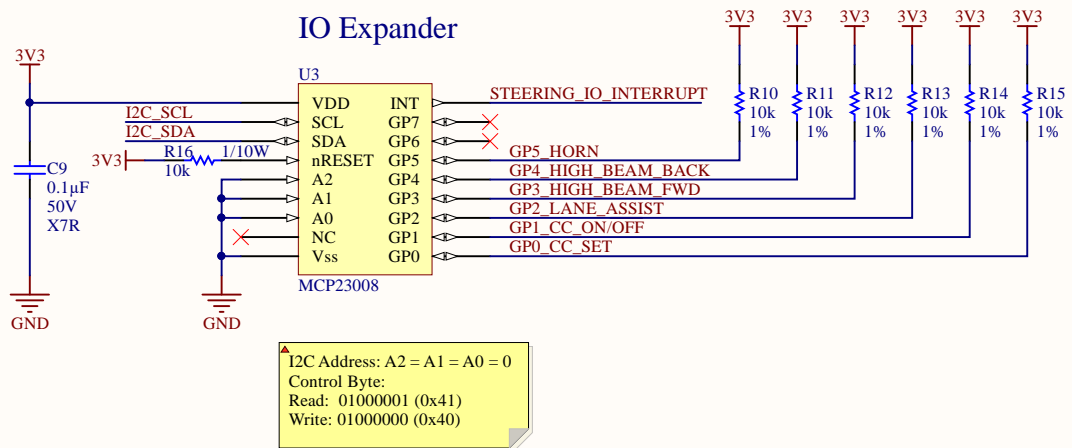
Power Supply



ADC



IO Expander



Project: **MSXII_SteeringWheelInterfaceBoard.PrjPcb**

Title: **Steering Wheel Interface Board**

Project Author: **Taiping Li**

Size: **Letter**

Date: **5/20/2018**

Revision: **1.1**

Sheet 1 of 1

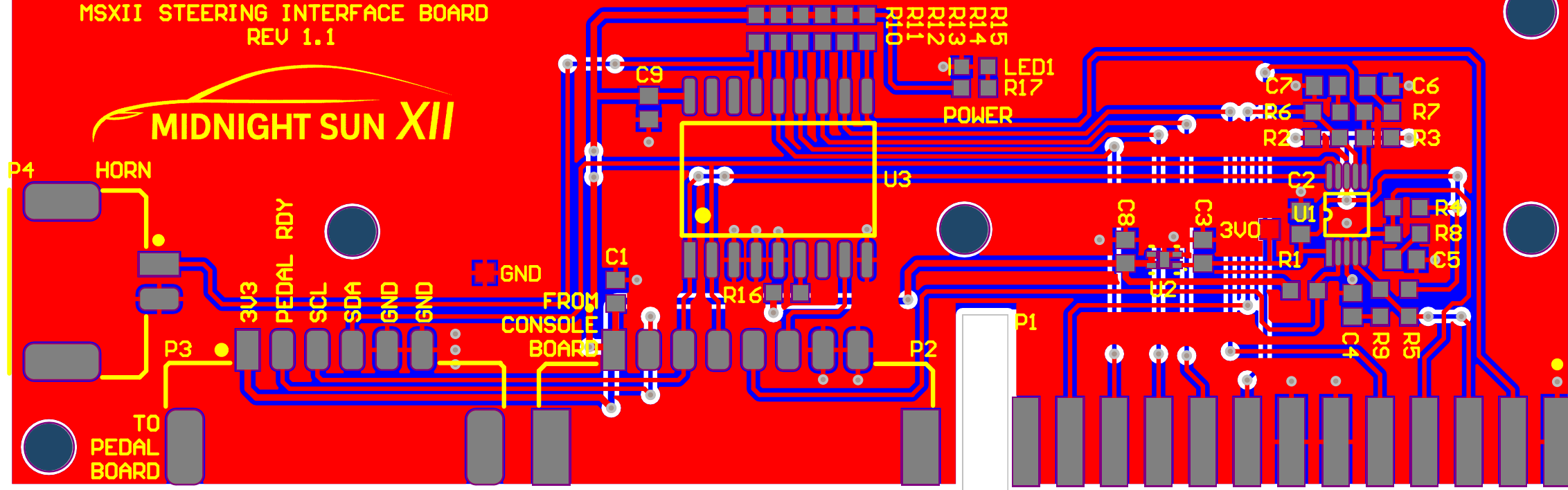


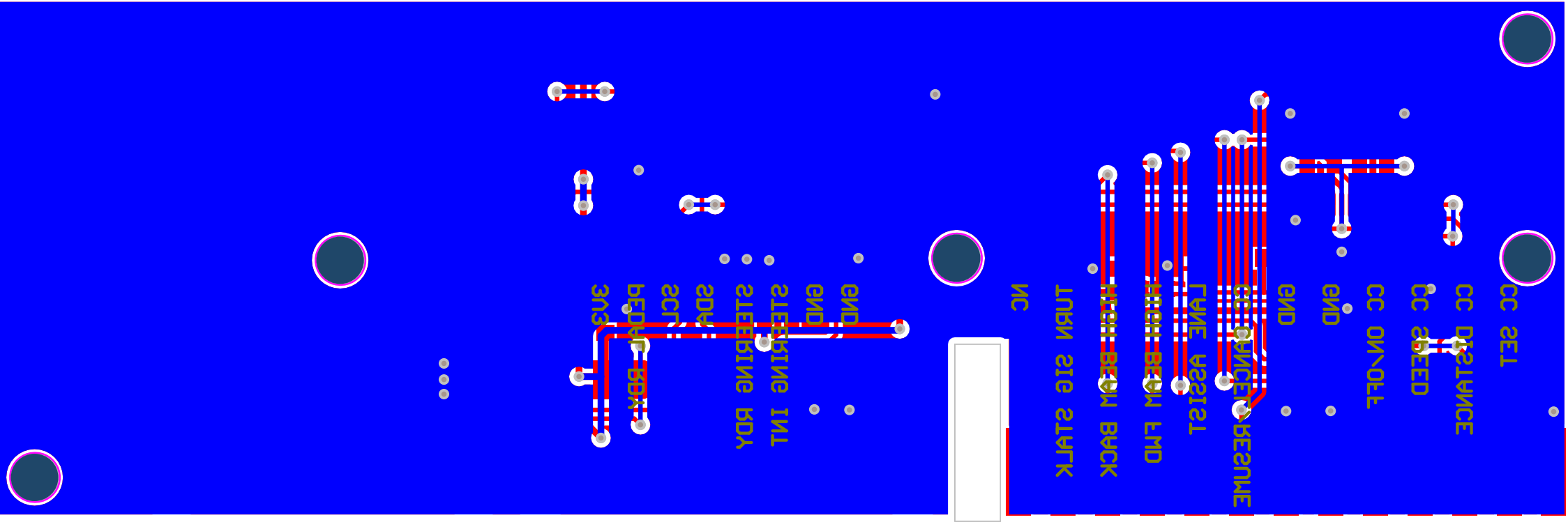
University of Waterloo
200 University Ave W
Waterloo, ON, Canada
N2L 3E9

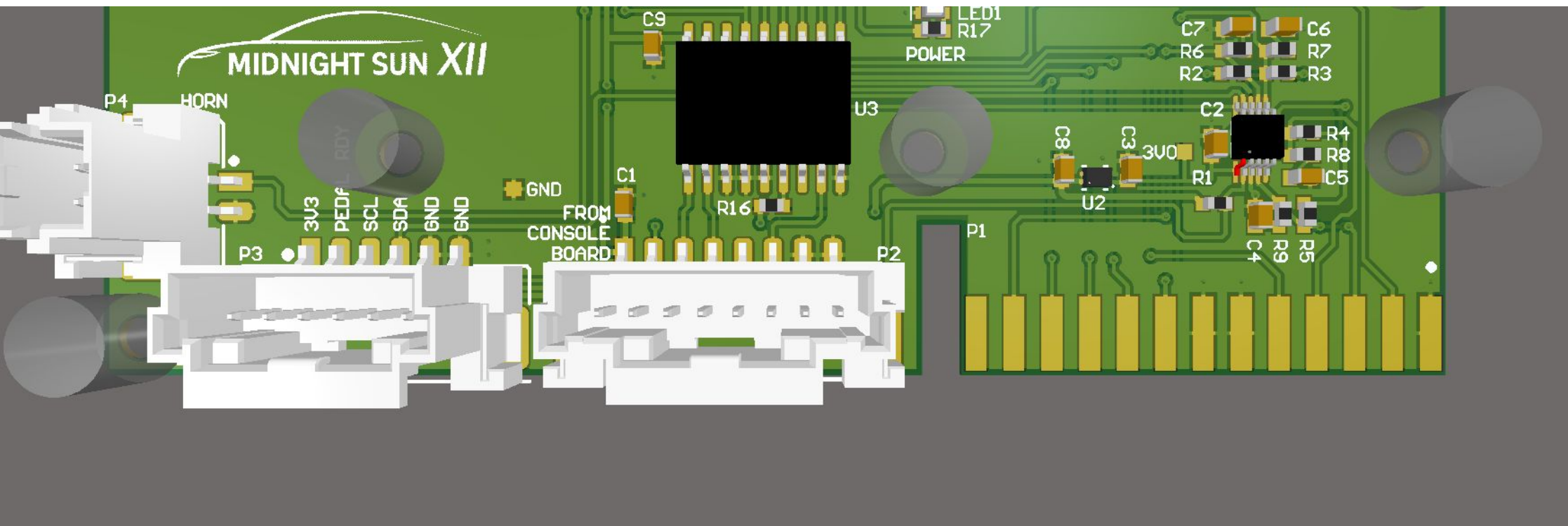
Website: www.uwmidsun.com

MSXII STEERING INTERFACE BOARD
REV 1.1

MIDNIGHT SUN *XII*







Electrical Rules Check Report

Class	Document	Message
Warning	Steering Wheel Interface.SchDoc	Net NetR16_2 has no driving source (Pin R16-2,Pin U3-6)

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII_SteeringWheelInterfa

Warnings 0
Rule Violations 59

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.508mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	5
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	18
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	27
Silk to Silk (Clearance=0.254mm) (All),(All)	9
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	59

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(19.9mm,14.88mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(55.002mm,15mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(87.5mm,15mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(87.5mm,27.5mm) on Multi-Layer Actual Hole Size = 2.7mm	

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	
Minimum Solder Mask Sliver Constraint: (0.188mm < 0.254mm) Between Pad LED1-1(56.342mm,24.339mm) on Top Layer And Pad	
Minimum Solder Mask Sliver Constraint: (0.188mm < 0.254mm) Between Pad LED1-2(54.842mm,24.339mm) on Top Layer And Pad	
Minimum Solder Mask Sliver Constraint: (0.217mm < 0.254mm) Between Pad R10-1(43.06mm,27.3mm) on Top Layer And Pad R11-1(44.33mm,27.3mm)	
Minimum Solder Mask Sliver Constraint: (0.217mm < 0.254mm) Between Pad R10-2(43.06mm,25.75mm) on Top Layer And Pad	
Minimum Solder Mask Sliver Constraint: (0.217mm < 0.254mm) Between Pad R11-1(44.33mm,27.3mm) on Top Layer And Pad R12-1(45.6mm,27.3mm) on	
Minimum Solder Mask Sliver Constraint: (0.217mm < 0.254mm) Between Pad R11-2(44.33mm,25.75mm) on Top Layer And Pad R12-2(45.6mm,25.75mm)	
Minimum Solder Mask Sliver Constraint: (0.217mm < 0.254mm) Between Pad R12-1(45.6mm,27.3mm) on Top Layer And Pad R13-1(46.87mm,27.3mm) on	
Minimum Solder Mask Sliver Constraint: (0.217mm < 0.254mm) Between Pad R12-2(45.6mm,25.75mm) on Top Layer And Pad R13-2(46.87mm,25.75mm)	
Minimum Solder Mask Sliver Constraint: (0.217mm < 0.254mm) Between Pad R13-1(46.87mm,27.3mm) on Top Layer And Pad R14-1(48.14mm,27.3mm)	
Minimum Solder Mask Sliver Constraint: (0.217mm < 0.254mm) Between Pad R13-2(46.87mm,25.75mm) on Top Layer And Pad	
Minimum Solder Mask Sliver Constraint: (0.217mm < 0.254mm) Between Pad R14-1(48.14mm,27.3mm) on Top Layer And Pad R15-1(49.41mm,27.3mm)	
Minimum Solder Mask Sliver Constraint: (0.217mm < 0.254mm) Between Pad R14-2(48.14mm,25.75mm) on Top Layer And Pad	
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U2-1(67.178mm,12.95mm) on Top Layer And Pad	
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.254mm) Between Pad U2-1(67.178mm,12.95mm) on Top Layer And Pad	
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.254mm) Between Pad U2-2(67.178mm,13.55mm) on Top Layer And Pad	
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U2-3(65.738mm,13.55mm) on Top Layer And Pad	
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.254mm) Between Pad U2-3(65.738mm,13.55mm) on Top Layer And Pad	
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.254mm) Between Pad U2-4(65.738mm,12.95mm) on Top Layer And Pad	

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (0.188mm < 0.254mm) Between Arc (67.686mm,12.696mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.042mm < 0.254mm) Between Pad 3V0-TP(72.5mm,15mm) on Top Layer And Text "3V0"
Silk To Solder Mask Clearance Constraint: (0.246mm < 0.254mm) Between Pad C2-1(74.3mm,14.729mm) on Top Layer And Text "U1" (74mm,15.5mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad C2-2(74.3mm,16.079mm) on Top Layer And Text "U1" (74mm,15.5mm) on
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED1-2(54.842mm,24.339mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P2-(31.3mm,2.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P2-(52.5mm,2.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.18mm < 0.254mm) Between Pad P4-3(3.25mm,16.605mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.241mm < 0.254mm) Between Pad P4-3(3.25mm,7.405mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad U1-1(75.93mm,13.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad U1-1(75.93mm,13.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.243mm < 0.254mm) Between Pad U1-10(75.93mm,18.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.195mm < 0.254mm) Between Pad U1-10(75.93mm,18.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.206mm < 0.254mm) Between Pad U1-2(76.43mm,13.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.206mm < 0.254mm) Between Pad U1-3(76.93mm,13.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.206mm < 0.254mm) Between Pad U1-4(77.43mm,13.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.206mm < 0.254mm) Between Pad U1-5(77.93mm,13.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-5(77.93mm,13.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.195mm < 0.254mm) Between Pad U1-6(77.93mm,18.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-6(77.93mm,18.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.195mm < 0.254mm) Between Pad U1-7(77.43mm,18.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.195mm < 0.254mm) Between Pad U1-8(76.93mm,18.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.195mm < 0.254mm) Between Pad U1-9(76.43mm,18.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U2-1(67.178mm,12.95mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U2-2(67.178mm,13.55mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U2-3(65.738mm,13.55mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U2-4(65.738mm,12.95mm) on Top Layer And Track

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Arc (33.5mm,10.48mm) on Top Overlay And Text "FROM"

CONSOLE**BOARD" (28.4mm,7.6mm) on Top Overlay Silk Text to Silk Clearance [0mm]****Silk to Silk (Clearance=0.254mm) (All),(All)**

Silk To Silk Clearance Constraint: (0.235mm < 0.254mm) Between Text "LED1" (57.4mm,23.935mm) on Top Overlay And Text "R17" (57.4mm,22.75mm)
Silk To Silk Clearance Constraint: (0.244mm < 0.254mm) Between Text "P3" (9.25mm,7.75mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.218mm < 0.254mm) Between Text "P3" (9.25mm,7.75mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "R10" (50.576mm,27.677mm) on Top Overlay And Text "R11"
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "R11" (51.776mm,27.677mm) on Top Overlay And Text "R12"
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "R12" (52.976mm,27.677mm) on Top Overlay And Text "R13"
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "R13" (54.176mm,27.677mm) on Top Overlay And Text "R14"
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "R14" (55.376mm,27.677mm) on Top Overlay And Text "R15"