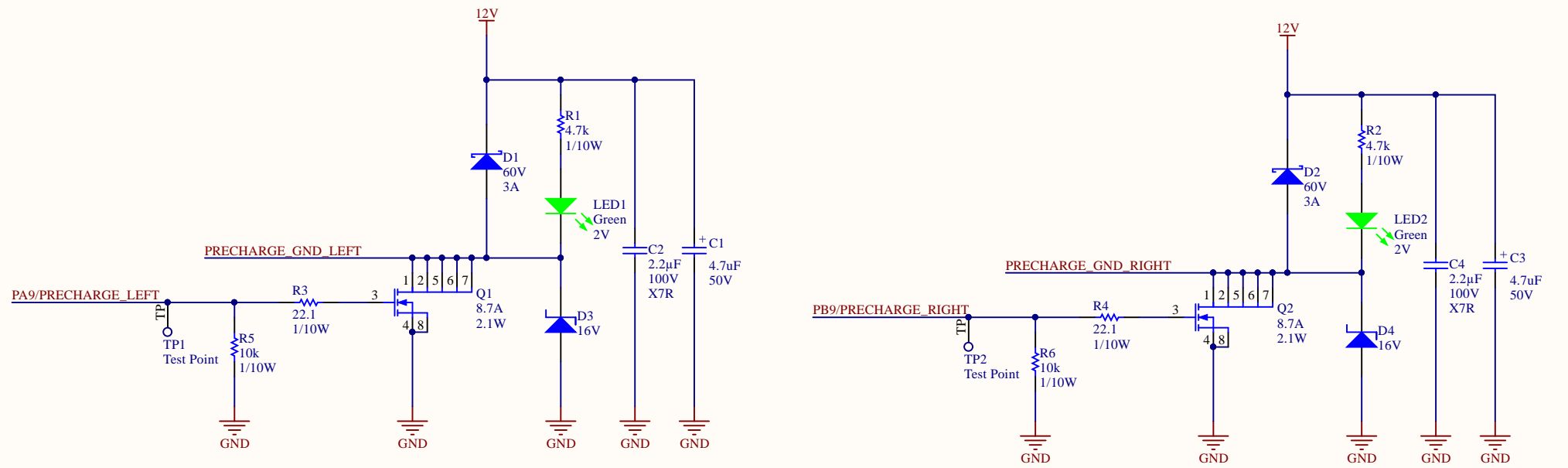
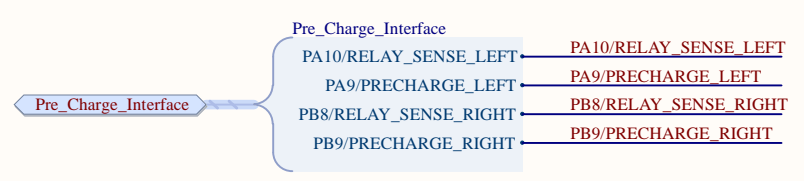
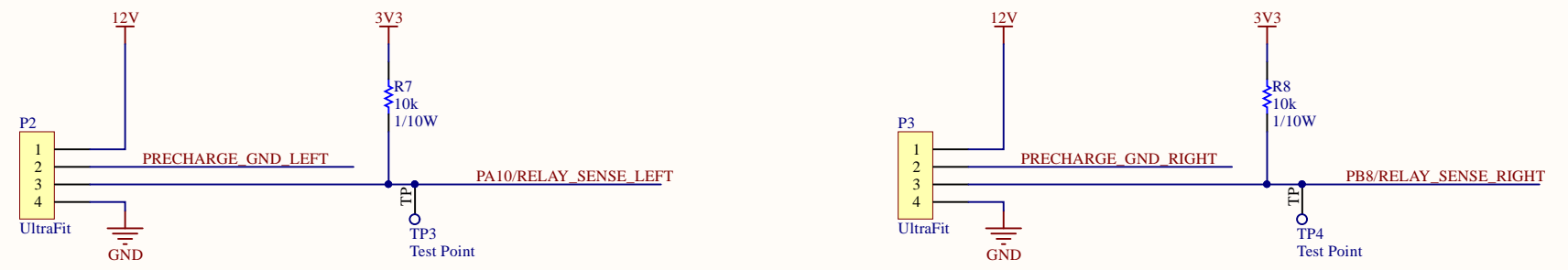



Precharge Control

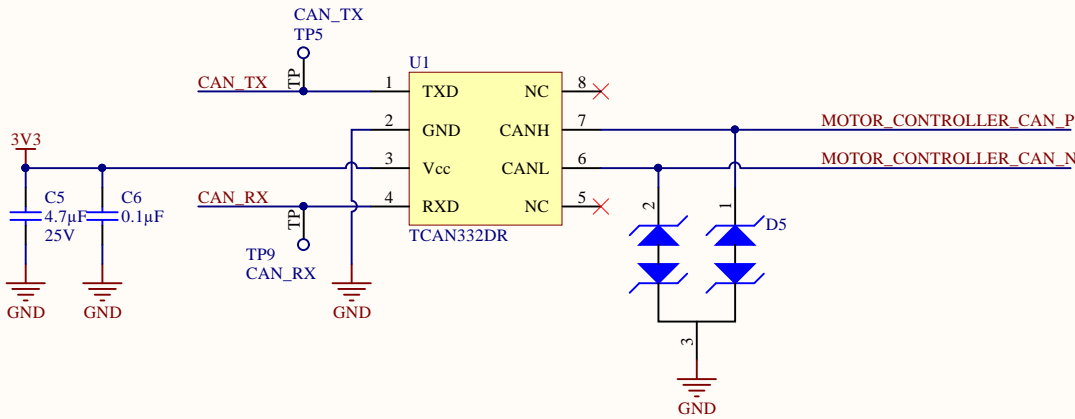


Relay Connectors

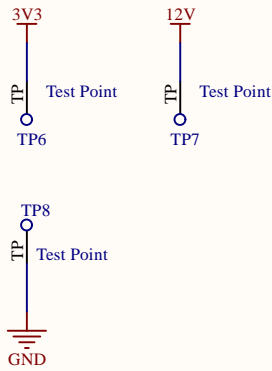


Project: <i>MSXII_MotorControllerInterface.PrjPcb</i>		<div>MIDNIGHTSUN</div>
Title: PreCharge Interface		
Project Author: Peiliang Guo		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9 Website: www.uwmidsun.com
Size: Letter	Revision: 1.6	
Date: 2018-06-22	Sheet2 of 3	

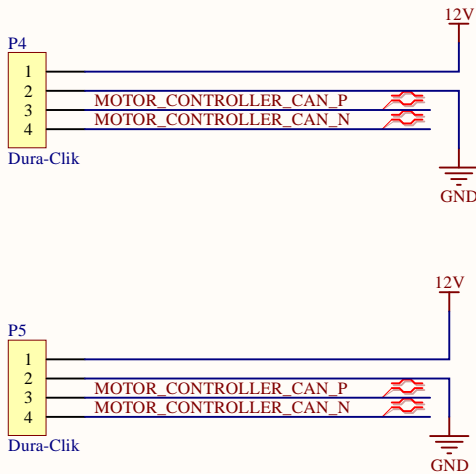
CAN Transceiver



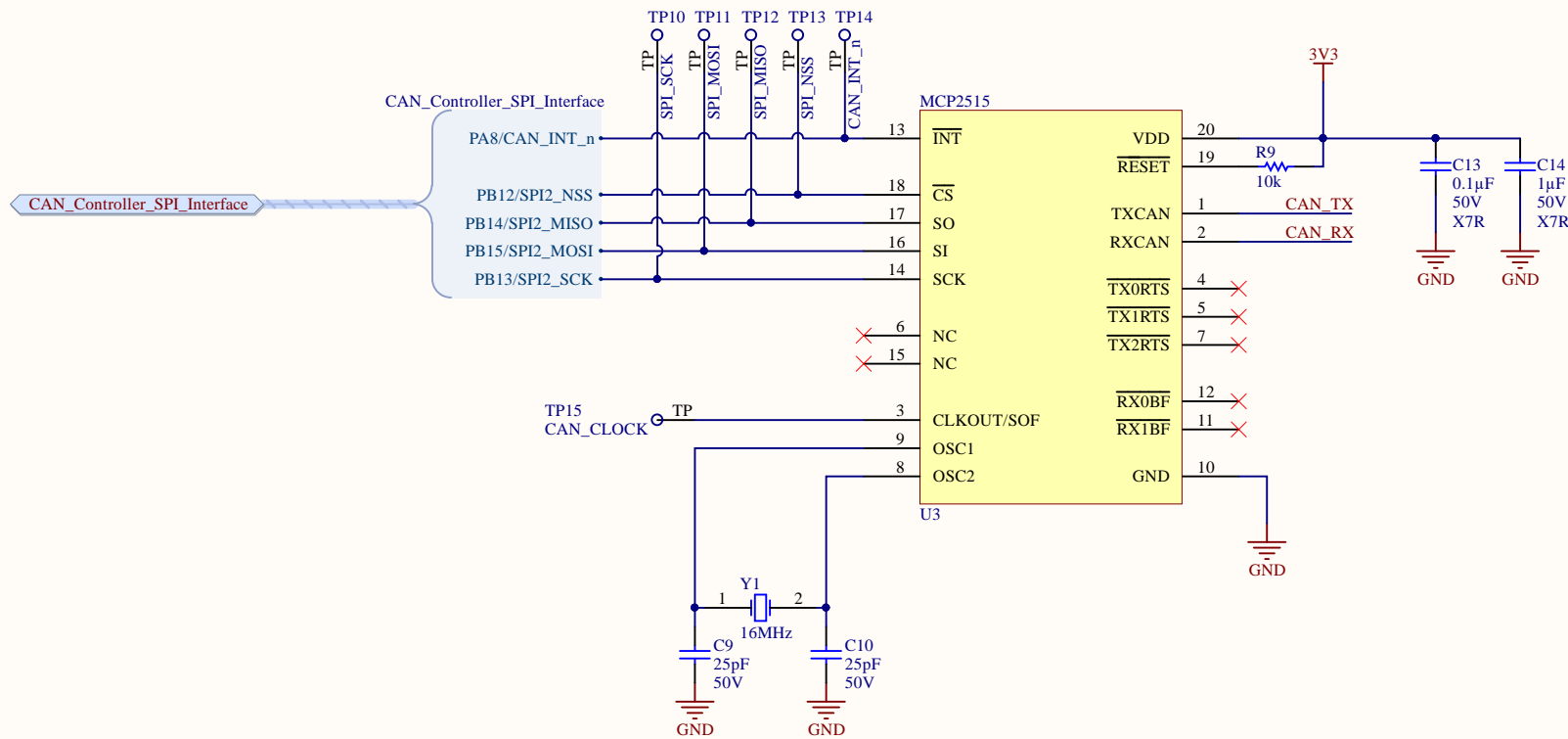
Power Test Points



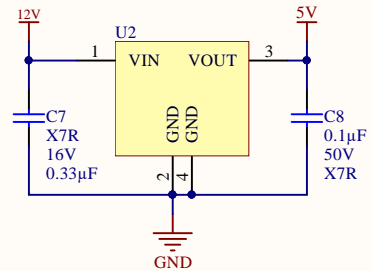
Connectors



CAN Controller



Power Supply



Project: **MSXII_MotorControllerInterface.PrjPcb**

Title: **Slave Controller**

Project Lead: Peiliang Guo

Size: Letter

Date: 2018-06-22

Revision: 1.6

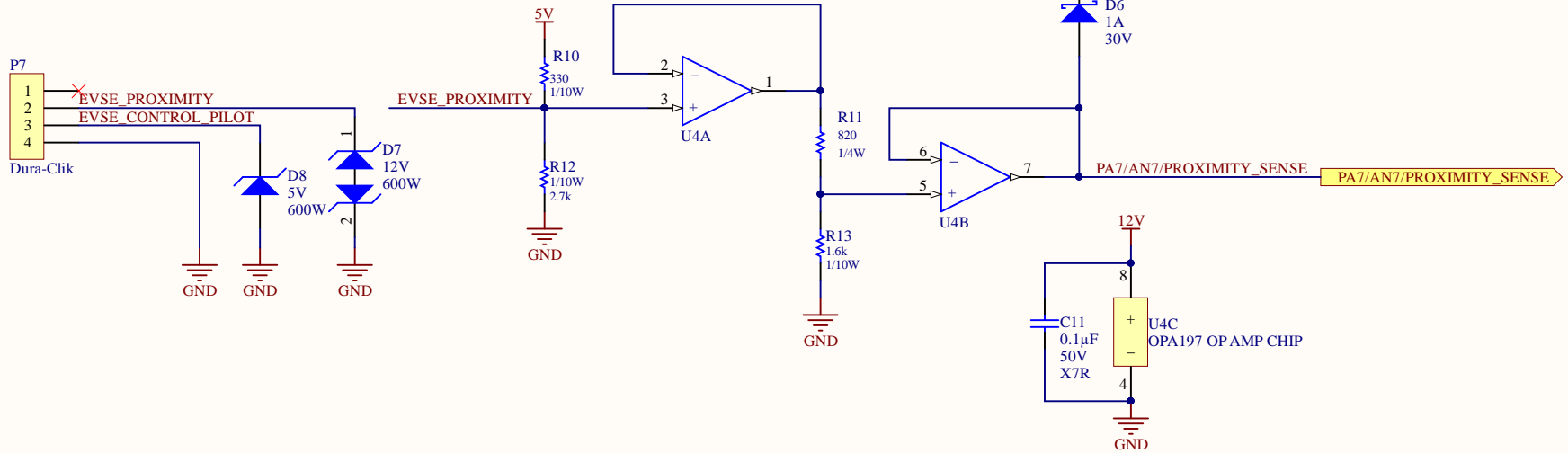
Sheet3 of 3



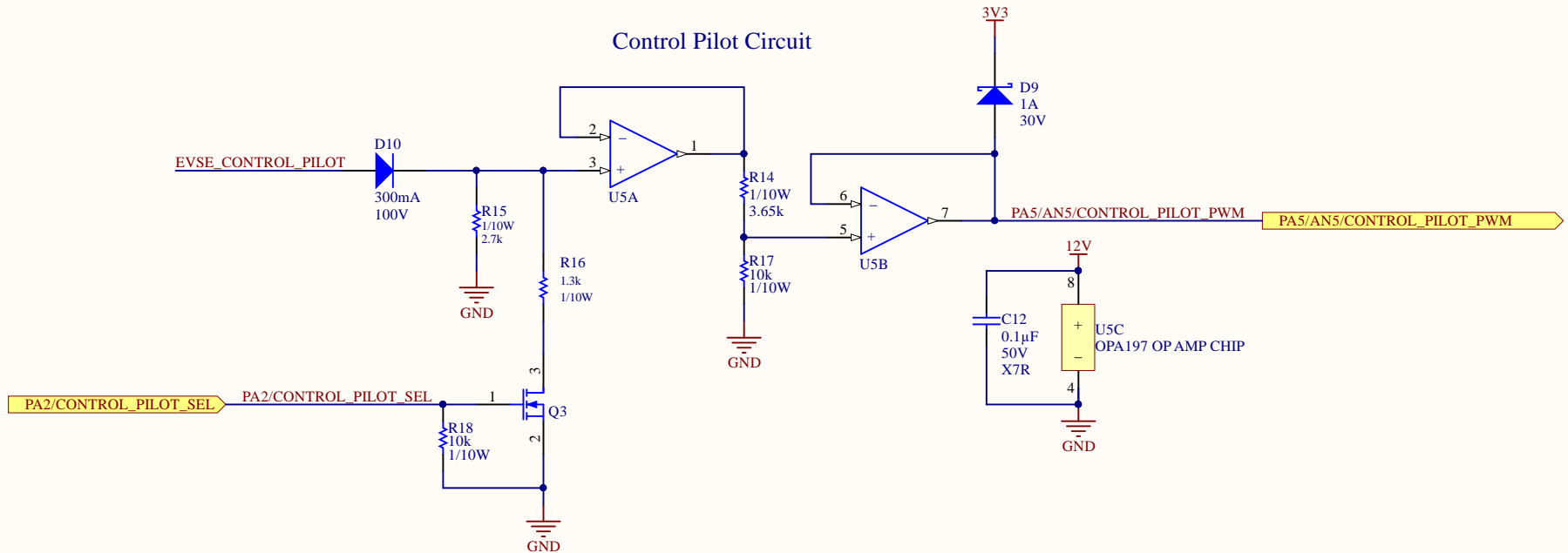
University of Waterloo
200 University Ave W
Waterloo, ON, Canada
N2L 3E9


Website: www.uwmidsun.com

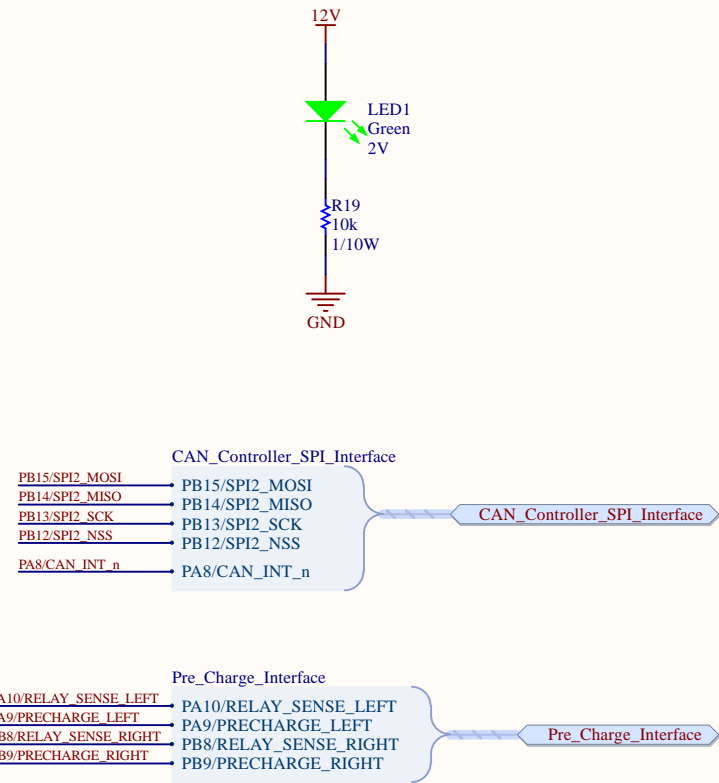
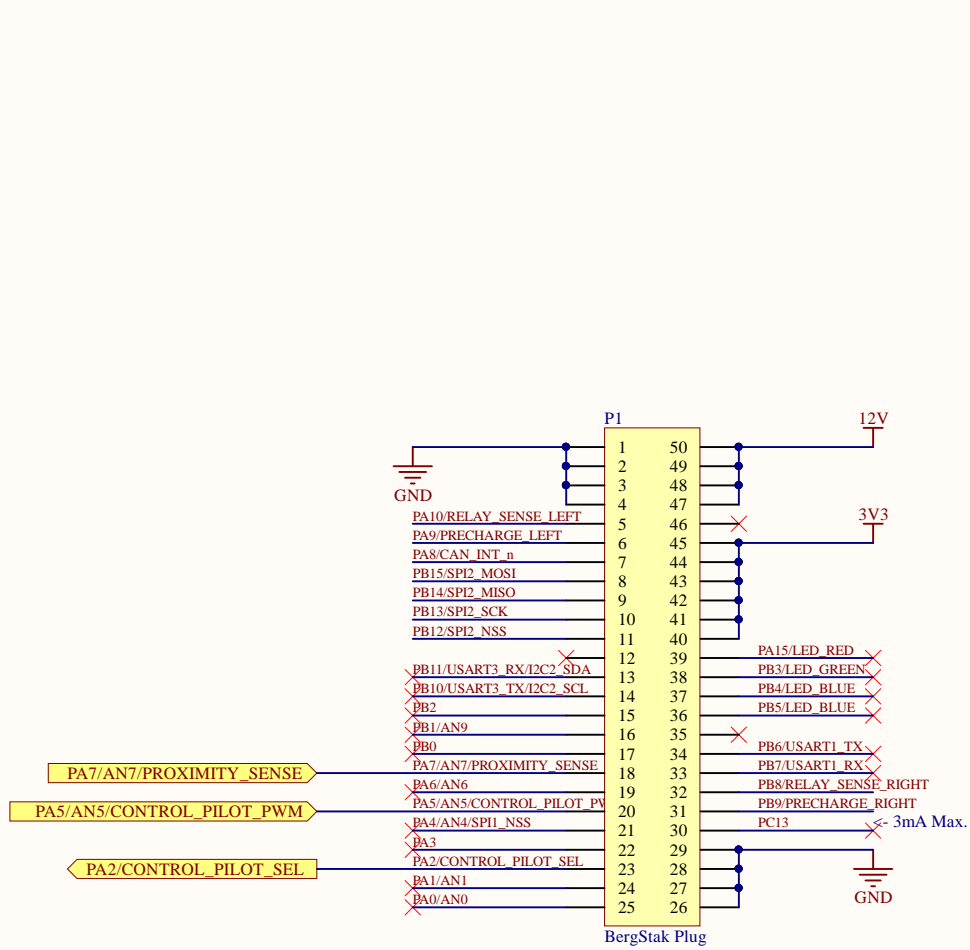
Vehicle Inlet




Control Pilot Circuit

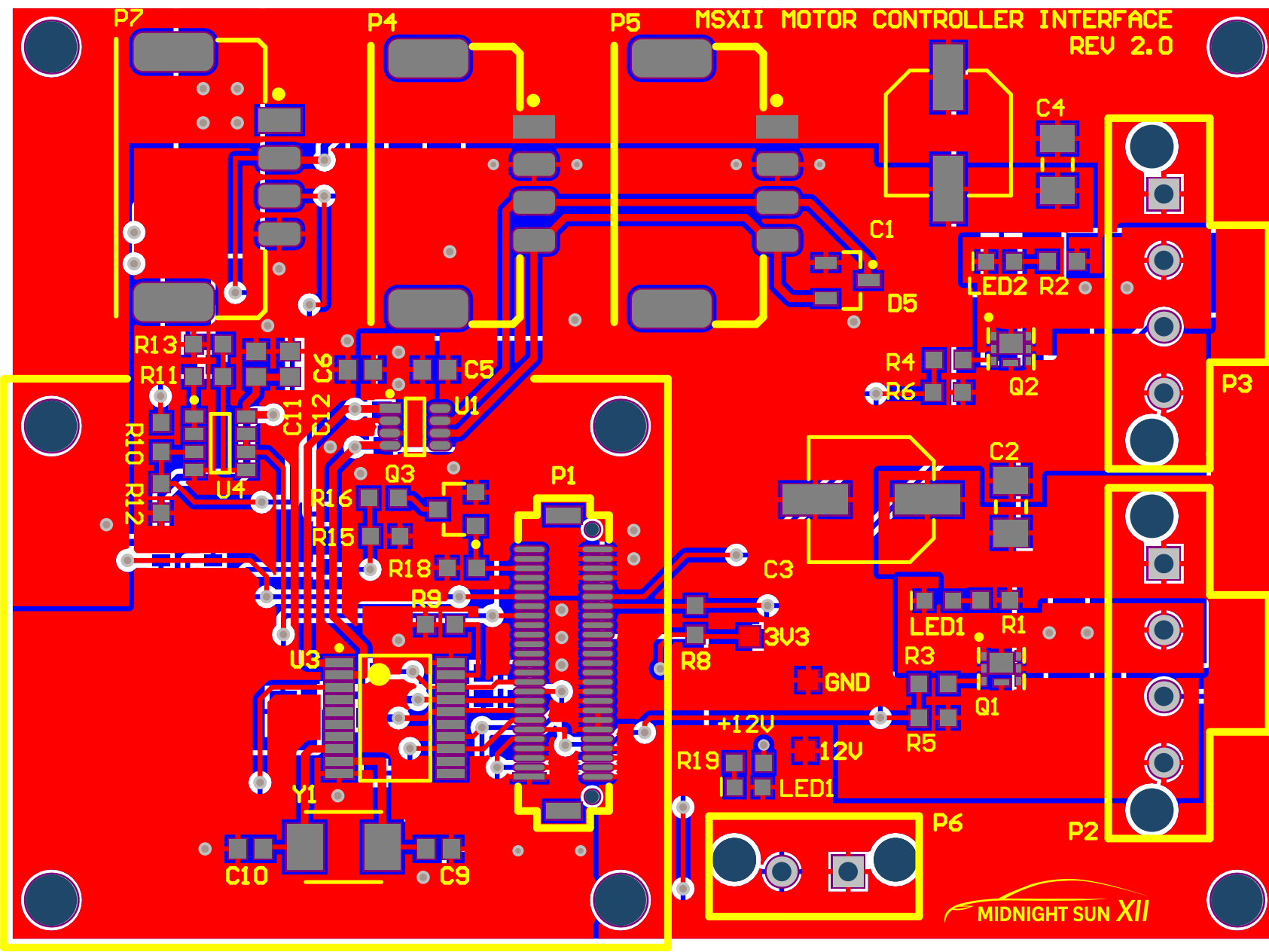


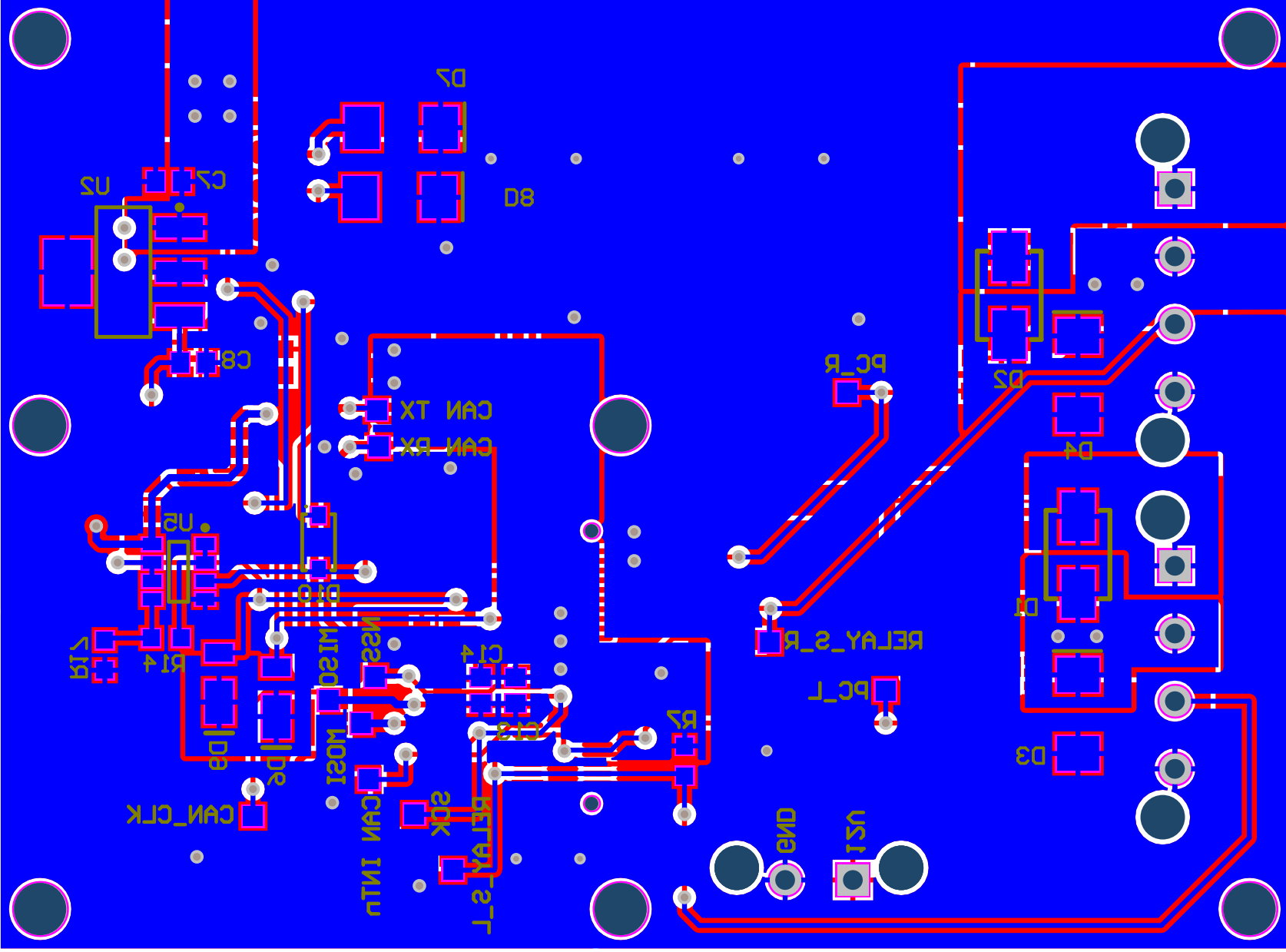
Project: MSXII_MotorControllerInterface.PrjPcb		<div>MIDNIGHTSUN</div>
Title: EVSE Interface & Charger Relay		
Project Author Peiliang Guo		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9 Website: www.uwmidsun.com
Size: Letter	Revision: 1.6	
Date: 2018-06-22	Sheet 3 of 4	



Project: <i>MSXII_MotorControllerInterface.PrjPcb</i>		<div><div>MIDNIGHT</div><div></div><div>SUN</div></div>
Title: *		
Project Author: <i>Peiliang Guo</i>		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: <i>Letter</i>	Revision: <i>1.6</i>	
Date: <i>2018-06-22</i>	Sheet* of *	
		Website: <i>www.uwmidsun.com</i>

MSXII MOTOR CONTROLLER INTERFACE
REV 2.0

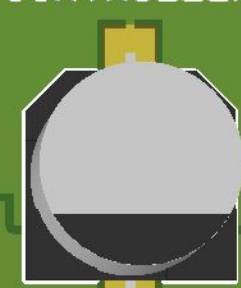
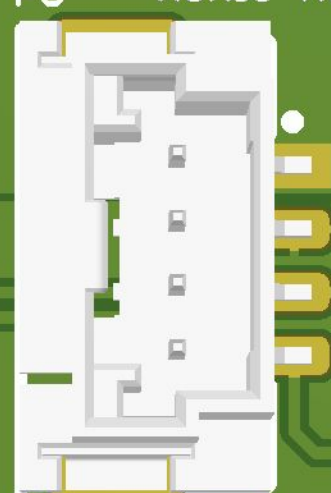
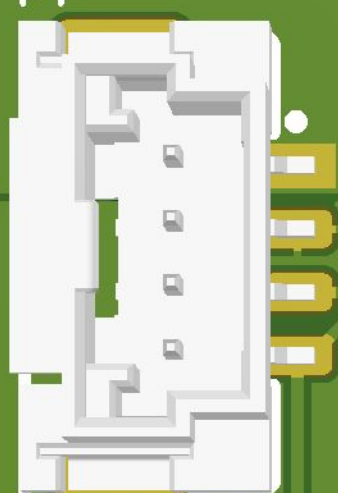
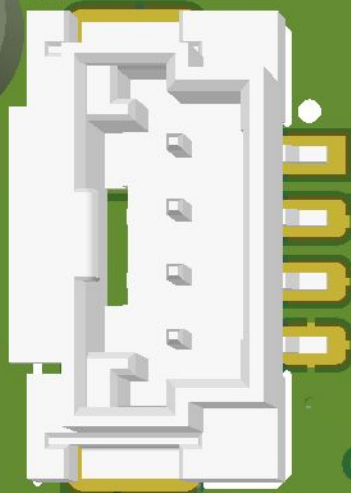




P7

P4

P5

MSXII MOTOR CONTROLLER INTERFACE
REV 2.0

C1

D5



R2

R13

D11

C6

C5

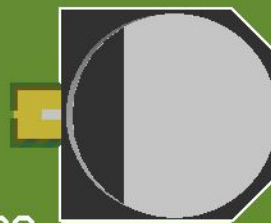
R4

R6

Q2



3



C3

3V3

R8

GND

LED1

R1

R3

Q1

+12V

12V

R19

LED1

R5

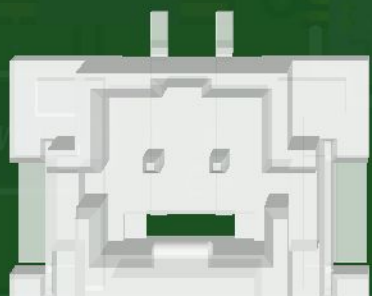
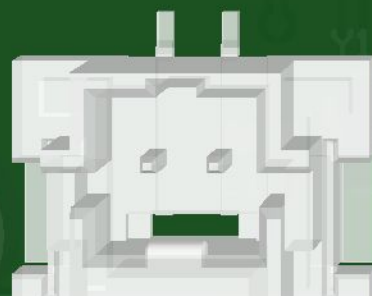
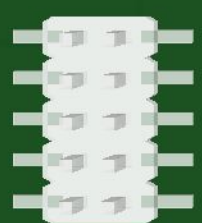


P6

P2



MIDNIGHT SUN XII



Electrical Rules Check Report

Class	Document	Message
Error	Controller_Board_Interface.SchDoc	Duplicate Component Designators LED1 at 4055mil,6350mil and 8055mil,7450mil
Warning	EVSEInterface&ChargerRelay.SchDoc	Net EVSE_PROXIMITY has no driving source (Pin D7-1,Pin P7-2,Pin R10-2,Pin R12-1,Pin U4-3)
Warning	EVSEInterface&ChargerRelay.SchDoc	Net D10_2 has no driving source (Pin D10-2,Pin R15-1,Pin R16-1,Pin U5-3)
Warning	EVSEInterface&ChargerRelay.SchDoc	Net R11_2 has no driving source (Pin R11-2,Pin R13-1,Pin U4-5)
Warning	EVSEInterface&ChargerRelay.SchDoc	Net R14_2 has no driving source (Pin R14-2,Pin R17-1,Pin U5-5)

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII_MotorControllerInterf

Warnings 0

Rule Violations 99

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=2.54mm) (Preferred=0.254mm) (All)	0
Width Constraint (Min=0.381mm) (Max=0.381mm) (Preferred=0.381mm) (InNet('12V'))	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.15mm) (All)	1
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)	48
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	46
Silk to Silk (Clearance=0.254mm) (OnLayer('Bottom Overlay')),(OnLayer('Bottom Overlay'))	0
Silk to Silk (Clearance=0.254mm) (OnLayer('Top Overlay')),(OnLayer('Top Overlay'))	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	4
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	99

Minimum Annular Ring (Minimum=0.15mm) (All)	
Minimum Annular Ring: (0.1mm < 0.15mm) Via (40.05mm,10.681mm) from Top Layer to Bottom Layer (Annular Ring=0.1mm) On (Top Layer)	

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C10-1(13.675mm,5.2mm) on Top Layer And Pad C10-2(12.325mm,5.2mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C11-1(13.284mm,30.079mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C12-1(15.088mm,30.099mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C13-1(27.077mm,14.478mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C14-1(25.273mm,14.478mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C5-1(23.408mm,30.487mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C6-1(18.125mm,30.487mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C7-1(9.819mm,40.112mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C8-1(9.739mm,30.754mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C9-1(22.225mm,5.2mm) on Top Layer And Pad C9-2(23.575mm,5.2mm) on
Minimum Solder Mask Sliver Constraint: (0.246mm < 0.3mm) Between Pad LED1-1(40mm,8.461mm) on Top Layer And Pad R19-2(40.05mm,9.736mm) on
Minimum Solder Mask Sliver Constraint: (0.246mm < 0.3mm) Between Pad LED1-2(38.5mm,8.461mm) on Top Layer And Pad R19-1(38.5mm,9.736mm) on
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(29.5mm,22.8mm) on Top Layer And Pad P1-(31mm,22.05mm) on
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(29.5mm,7.2mm) on Top Layer And Pad P1-(31mm,7.95mm) on Multi-Layer
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-1(51.653mm,15.36mm) on Top Layer And Pad Q1-2(51.653mm,14.71mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-2(51.653mm,14.71mm) on Top Layer And Pad Q1-3(51.653mm,14.06mm)
Minimum Solder Mask Sliver Constraint: (0.275mm < 0.3mm) Between Pad Q1-2(51.653mm,14.71mm) on Top Layer And Pad Q1-8(52.578mm,13.97mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-3(51.653mm,14.06mm) on Top Layer And Pad Q1-7(52.578mm,15.01mm)
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.3mm) Between Pad Q1-3(51.653mm,14.06mm) on Top Layer And Pad Q1-8(52.578mm,13.97mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-4(53.503mm,14.06mm) on Top Layer And Pad Q1-5(53.503mm,14.71mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-4(53.503mm,14.06mm) on Top Layer And Pad Q1-7(52.578mm,15.01mm)
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.3mm) Between Pad Q1-4(53.503mm,14.06mm) on Top Layer And Pad Q1-8(52.578mm,13.97mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-5(53.503mm,14.71mm) on Top Layer And Pad Q1-6(53.503mm,15.36mm)
Minimum Solder Mask Sliver Constraint: (0.275mm < 0.3mm) Between Pad Q1-5(53.503mm,14.71mm) on Top Layer And Pad Q1-8(52.578mm,13.97mm)
Minimum Solder Mask Sliver Constraint: (0.187mm < 0.3mm) Between Pad Q1-7(52.578mm,15.01mm) on Top Layer And Pad Q1-8(52.578mm,13.97mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q2-1(52.161mm,32.227mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q2-2(52.161mm,31.577mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.275mm < 0.3mm) Between Pad Q2-2(52.161mm,31.577mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q2-3(52.161mm,30.927mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.3mm) Between Pad Q2-3(52.161mm,30.927mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q2-4(54.011mm,30.927mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q2-4(54.011mm,30.927mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.3mm) Between Pad Q2-4(54.011mm,30.927mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q2-5(54.011mm,31.577mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.275mm < 0.3mm) Between Pad Q2-5(54.011mm,31.577mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.187mm < 0.3mm) Between Pad Q2-7(53.086mm,31.877mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U4-1(10.025mm,28.025mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U4-2(10.025mm,27.075mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U4-3(10.025mm,26.125mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U4-5(12.775mm,25.175mm) on Top Layer And Pad
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Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U4-7(12.775mm,27.075mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U5-1(11.027mm,21.364mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U5-2(11.027mm,20.414mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U5-3(11.027mm,19.464mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U5-5(8.277mm,18.514mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U5-6(8.277mm,19.464mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U5-7(8.277mm,20.414mm) on Bottom Layer And Pad

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D1-1(56.134mm,18.796mm) on Bottom Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D1-1(56.134mm,18.796mm) on Bottom Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D1-2(56.134mm,22.796mm) on Bottom Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D1-2(56.134mm,22.796mm) on Bottom Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D2-1(52.582mm,32.2mm) on Bottom Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D2-1(52.582mm,32.2mm) on Bottom Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D2-2(52.582mm,36.2mm) on Bottom Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D2-2(52.582mm,36.2mm) on Bottom Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad P1-1(27.7mm,9mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad P1-25(27.7mm,21mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.158mm < 0.178mm) Between Pad P1-26(31.3mm,21mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad P1-50(31.3mm,9mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad P4-4(27.95mm,37.3mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad P4-7(22.37mm,33.7mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.107mm < 0.178mm) Between Pad P4-7(22.37mm,46.9mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad P5-4(40.78mm,37.3mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad P5-7(35.2mm,33.7mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.107mm < 0.178mm) Between Pad P5-7(35.2mm,46.9mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.155mm < 0.178mm) Between Pad P7-7(8.941mm,34.036mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.17mm < 0.178mm) Between Pad P7-7(8.941mm,47.236mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q1-1(51.653mm,15.36mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q1-2(51.653mm,14.71mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q1-2(51.653mm,14.71mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q1-3(51.653mm,14.06mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q1-4(53.503mm,14.06mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q1-5(53.503mm,14.71mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q1-5(53.503mm,14.71mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q1-6(53.503mm,15.36mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q2-1(52.161mm,32.227mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q2-2(52.161mm,31.577mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q2-2(52.161mm,31.577mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q2-3(52.161mm,30.927mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q2-4(54.011mm,30.927mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q2-5(54.011mm,31.577mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q2-5(54.011mm,31.577mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q2-6(54.011mm,32.227mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q3-1(24.876mm,22.214mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q3-2(24.876mm,24.014mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U1-1(20.341mm,28.432mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U1-2(20.341mm,27.782mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U1-3(20.341mm,27.132mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U1-4(20.341mm,26.482mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U1-5(22.991mm,26.482mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U1-6(22.991mm,27.132mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U1-7(22.991mm,27.782mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U1-8(22.991mm,28.432mm) on Top Layer And Track	

Board Clearance Constraint (Gap=0mm) (All)	
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,0mm)(0mm,30mm) on Top Overlay	
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,0mm)(35mm,0mm) on Top Overlay	
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,30mm)(6.5mm,30mm) on Top Overlay	
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (35mm,0mm)(35mm,15.6mm) on Top Overlay	