

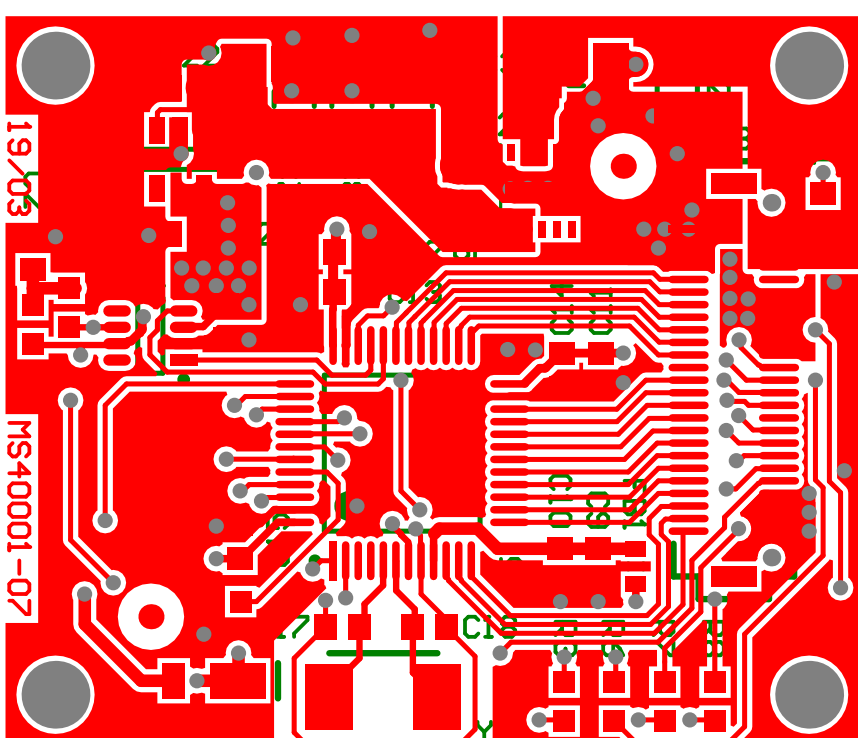
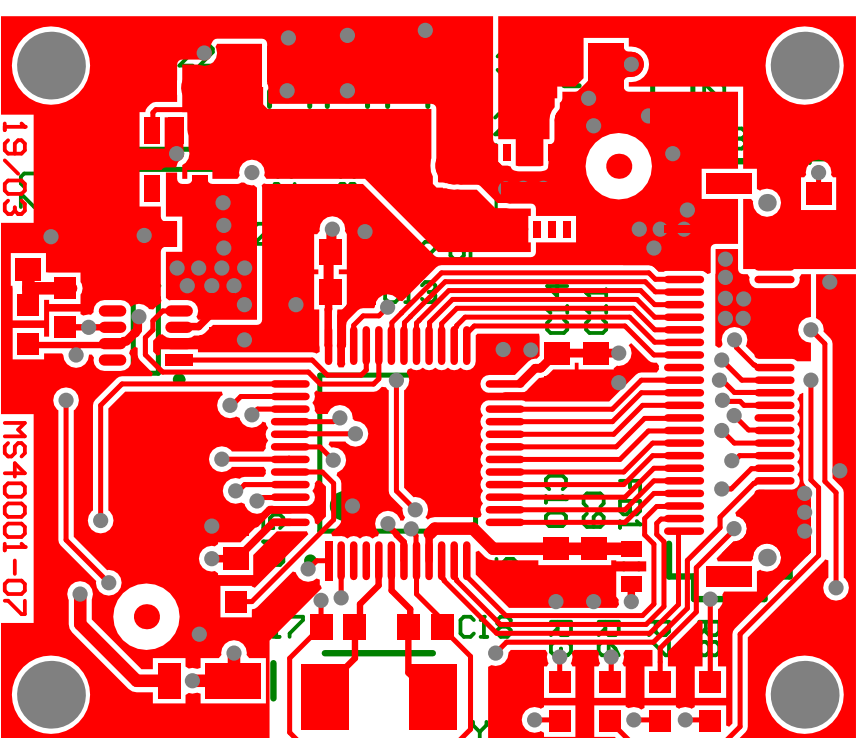
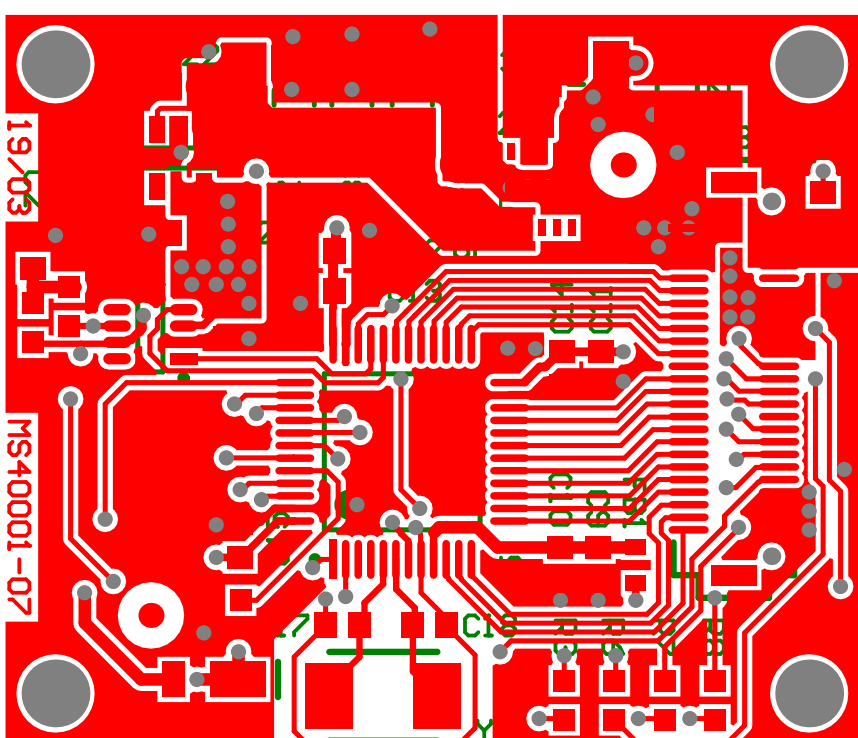
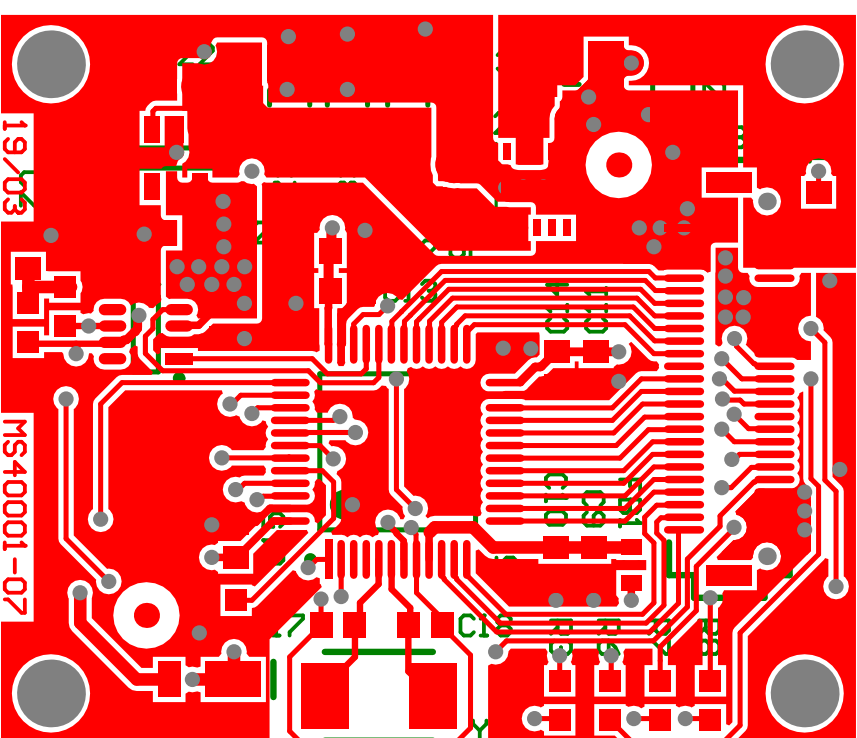
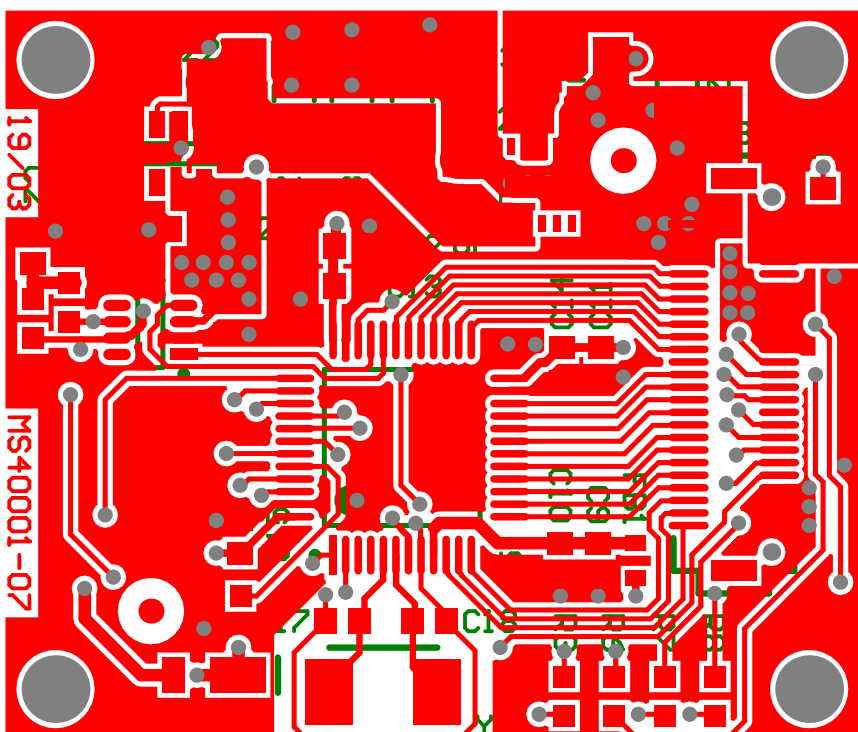
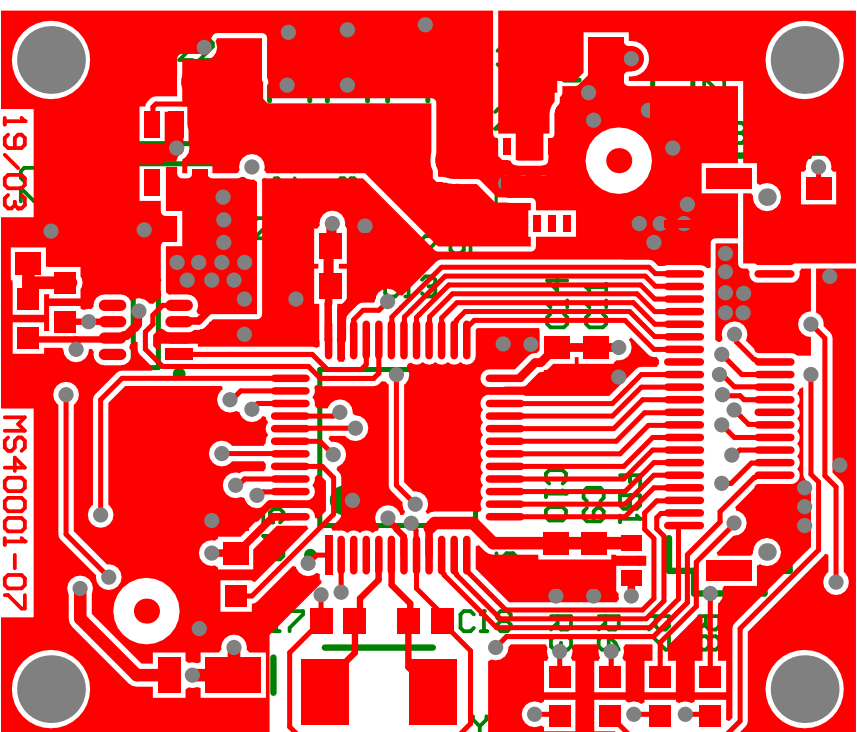
PROJECT	Controller_Board.PrjPcb	
DOCUMENT	Controller Board - Power & CAN	
PART NUMBER	MS40001-07	VARIANT [No Variations]
DRAWN BY	Taiping Li	REVISION 7.0
LAST MODIFIED	2020-01-16	SHEET 3 OF 3

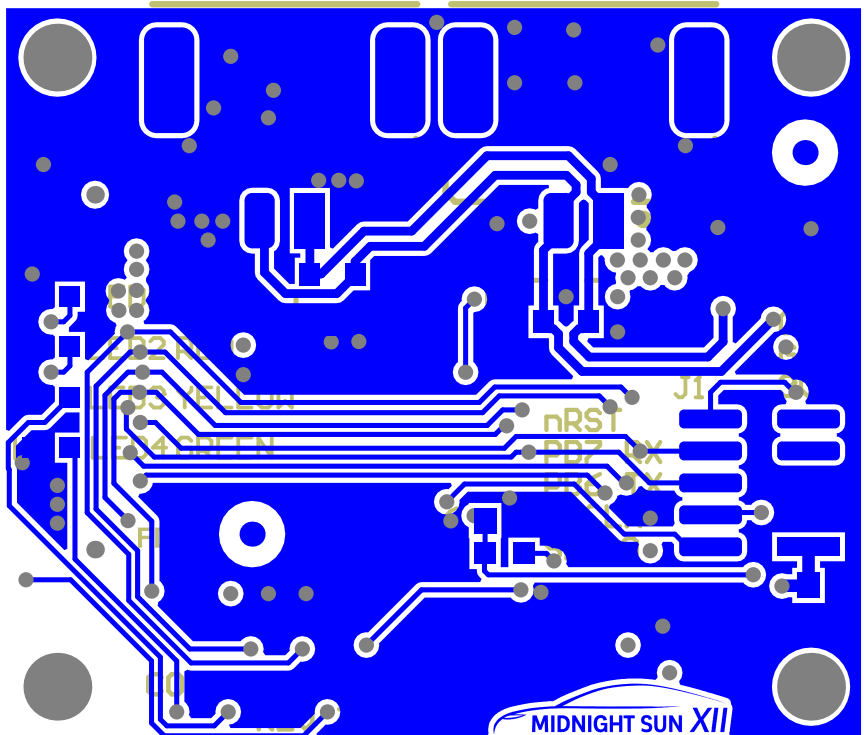
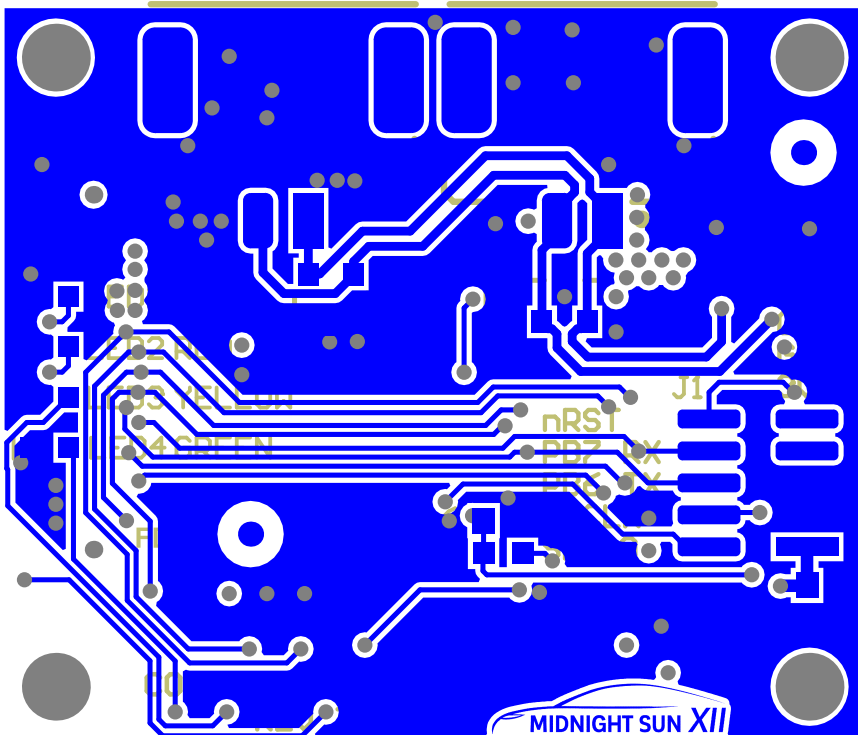
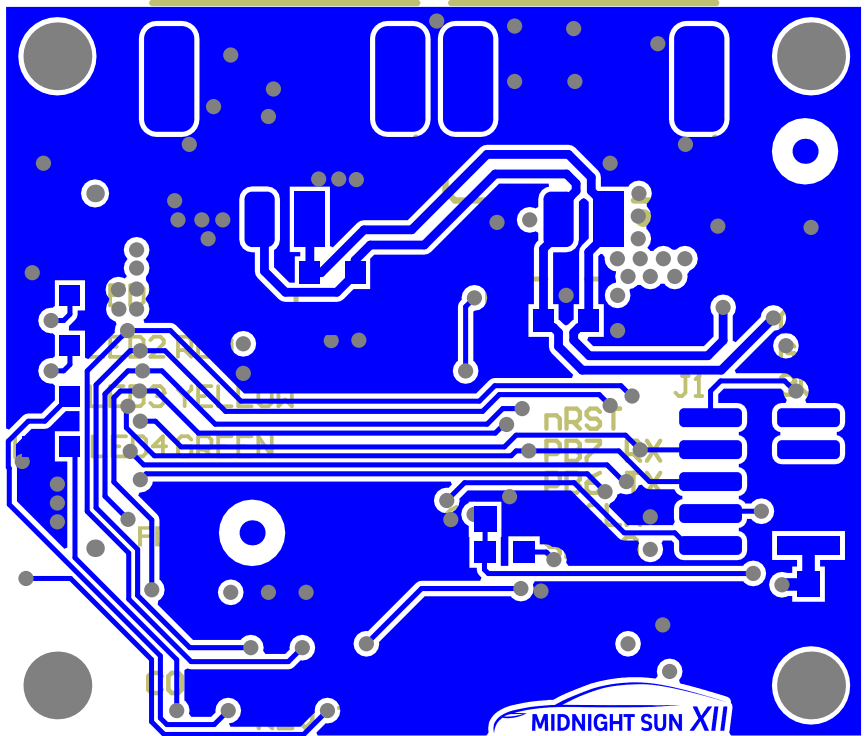
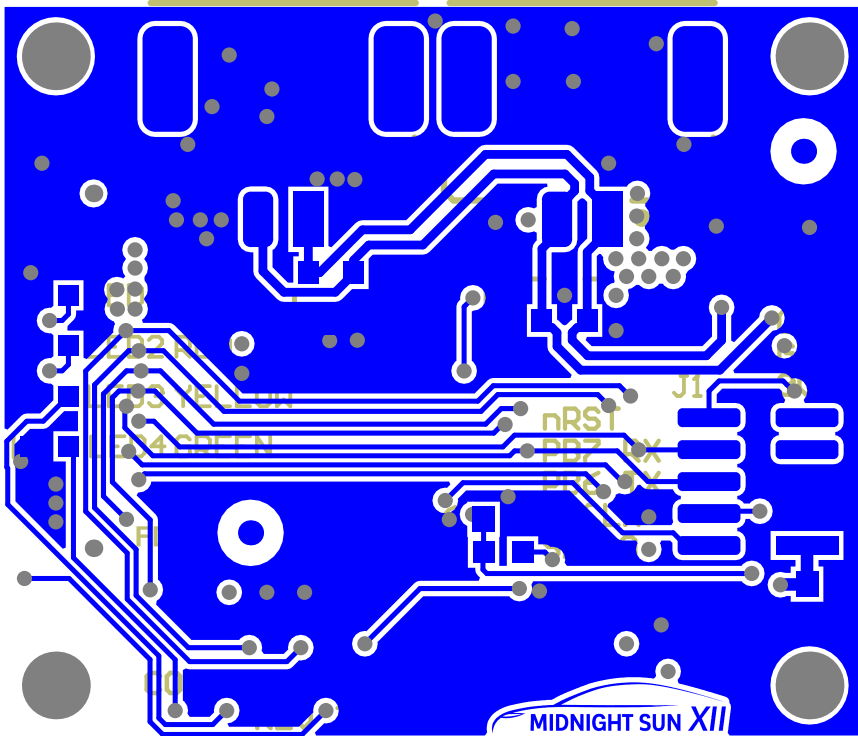
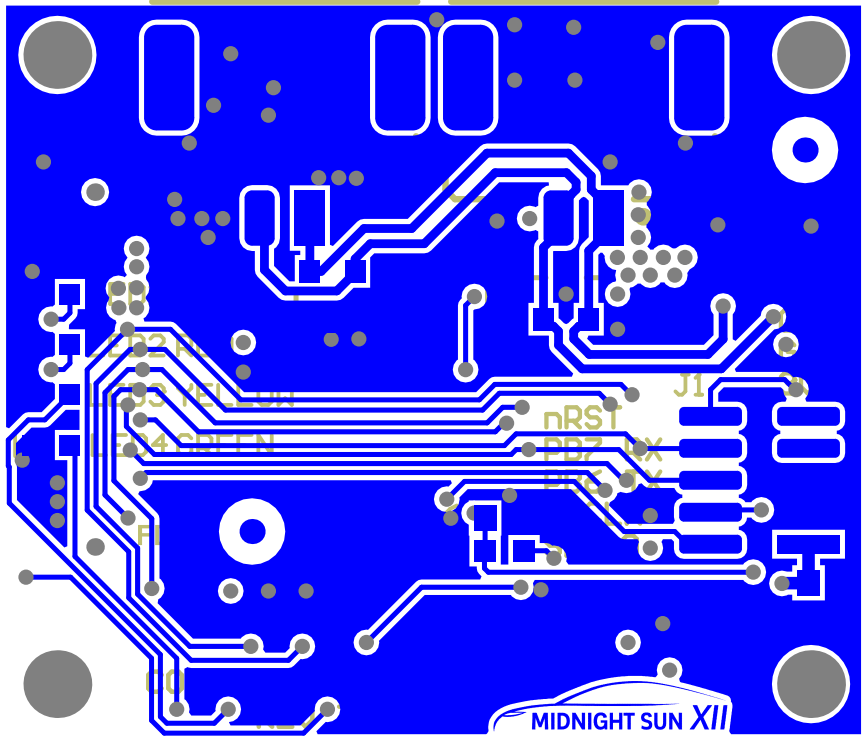
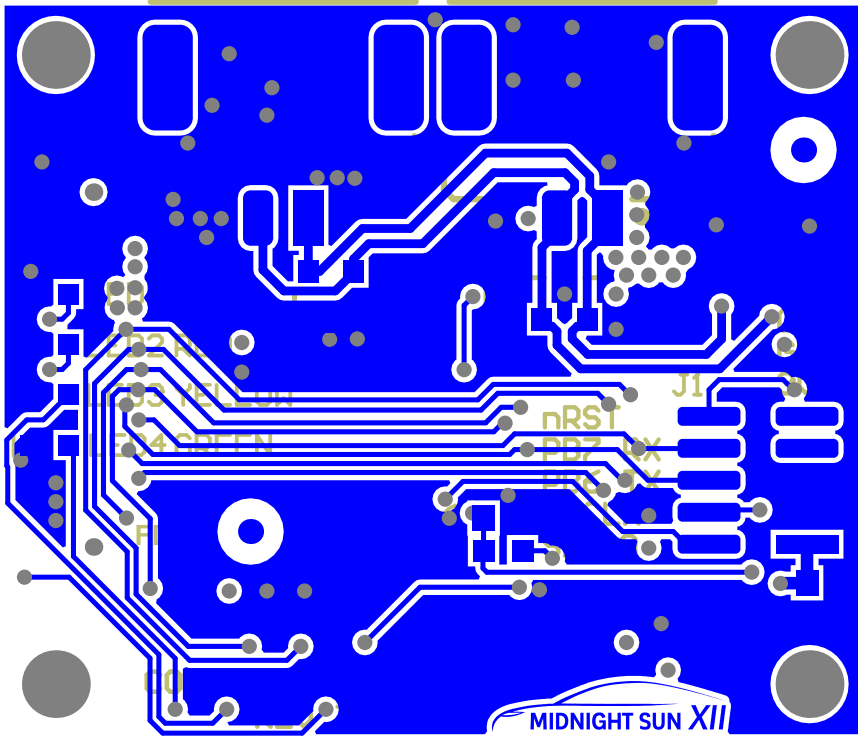
MIDNIGHT

SUN

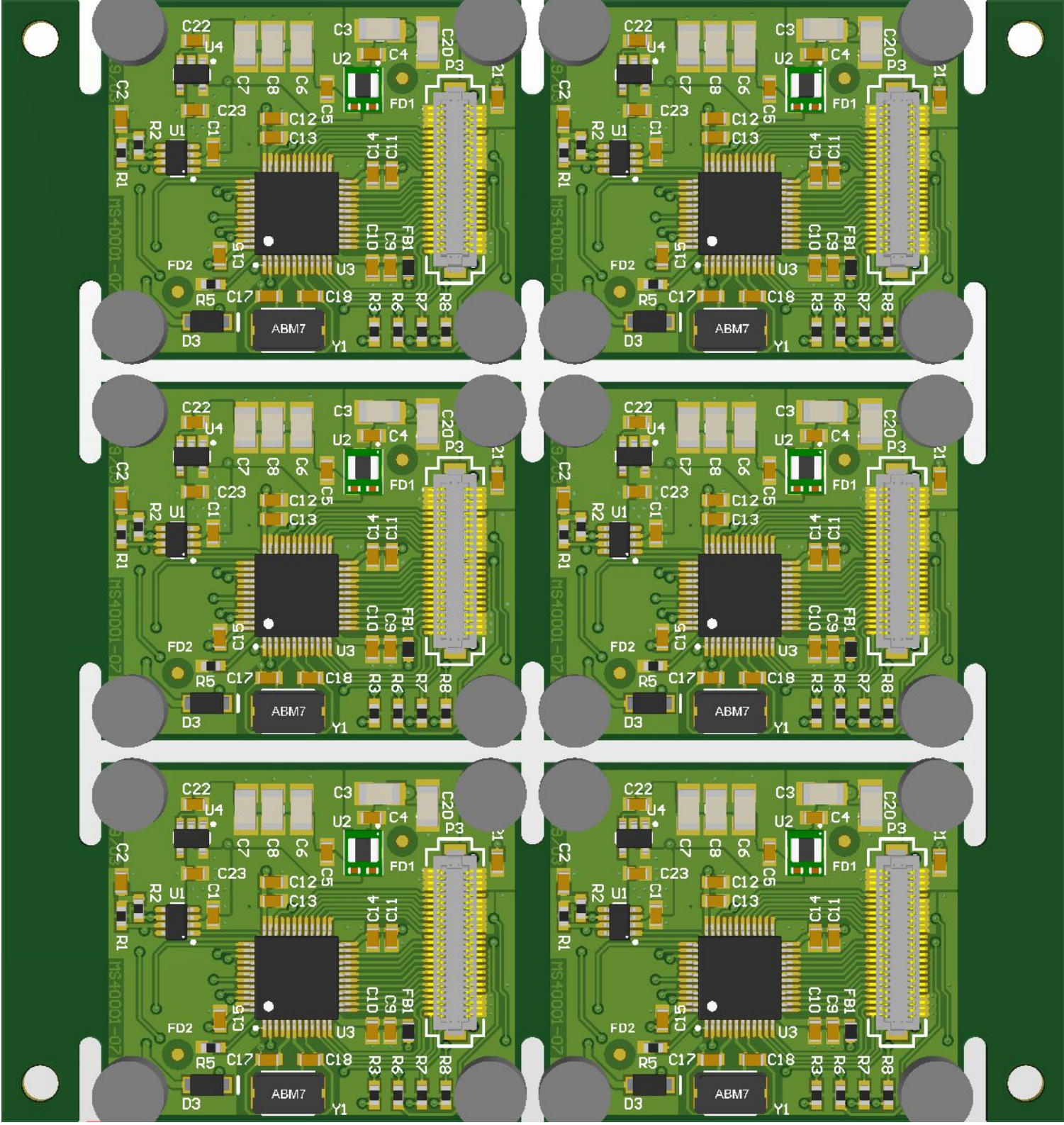
Engineering 5 - 1002  
University of Waterloo  
(519) 888-4567 x32978  
hardware@uwmidsun.com

Comment	Description	Designator	Footprint	LibRef	Quantity	Supplier 1	Supplier Part Number 1	Manufacturer 1	Manufacturer Part Number	Manufacturer Part Number 1
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## Design Rules Verification Report

Filename : C:\Users\Aashmika Mali\Documents\First Year\Midnight Sun\hardware\MSXII\_

Warnings 0  
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (not HasFootprint('FIDUCIAL')), (All)	0
Clearance Constraint (Gap=0mm) (HasFootprint('FIDUCIAL')), (HasFootprint('FIDUCIAL'))	0
Short-Circuit Constraint (Allowed=No) (All), (All)	0
Un-Routed Net Constraint ( (All) )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=5mm) (Preferred=0.2mm) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0mm) (Conductor Width=0.254mm) (Air Gap=0.254mm,	0
Hole Size Constraint (Min=0.025mm) (Max=3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All), (All)	0
Minimum Solder Mask Sliver (Gap=0mm) (All), (All)	0
Silk To Solder Mask (Clearance=0.15mm) (IsPad), (All)	0
Silk to Silk (Clearance=0.15mm) (All), (All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	0