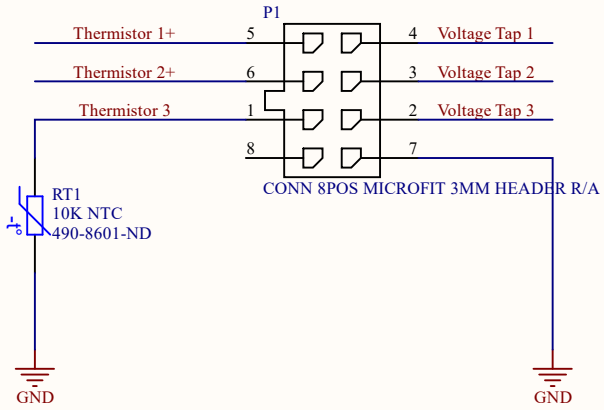
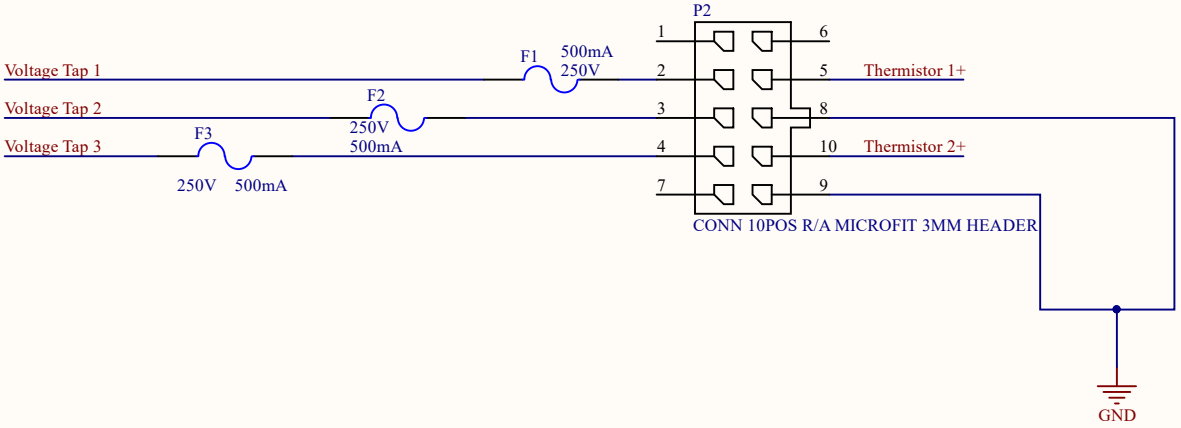


switched the pin designators on this so it would be cleaner to trace



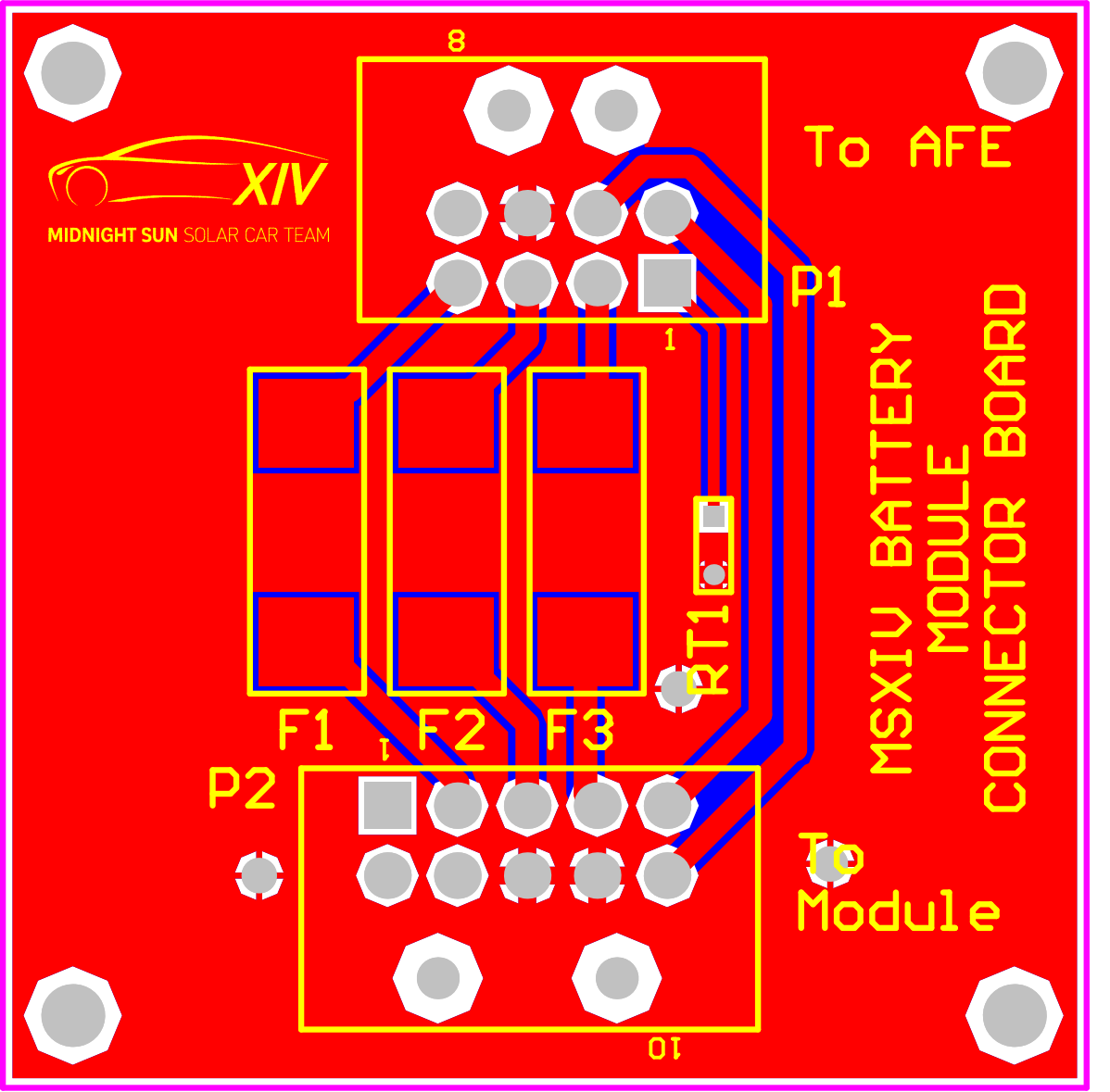
switched the pin designators on this so it would be cleaner to trace

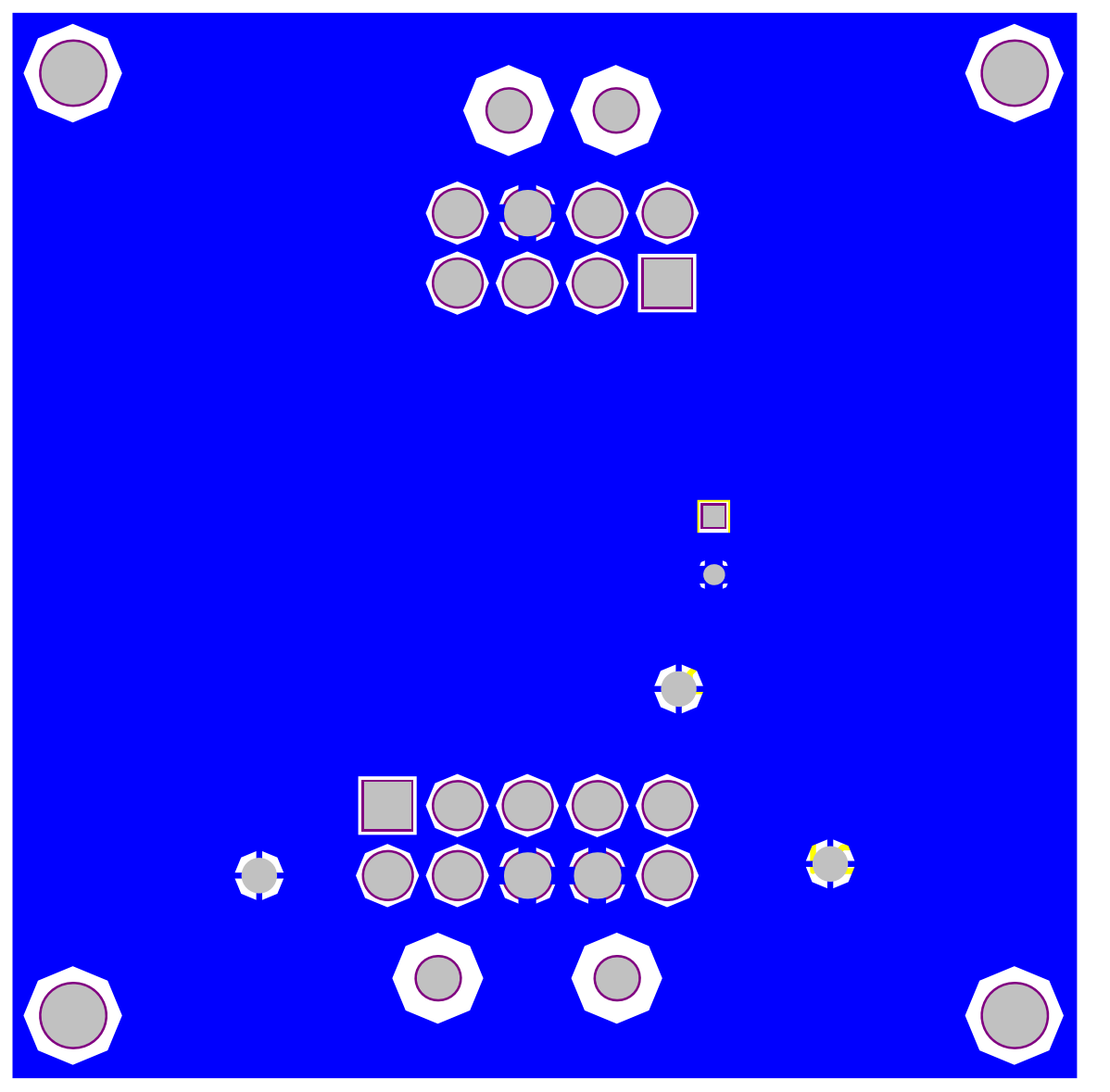
Project: MSXIV_BatteryModuleConnectorBoard.PrjPcb		MIDNIGHT SUN
Title: *		
Project Author: Aashmika Mali		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.0	
Date: 2019-09-15	Sheet* of *	Website: uwmidsun.com

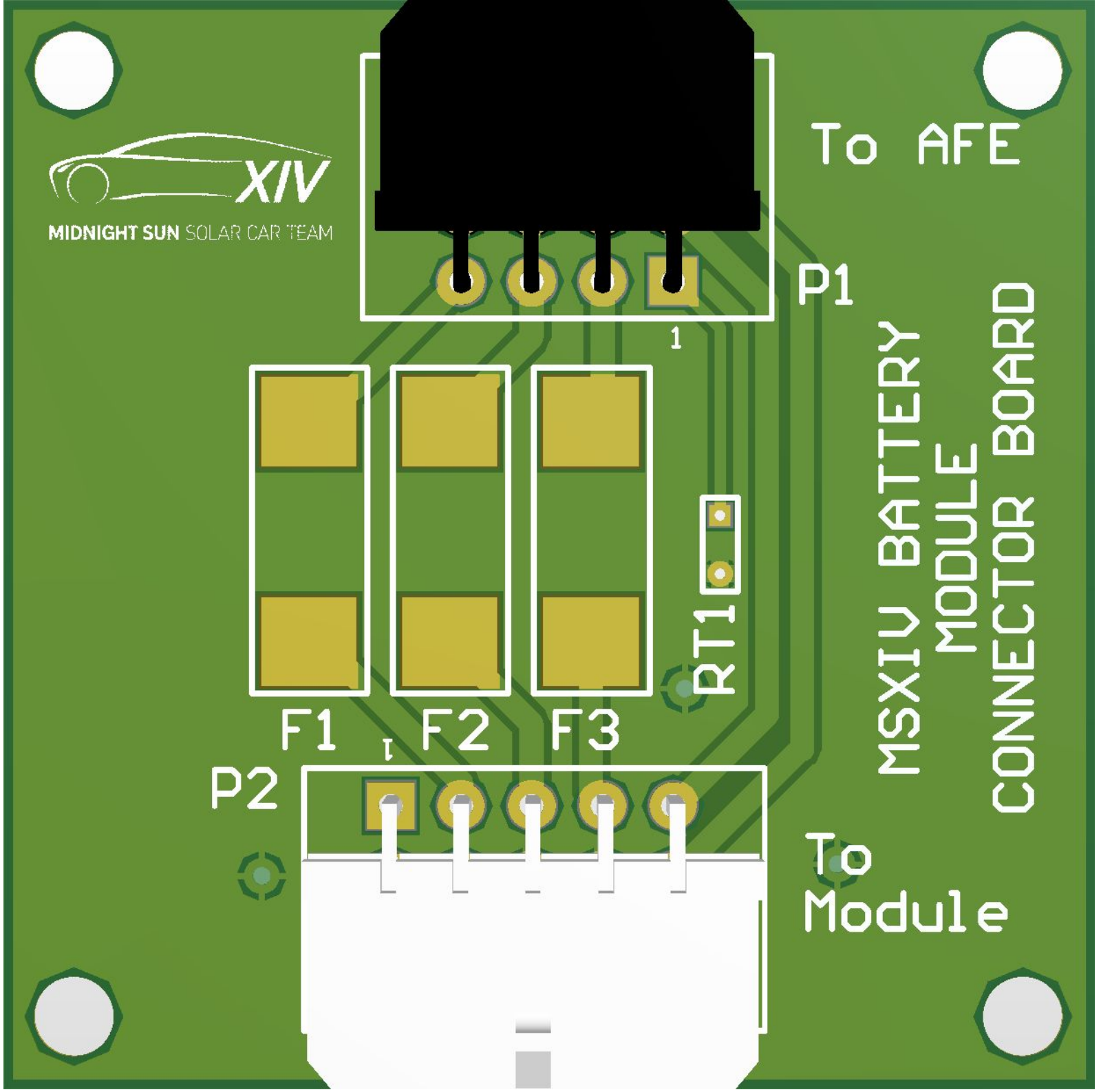
Bill of Materials

Project:	MV_BatteryModuleConnectorBoard.PrjPcb
Revision:	1.0
Project Lead:	Aashmika Mali
Generated On:	2019-09-15 4:50 PM
Production Quantity:	1
Currency	USD
Total Parts Count:	6

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Pric
FUSE SMT 3912 FAST 250V 500MA	F1, F2, F3		0678D0500-02	Digi-Key	507-2256-1-ND	
CONN 8POS MICROFIT 3MM HEADER R/A	P1	Molex	0430450800	Digi-Key	WM1816-ND	
CONN 10POS R/A MICROFIT 3MM HEADER	P2	Molex	0430451000	Digi-Key	WM1817-ND	
NTC THERMISTOR 10K 1% BEAD	RT1			Digi-Key	490-8601-ND	


XIV
MIDNIGHT SUN SOLAR CAR TEAM
8
To AFE
P1
1
MSXIV BATTERY MODULE CONNECTOR BOARD
RT1
F1
F2
F3
P2
1
To Module
10




XIV
MIDNIGHT SUN SOLAR CAR TEAM
To AFE
P1
1
MSXIV BATTERY MODULE CONNECTOR BOARD
RT1
F1
F2
F3
P2
1
To Module

Electrical Rules Check Report

Class	Document	Message
Warning	MSXIV_BatteryModuleConnectorBoard.SchDoc	Off grid Net Label Thermistor 1+ at 5980.115mil,4500mil
Warning	MSXIV_BatteryModuleConnectorBoard.SchDoc	Off grid Net Label Thermistor 2+ at 5980.115mil,4100mil
Warning	MSXIV_BatteryModuleConnectorBoard.SchDoc	Off grid Net Label Thermistor 3 at 4131.041mil,6900mil

Design Rules Verification Report

Filename : C:\Users\Aashmika Mali\Documents\First Year\Midnight Sun\hardware\MSXIV_BatteryModuleConnectorBoard\MSXIV_BatteryModul

Warnings
Rule Violations 2

Warnings	
Total	

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	
Short-Circuit Constraint (Allowed=No) (All),(All)	
Un-Routed Net Constraint ((All))	
Modified Polygon (Allow modified: No), (Allow shelved: No)	
Width Constraint (Min=10mil) (Max=100mil) (Preferred=10mil) (All)	
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	
Hole To Hole Clearance (Gap=10mil) (All),(All)	
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	1
Silk to Silk (Clearance=10mil) (All),(All)	
Net Antennae (Tolerance=0mil) (All)	
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	
Total	2

Hole Size Constraint (Min=1mil) (Max=100mil) (All)
Hole Size Constraint: (133.858mil > 100mil) Pad Free-(0mil,0mil) on Multi-Layer Actual Hole Size = 133.858mil
Hole Size Constraint: (133.858mil > 100mil) Pad Free-(0mil,1590.551mil) on Multi-Layer Actual Hole Size = 133.858mil
Hole Size Constraint: (133.858mil > 100mil) Pad Free-(1590.551mil,0mil) on Multi-Layer Actual Hole Size = 133.858mil
Hole Size Constraint: (133.858mil > 100mil) Pad Free-(1590.551mil,1590.551mil) on Multi-Layer Actual Hole Size = 133.858mil
Hole Size Constraint: (122.047mil > 100mil) Pad P1-(736.221mil,1527.559mil) on Multi-Layer Actual Hole Size = 122.047mil
Hole Size Constraint: (122.047mil > 100mil) Pad P1-(917.323mil,1527.559mil) on Multi-Layer Actual Hole Size = 122.047mil
Hole Size Constraint: (122.047mil > 100mil) Pad P2-(616.535mil,62.992mil) on Multi-Layer Actual Hole Size = 122.047mil
Hole Size Constraint: (122.047mil > 100mil) Pad P2-(918.898mil,62.992mil) on Multi-Layer Actual Hole Size = 122.047mil

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (9.567mil < 10mil) Between Pad F1-1(393.701mil,1000mil) on Top Layer And Track (299.213mil,543.307mil)(299.213mil,1090.551mil) on Top Overlay [Top Overlay] to [Top Sold
Silk To Solder Mask Clearance Constraint: (9.567mil < 10mil) Between Pad F1-2(393.701mil,629.921mil) on Top Layer And Track (299.213mil,543.307mil)(299.213mil,1090.551mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.614mil < 10mil) Between Pad F1-2(393.701mil,629.921mil) on Top Layer And Track (299.213mil,543.307mil)(492.126mil,543.307mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.567mil < 10mil) Between Pad F2-1(629.921mil,1000mil) on Top Layer And Track (535.433mil,543.307mil)(535.433mil,1090.551mil) on Top Overlay [Top Overlay] to [Top Sold
Silk To Solder Mask Clearance Constraint: (9.567mil < 10mil) Between Pad F2-2(629.921mil,629.921mil) on Top Layer And Track (535.433mil,543.307mil)(535.433mil,1090.551mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.614mil < 10mil) Between Pad F2-2(629.921mil,629.921mil) on Top Layer And Track (535.433mil,543.307mil)(728.346mil,543.307mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (9.567mil < 10mil) Between Pad F3-1(866.142mil,1000mil) on Top Layer And Track (771.654mil,543.307mil)(771.654mil,1090.551mil) on Top Overlay [Top Overlay] to [Top Sold
Silk To Solder Mask Clearance Constraint: (9.567mil < 10mil) Between Pad F3-2(866.142mil,629.921mil) on Top Layer And Track (771.654mil,543.307mil)(771.654mil,1090.551mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.614mil < 10mil) Between Pad F3-2(866.142mil,629.921mil) on Top Layer And Track (771.654mil,543.307mil)(964.567mil,543.307mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1082.677mil,842.52mil) on Multi-Layer And Track (1053.15mil,714.567mil)(1053.15mil,872.047mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1082.677mil,842.52mil) on Multi-Layer And Track (1053.15mil,872.047mil)(1112.205mil,872.047mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1082.677mil,842.52mil) on Multi-Layer And Track (1112.205mil,714.567mil)(1112.205mil,872.047mil) on Top Overlay [Top Overlay] to [T
Silk To Solder Mask Clearance Constraint: (9.941mil < 10mil) Between Pad RT1-2(1082.677mil,744.095mil) on Multi-Layer And Track (1053.15mil,714.567mil)(1053.15mil,872.047mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (8.833mil < 10mil) Between Pad RT1-2(1082.677mil,744.095mil) on Multi-Layer And Track (1053.15mil,714.567mil)(1112.205mil,714.567mil) on Top Overlay [Top Overlay] to [T
Silk To Solder Mask Clearance Constraint: (9.941mil < 10mil) Between Pad RT1-2(1082.677mil,744.095mil) on Multi-Layer And Track (1112.205mil,714.567mil)(1112.205mil,872.047mil) on Top Overlay [Top Overlay] to [T

Silk to Silk (Clearance=10mil) (All),(All)
Silk To Silk Clearance Constraint: (7.806mil < 10mil) Between Text "1" (1003.937mil,1125.984mil) on Top Overlay And Track (484.252mil,1173.228mil)(1169.291mil,1173.228mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (7.806mil < 10mil) Between Text "1" (531.496mil,464.567mil) on Top Overlay And Track (385.827mil,417.323mil)(1157.48mil,417.323mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "10" (1023.622mil,-39.37mil) on Top Overlay And Track (385.827mil,-23.622mil)(1157.48mil,-23.622mil) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "8" (637.795mil,1629.921mil) on Top Overlay And Track (484.252mil,1614.173mil)(1169.291mil,1614.173mil) on Top Overlay Silk Text to Silk Clearance