



# GW1NR series of FPGA Products

## **Data Sheet**

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## Revision History

Date	Version	Description
06/06/2018	1.6E	Initial version published.
06/25/2018	1.7E	<ul style="list-style-type: none"><li>● The PLL structure view updated. The input clock is CLKIN;</li><li>● MG81 package content added;</li><li>● PSRAM description and electrical characteristics added.</li></ul>
08/01/2018	1.8E	The systemIO status for blank chips added.
09/25/2018	1.9E	PSRAM description modified and PSRAM data width added.
12/13/2018	2.0E	<ul style="list-style-type: none"><li>● The recommended working conditions updated;</li><li>● The package and the memory table added;</li><li>● The device of GW1NR-4B added;</li><li>● The step delay of IODELAY changed from 25ps to 30ps</li><li>● The part name updated.</li></ul>
01/09/2019	2.1E	<ul style="list-style-type: none"><li>● Oscillator frequency updated;</li><li>● QN88 of GW1NR-4 embedded with PSRAM added;</li><li>● Reference manuals of SDRAM and PSRAM updated.</li></ul>

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# 1 About This Guide

## 1.1 Purpose

This data sheet describes the features, product resources and structure, AC/DC characteristics, timing specifications of the configuration interface, and the ordering information of the GW1NR series of FPGA product. It is designed to help you understand the GW1NR series of FPGA products quickly and select and use devices appropriately.

## 1.2 Supported Products

The information in this guide applies to the following products:

GW1NR series of FPGA products: GW1NR-4, GW1NR-4B, GW1NR-9

## 1.3 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at [www.gowinsemi.com](http://www.gowinsemi.com):

1. GW1NR series of FPGA Products Data Sheet
2. Gowin FPGA Products Programming and Configuration User Guide
3. GW1NR series of FPGA Products Package and Pinout
4. GW1NR-4&4B Pinout
5. GW1NR-9 Pinout

## 1.4 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are set out in Table 1-1 below.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Name
FPGA	Field Programmable Gate Array
SIP	System in Package

Abbreviations and Terminology	Name
SDRAM	Synchronous Dynamic RAM
PSRAM	Pseudo Static Random Access Memory
CFU	Configurable Function Unit
CLS	Configurable Logic Slice
CRU	Configurable Routing Unit
LUT4	4-input Look-up Tables
LUT5	5-input Look-up Tables
LUT6	6-input Look-up Tables
LUT7	7-input Look-up Tables
LUT8	8-input Look-up Tables
REG	Register
ALU	Arithmetic Logic Unit
IOB	Input/Output Block
S-SRAM	Shadow SRAM
B-SRAM	Block SRAM
SP	Single Port
SDP	Semi Dual Port
DP	Dual Port
DSP	Digital Signal Processing
DQCE	Dynamic Quadrant Clock Enable
DCS	Dynamic Clock Selector
PLL	Phase-locked Loop
DLL	Delay-locked Loop
QN88	QFN88
TDM	Time Division Multiplexing

## 1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: [www.gowinsemi.com](http://www.gowinsemi.com)

E-mail: [support@gowinsemi.com](mailto:support@gowinsemi.com)

+Tel: +86 755 8262 0391

# 2General Description

The GW1NR series of FPGA products are the first generation products in the LittleBee<sup>®</sup> family and represent one form of SIP chip. The main difference between the GW1N series and the GW1NR series is that the GW1NR series integrates abundant SDRAM. The GW1NR series also provides low power consumption, instant on, low cost, non-volatile, high security, various packages, and flexible usage.

GOWINSEMI provides a new generation of FPGA hardware development environment through market-oriented independent research and development that supports the GW1NR series of FPGA products and applies to FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

## 2.1 Features

- User Flash
  - Up to 1,792 Kbits
  - 10,000 write cycles
- Lower power consumption
  - 55 nm embedded flash technology
  - LV: supports 1.2 V core voltage
  - UV: 2.5 V±3.3 V power supply
  - Clock dynamically turns on and off
- Integrate SDRAM SIP chip
- Multiple I/O standards
  - LVC MOS33/25/18/15/12; LV TTL33, SSTL33/25/18 I, SSTL33/25/18 II, SSTL15; HSTL18 I, HSTL18 II, HSTL15 I; PCI, LVDS25, RSDS, LVDS25E, BLVDSE, MLVDSE, LVPECLE, RSDSE
  - Input hysteresis option
  - Supports 4 mA, 8 mA, 16 mA, 24 mA, etc. drive options
  - Slew rate option
  - Output drive strength option
  - Individual bus keeper, weak pull-up, weak pull-down, and open drain option

- Hot socket
- BANK0 of GW1NR-9 supports MIPI Input
- BANK2 of GW1NR-9 supports MIPI Output
- BANK0 and BANK2 of GW1NR-9 support I3C OpenDrain/PushPull conversion
- High performance DSP
  - High performance digital signal processing ability
  - Supports 9 x 9, 18 x 18, 36 x 36 bits multiplier and 54 bits accumulator;
  - Multipliers cascading
  - Registers pipeline and bypass
  - Adaptive filtering through signal feedback
  - Supports barrel shifter
- Abundant slices
  - Four-input LUT (LUT4)
  - Double-edge flip-flops
  - Supports shift register and distributed register
- Block SRAM with multiple modes
  - Supports dual port, single port, and semi-dual port
  - Supports bytes write enable
- Flexible PLLs+DLLs
  - Frequency adjustment (multiply and division) and phase adjustment
  - Supports global clock
- Built-in flash programming
  - Instant-on
  - Supports security bit operation
  - Supports AUTO BOOT and DUAL BOOT
- Configuration
  - JTAG configuration
  - GW1NR-4B supports JTAG transparent transmission
  - Offers up to six GowinCONFIG configuration modes: AUTOBOOT, SSPI, MSPI, CPU, SERIAL, DUAL BOOT

## 2.2 Product Resources

Table 2-1 Product Resources

Device	GW1NR-4/ GW1NR-4B	GW1NR-9
LUT4	4,608	8,640
Flip-Flop (FF)	3,456	6,480
Shadow SRAM S-SRAM (bits)	0	17,280
Block SRAM B-SRAM (bits)	180K	468K
B-SRAM quantity B-SRAM	10	26
User Flash (bits)	256K	608K
SDR SDRAM (bits)	64M	64M
PSRAM(bits)	64M	64M

Device	GW1NR-4/ GW1NR-4B	GW1NR-9
18 x 18 Multiplier	16	20
PLLs+DLLs	2+2	2+4
Total number of I/O banks	4	4
Max. user I/O <sup>1</sup>	70	120
Core Voltage (LV)	1.2V	1.2V
Core Voltage (UV)	2.5V/3.3V	

**Note!**

[1] JTAGSEL\_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.

## 2.3 Package Information

**Table2-2 Package and Memory Information**

Package	Device	Memory
QN88	GW1NR-4/4B	SDR SDRAM PSRAM
	GW1NR-9	SDR SDRAM PSRAM
MG81	GW1NR-4/4B	PSRAM
LQ144	GW1NR-9	PSRAM

**Table2-3 Package Information, Max. I/O, and LVDS Pairs**

Package	Pitch(mm)	Size(mm)	GW1NR-4/GW1NR-4B	GW1NR-9
QN88	0.4	10 x 10	70(11)	70 (17)
LQ144	0.5	22 x 22	68 (10)	-
MG81	0.5	4.5 x 4.5	-	120 (20)

**Note!**

- [1] The package types in this data sheet are written with abbreviations. See 5.1Part Name.
- For more detailed information, please refer to [GW1NR series of FPGA Products Pinout](#).
- The JTAGSEL\_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O. See [GW1NR series FPGA Products Data Sheet](#) for more details.

# 3 Architecture

## 3.1 Architecture Overview

Figure 3-1 GW1NR Architecture Overview

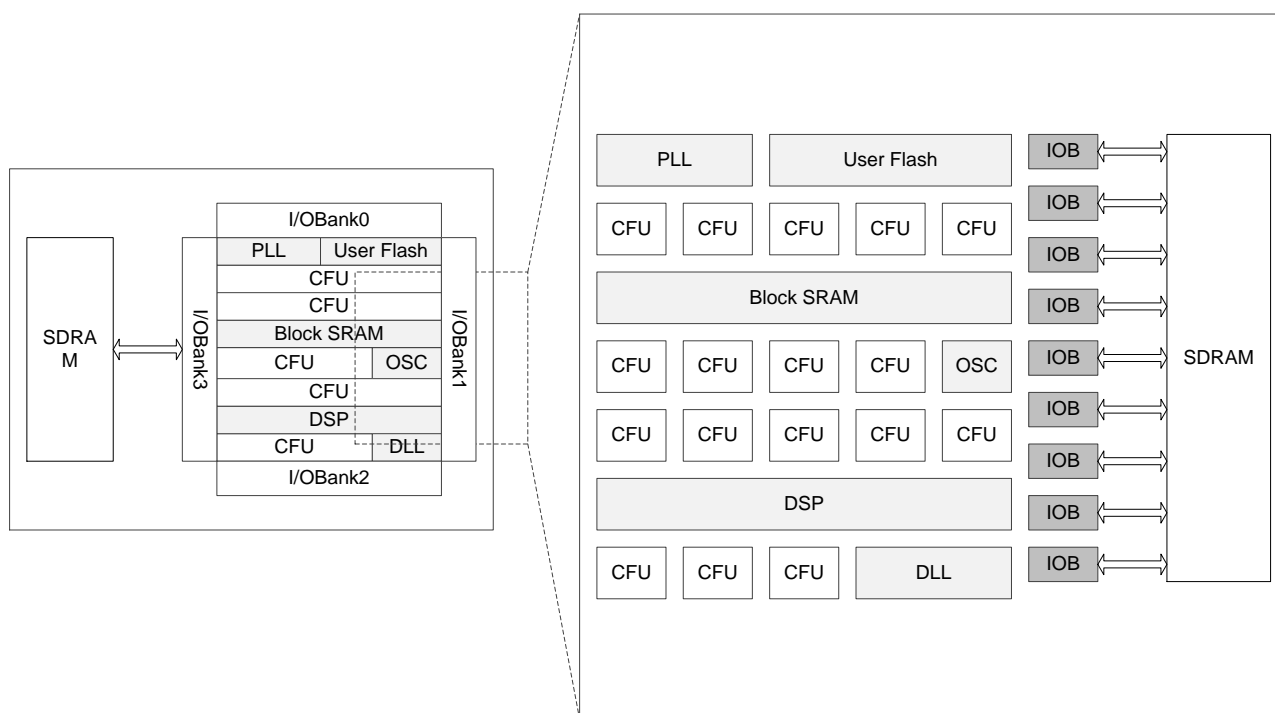


Figure 3-1 presents an overview of the architecture of the GW1NR devices. GW1NR is one form of SIP chip, integrated with the GW1N series of FPGA products and SDRAM chip. For SDRAM features and overview, see [3.2 SDRAM](#).

The core of the GW1NR devices is the array of configurable logic unit (CFU) surrounded by IO blocks. GW1NR also provides B-SRAM, DSP, PLL, DLL, user Flash, and on chip oscillator and supports Instant-on. See Table 2-1 for more detailed information on internal resources.

Configurable Function Unit (CFU) is the base cell for the array of the



GW1NR series of FPGA Products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode, ALU mode, and memory mode. Memory mode is supported in GW1NR-6 and GW1NR -9. See [3.3 Configurable Function Unit](#) for more detailed information.

The I/O resources in the GW1NR series of FPGA products are arranged around the periphery of the devices in groups referred to as banks, including Bank0, Bank1, Bank2, and Bank3. The I/O resources are connected with SDRAM for data storage. Partial of the I/O resources are bounded out. The I/O resources support multiple level standards, and support basic mode, SRD mode, and generic DDR mode. See [3.4 IOB](#) for more detailed information.

The B-SRAM is embedded as a row in the GW1NR series of FPGA products. In the FPGA array, each B-SRAM occupies three columns of CFU. Each B-SRAM has 18,432 bits (18 Kbits) and supports multiple configuration modes and operation modes. See [3.5 Block SRAM \(B-SRAM\)](#) for more detailed information.

The User Flash is embedded in the GW1NR series of FPGA products, without loss of data even if power off. See [3.6 User Flash](#) for more detailed information.

The GW1NR series of FPGA products also provide DSP. DSP blocks are embedded as a row in the FPGA array. Each DSP occupies nine CFU columns. Each DSP block contains two Macros, and each Macro contains two pre-adders, two multipliers with 18 by 18 inputs, and a three input ALU54. See [3.7 DSP](#) for more detailed information.

GW1NR provides one PLL and one DLL. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters. There is an internal programmable on-chip oscillator in each of the GW1NR series of the FPGA product. The on-chip oscillator supports the clock frequencies ranging from 2.5 MHz to 125 MHz, providing the clock resource for the MSPI mode. It also provides a clock resource for user designs with the clock precision reaching  $\pm 5\%$ . See [3.8Clock](#), [3.12On Chip Oscillator](#) for more detailed information.

FPGA provides abundant CRUs, connecting all the resources in the FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the GW1NR series of FPGA Products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. See [3.8Clock](#), [3.9Long Wire \(LW\)](#), [3.10Global Set/Reset \(GSR\)](#) for more detailed information.

## 3.2 SDARM

Different packages for the GW1NR series of FPGA products have different capacities and types. Please refer to [2.3 Package Information](#) for details.

### 3.2.1 SDR SDRAM

#### Features

- Access time: 4.5 ns/4.5 ns
- Clock rate: 200/166/143 MHz
- Data width: 16bits
- Synchronous operation
- Internal pipeline architecture
- Four internal Banks (1024K x 16 bits x 4BANK)
- Programmable mode
  - Column address strobe latency: 2 or 3
  - Burst length: 1, 2, 4, 8 bytes or full page
  - Burst type: sequential mode or interval mode
  - Burst-Read-Single-Write
  - Burst stop function
- Byte masking function
- Auto refresh and self refresh
- 4,096 refresh cycle / 64 ms
- 3.3V $\pm$ 0.3V power supply<sup>1</sup>
- LVTTTL Interface

#### Note!

For the more detailed information about power supply, please refer to Table 4-2.

#### Overview

SDRAM integrated in the GW1NR series of FPGA Products is a high-speed CMOS synchronous DRAM containing 64Mb. SDRAM consists of four banks, each BANK with size of 1M x16 bits, and each BANK consists of 4096 rows x 256 columns x 16 bits of memory arrays. Support read-write operation burst mode, accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The activation command is a must before reading or writing. Read or write burst lengths provide 1, 2, 4, and 8 bytes or full page, with a burst termination option. An auto pre-charge function may be enabled to provide a self-timed row pre-charge that is initiated at the end of the burst sequence. Both the auto- and self- refresh functions are easy to use. Through the use of a programmable mode register, the system can choose the most suitable modes to maximize performance.

The supply voltage for the SDRAM interface is 3.3V; the BANK voltage that connects to the SDRAM needs to be 3.3V. For more details, please refer to Table 4-2.

The IP Core Generator that is integrated into Gowin YunYuan Software supports both built-in and external SDR SDRAM controller IP. This controller IP can be used for the SDRAM power-up, initialization, read calibration, etc., by following the controller read/write timing. For the further detailed information, please refer to [Gowin SDRAM Controller User Guide](#).

### 3.2.2 PSRAM

#### Features

- Clock frequency:166 MHz, the maximum frequency can be DDR332
- Double-edge data transmission
- Data width: 16bits
- Read/write data latching (RWDS)
- Temperature compensated refresh
- Partial arrays self-refresh (PASR)
- Hybrid sleep mode
- Deep power down (DPD)
- Drive capability: 35,50,100 and 200 Ohm
- Burst access
- 16/32/64/128 bytes burst mode
- Status/control register
- 1.8V supply voltage<sup>1</sup>

#### Note!

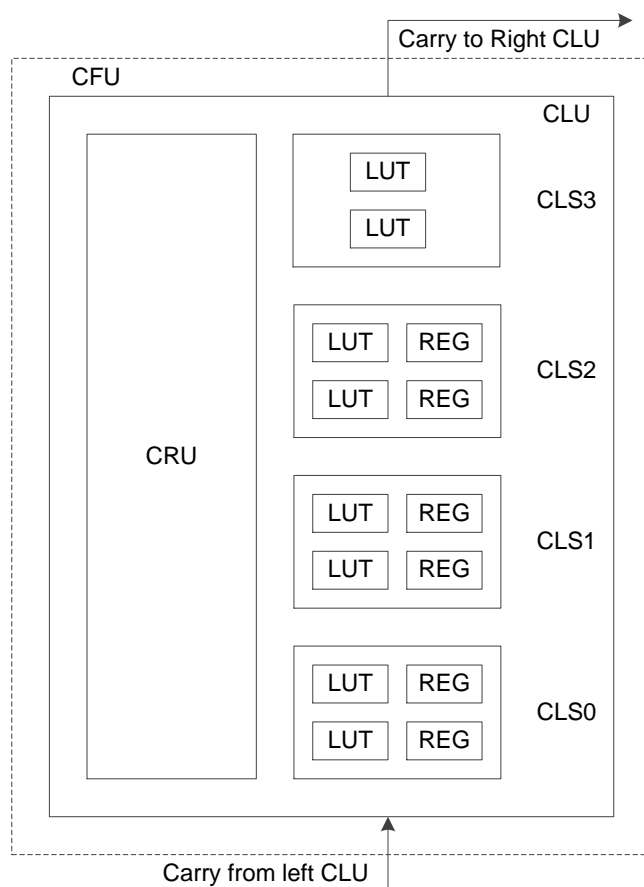
For the more information about power supply, please refer to Table 4-2.

The power supply for the PSRAM interface is 1.8V; the BANK voltage that connects to the PSRAM needs to be 1.8V. Please refer to Table 4-2 further details.

The IP Core Generator that is integrated into Gowin YunYuan Software supports both built-in and external PSRAM controller IP. This controller IP can be used for the PSRAM power-up, initialization, read calibration, etc., by following the controller read/write timing. For the further detailed information, please refer to *Gowin PSRAM Memory Interface IP User Guide*.

## 3.3 Configurable Function Unit

Configurable Function Unit (CFU) is the base cell for the array of GW1NR series FPGA Products. Each CFU consists of a Configurable Logic Unit (CLU) and its routing resource Configurable Routing Unit (CRU). In each CLU, there are four configurable logic slices (CLS). Each CLS contains look-up tables (LUT) and registers, as shown in Figure 3-2 below.

**Figure 3-2 CFU View**

### 3.3.1 CLU

The CLU supports three operation modes: basic logic mode, ALU mode, and memory mode.

- Basic Logic Mode

Each LUT can be configured as one four input LUT. A higher input number of LUT can be formed by combining LUT4 together.

- Each CLS can form one five input LUT5.
- Two CLSs can form one six input LUT6.
- Four CLSs can form one seven input LUT7.
- Eight CLSs (two CLUs) can form one eight input LUT8.

- ALU Mode

When combined with carry chain logic, the LUT can be configured as the ALU mode to implement the following functions.

- Adder and subtractor
- Up/down counter
- Comparator, including greater-than, less-than, and not-equal-to
- MULT

- Memory mode

GW1NR-9 supports memory mode. In this mode, a 16 x 4 S-SRAM or

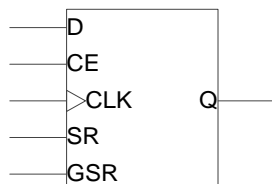
ROM can be constructed by using CLSs.

This S-SRAM can be initialized during the device configuration stage. The initialization data can be generated in the bit stream file from Gowin Yunyuan software.

### Register

Each configurable logic slice (CLS0~CLS2) has two registers (REG), as shown in Figure 3-3 below.

**Figure 3-3 Register in CLS**



**Table3-1 Register Description in CLS**

Signal	I/O	Description
D	I	Data input <sup>1</sup>
CE	I	CLK enable, can be high or low effective <sup>2</sup>
CLK	I	Clock, can be rising edge or falling edge triggering <sup>2</sup>
SR	I	Set/Reset, can be configured as <sup>2</sup> : <ul style="list-style-type: none"> <li>● Synchronized reset</li> <li>● Synchronized set</li> <li>● Asynchronous reset</li> <li>● Asynchronous set</li> <li>● Non</li> </ul>
GSR <sup>3,4</sup>	I	Global Set/Reset, can be configured as <sup>4</sup> : <ul style="list-style-type: none"> <li>● Asynchronous reset</li> <li>● Asynchronous set</li> <li>● Non</li> </ul>
Q	O	Register

#### Note!

- [1] The source of the signal D can be the output of a LUT, or the input of the CRU; as such, the register can be used alone when LUTs are in use.
- [2] CE/CLK/SR in CFU is independent.
- [3] In the GW1NR series of FPGA products, GSR has its own dedicated network.
- [4] When both SR and GSR are effective, GSR has higher priority.

### 3.3.2 CRU

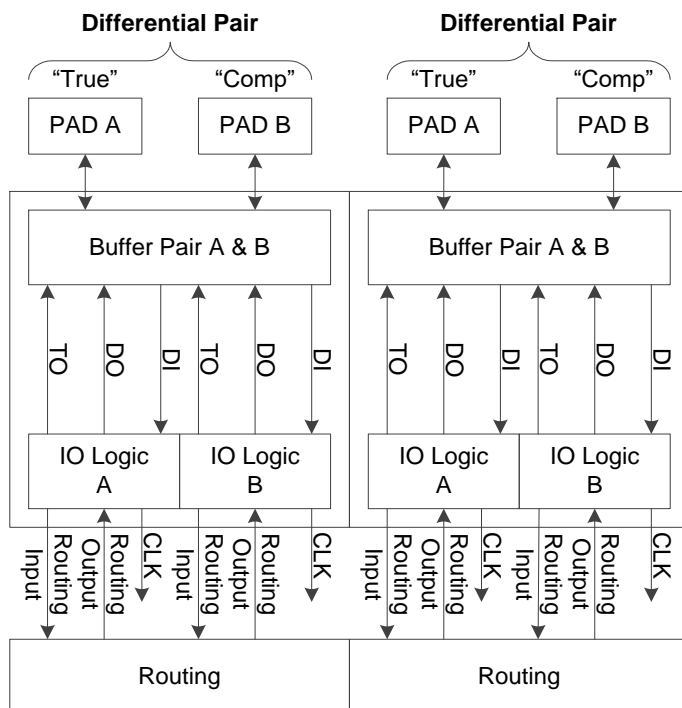
The main functions of the CRU are as follows:

- Input selection: Select input signals for the CFU.
- Configurable routing: Connect the input and output of the CFUs, including inside the CFU, CFU to CFU, and CFU to other functional blocks in FPGA.

## 3.4 IOB

The IOB in the GW1NR series of FPGA products includes IO buffer, IO logic, and its routing unit. As shown in Figure 3-4, each IOB connects to two pins (Marked A and B). They can be used as a differential pair or as two single-end input/output.

Figure 3-4 IOB Structure View



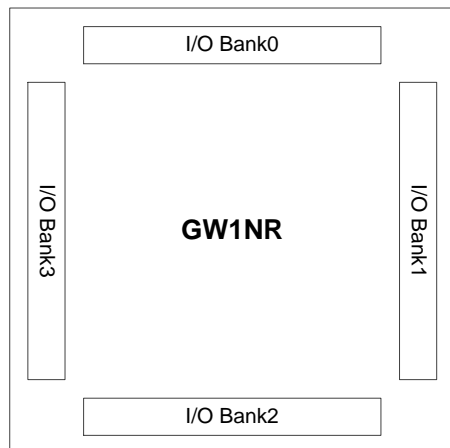
### IOB Features:

- $V_{CCO}$  supplied with each bank
- LVCMOS, PCI, LVTTL, LVDS, SSTL, and HSTL
- Input hysteresis option
- Output drive strength option
- Slew rate option
- Individual bus keeper, weak pull-up, weak pull-down, and open drain option
- Hot socket
- IO logic supports basic mode, SRD mode, and generic DDR mode
- BANK0 of GW1NR-9 supports MIPI Input
- BANK2 of GW1NR-9 supports MIPI Output
- BANK0 and BANK2 of GW1NR-9 support I3C OpenDrain/PushPull conversion

### 3.4.1 I/O Buffer

There are four IO Banks in the GW1NR series of FPGA products, as shown in Figure 3-5. To support SSTL, HSTL, etc., each bank also provides one independent voltage source ( $V_{REF}$ ) as referenced voltage. The user can choose from the internal reference voltage of the bank ( $0.5 \times V_{CC0}$ ) or the external reference voltage using any IO from the bank.

Figure 3-5 GW1NR I/O Bank Distribution



The GW1NR series of FPGA products support LV and UV.

LV devices support 1.2V  $V_{CC}$  to meet users' low power needs.

$V_{CC0}$  of LV devices can be set as 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V according to requirements<sup>1</sup>.

Linear voltage regulator is integrated IN UV devices to facilitate single power supply. The power supply for the UV devices integrated with SDR SDRAM is 3.3V. See Table 4-2 for further detailed information. The power supply for the UV devices integrated with DDR SDRAM is 2.5V. The UV devices embedded with PSRAM need two kinds of power supply: 1.8V and 2.5V/3.3V.

$V_{CCX}$  supports 2.5 V or 3.3 V power supply.

In GW1NR-9 devices, I/O of Bank0 supports MIPI input and I/O of Bank2 supports MIPI output. I/O of Bank0 and Bank2 support MIPI I3C OpenDrain/PushPull conversion. The other devices do not support.

**Note!**

- By default, the systemIO is weak pull-up for blank chips.
- For the recommended working conditions for different packages, please refer to [4.1Operating Conditions](#)

For the  $V_{CC0}$  requirements of different I/O standards, see Table 3-2.

Table 3-2 Output I/O Standards and Configuration Options

I/O output standard	Single/Differ	Bank $V_{CC0}$ (V)	Driver Strength (mA)
LVTTL33	Single end	3.3	4,8,12,16,24
LVC MOS33	Single end	3.3	4,8,12,16,24

I/O output standard	Single/Differ	Bank V <sub>CCO</sub> (V)	Driver Strength (mA)
LVC MOS25	Single end	2.5	4,8,12,16
LVC MOS18	Single end	1.8	4,8,12
LVC MOS15	Single end	1.5	4,8
LVC MOS12	Single end	1.2	4,8
SSTL25_I	Single end	2.5	8
SSTL25_II	Single end	2.5	8
SSTL33_I	Single end	3.3	8
SSTL33_II	Single end	3.3	8
SSTL18_I	Single end	1.8	8
SSTL18_II	Single end	1.8	8
SSTL15	Single end	1.5	8
HSTL18_I	Single end	1.8	8
HSTL18_II	Single end	1.8	8
HSTL15_I	Single end	1.5	8
PCI33	Single end	3.3	N/A
LVPECL33E	Differential	3.3	16
MVLDS25E	Differential	2.5	16
BLVDS25E	Differential	2.5	16
RSDS25E	Differential	2.5	8
LVDS25E	Differential	2.5	8
LVDS25	Differential	2.5/3.3	3.5/2.5/2/1.25
RSDS	Differential	2.5/3.3	2
MINILVDS	Differential	2.5/3.3	2
PPLVDS	Differential	2.5/3.3	3.5
SSTL15D	Differential	1.5	8
SSTL25D_I	Differential	2.5	8
SSTL25D_II	Differential	2.5	8
SSTL33D_I	Differential	3.3	8
SSTL33D_II	Differential	3.3	8
SSTL18D_I	Differential	1.8	8
SSTL18D_II	Differential	1.8	8
HSTL18D_I	Differential	1.8	8
HSTL18D_II	Differential	1.8	8
HSTL15D_I	Differential	1.5	8
MIPI	Differential	TBD	TBD



Table 3-3 Output I/O Standards and Configuration Options

I/O Input Standard	Single/Differ	Bank V <sub>CCO</sub> (V)	Hysteresis	Need V <sub>REF</sub>
LVTTTL33	Single end	1.5/1.8/2.5/3.3	Yes	No
LVC MOS33	Single end	1.5/1.8/2.5/3.3	Yes	No
LVC MOS25	Single end	1.5/1.8/2.5/3.3	Yes	No
LVC MOS18	Single end	1.5/1.8/2.5/3.3	Yes	No
LVC MOS15	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
LVC MOS12	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
SSTL15	Single end	1.5/1.8/2.5/3.3	No	Yes
SSTL25_I	Single end	2.5/3.3	No	Yes
SSTL25_II	Single end	2.5/3.3	No	Yes
SSTL33_I	Single end	3.3	No	Yes
SSTL33_II	Single end	3.3	No	Yes
SSTL18_I	Single end	1.8/2.5/3.3	No	Yes
SSTL18_II	Single end	1.8/2.5/3.3	No	Yes
HSTL18_I	Single end	1.8/2.5/3.3	No	Yes
HSTL18_II	Single end	1.8/2.5/3.3	No	Yes
HSTL15_I	Single end	1.5/1.8/2.5/3.3	No	Yes
PCI33	Single end	3.3	Yes	No
LVDS	Differential	2.5/3.3	No	No
RSDS	Differential	2.5/3.3	No	No
MINILVDS	Differential	2.5/3.3	No	No
PPLVDS	Differential	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
RSDS25E	Differential	2.5/3.3	No	No
LVPECL33	Differential	3.3	No	No
SSTL15D	Differential	1.5/1.8/2.5/3.3	No	No
SSTL25D_I	Differential	2.5/3.3	No	No
SSTL25D_II	Differential	2.5/3.3	No	No
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
SSTL18D_I	Differential	1.8/2.5/3.3	No	No
SSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL18D_I	Differential	1.8/2.5/3.3	No	No
HSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL15D_I	Differential	1.5/1.8/2.5/3.3	No	No
MIPI	Differential	TBD	TBD	TBD

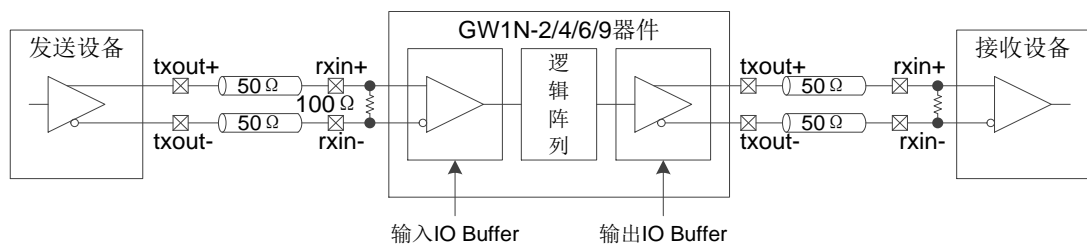
### 3.4.2 True LVDS Design

BANK1/2/3 in the GW1NR devices support true LVDS output, but BANK1/2/3 do not support internal 100Ω input differential matched resistance. Bank0 supports internal 100Ω input differential matched resistance. BANK 0/1/2/3 support LVDS25E, MLVDS25E, BLVDS25E, etc. For the detailed information on different levels, please refer to [Gowin systemIO User Guide](#).

For more detailed information on true LVDS, please refer to [GW1NR series of FPGA Products Pinout](#).

True LVDS input I/O needs external 100Ω terminal resistance for matching. See Figure 3-6 for the true LVDS design.

Figure 3-6 True LVDS Design



For more detailed information about LVDS25E, MLVDS25E, and BLVDS25E on IO terminal matched resistance, please refer to [Gowin SystemIO User Guide](#).

### 3.4.3 I/O Logic

Figure 3-7 shows the I/O logic output of the GW1NR series of FPGA products.

Figure 3-7 I/O Logic Output

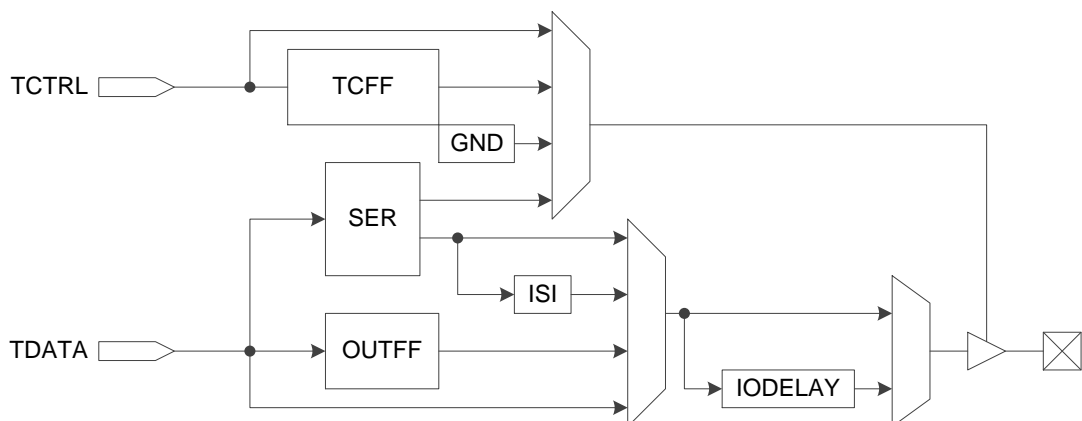
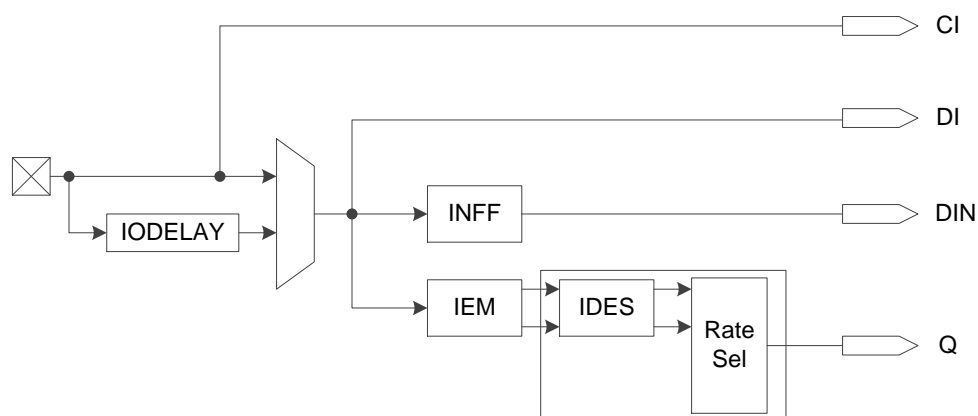


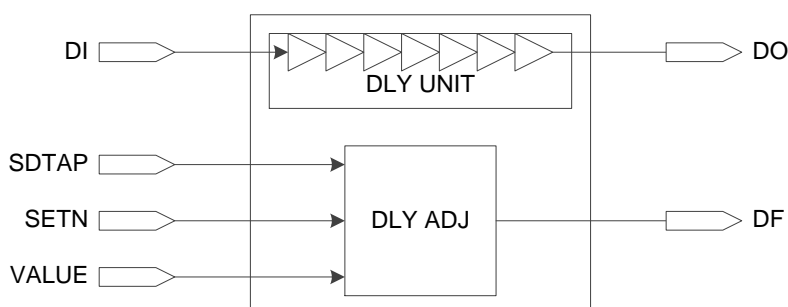
Figure 3-8 shows the I/O logic input of the GW1NR series of FPGA products.

**Figure 3-8 I/O Logic Input**

A description of the I/O logic modules of the GW1NR series of FPGA products is presented below:

### IODELAY

See Figure 3-9 for an overview of the IODELAY. Each I/O of the GW1NR series of FPGA products has an IODELAY cell. The longest delay it can provide is about  $128 \text{ steps} \times 30\text{ps} = 3840\text{ps}$ .

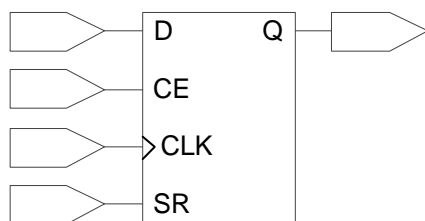
**Figure 3-9 IODELAY**

The delay cell can be controlled in two ways:

- Static control:
- Dynamic control: Usually used to sample delay window together with IEM. The IODELAY cannot be used for both input and output at the same time

### I/O Register

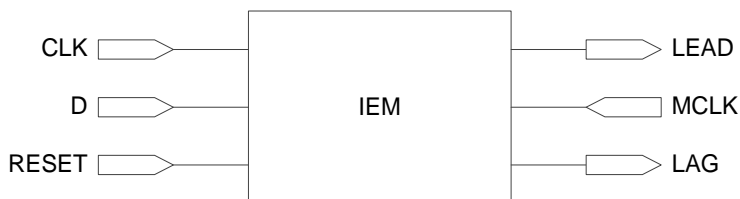
See Figure Figure 3-10 for the I/O register in the GW1NR series of FPGA products. Each I/O provides one input register, INFF, one output register, OUTFF, and a tristate Register, TCFF.

**Figure 3-10 Register Structure in I/O Logic****Note!**

- CE can be either active low (0: enable) or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The register can be programmed as register or latch.

**IEM**

IEM is for sampling clock edge and is used in the generic DDR mode. See Figure 3-11 for the IEM structure.

**Figure 3-11 IEM Structure****De-serializer DES and Clock Domain Transfer**

The GW1NR series of FPGA products provides a simple serializer SER for each output I/O to support advanced I/O protocols.

**Serializer SER**

The GW1NR series of FPGA products provides a simple serializer (SER) for each output I/O to support advanced I/O protocols.

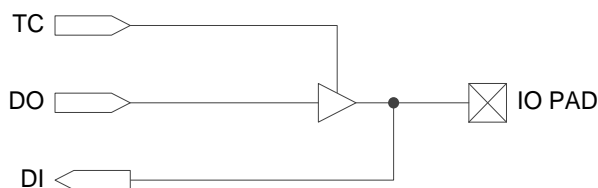
**3.4.4 I/O Logic Modes**

The I/O Logic in the GW1NR series of FPGA products supports several modes. In each operation, the I/O (or I/O differential pair) can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

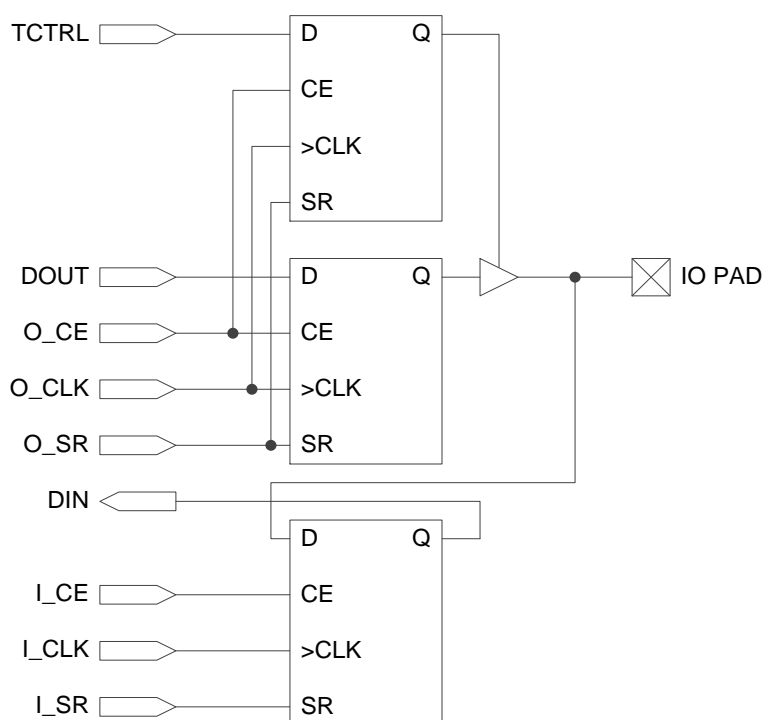
Not all the device pins support I/O logic. The pins IOL10 (A, B, C ... J) and IOR10 (A, B, C ..., J) of GW1NR-4/GW1NR-4B do not support IO logic. All GW1NR-9 pins support IO logic.

**Basic Mode**

In basic mode, the I/O Logic is as shown in Figure 3-12, and the TC, DO, and DI signals can connect to the internal cores directly through CRU.

**Figure 3-12 I/O Logic in Basic Mode****SDR Mode**

In comparison with the basic mode, SDR utilizes the IO register, as shown in Figure 3-13. This can effectively improve IO timing.

**Figure 3-13 I/O Logic in SDR Mode****Note!**

- CLK enable O\_CE and I\_CE can be configured as active high or active low;
- O\_CLK and I\_CLK can be either rising edge trigger or falling edge trigger;
- Local set/reset signal O\_SR and I\_SR can be either synchronized reset, synchronized set, asynchronous reset, asynchronous set, or no-function;
- I/O in SDR mode can be configured as basic register or latch.

**Generic DDR Mode**

Higher speed I/O protocols can be supported in generic DDR mode. GW1NR-9 devices support IDER16 mode and OSER16 mode. The other devices do not support.

Figure 3-14 shows the generic DDR input, with a speed ratio of the internal logic to PAD 1:2.

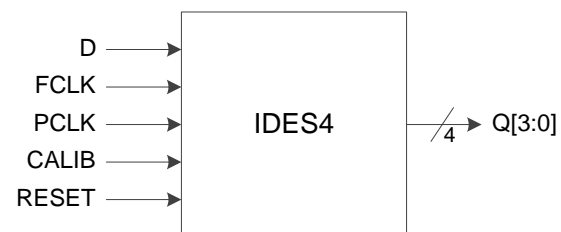
**Figure 3-14 I/O Logic in DDR Input Mode**

Figure 3-15 shows the generic DDR output, with a speed ratio of the PAD to FPGA internal logic 2:1.

**Figure 3-15 I/O Logic in DDR Output Mode**

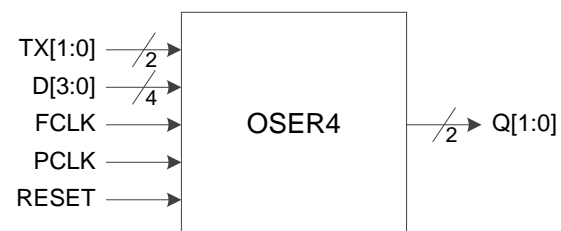
### IDES4

In IDES4 mode, the speed ratio of the PAD to FPGA internal logic is 1:4.

**Figure 3-16 I/O Logic in IDES10 Mode**

### OSER4 Mode

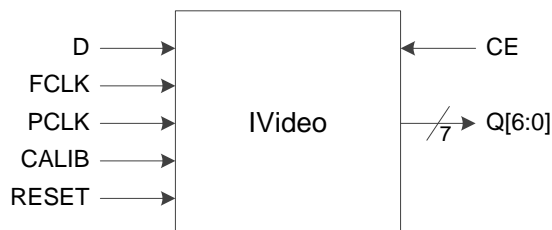
In OSER4 mode, the speed ratio of the PAD to FPGA internal logic is 4:1.

**Figure 3-17 I/O Logic in OSER4 Mode**

### IVideo Mode

In IVideo mode, the speed ratio of the PAD to FPGA internal logic is 1:7.

**Figure 3-18 I/O Logic in IVideo Mode**



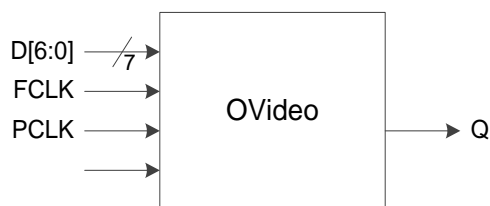
**Note!**

IVideo and IDES8/10 will occupy the neighboring I/O logic. If the I/O logic of a single port is occupied, the pin can only be programmed in SDR or BASIC mode.

### OVideo Mode

In OVideo mode, the speed ratio of the PAD to FPGA internal logic is 7:1.

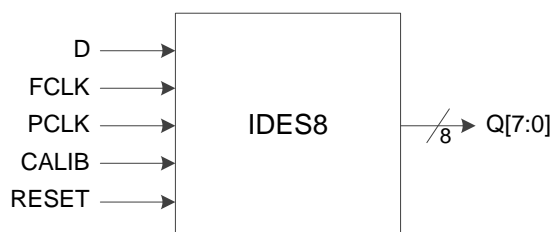
**Figure 3-19 I/O Logic in OVideo Mode**



### IDES8 Mode

In IDES8 mode, the speed ratio of the PAD to FPGA internal logic is 1:8.

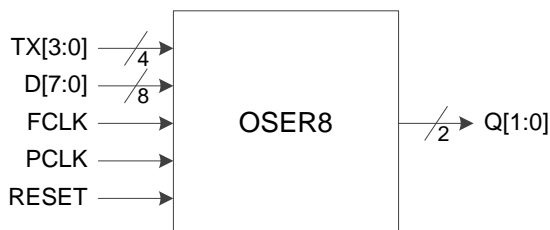
**Figure 3-20 I/O Logic in IDES8 Mode**



### OSER8 Mode

In OSER8 mode, the speed ratio of the PAD to FPGA internal logic is 8:1.

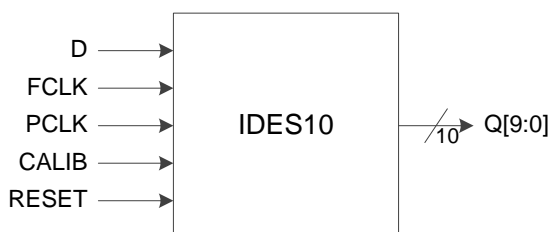
Figure 3-21 I/O Logic in OSER8 Mode



### IDES10 Mode

In IDES10 mode, the speed ratio of the PAD to FPGA internal logic is 1:10.

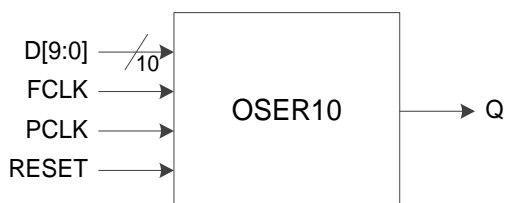
Figure 3-22 I/O Logic in IDES10 Mode



### OSER10 Mode

In OSER10 mode, the speed ratio of the PAD to FPGA internal logic is 10:1.

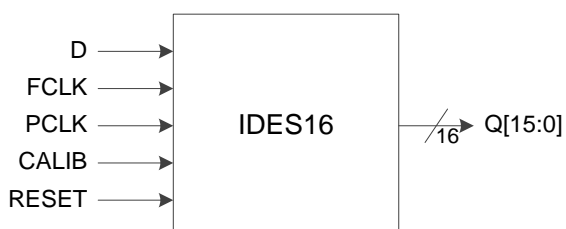
Figure 3-23 I/O Logic in OSER10 Mode



### IDES16 Mode

In IDES16 mode, the speed ratio of the PAD to FPGA internal logic is 1:16.

Figure 3-24 I/O Logic in IDES16 Mode



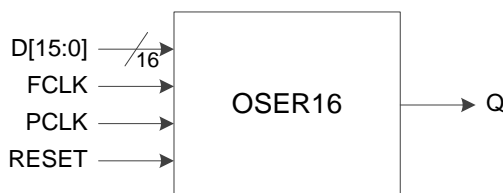
### OSER16 Mode

In OSER16 mode, the speed ratio of the PAD to FPGA internal logic is



16:1.

Figure 3-25 I/O Logic in OSER16 Mode



## 3.5 Block SRAM (B-SRAM)

### 3.5.1 Introduction

GW1NR series FPGA products provide abundant SRAM. The Block SRAM (B-SRAM) is embedded as a row in the FPGA array and is different from S-SRAM (Shadow SRAM). Each B-SRAM occupies three columns of CFU in the FPGA array. Each B-SRAM has 18,432 bits (18Kbits). There are five operation modes: single port, dual port, semi-dual port, ROM, and FIFO. The signals and functional descriptions of B-SRAM are listed in Table 3-4.

An abundance of B-SRAM resources provide a guarantee for the user's high-performance design. B-SRAM features include the following:

- Max.18,432 bits per B-SRAM
- B-SRAM itself can run at 190 MHz at max
- Single port
- Dual port
- Semi-dual port
- Parity bits
- ROM
- Data width from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Enable Byte operation for double byte or above
- Asynchronous reset, synchronous reset
- Normal Read and Write Mode
- Read-before-write Mode
- Write-through Mode

Table 3-4 B-SRAM Signals

Port Name	I/O	Description
DIA	I	Port A data input
DIB	I	Port B data input
ADA	I	Port A address
ADB	I	Port B address
CEA	I	Clock enable, Port A
CEB	I	Clock enable, Port B
RESETA	I	Register reset, Port A

RESETB	I	Register reset, Port B
WREA	I	Read/write enable, Port A
WREB	I	Read/write enable, Port B
BLKSEL	I	Block select
CLKA	I	Read/write cycle clock for Port A input registers
CLKB	I	Read/write cycle clock for Port B input registers
OCEA	I	Clock enable for Port A output registers
OCEB	I	Clock enable for Port B output registers
DOA	O	Port A data output
DOB	O	Port B data output

### 3.5.2 Configuration Mode

The B-SRAM mode in the GW1NR series of FPGA products supports different data bus widths. See Table 3-5.

**Table 3-5 Memory Size Configuration**

Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	Read Only
16K x 1	16K x 1	16K x 1	16K x 1
8K x 2	8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32	512 x 32
2K x 9	2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36	512 x 36

### 3.5.3 Mixed Data Bus Width Configuration

B-SRAM in the GW1NR series of FPGA products supports mixed data bus width operation. In the dual port and semi-dual port modes, the data bus width for read and write can be different. For the configuration options that are available, please see Table 3-6 and Table 3-7 below.

**Table 3-6 Dual Port Mixed Read/Write Data Width Configuration**

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		
1K x 16	*	*	*	*	*		

2K x 9						*	*
1K x 18						*	*

**Note!**

"\*" denotes the modes supported.

**Table 3-7 Semi Dual Port Mixed Read/Write Data Width Configuration**

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512 x 32	2K x 9	1K x 18	512 x 36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			
512x32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

**Note!**

"\*" denotes the modes supported.

### 3.5.4 Byte-enable

The B-SRAM in the GW1NR series of FPGA products supports byte-enable. For data longer than a Byte, the additional bits can be blocked, and only the selected portion is allowed to be written into. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB), and byte-enable parameter options can be used to control the B-SRAM write operation.

### 3.5.5 Parity Bit

There are parity bits in B-SRAM. The 9th bit in each byte can be used as a parity bit or for data storage. However, the parity operation is not yet supported.

### 3.5.6 Synchronous operation

- All the input registers of B-SRAM support synchronous write;
- The output registers can be used as pipeline register to improve design performance;
- The output registers are bypass-able.

### 3.5.7 Power up Conditions

B-SRAM initialization is supported when powering up. During the power-up process, B-SRAM is in standby mode, and all the data outputs are “0”. This also applies in ROM mode.

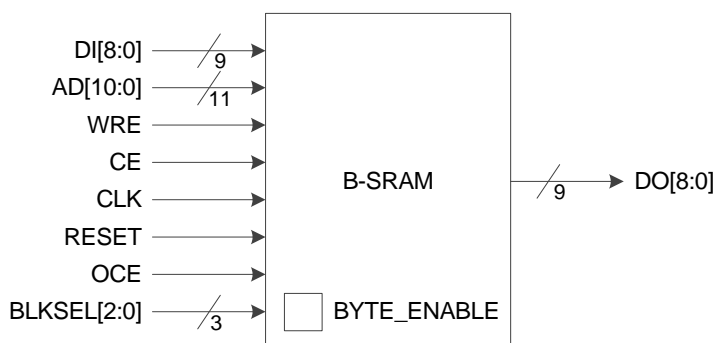
### 3.5.8 Operation Modes

The input registers of B-SRAM can be used for synchronous write. The output registers can be used as pipeline register to improve design performance. In the dual port mode, the two ports of B-SRAM can be operated totally independently. Port A and Port B have their own clock and are write-enabled; as such, both ports can be written to and read independently from each other.

#### Single Port Mode

In the single port mode, as shown below, B-SRAM can write to or read from one port at one clock edge. During the write operation, the data can show up at the output of B-SRAM. Normal write mode (Normal-write Mode) and write-through mode can be supported. When the output register is bypassed, the new data will show at the same write clock rising edge. For the single port 2 K x 9 bits block memory, see Figure 3-26 below.

Figure 3-26 Single Port Block Memory



The table below shows all the configuration options that are available in the single port mode:

Table 3-8 Single Port Block Memory Configuration

Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Data Depth
SP	B-SRAM_16K_S1	16K	16K x 1	16,384	1
	B-SRAM_8K_S2	16K	8K x 2	8,192	2
	B-SRAM_4K_S4	16K	4K x 4	4,096	4

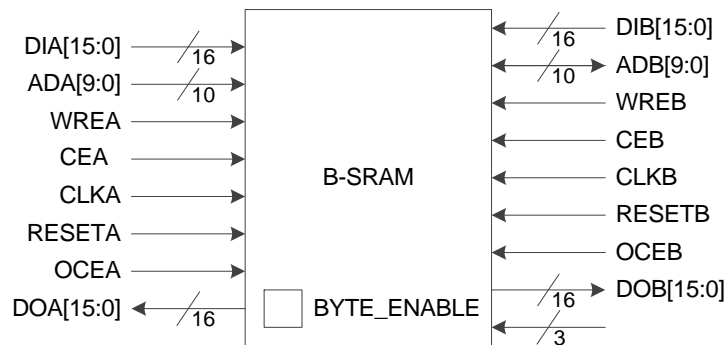
SPX9	B-SRAM_2K_S8	16K	2K x 8	2,048	8
	B-SRAM_1K_S16	16K	1K x 16	1,024	16
	B-SRAM_512_S32	16K	512 x 32	512	32
	B-SRAM_2K_S9	18K	2K x 9	2,048	9
	B-SRAM_1K_S18	18K	1K x 18	1,024	18
	B-SRAM_512_S36	18K	512 x 36	512	36

### Dual Port Mode

B-SRAM support dual port mode, as shown in Figure 3-27. The applicable operations are as follows:

- Two independent read
- Two independent write
- An independent read and an independent write at different clock frequencies

Figure 3-27 Dual Port Block Memory



All the configuration options for the dual port mode are as shown in Table 3-9 .

Table 3-9 Dual Port Memory Configuration

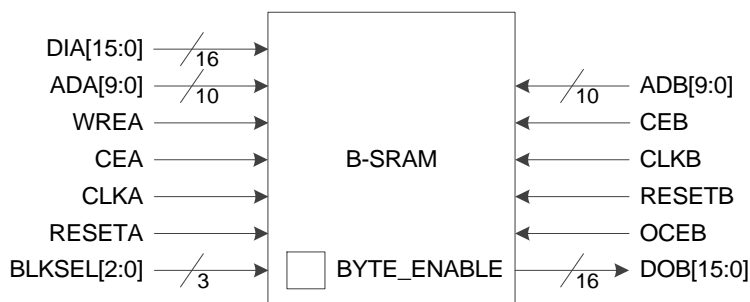
Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Data Depth
DP	B-SRAM_16K_D1	16K	16K x 1	16384	1
	B-SRAM_8K_D2	16K	8K x 2	8192	2
	B-SRAM_4K_D4	16K	4K x 4	4096	4
	B-SRAM_2K_D8	16K	2K x 8	2048	8
	B-SRAM_1K_D16	16K	1K x 16	1024	16
DPX9	B-SRAM_2K_D9	18K	2K x 9	2048	9
	B-SRAM_1K_D18	18K	1K x 18	1024	18

### Semi-Dual Port Mode

The figure below shows the semi Dual Port 1K x 16bit mode. It supports read and write at the same time on different ports. It is not possible to write and read to the same port at the same time. The system

only supports write on Port A, read on Port B.

**Figure 3-28 Semi Dual Port Block Memory**



All the configuration options for the dual port mode are as shown in Table 3-10.

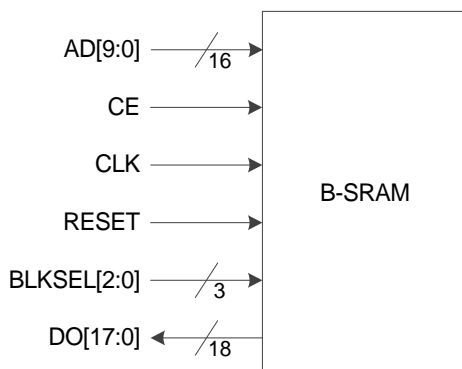
**Table 3-10Semi Dual Port Memory Configuration**

Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Data Depth
SDP	B-SRAM_16K_SD1	16K	16K x 1	16,384	1
	B-SRAM_8K_SD2	16K	8K x 2	8,192	2
	B-SRAM_4K_SD4	16K	4K x 4	4,096	4
	B-SRAM_2K_SD8	16K	2K x 8	2,048	8
	B-SRAM_1K_SD16	16K	1K x 16	1,024	16
	B-SRAM_512_SD32	16K	512 x 32	512	32
SDPX9	B-SRAM_2K_SD9	18K	2K x 9	2,048	9
	B-SRAM_1K_SD18	18K	1K x 18	1,024	18
	B-SRAM_512_SD36	18K	512 x 36	512	36

### Read Only

B-SRAM can be configured as ROM, as shown in Figure 3-29. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization completes during the device power-on process.

**Figure 3-29 ROM Block Memory**



Each B-SRAM can be configured as one 16 Kbits ROM. Table 3-11 lists all the configuration options for the ROM mode.

**Table 3-11 Block ROM Configuration**

Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Data Depth
ROM	B-SRAM_16K_O1	16K	16K x 1	16,384	1
	B-SRAM_8K_O2	16K	8K x 2	8,192	2
	B-SRAM_4K_O4	16K	4K x 4	4,096	4
	B-SRAM_2K_O8	16K	2K x 8	2,048	8
	B-SRAM_1K_O16	16K	1K x 16	1,024	16
	B-SRAM_512_O32	16K	512 x 32	512	32
ROMX9	B-SRAM_2K_O9	18K	2K x 9	2,048	9
	B-SRAM_1K_O18	18K	1K x 18	1,024	18
	B-SRAM_512_O36	18K	512 x 36	512	36

**Note!**

In the ROM mode, the RESET signal can only reset the input and output registers. It cannot clear the ROM content.

### 3.5.9 B-SRAM Operation Modes

B-SRAM supports five different operations, including two read operations (Bypass Mode and Pipeline Read Mode) and three write operations (Normal Write Mode, Write-through Mode, and Read-before-write Mode).

#### Read Mode

Read data from the B-SRAM via output registers or without using the registers.

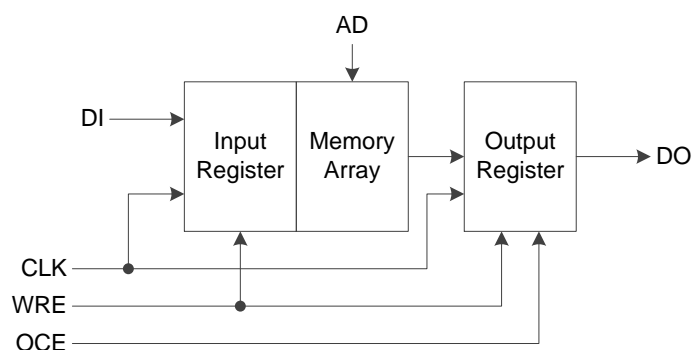
#### Pipeline Mode

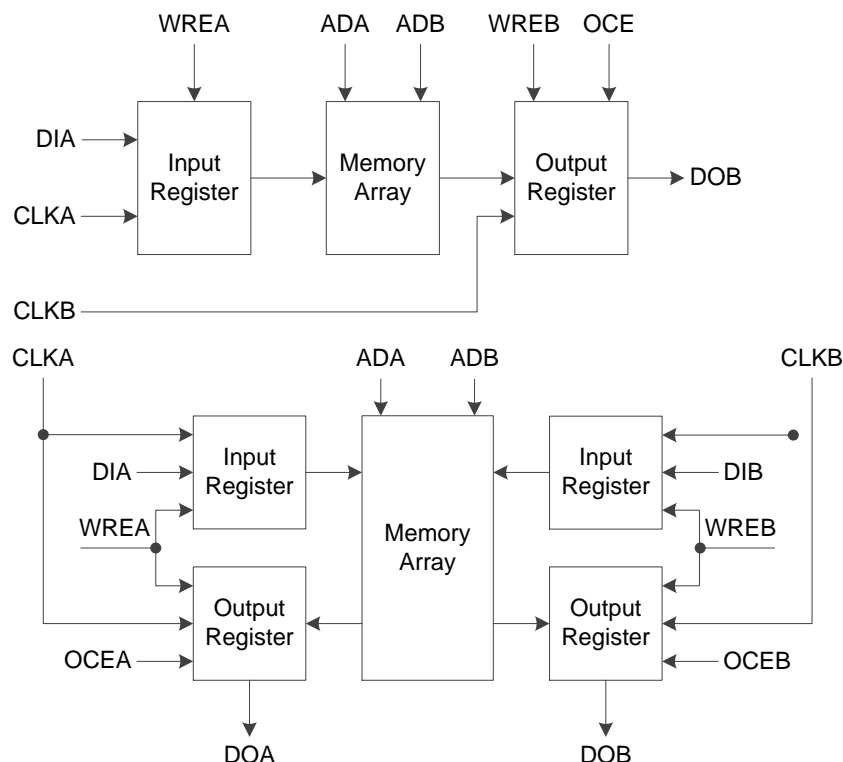
While writing in the B-SRAM, the output register and pipeline register are also being written. The data bus can be up to 36 bits in this mode.

#### Bypass Mode

The output register is not used. The data is kept in the output of the memory array.

**Figure 3-30 Pipeline Mode in Single Port, Dual Port and Semi Dual Port**





## Write Mode

### NORMAL WRITE MODE

In this mode, when the user writes data to one port, and the output data of this port does not change. The data written in will not appear at the read port.

### WRITE-THROUGH MODE

In this mode, when the user writes data to one port, and the data written in will also appear at the output of this port.

### READ-BEFORE-WRITE MODE

In this mode, when the user writes data to one port, and the data written in will be stored in the memory according to the address. The original data in this address will appear at the output of this port.

## 3.5.10 Clock Operations

Table 3-12 lists the clock operations in different B-SRAM modes:

**Table 3-12 Clock Operations in Different B-SRAM Modes**

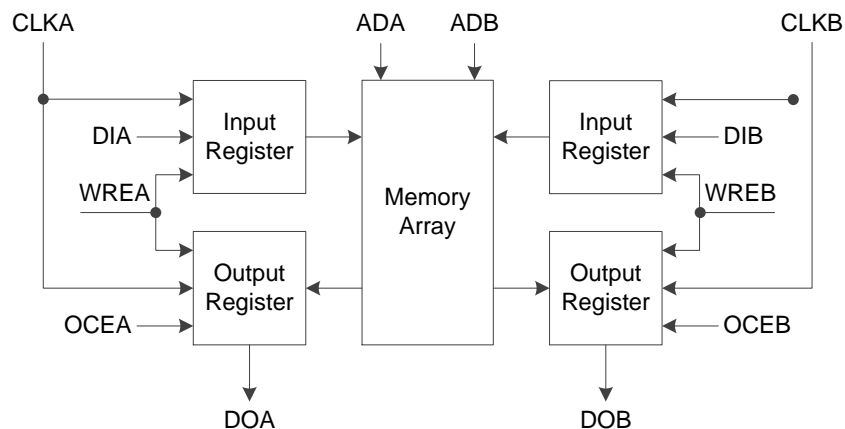
Clock Operations	Dual Port Mode	Semi-dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes



### Independent Clock Mode

Figure 3-31 shows the independent clocks in the dual port mode with each port with one clock. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

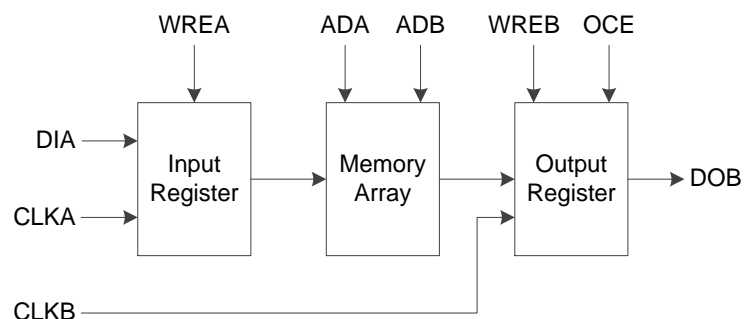
Figure 3-31 Independent Clock Mode



### Read/Write Clock Operation

Figure 3-32 shows the read/write clock operations in the semi-dual port mode with one clock at each port. The write clock (CLKA) controls Port A data inputs, write address and read/write enable signals. The read clock (CLKB) controls Port B data output, read address, and read enable signals.

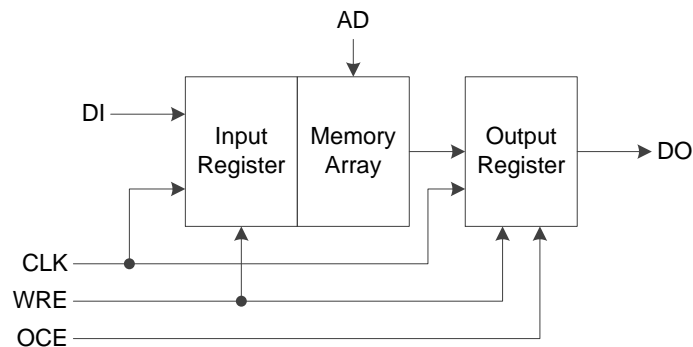
Figure 3-32 Read/Write Clock Mode



### Single Port Clock Mode

Figure 3-33 shows the clock operation in single port mode.

Figure 3-33 Single Port Clock Mode



## 3.6 User Flash

### 3.6.1 Introduction

The GW1NR series of FPGA products support User Flash. The features are as following:

- 10,000 write cycles
- Greater than 10 years data retention at +85 °C
- Page erase capability: 2,048 bytes per page
- Fast page erasure/word programming operation
- Clock frequency: 40 MHz
- Word programming time: ≤16 μs
- Page erasure time: ≤120 ms
- Electric current
  - Read current/duration: 2.19 mA/25 ns ( $V_{CC}$ ) & 0.5 mA/25 ns ( $V_{CCX}$ ) (MAX)
  - Program/erase operation: 12/12 mA (MAX)

## 3.6.2 User Flash Ports

Figure 3-34 GW1NR User Flash Ports

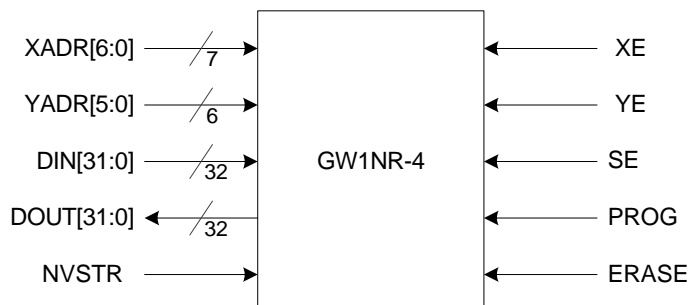


Table 3-13 Flash Module Signal Description

Pin name <sup>1</sup>	I/O	Description
XADR[5:0] <sup>2</sup>	I	X address bus, used to select one row within a page of main memory block.
YADR[5:0] <sup>2</sup>	I	Y address bus, used to select one column within a row of memory block.
DIN[31:0]	I	Data input bus.
DOUT[31:0]	O	Data output bus.
XE <sup>2</sup>	I	X address enable signal, if XE is 0, all of row addresses are not enabled.
YE <sup>2</sup>	I	Y address enable signal, if YE is 0, all of column addresses are not enabled.
SE <sup>2</sup>	I	Detect amplifier enable signal, active high.
ERASE	I	Erase port, active-high.
PROG	I	Programming port, active-high.
NVSTR	I	Flash data storage port, active-high.

**Note!**

- [1] Port names of Control, address, and data signals;
- [2] The read operation is valid only if  $XE = YE = V_{CC}$  and SE meets the pulse timing requirements ( $T_{pws}$ ,  $T_{nws}$ ). The address of read data is determined by XADR [5: 0] and YADR [5: 0].

### 3.6.3 User Flash Mode Truth Table

#### User Modes

Table 3-14 Truth Table in User Mode

Mode	XE	YE	SE	PROG	ERASE	NVSTR
Read mode	H	H	H	L	L	L
Programming mode	H	H	L	H	L	H
Page erasure mode	H	L	L	L	H	H

#### Note!

“H” and “L” means high level and low level of VCC.

## 3.7 DSP

### 3.7.1 Introduction

The GW1NR series of FPGA products have abundant DSP modules. Gowin DSP solutions can meet user demands for high performance digital signal processing design, such as FIR, FFT, etc. DSP blocks have the advantages of stable timing performance, high-usage, and low-power.

DSP offers the following functions:

- Multiplier with three widths: 9-bit, 18-bit, 36-bit
- 54-bit ALU
- Multipliers cascading to support wider data
- Barrel shifter
- Adaptive filtering through signal feedback
- Computing with options to round to a positive number or a prime number
- Supports pipeline mode and bypass mode.

#### Macro

DSP blocks are embedded as a row in the FPGA array. Each DSP occupies nine CFU columns. Each DSP block contains two Macro, and each Macro contains two pre-adders, two 18 x 18 bit multipliers, and one three-input ALU.

Figure 3-35 shows the structure of one Macro:

Figure 3-35 DSP Macro

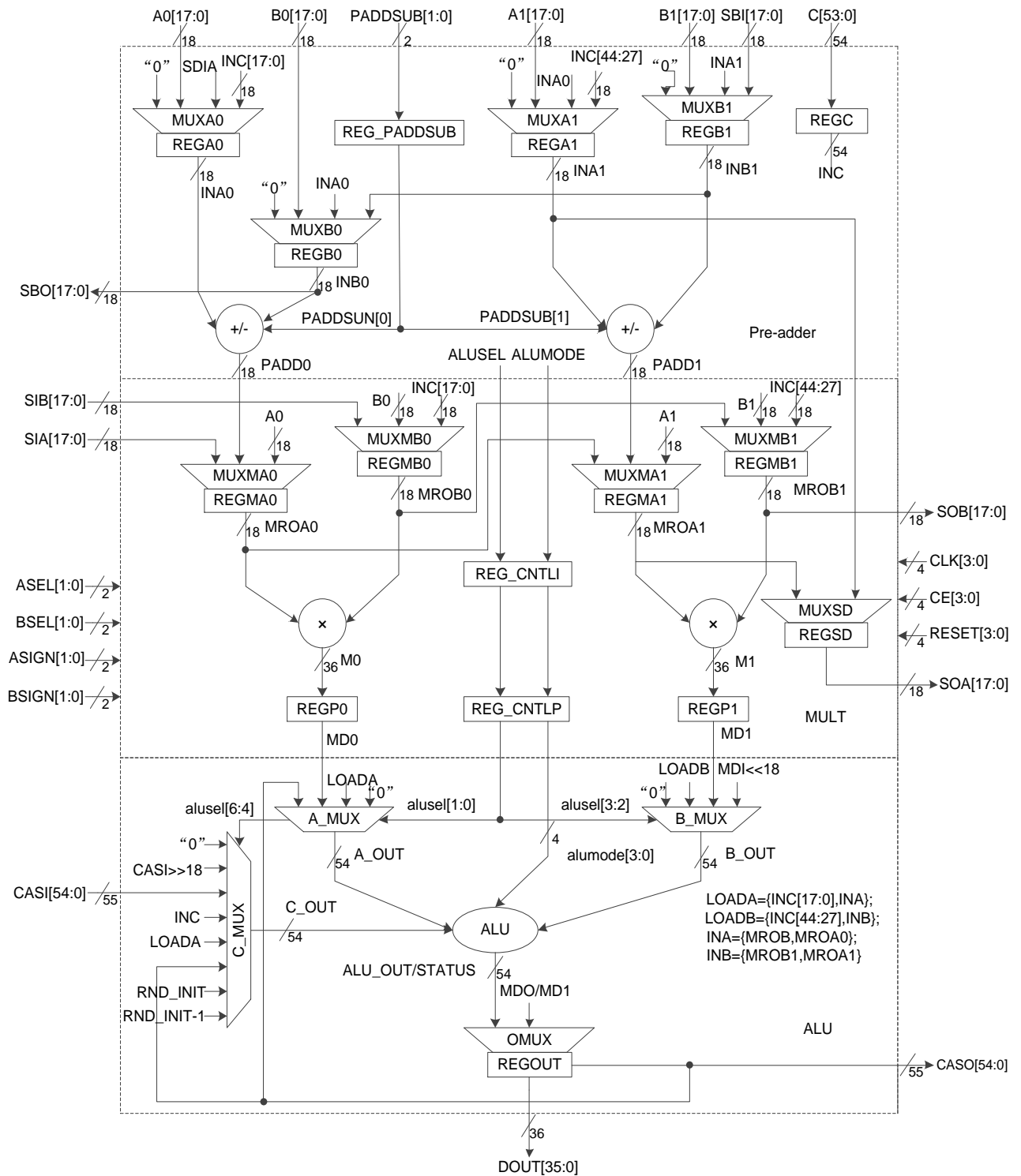


Table 3-15 shows DSP ports description.

Table 3-15 DSP Ports Description

Port Name	I/O	Description
A0[17:0]	I	18-bit data input A0
B0[17:0]	I	18-bit data input B0
A1[17:0]	I	18-bit data input A1
B1[17:0]	I	18-bit data input B1

Port Name	I/O	Description
C[53:0]	I	54-bit data input C
SIA[17:0]	I	Shift data input A, used for CASCADE connection. The input signal SIA is directly connected to the output signal SOA of previously adjacent DSP and the delay from SIA to SOA inside a DSP is one clock cycle.
SIB[17:0]	I	Shift data input B, used for CASCADE connection. The input signal SIB is directly connected to the output signal SOB of previously adjacent DSP and the delay from SIB to SOB inside a DSP is one clock cycle.
SBI[17:0]	I	Pre - adder logic shift input, backward direction.
CASI[54:0]	I	ALU input from previous DSP block, used for cascade connection.
PADDSI0[1:0]	I	Source select for Multiplier or pre-adder input A
BSEL[1:0]	I	Source select for Multiplier input B
ASIGN[1:0]	I	Sign bit for input A
BSIGN[1:0]	I	Sign bit for input B
PADDSUB[1:0]	I	Operation control signals of pre-adder, used for pre-adder logic add/subtract selection
CLK[3:0]	I	Clock input
CE[3:0]	I	Clock Enable
RESET[3:0]	I	Reset input, synchronous or asynchronous
SOA[17:0]	O	Shift data output A
SOB[17:0]	O	Shift data output B
SBO[17:0]	O	Pre - adder logic shift output, backward direction.
DOUT[35:0]	O	DSP output data
CASO[54:0]	O	ALU output to next DSP block for cascade connection, the highest bit is sign-extended.

Table 3-16 Internal Registers Description

Register	Description and Associated Attributes
A0 register	Registers for A0 input
A1 register	Registers for A1 input
B0 register	Registers for B0 input
B1 register	Registers for B1 input
C register	C register
P1_A0 register	Registers for A0 input of left multiplier
P1_A1 register	Registers for A1 input of right multiplier
P1_B0 register	Registers for B0 input of left multiplier
P1_B1 register	Registers for B1 input of right multiplier
P2_0 register	Registers for pipeline of left multiplier
P2_1 register	Registers for pipeline of right multiplier
OUT register	Registers for DOUT output
OPMODE register	Registers for operation mode control
SOA register	Registers for shift output at port SOA

## PADD

Each DSP macro features two units of pre-adders to implement pre-add, pre-subtraction, and shifting.

PADD locates at the first stage with two inputs:

- Parallel 18-bit input B or SBI;
- Parallel 18-bit input A or SIA.

Each input end supports pipeline mode and bypass mode.

GOWINSEMI PADD can be used as function block independently, which supports 9-bit and 18-bit width.

### **MULT**

Multipliers locate after the pre-adder. Multipliers can be configured as 9 x 9, 18 x 18, 36 x 18 or 36 x 36. Pipeline Mode and Bypass Mode are supported both in input and output ports. The configuration modes that a macro supports include:

- One 18 x 36 multiplier
- Two 18 x 18 multipliers
- Four 9 x 9 multipliers

Two adjacent DSP macros can form a 36 x 36 multiplier.

### **ALU**

Each Macro has one 54 bits ALU54, which can further enhance MULT's functions. Registered Mode and Bypass Mode are supported both in input and output ports. The functions are as following:

- Multiplier output data / 0, addition/subtraction operations for data A and data B;
- Multiplier output data / 0, addition/subtraction operations for data B and bit C;
- Addition/subtraction operations for data A, data B, and bit C;

## **3.7.2 DSP Operations**

- Multiplier
- Accumulator
- MULTADDALU

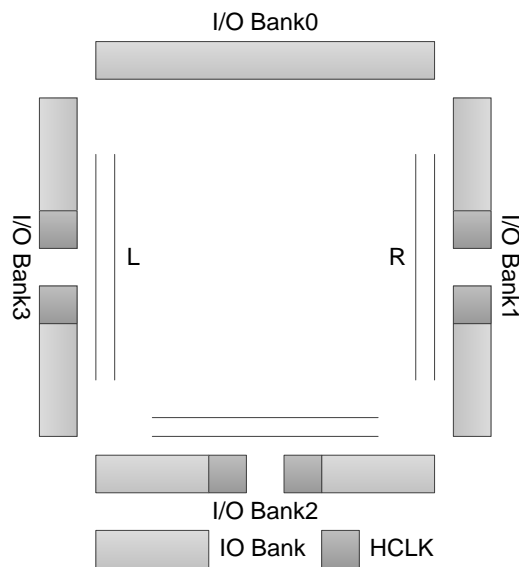
## 3.8 Clock

The clock resources and wiring are critical for high-performance applications in FPGA. The GW1NR series of FPGA products provide the global clock network (GCLK) which connects to all the registers directly. Besides the global clock network, the GW1NR series of FPGA products provide high-speed clock HCLK. PLL, DLL, etc are also provided.

### 3.8.1 Global Clock

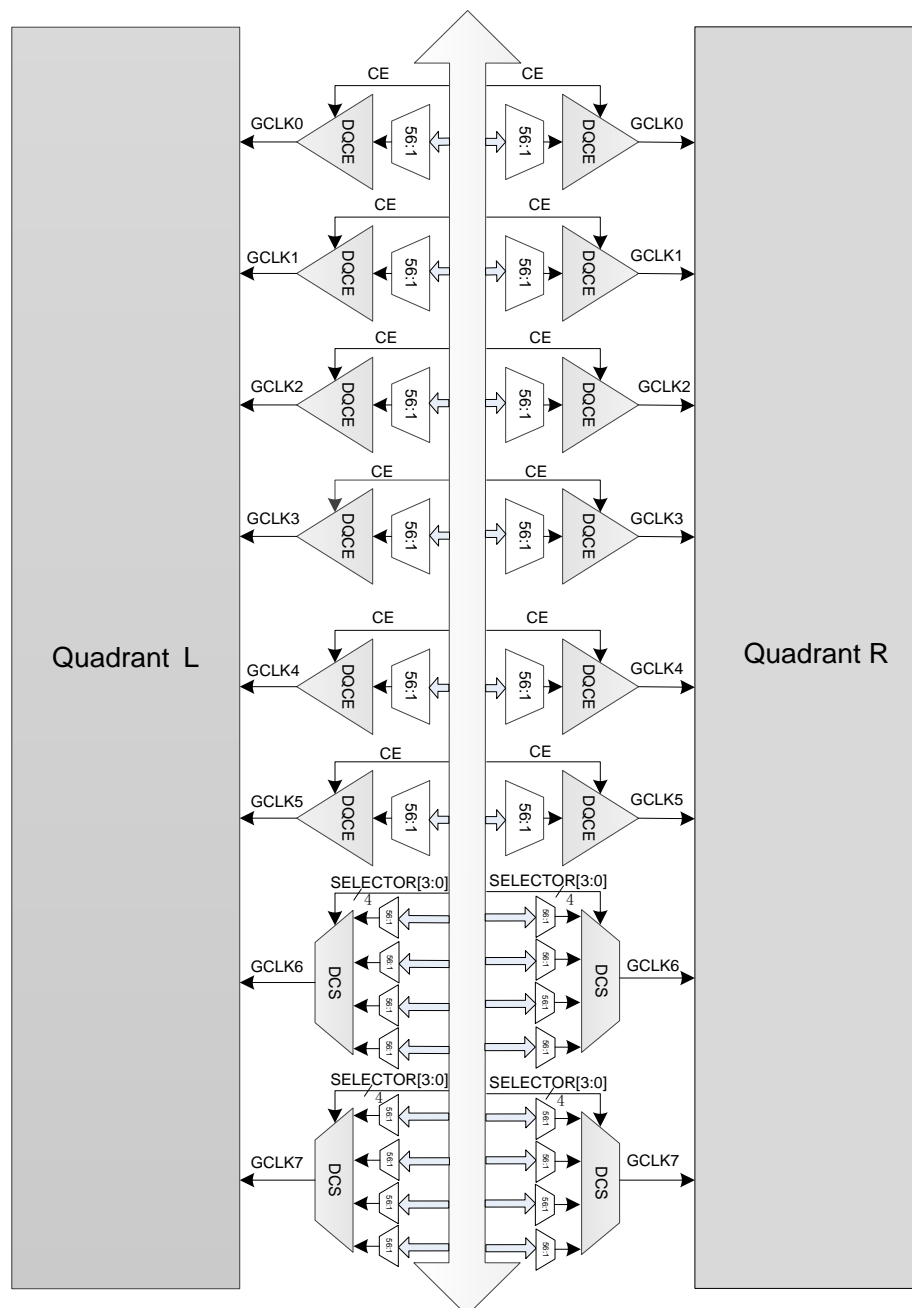
The GCLK is distributed in GW1NR series of FPGA products as two quadrants, L and R. Each quadrant provides eight GCLKs. The optional clock resources of GCLK can be pins or CRU. Users can employ dedicated pins as clock resources to achieve better timing.

Figure3-36 GW1NR-4/ GW1NR-4B Clock Resources

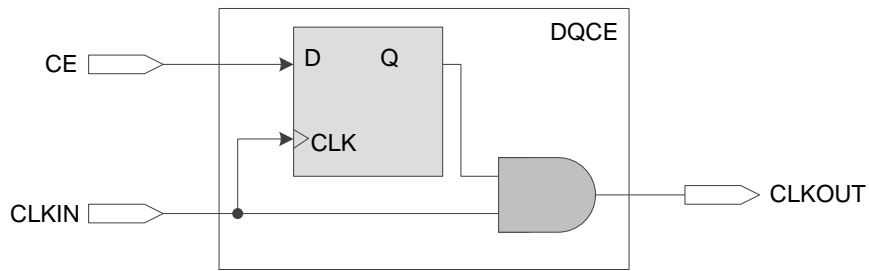




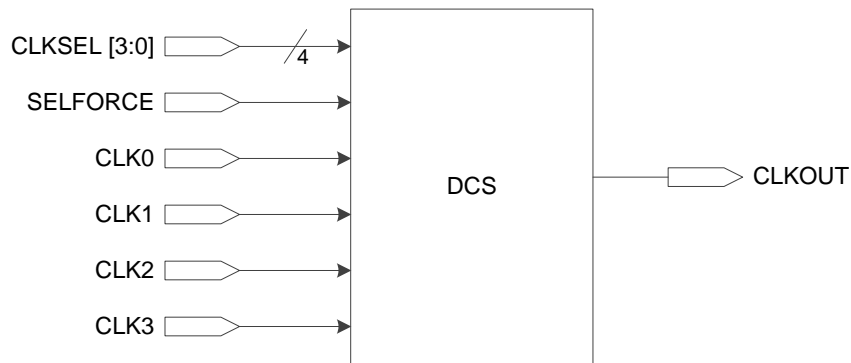
### Figure 3-37 GCLK Quadrant Distribution



GCLK0~GCLK5 can be turned on or off by dynamic quadrant clock enable (DQCE). When GCLK0~GCLK5 in the quadrant is off, all the logic driven by it will not toggle; therefore, lower power can be achieved.

**Figure 3-38 DQCE Concept**

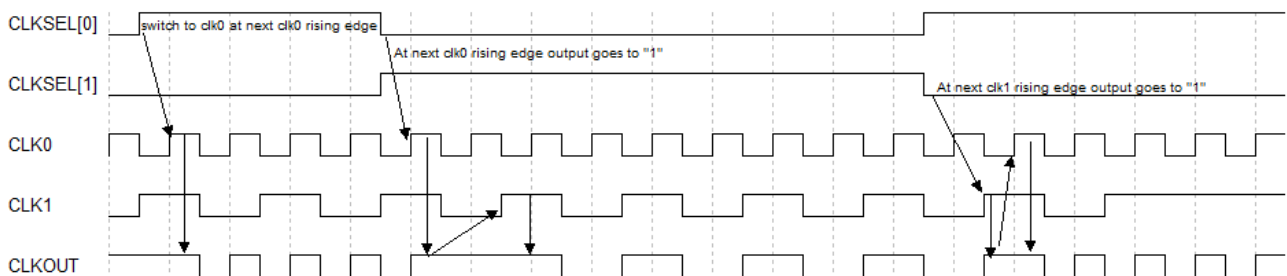
GCLK6~GCLK7 of each quadrant is controlled by the DCS, as shown in Figure 3-39. Select dynamically between CLK0~CLK3 by CRU, and output a glitch-free clock.

**Figure 3-39 DCS Concept**

DCS can be configured in the following modes:

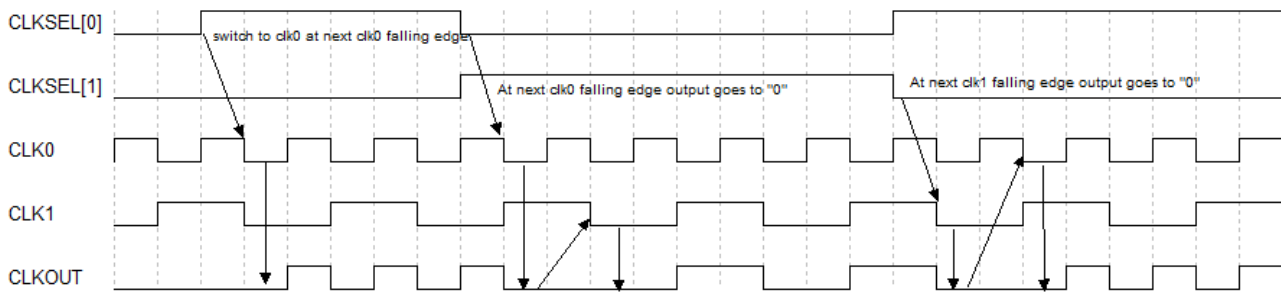
#### 1. DCS Rising Edge

Stay as 1 after current selected clock rising edge, and the new select clock will be effective after its first rising edge, as shown in Figure 3-40.

**Figure 3-40 DCS Rising Edge**

#### 2. DCS Falling Edge

Stay as 0 after current selected clock falling edge, and the new select clock will be effective after its first falling edge, as shown in Figure 3-41.

**Figure 3-41 DCS Falling Edge**

### 3. Clock Buffer Mode

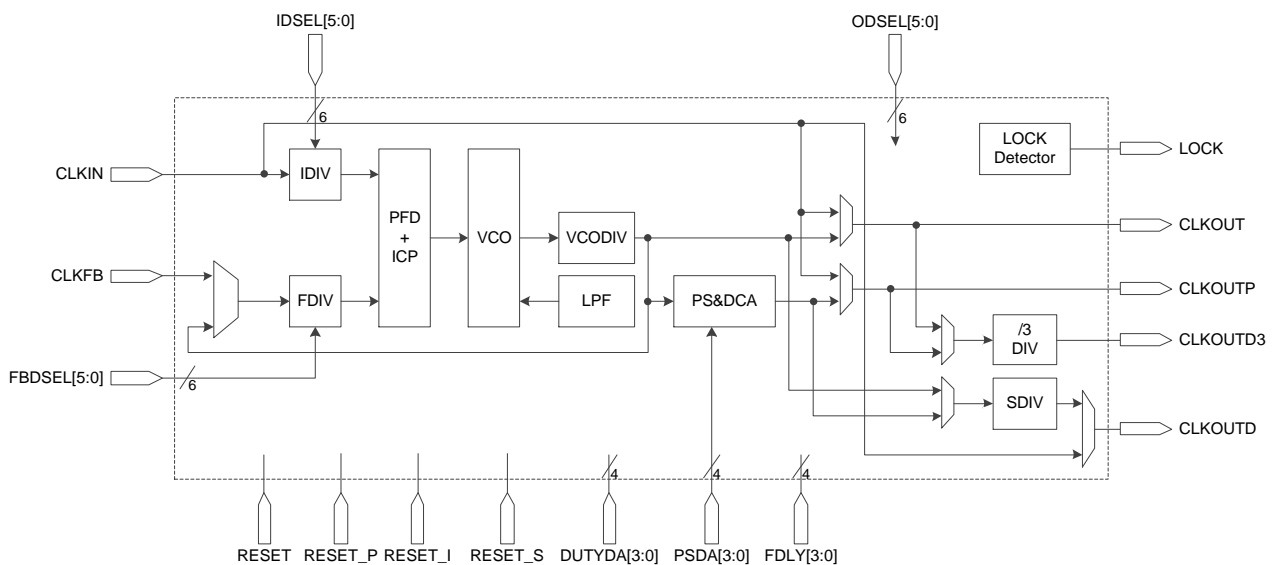
In this mode, DCS acts as a clock buffer.

## 3.8.2 PLL

Phase-locked Loop (PLL) is one kind of a feedback control circuit. The frequency and phase of the internal oscillator signal is controlled by the external input reference clock.

PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted by configuring the parameters.

See Figure 3-42 for the PLL structure.

**Figure 3-42 PLL Structure**

The PLL reference clock source can come from an external PLL pin or from internal routing GCLK, HCLK, or general data signal. PLL feedback signal can come from the external PLL feedback input or from internal routing GCLK, HCLK, or general data signal.

PLL features are as follows:

- Input frequency: 3 MHz~450 MHz
- VCO vibration frequency: 400 MHz~900 MHz

- CLKOUT output frequency: 3.125 MHz~450 MHz

PLL can adjust the frequency of the input clock CLKIN (multiply and division). The formulas for doing so are as follows:

1.  $f_{CLKOUT} = (f_{CLKIN} * FDIV) / IDIV$
2.  $f_{VCO} = f_{CLKOUT} * ODIV$
3.  $f_{CLKOUTD} = f_{CLKOUT} / SDIV$
4.  $f_{PFD} = f_{CLKIN} / IDIV = f_{CLKOUT} / FDIV$

**Note!**

- $f_{CLKIN}$ : The frequency of the input clock CLKIN
- $f_{CLKOUT}$ : The clock frequency of CLKOUT and CLKOUTP
- $f_{CLKOUTD}$ : The clock frequency of CLKOUTD, and CLKOUTD is the clock CLKOUT after division
- $f_{PFD}$ : PFD Phase Comparison Frequency

Adjust IDIV, FDIV, ODIV, and SDIV to achieve the required clock frequency.

See Table 3-17 for a definition of the PLL ports.

**Table 3-17 PLL Ports Definition**

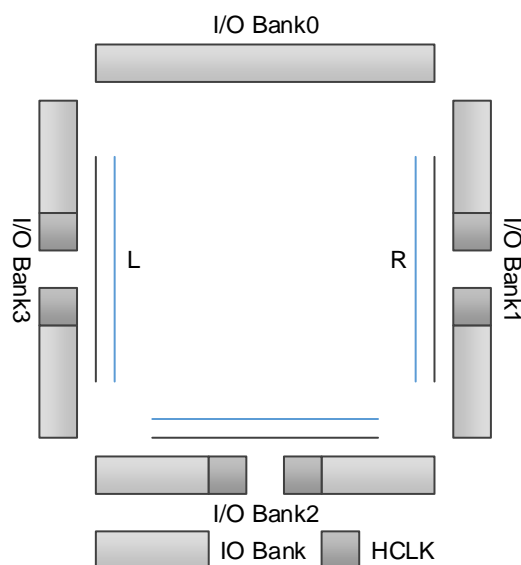
Port Name	Signal	Description
CLKIN [5: 0]	I	Reference clock input
CLKFB	I	Feedback clock input
RESET	I	PLL reset
RESET_P	I	PLL Power Down
RESET_I	I	IDIV reset
RESET_S	I	SDIV and DIV3 reset
INSEL[2: 0]	I	Dynamic clock control selector: 0~5
IDSEL [5: 0]	I	Dynamic IDIV control: 1~64
FBDSEL [5: 0]	I	Dynamic FDIV control:1~64
PSDA [3: 0]	I	Dynamic phase control (rising edge effective)
DUTYDA [3: 0]	I	Dynamic duty cycle control (falling edge effective)
FDLY[3:0]	I	CLKOUTP dynamic delay control
CLKOUT	O	Clock output with no phase and duty cycle adjustment
CLKOUTP	O	Clock output with phase and duty cycle adjustment
CLKOUTD	O	Clock divider from CLKOUT and CLKOUTP (controlled by SDIV)
CLKOUTD3	O	clock divider from CLKOUT and CLKOUTP (controlled by DIV3 with the constant division value 3)
LOCK	O	PLL lock status: 1: locked, 0: unlocked

### 3.8.3 HCLK

HCLK is the high-speed clock in the GW1NR series of FPGA products. It can support high-performance data transfer and is mainly suitable for

source synchronous data transfer protocols. See Figure Figure 3-43.

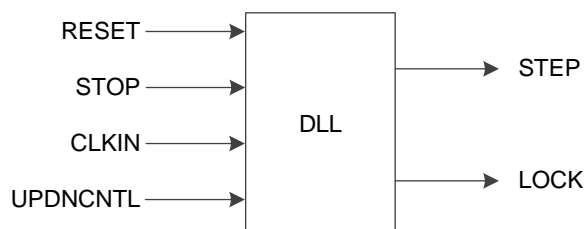
**Figure 3-43 GW1NR HCLK Distribution**



### 3.8.4 DLL

The GW1NR series of FPGA products support DLL. For DLL function, see Figure 3-44.

**Figure 3-44 GW1NR DLL Function**



The source of CLKIN can come from GCLK and the neighboring HCLK.

The calculated STEP will be sent to the neighboring Banks. For example, the signal STEP of DLL can be sent to HCLK in Bank2. At the same time, the signal STEP can also be sent to the user logic through the CRU.

## 3.9 Long Wire (LW)

As a supplement to the CRU, the GW1NR series of FPGA products provides another routing resource, Long wire, which can be used as clock, clock enable, set/reset, or other high fan out signals.

### 3.10 Global Set/Reset (GSR)

A global set/reset (GSR) network is built into the GW1NR series of

FPGA product. There is a direct connection to core logic. It can be used as asynchronous/synchronous set or asynchronous/synchronous reset, registers in CFU and I/O can be configured independently.

## 3.11 Programming Configuration

The GW1NR series of FPGA products support SRAM and Flash. The Flash programming mode supports on-chip Flash and off-chip Flash. The GW1NR series of FPGA products support DUAL BOOT, providing a selection for users to backup data to off chip Flash according to requirements.

Besides JTAG, the GW1NR series of FPGA products also supports GOWINSEMI's own configuration mode: GowinCONFIG (AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU). All the devices support JTAG and AUTO BOOT. For the detailed information, please refer to *GW1NR series FPGA Products Programming and Configuration User Guide*.

### 3.11.1 SRAM Configuration

When you adopt SRAM to configure the device, every time the device is powered on, the bit stream file needs to be downloaded to configure the device.

### 3.11.2 Flash Configuration

The Flash configuration data is stored in the on-chip flash. Each time the device is powered on, the configuration data is transferred from the Flash to the SRAM, which controls the working of the device. This mode can complete configuration within a few ms, and is referred to as "Quick Start".

B version of GW1NR devices has the feature of transparent transmission. That is to say, the B version device can program the on-chip Flash or off-chip Flash via the JTAG interface without affecting the current working state. During programming, the B version device works according to the previous configuration. After programming, provide one low pulse for RECONFIG\_N to complete the online upgrade. This feature applies to the applications with long online time and irregular upgrades.

The GW1NR series of FPGA products also support off-chip Flash configuration and dual-boot. Please refer to *Gowin FPGA Products Programming and Configuration Guide* for more detailed information.

## 3.12 On Chip Oscillator

There is an internal oscillator in each of the GW1NR series of FPGA product. During the configuration process, it can provide a clock for the MSPI mode. See Table 3-18 for the output frequency.

**Table 3-18 GW1NR-4/4B Oscillator Output Frequency Options**

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.1MHz <sup>1</sup>	8	7.8MHz	16	15.6MHz
1	5.4MHz	9	8.3MHz	17	17.9MHz
2	5.7MHz	10	8.9MHz	18	21MHz
3	6.0MHz	11	9.6MHz	19	25MHz
4	6.3MHz	12	10.4MHz	20	31.3MHz
5	6.6MHz	13	11.4MHz	21	41.7MHz
6	6.9MHz	14	12.5MHz	22	62.5MHz
7	7.4MHz	15	13.9MHz	23	125MHz <sup>2</sup>

**Table 3-19 GW1NR-9 Oscillator Output Frequency Options**

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.5MHz <sup>1</sup>	8	7.8MHz	16	15.6MHz
1	5.4MHz	9	8.3MHz	17	17.9MHz
2	5.7MHz	10	8.9MHz	18	21MHz
3	6.0MHz	11	9.6MHz	19	25MHz
4	6.3MHz	12	10.4MHz	20	31.3MHz
5	6.6MHz	13	11.4MHz	21	41.7MHz
6	6.9MHz	14	12.5MHz	22	62.5MHz
7	7.4MHz	15	13.9MHz	23	125MHz <sup>2</sup>

**Note!**

- [1] Default Frequency.
- [2] 125MHz is not suitable for MSPI programming mode.

The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters.

The following formula is employed to get the output clock frequency for GW1NR-9 devices:

$$f_{\text{out}} = 250\text{MHz}/\text{Param}$$

The following formula is employed to get the output clock frequency for GW1NR-4/GW1NR-4B device:

$$f_{\text{out}} = 210\text{MHz}/\text{Param}$$

“Param” is the configuration parameter with a range of 2~128. It supports even number only.

# 4 AC/DC Characteristics

## Note!

Users should ensure GOWINSEMI products are always used within recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI does not guarantee that all devices will operate as expected beyond the standard operating conditions and range.

## 4.1 Operating Conditions

**Table 4-1 Absolute Max. Ratings**

Name	Description	Min.	Max.
V <sub>CC</sub>	LV: Core Power	-0.5V	1.32V
	UV:Core Power	-0.5V	3.75V
V <sub>CCO</sub>	I/O Bank Power	-0.5V	3.75V
V <sub>CCX</sub>	Auxiliary Power	-0.5V	3.75V
Operating Temperature (Industrial)	Operating Temperature	-40 °C	+125 °C
Storage Temperature	Storage Temperature	-65 °C	+150 °C

**Table 4-2 Recommended Operating Conditions**

Name	Description	Min.	Max.
V <sub>CC</sub>	LV: Core Power	1.14V	1.26V
	UV:Core Power	2.375V	3.465V
V <sub>CCOx</sub>	I/O Bank Power	1.14V	3.465V
V <sub>CCX</sub>	Auxiliary voltage	2.375V	3.465V
T <sub>JCOM</sub>	Junction temperature Commercial operation	0°C	+85°C
T <sub>JIND</sub>	Junction temperature Industrial operation	-40°C	+100°C
T <sub>RAMP</sub>	Power supply ramp rates for all power supplies	0.01mV/μs	10mV/μs



**Table 4-3 Hot Socket Specifications**

Name	Description	Condition	Max.
$I_{HS}$	Input or I/O leakage current (Input or I/O leakage current)	$V_{IN}=V_{IL}$ (MAX)	TBD

## 4.2 ESD

**Table 4-4 GW1NR ESD - HBM**

Device	GW1NR-4/ GW1NR-4B	GW1NR-9
QN88	HBM>1,000V	HBM>1,000V
MG81	HBM>1,000V	-
LQ144	-	HBM>1,000V

**Table 4-5 GW1NR ESD - CDM**

Device	GW1NR-4/ GW1NR-4B	GW1NR-9
QN88	CDM>500V	CDM>500V
<b>MG81</b>	CDM>500V	-
LQ144	-	CDM>500V

Table 4-6 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
$I_{IL}, I_{IH}$	Input or I/O leakage	$V_{CCO} < V_{IN} < V_{IH} \text{ (MAX)}$	-	-	210 $\mu\text{A}$
		$0V < V_{IN} < V_{CCO}$	-	-	10 $\mu\text{A}$
$I_{PU}$	I/O Active Pull-up Current (I/O Active Pull-up Current)	$0 < V_{IN} < 0.7V_{CCO}$	-30 $\mu\text{A}$	-	-150 $\mu\text{A}$
$I_{PD}$	I/O Active Pull-down Current (I/O Active Pull-up Current)	$V_{IL} \text{ (MAX)} < V_{IN} < V_{CCO}$	30 $\mu\text{A}$	-	150 $\mu\text{A}$
$I_{BHLS}$	Bus Hold Low Sustaining Current (Bus Hold Low Sustaining Current)	$V_{IN} = V_{IL} \text{ (MAX)}$	30 $\mu\text{A}$	-	-
$I_{BHHO}$	Bus Hold High Sustaining Current (Bus Hold Low Sustaining Current)	$V_{IN} = 0.7V_{CCO}$	-30 $\mu\text{A}$	-	-
$I_{BHLO}$	Bus Hold Low Overdrive Current (Bus Hold Low Sustaining Current)	$0 \leq V_{IN} \leq V_{CCO}$	-	-	150 $\mu\text{A}$
$I_{BHHO}$	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{CCO}$	-	-	-150 $\mu\text{A}$
$V_{BHT}$	Bus hold trip points		$V_{IL} \text{ (MAX)}$	-	$V_{IH} \text{ (MIN)}$
$C_1$	I/O Capacitance (I/O Capacitance)			5 pF	8 pF
$V_{HYST}$	Hysteresis for Schmitt Trigger inputs	$V_{CCO} = 3.3V, \text{ Hysteresis} = \text{Large}$	-	482mV	-
		$V_{CCO} = 2.5V, \text{ Hysteresis} = \text{Large}$	-	302mV	-
		$V_{CCO} = 1.8V, \text{ Hysteresis} = \text{Large}$	-	152mV	-
		$V_{CCO} = 1.5V, \text{ Hysteresis} = \text{Large}$	-	94mV	-
		$V_{CCO} = 3.3V, \text{ Hysteresis} = \text{Small}$	-	240mV	-
		$V_{CCO} = 2.5V, \text{ Hysteresis} = \text{Small}$	-	150mV	-
		$V_{CCO} = 1.8V, \text{ Hysteresis} = \text{Small}$	-	75mV	-
		$V_{CCO} = 1.5V, \text{ Hysteresis} = \text{Small}$	-	47mV	-

Table 4-7 Static Supply Current

Name	Description	LV/UV	Device	Typ.
$I_{CC}$	Core current $V_{CCX} = 3.3V$ , $V_{CCX} = 2.5V$	UV	GW1NR-4	TBD
$I_{CCX}$	$V_{CCX}$ current ( $V_{CCX} = 3.3V$ )	UV	GW1NR-4	TBD
	$V_{CCX}$ current ( $V_{CCX} = 2.5V$ )	UV	GW1NR-4	TBD

I <sub>CCO</sub>	I/O Bank current (V <sub>CCO</sub> =2.5V)	UV	ALL	TBD
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## 4.3 DC Characteristics

Table 4-8 I/O Operating Conditions Recommended

Name	Output V <sub>CCO</sub> (V)			Input V <sub>REF</sub> (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.465	-	-	-
LVC MOS33	3.135	3.3	3.465	-	-	-
LVC MOS25	2.375	2.5	2.625	-	-	-
LVC MOS18	1.71	1.8	1.89	-	-	-
LVC MOS15	1.425	1.5	1.575	-	-	-
LVC MOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.465	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.465	1.3	1.5	1
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.465	-	-	-
LVPECL33E	3.135	3.3	3.465	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.465	-	-	-
SSTL33D_II	3.135	3.3	3.465	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

Table 4-9 IOB Single - Ended DC Electrical Characteristic

Name	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub> (Max)	V <sub>OH</sub> (Min)	I <sub>OL</sub> (mA)	I <sub>OH</sub> (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	V <sub>CCO</sub> -0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	V <sub>CCO</sub> -0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	V <sub>CCO</sub> -0.4V	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	V <sub>CCO</sub> -0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V <sub>CCO</sub>	0.65 x V <sub>CCO</sub>	3.6V	0.4V	V <sub>CCO</sub> 0.4V	4	-4
							8	-8
							12	-12
					0.2V	V <sub>CCO</sub> -0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V <sub>CCO</sub>	0.65 x V <sub>CCO</sub>	3.6V	0.4V	V <sub>CCO</sub> -0.4V	4	-4
							8	-8
					0.2V	V <sub>CCO</sub> -0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V <sub>CCO</sub>	0.65 x V <sub>CCO</sub>	3.6V	0.4V	V <sub>CCO</sub> -0.4V	2	-2
							6	-6
					0.2V	V <sub>CCO</sub> -0.2V	0.1	-0.1
PCI33	-0.3V	0.3 x V <sub>CCO</sub>	0.5 x V <sub>CCO</sub>	3.6V	0.1 V <sub>CCO</sub> x	0.9 x V <sub>CCO</sub>	1.5	-0.5
SSTL33_I	-0.3V	V <sub>REF</sub> -0.2V	V <sub>REF</sub> +0.2V	3.6V	0.7	V <sub>CCO</sub> -1.1V	8	-8
SSTL25_I	-0.3V	V <sub>REF</sub> -0.18V	V <sub>REF</sub> +0.18V	3.6V	0.54V	V <sub>CCO</sub> -0.62V	8	-8
SSTL25_II	-0.3V	V <sub>REF</sub> -0.18V	V <sub>REF</sub> +0.18V	3.6V	NA	NA	NA	NA
SSTL18_II	-0.3V	V <sub>REF</sub> -0.125V	V <sub>REF</sub> +0.125V	3.6V	NA	NA	NA	NA
SSTL18_I	-0.3V	V <sub>REF</sub> -0.125V	V <sub>REF</sub> +0.125V	3.6V	0.40V	V <sub>CCO</sub> -0.40V	8	-8
SSTL15	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	3.6V	0.40V	V <sub>CCO</sub> -0.40V	8	-8
HSTL18_I	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	3.6V	0.40V	V <sub>CCO</sub> -0.40V	8	-8
HSTL18_II	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	3.6V	NA	NA	NA	NA
HSTL15_I	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	3.6V	0.40V	V <sub>CCO</sub> -0.40V	8	-8
HSTL15_II	-0.3V	V <sub>REF</sub> -0.1V	V <sub>REF</sub> + 0.1V	3.6V	NA	NA	NA	NA

**Table 4-10 IOB Differential Electrical Characteristics**  
LVDS25 (GW1NR-1 does not support.)

Name	Description	Condition	Min.	Typ.	Max.	Unit
$V_{INA}, V_{INB}$	Input Voltage (Input Voltage)		0	-	2.4	V
$V_{CM}$	Input Common Mode Voltage (Input Common Mode Voltage)	Half the Sum of the Two Inputs	0.05	-	2.35	V
$V_{THD}$	Differential Input Threshold	Difference Between the Two Inputs	$\pm 100$	-	-	mV
$I_{IN}$	Input Current	Power On or Power Off	-	-	$\pm 10$	$\mu A$
$V_{OH}$	Output High Voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100\Omega$	-	-	1.60	V
$V_{OL}$	Output Low Voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100\Omega$	0.9	-	-	V
$V_{OD}$	Output Voltage Differential	$(V_{OP} - V_{OM}), R_T = 100\Omega$	250	350	450	mV
$\Delta V_{OD}$	Change in $V_{OD}$ Between High and Low		-	-	50	mV
$V_{OS}$	Output Voltage Offset	$(V_{OP} + V_{OM})/2, R_T = 100\Omega$	1.125	1.20	1.375	V
$\Delta V_{OS}$	Change in $V_{OS}$ Between High and Low		-	-	50	mV
$I_S$	Short-circuit current	$V_{OD} = 0V$ output short-circuit	-	-	15	mA

## 4.4 Switching Characteristics

### 4.4.1 Internal Switching Characteristics

**Table 4-11 CFU Block Internal Timing Parameters**

Name	Description	Speed Grade		Unit
		Min	Max	
$t_{LUT4\_CFU}$	LUT4 delay	-	0.674	ns
$t_{LUT5\_CFU}$	LUT5 delay	-	1.388	ns
$t_{LUT6\_CFU}$	LUT6 delay	-	2.01	ns
$t_{LUT7\_CFU}$	LUT7 delay	-	2.632	ns
$t_{LUT8\_CFU}$	LUT8 delay	-	3.254	ns
$t_{SR\_CFU}$	Set/Reset to Register output	-	1.86	ns
$t_{CO\_CFU}$	Clock to Register output	-	0.76	ns

**Table 4-12 B-SRAM Internal Timing Parameters**

Name	Description	Speed Grade		Unit
		Min	Max	
$t_{COAD\_BSRAM}$	Clock to output from read address/data	-	5.10	ns
$t_{COOR\_BSRAM}$	Clock to output from output register	-	0.56	ns

**Table 4-13 DSP Internal Timing Parameters**

Name	Description	Speed Grade		Unit
		Min	Max	
$t_{COIR\_DSP}$	Clock to output from input register	-	4.80	ns
$t_{COPR\_DSP}$	Clock to output from pipeline register	-	2.40	ns
$t_{COOR\_DSP}$	Clock to output from output register	-	0.84	ns

## 4.4.2 External Switching Characteristics

**Table 4-14 External Switching Characteristics**

Name	Description	Device	-4		-5		-6		Unit
			Min	Max	Min	Max	Min	Max	
Clocks	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
Pin-LUT-Pin Delay	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
General I/O Pin Parameters	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

**Table 4-15 On chip Oscillator Output Frequency**

Name	Description	Min.	Typ.	Max.
$f_{MAX}$	Output Frequency (0 to +85°C)	106.25MHz	125MHz	143.75MHz
	Output Frequency (-40 to +100°C)	100MHz	125MHz	150MHz
$t_{DT}$	Output Clock Duty Cycle	43%	50%	57%
$t_{OPJIT}$	Output Clock Period Jitter	0.01UIPP	0.012UIPP	0.02UIPP

## 4.5 User Flash Characteristics

### 4.5.1 DC Characteristics<sup>1</sup>

( $T_J = -40 \sim +100^\circ\text{C}$ ,  $V_{CC} = 1.08 \sim 1.32\text{V}$ ,  $V_{CCX} = 1.62 \sim 3.63\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Table 4-16 User Flash DC Characteristics

Name	Parameter	Max.		Unit	Wake-up Time	Condition
		$V_{CC}^3$	$V_{CCX}$			
Read mode (w/ 25ns) <sup>1</sup>	$I_{CC1}^2$	2.19	0.5	mA	NA	Min. Clcok period, duty cycle 100%, VIN = "1/0"
Write mode		0.1	12	mA	NA	
Erase mode		0.1	12	mA	NA	
Page Erasure Mode		0.1	12	mA	NA	
Read mode static current (25-50ns)	$I_{CC2}$	980	25	$\mu\text{A}$	NA	XE=YE=SE="1", between $T=T_{acc}$ and $T=50\text{ns}$ , I/O=0mA; later than $T=50\text{ns}$ , read mode is turned off, and I/O current is the current of standby mode.
Standby mode	$I_{SB}$	5.2	20	$\mu\text{A}$	0	$V_{SS}$ , $V_{CCX}$ , and $V_{CC}$

**Note!**

- [1] Means the average current, and the peak value is higher than the average one.
- [2] Calculated in different  $T_{new}$  clock periods.
  - $T_{new} < T_{acc}$  is not allowed
  - $T_{new} = T_{acc}$
  - $T_{acc} < T_{new} - 50\text{ns}$ :  $I_{CC1}(\text{new}) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + I_{CC2}$
  - $T_{new} > 50\text{ns}$ :  $I_{CC1}(\text{new}) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + 50\text{ns} \times I_{CC2}/T_{new} + I_{SB}$
  - $t > 50\text{ns}$ ,  $I_{CC2} = I_{SB}$
- [3]  $V_{CC}$  must be greater than 1.08V from the zero wake-up time.

### 4.5.2 Timing Parameters<sup>1,5,6</sup>

( $T_J = -40 \sim +100^\circ\text{C}$ ,  $V_{CC} = 0.95 \sim 1.05\text{V}$ ,  $V_{CCX} = 1.7 \sim 3.45\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Table 4-17 User Flash Timing Parameters

User Modes	Parameter	Name	Min.	Max.	Unit
Access time <sup>2</sup>	WC1	$T_{acc}^3$	-	25	ns
	TC		-	22	ns
	BC		-	21	ns
	LT		-	21	ns
	WC		-	25	ns
Program/Erase to data storage		$T_{nvs}$	5	-	$\mu\text{s}$
Data storage hold time		$T_{nvh}$	5	-	$\mu\text{s}$
Data storage hold time (Overall erase)		$T_{nvh1}$	100	-	$\mu\text{s}$

User Modes	Parameter	Name	Min.	Max.	Unit
	Time from data storage to program setup	$T_{pgs}$	10	-	$\mu s$
	Program hold time	$T_{pgh}$	20	-	ns
	Write time	$T_{prog}$	8	16	$\mu s$
	Write ready time	$T_{wpr}$	>0	-	ns
	Erase hold time	$T_{whd}$	>0	-	ns
	Time from control signal to write/Erase setup	$T_{cps}$	-10	-	ns
	Time from SE to read setup	$T_{as}$	0.1	-	ns
	E pulse high level time	$T_{pws}$	5	-	ns
	Address/data setup time	$T_{ads}$	20	-	ns
	Address/data hold time	$T_{adh}$	20	-	ns
	Data hold-up time	$T_{dh}$	0.5	-	ns
Read address time <sup>3</sup>	WC1	$T_{ah}$	25	-	ns
	TC		22	-	ns
	BC		21	-	ns
	LT		21	-	ns
	WC		25	-	ns
	SE pulse low level time	$T_{nws}$	2	-	ns
	Recovery time	$T_{rcv}$	10	-	$\mu s$
	Data storage time	$T_{hv}$ <sup>4</sup>	-	6	ms
	Erasure time	$T_{erase}$	100	120	ms
	Overall erase time	$T_{me}$	100	120	ms
	Wake-up time from power down to standby mode	$T_{wk\_pd}$	7	-	$\mu s$
	Standby hold time	$T_{sbh}$	100	-	ns
	$V_{CC}$ setup time	$T_{ps}$	0	-	ns
	$V_{CCX}$ hold time	$T_{ph}$	0	-	ns

**Note!**

- [1] The parameter values may change;
- [2] The values are simulation data only.
- [3] After XADR, YADR, XE, and YE are valid,  $T_{acc}$  start time is SE rising edge. DOUT is kept until the next valid read operation;
- [4]  $T_{hv}$  is the time between write and the next erasure. The same address can not be written twice before erasure, so does the same register. This limitation is for safety;
- [5] Both the rising edge time and falling edge time for all waveform is 1ns;
- [6] TX, YADR, XE, and YE hold time need to be  $T_{acc}$  at least, and  $T_{acc}$  start from SE rising edge.



### 4.5.3 Operation Timing Diagrams

Figure 4-1 GW1NR User Flash Read Operation

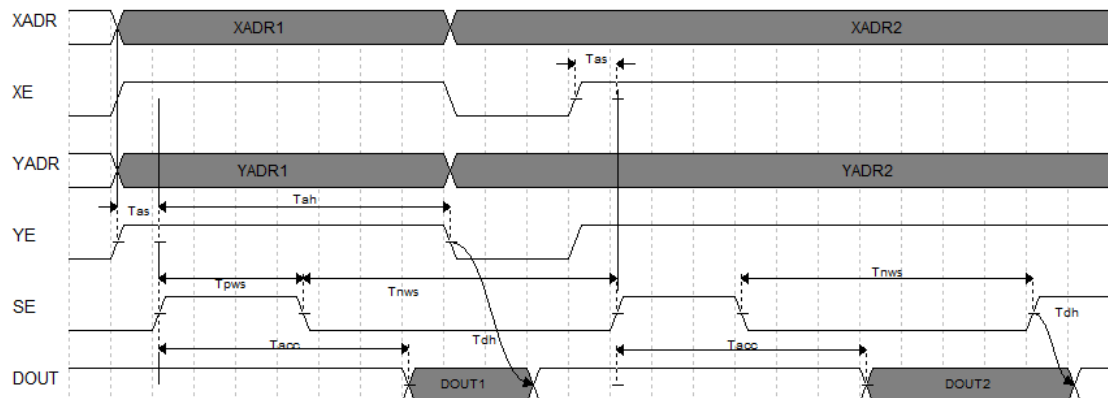


Figure 4-2 GW1NR User Flash Program Operation

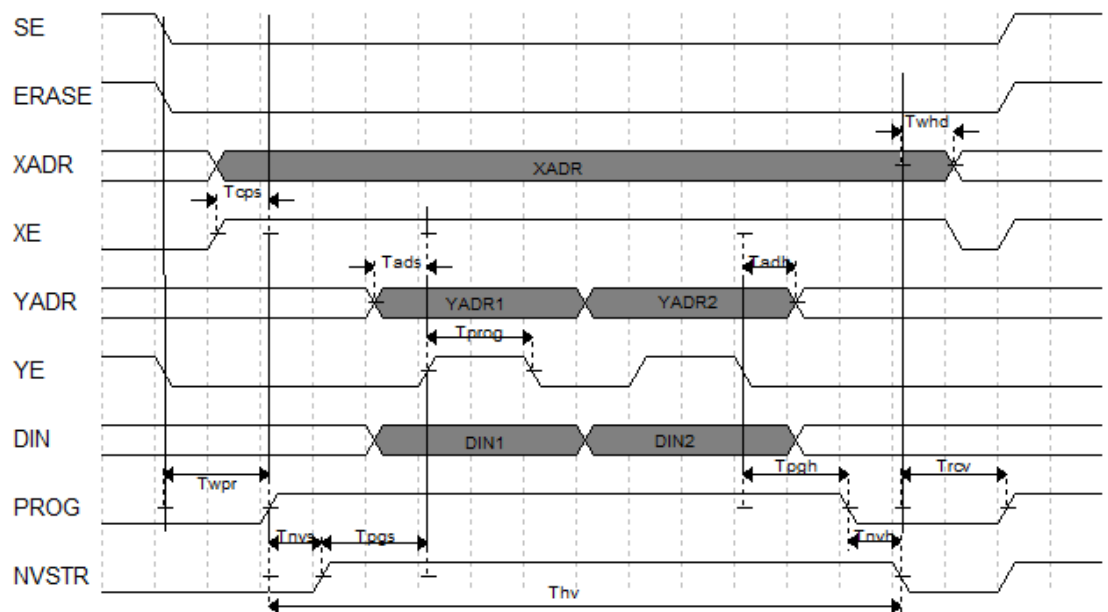
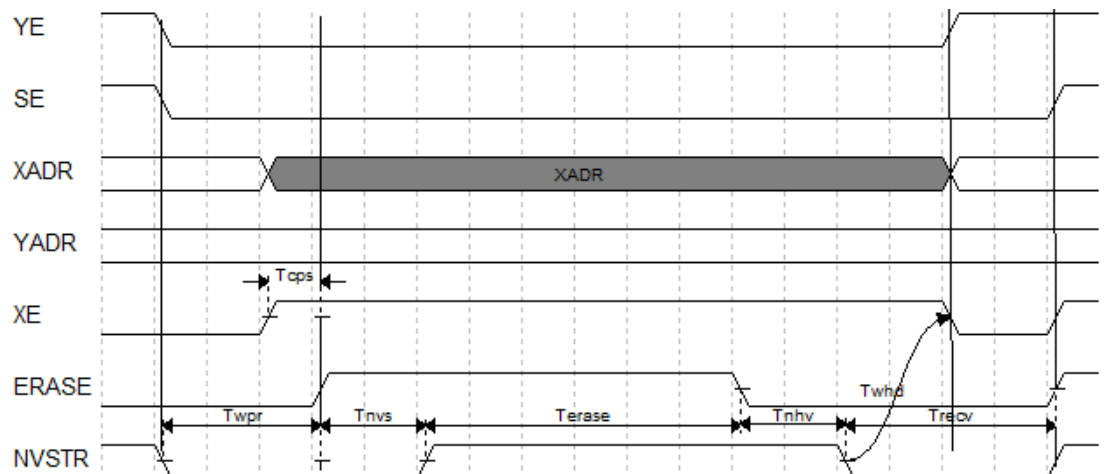


Figure 4-3 GW1NR User Flash Erase Operation



## 4.6 Configuration Interface Timing Specification

The GW1NR series of FPGA products GowinCONFIG support six configuration modes: AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU. For more detailed information, please refer to *GW1NR series FPGA Products Programming and Configuration User Guide*.

### 4.6.1 JTAG Port Timing Specifications

The JTAG mode of the GW1NR series of FPGA products complies with IEEE1532 and IEEE1149.1 boundary scan standards.

JTAG mode downloads the bitstream to SRAM, and the data is lost after power off.

See Figure 4-4 for JTAG timing.

Figure 4-4 JTAG Timing

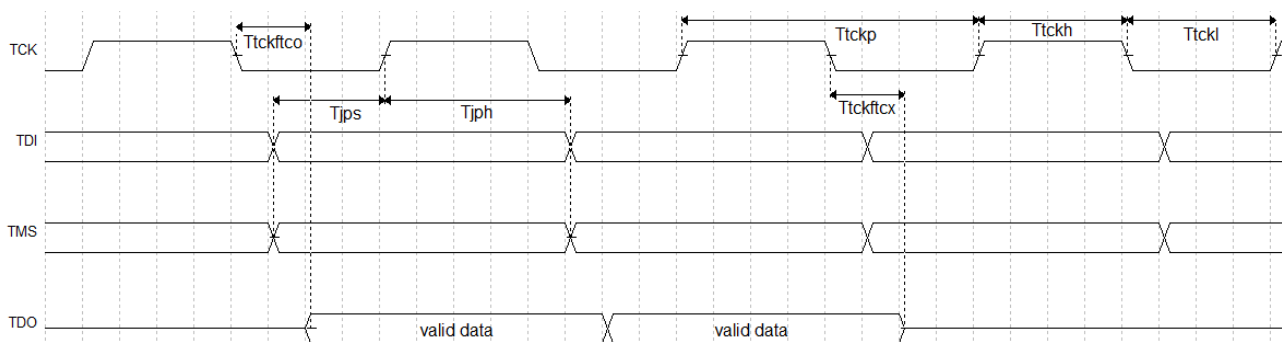


Table 4-18 JTAG Timing Parameters

Name	Description	Min.	Max.
$T_{tckftco}$	Time from TCK falling edge to output		10ns
$T_{tckftcx}$	Time from TCK falling edge to high impedance		10ns
$T_{tckp}$	TCK clock period	40ns	-
$T_{tckh}$	TCK clock high time	20ns	-
$T_{tckl}$	TCK clock low time	20ns	-
$T_{jps}$	JTAG PORT setup time	10ns	
$T_{jph}$	JTAG PORT hold time	8ns	

Other than the power requirements, the following conditions need to be met to use the MSPI configuration mode:

- MSPI port enable

Set RECONFIG\_N as “NON-RECOVERY” for the first programming activity after power-up or the previous programming activity.

- Initiate new program

Power-up again or provide one low pulse for programming pin

RECONFIG\_N.

## 4.6.2 AUTO BOOT Port Timing Specifications

The AUTOBOOT mode offers instant-on feature for the GW1NR series of FPGA products. In this mode, FPGA reads data from the on-chip Flash directly for the program to load after the chip is powered on.

On-chip Flash is configured via the JTAG interface. After the configuration, RECONFIG\_N is triggered by a low level pulse, or auto boot configuration starts after power recycle. Figure 4-5 shows the timing.

Figure 4-5 Power Recycle Timing

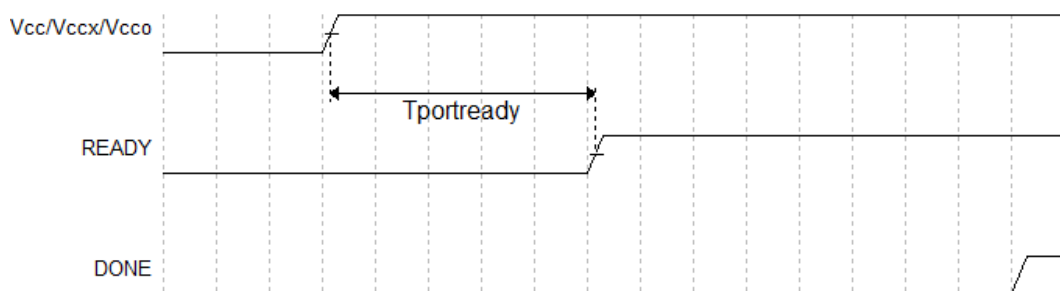


Figure 4-6 RECONFIG\_N Trigger Timing

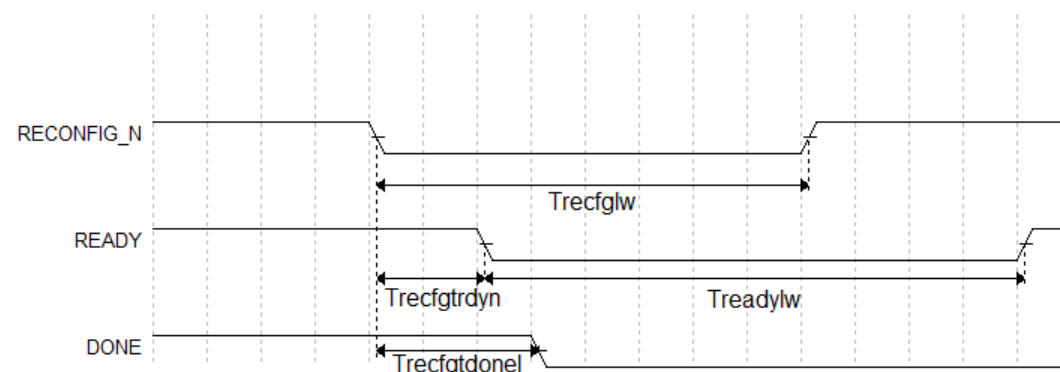


Table 4-19 shows the timing parameters.

Table 4-19 Parameters for Power Recycle and RECONFIG\_N Trigger Timing

Name	Description	Min.	Max.
$T_{portready}^1$	Time from application of $V_{CC}$ , $V_{CCX}$ and $V_{CCO}$ to the rising edge of READY	50 $\mu$ s	200 $\mu$ s
$T_{recfglw}$	RECONFIG_N low pulse width	25ns	
$T_{recfgtrdyn}$	Time from RECONFIG_N falling edge to READY low	-	70ns
$T_{readylw}$	READY low pulse width	TBD	
$T_{recfgtdonel}$	Time from RECONFIG_N falling edge to DONE low	-	80ns

**Note!**

MODE0=0, the device power-up waiting time is 200  $\mu$ s; MODE0=1, the device power-up waiting time is 50  $\mu$ s.

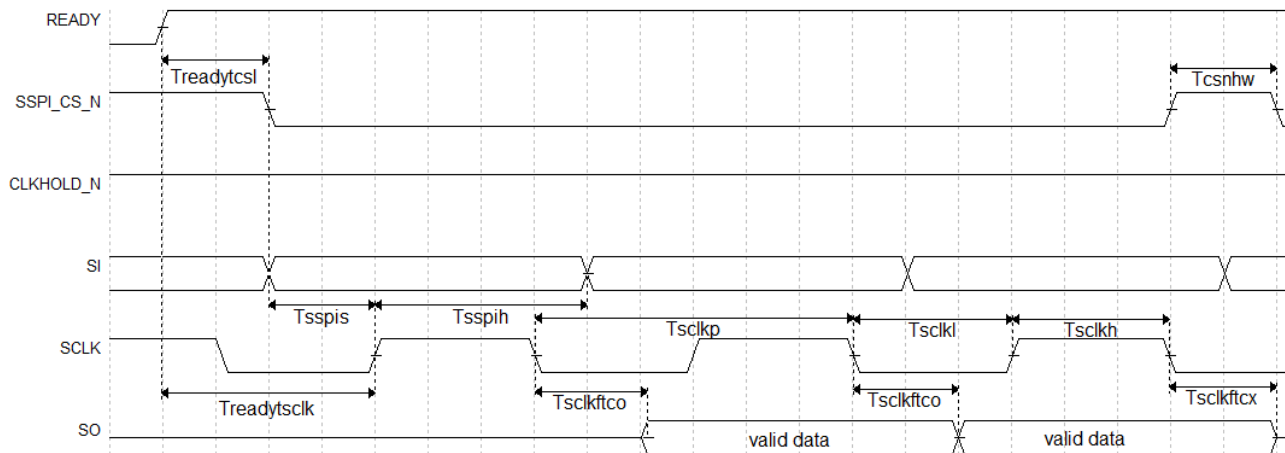
## 4.6.3 SSPI Port Timing Specifications

In the slave SSPI mode, the GW1NR series of FPGA products are

configured by the hardware processor via SPI.

See Figure 4-7 for the SSPI timing diagram.

**Figure 4-7 SSPI Timing Diagram**



See Table 4-20 for the timing parameters.

**Table 4-20 SSPI Timing parameters**

Name	Description	Min.	Max.
$T_{scclkp}$	SCLK clock period	15 ns	-
$T_{scclkh}$	SCLK clock high time	7.5 ns	-
$T_{scclkl}$	SCLK clock low time	7.5 ns	-
$T_{sspis}$	SSPI PORT setup time	2 ns	-
$T_{sspih}$	SSPI PORT hold time	0 ns	-
$T_{scclftco}$	Time from SCLK falling edge to output	-	10 ns
$T_{scclftcx}$	Time from SCLK falling edge to high impedance	-	10 ns
$T_{csnhw}$	CSN high time	25 ns	-
$T_{readytcsi}$	Time from READY rising edge to CSN low		
$T_{readytsclk}$	Time from READY rising edge to first SCLK edge	TBD	-

Other than the power requirements, the following conditions need to be met to use the SSPI configuration mode:

- SSPI port enabled  
Set RECONFIG\_N as “NON-RECOVERY” for the first programming activity after power up or the previous programming activity.
- Initiate new program  
Power recycle or provide one low pulse for programming pin RECONFIG\_N.

## 4.6.4 MSPI Port Timing Specifications

In master MSPI mode, the configuration data is retrieved automatically from the off-chip SPI Flash. The default MCLK frequency of the GW1NR-1 and GW1NR-9 is 2.5 MHz; the default MCLK frequency of GW1NR-4 is

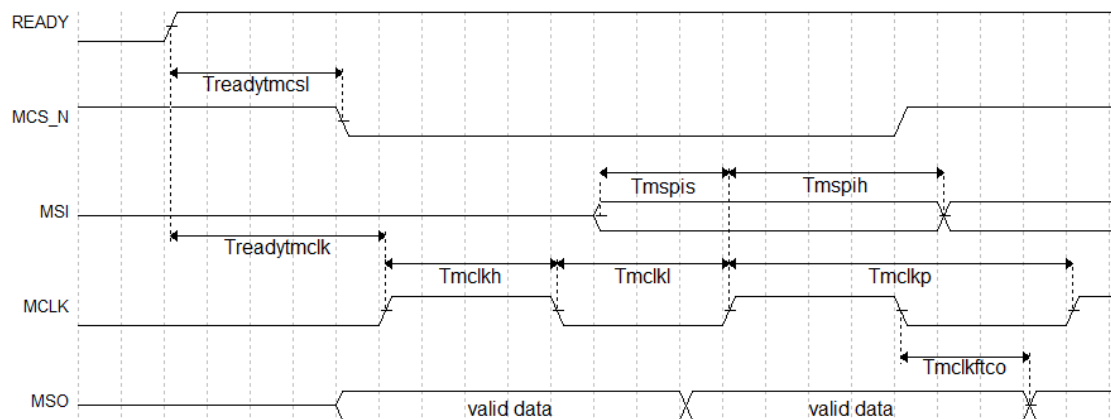
2.1MHz. The MCLK accuracy is +/- 5%.

After MSPI writes the configuration data to the off-chip Flash, power recycle or RECONFIG\_N will trigger device configuration. GW1NR-1 and GW1NR-4 only support one auto MSPI configuration; if this fails, power recycle or RECONFIG\_N will trigger device configuration.

GW1NR-9 supports multiple auto MSPI configurations; if this fails for the first time, FPGA automatically reads external Flash twice. Users can set the address, and the default address is 0.

See Figure 4-8 for the MSPI Timing Diagram.

**Figure 4-8 MSPI Timing Diagram**



See Table 4-21 for the MSPI timing diagram.

**Table 4-21 MSPI Timing Parameters**

Name	Description	Min.	Max.
T <sub>mckp</sub>	MCLK clock period	15 ns	-
T <sub>mclkh</sub>	MCLK clock high time	7.5 ns	-
T <sub>mckl</sub>	MCLK clock low time	7.5 ns	-
T <sub>mcpis</sub>	MSPI PORT setup time	5 ns	-
T <sub>mcpih</sub>	MSPI PORT hold time	1 ns	-
T <sub>mckftco</sub>	Time from MCLK falling edge to output	-	10 ns
T <sub>readytmcs1</sub>	Time from READY rising edge to MCS_N low	100 ns	200 ns
T <sub>readytmclk</sub>	Time from READY rising edge to first MCLK edge	2.8 μs	4.4 μs

## 4.6.5 DUAL BOOT

In DUAL BOOT mode, the configuration data is retrieved automatically from the off chip Flash or from on chip Flash.

GW1NR-1 and GW1NR-9 products try to configure first from the on-chip Flash memory. If there is no data in the on-chip Flash or the configuration fails, the device attempts to configure from the off-chip Flash memory. If that fails too, the device cannot work. In addition, GW1NR-9

devices also support to preferentially start from the external Flash. When the external Flash fails to configure, the device chooses to read the data stored on the built-in Flash for configuration. When the external Flash is empty, the device will not be configured.

GW1NR-9 devices support multiple times configuration no matter starting from the off-chip Flash or from the on-chip Flash: the preferred store path can be started for three times; if those all fails, the other path will be employed for configuration. You can start internal Flash only from address 0, but for external Flash start, you can try three different start addresses.

See *DUAL BOOT Download Solution based on GW1N-4 Device* for the DUAL BOOT Config Mode implementation of GW1NR-4/GW1NR-4B.

## 4.6.6 CPU

In CPU mode, the GW1NR series of FPGA products are configured by hardware processor via DBUS interface. Other than the power requirements, the following conditions need to be met to use the CPU configuration mode:

- CPU port enable  
Set RECONFIG\_N as “NON-RECOVERY” for the first programming activity after power up or the previous programming activity.
- Initiate new program  
Power recycle or provide one low pulse for programming pin RECONFIG\_N.

## 4.6.7 SERIAL

In SERIAL mode, the GW1NR series FPGA products are configured by the hardware processor via serial interface. Other than the power requirements, the following conditions need to be met to use the SERIAL configuration mode:

- SERIAL port enable  
Set RECONFIG\_N as “NON-RECOVERY” for the first programming activity after power-up or the previous programming activity.
- Initiate new program  
Power recycle or provide one low pulse for programming pin RECONFIG\_N.

# 5Ordering Information

## 5.1 Part Name

Figure 5-1 Part Naming-ES (PSRAM Embedded)

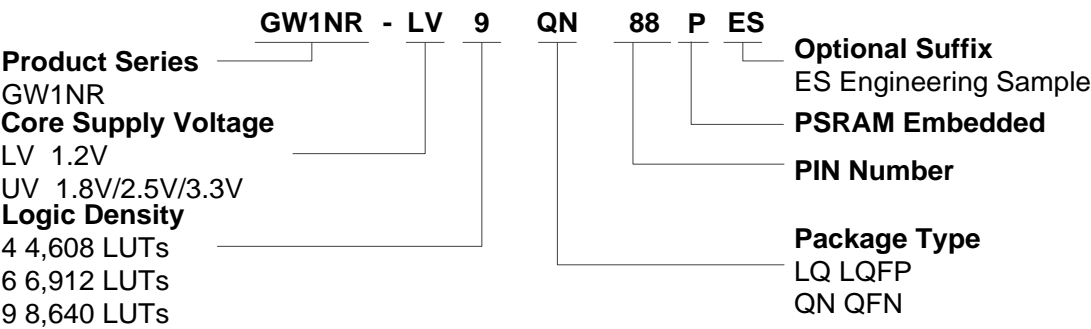


Figure 5-2 Part Naming-Production (SDRAM Embedded)

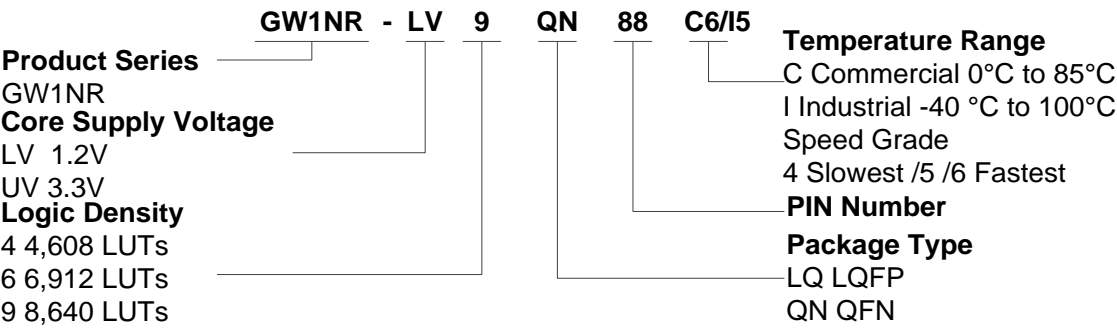
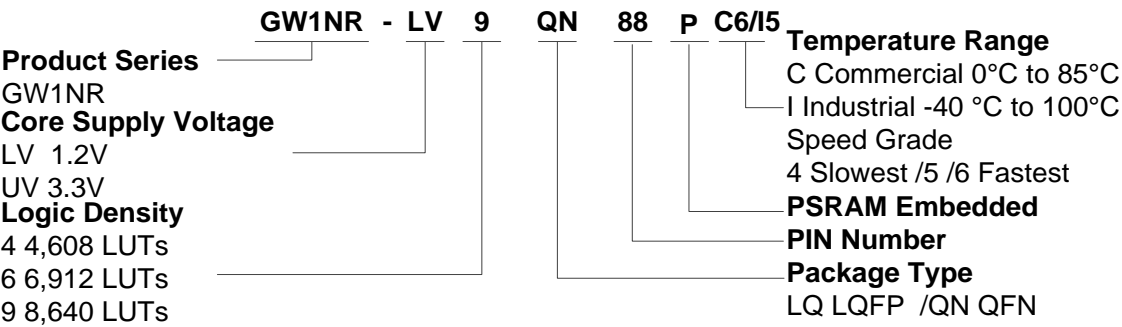


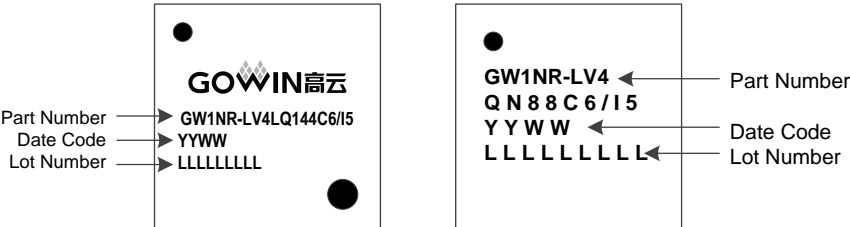
Figure 5-3 Part Naming-Production (PSRAM Embedded)



## 5.2 Package Mark

The device information of GOWINSEMI is marked on the chip surface, as shown in Figure Figure 5-4.

Figure 5-4 Package Mark



**Note!**

The first two lines in the right figure above are the “Part Number”.



