

GW1N series of FPGA Products Package & Pinout User Guide

UG103-1.3E, 01/11/2019

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Revision History

Date	Version	Description			
03/03/2016	1.05E	Initial version.			
05/11/2018	1.17E	Max. user I/O information modified.			
09/13/2018	1.18E	The UG256 package added.			
11/02/2018	1.19E	LVDS paris added in Table 2-1;The quantity of IO in GW1N6/9 QN88 bank modified.			
12/12/2018	1.2E	GW1N-2B,GW1N-4B added;GW1N-1 MG160 and GW1N-1 PG201 removed.			
01/11/2019	1.3E	 IO BANK description updated; View of pin distribution for all packages updated; Quantity of GW1N-6/9 pins updated. 			

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1.1Purpose

1 About This Guide

1.1 Purpose

This manual contains an introduction to the GW1N series of FPGA products together with a definition of the pins, list of pin numbers, distribution of pins, and package diagrams.

1.2 Supported Products

The information in this guide applies to the following products:

GW1N series of FPGA products: GW1N-1, GW1N-2, GW1N-2B, GW1N-4, GW1N-4B, GW1N-6, and GW1N-9.

1.3 Related Documents

The latest user guidelines are available on the Gowin website at www.gowinsemi.com:

- 1. GW1N series of FPGA Products Data Sheet
- 2. GW1N series of FPGA Products Package and Pinout
- 3. GW1N-1 Pinout
- 4. GW1N-2&2B&4&4B Pinout
- 5. GW1N-6&9 Pinout
- 6. Gowin FPGA Products Programming and Configuration User Guide

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1.4 Abbreviations and Terminology

The abbreviations and terminologies that are used in this manual are delineated in Table 1-1.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Full Name	Meaning
FPGA	Field Programmable Gate Array	Field Programmable Gate Array
CS30	WLCSP30	WLCSP30 package
QN32	QFN32	QFN32 package
QN48	QFN48	QFN48 Package
CM64	WLCSP64	WLCSP64 package
CS72	WLCSP72	WLCSP72 package
QN88	QFN88	QFN88
LQ100	LQFP100	LQFP100 package
LQ144	LQFP144	LQFP144 package
MG160	MBGA160	MBGA160 package
LQ176	LQFP176	LQFP176 package
PG256	PBGA256	PBGA256 package
PG256M	PBGA256M	PBGA256M package
UG332	UBGA332	UBGA332 package

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly via the following channels.

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20verview 2.1PB-Free Package

2_{Overview}

The GW1N series of FPGA Products are the first-generation products of GOWINSEMI® (LittleBee®) family. They are available in various forms that offer high I/O compatibility and flexible usage.

2.1 PB-Free Package

The GW1N series of FPGA products are PB free in line with the EU ROHS environmental directives. The substances used in the GW1N series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Package and Max. I/O Information

Table 2-1 Package and Max. I/O Information

Package	Pitch (mm)	Size (mm)	GW1N-1	GW1N-2/ GW1N-2B	GW1N-4/ GW1N-4B	GW1N-6	GW1N-9
CS30	0.4	2.3 x 2.4	24	-	-	-	-
QN32	0.5	5 x 5	26	24 (3)	24 (3)	-	-
QN48	0.4	6 x 6	41	40 (9)	40 (9)	40 (12)	40 (12)
CM64	0.5	4.1 x 4.1				55 (16)	55 (16)
CS72	0.4	3.6 x 3.3	-	57 (19)	57 (19)	-	-
QN88	0.4	10 x 10	-	70 (11)	70 (11)	70 (19)	70 (19)
LQ100	0.5	16 x 16	79	79 (13)	79 (13)	79 (20)	79 (20)
LQ144	0.5	22 x 22	116	119 (22)	119 (22)	120 (28)	120 (28)
MG160	0.5	8 x 8	-	131 (25)	131 (25)	131 (38)	131 (38)
LQ176	0.4	22 x 22	-	-	-	147 (37)	147 (37)
PG256	1.0	17 x 17	-	207 (32)	207 (32)	207 (36)	207 (36)
PG256M	1.0	17 x 17	-	207 (32)	207 (32)	-	-
UG256	0.8	14 x 14	-	-	-	207 (36)	207 (36)
UG332	0.8	17 x 17	-	-	-	273 (43)	273 (43)

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20verview 2.3Dedicated Pins

Note!

In this manual, abbreviations are employed to refer to the package types. See section
 1.4 Abbreviations and Terminology;

- "" indicates that the various device pins are compatible when the package types are the same;
- The GW1N-2 and GW1N-4 pins are fully compatible; GW1N-6 and GW1N-9 pins are fully compatible;
- In terms of the MG160 package, the GW1N-1, GW1N-2, and GW1N-4 pins are compatible; however, the GW1N-1 series has less I/O pins. Please refer to <u>GW1N</u> <u>FPGA Products Pinout and GW1N-2&2B&4&4B Products Pinout for the detailed</u> information;
- The JTAGSEL_N and JTAG pins are exclusive. The four pins of JTAGSEL_N and loaded JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O. The data noted in this Table refer to when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.

2.3 Dedicated Pins

Table 2-2 GW1N Pins

VCC	VCCO0	VCCO1	VCCO2
VCCO3	VCCX	VSS	NC

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2.4 Pin Quantity

2.4.1 Quantity of GW1N-1 Pins

Table 2-3 Quantity of GW1N-1 Pins

Pin Type		GW1N-1				
		CS30	QN32	QN48	LQ100	LQ144
I/O Single end/Differ-e	BANK0	0/0	3/1	9/4	21/10	29/14
	BANK1	10/4	10/4	9/3	18/9	26/13
ntial pair ¹	BANK2	2/1	3/1	12/5	22/9	34/17
·	BANK3	11/5	9/4	9/4	17/8	25/12
Max. User I/C) 2	24	26	41	79	116
Differential Pa	air	10	10	16	36	56
VCC		1	2	2	4	4
VCCO0		0	1	0	2	2
VCCO1	VCCO1		0	1	3	3
VCCO2		0	0	1	2	2
VCCO3		0	1	0	3	3
VCCO0/VCC	O3 ³	1	0	1	0	0
VCCO1/VCC	O2 ³	2	1	0	0	0
VSS		2	1	2	6	10
MODE0		1	1	1	1	1
MODE1		0	0	1	0	1
MODE2		0	0	0	0	0
JTAGSEL_N		0	0	0	1	1
NC		0	0	0	0	3

Note!

- [1]Single end/ Differential I/O quantity include CLK pins, and download pins;
- [2]The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data noted in this table refer to when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;
- [3]Pin multiplexing.

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2.4.2 Quantity of GW1N-2/GW1N-2B Pins

Table 2-4 Quantity of GW1N-2/GW1N-2B Pins

Pin Type		GW1N-2/GW1N-2B								
		QN32	QN48	CS72	QN88	LQ100	LQ144	MG160	PG256	PG256M
I/O	BANK0	3/1/0	10/5/ 0	9/4/0	18/6/ 0	21/10/0	31/14/0	32/16/0	51/24/0	51/25/0
Single end/Diff-	BANK1	9/4/1	9/4/2	5/4/2011	6/2/2 015	8/1/201 6	12/5/20 24	26/13/6	42/21/8	42/21/8
erential pair ¹	BANK2	4/2/2	12/6/ 6	11/11/20 22	9/7/2 023	12/10/2 026	38/18/1 2	43/20/1 3	70/36/1 6	70/35/16
рап	BANK3	7/2/0	8/3/1	6/4/201 4	4/2/2 012	7/2/201 5	11/5/202 4	12/6/20 27	41/20/8	41/20/8
Max. Use	r I/O ²	24	40	57	70	79	119	131	207	207
Differential Pair		9	18	26	25	37	55	61	101	101
LVDS		3	9	19	11	13	22	25	32	32
VCC		2	2	3	4	4	4	4	8	8
VCCO0		1	0	1	1	2	2	2	4	4
VCCO1		1	0	1	1	2	2	2	3	3
VCCO2		1	0	1	2	2	2	2	4	4
VCCO3		1	0	1	1	2	2	2	3	3
VCCO0/V	CCO3 ³	0	1	0	0	0	0	0	0	0
VCCO1/V	CCO2 ³	0	1	0	0	0	0	0	0	0
VCCX		1	1	1	2	2	2	4	2	2
VSS		1	2	6	6	6	10	12	24	24
MODE0		0	0	1	1	1	1	1	1	1
MODE1		1	1	0	1	0	1	1	1	1
MODE2		0	0	0	0	0	0	1	1	1
JTAGSEL	_N	0	1	1	1	1	1	1	1	1

Note!

- [1]Single end/ Differential I/O quantity include CLK pins, and download pins;
- [2]The max. user I/O excludes dedicated MODE pins; The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The Max. I/O noted in this table refer to when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;
- [3]Pin multiplexing.

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2.4.3 Quantity of GW1N-4/GW1N-4B Pins

Table 2-5 Quantity of GW1N-4/GW1N-4B Pins

Pin Type		GW1N-4/GW1N-4B								
Pin Typ	e	QN32	QN48	CS72	QN88	LQ100	LQ144	MG160	PG256	PG256M
I/O	BANK0	3/1/0	10/5/ 0	9/4/0	18/6/ 0	21/10/0	31/14/0	32/16/0	49/24/ 0	51/25/0
Single end/	BANK1	9/4/1	9/4/2	5/4/2 011	6/2/2 015	8/1/201 6	12/5/20 24	26/13/6	42/21/ 8	42/21/8
Differ- ential	BANK2	4/2/2	12/6/ 6	11/11/ 2022	9/7/2 023	12/10/2 026	38/18/1 2	43/20/1 3	72/36/ 16	70/35/16
pair ¹	BANK3	7/2/0	8/3/1	6/4/2 014	4/2/2 012	7/2/201 5	11/5/202 4	12/6/20 27	41/20/ 8	41/20/8
Max. U	ser I/O ²	24	40	57	70	79	119	131	207	207
Differer	ntial Pair	9	18	26	25	37	55	62	101	101
LVDS		3	9	19	11	13	22	25	32	32
VCC		2	2	3	4	4	4	4	8	8
VCCO)	1	0	1	1	2	2	2	4	4
VCCO1		1	0	1	1	2	2	2	3	3
VCCO2	2	1	0	1	2	2	2	2	4	4
VCCO		1	0	1	1	2	2	2	3	3
3)/VCCO3	0	1	0	0	0	0	0	0	0
VCCO1	/VCCO2	0	1	0	0	0	0	0	0	0
VCCX	VCCX		1	1	2	2	2	4	2	2
VSS		1	2	6	6	6	10	12	24	24
MODE0		0	0	1	1	1	1	1	1	1
MODE1		1	1	0	1	0	1	1	1	1
MODE	2	0	0	0	0	0	0	1	1	1
JTAGS	EL_N	0	1	1	1	1	1	1	1	1

Note!

- [1]Single end/ Differential I/O quantity include CLK pins, and download pins;
- [2]The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data noted in this table refer to when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.
- [3]Pin multiplexing.

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2.4.4 Quantity of GW1N-6 Pins

Table 2-6 Quantity of GW1N-6 Pins

D'. T		GW1N-	GW1N-6								
Pin Type		QN48	CM64	QN88	LQ100	LQ144	MG160	LQ176	PG256	UG256	UG332
	BANK0	4/2/0	12/6/0	0/0/0	9/4/0	18/9/0	20/10/0	17/8/0	36/16/0	46/23/0	46/23/0
I/O Single	BANK1	13/6/3	12/6/4	25/6/4	24/12/4	32/16/8	34/17/9	36/17/ 7	56/28/1 0	58/29/12	68/34/11
end/Dif- ferential	BANK2	12/6/6	18/9/9	23/9/11	26/13/1 2	40/19/1 4	43/21/1 9	54/26/ 20	70/35/1 6	52/26/12	90/45/20
pair ¹	BANK3	11/4/3	13/5/3	22/4/4	20/9//4	30/13/6	34/16/1 0	40/18/ 10	49/23/1 0	51/25/12	69/34/12
Max. Use	er I/O ²	40	55	70	79	120	131	147	207	207	273
Differentia	al Pair	18	26	30	38	57	64	69	102	103	136
LVDS		12	16	19	20	28	38	37	36	36	43
VCC		2	2	4	4	4	4	4	8	8	8
VCCX		1	2	2	2	2	4	4	2	1	2
VCCO0		0	0	1	2	2	2	3	4	4	3
VCCO1		0	0	1	2	2	2	3	3	4	4
VCCO2		0	0	2	2	2	2	3	4	4	5
VCCO3		0	0	1	2	2	2	3	3	3	3
VCCO0/\	/CCO3 ³	1	0	0	0	0	0	0	0	0	0
VCCO1/\	/CCO2 ³	1	0	0	0	0	0	0	0	0	0
VCCO0/\	/CCO2 ³	0	1	0	0	0	0	0	0	0	0
VCCO1/\	/CCO3 ³	0	1	0	0	0	0	0	0	0	0
VSS	VSS		2	6	6	9	12	8	24	24	27
MODE0		0	0	1	1	1	1	1	1	0	1
MODE1		0	0	1	0	1	1	1	1	0	1
MODE2		0	0	0	0	0	1	1	1	0	1
MODE1/MODE2 ³		1	0	0	0	0	0	0	0	0	0
JTAGSEL	_N	1	1	1	1	1	1	1	1	1	1
NC		0	0	0	0	0	0	0	0	0	6

Note!

- [1]Single end/ Differential I/O quantity include CLK pins, and download pins;
- [2]The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data noted in this table refer to when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.

• [3]Pin multiplexing.

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2.4.5 Quantity of GW1N-9 Pins

Table 2-7 Quantity of GW1N-9 Pins

Pin Type		GW1N-	9								
Pin Typ	е	QN48	CM64	QN88	LQ100	LQ144	MG160	LQ176	PG256	UG256	UG332
I/O	BANK0	4/2/0	12/6/0	0/0/0	9/4/0	18/9/0	20/10/0	17/8/0	36/16/0	46/23/0	46/23/0
Single end/	BANK1	13/6/3	12/6/4	25/6/4	24/12/ 4	32/16/ 8	34/17/9	36/17/7	56/28/10	58/29/12	68/34/1 1
Differ- ential	BANK2	12/6/6	18/9/9	23/9/11	26/13/ 12	40/19/ 14	43/21/1 9	54/26/2 0	70/35/16	52/26/12	90/45/2 0
pair ¹	BANK3	11/4/3	13/5/3	22/4/4	20/9/4	30/13/ 6	34/16/1 0	40/18/1 0	49/23/10	51/25/12	69/34/1 2
Max. Us	ser I/O ²	40	55	70	79	120	131	147	207	207	273
Differen	itial Pair	18	26	30	38	57	64	69	102	103	136
LVDS		12	16	19	20	28	38	37	36	36	43
VCC		2	2	4	4	4	4	4	8	8	8
VCCX		1	2	2	2	2	4	4	2	1	2
VCC00		0	0	1	2	2	2	3	4	4	3
VCCO1		0	0	1	2	2	2	3	3	4	4
VCCO2		0	0	2	2	2	2	3	4	4	5
VCCO3		0	0	1	2	2	2	3	3	3	3
VCC00	/VCCO3 ³	1	0	0	0	0	0	0	0	0	0
VCCO1	/VCCO2 ³	1	0	0	0	0	0	0	0	0	0
VCC00	/VCCO2 ³	0	1	0	0	0	0	0	0	0	0
VCCO1	/VCCO3 ³	0	1	0	0	0	0	0	0	0	0
VSS		2	2	6	6	9	12	8	24	24	27
MODEO)	0	0	1	1	1	1	1	1	0	1
MODE1		0	0	1	0	1	1	1	1	0	1
MODE2	2	0	0	0	0	0	1	1	1	0	1
MODE1/MODE2 ³		1	0	0	0	0	0	0	0	0	0
JTAGSE	EL_N	1	1	1	1	1	1	1	1	1	1
NC		0	0	0	0	0	0	0	0	0	6

Note!

- [1]Single end/ Differential I/O quantity include CLK pins, and download pins;
- [2]The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data noted in this table refer to when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.

• [3]Pin multiplexing.

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20verview 2.5Pin Definitions

2.5 Pin Definitions

The location of the pins in the GW1N series of FPGA products varies according to the different packages.

Table 2-8 provides a detailed overview of user I/O, multi-function pins, dedicated pins, and other pins.

Table 2-8 Definition of the Pins in the GW1N series of FPGA products

Pin Name	I/O	Description
User I/O Pins		
IO[End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left) R(right) B(bottom), and T(top) [Row/Column Number] indicates the pin Row/Column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the Row number of the corresponding CFU. [A/B] indicates differential signal pair information.
Multi-Function Pins		
IO[End][Row/Column Nu	umber][A/B]/MMM	/MMM represents one or more of the other functions in addition to being general purpose user I/O. When not used for the special functions, these pins can be user I/O.
RECONFIG_N	I, internal weak pull-up	Start new GowinCONFIG mode when low pulse
READY	I/O	When high, device can be programmed and configured When low, device cannot be programmed and configured
DONE	I/O	High indicates successful completion of programming and configuration Low indicates incomplete or failed programming and configuration
FASTRD_N /D3	I/O	In MSPI mode, FASTRD_N is used as Flash access speed port. Low indicates high-speed Flash access mode; high indicates regular Flash access mode. Data port D3 in CPU mode
MCLK /D4	I/O	Clock output MCLK in MSPI mode Default frequency: GW1N-1/6/9: 2.5Mhz, +/-5% GW1N-2/4: 2.1Mhz, +/-5% Data port D4 in CPU mode
MCS_N /D5	I/O	Enable signal MCS_N in MSPI mode, active-low Data port D5 in CPU mode
MI /D7	I/O	MISO in MSPI mode: Master data input/Slave data output Data port D7 in CPU mode
MO /D6	I/O	MISO in MSPI mode: Master data output/Slave data input Data port D6 in CPU mode
SSPI_CS_N/D0	I/O	Enable signal SSPI_CS_N in SSPI mod, active-low, Internal Weak Pull Up

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20verview 2.5Pin Definitions

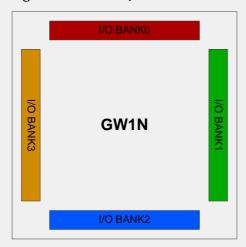
Pin Name	I/O	Description
		Data port D0 in CPU mode
SO /D1	I/O	MISO in MSPI mode: Master data input/Slave data output Data port D1 in CPU mode
SI /D2	I/O	MISO in MSPI mode: Master data output/Slave data input Data port D2 in CPU mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode, which needs to be connected with 4.7 K drop-down resistance on PCB
TDI	I, internal weak pull-up	Serial data input in JTAG mode
TDO	0	Serial data output in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Select signal in JTAG mode, active-low
SCLK	I	Clock input in SSPI, SERIAL, and CPU mode
DIN	I, internal weak pull-up	Input data in SERIAL mode
DOUT	0	Output data in SERIAL mode
CLKHOLD_N	I, internal weak pull-up	High, SCLK will be connected internally in SSPI mode or CPU mode Low, SCLK will be disconnected from SSPI mode or CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode
GCLKT_[x]	1	Pins in global clock input, T(True), [x]: global clock No.
GCLKC_[x]	I	Pins in global clock input, C(Comp), [x]: global clock No.
LPLL_T_fb/RPLL_T_fb	I	L/R PLL feedback the input pin, T(True)
LPLL_C_fb/RPLL_C_fb	I	L/R PLL feedback the input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	L/R PLL clock input pin, T(True)
LPLL_C_in/RPLL_C_in	I	L/R PLL clock input pin, C(Comp)
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin.
Other Pins		
NC	NA	Reserved.
VSS	NA	Ground pins
VCC	NA	Power supply pins in the internal core logic.
VCCO#	NA	Power supply pins in I/O voltage of I/O BANK#.
VCCX	NA	Power supply pins in auxiliary voltage.

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2.6 Introduction to the I/O BANK

There are four I/O Banks in the GW1N series of FPGA products, as shown in Figure 2-1.

Figure 2-1 GW1N I/O Bank Distribution



This manual provides an overview of the distribution view of the pins in the GW1N series of FPGA products. Four IO Banks in GW1N series FPGA products are marked with four different colors.

User I/O, power, and ground are marked with different symbols and colors. The various symbols and colors used for the various pins are defined as follows:

- "D" denotes I/Os in BANK0. The filling color changes with the BANK.
- "D" denotes I/Os in BANK1. The filling color changes with the BANK.
- "D" denotes I/Os in BANK2. The filling color changes with the BANK.
- "D" denotes I/Os in BANK3. The filling color changes with the BANK.
- "\(\brace \)" denotes VCC, VCCX, and VCCO. The filling color does not change.
- "=" denotes VCC. The filling color does not change.
- "Description of the second of the

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3 View of Pin Distribution

3.1 View of GW1N-1 Pins Distribution

3.1.1 View of CS30 Pins Distribution

Figure 3-1 View of GW1N-1 CS30 Pin Distribution (Top View)

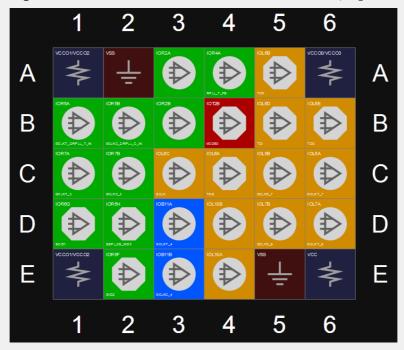


Table 3-1 Other Pins in GW1N-1 CS30

VCC	E6
VCCO0/VCCO3	A6
VCCO1/VCCO2	E1,A1
VSS	A2,E5

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3.1.2 View of QN32Pins Distribution

Figure 3-2 View of GW1N-1 QN32 Pins Distribution (Top View)

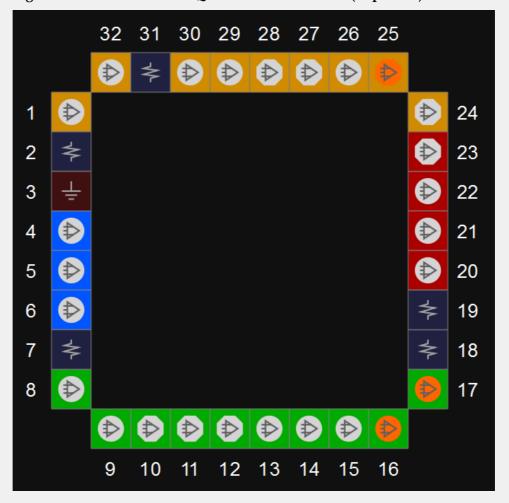


Table 3-2 Other pins in GW1N-1 QN32

VCC	2, 18
VCCO0	19
VCCO1/VCCO2	7
VCCO3	31
VSS	3

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3.1.3 View of QN48 Pins Distribution

Figure 3-3 View of GW1N-1 QN48 Pins Distribution (Top View)

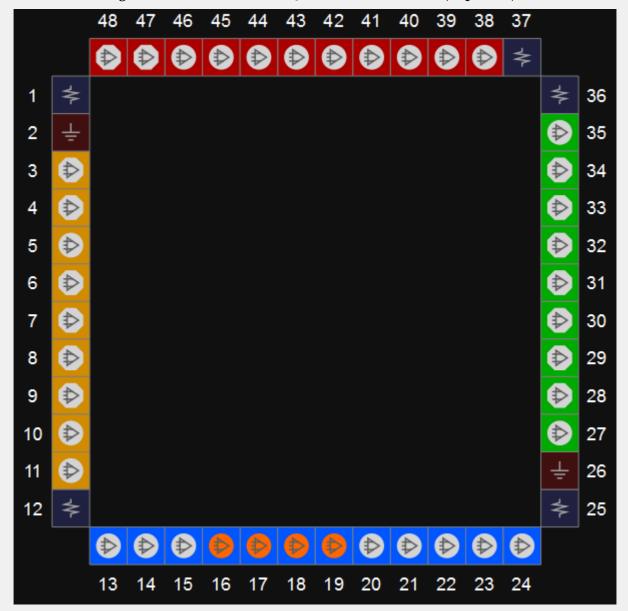


Table 3-3 Other pins in GW1N-1 QN48

VCC	12, 37
VCCO0/VCCO3	1
VCCO1	36
VCCO2	25
VSS	2, 26

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3.1.4 View of LQ100Pins Distribution

Figure 3-4 View of GW1N-1 LQ100 Pins Distribution (Top View)

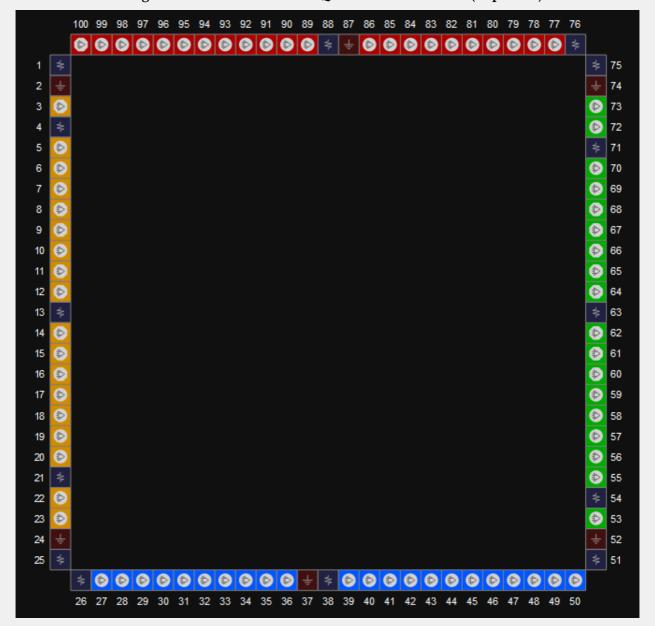


Table 3-4 Other pins in GW1N-6 LQ100

VCC	1, 25, 51, 75
VCCO0	76, 88
VCCO1	54, 63, 71
VCCO2	26, 38
VCCO3	4, 13, 21
VSS	2, 24, 37, 52, 74, 87

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3.1.5 View of LQ144Pins Distribution

Figure 3-5 View of GW1N-1 LQ144 Pins Distribution (Top View)

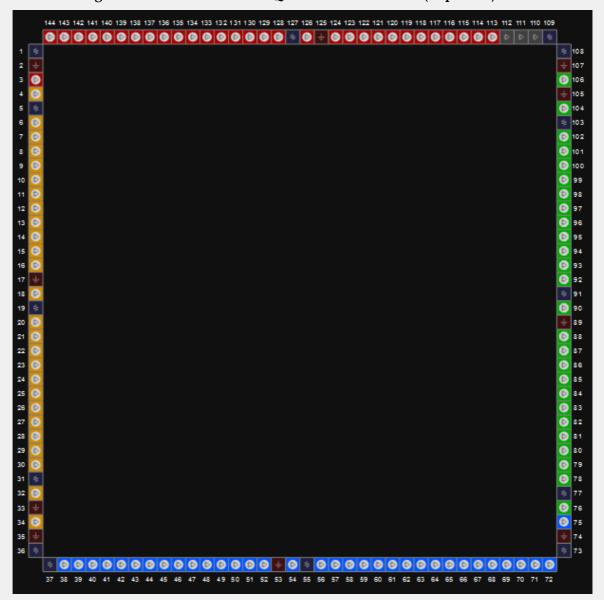


Table 3-5 Other pins in GW1N-6 LQ100

VCC	1, 36, 73, 108
VCC00	109, 127
VCCO1	77, 91, 103
VCCO2	37, 55
VCCO3	5, 19, 31
VSS	2, 17, 33, 35, 53, 74, 89, 105, 107, 125
NC	110, 111, 112

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3.2 View of GW1N-2/GW1N-2B Pins Distribution

3.2.1 View of QN32 Pins Distribution

Figure 3-6 View of GW1N-2/GW1N-2B QN32 Pins Distribution (Top View)

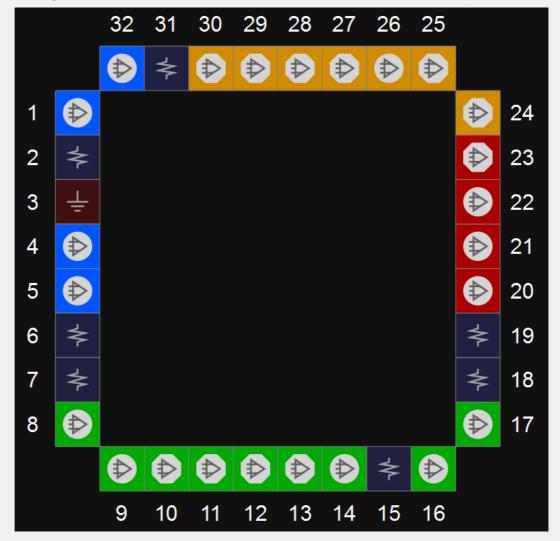


Table 3-6 Other pins in GW1N-2/GW1N-2B LQ100

VCC	2, 18
VCCO0	19
VCCO1	7
VCCO2	6
VCCO3	31
VCCX	15
VSS	3

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3.2.2 View of QN48 Pins Distribution

Figure 3-7 View of GW1N-2/GW1N-2B QN48 Pins Distribution (Top View)

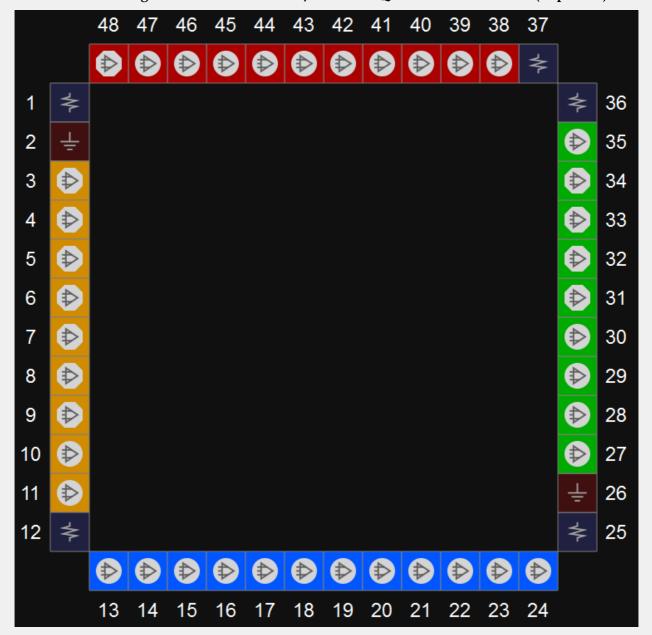


Table 3-7 Other pins in GW1N-2/GW1N-2B QN48

VCC	12, 37
VCCO0/VCCO3	1
VCCO1/VCCO2	25
VCCX	36
VSS	2, 26

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3.2.3 View of CS72 Pins Distribution

Figure 3-8 View of GW1N-2/GW1N-2B CS72 Pins Distribution (Top View)

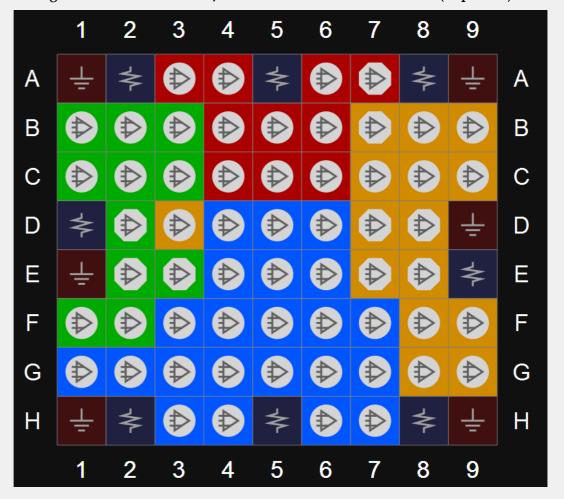


Table 3-8 Other pins in GW1N-2/GW1N-2B CS72

VCC	A2, A8, H8
VCCO0	A5
VCCO1	D1
VCCO2	H5
VCCO3	E9
VCCX	H2
VSS	A1, A9, D9, E1, H1, H9

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3.2.4 View of QN88 Pins Distribution

Figure 3-9 View of GW1N-2/GW1N-2B QN88 Pins Distribution (Top View)

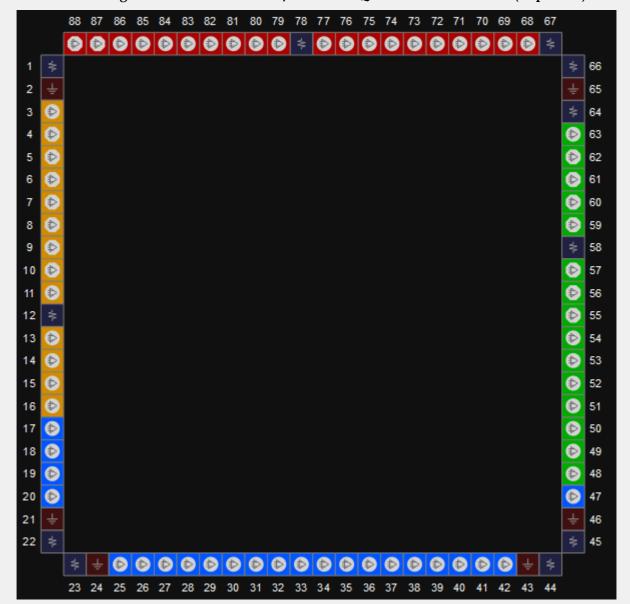


Table 3-9 Other pins in GW1N-2/GW1N-2B QN48

VCC	1, 22, 45, 66
VCC00	67
VCCO1	58
VCCO2	23, 44
VCCO3	12
VCCX	64, 78
VSS	2, 21, 24, 43, 46, 65

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3.2.5 View of LQ100 Pins Distribution

Figure 3-10 View of GW1N-2/GW1N-2B LQ100 Pins Distribution (Top View)

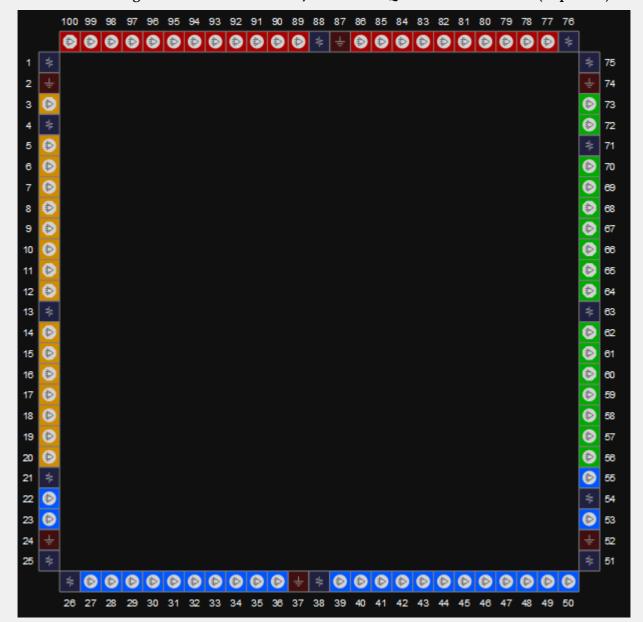


Table 3-10 Other pins in GW1N-2/GW1N-2B LQ100

VCC	1, 25, 51, 75
VCCO0	76, 88
VCCO1	54, 63
VCCO2	26, 38
VCCO3	4, 13
VCCX	21, 71
VSS	2, 24, 37, 52, 74, 87

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3.2.6 View of LQ144 Pins Distribution

Figure 3-11 View of GW1N-2/GW1N-2B LQ144 Pins Distribution (Top View)



Table 3-11 Other pins in GW1N-2/GW1N-2B LQ144

VCC	1, 36, 73, 108
VCC00	109, 127
VCCO1	77, 91
VCCO2	37, 55
VCCO3	5, 19
VCCX	31, 103
VSS	2, 17, 33,35, 53, 74, 89, 105,107, 125

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3.2.7 View of MG160 Pins Distribution

Figure 3-12 View of GW1N-2/GW1N-2B MG160 Pins Distribution (Top View)

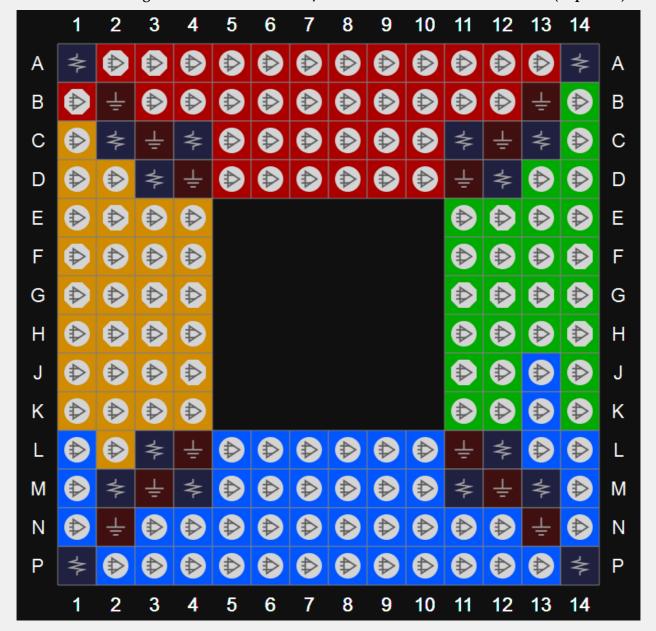


Table 3-12 Other pins in GW1N-2/GW1N-2B MG160

VCC	A1, A14, P1, P14
VCCO0	C4, C11
VCCO1	D12, L12
VCCO2	M4, M11
VCCO3	D3, L3
VCCX	C2, C13, M2, M13
VSS	B2, B13, C3, C12, D4, D11, L4, L11, M3, M12, N2, N13

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3.2.8 View of PG256 Pins Distribution

Figure 3-13 View of GW1N-2/GW1N-2B PG256 Pins Distribution (Top View)

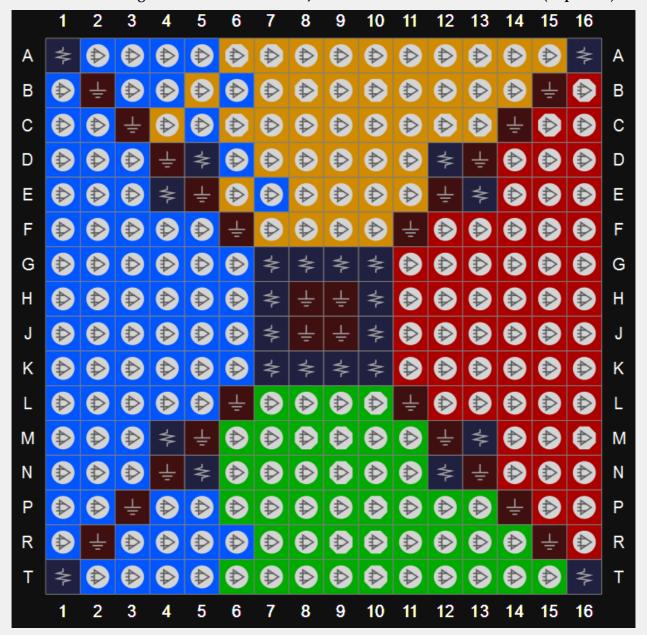


Table 3-13 Other pins in GW1N-2/GW1N-2B PG256

VCC	A1, A16, G7, G10, K7, K10, T1, T16
VCC00	E13, J10, M13, H10
VCCO1	K8, N5, N12
VCCO2	E4, H7, M4, J7
VCCO3	D12, D5, G9
VCCX	G8, K9
VSS	B2, B15, C3, C14, D4, D13, E5, E12, F6, F11, H8, H9,
	J8, J9, L6, L11, M5, M12, N4, N13, P3, P14, R2, R15

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3.2.9 View of PG256M Pins Distribution

Figure 3-14 View of GW1N-2/GW1N-2B PG256M Pins Distribution (Top View)



Table 3-14 Other pins in GW1N-2/GW1N-2B PG256M

VCC	F10, G11, H10, H8, J7, J9, K6, L7
VCC00	A14, A3, F8, F9
VCCO1	C16, J11, P16
VCCO2	L8, L9, T3, T14
VCCO3	C1, H6, P1
VCCX	H11, J6
VSS	A1, A16, B15, B2, F7, G10, G6, G7, G8, G9, K10, K11,
	K7, K8, K9, L10, R2, R15, T1, H9, H7, J10, J8

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3.3 View of GW1N-4/GW1N-4B Pins Distribution

3.3.1 View of QN32 Pins Distribution

Figure 3-15 View of GW1N-4/GW1N-4B QN32 Pins Distribution (Top View)

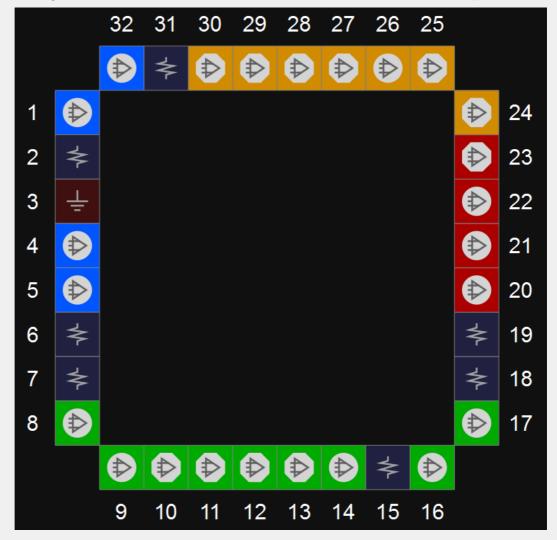


Table 3-15 Other pins in GW1N-4/GW1N-4B QN32

VCC	2, 18
VCCO0	19
VCCO1	7
VCCO2	6
VCCO3	31
VCCX	15
VSS	3

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3.3.2 View of QN48 Pins Distribution

Figure 3-16 View of GW1N-4/GW1N-4B QN48 Pins Distribution (Top View)

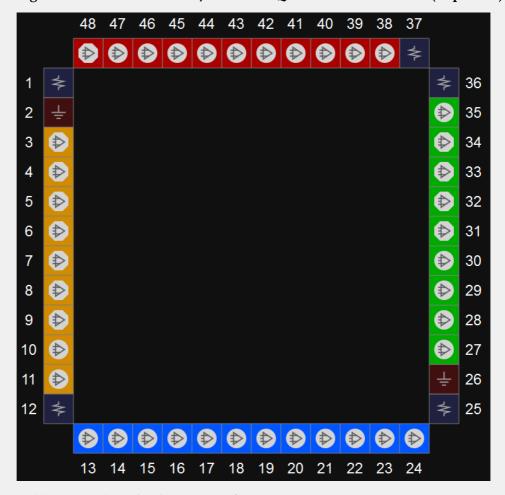


Table 3-16 Other pins in GW1N-4/GW1N-4B QN48

VCC	12, 37
VCCO0/VCCO3	1
VCCO1/VCCO2	25
VCCX	36
VSS	2, 26

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3.3.3 View of CS72 Pins Distribution

Figure 3-17 View of GW1N-4/GW1N-4B CS72 Pins Distribution (Top View)

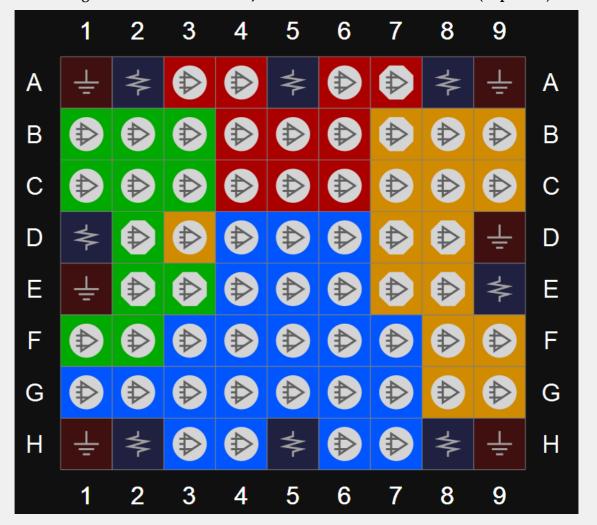


Table 3-17 Other pins in GW1N-4/GW1N-4B CS72

VCC	A2, A8, H8
VCCO0	A5
VCCO1	D1
VCCO2	H5
VCCO3	E9
VCCX	H2
VSS	A1, A9, D9, E1, H1, H9

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3.3.4 View of QN88 Pins Distribution

Figure 3-18 View of GW1N-4/GW1N-4B QN88 Pins Distribution (Top View)

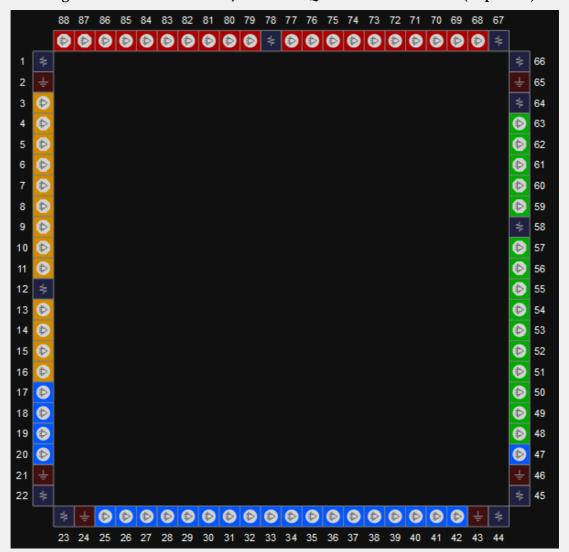


Table 3-18 Other pins in GW1N-4/GW1N-4B QN48

VCC	1, 22, 45, 66
VCC00	67
VCCO1	58
VCCO2	23, 44
VCCO3	12
VCCX	64, 78
VSS	2, 21, 24, 43, 46, 65

UG103-1.3E 30(69)

3.3.5 View of LQ100 Pins Distribution

Figure 3-19 View of GW1N-4/GW1N-4B LQ100 Pins Distribution (Top View)

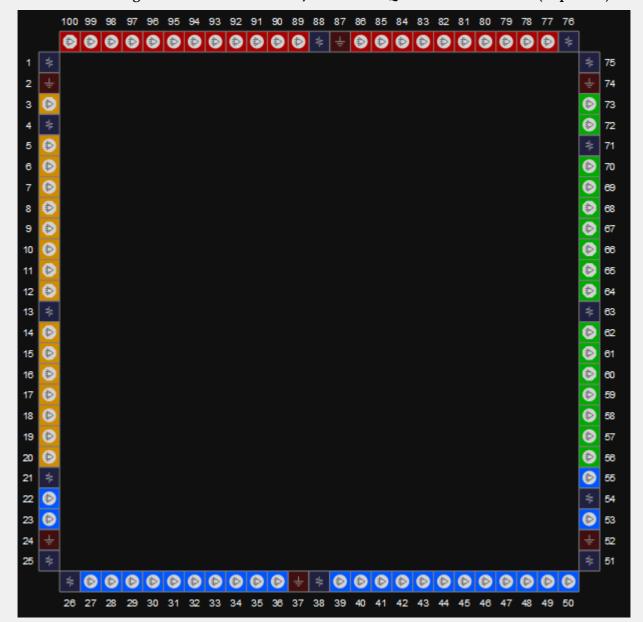


Table 3-19 Other pins in GW1N-4/GW1N-4B LQ100

VCC	1, 25, 51, 75
VCCO0	76, 88
VCCO1	54, 63
VCCO2	26, 38
VCCO3	4, 13
VCCX	21, 71
VSS	2, 24, 37, 52, 74, 87

UG103-1.3E 31(69)

3.3.6 View of LQ144 Pins Distribution

Figure 3-20 View of GW1N-4/GW1N-4B LQ144 Pins Distribution (Top View)



Table 3-20 Other pins in GW1N-4/GW1N-4B LQ100

VCC	1, 36, 73, 108
VCC00	109, 127
VCCO1	77, 91
VCCO2	37, 55
VCCO3	5, 19
VCCX	31, 103
VSS	2, 17, 33,35, 53, 74, 89, 105,107, 125

UG103-1.3E 32(69)

3.3.7 View of MG160 Pins Distribution

Figure 3-21 View of GW1N-4/GW1N-4B MG160 Pins Distribution (Top View)

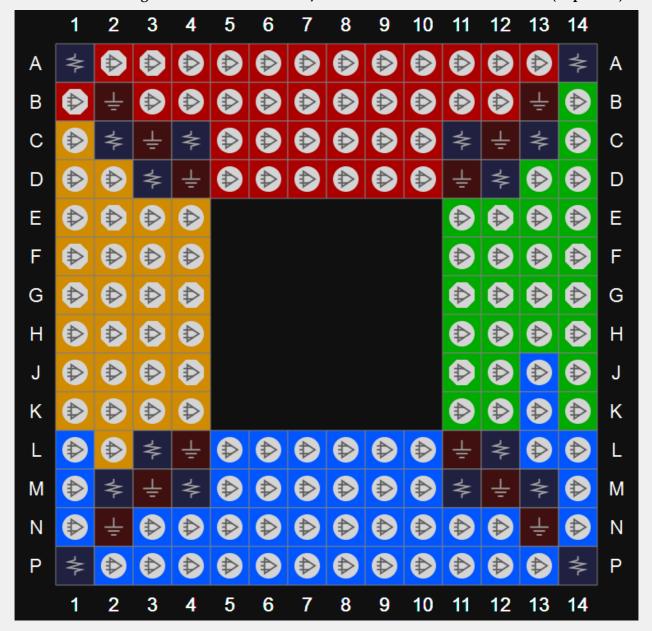


Table 3-21 Other pins in GW1N-4//GW1N-4B MG160

VCC	A1, A14, P1, P14
VCCO0	C4, C11
VCCO1	D12, L12
VCCO2	M4, M11
VCCO3	D3, L3
VCCX	C2, C13, M2, M13
VSS	B2, B13, C3, C12, D4, D11, L4, L11, M3, M12, N2, N13

UG103-1.3E 33(69)

3.3.8 View of PG256 Pins Distribution

Figure 3-22 View of GW1N-4/GW1N-4B PG256 Pins Distribution (Top View)

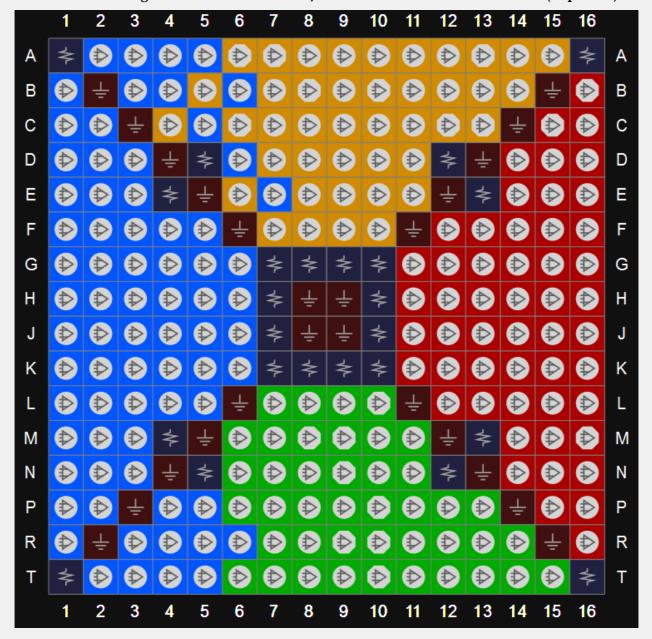


Table 3-22 Other pins for GW1N-4/GW1N-4B PG256

VCC	A1, A16, G7, G10, K7, K10, T1, T16
VCCO0	E13, J10, M13, H10
VCCO1	K8, N5, N12
VCCO2	E4, H7, M4, J7
VCCO3	D12, D5, G9
VCCX	G8, K9
VSS	B2, B15, C3, C14, D4, D13, E5, E12, F6, F11, H8, H9,
	J8, J9, L6, L11, M5, M12, N4, N13, P3, P14, R2, R15

UG103-1.3E 34(69)

3.3.9 View of PG256M Pins Distribution

Figure 3-23 View of GW1N-4/GW1N-4B PG256M Pins Distribution (Top View)



Table 3-23 Other pins in GW1N-4/GW1N-4B PG256M

VCC	F10, G11, H10, H8, J7, J9, K6, L7
VCC00	A14, A3, F8, F9
VCCO1	C16, J11, P16
VCCO2	L8, L9, T3,T14
VCCO3	C1, H6, P1
VCCX	H11, J6
VSS	A1, A16, B15, B2, F7, G10, G6, G7, G8, G9, K10, K11,
	K7, K8, K9, L10, R2, R15, T1, H9, H7, J10, J8

UG103-1.3E 35(69)

3.4 View of GW1N-6 Pins Distribution

3.4.1 View of QN48 Pins Distribution

Figure 3-24 View of GW1N-6 QN48 Pins Distribution (Top View)

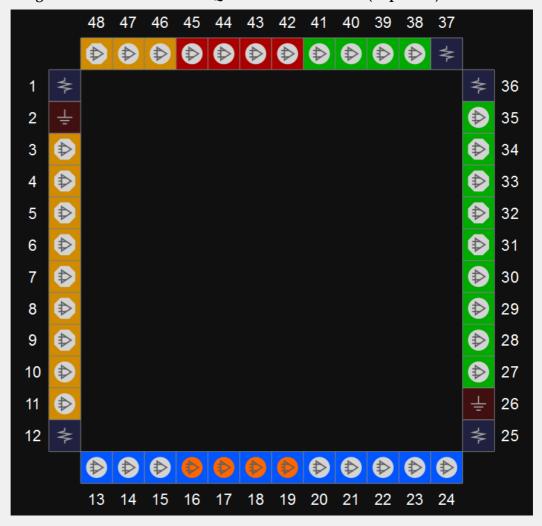


Table 3-24 Other pins in GW1N-6 QN48

VCC	12, 37
VCCO0/VCCO3	1
VCCO1/VCCO2	25
VCCX	36
VSS	2, 26

UG103-1.3E 36(69)

3.4.2 View of CM64 Pins Distribution

Figure 3-25 View of GW1N-6 CM64 Pins Distribution (Top View)

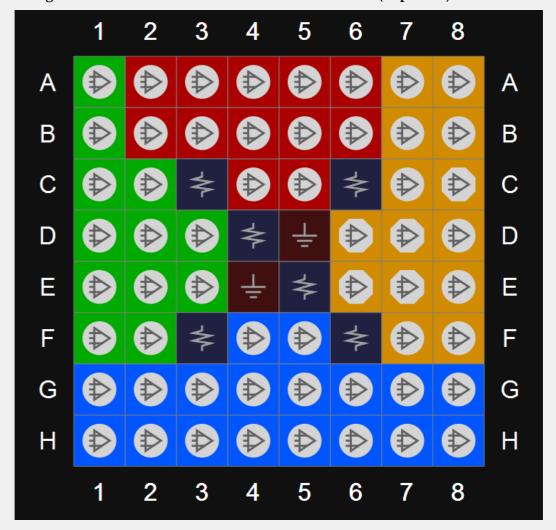


Table 3-25 Other pins in GW1N-6 CM64

VCC	D4, E5
VCCO0/VCCO2	C6
VCCO1/VCCO3	F3
VCCX	C3, F6
VSS	E4, D5

UG103-1.3E 37(69)

3.4.3 View of QN88 Pins Distribution

Figure 3-26 View of GW1N-6 QN88 Pins Distribution (Top View)

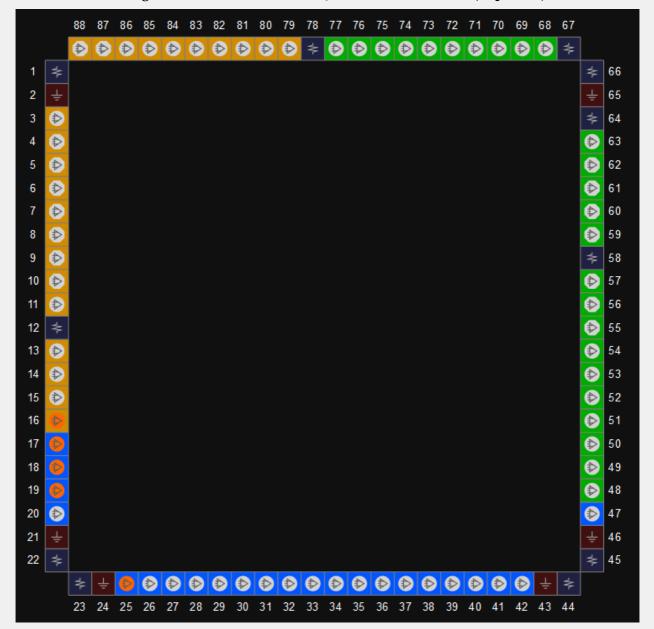


Table 3-26 Other pins in GW1N-6 QN88

VCC	1, 22, 45, 66
VCC00	67
VCCO1	58
VCCO2	23, 44
VCCO3	12
VCCX	64, 78
VSS	2, 21, 24, 43, 46, 65

UG103-1.3E 38(69)

3.4.4 View of LQ100 Pins Distribution

Figure 3-27 View of GW1N-6 LQ100 Pins Distribution (Top View)

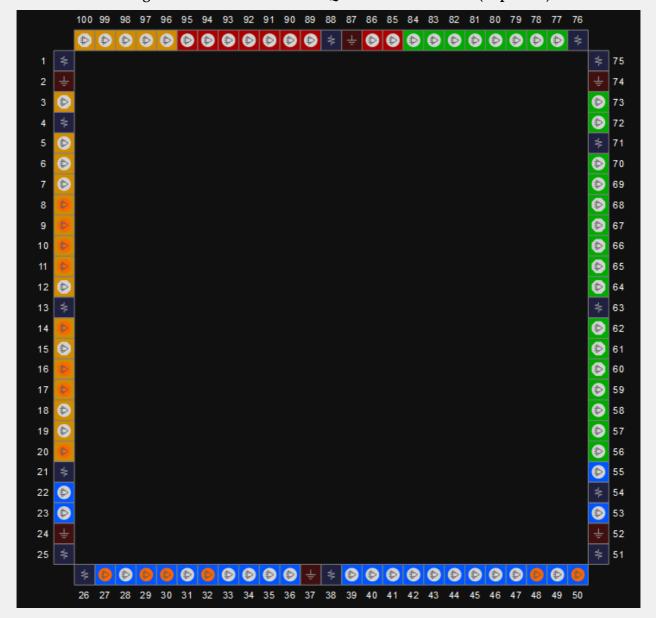


Table 3-27 Other pins in GW1N-6 LQ100

VCC	1, 25, 51, 75
VCCO0	76, 88
VCCO1	63, 71
VCCO2	26, 38
VCCO3	4, 13
VCCX	21, 54
VSS	2, 24, 52, 74, 87, 37

UG103-1.3E 39(69)

3.4.5 View of LQ144 Pins Distribution

Figure 3-28 View of GW1N-6 LQ144 Pins Distribution (Top View)

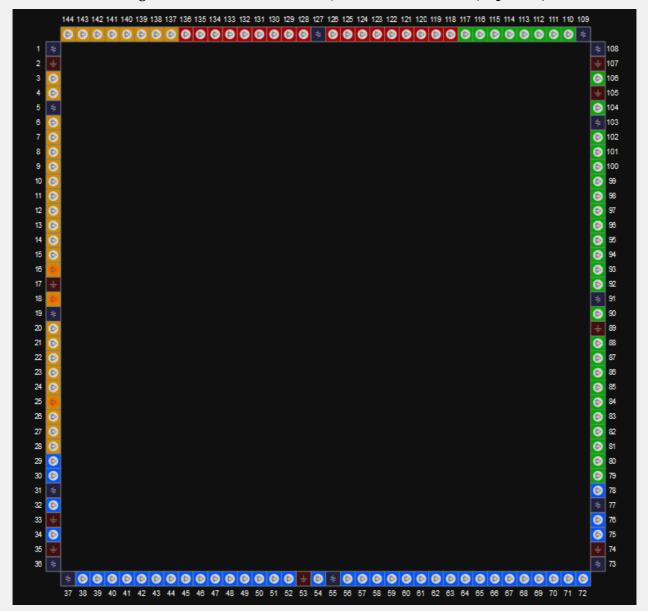


Table 3-28 Other pins in GW1N-6 LQ144

VCC	1, 36, 73, 108
VCC00	109, 127
VCCO1	77, 91
VCCO2	37, 55
VCCO3	5, 19
VCCX	31, 103
VSS	2, 17, 33, 35, 53, 74, 89, 105,107, 107, 125

UG103-1.3E 40(69)

3.4.6 View of MG160 Pins Distribution

Figure 3-29 View of GW1N-6 MG160 Pins Distribution (Top View)

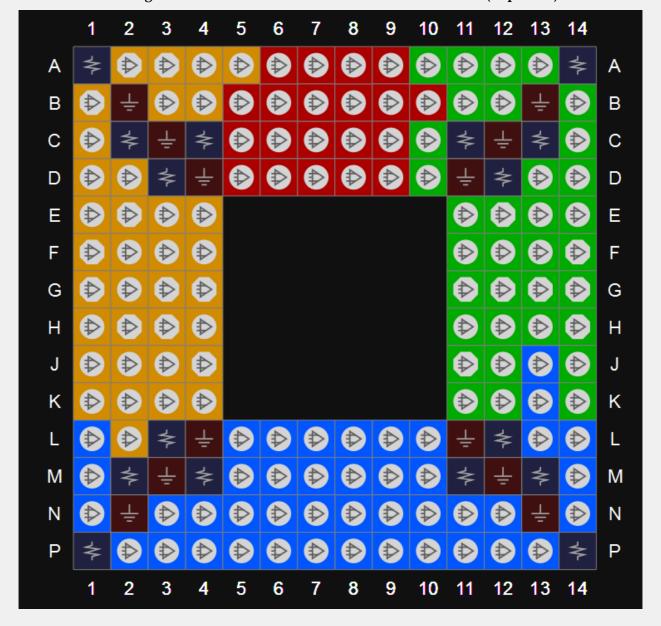


Table 3-29 Other pins in GW1N-6 MG160

VCC	A1, A14, P1, P14
VCCO0	C4, C11
VCCO1	D12, L12
VCCO2	M11, M4
VCCO3	D3, L3
VCCX	C13, C2, M13, M2
VSS	B13, B2, C12, C3, D11, D4, L11, L4, M12, M3, N13, N2

UG103-1.3E 41(69)

3.4.7 View of LQ176 Pins Distribution

Figure 3-30 View of GW1N-6 LQ176 Pins Distribution (Top View)

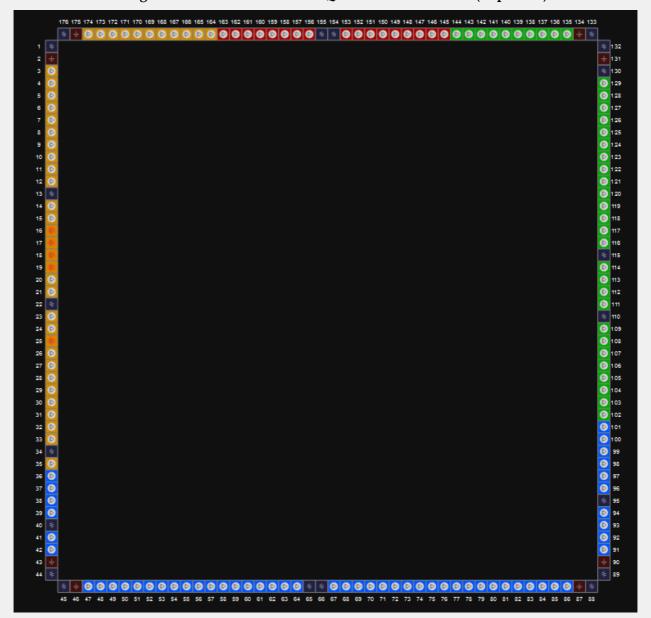


Table 3-30 Other pins in GW1N-6 LQ176

VCC	1, 44, 89, 132
VCC00	133, 155, 176
VCCO1	95, 110, 115
VCCO2	45, 65, 88
VCCO3	13, 22, 34
VCCX	40, 66, 130, 154
VSS	2, 43, 46, 87, 90, 131, 134, 175

UG103-1.3E 42(69)

3.4.8 View of PG256 Pins Distribution

Figure 3-31 View of GW1N-6 PG256 Pins Distribution (Top View)

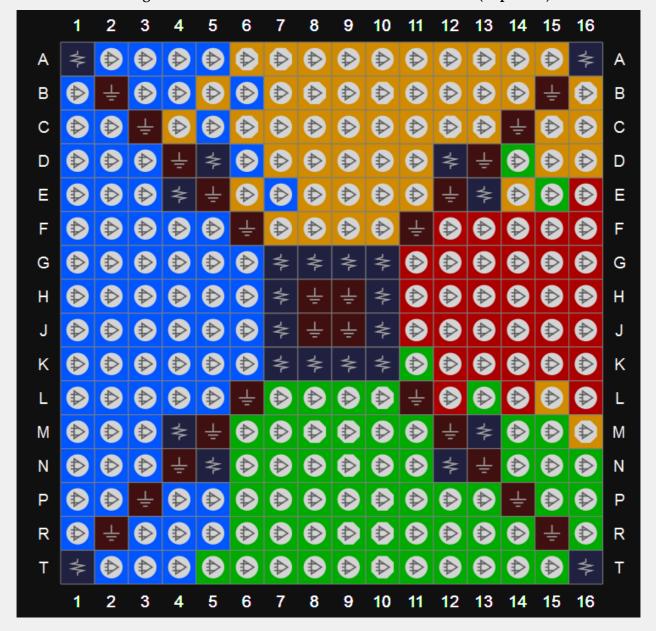


Table 3-31 Other pins in GW1N-6 PG256

VCC	A1, A16, G7, G10, K7, K10, T1, T16
VCCO0	E13, J10, M13, H10
VCCO1	K8, N5, N12
VCCO2	E4, H7, M4, J7
VCCO3	D12, D5, G9
VCCX	G8, K9
VSS	B2, B15, C3, C14, D4, D13, E5, E12, F6, F11, H8, H9, J8, J9, L6, L11, M5, M12, N4, N13, P3, P14, R2, R15

UG103-1.3E 43(69)

3.4.9 View of UG256 Pins Distribution

Figure 3-32 View of GW1N-6 UG256 Pins Distribution (Top View)

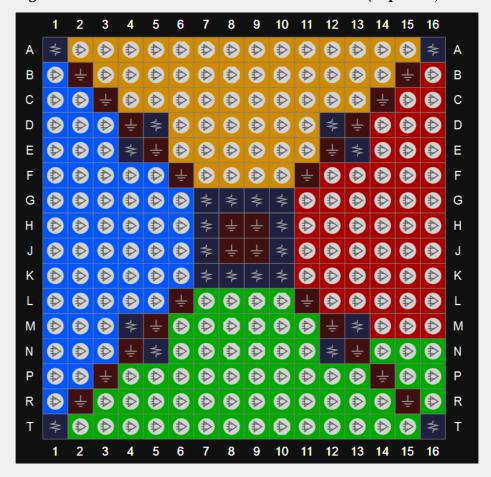


Table 3-32 Other pins in GW1N-6 UG256

VCC	A1, A16, G10, G7, K10, K7, T1, T16
VCC00	E13, H10, J10, M13
VCCO1	K8, K9, N12,N5
VCCO2	E4, H7, J7, M4
VCCO3	D12, D5, G9
VCCX	G8
VSS	B15, B2, C14, C3, D13, D4, E12, E5, F11, F6, H8, H9, J8, J9, L11, L6,
v 33	M12, M5, N13, N4, P14, P3, R15, R2

UG103-1.3E 44(69)

3.4.10 View of UG332 Pins Distribution

Figure 3-33 View of GW1N-6 UG332 Pins Distribution (Top View)



Table 3-33 Other pins in GW1N-6 UG332

VCC	J10, J11, K9, K12, L9, L12, M10, M11
VCC00	J13, K13, K5, L8
VCCO1	N9, N12, M8,J8
VCCO2	K8, H11, N10, N11, L13
VCCO3	H10, H9, H12
VCCX	A1, M13
VSS	A10, A20, C3, C18, E11, H8, H13, J9, J12, K10, K11, K20, L5, L10,
	L11, L16, M9, M12, N8, N13, T10, V3, V18, Y1, Y11, Y20, N18
NC	N18, P20, G1, H3

UG103-1.3E 45(69)

3.5 View of GW1N-9 Pins Distribution

3.5.1 View of QN48 Pins Distribution

Figure 3-34 View of GW1N-9 QN48 Pins Distribution (Top View)

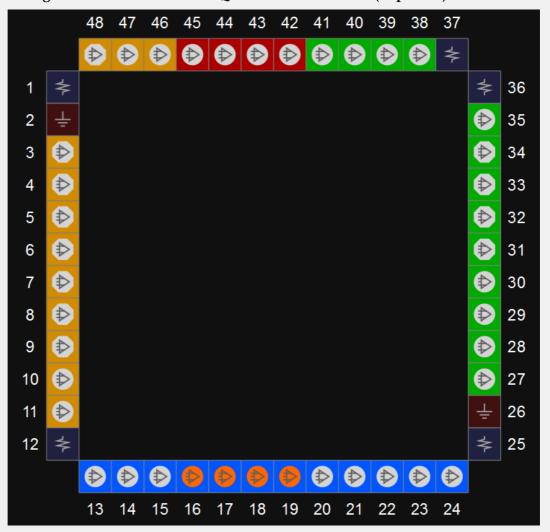


Table 3-34 Other pins in GW1N-9 QN48

VCC	12, 37
VCCO0/VCCO3	1
VCCO1/VCCO2	25
VCCX	36
VSS	2, 26

UG103-1.3E 46(69)

3.5.2 View of CM64 Pins Distribution

Figure 3-35 View of GW1N-9 CM64 Pins Distribution (Top View)

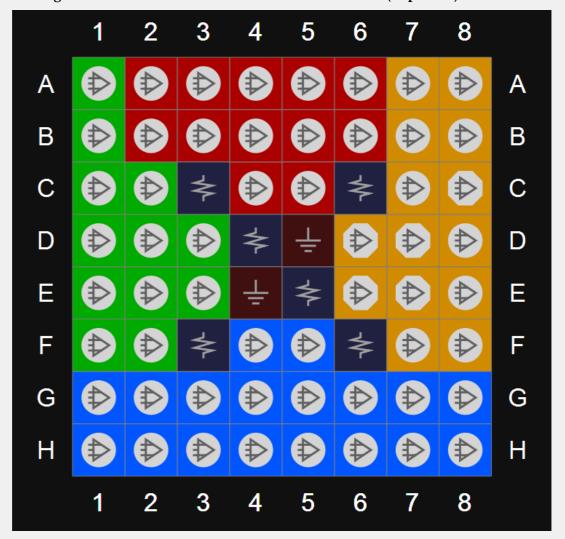


Table 3-35 Other pins in GW1N-9 CM64

VCC	D4, E5
VCCO0/VCCO2	C6
VCCO1/VCCO3	F3
VCCX	C3, F6
VSS	D5, E4

UG103-1.3E 47(69)

3.5.3 View of QN88 Pins Distribution

Figure 3-36 View of GW1N-9 QN88 Pins Distribution (Top View)

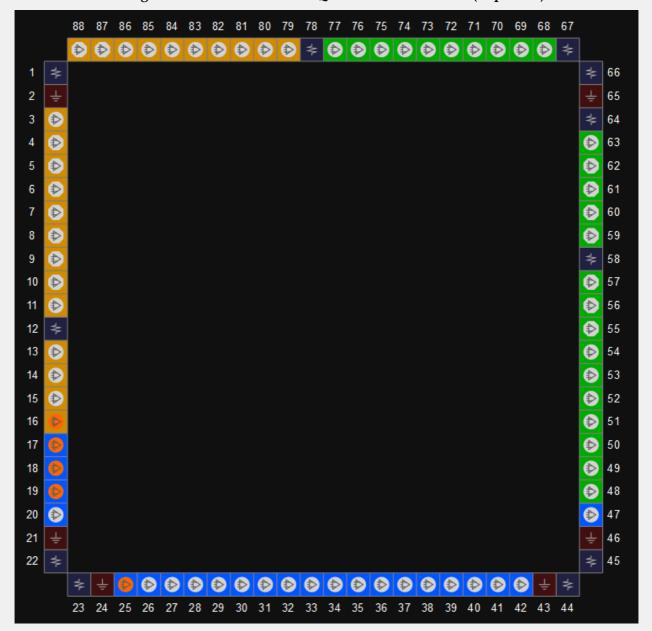


Table 3-36 Other pins in GW1N-9 QN48

VCC	1, 22, 45, 66
VCCO0	67
VCCO1	58
VCCO2	23, 44
VCCO3	12
VCCX	64, 78
VSS	2, 21, 24, 43, 46, 65

UG103-1.3E 48(69)

3.5.4 View of LQ100 Pins Distribution

Figure 3-37 GW1N-9 LQ100 Pins Distribution View (Top View)

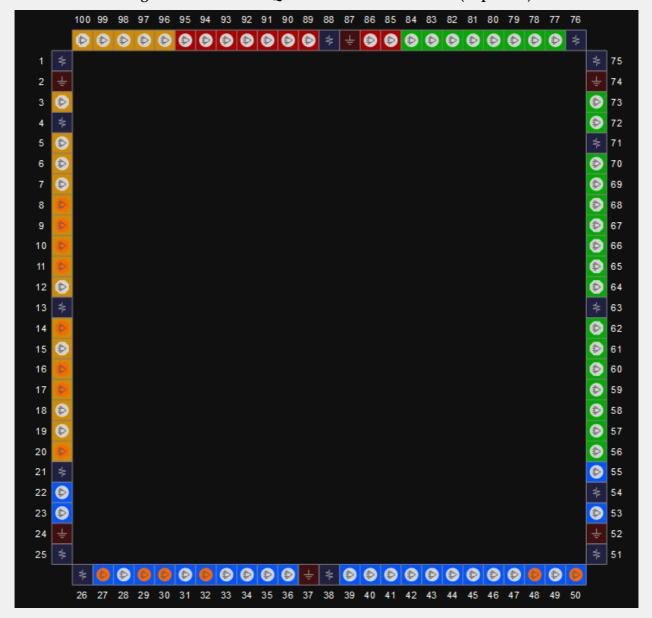


Table 3-37 Other pins in GW1N-9 LQ100

VCC	1, 25, 51, 75
VCC00	76, 88
VCCO1	63, 71
VCCO2	26, 38
VCCO3	4, 13
VCCX	21, 54
VSS	2, 24, 52, 74, 87, 37

UG103-1.3E 49(69)

3.5.5 View of LQ144 Pins Distribution

Figure 3-38 View of GW1N-9 LQ144 Pins Distribution (Top View)

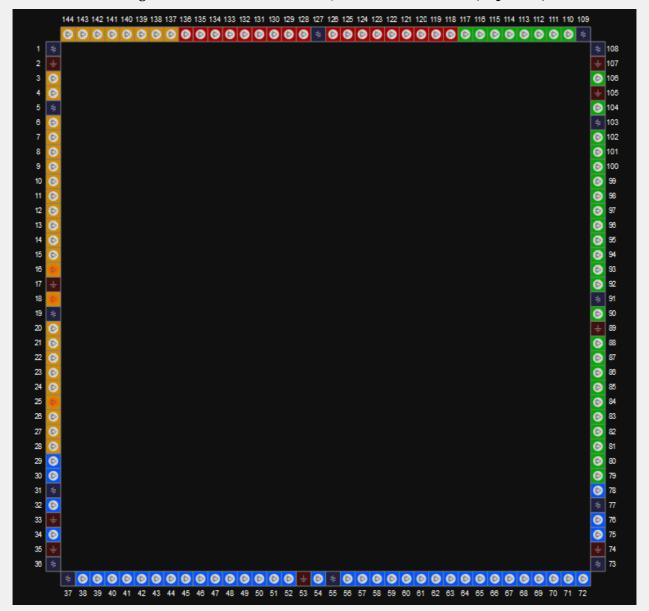


Table 3-38 Other pins in GW1N-9 LQ144

VCC	1, 36, 73, 108
VCCO0	109, 127
VCCO1	77, 91
VCCO2	37, 55
VCCO3	5, 19
VCCX	31, 103
VSS	2, 17, 33, 35, 53, 74, 89, 105,107, 107, 125

UG103-1.3E 50(69)

3.5.6 View of MG160 Pins Distribution

Figure 3-39 GW1N-9 MG160 Pins Distribution View (Top View)

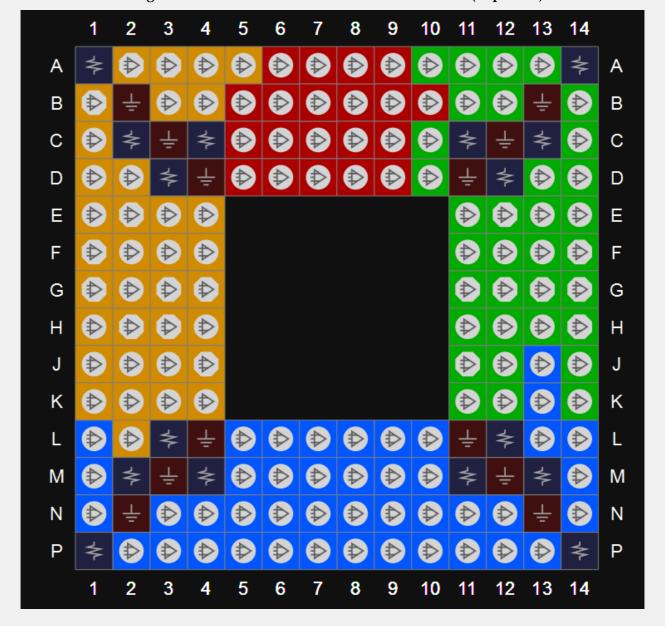


Table 3-39 Other Pins in GW1N-9 MG160

VCC	A1, A14, P1, P14
VCC00	C4, C11
VCCO1	D12, L12
VCCO2	M11, M4
VCCO3	D3, L3
VCCX	C13, C2, M13, M2
VSS	B13, B2, C12, C3, D11, D4, L11, L4, M12, M3, N13, N2

UG103-1.3E 51(69)

3.5.7 View of LQ176 Pins Distribution

Figure 3-40 View of GW1N-9 LQ176 Pins Distribution (Top View)

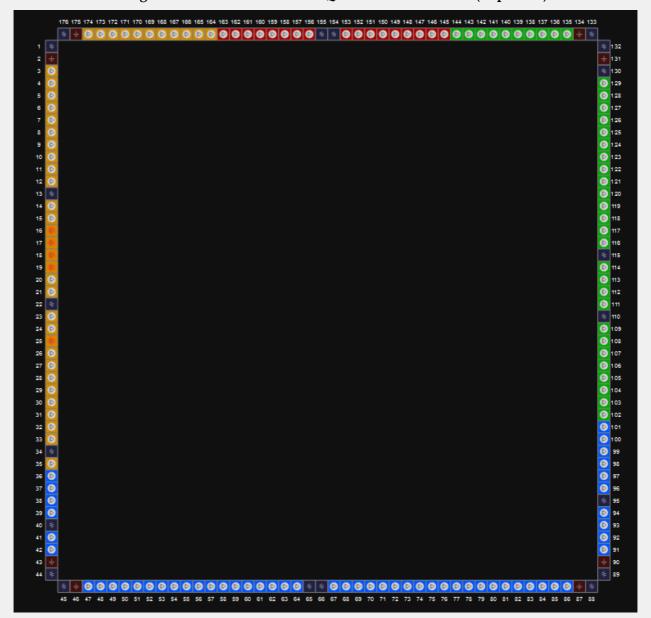


Table 3-40 Other pins for GW1N-9 LQ176

VCC	1, 44, 89, 132
VCC00	133, 155, 176
VCCO1	95, 110, 115
VCCO2	45, 65, 88
VCCO3	13, 22, 34
VCCX	40, 66, 130, 154
VSS	2, 43, 46, 87, 90, 131, 134, 175

UG103-1.3E 52(69)

3.5.8 View of PG256 Pins Distribution

Figure 3-41 View of GW1N-9 PG256 Pins Distribution (Top View)

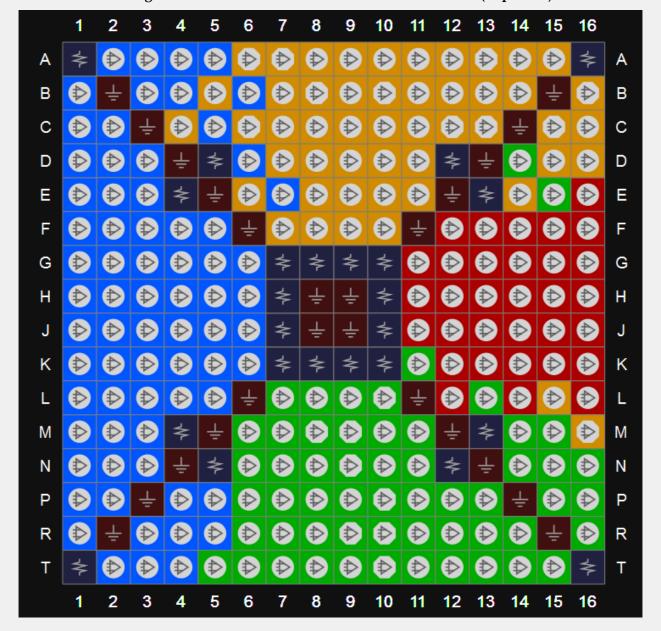


Table 3-41 Other pins in GW1N-9 PG256

VCC	A1, A16, G7, G10, K7, K10, T1, T16
VCC00	E13, J10, M13, H10
VCCO1	K8, N5, N12
VCCO2	E4, H7, M4, J7
VCCO3	D12, D5, G9
VCCX	G8, K9
VSS	B2, B15, C3, C14, D4, D13, E5, E12, F6, F11, H8, H9, J8, J9, L6, L11,
V 33	M5, M12, N4, N13, P3, P14, R2, R15

UG103-1.3E 53(69)

3.5.9 View of UG256 Pins Distribution

Figure 3-42 View of GW1N-9 UG256 Pins Distribution (Top View)

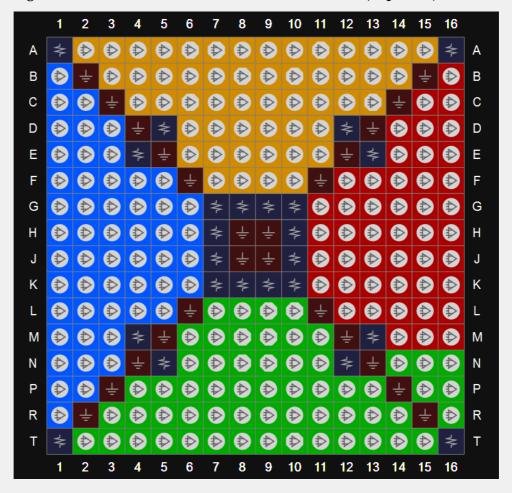


Table 3-42 Other pins in GW1N-9 UG256

VCC	A1, A16, G10, G7, K10, K7, T1, T16
VCCO0	E13, H10, J10, M13
VCCO1	K8, K9, N12,N5
VCCO2	E4, H7, J7, M4
VCCO3	D12, D5, G9
VCCX	G8
VSS	B15, B2, C14, C3, D13, D4, E12, E5, F11, F6, H8, H9, J8, J9, L11, L6,
700	M12, M5, N13, N4, P14, P3, R15, R2

UG103-1.3E 54(69)

3.5.10 View of UG332 Pins Distribution

Figure 3-43 View of GW1N-9 UG332 Pins Distribution (Top View)



Table 3-43 Other pins in GW1N-9 UG332

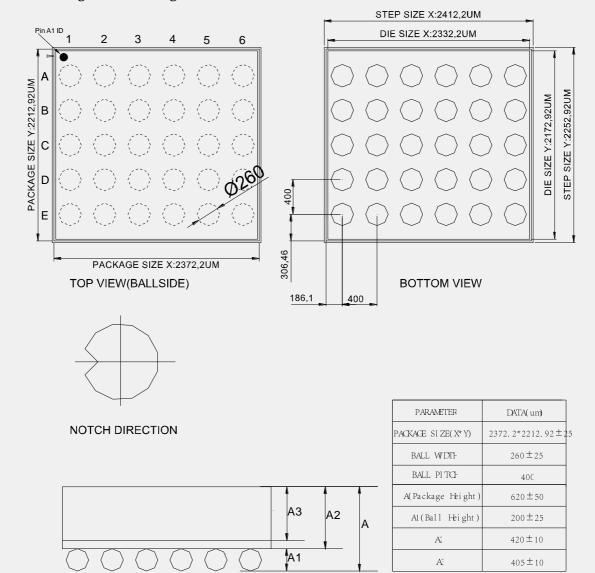
VCC	J10, J11, K9, K12, L9, L12, M10, M11
VCC00	J13, K13, K5, L8
VCCO1	N9, N12, M8,J8
VCCO2	K8, H11, N10, N11, L13
VCCO3	H10, H9, H12
VCCX	A1, M13
VSS	A10, A20, C3, C18, E11, H8, H13, J9, J12, K10, K11, K20, L5, L10,
VSS	L11, L16, M9, M12, N8, N13, T10, V3, V18, Y1, Y11, Y20, N18
NC	N18, P20, G1, H3

UG103-1.3E 55(69)

4 Package Diagrams

4.1 CS30 Package Outline (2.3mm x 2.4mm)

Figure 4-1 Package Outline CS30

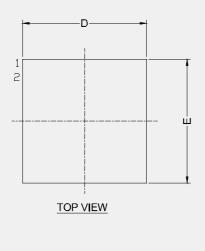


UG103-1.3E 56(69)

* CONTROLLING DIMENSION: MM

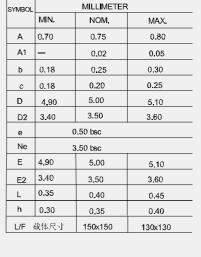
4.2 QN32 Package Outline (5mm x 5mm)

Figure 4-2 Package Outline QN32









EXPOSED THERMAL PAD ZERO

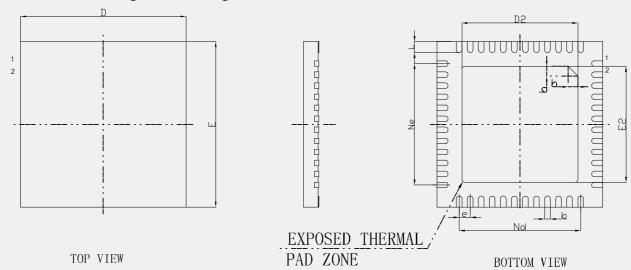
BOTTOM VIEW

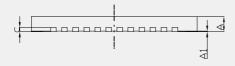
SIDE VIEW

UG103-1.3E 57(69)

4.3 QN48 Package Outline (6mm x 6mm)

Figure 4-3 Package Outline QN48





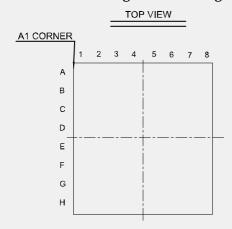
SIDE VIEW

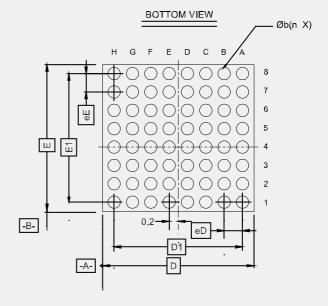
SYMBOL	MILLIMETER				
STMBOL	MIN	NOM	MAX		
A	0.50	0.55	0.60		
A1	0	0.02	0.05		
b	0. 15	0.20	0. 25		
c	0.10	0.15	0. 20		
D	5. 90	6.00	6. 10		
D2	4. 10 4.20		4. 30		
e	0. 40BSC				
Ne	4	4. 40BSC			
Nd	4	4. 40BSC			
Е	5. 90	6.00	6. 10		
E2	4. 10	4.20	4. 30		
L	0.35	0.40	0.45		
h	0. 30	0.40			
L/F裁体尺寸 (WIL)	177*177				

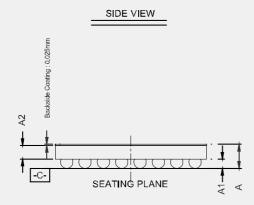
UG103-1.3E 58(69)

4.4 CM64 Package Outline (4.1mm x 4.1mm)

Figure 4-4 Package Outline CM64





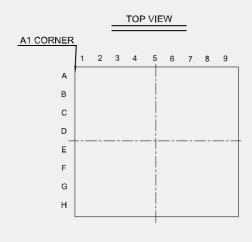


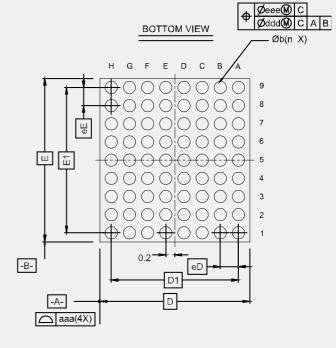
		COMMON DIMENSIONS			
	SYMBOL	MIN.	NOM.	мах.	
Total Thickness	Α	0.570	0.620	0.670	
Stand Off	A1	0.175	0.200	0.225	
Wafer Thickness	A2	0.400 ±0.025			
Body Size	D		4,1	BSC	
Body Size	Е		4.1	BSC	
Ball Diameter(Size)		0.260			
Ball/Bump Width	b	0.230	0.260	0.290	
	θD		0.500		
Ball/Bump Pitch	еE	0.500			
Ball/Bump Count	n		64		
Edge Ball Center to Center	D1		3.500	BSC	
Edge Ball Center to Center	E1		3.500	BSC	

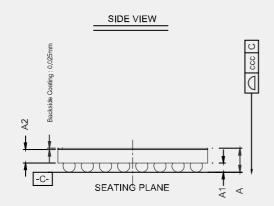
UG103-1.3E 59(69)

4.5 CS72 Package Outline (3.6mm x 3.3mm)

Figure 4-5 Package Outline CS72





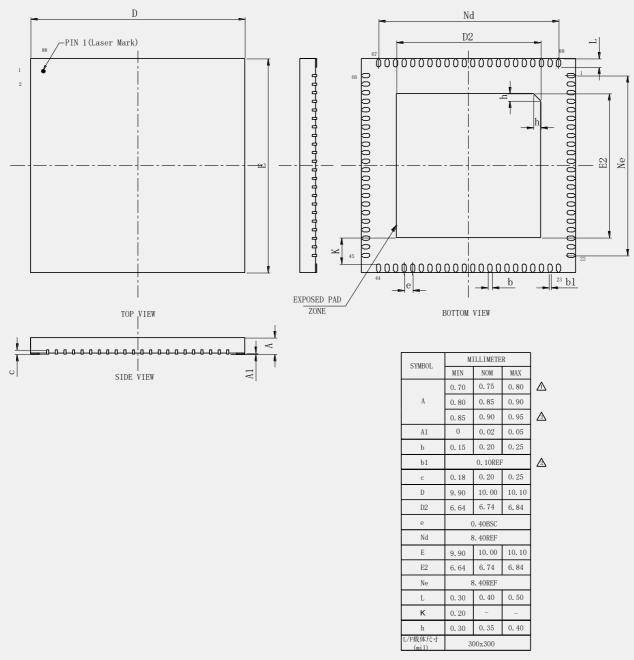


	SYMBOL COMMON DIMENSION			ISIONS
	SYMBOL	MIN.	NOM.	MAX.
Total Thickness	Α	0.485	0.525	0.565
Stand Off	A1	0.170	-	0.230
Wafer Thickness	A2	0.3	00 ±0.02	5
Body Size	D		3,3	BSC
Body Size	Е		3.6	BSC
Ball Diameter(Size)			0.250	
Ball/Bump Width	b	0.240	0.270	0.300
	eD		0.400	
Ball/Bump Pitch	eE		0.400	
Ball/Bump Count	n		72	
Edge Ball Center to Center	D1	2.800 B		
Edge Ball Center to Center	E1	3.200		BSC
Package Edge Tolerance	aaa		0.030	
Coplanarity(whole wafer)	ccc		0.075	
Ball/Bump Offset(Package)	ddd		0.050	
Ball/Bump Offset(Ball)	eee		0.015	

UG103-1.3E 60(69)

4.6 QN88 Package Outline (10mm x 10mm)

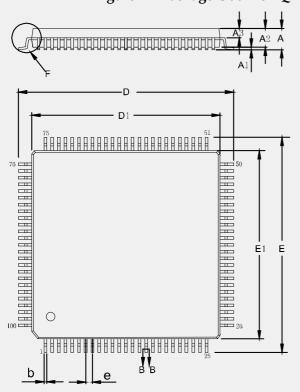
Figure 4-6 Package Outline QN88

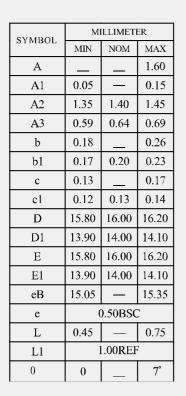


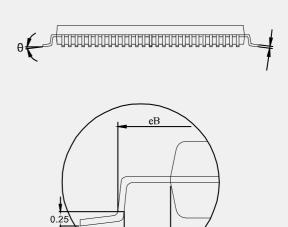
UG103-1.3E 61(69)

4.7 LQ100 Package Outline (16mm x 16mm)

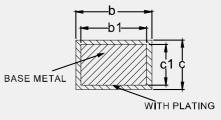
Figure 4-7 Package Outline LQ100







DETAIL: F

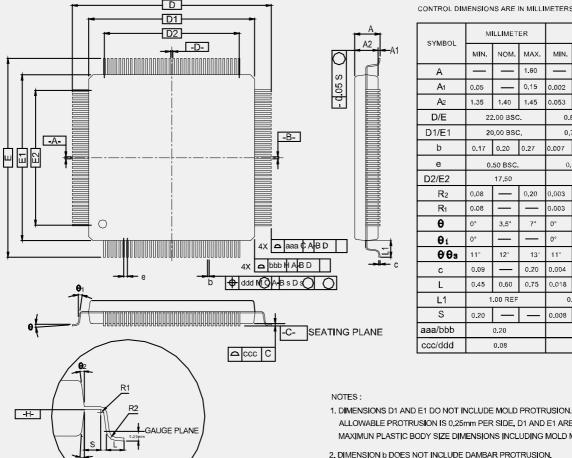


SECTION B-B

UG103-1.3E 62(69)

4.8 LQ144 Package Outline (22mm x 22mm)

Figure 4-8 Package Outline LQ144



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER		INCH			
STIMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
Α	_	_	1.60	_	_	0.063
A ₁	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D/E	22	2.00 BSC	; .	0.8	866 BSC	
D1/E1	20	0.00 BSC).	0.787 BSC.		
b	0.17	0.20	0.27	0.007	800.0	0.011
е	0.	.50 BSC.		0.020 BSC.		
D2/E2		17.50		0.689		
R ₂	80.0		0.20	0.003	1	0.008
R ₁	80.0	1	1	0.003	l	l
θ	0°	3.5°	7°	0°	3.5°	7°
θí	0°	_	1	0°	1	
∂ Өз	11°	12°	13°	11°	12°	13°
С	0.09	-	0.20	0.004	l	800.0
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	_		0.008	_	_
aaa/bbb	0.20 0.008					
ccc/ddd		80.0	, The state of the	0.003		

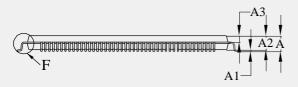
- ALLOWABLE PROTRUSION IS 0.25mm PER SIDE, D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH,
- 2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

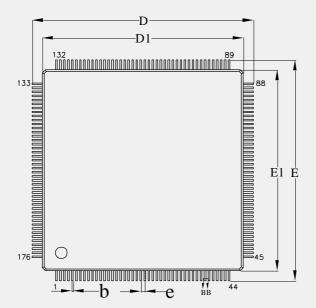
DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.

UG103-1.3E 63(69)

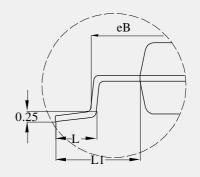
4.9 LQ176 Package Outline (22mm x 22mm)

Figure 4-9 Package Outline LQ176

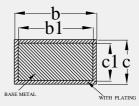








DETAIL: F



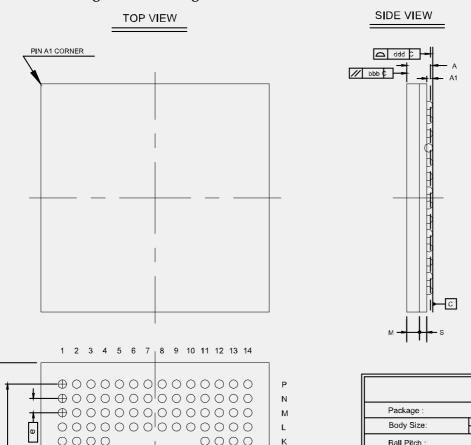
SECTION B-B

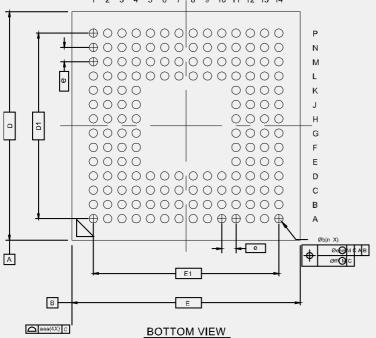
SYMBOL	M	MILLIMETER			
STNIBOL	MIN	NOM	MAX		
A			1.60		
A1	0.05	0.10	0.15		
A2	1.30	1.40	1.50		
A3	0.59	0.64	0.69		
b	0.14		0.22		
b1	0.13	0.16	0.19		
c	0.13		0.17		
c1	0.12	0.13	0.14		
D	21.80	22.00	22.20		
D1	19.90	20.00	20.10		
Е	21.80	22.00	22.20		
E1	19.90	20.00	20.10		
e	0.40BSC				
eB	21.15		21.40		
L	0.45	0.60	0.75		
L1	1.00REF				
θ	0 7°				

UG103-1.3E 64(69)

4.10 MG160 Package Outline (8mm x 8mm)

Figure 4-10 Package Outline MG160



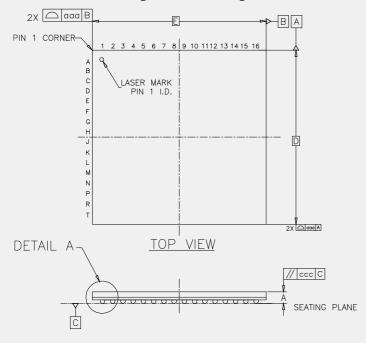


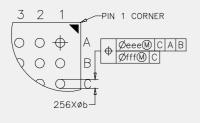
			Common Dimensions		
		Symbol	MIN.	NOM.	MAX.
Package :			MBGA		
Body Size:	X	EC		8.000	
Ball Pitch :		е		0.500	
Total Thickness:		Α	-	-	1.000
Mold Thickness:		М		0,450	Ref.
Substrate Thickness :		Ø	0.260 Ref.		
Ball Diameter:			0.300		
Stand Off :		A1	0.160	1	0.260
Ball Width :		b	0.270	-	0.370
Package Edge Tolerand	e :	888		0.100	
Mold Parallelism :		ccc		0.100	
Coplanarity:		ddd	0.080		
Ball Offset (Package) :	666	0.150			
Ball Offset (Ball):	fff		0.080		
Ba ll Count :	Ball Count: n 160				
Edge Ball Center to Center :	X	E1 D1	-		

UG103-1.3E 65(69)

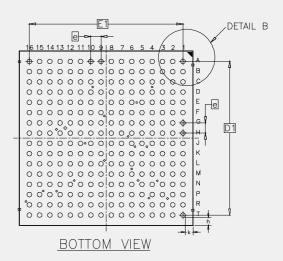
4.11 PG256M Package Outline (17mm x 17mm)

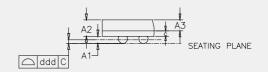
Figure 4-11 Package Outline PG256M





DETAIL B(2:1)





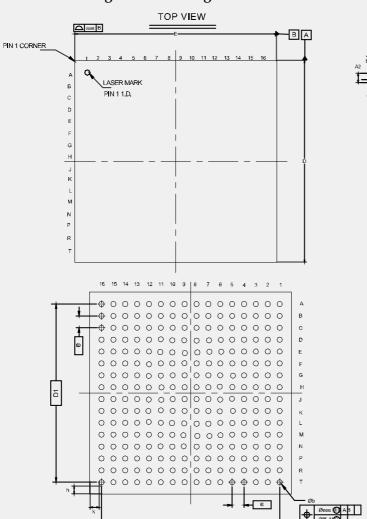
DETAIL A(2:1)

SYMBOL	MILLIMETER				
	MIN	NOM	MAX		
Α			1.22		
A1	0.30	0.35	0.40		
A2	0.74	0.79	0.84		
C	0.22	0.26	0.30		
А3	0	.53 BASI			
D	16.90	17.00	17.10		
D1	15.00 BASIC				
E	16.90	17.00	17.10		
E1	1:	5.00 BAS	iIC		
Φ	1	.00 BASI)		
b	0.40	0.45	0.50		
aaa		0.10			
ccc		0.20			
ddd	0.12				
eee	0.15				
fff	0.08				
h	0.775 REF				
k	0.775 REF				

UG103-1.3E 66(69)

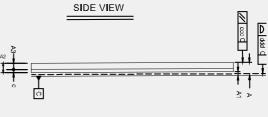
4.12 PG256 Package Outline (17mm x 17mm)

Figure 4-12 Package Outline PG256



E1

BOTTOM VIEW

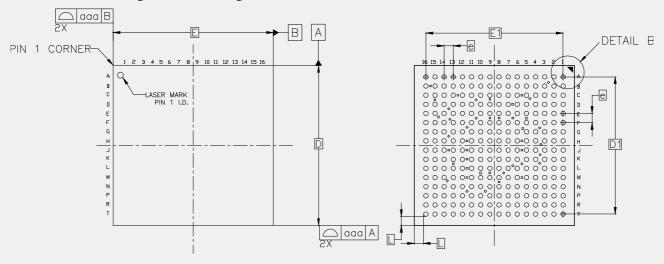


SYMBOL MILLIMETER					
	MIN	NOM	MAX		
Α	_	_	1.22		
A1	0.30	0.35	0.40		
A2	0.74	0.79	0.84		
С	0.22	0.26	0.30		
A3	0.53 BASIC				
D	16.90	17.00	17.10		
D1	15.00 BASIC				
Е	1.22	1.22	1.22		
E1	15.00 BASIC				
е	1.00 BASIC				
b	0.40	0.45	0.50		
aaa		0.10			
ccc	0.20				
ddd	0.12				
eee	0.15				
fff	0.08				
h	0.775 REF				
k	0.775 REF				

UG103-1.3E 67(69)

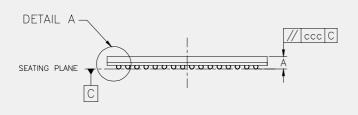
4.13 UG256 Package Outline (14mm x 14mm)

Figure 4-13 Package Outline UG256

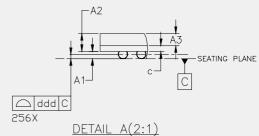


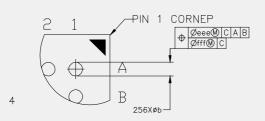
TOP VIEW

BOTTOM VIEW









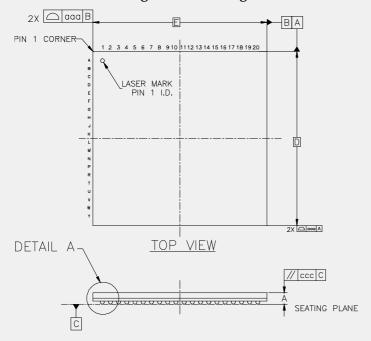
DETAIL B(3:1)

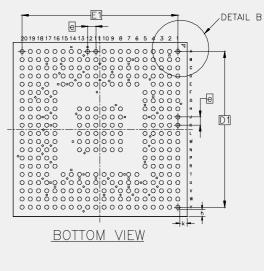
SYMBOL	MILLIMETER				
	MIN	MOM	MAX		
Α			1.18		
A1	0.26	0.31	0.36		
A2	0.74	0.79	0.84		
A3	0.53 BASIC				
С	0.22	0.26	0.30		
D	13.90	14.00	14.10		
D1	12.00 BASIC				
E	13.90	14.00	14.10		
E1	12.00 BASIC				
е	0.8 BASIC				
ь	0.35	0.40	0.45		
L	0,8 REF				
aaa	0.10				
ccc	0.20				
ddd	0.12				
eee	0.15				
fff	0.08				

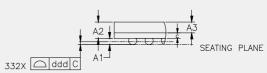
UG103-1.3E 68(69)

4.14 UG332 Package Outline (17mm x 17mm)

Figure 4-14 Package Outline UG332







4 3 2 1 PIN 1 CORNER

O O O B

Øeee® C A B

Øfff® C

332×øb

DETAIL B(2:1)

DETAIL A(2:1)

SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
Α			1.18	
A1	0.26	0.31	0.36	
A2	0.74	0.79	0.84	
С	0.22	0.26	0.30	
А3	0.53 BASIC			
D	16.90	17.00	17.10	
D1	15.20 BASIC			
E	16.90	17.00	17.10	
E1	15.20 BASIC			
е	0.800 BASIC			
b	0.35	0.40	0.45	
aaa	0.15			
ccc	0,15			
ddd	0.10			
eee	0.15			
fff	0.08			
h	0.700 REF			
k	0.700 REF			

UG103-1.3E 69(69)

