

YIFEI CUI

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EDUCATION

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| University of Electronic Science and Technology of China (UESTC) | 09/2021-07/2025 |
| Glasgow College, jointly held by the University of Glasgow | |
| <ul style="list-style-type: none">Major: Electronic Information Engineering, BEngGPA: 3.91/4.0, Weighted Average: 89.87/100, Ranking: 4/247(1.6%) | |
| University of Glasgow | 09/2021-07/2025 |
| <ul style="list-style-type: none">Program: Electronics and Electrical Engineering, BEngExpected: First-class Degree with Distinction | |
| National University of Singapore, NUS, winter program | 01/2022-02/2022 |
| Artificial Intelligence and Machine Learning – Computer Vision | |
| <ul style="list-style-type: none">Learned the principles and background of neural networksRealized traffic sign recognition using the scikit-learn library and convolutional neural network in the python platform | |

RESEARCH EXPERIENCE

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| Neural Network based Surface Decoder for the Scalable Quantum Error Correction | 08/2023-06/2025 |
| Supervisor: Prof. Cheng Wang | |
| <ul style="list-style-type: none">Project Focus: Developing a scalable neural network-based surface decoder for quantum error correction to address the inefficiencies of traditional decoders, such as Minimum Weight Perfect Matching (MWPM), in large-scale quantum systems. | |
| Key Responsibilities: | |
| <ul style="list-style-type: none">Noise Modeling: Designed a quantum noise model covering measurement errors, data qubit idling (T1, T2 parameters), syndrome extraction errors, and qubit leakage. [Completed]Model Verification: Compared model accuracy with standard error models using error pair correlation matrices from experiments and simulations. [Near Completion]Neural Network Decoder: Initiated the design of a machine learning-based decoder aimed at improving speed and accuracy over MWPM. [In Progress] | |

PROJECT EXPERIENCES

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| An Intelligent Rover Design, team leader | 02/2024-06/2024 |
| <ul style="list-style-type: none">Completed the main program design using STM32CubeIDE, and realized the task execution and switching via polling and external environment interruptRealized visual algorithm with OpenMV and its IDE, adopted H-bridge to design the driver module PCB independently, and finished physical verificationUsed STM32F446RE, McNamum wheel, Openmv Cam, ultrasonic module, DCDC power module, lithium battery and self-designed driven module to realize the hardware welding of the rover, and finally ensure the functions, including line patrol, direction sign and traffic light recognition, pedestrian and obstacle avoidance, wireless switch parking lever | |
| Cross-coupled Cavity Filter Design | 02/2024-06/2024 |
| <ul style="list-style-type: none">Applied cross-coupling technology to increase bandwidth, enhance coupling, and provide additional attenuationDetermined the filter topology by simulating filter parameters with CoupleFilDesigned and simulated using HFSS, and adjusted iteratively according to the results until it meets the design requirements (center frequency: 1.5GHz; Bandwidth: 20MHz; Attenuation: >35dB@ (1520-1540) MHz; Insertion loss: <1dB return loss: >20dB) | |
| Digital CPU Design | 02/2023-07/2023 |
| <ul style="list-style-type: none">Datapath Design: Composed a specification for basic CPU, designed ALU component, coded, synthesized and conducted verification for datapath componentController Design: Understood the STG for the control unit, designed state transition component, coded, synthesized and conducted verification for controller component | |

- CPU Integration: Combined the datapath and the controller, coded, synthesized and conducted simulation for the whole CPU
- CPU Verification and Design Improvement: Downloaded the bitstream to FPGA & conducted verification again, added other instructions, implemented accumulator function, enhanced CPU feature by enlarge the number of registers, the word-length, and so on

Design of Folded Common-source Common-gate Amplifier

06/2023-07/2023

- Employed 2.5V devices, nmos_rf_25 and pmos_rf_25, under the TSMC 65nm GP process in Cadence Virtuoso to design folded common-source common-gate amplifiers
- Calculated transconductance, intrinsic gain and current cutoff frequency to complete the Schematic simulation
- Drew layout and performed DRC, LVS and PEX, and finished layout simulation

Weather Clock Embedded System Design

02/2022-06/2022

- Designed the embedded program on Mbed platform, completed the hardware connection via the combination of STM32L432KC single chip microcomputer, esp8266 WIFI module, and OLED display
- Obtained weather time data through the network API, and realized real-time time query and alarm clock setting, and querying the weather of the day and the future

EXTRACURRICULAR ACTIVITIES

Volunteer Activities

- Labour Practice - Road tree maintenance
- Community support - Children's Science and Innovation Experience Courses in the city Science and Technology Museum
- School Anniversary Video Shooting
- Campus Environmental Publicity

Sports Competitions

- Third place in Glasgow College Basketball Class League 05/2023
- UESTC, Freshmen Cup Table Tennis Competition 11/2021
- Glasgow College Freshmen Cup football participation 09/2021

AWARDS AND HONORS

National Scholarship (Top 4%, 10000¥)

First-class Scholarship for Outstanding Students of UESTC

12/2022&2023&2024

Academic Performance Scholarship, (Top 5%, 30000¥)

12/2022&2023&2024

Finalist Prize in the Mathematical Contest In Modeling & Interdisciplinary Contest In Modeling (Top 2%)

05/2023

Second Prize in the Mathematical Modeling Contest of UESTC

11/2022

Watt Innovative Talent Scholarship

12/2022

UESTC Outstanding Social Practice Individual

12/2022

SKILLS

Professional Tools: Keil5, Xilinx, Vivado, PSpice, Cadence Virtuoso, HFSS, LaTeX, MATLAB

Programming Language: C, C++, Python

Others: IELTS- Overall 7.5