**CS 210201 Logic Design –Midterm #2** **Class:** _____

**ID:** _____

**Name:** _____

**(Note: inverted inputs are allowed)**

1. (10%) Find a minimum (shared) two-level, multiple-output NAND-NAND circuit to realize $f_1(A, B, C, D) = \sum m (0, 4, 7, 10, 11, 14, 15)$ and $f_2(A, B, C, D) = \sum m (0, 1, 4, 5, 9, 10, 11, 13, 14)$. (Note: $m_7 = A'BCD$). Draw the network.

**Ans: F1 =a'c'd'+bcd+acd'+ab'c, F2= a'c'd'+c'd+acd'+ab'c**

2. (6%) Complete the timing diagram for the circuit as shown in Fig. 1 (Y from 3~28ns, Z from 2 ~28ns). Assume the AND gate has delay of 3ns and the NOR gate has delay of 2ns.

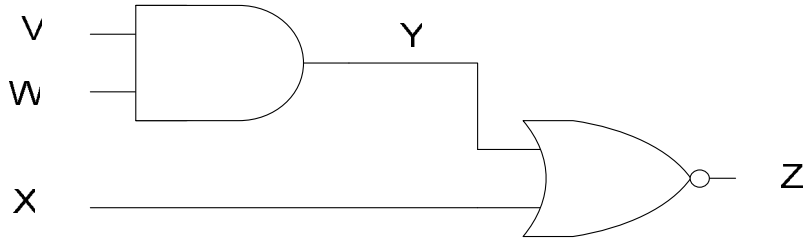
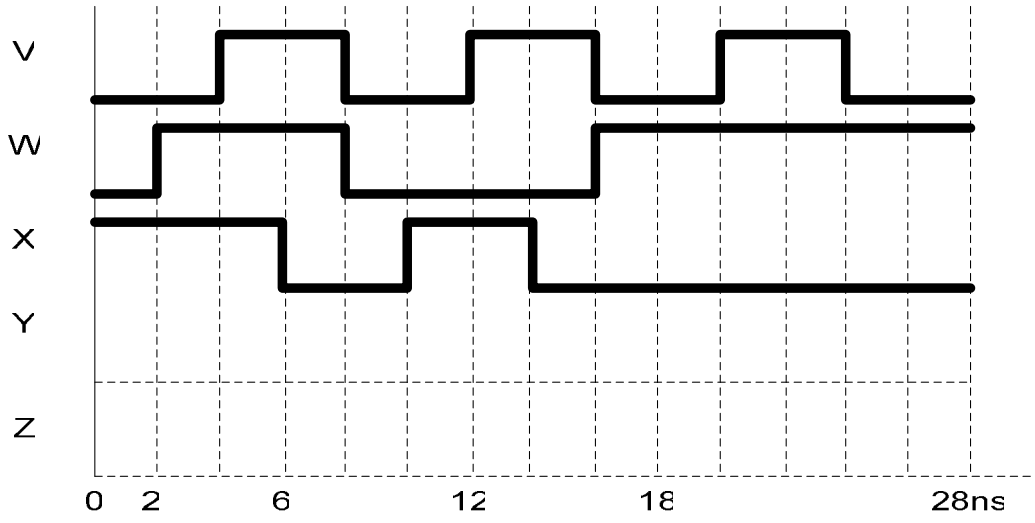



Fig. 1




**A**

**ns: omitted.**

3. (6%) Assume the input transition only differs one bit a time. Consider the function F(A, B, C, D) = ∑ m (0, 2, 5, 7, 8, 10, 13, 14, 15). (a) (2%) Find a minimum AND-OR circuit which implements F. (b) (2%) Identify a 1-hazard in your implementation. (c) (2%) Find an AND-OR circuit for F which has no hazards.

**Ans: (a) F=b'd'+ bd + (abc or acd')**
**(b) 1110 ←→ 1010 or 1110 ←→ 1111**
**(c) F=b'd'+ bd + abc + acd'**

4. (10%) Realize Z = A'C'F + A'DF + A'EF + BC'F + BDF + BEF + A'C'G + A'DG + A'EG + BC'G + BDG + BEG using only eight 2-input NOR gates. Inverted inputs are allowed. (Draw the logic network.)

**Ans: Z= [(F+G) (A'+B)] [(C'+D)+E]**

5. (8%) Given a logic circuit as shown in Fig. 2. According to the SPEC, with applying the input vector (A, B, C, D) = (0, 0, 1, 1), the output value at W should be 0. However, the actual simulation result is 1. Assume the possible errors are only AND ←→NAND, OR←→NOR, Inverter ←→ Buffer, and only one error occurs at a time. Please indicate all possible error locations in which a single error occurs.

**Ans: G1, G3, G4, G6**

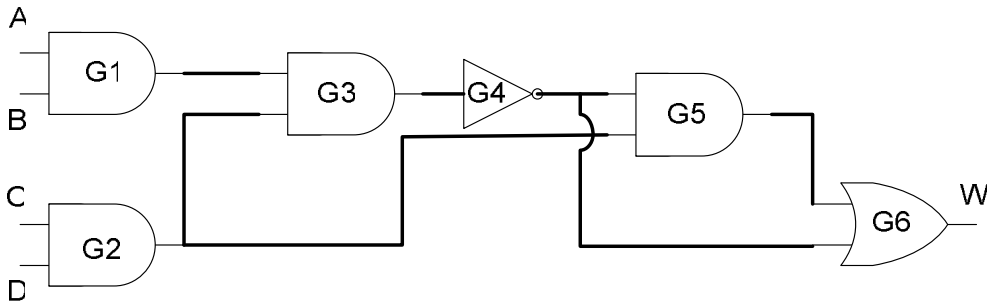



Fig. 2

6. (8%) Implement the function G (A, B, C, D) = ∑ m (0, 1, 5, 6, 7, 9, 11, 12, 13) using an 8:1 MUX with selection inputs A, B, and C as shown in Fig. 3. (Note: $m_3$ = ABCD = 0011, and when ABC=011, $I_3$ will be selected).(Hint: To determine the $I_0$~$I_7$.)

**Ans: $I_0$~$I_7$=10D1DD10**

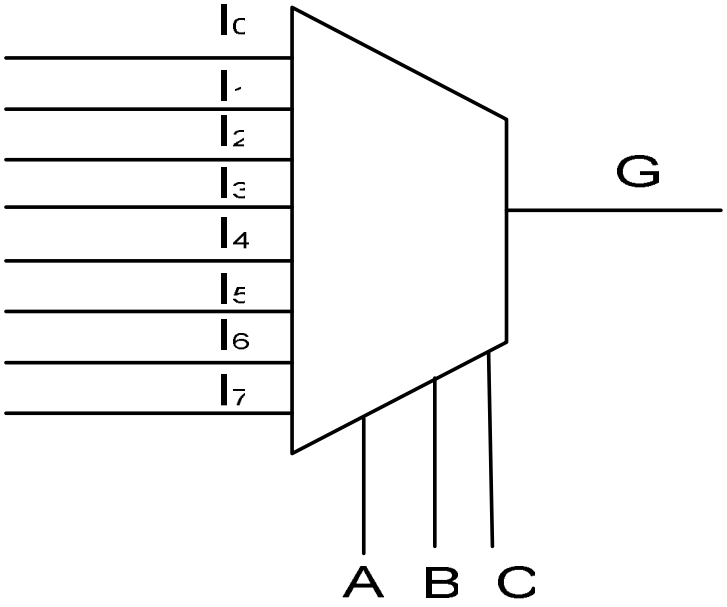



Fig. 3

7. (12%) The PLA in Fig. 4 will be used to implement for the following equations:

   X = A'BD + A'C+ BC + CD
   Y = A'C + AC' + C'D'
   Z= C'D' + AC' + A'BD

   Indicate the connections that will be made to program the PLA to implement these equations.

**Ans: Omitted**

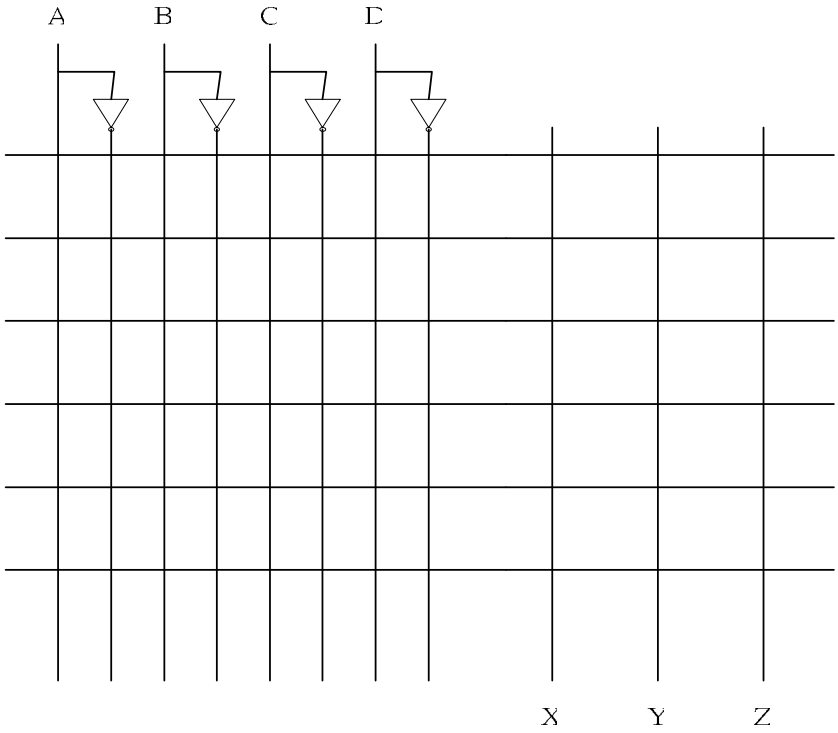



Fig. 4

8. (8%) Show that a 3-input minority gate is a functionally complete set of gate.

**Ans:Omitted**

9. (6%) Implement a 1:4 de-multiplexer by using AND, NOT gates only. Assume D is the data input, Y0~Y3 are the data outputs. S0~S1 are the control lines and when (S0, S1)=(0, 1), D is passed to Y1.

**Ans:Omitted**

10. (6%) Given F = ABC + DE' + A'BE + BD'E. Expand F about the variables C and D.

**Ans:F=C'D'(BE) + C'D(E'+A'BE) + CD'(AB+BE) + CD(AB+E'+A'BE)**

11. (6%) What is the logic function F of the circuit shown in Fig. 5.

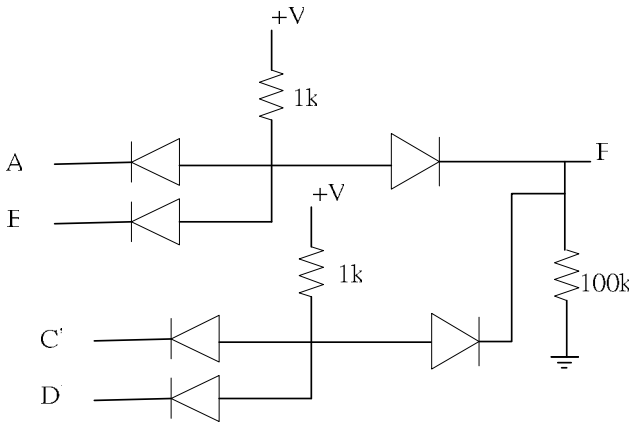



Fig. 5

**Ans:F=AB+C'D"**

12. (8%) Implement an 8:1 multiplexer as Fig. 3 by using two 4:1 multiplexers and one 2:1 multiplexer. Also indicate the control lines ABC's values if we want to pass $I_4$ to the output G.

**Ans:Omitted**

13. (16%)Use the Quine-McCluskey method to find a minimum SOP solution for F(A, B, C, D) = $\sum$ m (1, 3, 4, 5, 6, 7, 10, 12, 13) + $\sum$ d (2, 9, 15). (Note: $m_7$ = A'BCD).

**Ans: BC'+B'CD'+A'D+A'B**