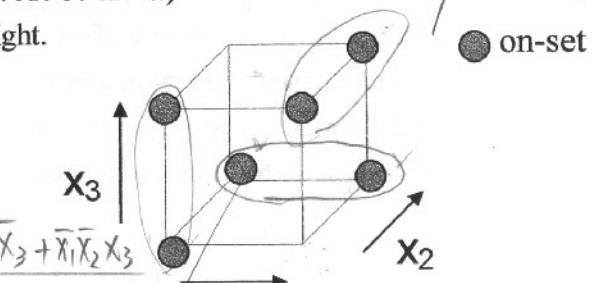
CS 3130 Introduction to Computer-Aided Design of Integrated Circuits

Mid-term Exam (Time allowed: 80 mins.)

1. The on-set of a Boolean function f is shown on the right.
   a. Express f as a sum of minterms. (5 pts.)
   b. List all prime implicants of f. (10 pts.)
   c. Find a minimum cover for f. (5 pts.)



(a) $f = \bar{x}_1\bar{x}_2\bar{x}_3 + x_1\bar{x}_2x_3 + x_1x_2x_3 + x_1x_2\bar{x}_3 + \bar{x}_1x_2\bar{x}_3 + \bar{x}_1\bar{x}_2x_3$

(b)

x_1 \ x_2x_3	00	01	11	10
0	1	1	0	1
1	0	1	1	1

Ans: $\bar{x}_1\bar{x}_2$, $\bar{x}_2x_3$, x_1x_3, x_1x_2, $x_2\bar{x}_3$, $\bar{x}_1\bar{x}_3$

(c) $\{\bar{x}_1\bar{x}_2, x_1x_3, x_2\bar{x}_3\}$

($f = \bar{x}_1\bar{x}_2 + x_1x_3 + x_2\bar{x}_3$)

2. a. What is the difference between implicants and prime implicants? (5 pts.)
   b. People typically divide high-level synthesis into three subtasks, what are they? (6 pts.)
   c. Explain what is a critical path in a combinational circuit. (5 pts.)

(a) implicant：只要其包含的點都在 on-set 或 dc-set 即可

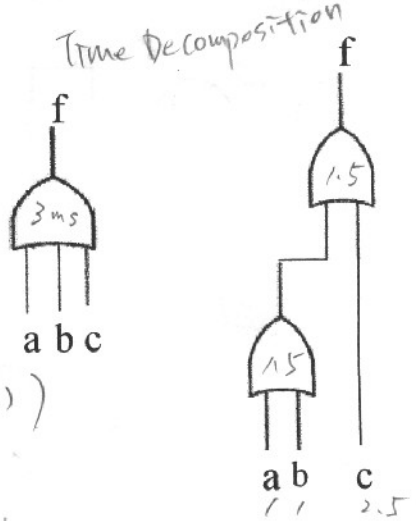
prime implicant：此種 implicant 不可被其他 implicant 包含

(b) Allocation, Scheduling, Assignment

(c) critical path 上的 delay 會 bound 住整體 circuit，即為擁有最大從 input 到 output delay time 的 path.

因 performance

3. Suppose the delay of a 3-input OR gate is 3ms and the delay of a 2-input OR gate is 1.5ms. Give a situation for which the arrival time of output f is better in the right hand circuit than in the left hand circuit below. (10 pts.)



assume input arrival time

$a = 1$ ms

$b = 1$ ms

$c = 2.5$ ms

⇒ 左圖 time(f) $= 3 + \max(a, b, c)$

$= 3 + 2.5 = 5.5$

右圖 time(f) $= 1.5 + \max(c, 1.5 + \max(a, b))$

$= 1.5 + \max(2.5, 1.5 + 1)$

$= 1.5 + 2.5 = 4$ ⇒ better !!

4. a. Which of the following expressions are cube-free? (8 pts.)

(i) abc+de (ii) ab+bc (iii) ab(a+d)(e+d') (iv) (a+bc)(d+e)+f

b. Let x=abcdg+abcd+abce+abcf+ag.

(i) Construct the cube-literal matrix of x. (6 pts.)

(ii) Find all prime rectangles in the cube-literal matrix and give the kernel co-kernel pairs corresponding to the prime rectangles. (10 pts.)

-2

a, Ans: (i), (iv)

(since iii) 中 b可整除, (iii) ab可整除, 非cubefree)

b, (ii) (R, C)

({1,2}, {1,2,3,4}) ⇒ kernel: g+1, co-kernel: abcd

({1,2,3,4}, {1,2,3}) ⇒ kernel: dg+d+e+f, co-kernel: abc

({1,5}, {1,7}) ⇒ kernel: 1+bcd, co-kernel: ag

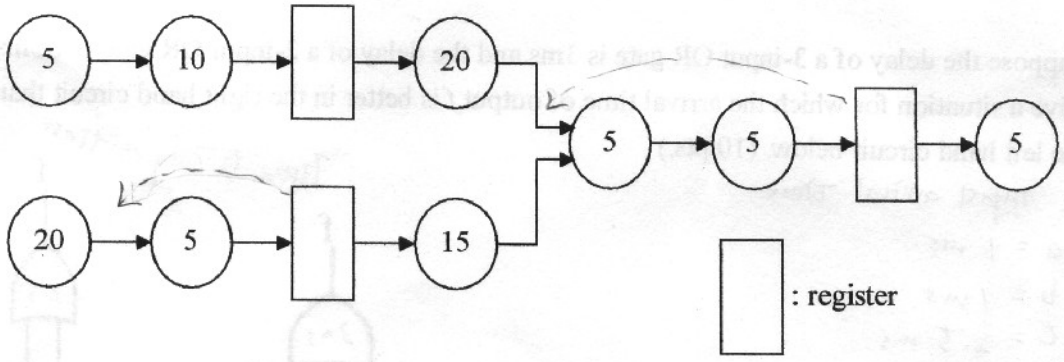
({1,2,3,4,5}, {1}) ⇒ kernel: bcdg+bcd+bce+bcf+g, co-kernel: a

b, i)

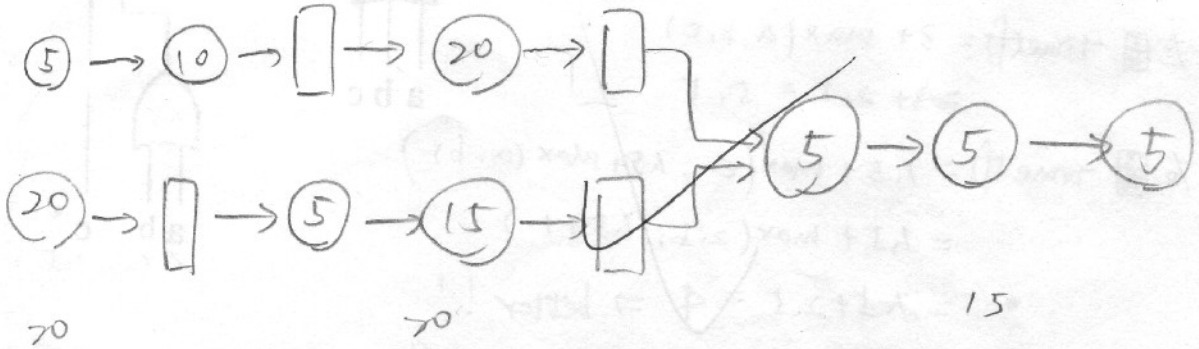
	a	b	c	d	e	f	g
abcdg	1	1	1	1	0	0	(1)
abcd	1	1	1	1	0	0	0
abce	1	1	1	0	1	0	0
abcf	1	1	1	0	0	1	0
ag	(1)	0	0	0	0	0	(1)

kernel	co-kernel: a
1	abce
1	abcf
1	abcdg

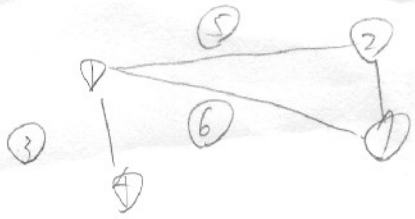
5. Consider the following circuit where the numbers inside a node denotes its delay. Is it possible to reduce the cycle time to 20 by retiming without increasing the number of pipeline stages? Justify your answer (i.e., either give a possible solution or show that it cannot be done). (15 pts.)



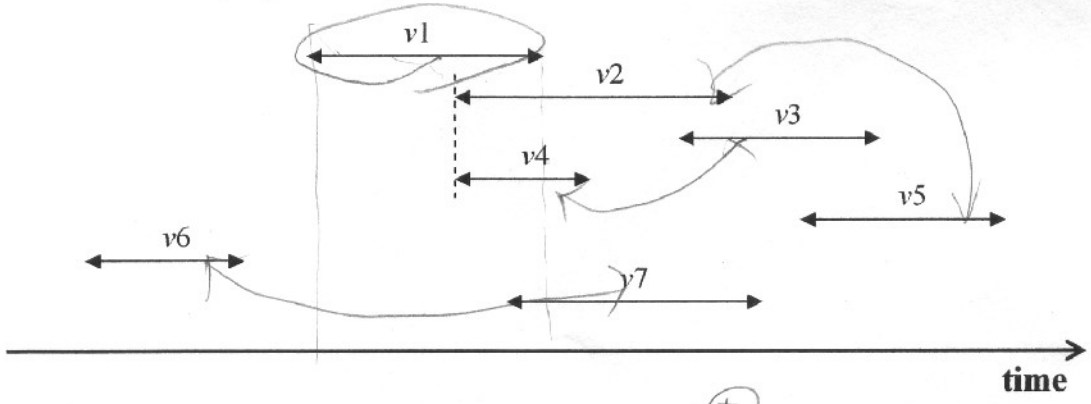
可



此解仍為3個 stage, cycle可降至20. (只是需要多1個 register)



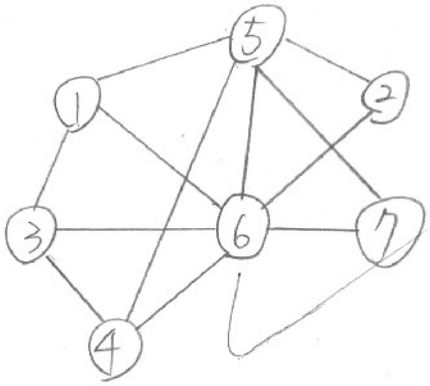
6. Suppose the durations of tasks v1 to v7 are as shown below.
   a. Draw a compatibility graph for v1 to v7. (7 pts.)
   b. Hence find a clique partitioning for v1 to v7 with the minimum number of cliques. (8 pts.)



(a) lifetime 未 cover 的狀況

v1 = v3, v5, v6,
v2 = v5, v6,
v3 = v1, v4, v6,
v4 = v3, v5, v6,
v5 = v1, v2, v4, v6, v7
v6 = v1, v2, v3, v4, v5, v7
v7 = v5, v6

⇒



edge 的兩端代
許 share 同一 register

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(b) 找 complete sub-graph (找3個以上的，2個的有 edge 都可)

1-3-6
1-5-6
2-5-6
3-4-6
4-5-6
5-6-7

} 一定有6，此拆法不見得好 (用其中一個，安便得某2個 task 獨立一組)

∴ 載多 edge 的 5, 6 配載少的 2, 7；剩下的 1, 3, 4 不得已拆2組

∴ {5,2}, {6,7}, {3,4}, {1}

~~{2,5,6}, {7}~~.