Circuits and Electronics (I) Final Examination **Class:** _____

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Choose all the correct answers in a question: (106%, you get 4 (or 5) points if your answer is correct, 0 point if you do not answer, but -1 (-2) point if your answer is incorrect)

3 1. The so-called 28nm process in IC fabrication means the [~~(1)~~ channel length ~~(2)~~ channel width (3) oxide thickness (4) none of the above] of MOS is greater than 28nm, or equal to 28nm.

1,3 2. Which of the following breakdowns is a permanent failure in a MOS? [(1) PN-junction breakdown (2) Punch-through breakdown (3) Oxide breakdown (4) none of the above].

V_{TN} ∝ $\frac{t_{ox}}{\varepsilon_{ox}}$

2 3. To [(1) decrease (2) increase (3) keep unchanged (4) none of the above] the V_{TN} of an enhancement nMOS, Cox has to be decreased.

C_{ox} $\frac{\varepsilon_{ox}}{t_{ox}}$ ↓

4 4. (5%) For an enhancement nMOS. Given V_{TN}=0.8V, kn=0.1mA/V^2, V_{GS} = 1.8V, VA=50V, V_{DS} = 2. What is the output resistance *ro* of the circuit? [(1) 400kΩ (2) 200kΩ (3) 500kΩ (4) none of the above].

$I_D = k_n(\quad) = 0.1mA$ $\quad r_o = \frac{1}{k_n(V_{GS}-V_{TN})}$

$k_n = \frac{1}{2}k_n'\frac{W}{L}$ (100kΩ)

$\frac{1}{k_n(V_{GS}-V_{TN})}$

-1 -2

2 5. (5%) For an enhancement pMOS. Given k_p'=40μA/V^2. Assume the drain current is 0.225mA when V_{GS} = V_{DS} = -3V and the drain current is 1.4mA when V_{GS} = V_{DS} = -4V. What is the W/L ratio? (Hint: V_{TP} <0V) [(1)35.1 (2) 25.1 (3) 15.1 (4) 5.1].

$V_{DS} < V_{GS}-V_{TN}$ at sat

$V_{TP} = -2.33$ $\quad 0.225mA = \frac{1}{2}k_p'\frac{W}{L}[V_{GS}-V_{TN}]^2$

$1.4mA = \frac{1}{2}k_p\frac{W}{L}[V_{GS}-V_{TN}]^2$

$\frac{225}{1400} = \frac{(-3-V_{TN})^2}{(-4-V_{TN})^2}$

$\frac{225}{1400} = \frac{9V_{TN}^2+6V_{TN}+1}{V_{TN}^2+8V_{TN}+16}$

56

$9V_{TN}^2+72V_{TN}+144 = 56V_{TN}^2+336V_{TN}+504$

$47V_{TN}^2+264V_{TN}+360$

1 6. One way to make the threshold voltage of nMOS smaller is to [(1) decrease (2) increase (3) keep unchanged (4) none of the above] the impurity concentration of p-type substrate.

$\frac{-309}{94}$ v $\frac{-219}{94}$ $\frac{-264\pm44.9}{94}$ $\frac{-360}{94}$ v $\frac{-188}{94}$ ÷2

1,2 7. Which of the following statements about current in MOS circuit is correct? [(1) The MOS current will decrease when the temperature increases (2) The source, drain currents of a CMOS inverter circuit are 0 when the inverter is operated at non-switching, or stable state (3) The gate current in a normal MOS is always 0 (4) None of the above.

1,2,4 8. Which of the following factors affects the value of threshold voltage of MOS? [(1) oxide thickness (2) oxide permittivity (3) channel length (4) substrate impurity concentration].

$V_{TP}>0$ for pMOS

3 9. How about the variation of channel thickness (be distinguished from length, width) when negative V_{GS} is applied into the depletion mode pMOS? [(1) not changed (2) decrease (3) increase (4) depend on the relation of V_{GS} and V_{TP}].

4 10. (5%) Consider a depletion pMOS with V_{TP}=2V, kp=0.5mA/V^2. What is the drain current when V_{GS} = 0V, V_{DS} = -1V? [(1) 4mA (2) 3mA (3) 2.5mA (4)1.5mA].

$V_{DS}=-1 > V_{GS}-V_{TP}=-2$ at triode

$I_D = 0.5m\,(2(-2)(-1)-1)$

$= 0.5m\ 3$

$= 1.5m$

1 11. The mechanism that the depletion region around the drain extends completely through the channel to the source terminal is called [(1) punch-through breakdown effect (2) body effect (3) Early effect (4) subthreshold conduction effect].

12. For a MOS circuit as shown in Fig. 1. Given V_{TN}=2V, kn'=60μA/V², and W/L =60.

(a) (5%) What is the value of V_{GS}? (1) 0.62V (2) 1.62V (3) 2.62V (4) 3.62V.

(b) (5%) What is the value of drain current? (1) 1.76mA (2) 2.76mA (3) 3.76mA (4) 4.76mA.

(c) (5%) What is the value of V_{DS}? (1) 11.9V (2) 10.9V (3) 7.9V (4) 6.9V.

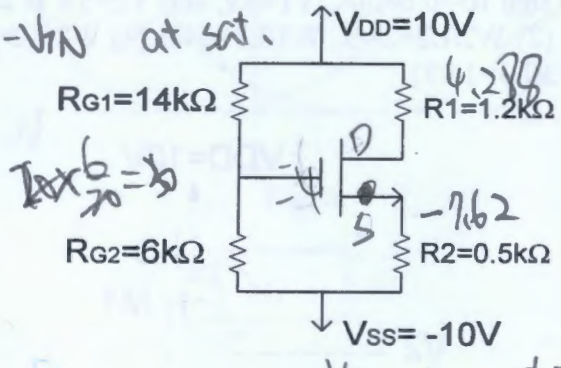


Fig. 1

13. Given an nMOS with V_{TN0}=1V, γ=0.35V^1/2, ϕ_f=0.4V, what is the value of V_{TN} when V_{SB}=2V? [(1) 1.153V (2) 1.229V (3) 1.273V (4) none of the above].

14. What is the boundary equation of triode region and saturation region in nMOS? (1)$I_D = kn \times V_{DS}$ (2) $I_D = kn \times V_{GS}^2$ (3) $I_D = kn \times V_{DS}^2$ (4) $I_D = kn \times (V_{GS} - V_T)^2$

15. (5%) Given an nMOS with V_{TN}= -1V, kn=0.5mA/V², V_{DS}=2V, What is the value of I_{DSS}? (1) 0mA (2) 2mA (3) 8mA (4) none of the above.

2

16. The effect that a change in V_{SB} alters the threshold voltage is called (1) punch-through breakdown effect (2) body effect (3) Early effect (4) subthreshold conduction effect.

4

17. (5%) Consider the circuit in Fig. 2. The transistor parameters are V_{TN}= 1V, $kn'=100\mu A/V^2$ for all three transistors. Which width-to-length ratio required in each transistor such that ID=0.64mA, V1=3V, and V2=5V is correct? [(1) W1/L1 = 4/5, W2/L2=16/5 (2) W2/L2=24/5, W3/L3=64/5 (3) W2/L2=16/5, W3/L3=96/5 (4) W1/L1 = 4/5, W3/L3=16/5]

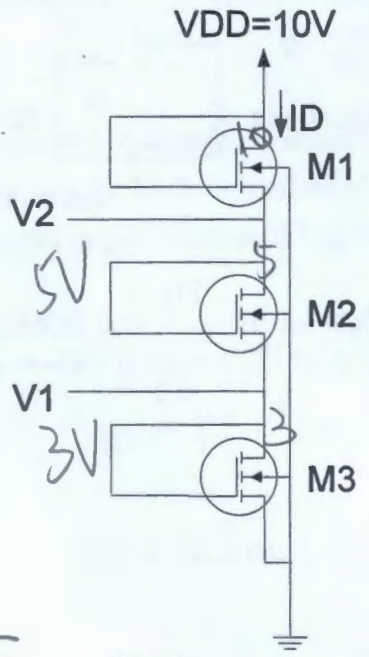


Fig. 2

M_1 $V_{GS}=5$

$V_{DS}=5 > V_{GS}-V_{TN}=4$

$0.64m=50\mu\frac{W}{L}(4)^2$

$\frac{W}{L}=\frac{4}{5}$

M_2 $V_{GS}=2$

$V_{DS}=2 > V_{GS}-V_{TN}=1$

$0.64=50\mu\frac{W}{L}(1)^2$

$\frac{W}{L}=\frac{16}{5}$

M_3 $V_{GS}=3$

$V_{DS}=3$

$0.64=50\mu\frac{W}{L}(2)^2$

$\frac{W}{L}=\frac{16}{5}$

$AB+A'B'$

$(AB)'(A'B')'$

3

18. Given a CMOS logic circuit as shown in Fig. 3 where the pMOS network is not shown explicitly. What does the logic function Fig. 3 implement from Vo? [(1) A+B' (2) (A+B')' (3) (A+ B)(A'+B') (4) (A'B + AB')'].

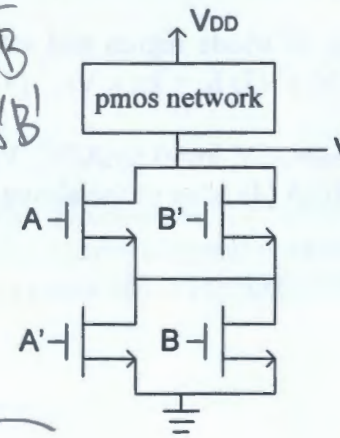


Fig. 3

$A+B$

$A'B'$

10 =1

01 =1

11 =0

00 =0

$(A+B')(A'+B)$

$(A+B')'+(A'+B)'$

$(A'B)+(AB')$

$AB+A'B'$

$(A+B')(A'+B)$

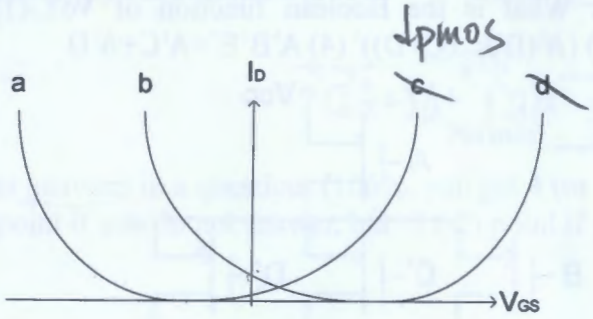
$A'B'+AB$

$(A'B)+(AB')$

$A'B'+AB$

2

19. Which curve does a depletion pMOS probably behave in Fig. 4? (1)a (2)b (3)c (4)d.



pmos

$V_{TP} > 0$

$V_{GS} < V_{TP}$

Fig. 4

20. Consider the circuit in Fig. 5. The transistor parameters are V_{TN1}= -2V, V_{TN2} = 1V, kn_1= 10μA /V², kn_2= 80μA /V². If V_I = 5V,

4 (a) (5%)1 What is the value of Vo? (1) 0.063V (2)0.083V (3) 0.107V (4) 0.127V.

3 (b) (5%)3 What is the value of I_{D1}? (1) 80μA (2) 60μA (3) 40μA (4) 0μA.

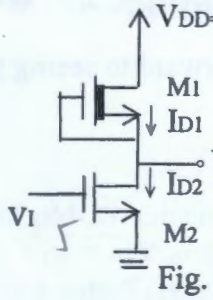


Fig. 5

M_1 $V_{GS}=0 > V_{TN_1}$

$V_{DS} > V_{GS} - V_{N_1} = 2$ at sat

0.127

M_2 $V_{GS}=5$

$V_{DS} < V_{GS} - V_{TN} = 4$ at triode

$$10\mu\left[2\right]^2 = 80\mu\left[(4)V_o - V_o^2\right]$$

$$1 = 2(4V_o - V_o^2)$$

$$V_o^2 - 8V_o + 1 = 0$$

$$\frac{8 \pm \sqrt{64-4}}{2}$$

$$4 \pm \frac{\sqrt{60}}{2}$$

1.746

3.873

4 21. Given a CMOS logic circuit as shown in Fig. 6 where the nMOS network is not shown explicitly. What is the Boolean function of Vo? (1) ABE+C'+D' (2) A(BE+C'+D') (3) (A'(B'E'+C+D))' (4) A'B'E'+A'C+A'D.

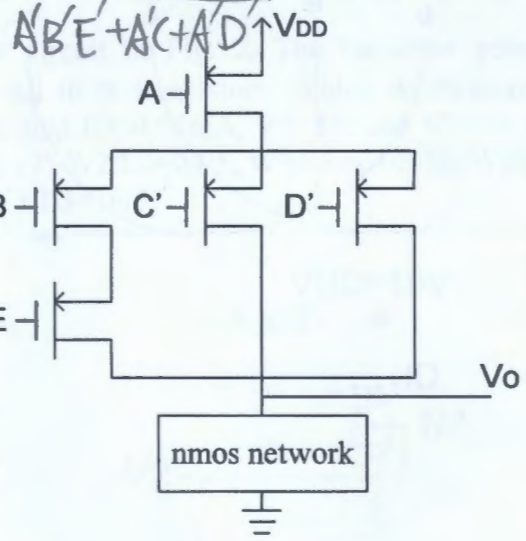


Fig. 6

A(BE+C'+D')

A+(BE)(C')(D')

A'(B'E')+AC+AD

ABC+AC'+AD'

(A+B'+C')(A'+C)(A'+D)

A(B'

ABE+AC'+AD'

(ABE')(AC')'(AD')

Have a Nice Summer Break !!

Thanks for your cooperation, looking forward to seeing you again in the future!