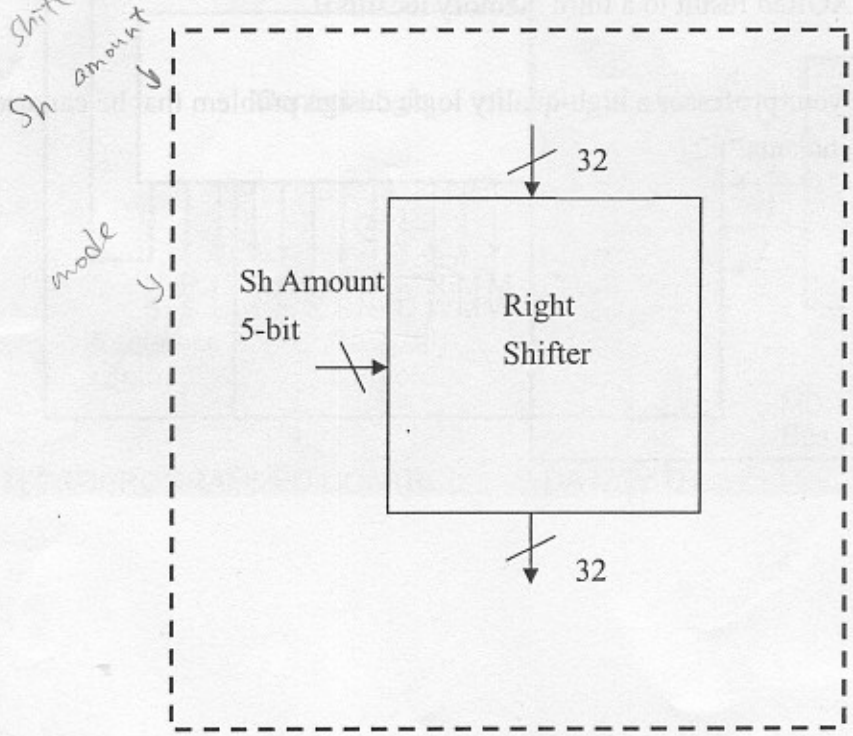
林永隆邏設final

CS2102 Digital Logic Design Final Exam

10:10-11:50am, January 11, 2005

1. (42 pts)
   A. What is a datapath?
   B. What is a register file?
   C. What is microprogrammed control?
   D. What is the difference between RAM and ROM?
   E. What is the difference between SRAM and DRAM?
   F. What is the difference between Algorithmic State Machine and Finite State Machine?

2. (10 pts) Given a circuit that can (zero-fill) shift right a 32-bit input by any number of bits. Add some circuit to it so that it can also perform shift left function. Note that you need a mode selection input in addition to original signals.



3. (15 pts) Design a sequential circuit that counts the sequence of 0, 2, 3, 1, 0, 2, 3, 1, …

4. (10 pts) Design a 512Mbyte memory module using 1Gbit SRAM chips. The chip is organized as 128M X 8-bit and the module should be 256M X 16-bit.

5. (10 pts) A circuit has 5 N-bit registers R1, R2, R3, R4 and R5. Connect them with multiplexors and appropriate control signals so that we can perform 3 set of concurrent register transfers below:

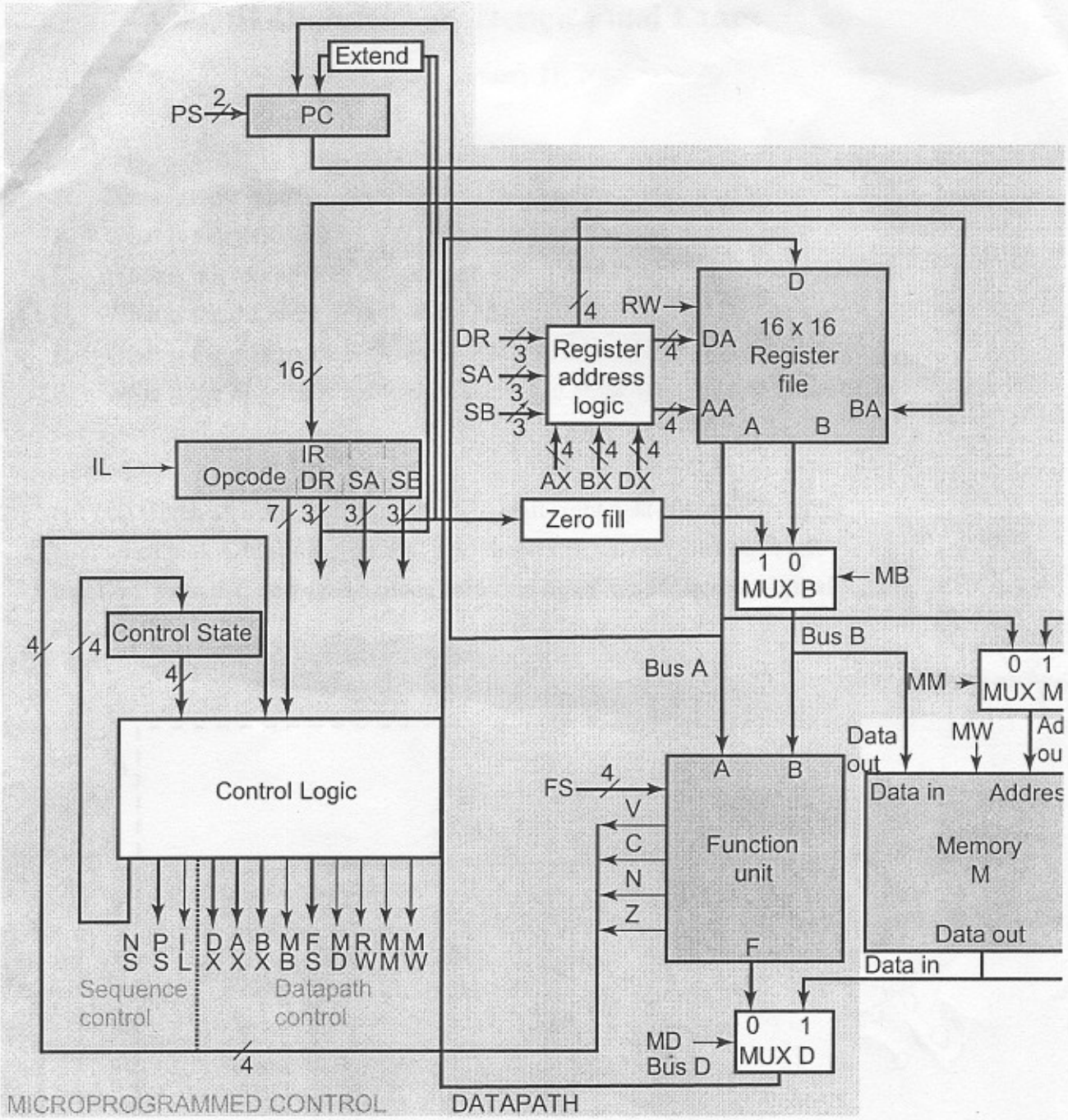
Cond1:	R1 ← R2;	R3 ← R2;	R4 ← R1
Cond2:	R2 ← R4;	R3 ← R4;	R4 ← R3
Cond3:	R5 ← R1;	R1 ← R3;	R2 ← R3

6. (15 pts) Use the multi-cycle computer from Chapter 10 of the text book and copied in the next page. Design an algorithmic state machine so that it can perform the new instruction

M[Ri] ← XOR(M[Rj], M[Rk]), SWAP (M[Rj], M[Rk])

Note that the instruction swaps the contents of two memory locations and stores their bitwise XORed result to a third memory location.

7. (10 pts) Give your professor a high-quality logic design problem that he can use to test future students.


Extend
PS
2
PC
16
IL
IR
Opcode
DR
SA
SB
7
3
3
3
Zero fill
RW
4
DR
SA
SB
3
3
3
Register address logic
4
4
4
4
AX
BX
DX
D
DA
16 x 16 Register file
AA
A
B
BA
1 0
MUX B
MB
Bus B
Bus A
Control State
4
4
4
Control Logic
MM
0 1
MUX M
Data out
MW
Ad
ou
A
B
FS
4
V
C
N
Z
Function unit
F
Data in
Addres
Memory M
Data out
Data in
MD
Bus D
0 1
MUX D
4
N S
P S
I L
D X
A X
B X
M B
F S
M D
R W
M M
M W
Sequence control
Datapath control
MICROPROGRAMMED CONTROL
DATAPATH