Part I: Questions and answers (36%, 6% each)

1. Design a diode logic circuit which implements F = a + bcd.

2. State the reasons about the naming of MOSFETs.

3. What is "Hole Inversion Layer" and how to form it in a MOS?

4. Explain the Early Effect of a MOS.

5. Use diodes to design a Gate input protection circuit for a MOS such that the Gate voltage will be never greater than 10V. Assume the Vr of a diode is 0.6V when forward biased.

6. Use 10 MOSFETs to design a CMOS logic circuit which implements F = (a'+b)c + d'e. Assume the inverted inputs are allowed.

Part II: Choose a correct answer: (74%, 3% each except notified)

1. The so-called 45nm process in IC fabrication means the [(1) channel width (2) channel length (3) oxide thickness (4) none of the above] of MOS is greater than 45nm, or equal to 45nm.

2. The Early Effect is getting more important when the channel length of MOS is [(1) getting smaller (2) getting larger (3) unchanged (4) none of the above].

3. To [(1) decrease (2) increase (3) keep unchanged (4) none of the above] the V_{TN} of enhancement mode nMOS, Cox has to be increased.

4. Which one is not the operation mode in the depletion mode pMOS? [(1) depletion mode (2) enhancement mode (3) linear mode (4) none of the above]

5. One way to make the threshold voltage of an enhancement nMOS smaller is to [(1) decrease (2) increase (3) keep unchanged (4) none of the above] the impurity concentration of p-type substrate.

6. The threshold voltage of an enhancement nMOS will [(1) increase (2) decrease (3) keep unchanged (4) none of the above] when the temperature increases.

7. (5%) Given an input waveform and a diode circuit as shown in Fig. 1 and Fig. 2, respectively. Determine the output waveform at Vo. (Assume the diode is an ideal diode, forward -> ON, reverse -> OFF).

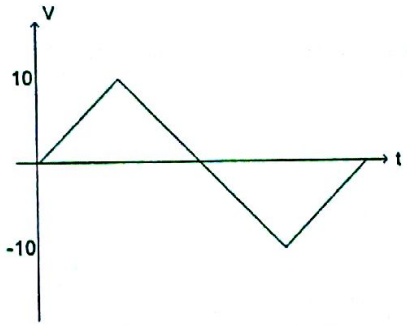


Fig. 1 Input waveform

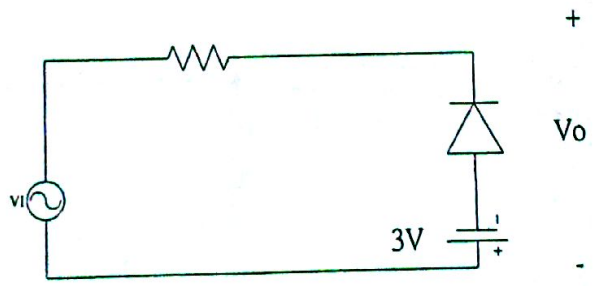
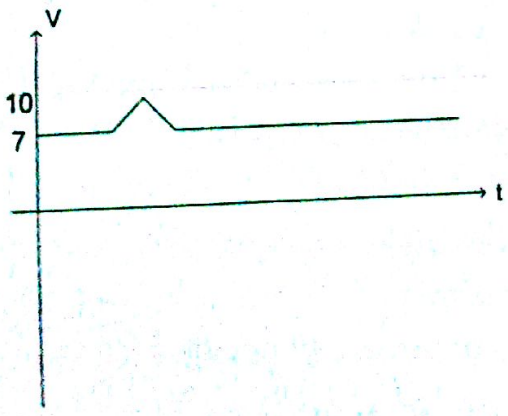
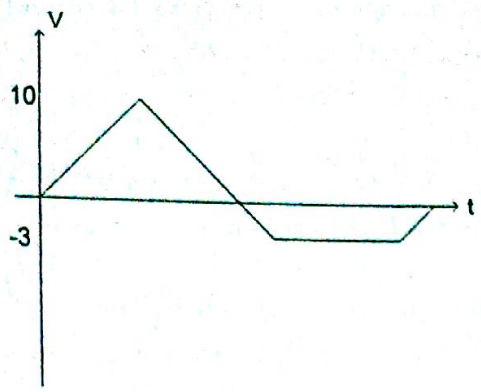


Fig. 2 Diode circuit

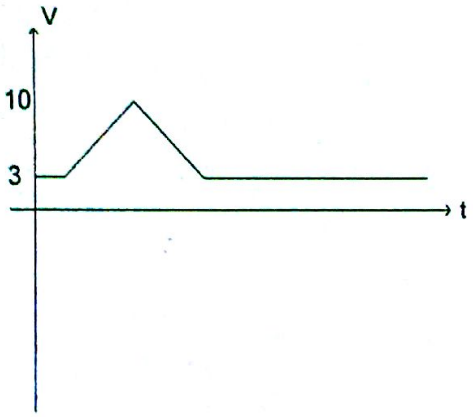
(1)



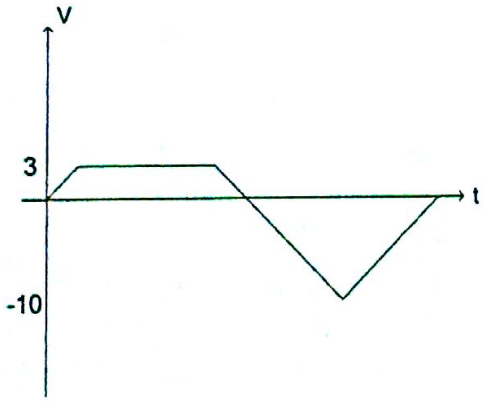
(2)



(3)



(4)



8. For the circuit in Fig. 3. (Assume the diodes have Vr=0.6V when forward biased)
   (a)What is the value of ID? [(1) 0mA (2) 1mA (3) 2mA (4) None of the above]
   (b)What is the value of Vo? [(1) -7.5V (2) -5V (3) 4.4 V (4) None of the above]

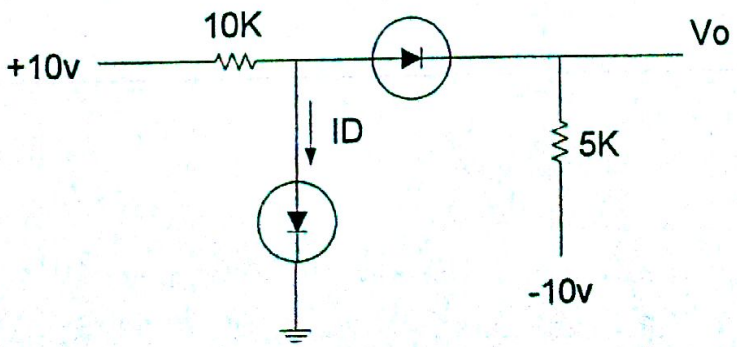


Fig. 3

9. The mechanism that the depletion region around the drain terminal extends completely through the channel to the source terminal is called [(1) punch-through breakdown effect (2) body effect (3) Early effect (4) subthreshold conduction effect].

10. Given a pMOS with V_{TP}= 2V, kp=0.5mA/V^2 at Saturation region, what is the value of I_{DSS}? [(1) 2mA (2) 4.5mA (3) 8mA (4) none of the above]

11. (5%) Given an input waveform and an output waveform as shown in Fig. 4 and Fig. 5, respectively. Determine the diode circuit. (Assume the diode is an ideal diode, forward -> ON, reverse -> OFF).

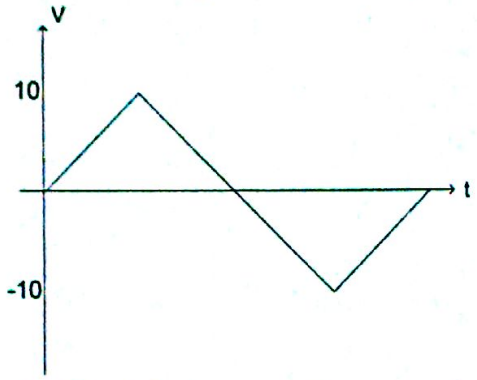


Fig. 4 Input waveform

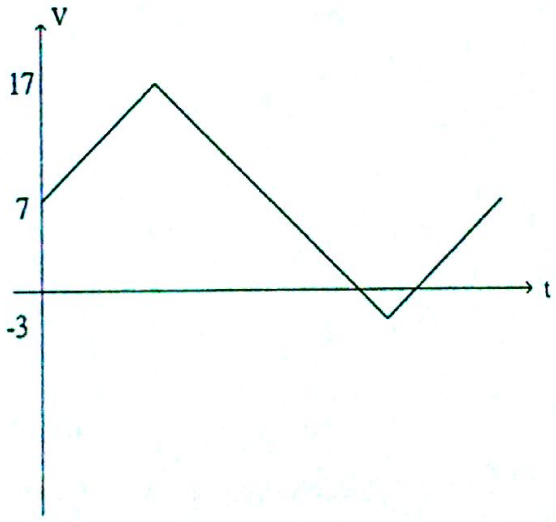
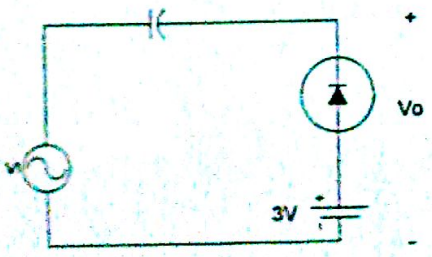
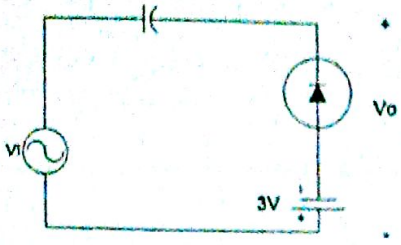


Fig. 5 Output waveform

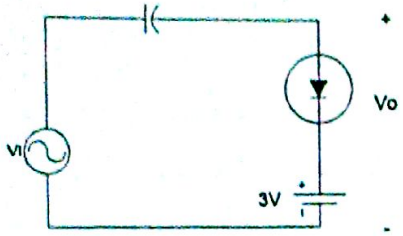
(1)



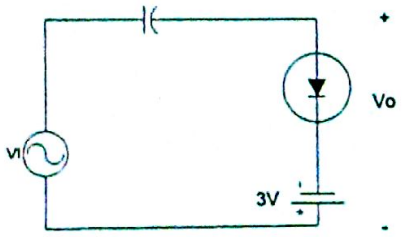
(2)



(3)



(4)



12. Consider the circuit in Fig. 6. The transistor parameters are V_{TN}= 1V, kn'=50μA/V^2.
    (a) Design the width-to-length ratio required in M1 transistor such that ID=0.64mA, V1=2V, and V2=5V. [(1) 4/5 (2) 8/5 (3) 16/5 (4) 32/5]
    (b) Design the width-to-length ratio required in M3 transistor such that ID=0.64mA, V1=2V, and V2=5V. [(1) 16/5 (2) 32/5 (3) 64/5 (4) 128/5]

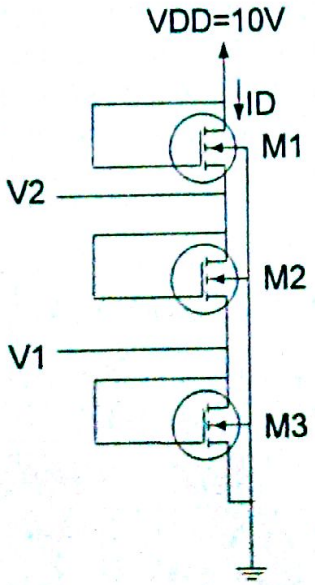


Fig. 6

13. Consider an enhancement nMOS. Given V_{TN}= 1V, kn=0.1mA/V², V_{GS}=2V, VA=50V, and V_{DS}=3V.
    (a) Determine the output resistance (ro). [(1)125kΩ (2)166.7kΩ (3)500kΩ (4)None of the above]
    (b) Determine the current I_D. [(1)0.102mA (2)0.106mA (3)0.108mA (4)0.11mA]

14. Which of the following does not affect the value of threshold voltage of MOS? [(1) channel length (2) oxide permittivity (3) oxide thickness (4) substrate impurity concentration]

15. (5%) Consider the circuit in Fig. 7. The transistor parameters are V_{TN}= 2V, kn'= 20μA /V², L= 10μm, W = 400 μm. Design Rs such that I_D=0.4mA. [(1) 2kΩ (2) 5kΩ (3) 7.5kΩ (4) None of the above]

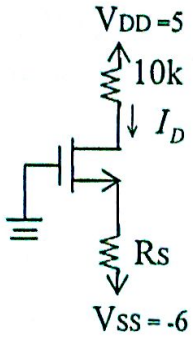


Fig. 7

16. For a MOS circuit as shown in Fig. 8. Given V_{TN}= -1V, kn'=20uA/V².
    (a) Determine the maximal value of R_D such that the MOS is at Saturation region and I_D=50μA. [(1) 20 kΩ (2) 40 kΩ (3) 60 kΩ (4) 80 kΩ]
    (b) Determine the minimal value of R_D such that the MOS is at Saturation region and I_D=50μA. [(1) 30 kΩ ( ) 40 kΩ ( ) 50 kΩ (4) None of the above]

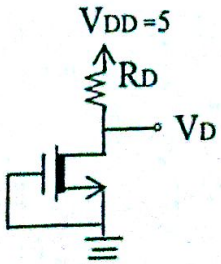


Fig. 8

17. What is the boundary equation between triode region and saturation region in nMOS? [(1)$I_D = kn \times V_{DS}$ (2) $I_D = kn \times (V_{GS} - V_{TN})^2$ (3) $I_D = kn \times V_{DS}^2$ (4) $I_D = kn \times V_{GS}^2$]

18. (5%) Given a CMOS logic circuit as shown in Fig. 9 where the nMOS network is not shown explicitly. What is the Boolean function of Vo? (A' means the complement of A) (1) A'B'E'+C'+D'F' (2) A'B'E'+A'C'+A'D'F' (3) (A(BE+C+DF))' (4) A(BE+C+DF).

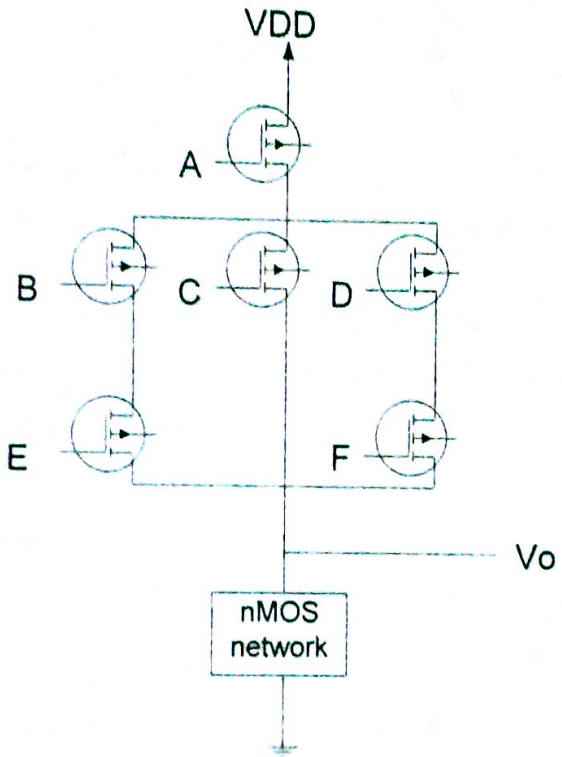


Fig. 9

Enjoy Your Summer Break !!

Thanks for your cooperation, looking forward to seeing you again in the future!