CS2102 01 Digital Logic Design Midterm 2 (10:10am-12:00pm, Dec 9th)

Name: _____ **ID:** _____ **(Return this with your answer sheet)**

Truth or False (24%):

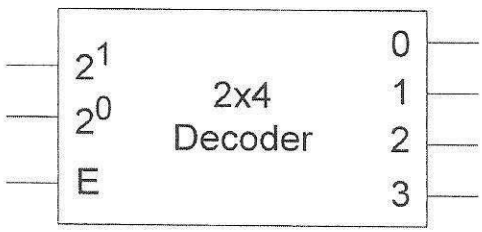
(Write down T or F. You don't need to give the reason.)

1. _____ Combinational circuits are time-invariant. That is, their outputs are determined directly and only from the present input combination.
2. _____ For the n-bit signed-2's complement addition ($\{C_n, S_{n-1}, S_{n-2}, \dots, S_1, S_0\} = \{A_{n-1}, A_{n-2}, \dots, A_1, A_0\} + \{B_{n-1}, B_{n-2}, \dots, B_1, B_0\}$), overflow occurs when the carry signals $C_{n-1} \oplus C_{n-2} = 1$.
3. _____ The outputs of sequential circuits are determined from the present state of the memory cells only.
4. _____ A decoder with enable input is also called demultiplier.
5. _____ Multiplexers can be implemented by using three-state gates.
6. _____ The state table can be uniquely derived from the state diagram.
7. _____ Latch, which is an edge-triggered device, is an asynchronous sequential circuit as its state changes whenever the inputs change.
8. _____ Mealy model of finite state machine is defined as that outputs are functions of the present state only.

Answer the following questions: (76%)

(Write down your intermediate results. Do not give the final answer only.)

1. (4%) **[Carry lookahead]** Derive the two-level Boolean expression for the carry C_4 in the carry lookahead generator. You should start with the definition of Carry Generate and Carry Propagate.
2. (8%) **[Decoder]**
   (a) (4%) Draw the logic diagram and the truth table of the 2x4 (2-to-4-line) decoder using NAND gates with complemented outputs and active-low enable input. Also list the truth table. (Hint: the inputs are A, B, E; the outputs are D_0, D_1, D_2, and D_3.)
   (b) (4%) Using the 2x4 decoders in (a) as basic blocks, construct the 4x16 decoder. You should label all the inputs $\{A_3A_2A_1A_0\}$ and E, and outputs $\{D_0D_1D_2 \dots D_{15}\}$ on the block diagram.
   Hint: The block diagram of the 2x4 decoder:



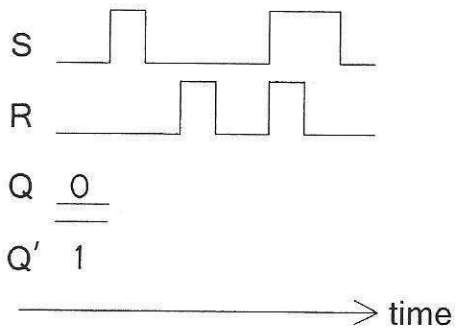
3. (8%) **[Multiplexer]** Implement the Boolean function $F(A, B, C, D) = \prod(4, 7, 12, 15)$ with a multiplexer.

4. (7%) **[Decoder]** Using a decoder and an external gate to design the combinational circuit defined by the Boolean function $F = xy + y'z' + xz$. You should minimize the fan-ins of the external gate.
5. (12%) **[Combinational design]** Design a game box with two players for Rock-Paper-Scissors game (you know the game well). Rock beats scissors; paper beats rock; and scissors beat paper. Each player enters a two-bit vector to indicate rock, paper, or scissors. For two players, A and B, there are four bits of inputs $\{A_1A_0B_1B_0\}$. The two-bit output $\{Y_1Y_0\}$ identifies who the winner is between A and B, or a tie (i.e., no one wins). The coding of input and output is defined as follows:

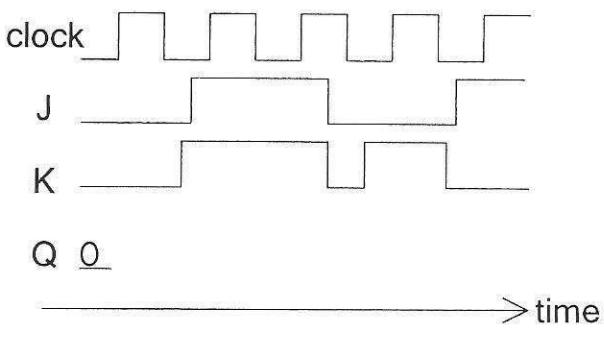
	Inputs $\{A_1A_0\}$ or $\{B_1B_0\}$
Rock	01
Paper	10
Scissors	11

	Outputs $\{Y_1Y_0\}$
A wins	10
B wins	01
Tie	00

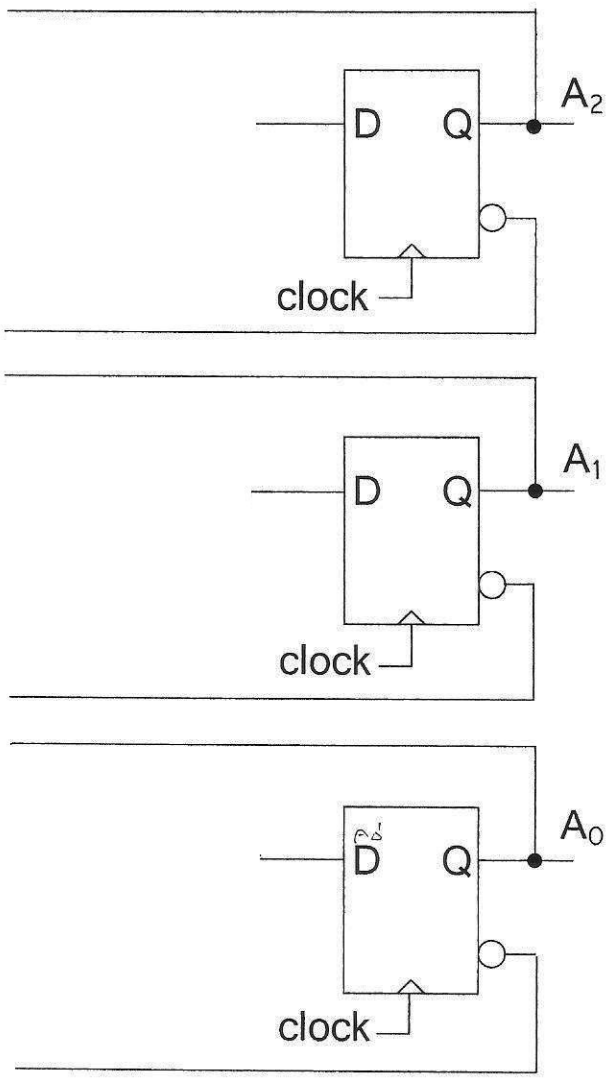
   (a) (5%) List the truth table of the game box. (Hint: You may use don't-cares if any.)
   (b) (5%) List the simplified sum-of-products function.
   (c) (2%) Draw the logic diagram of the game box by using NAND gates only.
6. (15%) **[Latch and Flip-Flop]**
   (a) (5%) Complete the following timing diagram for an SR latch with NOR gates. Assume Q begins at 0 (Q' begins at 1). Ignore the delay of the SR latch (i.e., the delay of the two NOR gates is zero).



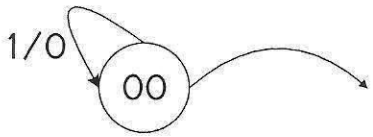
   (b) (5%) Show the characteristic equation of a T flip-flop (i.e., $Q(t+1) =?$). Construct a T flip-flop using a D flip-flop and a two-to-one-line multiplexer.
   (c) (5%) Complete the following timing diagram for a positive-edge-triggered JK flip-flop. Assume Q begins at 0. Ignore the delay of the JK flip-flop.



7. (10%) **[Analysis of Sequential Circuit]** Assume that initially the state of the following circuit is all zero {000} after direct reset (the reset signals are omitted for the simplicity). The output is $\{A_2, A_1, A_0\}$, the same as the state.
   (a) (4%) Derive the state equations of $A_2(t+1)$, $A_1(t+1)$ and $A_0(t+1)$.
   (b) (4%) Derive its state table and state diagram.
   (c) (2%) Is it a Mealy machine or Moore machine?



8. (12%) **[Sequential Design]** Design a sequential counter with two D flip-flops A and B, one input Hold, and one output Carry_Out. When Hold=1, the state of the circuit remains the same. When Hold=0, the circuit goes through the state transitions from 00 to 01, to 10, to 11, then back to 00, and repeats. The output Carry_Out=1 only when the state transits from 11 to 00
   (a) (5%) Complete the state diagram.



(b) (2%) Is it a Mealy machine or Moore machine?

(c) (5%) Simplify the input equation of each D flip-flop using the K-map method and draw the circuit.

Good luck and happy examination!!

If you have too much time left, there is still a joke for you:

A professor experienced a serious headache in the classroom. And he went to see a doctor. After medical examination, doctor told him:

"Mr. professor, after my detailed examination, we found out that your brain has two parts: one is left, and the other is right."

"Your left brain has nothing right. And your right brain has nothing left!"