CS2102 02 Digital Logic Design Midterm 2 (1:20pm-3:10pm, May 11th)

Name: _____ **ID:** _____ **(Return this with your answer sheet)**

Truth or False (33%):

(Write down T or F on your answer sheet! You don't need to give the reason.)

1. T Connecting the output of an n: 2^n decoder to the input of a 2^n: n encoder, the n-bit output of the encoder will equal to the n-bit input of the decoder.
2. F Priority encoder converts the one-hot output of the arbiter to its binary value. Therefore, for the policy of finding the least significant 1, the priority encoder will output '3' when its input is 01011000.
3. F Arbitrary n-input combinational logic function can be implemented using a one-hot-select 2^{n-1}:1 MUX.
4. F For a 3-bit vector $\{x, y, z\}$, the even parity P can be generated by $P = x \oplus y \oplus z$. To check if there is an error, one can use $C = P \oplus x \oplus y \oplus z$, where $C = 1$ indicates even number of errors. (Hint: $\oplus$ is an XOR operator.)
5. T An n-bit 2's complement number can represent 2^n different numbers, from -2^{n-1} to $2^{n-1} - 1$.
6. T For the n-bit signed 2's complement addition ($\{C_n, S_{n-1}, S_{n-2}, \cdots, S_1, S_0\} = \{A_{n-1}, A_{n-2}, \cdots, A_1, A_0\} + \{B_{n-1}, B_{n-2}, \cdots, B_1, B_0\} + C_0$), overflow occurs when the carry signals $C_{n-1} \oplus C_{n-2} = 1$.
7. F When implementing the magnitude comparator of two positive integers with binary representation, you can have iterative design to compare the two numbers bit by bit iteratively, only from LSB to MSB, but not from MSB to LSB.
8. T The result of multiplying an n-bit number and an m-bit number will be (at most) an $(n + m)$-bit number.
9. F The controlling value of NAND gate and OR gate is the same.
10. T The setup time of a flip-flop defines the time that data input must be maintained at a constant value prior to the specific positive (rising) clock edge.
11. T In a Moore machine, the outputs depend on the present state only; the next-state combinational logic, on the other hand, is a function of both the present state and primary inputs.

Answer the following questions: (72%)

(Write down your intermediate results with the final answer to get the scores.)

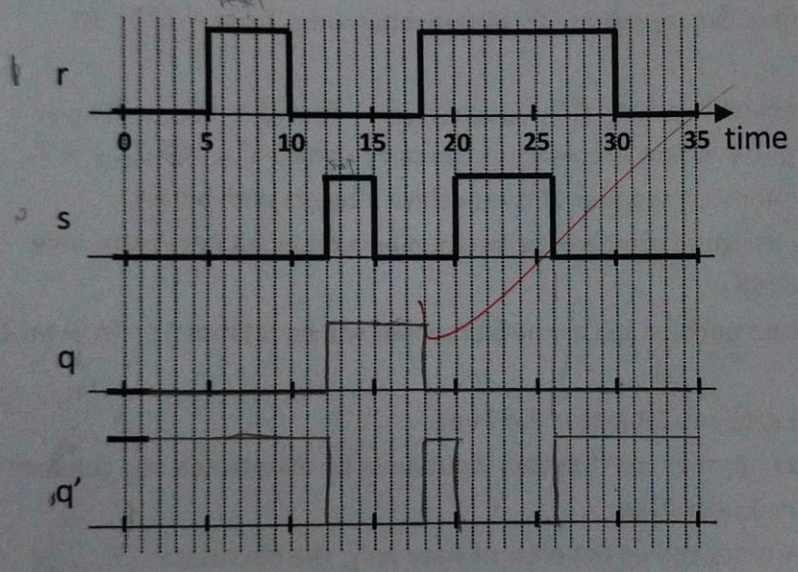
1. (8%) **[Conversion]** Convert $(35.71875)_{10}$ to binary representation, then to hexadecimal representation. You should show the intermediate results by using the procedures in the lecture.
2. (8%) **[2's Complement]** Show the detailed procedure of the following additions with 7-bit binary numbers in 2's complement representation. You should also translate the result to decimal, and indicate how you determine if there is an overflow in **hardware's viewpoint**.
   (a) (4%) (+50) – (–13);
   (b) (4%) (–26) – (+50).
3. (16%) **[Combinational Block]** Design a 3-input function $f(a_2, a_1, a_0) = \sum_m(0, 1, 2, 5, 6, 7)$.

(a) (8%) **[MUX]** Use three 2:1 MUXes to design the circuit. Draw the logic diagram given that the select inputs of the 2:1 MUXes are either a_2 or a_1.

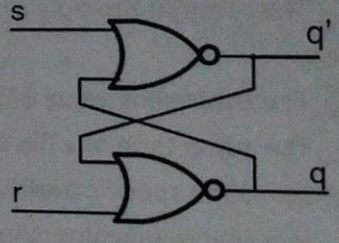
(b) (8%) **[Decoder]** Use a 2:4 decoder, AND gates and one NOR gate to design the circuit. The decoder's input is $\{a_2, a_1\}$. Hint: Use the 2:4 decoder with AND gates to build up the 3:8 decoder. Then use the 3:8 decoder and one NOR gate to implement the function. You may skip the unused outputs of the 3:8 decoder for the simplicity.

4. (5%) For the n-bit addition $(\{C_n, S_{n-1}, S_{n-2}, \cdots, S_1, S_0\} = \{A_{n-1}, A_{n-2}, \cdots, A_1, A_0\} + \{B_{n-1}, B_{n-2}, \cdots, B_1, B_0\} + C_0)$, consider the carry lookahead adder (CLA) with carry-propagate $P_i = A_i \oplus B_i$ and carry-generate $G_i = A_i B_i$. Derive the Boolean function for $C_3 = f(P_2, G_2, P_1, G_1, P_0, G_0, C_0)$ in sum-of products form. (The Boolean function only depend on the carry-in C_0, carry-propagate P_i and carry-generate G_i.) Hint: The carry $C_{i+1} = G_i \vee P_i C_i$.

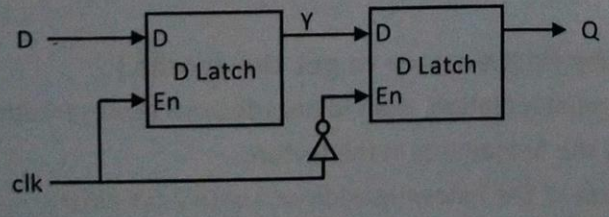
5. (5%) **[Latch]** Complete the following timing diagram for the RS latch with two NOR gates. Assume $q = 0$ ($q' = 1$) initially. Assume the timing is ideal without any delay (that is, the delay of all the gates is zero). There is also the gate-level logic diagram of RS latch for your reference. You may draw the answer directly on the problem sheet.

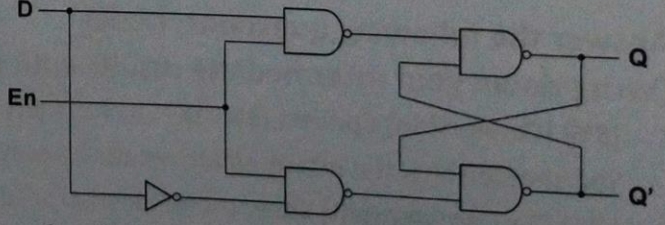


r=0 s=0 no change
r=1 s=0 reset
r=1 s=1 invalid.
r=0 s=1 set

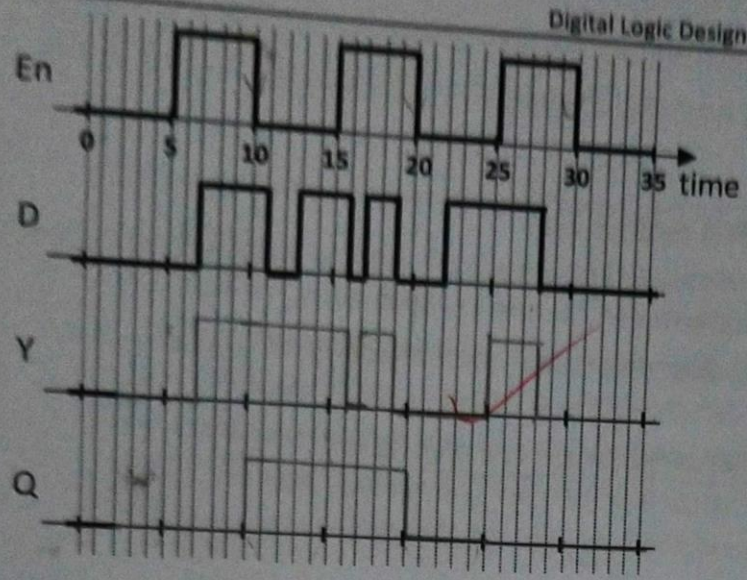


6. (10%) **[DFF]** Consider the following D flip-flop of two gated D latches with NAND gates. There is also the gate-level logic diagram of D latch for your reference.





Complete the following timing diagram. Assume $Y = Q = 0$ at time 0, and there is no delay of the circuit. You may draw the answer directly on the problem sheet.

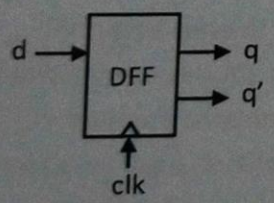


7. (20%) **[sequential design]** Design a binary up-down counter. The counter has three 1-bit inputs (**`dir`**, **`rst_n`** and **`clk`**). The outputs include the 2-bit **`out`** and a 1-bit carry out **`co`**. Initially the output is 00 after the reset. When **`dir==1`**, the counter up-counts from 00 to 01, to 10, to 11, then back to 00, and repeats. The **`co`** is equal to 1 when the **`out`** transits from 11 to 00, otherwise it is 0. When **`dir==0`**, the counter down-counts from 00 to 11, to 10 to 01, back to 00, and repeats. The **`co`** is equal to 1 when the **`out`** transits from 00 to 11, otherwise it is 0.

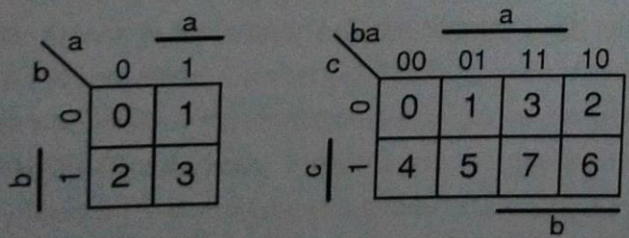
   (a) (5%) Draw the state diagram of this finite-state machine (FSM) design. (The state $\{s_1, s_0\}$ can be the same as the output **`out`**.)

   (b) (5%) Draw the state table.

   (c) (10%) Derive the logic to compute the next-state and output using K-map. Draw the gate-level diagram of this counter. You may use AND, NAND, OR, NOR, INV, XOR, or XNOR gates.
   Hint: A three-input XOR function is $x \oplus y \oplus z = \bar{x}\,\bar{y}\,z \vee \bar{x}\,y\,\bar{z} \vee x\,\bar{y}\,\bar{z} \vee x\,y\,z$.
   The block diagram of DFF is also shown in the following. The reset is skipped for the simplicity.



For those who forgot what K-map is, here is also a hint for you:



Good Luck!!

If you have too much time left, there is still a joke for you:

A professor experienced a serious headache in the classroom. And he went to see a doctor. After medical examination, doctor told him:

"Mr. professor, after my detailed examination, we found out that your brain has two parts: one is left, and the other is right."

"Your left brain has nothing right. And your right brain has nothing left!"