Subject: Close-book mid-term exam of CS3120-02, November 21, 2006

Seven Hints and Rules for a Fair Examination:

A. We suggest that everyone avoid using pencils. If you insist in using a pencil, that is OK.
B. Close books and turn off all personal electronics including the cell phone's sound and vibration.
C. If you feel some number/word/sentence in one of this exam's ten questions is wrong, you may write down the wrong on the answer sheet to earn extra credits. No penalty if the wrong pointed out by you turns out to be correct.
D. Please raise your hand with patience when you want to talk to the teacher or a TA.
E. Please try to understand and answer the questions properly.
F. Please express your "thought process" succinctly to avoid jump-to-conclusion answer; please make each of your final answers stands out clearly and explicitly to avoid grading errors.
G. Between 3:20PM and 5:00PM, you are welcome and allowed to talk to the teaching assistants. No chatting or any other form of communications between classmates will be allowed. All kinds of hand-held calculator or PDA are allowed and welcome. However, notebook computers or any other non-hand-held computers are not allowed.

1. In Prof. Uyemura's VLSI book, Chapter Four, he states the following four sentences:
Dry etching techniques do not etch copper. To get around this problem, we use the Damascene process based on the method used in ancient times to inlay gold or silver into an iron sword. In this technique, the copper pattern is first etched into a silicon dioxide layer; copper is then deposited [using, for example electroplating] on the surface. To avoid the etching problem, we subject the wafer to a chemical-mechanical polishing (CMP) step that planarizes the surface and removes copper not in an oxide trench.

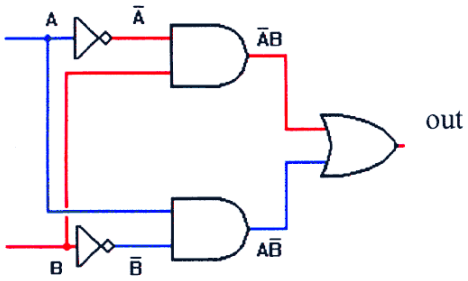
(a) Please use Chinese language to describe this sentence: "**Dry etching techniques do not etch copper.**"
(b) In your answer sheet, please draw a picture showing the result of this step: "**The copper pattern is first etched into a silicon dioxide layer.**"
(c) In your answer sheet, please modify the picture in (b) above showing the result of this step: "**Copper is then deposited [using, for example electroplating] on the surface.**"
(d) In your answer sheet, please modify the picture in (c) above showing the result of this step: "**We subject the wafer to a chemical-mechanical polishing (CMP) step that planarizes the surface and removes copper not in an oxide trench.**"

(Please note: It is not necessary for your drawn pictures in the above to be exactly the same as the picture in the textbook to get the full credits.)

2. The following is a truth table example.

A	B	out
0	0	1
0	1	0
1	0	0
1	1	1

Examining the above table and the following drawing,



(a) Is the above drawing a logic diagram, a circuit, or a layout?

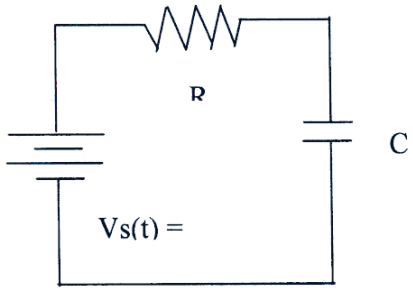
(b) The above drawing can be made by using nMOS and pMOS transistors. How many MOS transistors are needed to make the above drawing's function? Please explain why.

(c) How many inputs are there in the above drawing?

(d) How many outputs are there in the above drawing?

(e) Can the above truth table in this page be used to describe the above drawing's function? If yes, why? If the above truth table cannot describe the above drawing's function, please provide the correct truth table.

3. A simple electric circuit is depicted in the following:

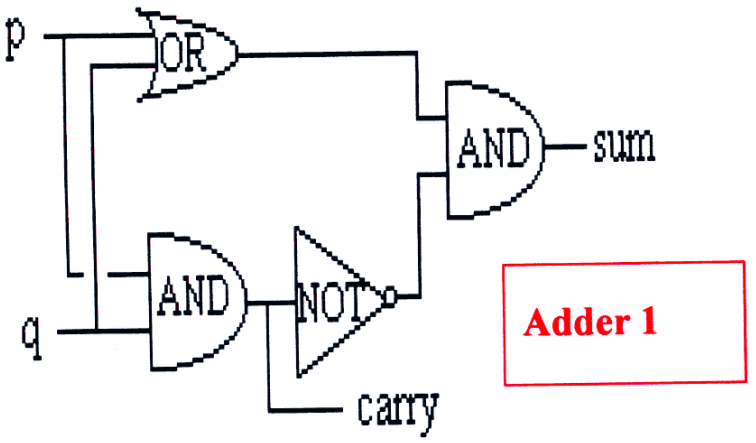


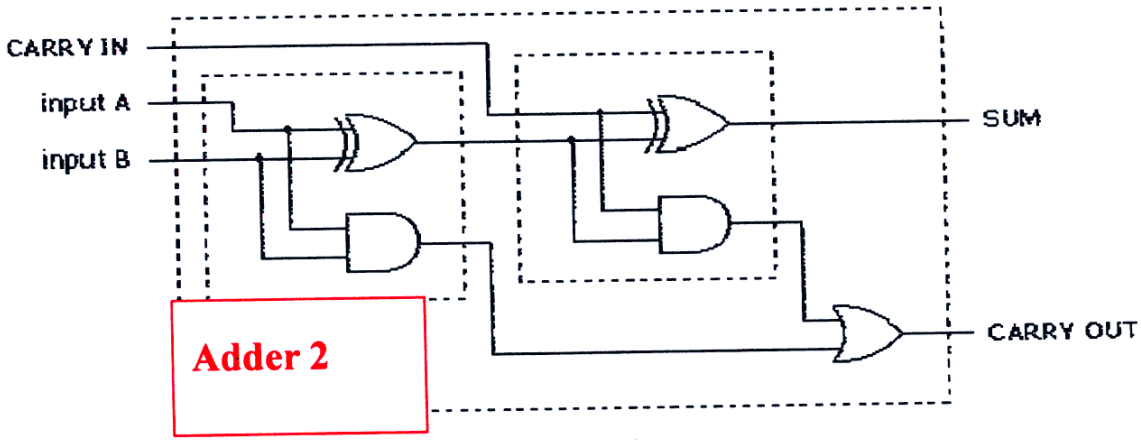
(a) Vs(t) is the supply voltage source and the voltage of the source is a positive constant K volt. $v_c(t)$ is the voltage across the above capacitor "C" and i(t) is the current flowing through the above resistor "R". Please provide a correct ordinary differential equation (ODE) that can model the above circuit by using $v_c(t)$ as the dependent variable. You may use the following four circuit concepts: (i) KVL, (ii) KCL, (iii) $Q(t) = C * v_c(t)$, and (iv) $i(t) = dQ(t)/dt$.

(b) If $v_c(t=0)=0$ for the above ODE. $Vs(t)=K=1$ volt for all t, please analytically solve the above ODE to achieve an explicit solution that describes v_c as function of t.

(c) If the R value is 400 Ohm and the C value is 0.005 Farad, please calculate the value of $v_c(t)$ when t is 2.0 second.

4. Two adders are shown in the following:

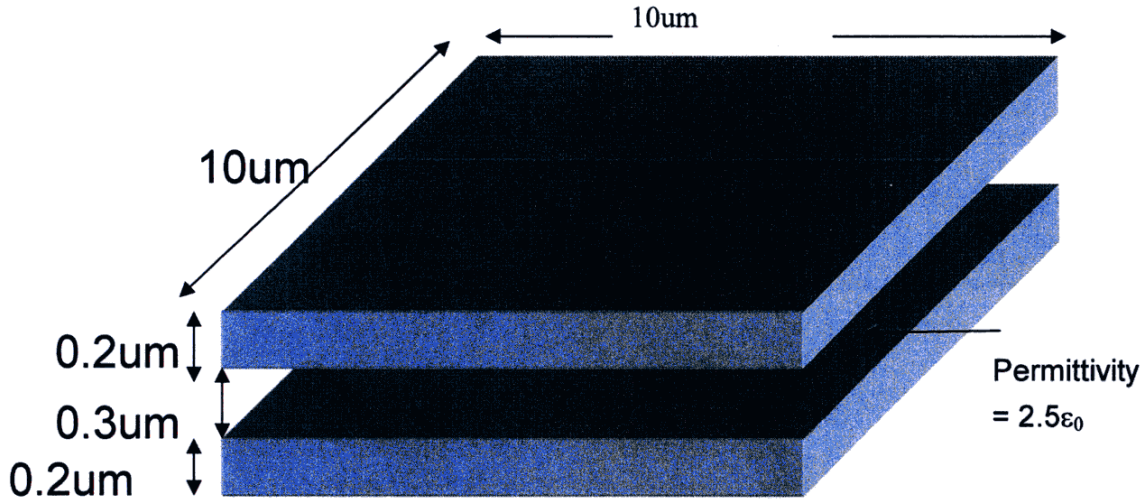




(a) Please redraw one of the above two adders in your answer sheet and use a truth table to prove that it is a half adder.

(b) Please redraw one of the above two adders in your answer sheet and use a truth table to prove it to be a full adder.

5. Examining the following capacitor with two parallel 0.2umX10umX10um metal plates insulated by an insulator layer with thickness 0.3um and permittivity $2.5\varepsilon_0$, where ε_0 is 8.854 $\times$ 10^{-12} F/m and is the permittivity of free space. Please calculate the following's capacitance value.



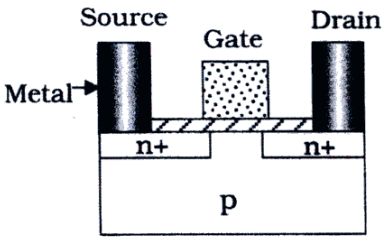
6. We have discussed this equation [1]: $\mathbf{I = \mu_n C_{ox} (W/L) (V_G - V_{Tn}) V}$

Assume μ_n is 500 (unit being cm^2/V-sec) and $V_G - V_{Tn}$ is (3.0 − 0.7) Volt.

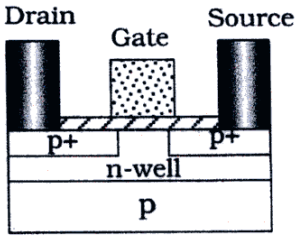
(a) Use the above equation [1] and the capacitance calculation method in Question 5 above to find the C_{ox} and the NMOS resistance if W = 10um and L = 0.5um, and t_{ox} = 10nm.

(b) Find the C_{ox} and the NMOS resistance again if W = 22um and L = 0.5um, and t_{ox} = 10nm.

7. (a) When we apply a ground or negative voltage on the two gates of the following two drawings, which of the two MOSFETs will be turned on?



(a) nFET cross-section

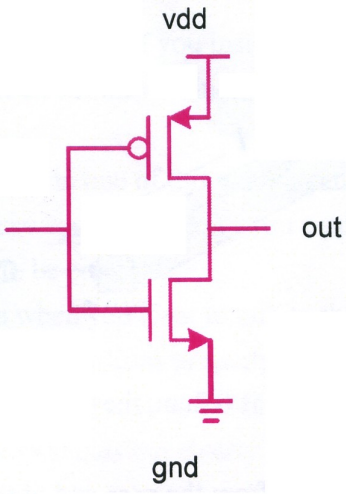


(b) pFET cross-section

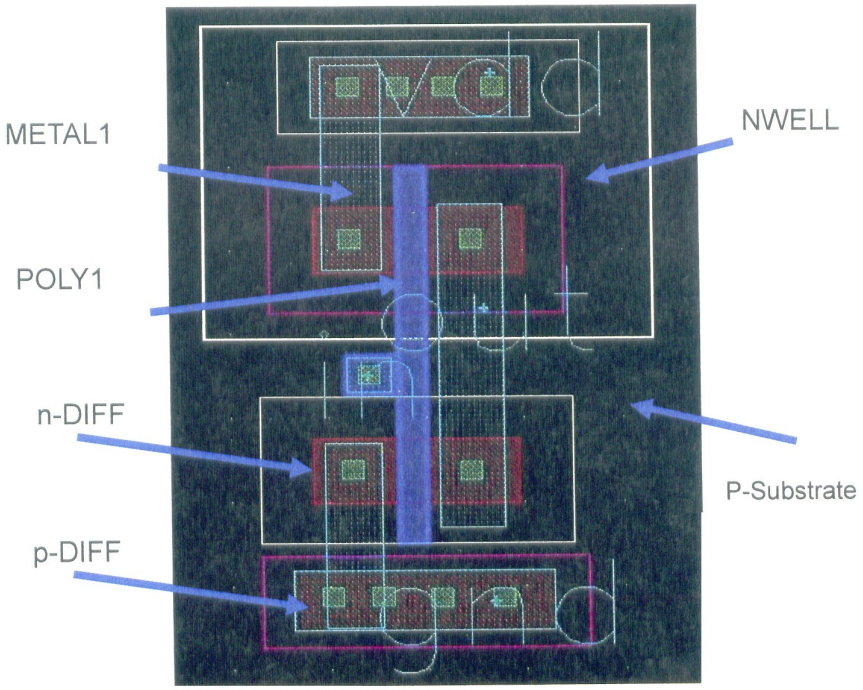
(b) MOSFET is shorthand of six English words. Please spell out the six English words in full by using English language.

8.

(A)



(B)



Please examine the above (A) and (B) color drawings.

(a) Is the above (A) drawing a logic diagram, a circuit, or a layout?

(b) Is the above (B) drawing a logic diagram, a circuit, or a layout?

(c) How many n-DIFF rectangles are there in the above (B) ?

(d) How many p-DIFF rectangles are there in the above (B) ?

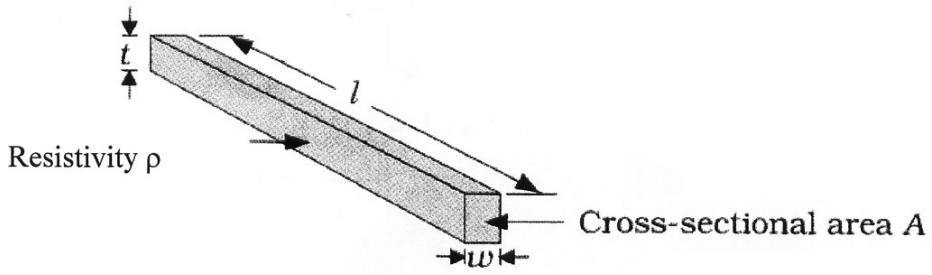
(e) How many contacts are there in the above (B) ?

(f) How many transistors are there in the above (B) ?

(g) How many transistors are there in the above (A) ?

(h) There is a p-DIFF rectangle in the bottom of (B). What is the purpose of that P-DIFF?

9. In the following drawing of a copper wire,



the "*l* (length)" is 100um, the "t" is 0.2um, the "*w*" is 0.2um, and the resistivity of copper at 30°C is 1.8×10^{-8} Ohm-m.

(a) If an electrical current flows from the near-end of the copper wire (marked with "cross-sectional area A") to the far-end, what is the resistance value?

(b) If the current flows from the bottom surface of the above copper wire to the top surface of the copper wire, what is the resistance value?

10. Please design an XNOR gate using a 4:1 MUX and provide the corresponding truth table of XNOR.