Midterm 2

1.

(a)

State transitions of synchronous sequential circuit happen at discrete instant of time while state transitions of asynchronous sequential circuit can be at any instants.

(b)

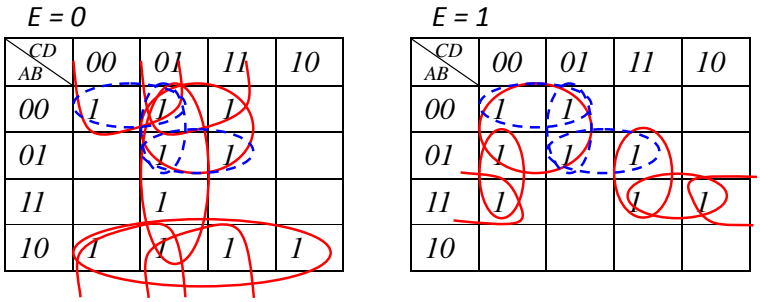
Latches are level sensitive while flip-flops are edge-triggered.

(c)

In ripple carry adder, the higher bit adder needs to wait the carry computed by previous adders while the carries of a carry look-ahead adder are computed by P, G or even primary inputs directly.

2.

(a)



(b)

(i) AB'E', C'DE', A'DE', B'C'E', B'DE', A'C'E, BC'D'E, BCDE, ABCE, ABD'E, A'B'C', A'C'D, A'BD

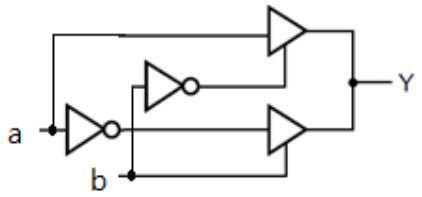
(ii) AB'E', C'DE'

(c)

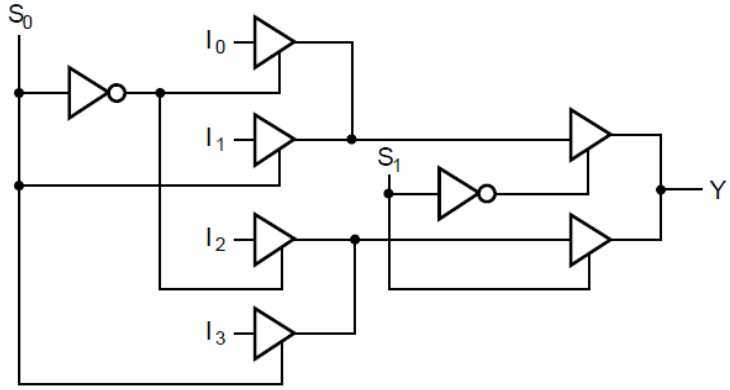
F = AB'E'+C'DE'+A'B'C'+A'BD+A'DE'+BC'D'E+ABCE

3.

(a)input: a, b output: Y



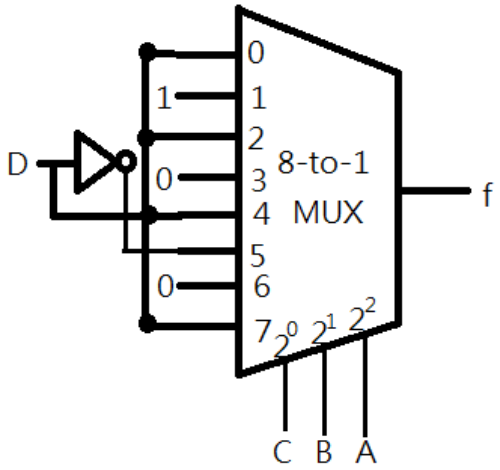
(b)input: S_1S_0, I_3, I_2 , I_1, I_0 output: Y



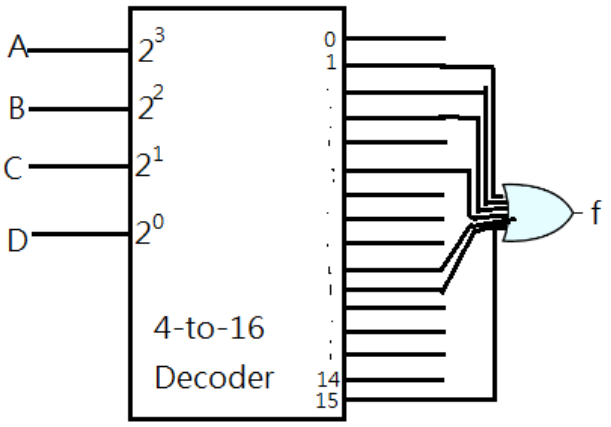
4.

(a)

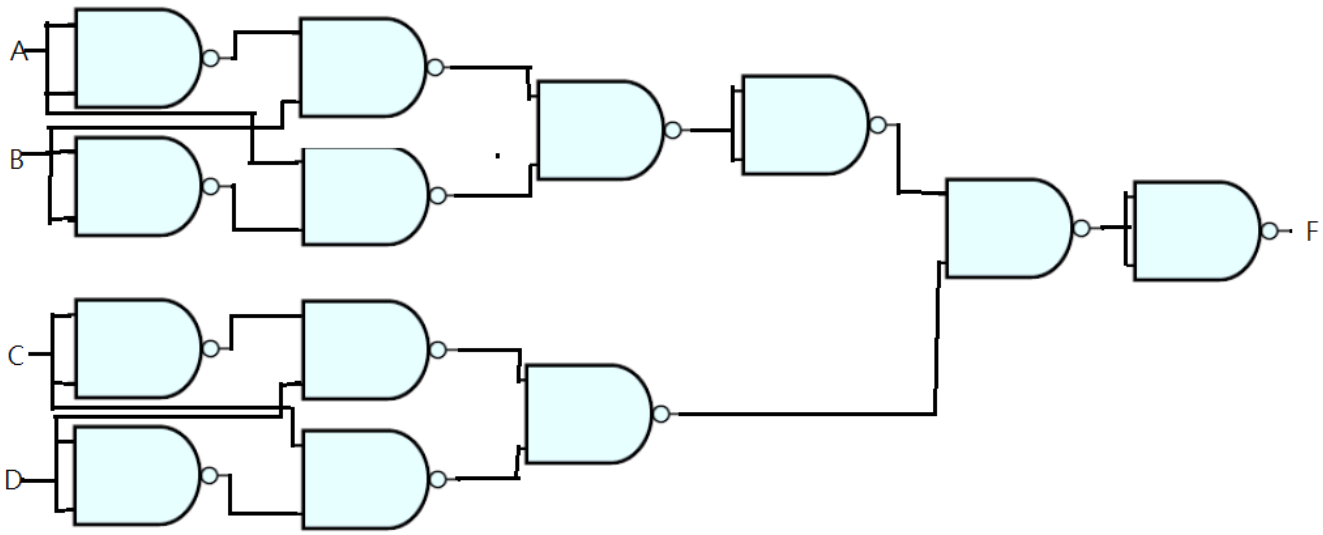
A	B	C	D	f	f=?
0	0	0	0/1	0/1	D
0	0	1	0/1	1/1	1
0	1	0	0/1	0/1	D
0	1	1	0/1	0/0	0
1	0	0	0/1	0/1	D
1	0	1	0/1	1/0	D’
1	1	0	0/1	0/0	0
1	1	1	0/1	0/1	D



(b)



5.



6.

(a)

SR latch

(b)

(S,R)=(0,0) keep the previous value (no operation)

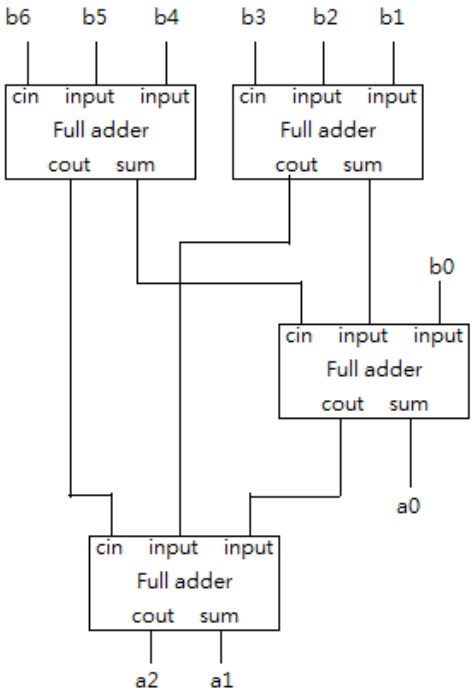
(S,R)=(0,1) reset Q (Q=0)

(S,R)=(1,0) set Q (Q=1)

(S,R)=(1,1) indeterminate value

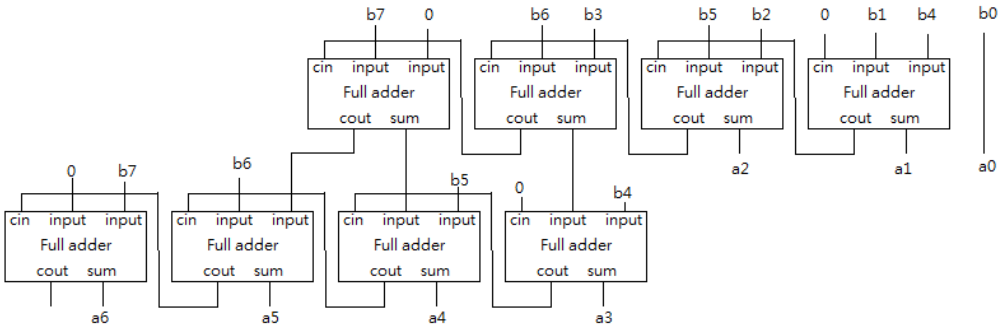
7.

Input: b6b5b4b3b2b1b0 output: a2a1a0



8.

Input: b7b6b5b4b3b2b1b0 output: a6a5a4a3a2a1a0



9.

Input: a, b, cin output: sum, cout