**CS 210201 Logic Design – Final** **Class:** _____

**ID:** _____

**Name:** _____

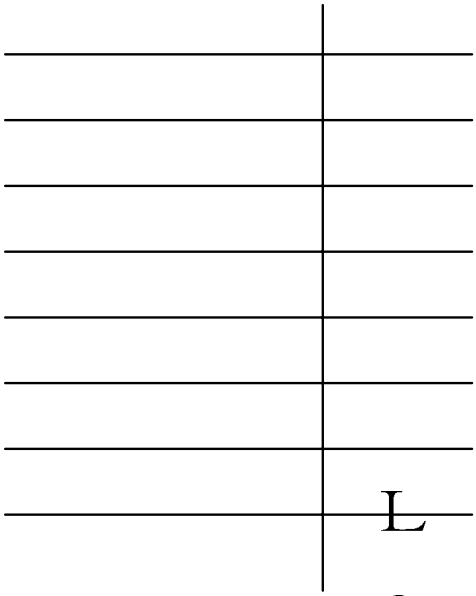
1. (20%)
   Use 3 JK-F/Fs (A, B, C) and gates to design a 3-bit counter which counts in the following sequence: 011(A=0, B=1, C=1), 001, 111, 101, 000, (repeat) 011, … Note that the counter you designed has to enter the main counting loop (sequence) 1 cycle later if it starts in any of unused states. For example, if it starts in an unused state, 110, the next state must be one of 011, 001, 111, 101, or 000. Please show all design processes, including state graph, state table, K-map, F/F input equations, and the final circuit.

Ans:
(ABC)

| p.s | n.s | | Ja | Ka | Jb | Kb | Jc | Kc |
|---|---|---|---|---|---|---|---|---|
| 000 | 011 | | 0 | x | 1 | x | 1 | x |
| 001 | 111 | | 1 | x | 1 | x | 0 | x |
| 010 | 111 | my assigned | 1 | x | x | 0 | 1 | x |
| 011 | 111 | | 0 | x | x | 1 | x | 0 |
| 100 | 111 | my assigned | x | 0 | 1 | x | 1 | x |
| 101 | 000 | | x | 1 | 0 | x | x | 1 |
| 110 | 111 | my assigned | x | 0 | x | 0 | 1 | x |
| 111 | 101 | | x | 0 | x | 1 | x | 0 |

Ja= b'c + bc'
Ka=b'c
Jb=a'+c'
Kb=c
Jc= 1
Kc = ab'

2. (15%)
(a) (7%) Given a falling-edge-trigger L-V Flip-Flop whose truth table is as shown in Fig. 1. Please implement this L-V Flip-Flop by using a falling-edge-trigger JK Flip-Flop and other logic gates if necessary.
(b) (8%) Please implement a T Flip-Flop by using this L-V Flip-Flop with other logic gates if necessary. Also verify that your design is really a T Flip-Flop.



| L | V | Q | Q+ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Fig. 1

(a) J=L, K=L+V
(b) L=V=T

3. (13%)
(a) (5%) Given a counter as designed in Fig. 2, draw its state graph. Assume the initial state is AB=00. What is the main counting sequence of this counter?
(b) (8%) If the counter in Fig. 2 starts at the states which are not in the main counting sequence, it will not enter into the main counting sequence. Please redesign the counter without adding any gate such that the new counter will enter into the main counting sequence when it starts at any state. You will get 0 point if you do not show the design process.

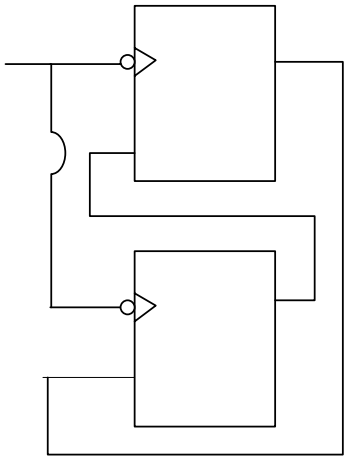


Fig. 2

(a) 00->11->00 (main), 01->01, 10->10

(b) Da=A'=Db

4. (8%)
   A Moore machine has one input X and one output Z. When the number of 1 in the input sequence is the multiples of 3 (0, 3, 6, …), the output becomes 1, else the output is 0. For example, the input sequence

   X = 0 1 0 0 1 0 1 0 0 1 1 1 0 0 1

   has the output

   Z = (1) 1 0 0 0 0 0 1 1 1 0 0 1 1 1 0

   Derive the state graph with the minimum number of states (3 states). Indicate which state is the reset state in your state graph.

| p.s | n.s | | z |
|---|---|---|---|
| | x=0, | x=1 | |
| S0 | S0 | S1 | 1 |
| S1 | S1 | S2 | 0 |
| S2 | S2 | S0 | 0 |

5. (15%)
   A sequential circuit has 2 inputs (X1 and X2) and one output (Z). The output begins as 0 and remains a constant value unless one of the following input sequence occurs
   (a) The input sequence X1X2=01, 00 causes the output to become 0.
   (b) The input sequence X1X2=11, 00 causes the output to become 1.
   (c) The input sequence X1X2=10, 00 causes the output to toggle.
   Please derive a Moore machine state graph with the minimum number of states (4 states). Indicate which state is the reset state in your state graph.

omitted

6. (10%)
A Mealy machine has one input X and one output Z. The output is the same as the input 3 clock periods previously. For example, the input sequence

X = 0 1 0 1 1 0 1 0 1 1 0 1 0 0 0 1

has the output

Z = 1 1 1 0 1 0 1 1 0 1 0 1 1 0 1 0

The first three values of Z are 1. Derive the state graph with the minimum number of states (8 states). Indicate which state is the reset state in your state graph.

omitted

7. (7%)
Given a state table as shown in Fig. 3. Please use the state assignment guideline 1 and guideline 2 to get the optimal state assignment, i.e., an assignment which satisfies the most suggestions in guideline 1 and guideline 2. Assume 000 is assigned to S0. Please also show the assignment map.

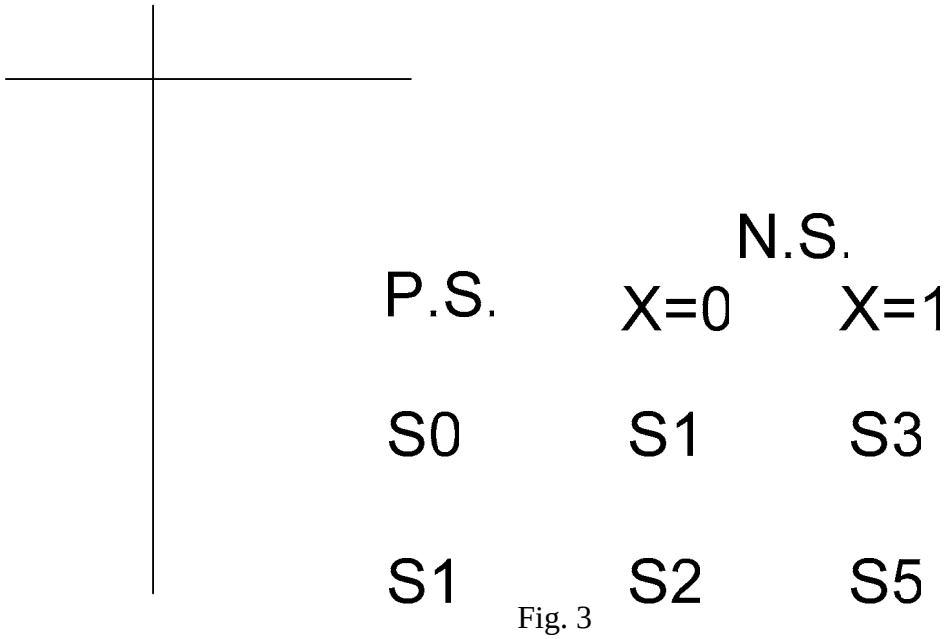



Fig. 3

S0=000, S1=011, S2=010, S3=100, S3=101, S5=110, S6=111

8. (10%)
   Please reduce the state table in Fig. 4 to the one with a minimum number of states. (Hint: use the implication chart method to minimize the number of states)

Fig. 4

S1= S2=S4, S3=S5

9. (10%)
   Please use an example to explain why guideline 1 and guideline 2 in state assignment do not work for minimizing the input equation in the designs with T flip-flops.

Omitted

10. (12%)
    Complete the following partial code of a half adder design.

```
module half_adder (sum, c_cout, a, b);

   (1)     a, b;
output     sum, c_out;
   (2)     sum, c_out;
always @ (  (3)  or  (4)  )
  begin
    sum = a ^ b ;
    c_out = a & b ;
  end
endmodule
```

(1) input
(2) reg
(3) a
(4) b

Have a Nice Vacation !!