國立清華大學 電機工程學系
九十五學年度 第一學期
EE-2280 邏輯設計 期中考試題
本試題－共計兩頁，七大題，總分 100 分
Closed-Book Examination (考試日期: 11/7/2006)

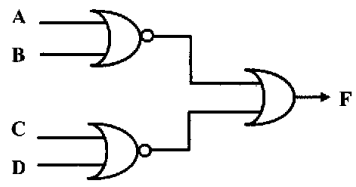
1. (40%) Answer the following questions briefly.
   (a) Calculate the *13's complement* of $(ABBA)_{14}$. Note that you answer should be in radix-14 notation. (5%)
   (b) What is the *most negative number* that can be represented using 10-bit 2's complement integer representation? (5%)
   (c) State the distinctive feature of the *Gray code* in one sentence. (5%)
   (d) Will an addition operation (-3)+(2) yield an *end carry*? Assume that the 2's complement notation is used for representing the 4-bit signed integers. (Simply answer yes or no). (5%)
   (e) How many output signals does a normal *k*-input decoder have? (5%)
   (f) An *essential prime implicant* is a prime implicant containing an essential minterm. What is an *essential minterm*? Define it in one sentence. (5%)
   (g) Express the function of the *sum bit*, S_i, of a full-adder cell in terms of its three inputs, A, B, C_{in}. (Feel free to use any primitive logic operator we ever discussed in class.) (5%)
   (h) Express the *carry output bit* function C_{i+1} at a bit position of a binary adder in terms of the *carry input signal* C_i, its *carry propagate signal* P_i, and *carry generate signal* G_i. (5%)

2. (10%) Cover $(3.4)_{10}$ to its unsigned binary format, $(YY.XXXX)_2$, where symbol 'X' or 'Y' is a binary bit.
   (a) Show the binary code of "YY". (5%)
   (b) Show the binary code of "XXXX". (5%)

3. (10%) Determine the base (or radix) of the numbers so that (54)/4 = (13).

4. (10%) Minimize a function into its product-of-sum form, $F(x, y, z) = x'y'z + x'yz + xyz$.

5. (10%) Convert the following NOR-OR implementation into its equivalent All-NAND two-level implementation. Draw your logic circuit and mark each input clearly.



6. (10%) Draw a complete 4-bit adder/subtractor using full-adders (FA) and XOR gates as the building blocks. Let the two inputs be $(A_3\ A_2\ A_1\ A_0)$ and $(B_3\ B_2\ B_1\ B_0)$. The circuit performs addition $A+B$ when the mode select signal M=0, and subtraction $A-B$ when M=1. Indicate your sum bits $(S_3\ S_2\ S_1\ S_0)$ and the overflow/underflow detection bit V clearly.

7. (10%) Consider the design of a 4-to-2 binary encoder.
   (a) Fill in the missing input combination in the following simplified truth table. (Note: impossible input combinations are ignored in a simplified truth table.) (5%)
   (b) Derive the Boolean expression of output function x. (5%)

Input ($D_3D_2D_1D_0$)	Output ($x\ y$)
0 0 0 1	0 0
0 0 1 0	0 1
0 1 0 0	1 0
(To be filled in)	1 1