Subject: Close-book quiz of CS3120-02, Oct. 24, 2006

Six Hints and Rules for a Fair Examination:

A. Close books and turn off all personal electronics including the cell phone's sound and vibration.

B. If you feel some number/word/sentence in one of this quiz's ten questions is wrong, you may write down the wrong on the answer sheet to earn extra credits. No penalty if the wrong pointed out by you turns out to be correct.

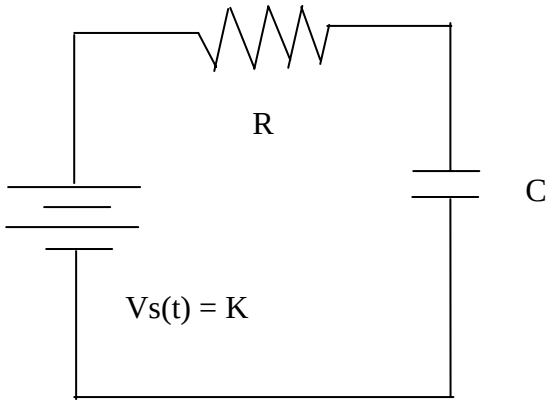
C. Please raise your hand with patience when you want to talk to the teacher or a TA.

D. Please try to understand and answer the questions properly.

E. Please express your "thought process" succinctly to avoid jump-to-conclusion answer; please make each of your final answers stands out clearly and explicitly to avoid grading errors.

F. Between 3:20PM and 5:00PM, you are welcome and allowed to talk to the teaching assistants. No chatting or any other form of communications between classmates will be allowed. All kinds of hand-held calculator or PDA are allowed and welcome. However, notebook computers or any other non-hand-held computers are not allowed.

1. A simple electric circuit is depicted in the following:



(a) Vs(t) is the supply voltage source and the voltage of the source is a positive constant K volt. $v_c(t)$ is the voltage across the above capacitor "C" and i(t) is the current flowing through the above resistor "R". Please provide a correct ordinary differential equation (ODE) that can model the above circuit by using $v_c(t)$ as the dependent variable and the following four circuit concepts:

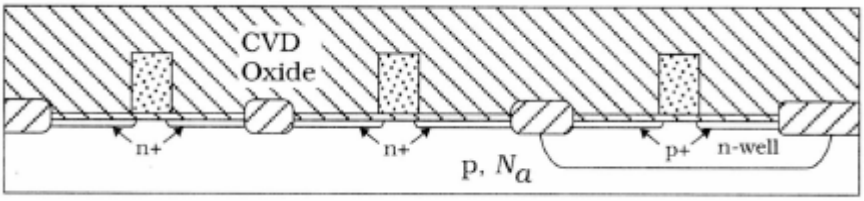
- KVL,
- KCL,
- $Q(t) = C * v_c(t)$,
- $i(t) = dQ(t)/dt$.

(b) If $v_c(t=0)=0$ for the above ODE. Vs(t)=K=1 volt for all t, please analytically solve the above ODE to achieve an explicit solution that describes v_c as function of t.

(c) If the R value is 500 Ohm and the C value is 0.002 Farad, what is the value of $v_c(t)$ when t is 1.0 second?

2. For the state-of-the-art nanometer CMOS process example depicted in the following, it is achieved using the following seven essential processing steps:

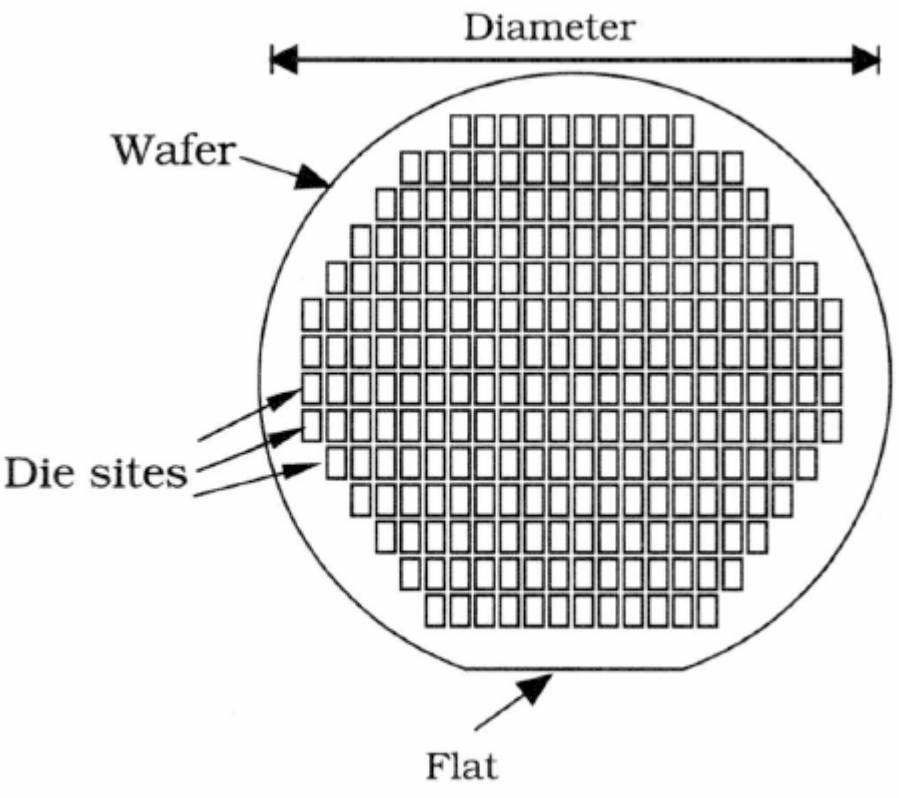
(1) deposit and pattern polysilicon gates
(2) deposit CVD oxide
(3) create thin oxide
(4) create field oxide
(5) purchase p-type wafers
(6) create n and p diffusions
(7) create n wells.



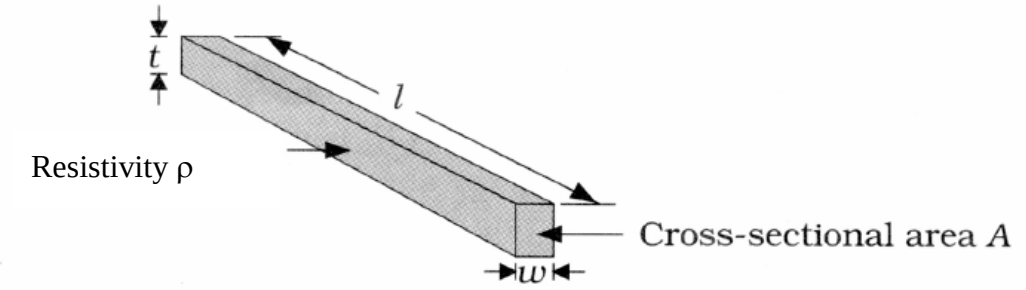
However, the above (1) to (7) steps are out of order. Please rewrite the above seven steps with the correct ordering.

3. Examining the following wafer carefully,

(a) What is the typical wafer diameter in Hsinchu today? Please use mm as the unit to answer.
(b) What is the typical thickness of a wafer?
(c) If the whole wafer is successfully processed with all steps perfectly, please estimate the maximum number of electronic commercial products that can be obtained from the following wafer?



4. In the following drawing of a copper wire,



the "*l* (length)" is 50um, the "t" is 0.5um, the "*w*" is 0.5um, and the resistivity of copper at 25°C is 1.7×10^{-8} Ohm-m.

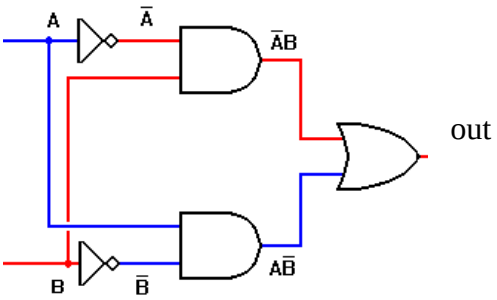
(a) If an electrical current flows from the near-end of the copper wire (marked with "cross-sectional area A") to the far-end, what is the resistance value?

(b) If the current flows from the bottom surface of the above copper wire to the top surface of the copper wire, what is the resistance value?

5. The following is a truth table example.

A	B	out
0	0	1
0	1	0
1	0	0
1	1	1

Examining the above table and the following drawing,



(a) Is the above drawing a logic diagram, a circuit, or a layout?

(b) The above drawing can be made by using nMOS and pMOS transistors. How many MOS transistors are needed to make the above drawing's function? Please explain why.

(c) A and B in the above drawing are the drawing's two binary inputs. On the right-hand side of the drawing, out is the drawing's only output. Can the above truth table in this page be used to describe the above drawing's function? If yes, why? If the above truth table cannot describe the above drawing's function, please provide the correct truth table.

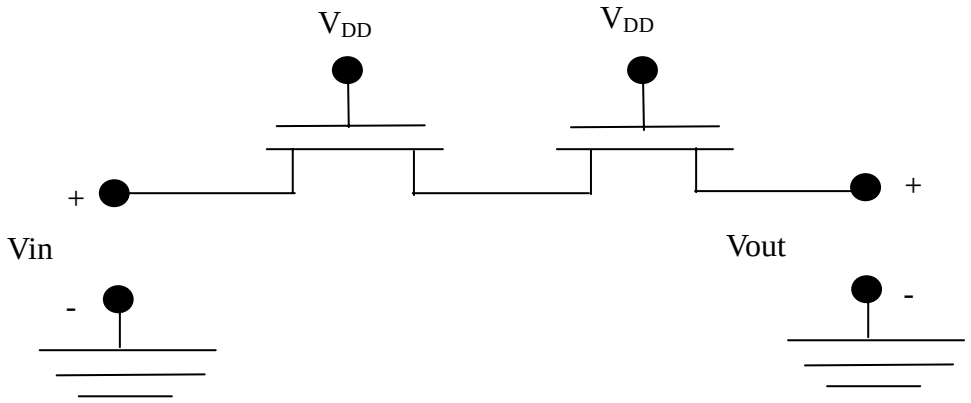
6. A sample of pure silicon sample is doped with phosphorous atoms with the density 5×10^{14} cm^{-3}

(a) Using the intrinsic carrier density of pure silicon as 1.45×10^{10} cm^{-3}, please find the majority and minority carrier densities.

(b) Please calculate the resistivity of the sample if $\mu n = 660$ cm^2/V-sec and $\mu p = 220$ cm^2/V-sec.

(c) If the sample's dimension is 2um x 0.5um x 50um, please find the largest possible resistance of the sample.

7. Consider the two-MOS chain in the following drawing,

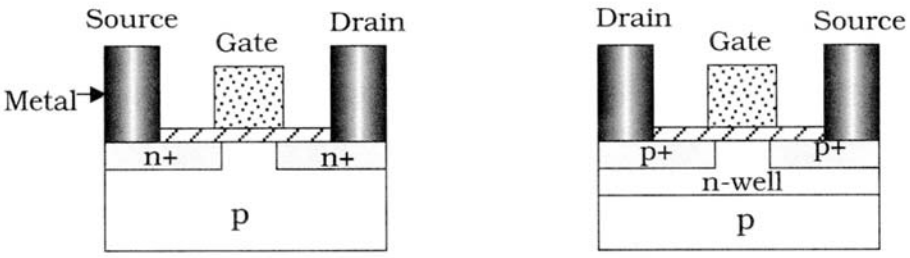


The power supply is $V_{DD} = 3V$ and the nMOS threshold voltage is $V_{Tn} = 0.5V$. Please find the output voltage Vout at the right of the chain for the following Vin:

(a) Vin = 2.9V; (b) Vin = 3.0V; (c) Vin = 1.4V.

8. Please design an XOR gate using a 4:1 MUX.

9. (a) When we apply a ground or negative voltage on the two gates of the following two drawings, which of the two FETs will be turned on?



(a) nFET cross-section (b) pFET cross-section

(b) FET is shorthand of three English words. Please spell out the three English words in full.

10. Examining the following capacitor with two parallel 0.2umX10umX10um metal plates insulated by an insulator layer with thickness 0.25um and permittivity $2.5\varepsilon_0$, where ε_0 is 8.854×10^{-12} F/m and is the permittivity of free space. Please calculate the following's capacitance value.