Department of Computer Science
Tsing Hua University
CS4100 Computer Architecture
Midterm, Spring 2010
April 27, 2010
7:00-9:00PM

1. (10%) Explain the following terms:
   (a) Yield
   (b) RISC vs. CISC
   (c) Harvard Architecture
   (d) Sign Extension (explain by an example)

2. (10%) Suppose you have a machine which executes a program consisting of 50% floating point multiply, 20% floating point divide, and the remaining 30% are from other instructions. Management wants the machine to run 4 times faster. You can make the divide run at most 3 times faster and the multiply run at most 8 times faster. Can you meet management's goal by making only one improvement, and which one? Show how you get your answer.

3. (15%) In MIPS assembly, write an assembly language version of the following C code segment:

```
int A[100], B[100];
  for (i=1; i < 100; i++) {
  A[i] = A[i-1] + B[i];
}
```

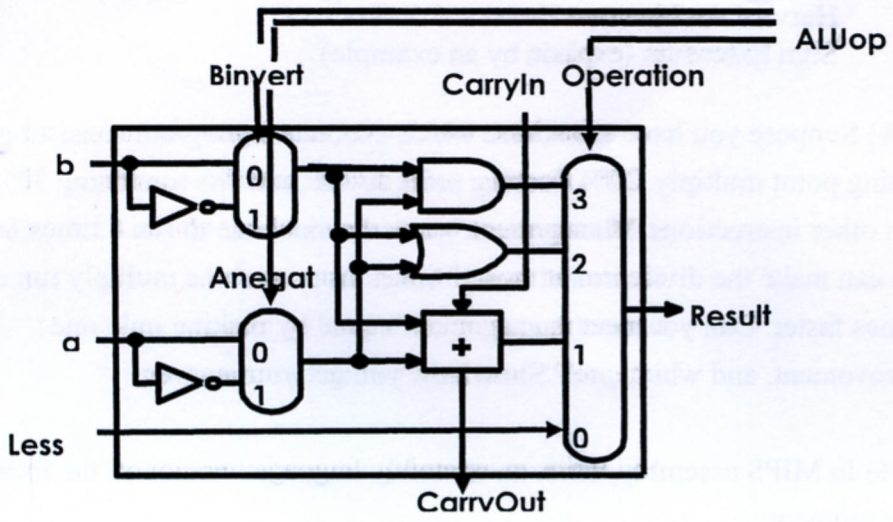
   At the beginning of this code segment, the only values in registers are the base address of arrays A and B in registers $a0 and $a1. Avoid the use of multiplication instructions–they are unnecessary.

4. (10%) You wish to call a subroutine named FOO. $a0 and $a1 are already used in the caller routine and the caller also needs to pass its two arguments using these two registers. Moreover, the called subroutine will use register $t1. Write a MIPS code segment to perform the following operations: Before calling FOO, save $t1, $a0 and $a1 on the stack, then call FOO. Once FOO returns, restore the values from the stack back to $t1, $a0 and $a1. Note that this is an example of caller-saved subroutine.

5. (10%) Please give the three types of instruction format in MIPS. Explain each field briefly.

6. (10%) The following figure shows an implementation of ALU. Please give the function specifications of the following operations.

Operations 4 bits (Anegat, Binvert, ALUop)
Sub
Nor
Nand



7. (10%) Adder design.
   (a) (5%) Design a carry look-ahead adder. Please give the logic equation of pi (propagate term) and gi (generate term). Given c0, p1, g1, p2, g2, p3, g3. Give the equation to produce c3.
   (b) (5%) Design a 4*n*-bit carry select adder. Let the adder be partitioned into four *n*-bit adders. (a) Give the block diagram of the design (b) What is the propagation delay of the adder in terms of *n*-bit adder and mux delay?
8. (15%) Let *a, b, c* be three 8-bit operands to a carry save adder and their values be *a* = 00110110, b = 11101101 and c = 01001011.
   (a) (5%) What are the two outputs of this carry save adder?
   (b) (5%) Given the above carry save adder as basic building block, please show the block diagram of 8 × 16 Wallace-tree multiplier with minimum delay.
   (c) (5%) Assume that the last stage is performed by carry ripple adder. Give the minimum delay in terms of full adder delay.
9. (10%) Representation of floating point number
   (a) (5%) Let the 32-bit pattern, 11010101101010…000, represent a single precision floating point, where bit 31 is a sign-bit, bits 30 to 23 represent the exponent, bit 22 to 0 the significant, bias 127 is used for exponent and hidden 1 is used. What is the number?
   (b) (5%) By the above representation, show how to represent a decimal number 64.28.