DEPARTMENT OF COMPUTER SCIENCE
NATIONAL TSING HUA UNIVERSITY
CS 4100: Computer Architecture
Fall 2004, Final Examination

1. (15%) Explain the following terms:
   a. Superscalar and VLIW processor
   b. Write buffer
   c. Principle of locality

2. (20%) [SINGLE-CYCLE PROCESSOR] Consider the single-cycle datapath shown in Fig. 1 of the attached sheet. (a) (12%) Mark directly on the diagram all the paths and components that are actively in use in executing a `sw` instruction. Return the sheet together with your answer book. (b) (8%) Which components are used as sequential circuit?

3. (10%) [MULTIPLE-CYCLE PROCESSOR] Modify the microprogram and dispatch ROM1 in Fig. 2 of the attached sheet to implement the control for the instruction `bne`. Let the opcode of `bne` be 000101. Suppose the "PCWrite Control" field takes a fourth value, `ALUOut-cond-not`, which indicates to write the PC with the content of ALUOut if the Zero output of the ALU is inactive.

4. (20%) [PIPELINE DESIGN] (a) (12%) Reschedule the following code so that as many stalls as possible can be eliminated when the code is executed on the pipelined machine described in the text book. Assume that the data-path contains both the Forwarding Unit and the Hazard Detection Unit.

```
        add   $5,   $0,    $3
loop    lw    $2,   100($20)
        add   $5,   $5,    $2
        add   $4,   $5,    $6
        add   $8,   $5,    $7
        addi  $20,  $20,   -4
        bne   $20,  $0,    loop
```

   (b) (8%) Let the above loop be executed 30 times. How many cycles are needed to complete the rescheduled code on the pipelined machine?

5. (5%) [PIPELINE DESIGN] Consider the above code again. If the branch `bne` is implemented as a delay branch. How will you schedule the code to take advantage of the delay slot?

6. (20%) [MEMORY HIERARCHY] Consider the following system:
   Virtual address 34 bits;
   TLB 2-way set associative with 512 total entries in TLB;
   4KB page size;
   Physical address 36 bits;
   Total cache data size = 256 KB;
   Cache block size = 64 B;
   Cache 2-way set associative.
   (a) (15%) Show the size of the labeled fields a, b, c, d, e, f in Fig. 3 (see reverse side) of TLB and cache. (b) (5%) What is the organization of the TBL and cache, e.g. direct-mapped, N-way set-associative, or fully associative?

7. (10%) Give two reasons why the situation, (cache hit, TLB hit, virtual memory miss), will never occur.

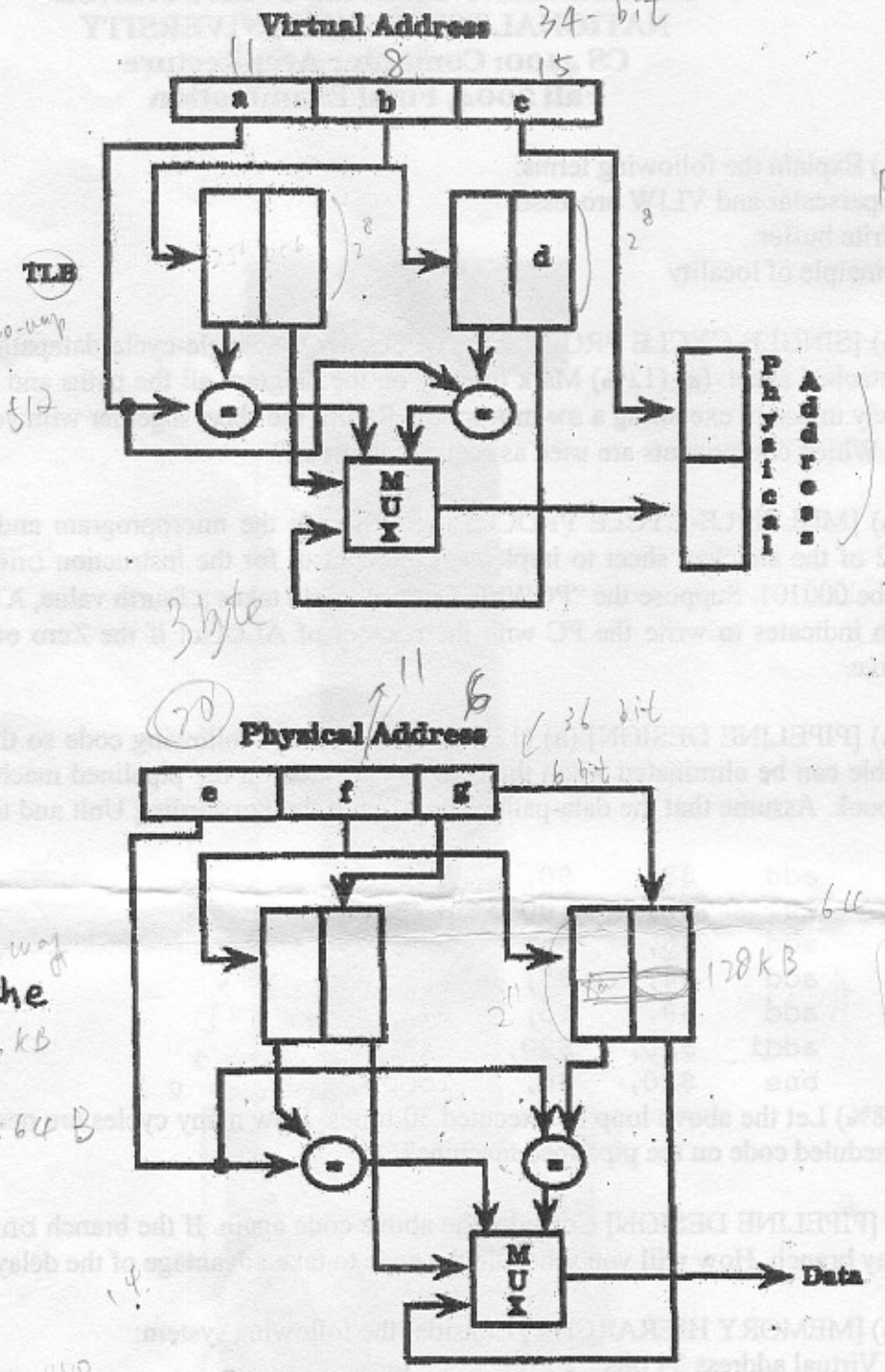
Virtual Address
a
b
c
TLB
d
MUX
Physical Address
Physical Address
e
f
g
Cache
MUX
Data

Fig. 3

Return this sheet with your answer book! **Name:**_____ **ID:**_____

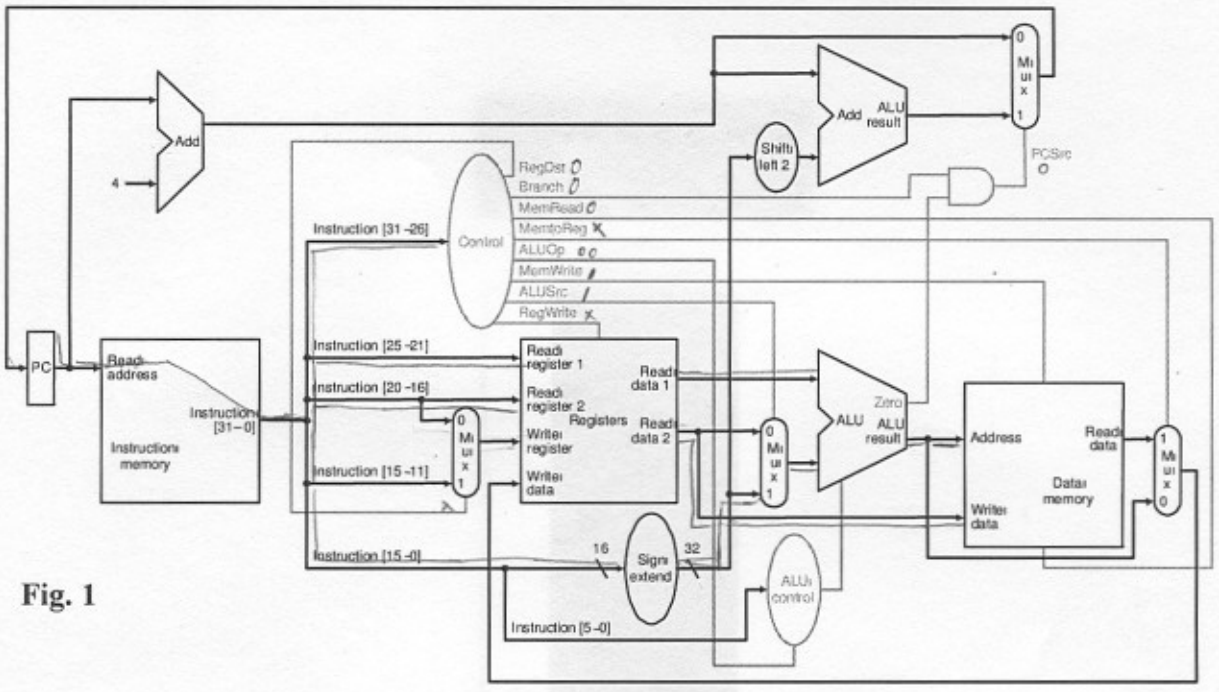

Fig. 1

Label	ALU control	SRC1	SRC2	Register control	Memory	PCWrite control	Sequencing
Fetch	Add	PC	4		Read PC	ALU	Seq
	Add	PC	Extshft	Read			Dispatch 1
Mem1	Add	A	Extend				Dispatch 2
LW2					Read ALU		Seq
				Write MDR			Fetch
SW2					Write ALU		Fetch
Rformat1	Func code	A	B				Seq
				Write ALU			Fetch
BEQ1	Subt	A	B			ALUOut-cond	Fetch
JUMP1						Jump address	Fetch

Fig. 2