1. Hardware Design by Verilog: design a SMUX (out = a*sel + b*$\overline{sel}$) using three different methods in Figure 1a. (15%)
   i. assign: {assign …}
   ii. always block: {always @ (a or b or sel)}
   iii. Gate level modeling: {not U0(sel_n, sel); and U1(…);}
2. Hardware Design by Verilog: design a positive edge FF with asynchronous and with synchronous set (15%)

```
module SMUX(out, a, b, sel);
        output out;
        input a,b,sel;
        wire out;
```

(a)

```
module xxx(result,a,b,sel);
output [5:0]result;
input [2:0] a,b;
input [1:0] sel;
reg [2:0] a,b;

always @(a or b or sel)
begin
case (sel)
0:    result = a + b;
1:    result = a & b;
2:    result = a * b;
3:    result = a / b;
end
endmodule
```

(b)

Figure 1

3. Describe what are the problems of the followings. Hint: in data types (10%)
   甲、wire [7:0] databus; always @(read or addr) databus=read ? mem[addr] : 'bz;
   乙、reg myreg; and (myreg, net1, net2);
4. Describe what is hardware design using schematic and what are the advantages of using HDL designs compared to using schematic design? (10%)
5. Describe what is the placement and routing (10%)
6. Describe what is an FPGA? Describe what does look up table mean? (10%)
7. There are 3 syntax errors in the following code. Please find them out and fix them. (15%)
8. The frequency of the clock generator on the demo board is 20 MHz. In order to let the LED of the demo board to respond every second, we need to do **dividing frequency** (lab3: running light, lab4: clock counter). Explain how you do the frequency dividing. (15%)