CS 210201 Logic Design –Midterm #2 **Class:** _____

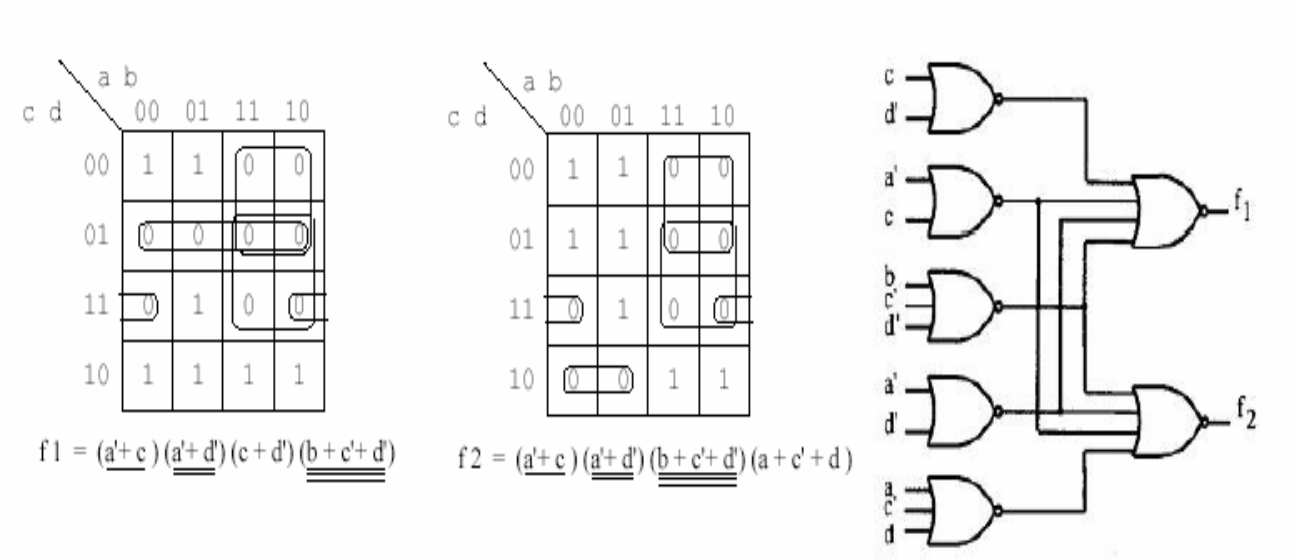
ID: _____

Name: _____

(Note: inverted inputs are allowed)

1. (12%) Find a minimum (shared) two-level, multiple-output NOR-NOR circuit to realize $f_1(A, B, C, D) = \sum m(0, 2, 4, 6, 7, 10, 14)$ and $f_2(A, B, C, D) = \prod M(2, 3, 6, 8, 9, 11, 12, 13, 15)$. (Note: $m_7 = A'BCD$, $M_7 = (A + B' + C' + D')$).

Ans:



2. (6%) Complete the timing diagram for the circuit as shown in Fig. 1 (Y from 1~28ns, Z from 3 ~28ns). Assume the AND gate has delay of 1ns and the NOR gate has delay of 3ns.

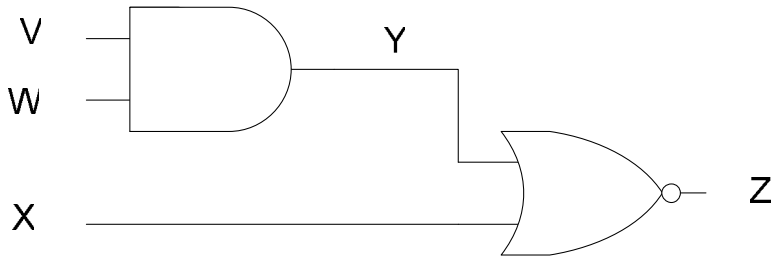
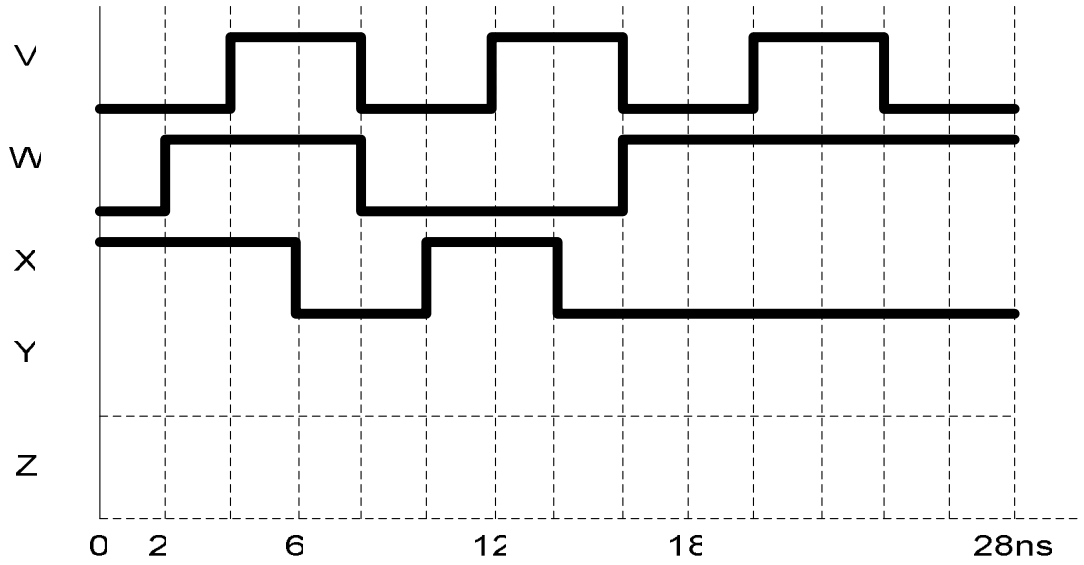
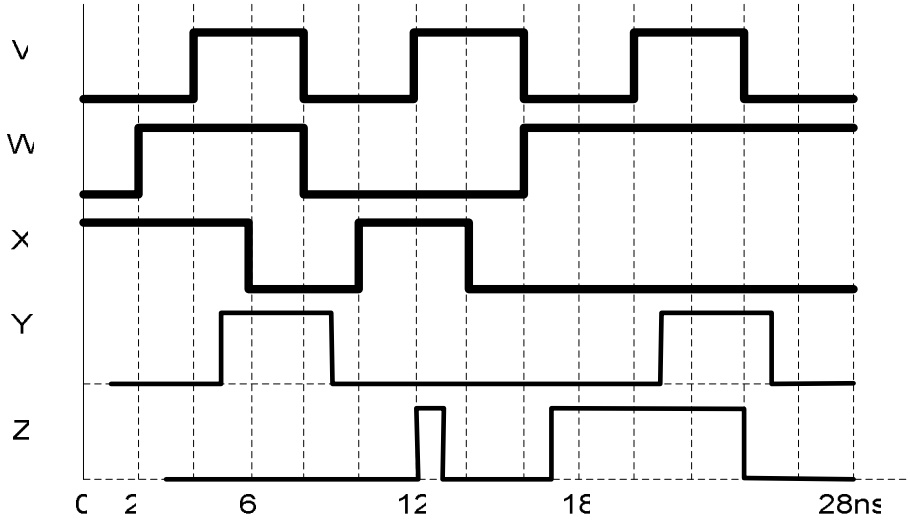


Fig. 1



Ans:

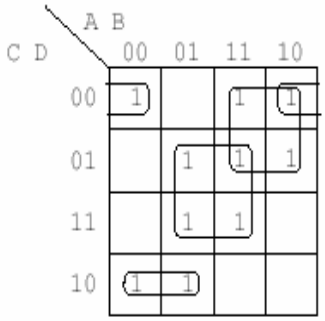


3. (13%) Consider the function F(A, B, C, D) = ∑ m (0, 2, 5, 6, 7, 8, 9, 12, 13, 15). (a) (3%) Find a minimum AND-OR circuit which implements F. (b) (6%) Identify two 1-hazards in your implementation. (c) (4%) Find an AND-OR circuit for F which has no hazards.

Ans:

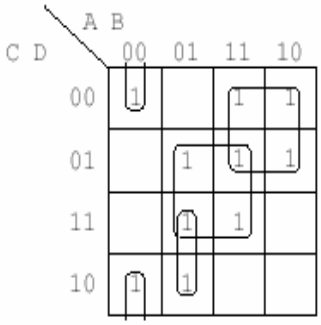
8.10 (a) $F(A, B, C, D) = \sum m(0, 2, 5, 6, 7, 8, 9, 12, 13, 15)$

There are 3 different minimum AND-OR solutions to this problem. The problem asks for any two of these.



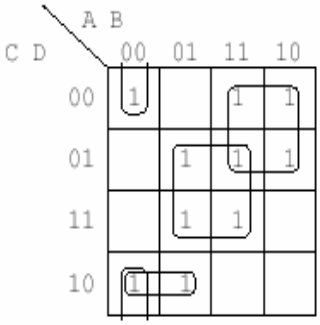
F = B D + A C' + A'C D' + B'C'D'

Solution 1: 1-hazards are between 0000↔0010 and 0111↔0110



F = B D + A C' + A'B'D' + A'B C

Solution 2: 1-hazards are between 0010↔0110 and 0000↔1000



F = B D + A C' + A'B'D' + A'C D'

Solution 3: 1-hazards are between 0111↔0110 and 0000↔1000

Without hazards:

$F' = BD + AC' + B'C'D' + A'CD' + A'B'D' + A'BC$

8.10 (b)

4. (4%) Explain these two terms. (a) (2%) Verification. (b) (2%) Testing.

Ans: Omitted

5. (12%) Given a logic circuit as shown in Fig. 2. According to the SPEC, with applying the input vector (A, B, C, D) = (1, 1, 0, 0), the output value at W should be 0. However, the actual simulation result is 1. Assume the possible errors are only either AND ←→OR, or Inverter ←→ Buffer, and only one error occurs at a time. Please indicate three possible error locations in which a single error occurs.

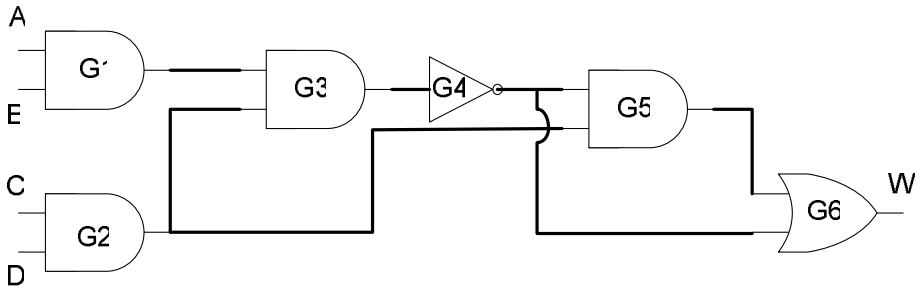


Fig. 2

Ans:G6, or G4, or G3

6. (6%) Implement the function G (A, B, C) = ∑ m (0, 4, 6, 7) using a 4-to-1 MUX with selection inputs A and B as shown in Fig. 3. (Note: m_3 = ABC = 011, and when AB=10, I_2 will be selected).(Hint: To determine the I_0~I_3.)

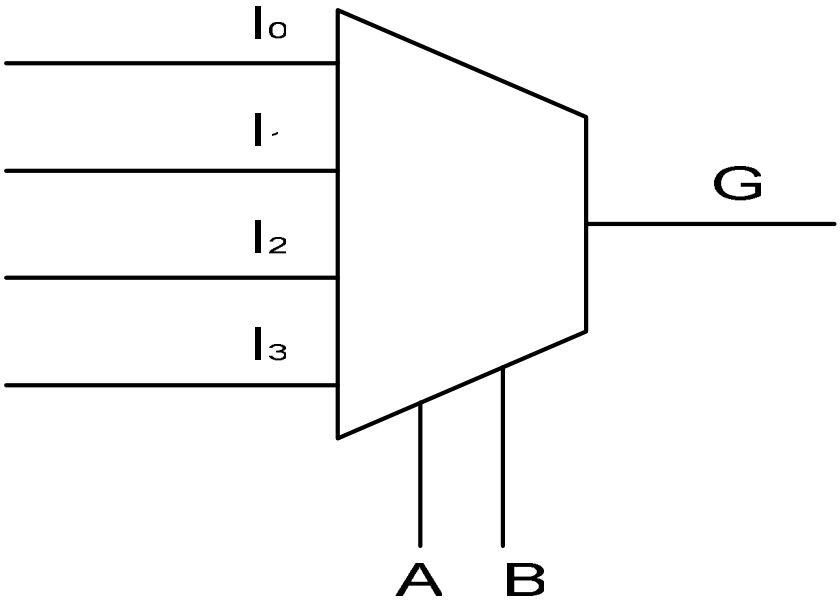
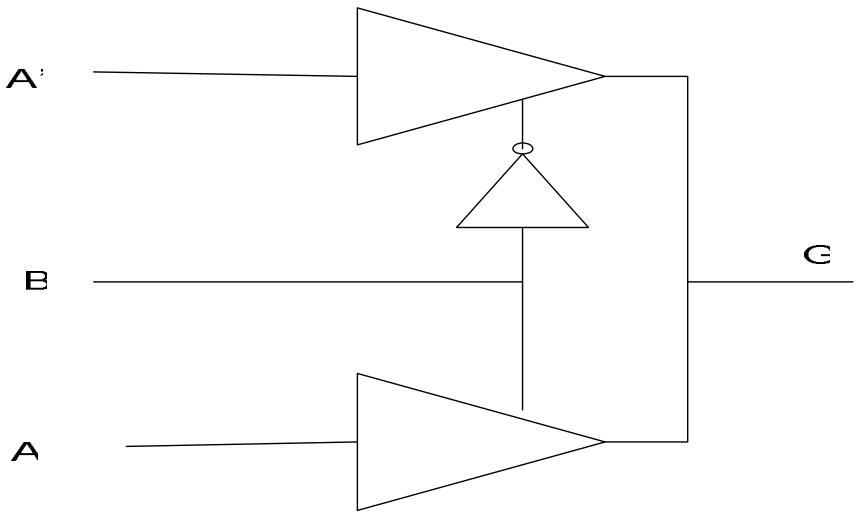


Fig. 3

Ans: I_0~I_3 =c', 0, c', 1

7. (5%) Implement the function G = A'B'+AB using two three-state (tri-state) buffers and one inverter. Assume B is the control line of three-state buffers.

Ans:



8. (6%) Given F = ABC + DE' + A'BE + BD'E. Expand F about the variables A and B.

Ans: A'B'(DE') + A'B(DE' +E) + AB'(DE') + AB (C+DE' +D'E)

9. (12%) The PLA in Fig. 4 will be used to implement for the following equations:

X = ABD + A'C+ BC + CD
Y = A'C + AC' + C'D'
Z= CD + A'C + ABD

Indicate the connections that will be made to program the PLA to implement these equations.

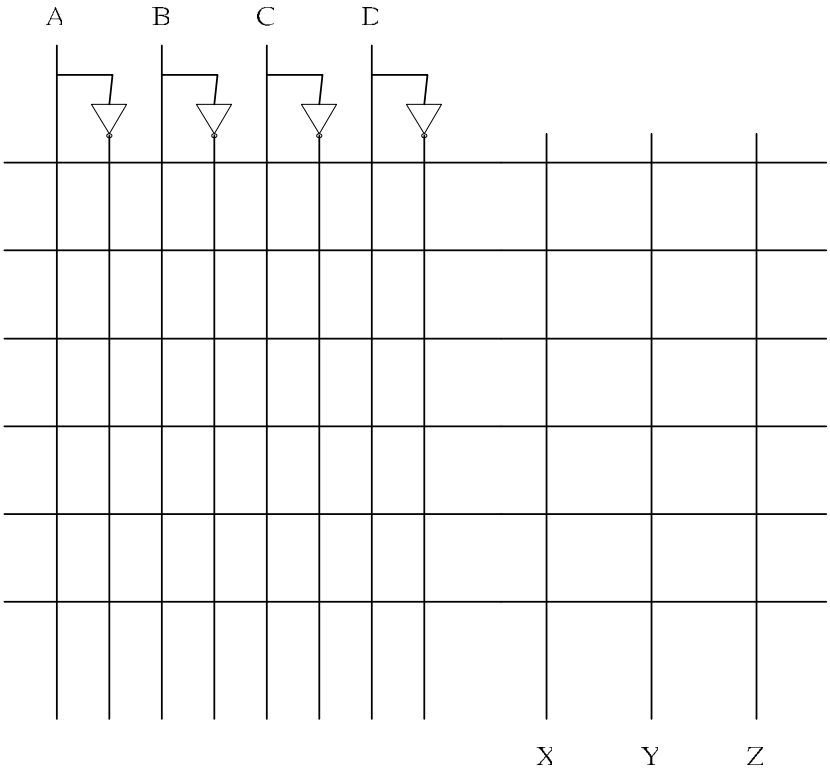
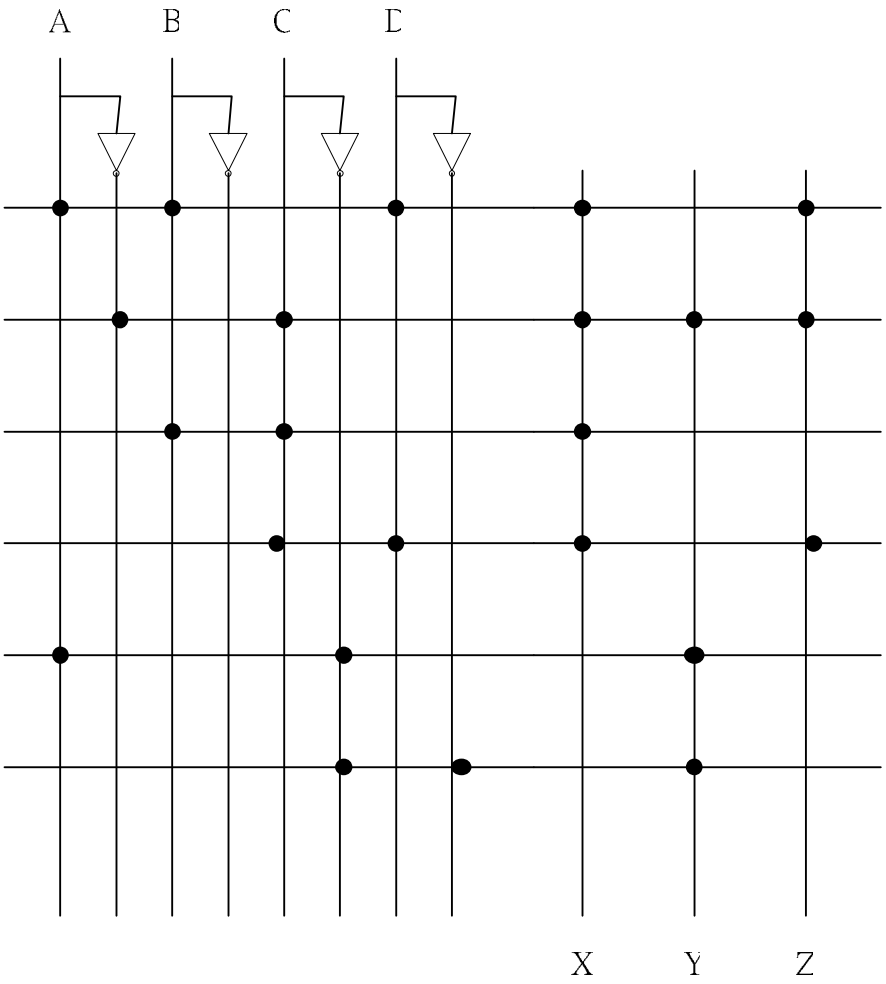


Fig. 4

Ans:

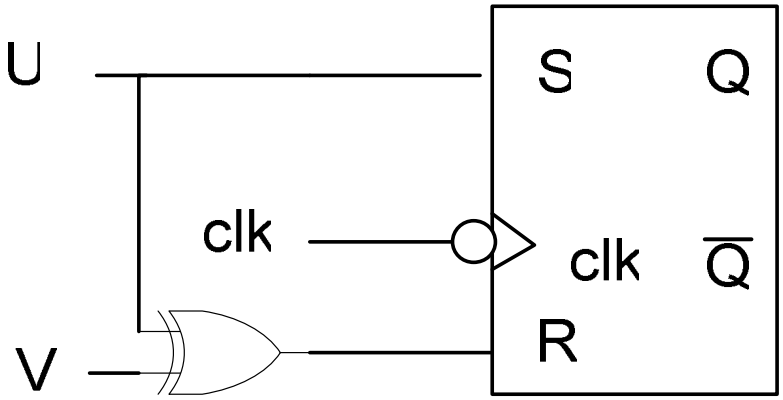


10. (6%) Given a falling-edge-trigger U-V Flip-Flop whose truth table is as shown in Fig. 5. Please implement this U-V Flip-Flop by using a falling-edge-trigger S-R Flip-Flop and other logic gates if necessary.

U	V	Q	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	Inputs are not allowed
1	0	1	Inputs are not allowed
1	1	0	1
1	1	1	1

Fig. 5

Ans:



11. (8%) Given a sequential circuit consists of four T Flip-Flops as shown in Fig. 6. Assume the initial state $Q_4Q_3Q_2Q_1$ is 0000. Draw the state graph of this circuit. (That is, the state sequence from the initial state 0000).

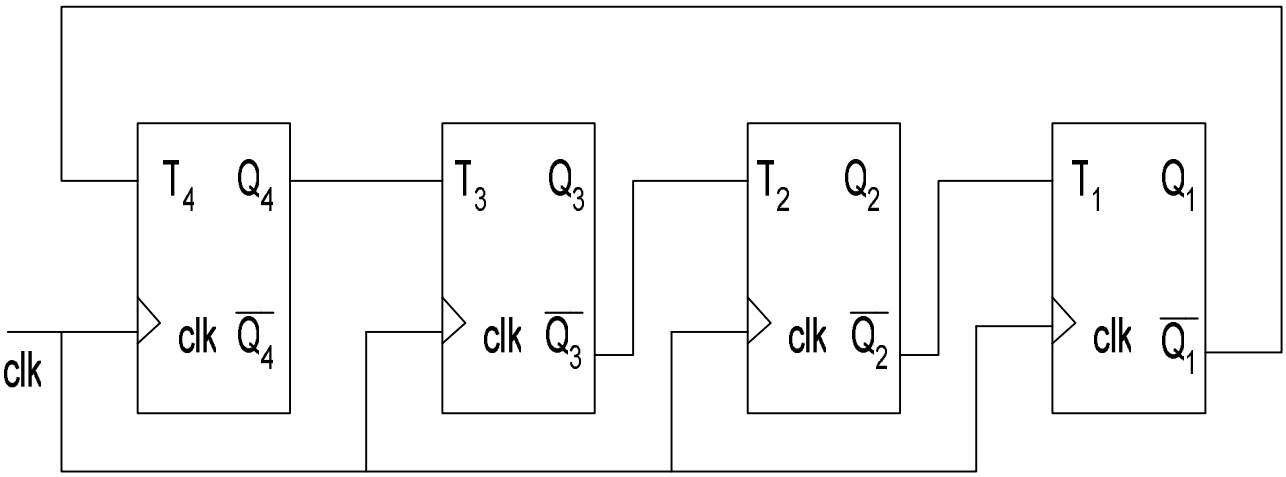


Fig. 6

Ans: 0000→ 1011→1101→1000→0111

12. (10%) Design a 4-bit bi-directional rising-edge-trigger shift register as shown in Fig. 7. Inputs are (clk, D_4 ~D_1, SIL, SIR, SHL, SHR); output are (Q_4, Q_1). Its operations are summarized in the following table. (Hint: you may need four D Flip-Flops and 4 MUXes for the design.)

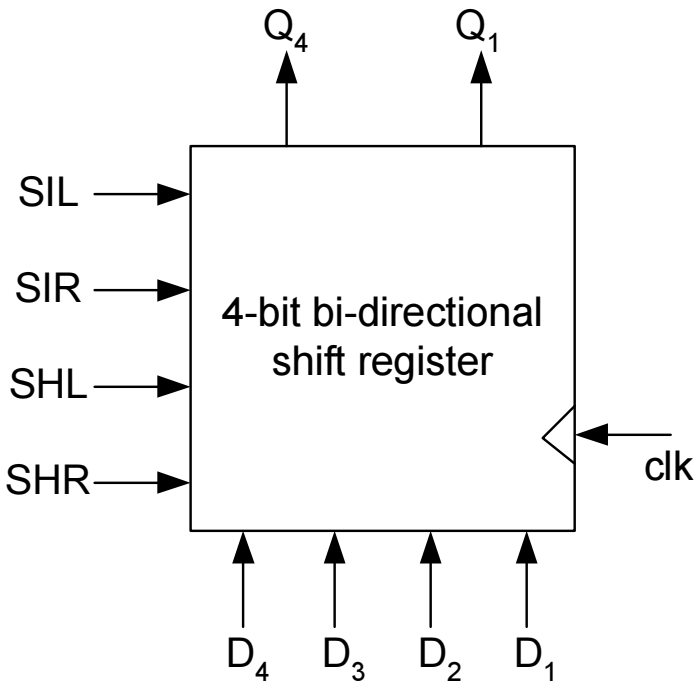
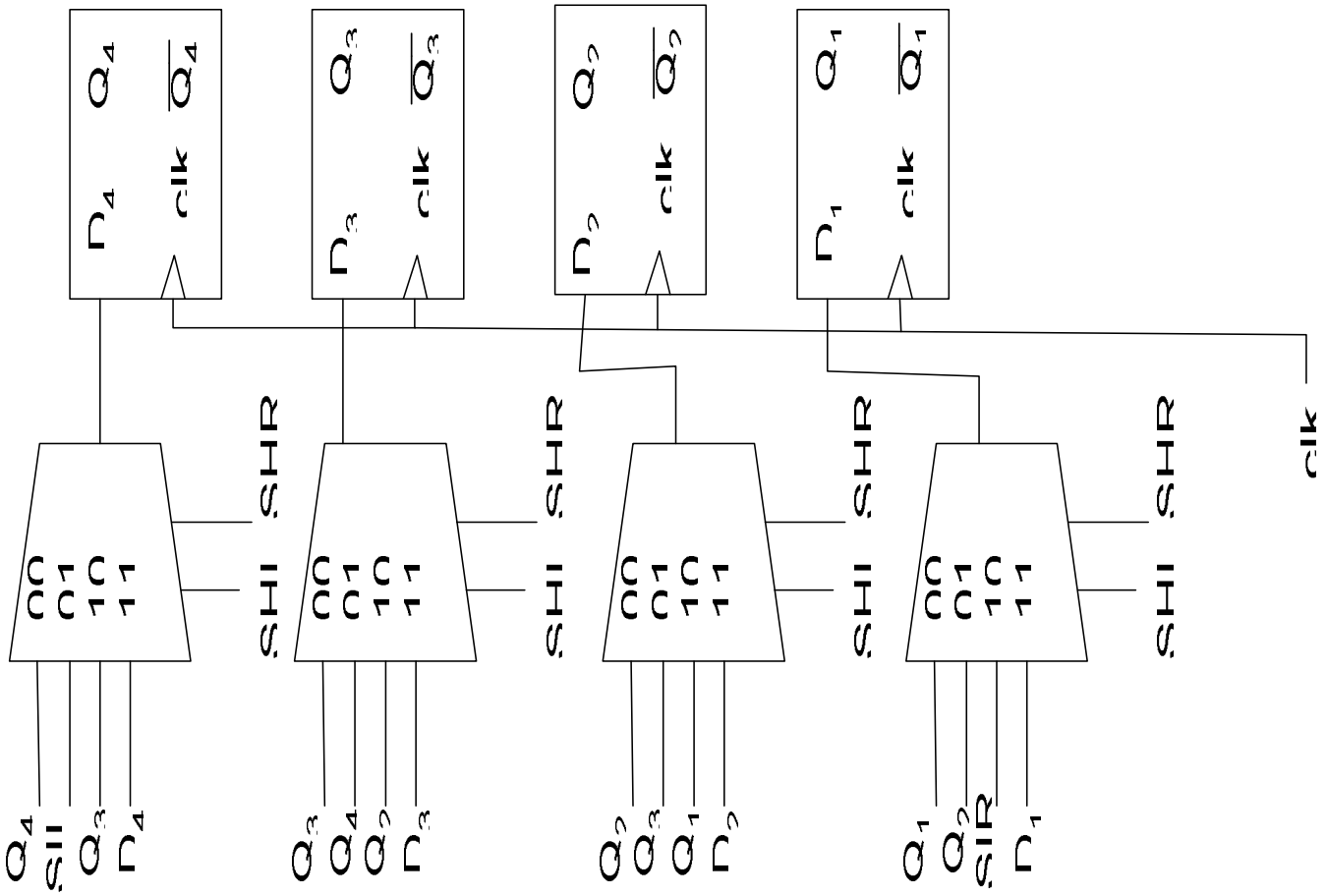


Fig. 7

SHL	SHR	Operations
0	0	Data remain intact
0	1	Shift right, the leftmost FF get the data from SIL and the rightmost FF shift out the date at Q_1
1	0	Shift left, the rightmost FF get the data from SIR and the leftmost FF shift out the date at Q_4
1	1	Load D_4 ~D_1 to the register

Ans:



13. (6%) Bonus: What are three wishes made by the man, the woman, and the guy from Magic Lamp in the joke I talked during the course?

Ans: Omitted