

CS2101 Midterm II

Date: 3:30-5:10pm, Thursday, May 21, 2015

1. (40pt) Analyze the FSM below

i. (12pt) Find next state function and output function

■ $NS1 = f1(PS1, PS0, X)$

■ $NS0 = f2(PS1, PS0, X)$

■ $Y = f3(PS1, PS0, X)$

ii. (13pt) Write state transition table

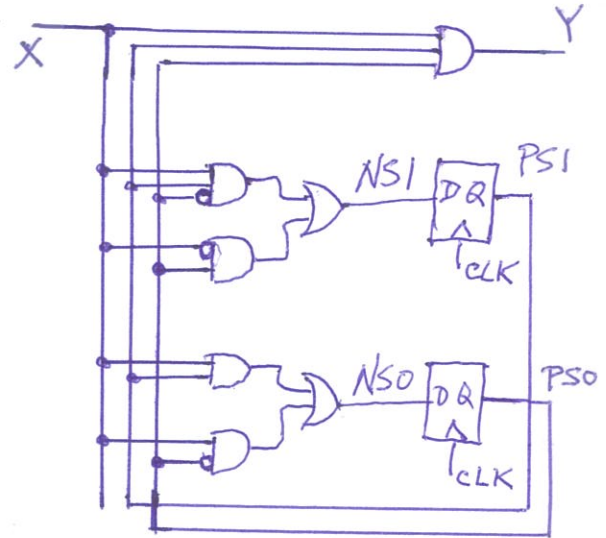
Truth Table Format

X	PS1	PS0	NS1	NS0	Y
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

*Hint: Three 1s in Column NS1 & NS0; One 1 in Column Y

Symbolic State Format

PS	NS		Y	
	X = 0	X = 1	X = 0	X = 1
A (00)				
B (01)				
C (10)				
D (11)				



iii. (5pt) Draw symbolic state transition diagram. It's a Mealy machine with four states and eight transitions.

iv. (5pt) Find state transition S and output stream Y given input stream X. Assume initial state A.

X	1	0	1	1	1	0	1	1	0	1	1	1	0	0	1	1	0	0
S	A																	
Y																		

v. (5pt) Describe its functionality

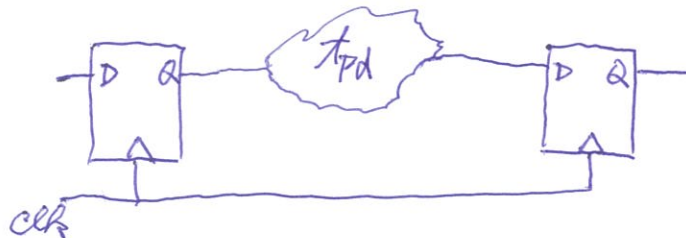
2. (35pt) Design an FSM that has one input X and one output Y. Y should output “1” when the FSM sees the end of a string of 1s; and “0” otherwise.

E.g.,

X: 0001 0111 0011 00

Y: 0000 1000 1000 10

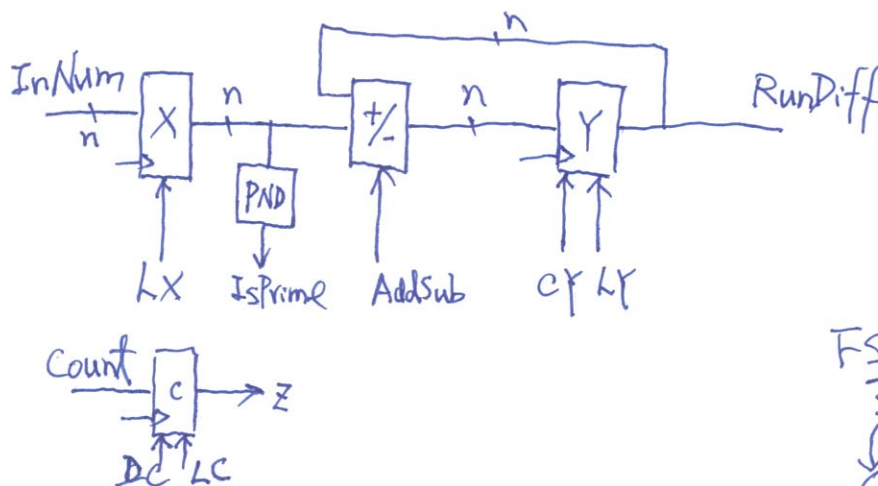
- i. (10pt) Draw symbolic state transition diagram. Use Mealy style machine with two states, A and B, where A is the initial state.
 - ii. (5pt) Write state transition table.
 - iii. (5pt) Assign binary codes to states ($A \leftarrow "0"$, $B \leftarrow "1"$) and write state transition table in truth table form.
 - iv. (5pt) Define next state function $NS = f(PS, X)$
 - v. (5pt) Define output function $Y = g(PS, X)$
 - vi. (5pt) Draw logic gate circuit diagram
3. (10pt) A positive-edge-triggered D-type flip-flop has following timing spec
- Set-up time constraint (t_s) = 35ps
- Hold time constraint (t_h) = 20ps
- Contamination delay (t_{cCQ}) = 10ps
- Propagation delay (t_{dCQ}) = 25ps
- i. When combinational delay $t_{pd} = 140ps$. How fast can the system being clocked (in GHz)?
 - ii. What is the minimal value of t_{pd} to guarantee no hold-time violation?



4. (15pt) Given a datapath below and an incomplete controlling FSM that calculates the running difference between the sum of prime numbers and sum of non-prime numbers. Write actions associated with each of three transitions.

E.g.,

Start	0	1	0	0	0	0	0	0	0	0	0	0
Count	-	8	-	-	-	-	-	-	-	-	-	-
InNum	-	-	2	5	6	8	7	11	14	17	-	-
RunDiff	-	-	0	2	7	1	-7	0	11	-3	14	-
Done	0	0	0	0	0	0	0	0	0	0	1	-



FSM Input & Output:

Start: Begin Operation

Done: Job is done

Datapath Input and Output:

Count: Number of Input Data to be processed

InNum: Input Port of Data

RunDiff: Running Difference

Command Signals to Datapath:

LC: Load Counter C from input "Count"

~~CC: Clear Counter C to 0~~ DC: Down Count C

LX: Load Register X

CY: Clear Register Y

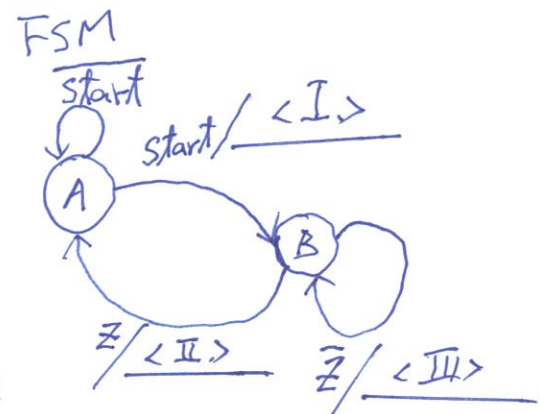
LY: Load Register Y

AddSub: 0 for Addition; 1 for Subtraction

Status Signals from Datapath:

IsPrime: The Value of Register X is Prime

Z: The Value of the Counter is zero



1. <i>
$$NS1 = X \cdot PS1 \cdot \overline{PS0} \mid \overline{X} \cdot PS0$$

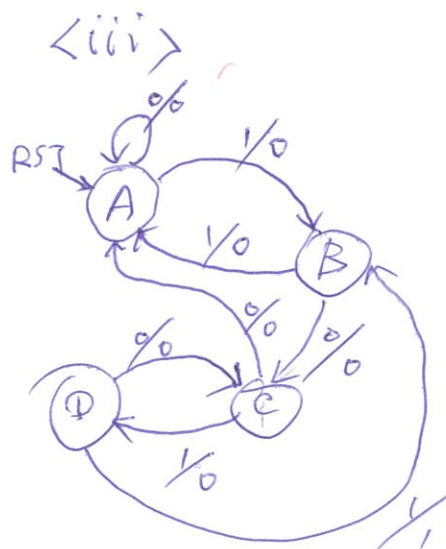
$$NS0 = X \cdot PS1 \mid X \cdot \overline{PS0}$$

$$Y = X \cdot PS1 \cdot PS0$$

<ii>

X	PS1	PS0	NS1	NS0	Y
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	0	0	0
1	1	0	1	1	0
1	1	1	0	1	1

PS	X=0	X=1	Y=0	Y=1
A	A	B	0	0
B	C	A	0	0
C	A	D	0	0
D	C	B	0	1



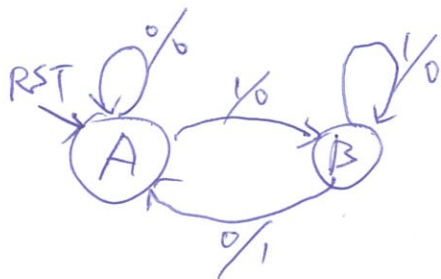
<iv>

$X = 101110110111001100$
 $S = ABCDBAABBAABAAABAA$
 $Y = 000100000000000000$

<v> It detects 1st "1011".

It was meant to detect all "1011". if $B \rightarrow A$ is changed to $B \rightarrow B$.

2. <i>



<ii>

PS	NS		Y	
	X=0	X=1	X=0	X=1
A	A	B	0	0
B	A	B	1	0

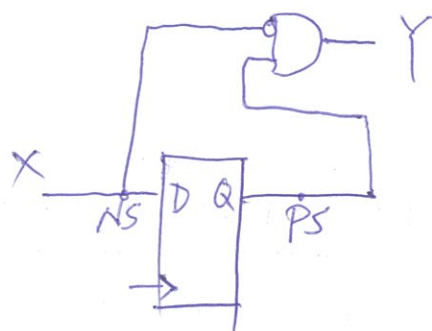
<iii>

X	PS	NS	Y
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	0

<iv> $NS = X$

<v> $Y = \bar{X} \cdot PS$

<vi>



~~(i) $NS = X$~~

$$3. \langle i \rangle T_{\text{cycle}} \geq T_{\text{dcq}} + T_{\text{pd}} + T_{\text{s}} \\ = 25 + 140 + 35 \\ = 200 \text{ ps}$$

$$f_{\text{req}} = \frac{1}{T_{\text{cycle}}} \leq \frac{1}{200 \times 10^{-12}} = 5 \text{ GHz} \quad \dots \text{Max Speed}$$

$$\langle ii \rangle T_{\text{ccq}} + T_{\text{pd}} \leq T_{\text{h}}$$

$$10 + T_{\text{pd}} \leq 20$$

$$T_{\text{pd}} \leq 10 \text{ ps}$$

confirmation
✓

Min Path delay to meet hold time constraint

4.

	LC	DC	LX	CY	LY	AddSub	Done
<I>	1	0	X	1	0	X	0
<II>						X	1
<III>	0	1	1	0	1	$\overline{\text{IsPrime}}$	0

0(不做)跟X(don't care)的區別: 用"別人問你"去想