CS2102 01 Digital Logic Design Final Exam (10:10am-12:00pm, Jan 13th)

Name: _____ **ID:** _____ **(Return this with your answer sheet)**

Truth or False (30%):

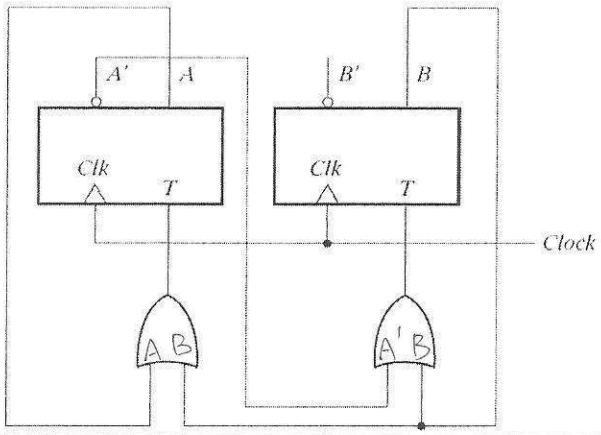
(Write down T or F. You don't need to give the reason.)

1. _____ For a circuit with 4 inputs $\{w, x, y, z\}$, $P = w \oplus x \oplus y \oplus z$ is an even parity generator, and $C = P \oplus w \oplus x \oplus y \oplus z$ is its odd parity checker.
2. _____ The following properties of XOR are all true: $A' \oplus B = (A \oplus B)'$, $A \oplus B \oplus C \oplus D = \sum(1, 2, 4, 7, 8, 11, 13, 14)$.
3. _____ Two states, s_j and s_k in an FSM are said to be equivalent ($s_j \equiv s_k$), iff $\forall i \in x$, $h(s_j, i) = h(s_k, i)$ and $f(s_j, i) = f(s_k, i)$ where f is the output function, h is the next-state function, and x is the set of inputs.
4. _____ Asynchronous counters are special type of register that counts upward or downward, or in any other pre-specified sequence. All flip-flops of an asynchronous counter are triggered by a common clock signal.
5. _____ A binary ripple counter with negative-edge triggered T FFs is a down counter.
6. _____ A self-correcting counter ensures that when a circuit enters one of its unused states, it eventually goes into one of the valid states after one or more clock pulses so that the circuit can resume its normal operation.
7. _____ ROM and flash memory are non-volatile memories.
8. _____ The access time of a memory is the time required to select a word and write it.
9. _____ For a $32M \times 16$ RAM, there are 25 address lines and memory storage consists of 2^{29} bytes.
10. _____ One of the major differences between SRAM and DRAM is that DRAM need to be refreshed periodically, but SRAM need not.

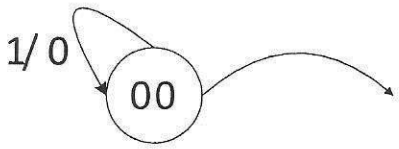
Answer the following questions: (70%)

(Write down your intermediate results. Do not give the final answer only.)

1. (8%) **[sequential circuit with T flip-flops]** Derive the state table and the state diagram of the sequential circuit shown in the following. Explain the function that the circuit performs.



2. (12%) **[sequential Design]** Design a sequential gray-code counter with two JK flip-flops A and B, one input Hold, and one output Carry_Out. When Hold=1, the state of the circuit remains the same. When Hold=0, the circuit goes through the state transitions from 00 to 01, to 11, to 10, then back to 00, and repeats. The output Carry_Out=1 only when the state transits from 10 to 00.
   (a) (3%) List the characteristic table and excitation table of JK FF.
   (b) (3%) Complete the state diagram.



   (c) (6%) Simplify the input equation of each JK flip-flop using the K-map method.
3. (10%) **[state reduction]**
   (a) Reduce the number of states in the following state table step by step, and tabulate the reduced state table.

	Next State		Output	
Present State	X=0	X=1	X=0	X=1
A	F	B	0	1
B	D	C	0	1
C	G	A	1	1
D	F	E	0	1
E	D	C	0	1
F	F	B	1	0
G	G	H	0	0
H	G	A	1	1

   (b) Using binary encoding for the state assignment, draw the state diagram.
4. (6%) **[register]** Design a three-bit register with a parallel **load** control, a left **shift** control and a synchronous **clear** signal. The parallel data input is $\{I_2 I_1 I_0\}$ and the serial data input is I_S. The data output is $\{A_2 A_1 A_0\}$. The register is cleared synchronously when the clock goes through a positive transition and the clear input is equal to 1. Otherwise, when {load, shift} = {10}, the register performs the parallel load, $\{A_2 A_1 A_0\}=\{I_2 I_1 I_0\}$; when {load, shift} = {01}, the register performs the left-shifting with the serial data input I_S; the register holds otherwise. You can use D flip-flops, AND/OR/INV/XOR gates, MUXes, etc.
5. (10%) **[counter]** Design a counter with D flip-flops that goes through the following repeated binary sequence: 0, 1, 5, 3. Simplify the input equations for the circuit and draw the state diagram. Show that if the simplified circuit is a self-correcting counter or not. Also draw the logic diagram.
6. (6%) **[memory]** For a 256×1 memory, if the coincident decoding is used by splitting the internal decoder into X-selection and Y-selection using two smaller decoders of the same size.
   (a) What is the size of each decoder? And how many AND gates are required for decoding the address?

(b) Determine the X and Y selection lines that are enabled when the input address is the binary equivalent of $(61)_{10}$. Draw a simple two-dimensional decoding structure with the two decoder to help illustrate it.

7. (8%) **[memory]** Using 4x4 RAM blocks to construct a 16x4 RAM. Hint: The inputs of the 4x4 RAM block are $\{A_1A_0\}$ (as the address), $\{D_3D_2D_1D_0\}$ (as the data-in), 1-bit enable, and 1-bit read/write (to control the memory read and write). The output is $\{Q_3Q_2Q_1Q_0\}$ (as the data-out). You may use a decoder, four 4x4 RAM blocks and four OR gates.
8. (10%) **[PLA]** Derive the PLA programming table for the combinational circuit that squares a three-bit number $\{A_2A_1A_0\}$ to produce a five-bit output $\{B_4B_3B_2B_1B_0\}$. Minimize the number of product terms in the PLA. Draw the squarer using the PLA logic diagram.
   Hint: the ROM implementation of this squarer is shown in the lecture notes.

Good luck and happy examining! Also Happy Chinese New Year!

If you still have too much time left, there is always a (longer) joke for you:

Two students were doing pretty well on all of the quizzes, midterms, and assignments so that they decided to go up to a party and had a great time at the night before the final exam. However, they ended up staying longer than planned, and they didn't make it back to the exam in time. They found the professor after the final. They lied to him, and told him that they went home and planned to come back in time to study, but that they had a flat tire on the way back and didn't have a spare and couldn't get help for a long time. So they were late getting back to campus. Professor thought over and agreed that they could make up the final. He placed them in separate rooms, handed each of them a test sheet. They looked at the first problem, which was 5 points and quite simple. "Cool" they thought, "this is going to be easy." They did that problem and then turned the page. They were unprepared, however, for what they saw on the next page. It said: (95 points) "Which tire?"