HW4a

1. Design a single digit decimal adder with input A[3:0], B[3:0], C_{in}(ci), and output S[3:0]and C_{out}(co).
   (a) Provide a logic function or logic diagram
   (b) Verilog RTL representation with Verification.
2. Design a 3-to-8-line decoder with enable (input ***in***[2:0], enable ***en*** and output ***d***[7:0]).
   (a) Provide a logic function or logic diagram
   (b) Verilog RTL representation with verification.

