Verilog Introduction

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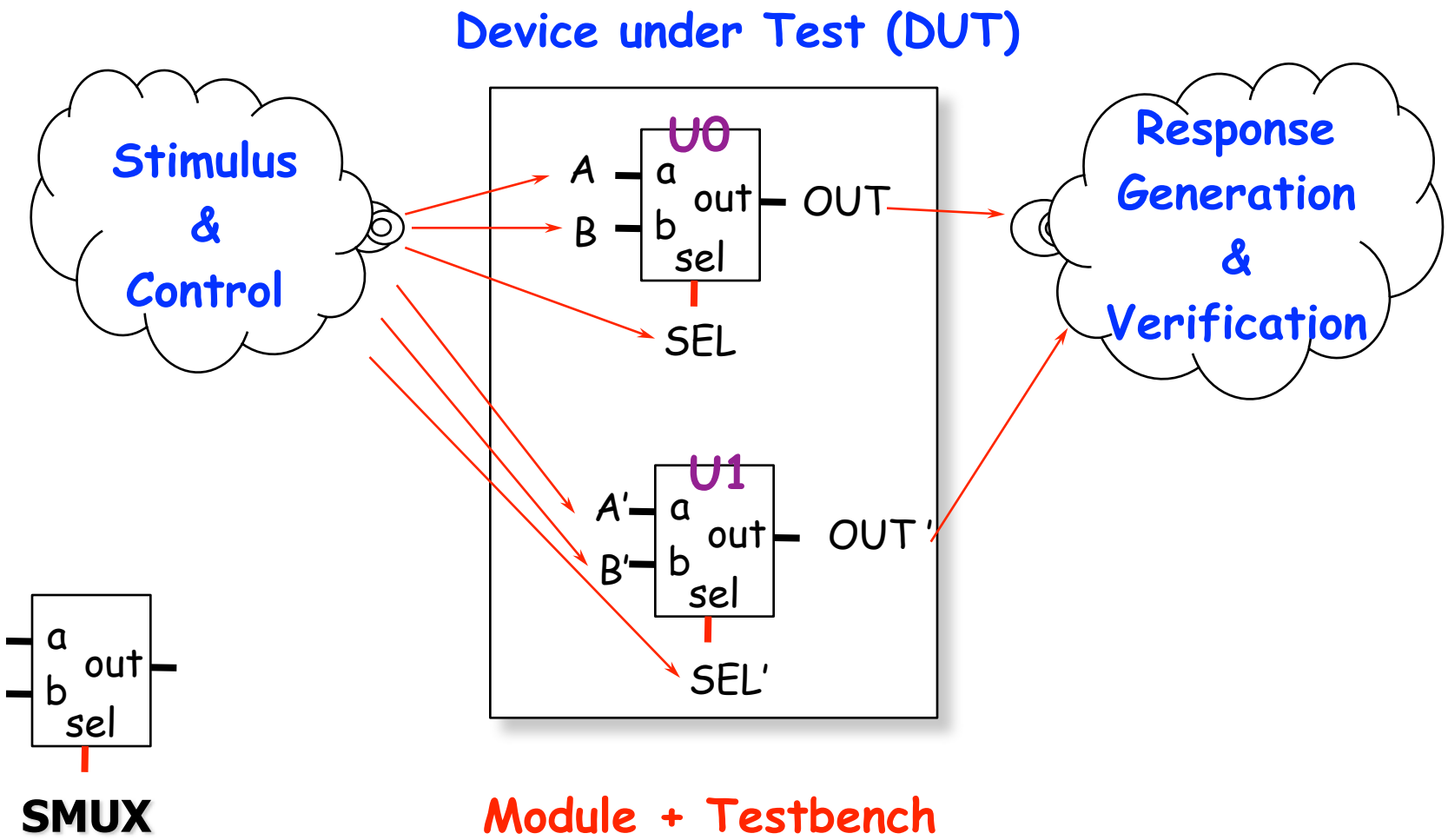
Hardware Description Language

- A high-level programming language offering special constructs to model microelectronic circuits
  - Describe the operation of a circuit at various level of abstraction
    - Behavior
    - Function
    - Structure
  - Describe the timing of a circuit
  - Express the concurrency of circuit operation

Scenario


Device under Test (DUT)
Stimulus & Control
Response Generation & Verification
U0
A
B
a
b
out
sel
OUT
SEL
U1
A'
B'
a
b
out
sel
OUT'
SEL'
a
b
out
sel
SMUX
Module + Testbench

Verilog Module

module name declaration

I/O definition

module functionality

```
module smux(out, a, b, sel);
output out;
input a,b,sel;

assign out = (a&sel) | (b&(~sel));

endmodule
```

Verilog Testbench

module name declaration

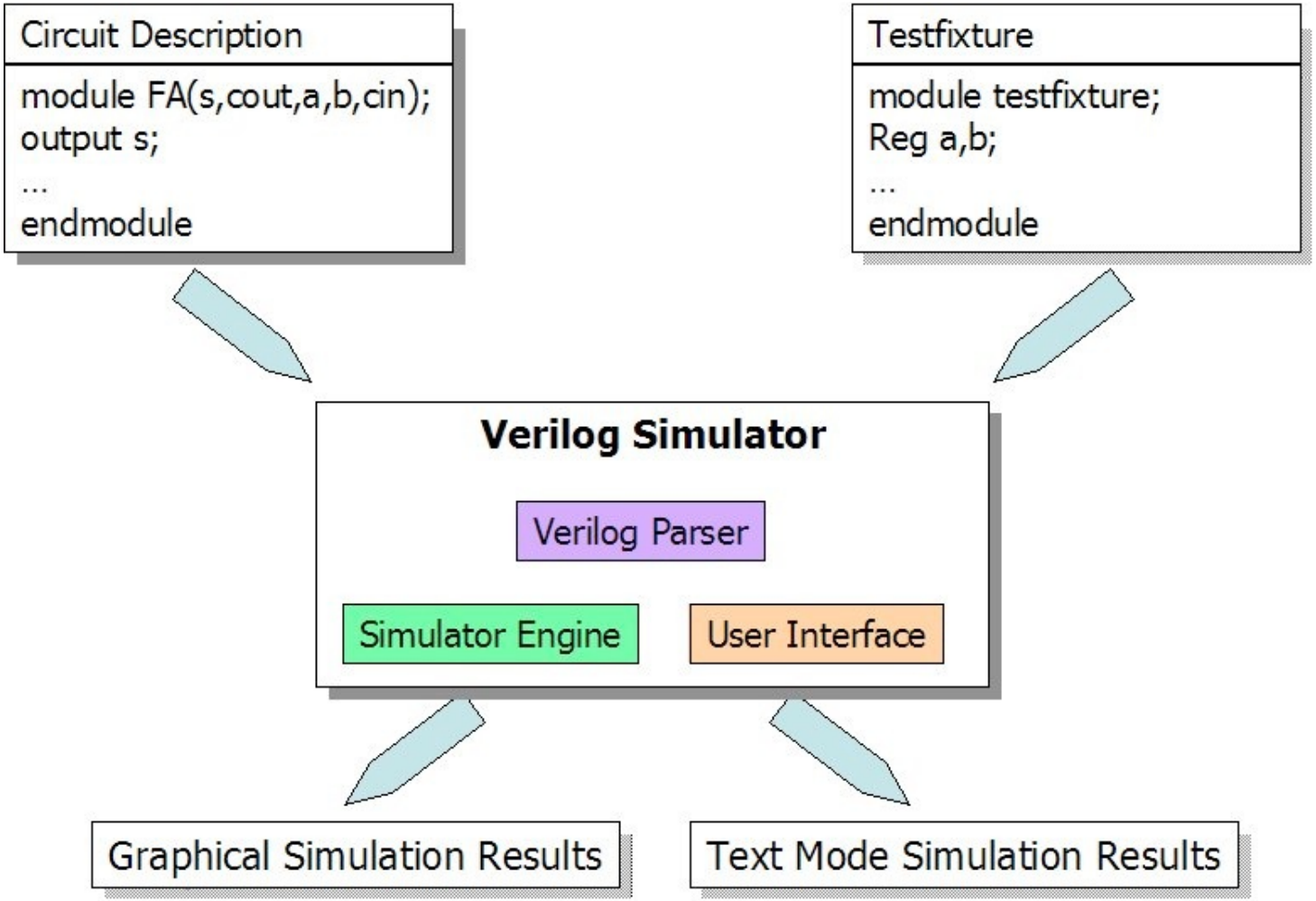
I/O definition

module instantiation

apply stimulus

```
module test_smux;

wire OUT;
reg A,B,SEL;

smux U0(.out(OUT),.a(A),.b(B),.sel(SEL));

initial
begin
  A=0;B=0;SEL=0;
  #10 A=0;B=0;SEL=1;
  #10 A=0;B=1;SEL=0;
  #10 A=0;B=1;SEL=1;
  #10 A=1;B=0;SEL=0;
  #10 A=1;B=0;SEL=1;
  #10 A=1;B=1;SEL=0;
  #10 A=1;B=1;SEL=1;
end

endmodule
```

Verilog Simulation



Event Simulation of a Verilog Model

- Compilation
  - Compilation and elaboration
- Initialization
  - Initialize module parameters
    - Set other storage element to unknown (X) state
      - Unknown or un-initialized
    - Set undriven nets to the high-impedance (Z) state
      - Tri-state or floating
- Simulation

Example 1 (1/3)

$$f_1 = x'y'z + xy'z' + xyz$$
$$= m_1 + m_4 + m_7 = \sum(1,4,7)$$

x	y	z	f_1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

- Module definition

```
module exp1(f1, x, y, z);
output f1;
input x,y,z;

assign f1 = ((~x)&(~y)&z) | (x&(~y)&(~z) | x&y&z);

endmodule
```

Example 1 (2/3)

- Testbench

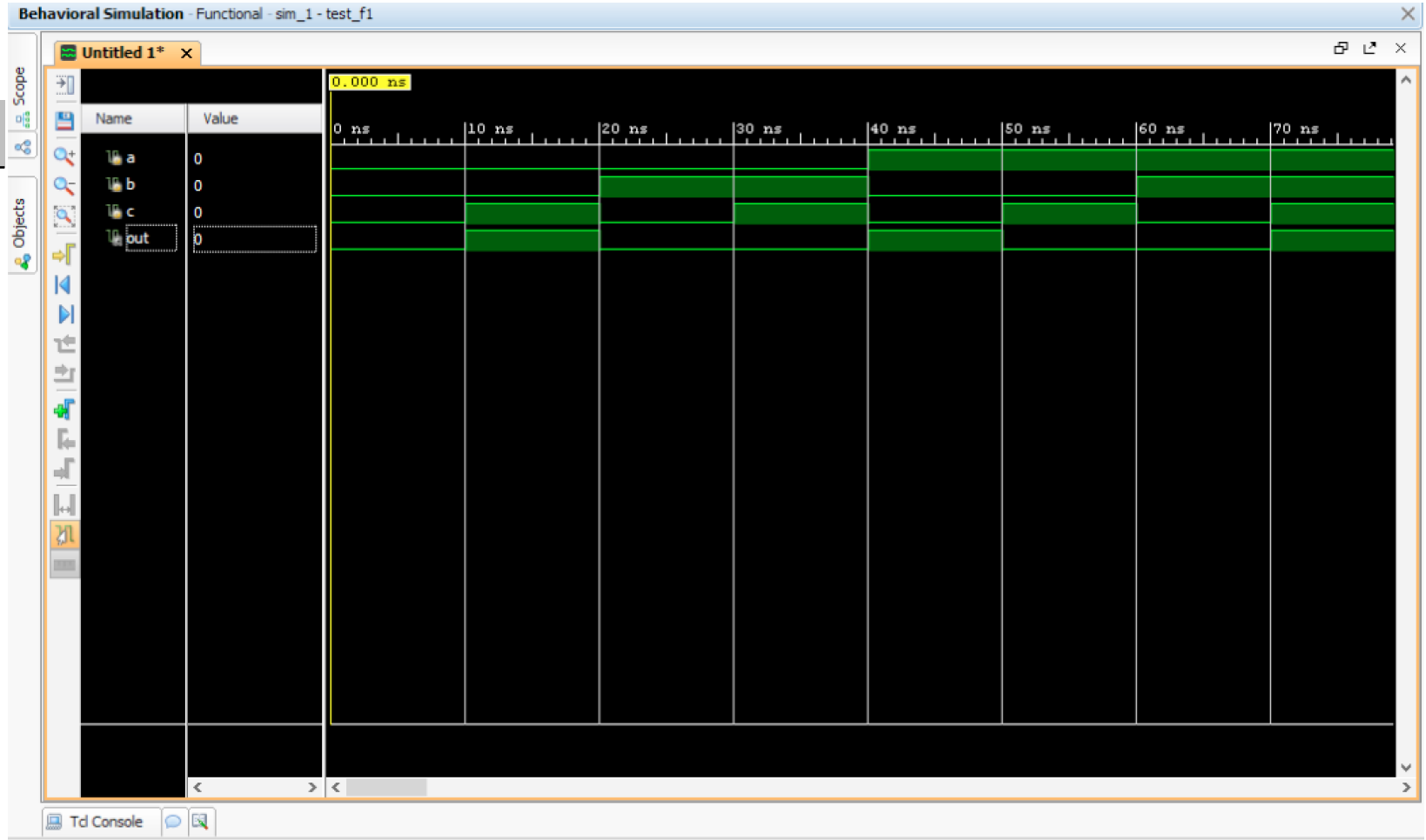
```
module test_f1;
wire out;
reg a,b,c;

exp1 U0(.f1(out),.x(a),.y(b),.z(c));

initial
begin
  a=0;b=0;c=0;
  #10 a=0;b=0;c=1;
  #10 a=0;b=1;c=0;
  #10 a=0;b=1;c=1;
  #10 a=1;b=0;c=0;
  #10 a=1;b=0;c=1;
  #10 a=1;b=1;c=0;
  #10 a=1;b=1;c=1;
end

endmodule
```

x	y	z	f_1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Example (3/3)

- Simulation Results

x	y	z	f_1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



Example 2 (1/3)

$$
\begin{aligned}
f_2 &= x'yz + xy'z + xyz' + xyz \\
&= m_3 + m_5 + m_6 + m_7 = \sum(3,5,6,7)
\end{aligned}
$$

x	y	z	f_2
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

- Module definition

```
module exp2(f2, x, y, z);
output f2;
input x,y,z;

assign f2 = ((~x)&y&z) | (x&(~y)&z) |( x&y&(~z))| (x&y&z);

endmodule
```

Example 1 (2/3)

- Testbench

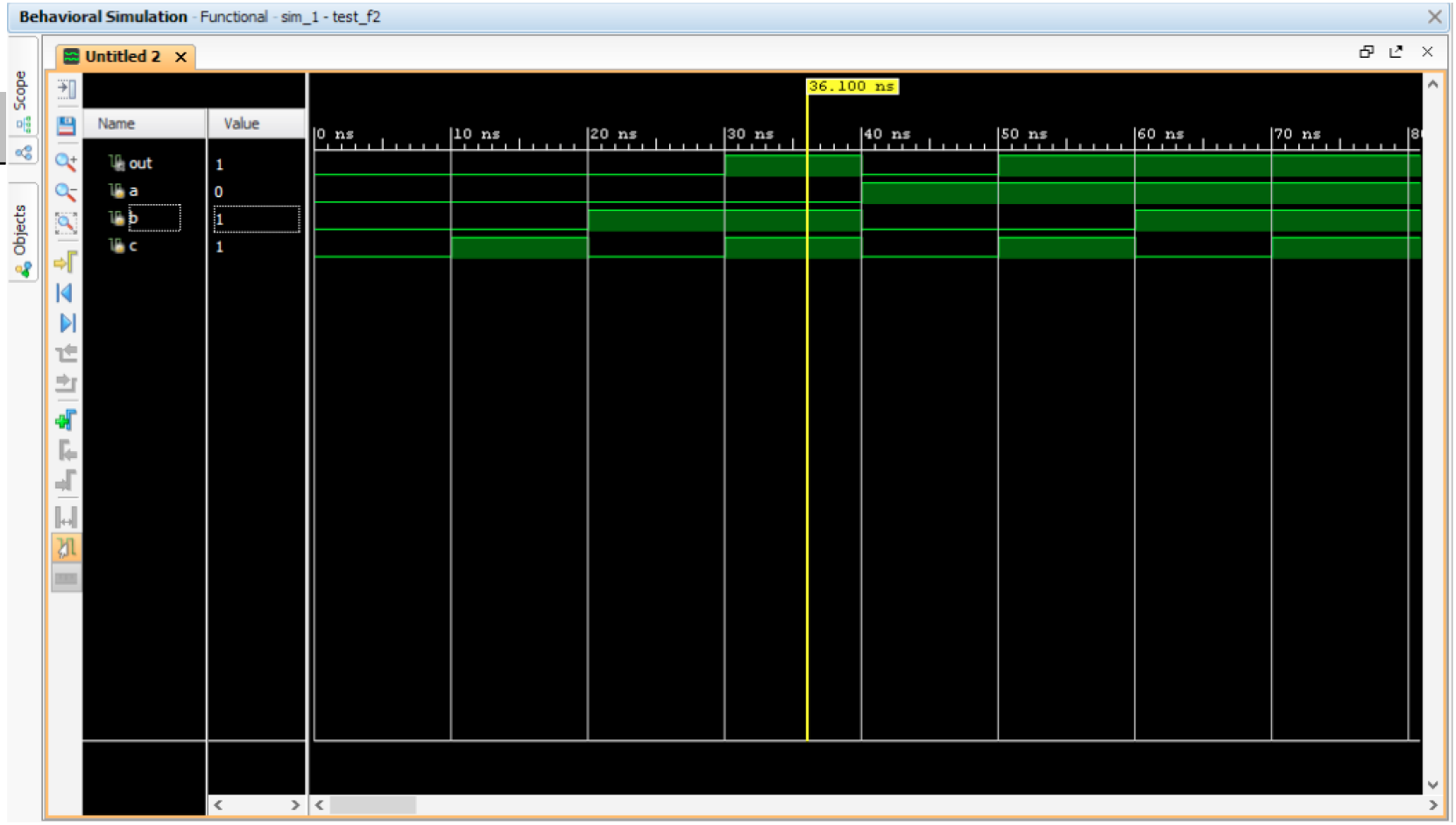
```
module test_f2;
wire out;
reg a,b,c;

exp2 U0(.f2(out),.x(a),.y(b),.z(c));

initial
begin
  a=0;b=0;c=0;
  #10 a=0;b=0;c=1;
  #10 a=0;b=1;c=0;
  #10 a=0;b=1;c=1;
  #10 a=1;b=0;c=0;
  #10 a=1;b=0;c=1;
  #10 a=1;b=1;c=0;
  #10 a=1;b=1;c=1;
end

endmodule
```

x	y	z	f_2
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Example (3/3)

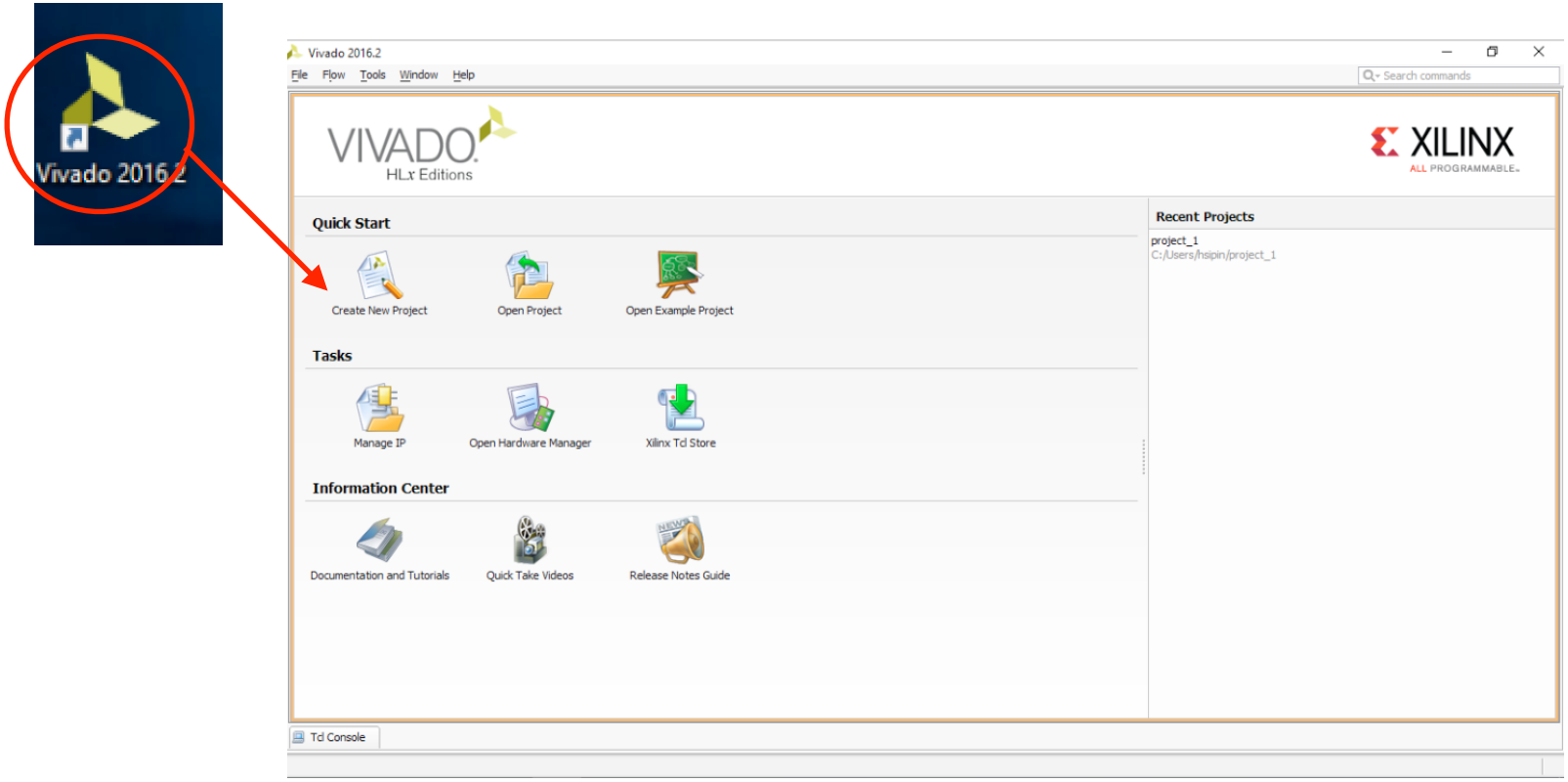
- Simulation Results

x	y	z	f_2
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



Logic Modeling and Simulation Using Xilinx Vivado

Open Vivado


Vivado 2016.2
Vivado 2016.2
File Flow Tools Window Help
Search commands
VIVADO
HLx Editions
XILINX
ALL PROGRAMMABLE.
Quick Start
Create New Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
Xilinx Tcl Store
Information Center
Documentation and Tutorials
Quick Take Videos
Release Notes Guide
Recent Projects
project_1
C:/Users/hsipin/project_1
Tcl Console

Open New Project (1/3)

Vivado 2016.2

File Flow Tools Window Help

VIVADO HLx Editions

Double Click

Quick Start

Create New Project | Open Project | Open Example Project

Tasks

Manage IP | Open Hardware Manager | Xilinx Tcl Store

Information Center

Documentation and Tutorials | Quick Take Videos | Release Notes Guide

Tcl Console

New Project

Create a New Vivado Project

This wizard will guide you through the creation of a new project.

To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a

New Project

Project Name

Enter a name for your project and specify a directory where the project data

Project name: smux

Project location: C:/Users/hsipin

☑ Create project subdirectory

Project will be created at: C:/Users/hsipin/smux

Open New Project (2/3)

New Project

Project Type

Specify the type of project to create.

- RTL Project
  You will be able to add sources, create block designs i
  and analysis.
  - Do not specify sources at this time
- Post-synthesis Project: You will be able to add sources
  - Do not specify sources at this time
- I/O Planning Project
  Do not specify design s
- Imported Project
  Create a Vivado projec
- Example Project
  Create a new Vivado p

?

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: Parts Boards

Filter

Product category:	All	Speed grade:	All
Family:	All	Temp grade:	All
Package:	All		

Reset All Filters

New Project

VIVADO HLx Editions

New Project Summary

A new RTL project named 'smux' will be created.

The default part and product family for the new project:
Default Part: xc7k70tfbv676-1
Product: Kintex-7
Family: Kintex-7
Package: fbv676
Speed Grade: -1

Finish

Transceivers	Available IOBs
	300
	300
	285
	300
	285
	300
	285
	285
	285

xt > Finish

Open New Project (3/3)

smux - [C:/Users/hsipin/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Help

Search commands

Default Layout

Ready

Flow Navigator

- **Project Manager**
  - Project Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP Integrator
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- Simulation
  - Simulation Settings
  - Run Simulation
- RTL Analysis
  - Elaboration Settings
  - Open Elaborated Design
- Synthesis
  - Synthesis Settings
  - Run Synthesis
  - Open Synthesized Desig
- Implementation
  - Implementation Settings
  - Run Implementation
  - Open Implemented Desig

Project Manager - smux

Sources

- Design Sources
- Constraints
- Simulation Sources
  - sim_1

Hierarchy | Libraries | Compile Order

Properties

Select an object to see properties

Project Summary

Project Settings Edit

Project name:	smux
Project location:	C:/Users/hsipin/smux
Product family:	Kintex-7
Project part:	xc7k70tfbv676-1
Top module name:	Not defined
Target language:	Verilog
Simulator language:	Mixed

Synthesis

Status:	Not started
Messages:	No errors or warnings
Part:	xc7k70tfbv676-1
Strategy:	Vivado Synthesis Defaults

Implementation

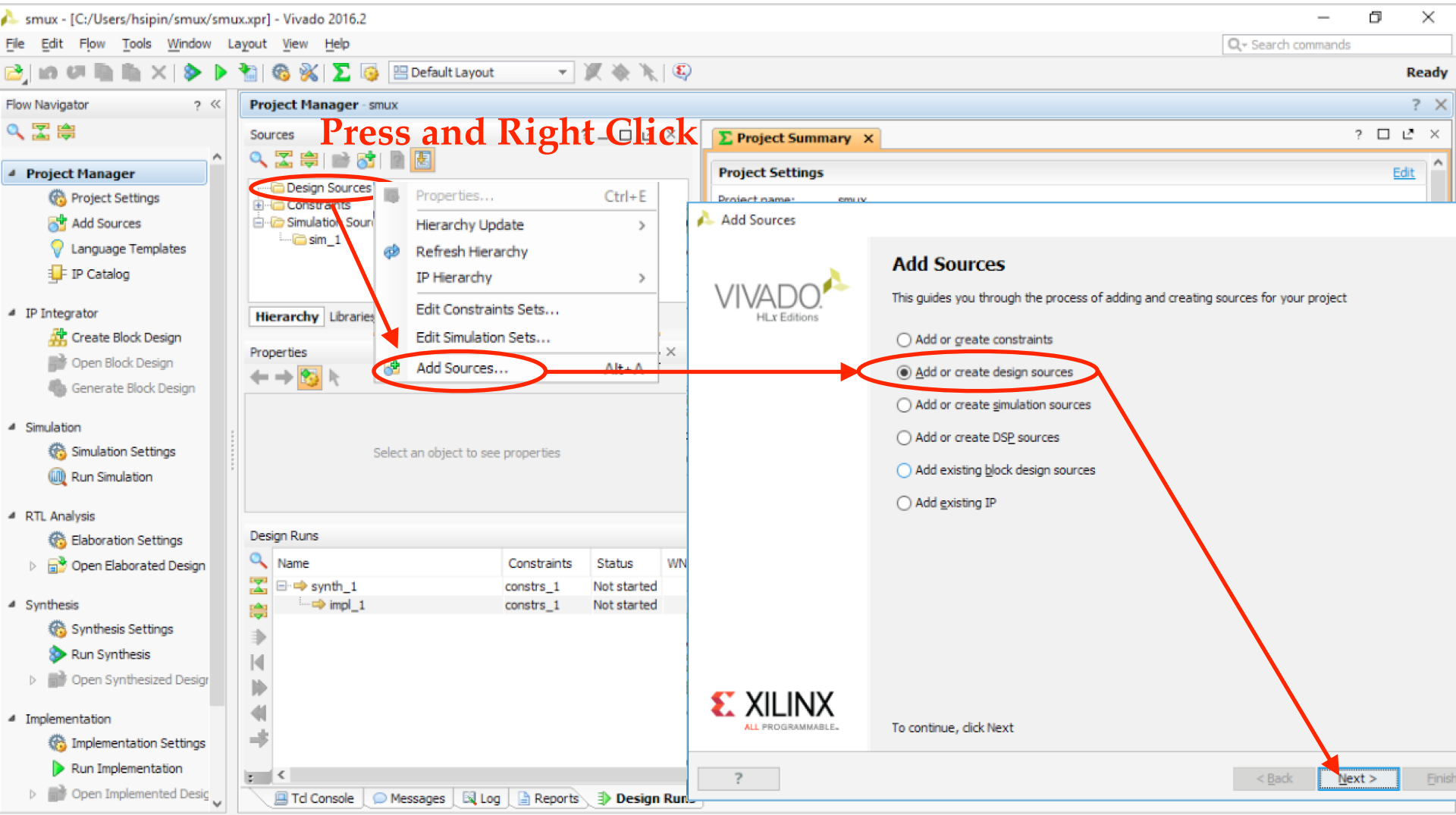
Status:	Not started
Messages:	No errors or warnings
Part:	xc7k70tfbv676-1
Strategy:	Vivado Implementation Defaults

Design Runs

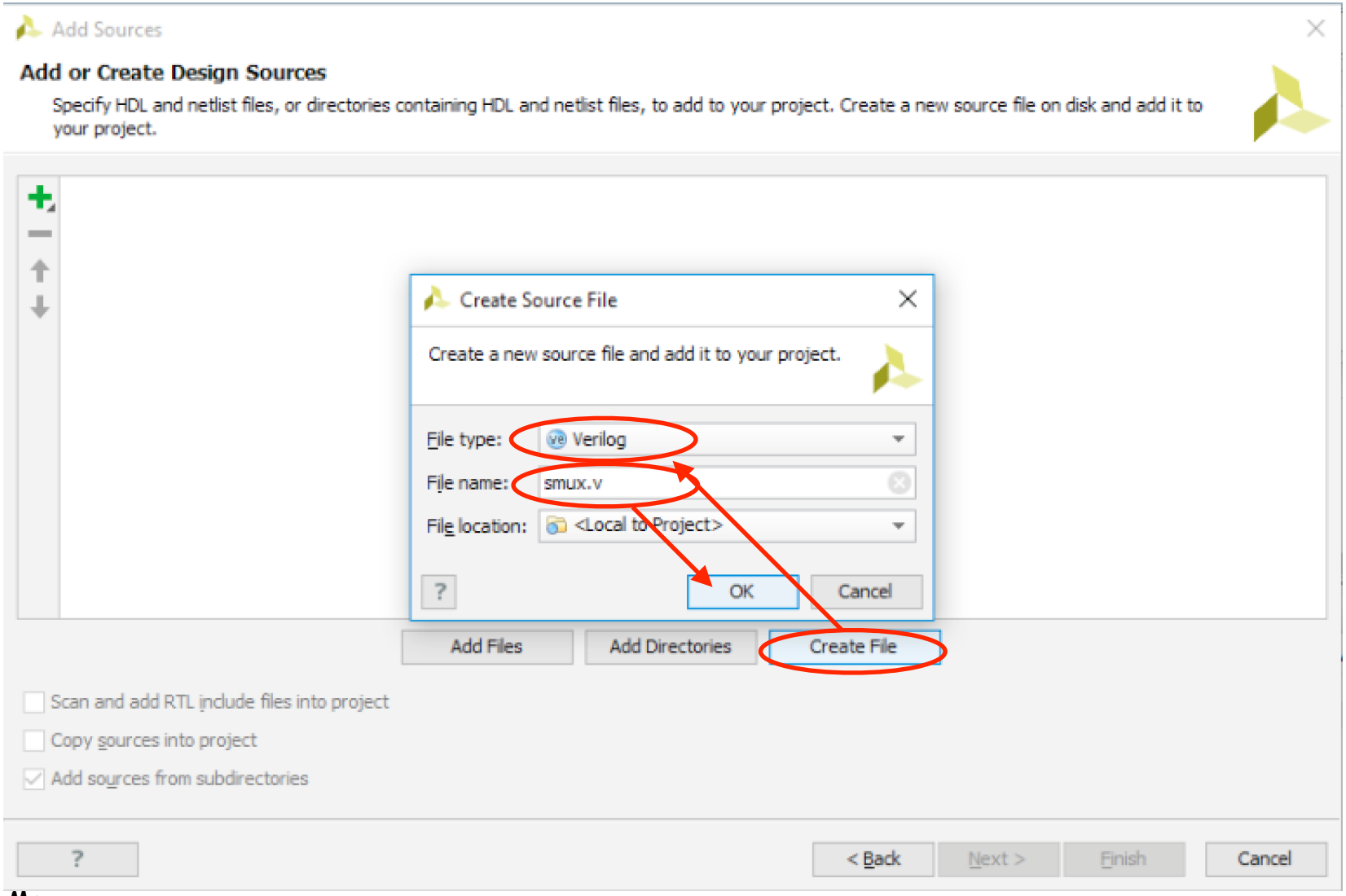
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed
synth_1	constrs_1	Not started													
impl_1	constrs_1	Not started													

Tcl Console | Messages | Log | Reports | Design Runs

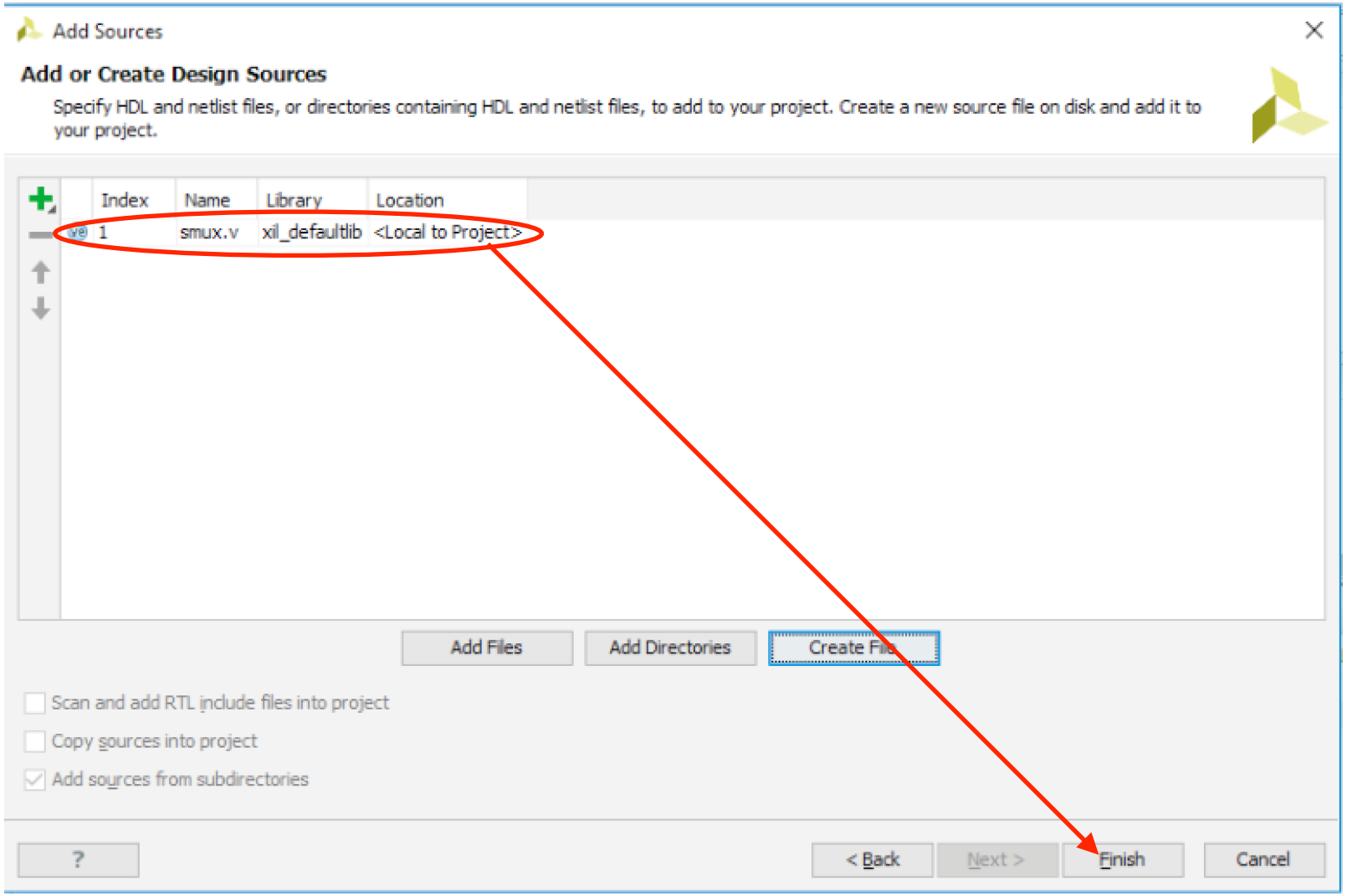
New Source (1/6)



New Source (2/6)



New Source (3/6)



New Source (4/6)

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Module name: smux

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
a	input	☐	0	0
b	input	☐	0	0
c	input	☐	0	0
out	input	☐	0	0

input
output
inout

OK Cancel

New Source (5/6)

smux - [C:/Users/hsipin/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Help

Flow Navigator

Project Manager

Project Settings

Add Sources

Language Templates

IP Catalog

IP Integrator

Create Block Design

Open Block Design

Generate Block Design

Simulation

Simulation Settings

RTL Analys

Synthesis

Implementa

Project Manager - smux

Sources

Design Sources (1)

smux (smux.v)

Constraints

Simulation Sources (1)

Hierarchy Libraries Compile Order

Source File Properties

smux.v

Enabled

press and double click

Project Summary smux.v

C:/Users/hsipin/smux/smux.srcs/sources_1/new/smux.v

```
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ////////////////////////////////////////////////////////////////////////////////
21
22
23 module smux(
24     input a,
25     input b,
26     input c,
27     output out
28     );
29 endmodule
```

Project Summary smux.v *

C:/Users/hsipin/smux/smux.srcs/sources_1/new/smux.v

```
18 // Additional Comments:
19 //
20 ////////////////////////////////////////////////////////////////////////////////
21
22
23 module smux(
24     input a,
25     input b,
26     input c,
27     output out
28     );
29
30 assign out = (a&sel) | (b&(~sel));
31
32 endmodule
33
```

THS TPWS Failed Routes LUT FF BRAM URAM DSP Start Elapsed

23:0 Insert Verilog

New Source (6/6)

smux - [C:/Users/hsipin/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Help

- New Project...
- Open Project...
- Open Recent Project
- Open Example Project...
- Save Project As...
- Write Project Tcl...
- Archive Project...
- Close Project
- Open Checkpoint...
- Open Recent Checkpoint
- Write Checkpoint...
- New IP Location...
- Open IP Location...
- Open Recent IP Location
- New File...
- Open File... Ctrl+O
- Open Recent File
- Open IP-XACT File...
- Save File Ctrl+S
- Save File As...
- Save All Files...
- Add Sources... Alt+A
- Open Source File... Ctrl+N
- Import
- Export
- Launch SDK
- Open Log File
- Open Journal File
- Print... Ctrl+P
- Exit

Project Manager - smux

Design Sources (1)
smux (smux.v)
Constraints
Simulation Sources (1)
sim_1 (1)

Hierarchy Libraries Compile Order

Source File Properties
smux.v
Enabled
Location: C:/Users/hsipin/smux/smux.srcs/sources_1/new
General Properties

Project Summary | smux.v *

C:/Users/hsipin/smux/smux.srcs/sources_1/new/smux.v

```
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////


module smux(
    input a,
    input b,
    input c,
    output out
    );

assign out = (a&sel) | (b&(~sel));

endmodule
```

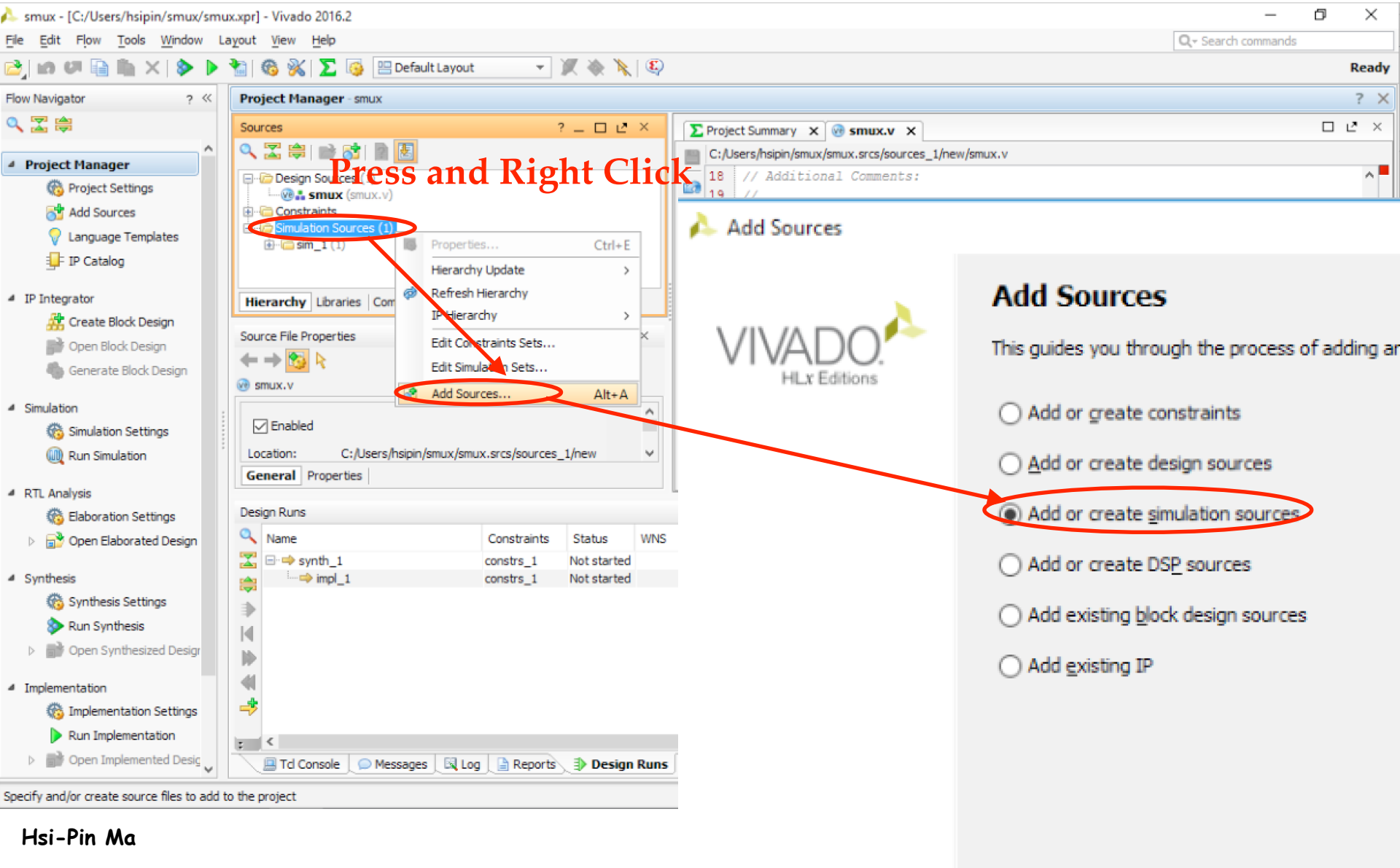
Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed
synth_1	constrs_1	Not started													
impl_1	constrs_1	Not started													

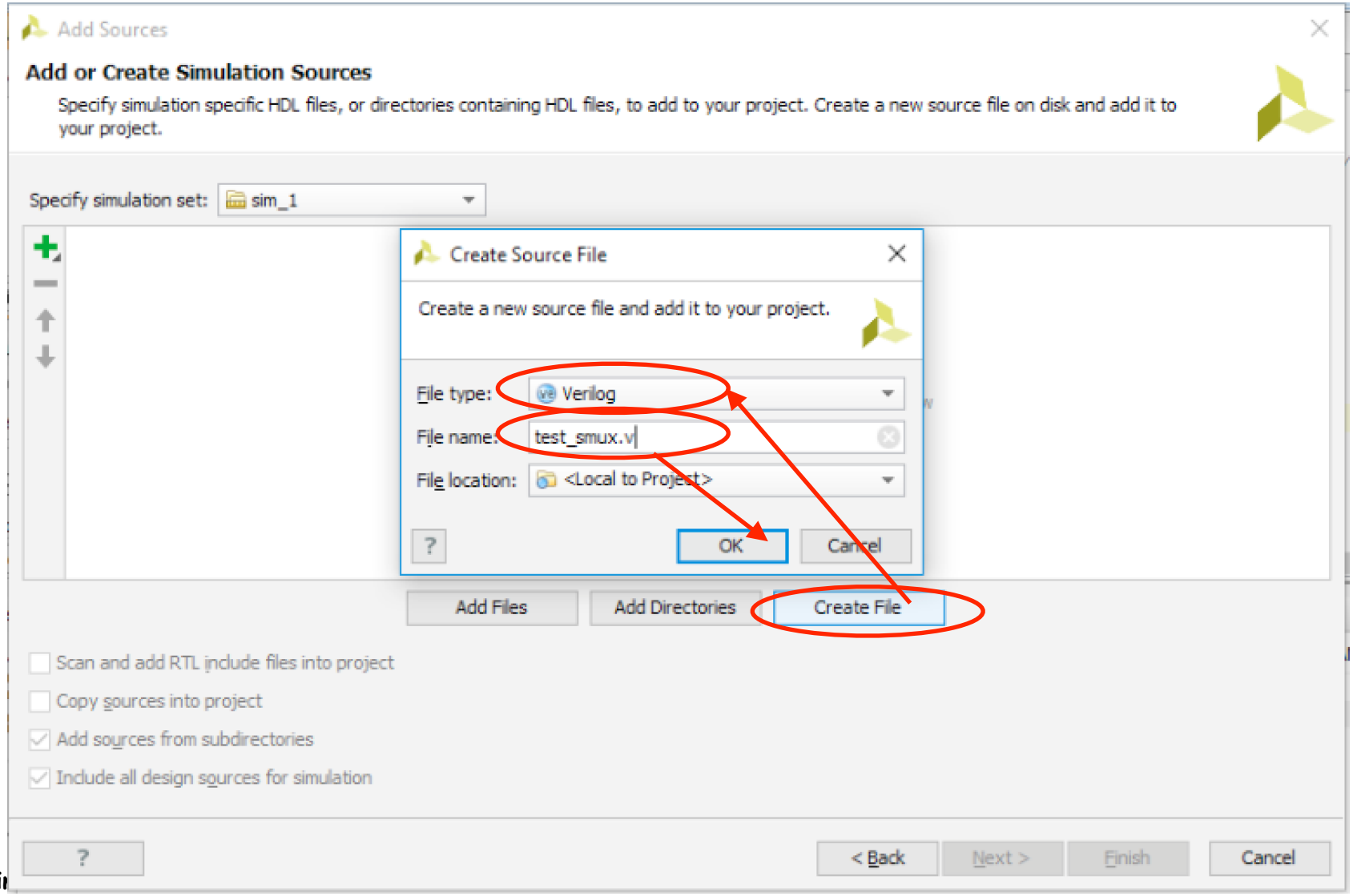
Tcl Console | Messages | Log | Reports | Design Runs

Remember to save files

Add Testbench (1/5)



Add Testbench (2/5)



Add Testbench (3/5)

Add Sources

Add or Create Simulation Sources

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set: sim_1

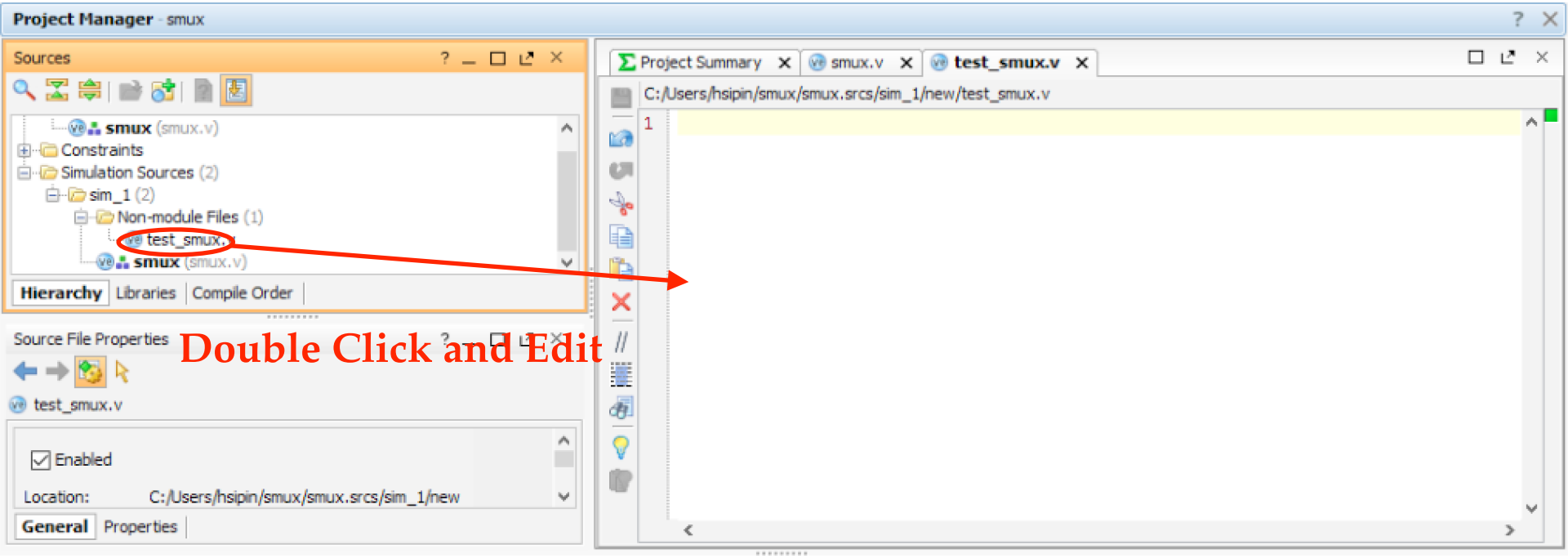
Index	Name	Library	Location
1	test_smux.v	xil_defaultlib	<Local to Project>

Add Files | Add Directories | Create File

- [ ] Scan and add RTL include files into project
- [ ] Copy sources into project
- [x] Add sources from subdirectories
- [x] Include all design sources for simulation

? | < Back | Next > | Finish | Cancel

Add Testbench (4/5)



Add Testbench (5/5)

smux - [C:/Users/hsipin/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Help

Sources

- Design Sources (1)
  - smux (smux.v)
- Constraints
- Simulation Sources (1)
  - sim_1 (1)
    - test_smux (test_smux.v) (1)
      - U0 - smux (smux.v)

Hierarchy | Libraries | Compile Order

C:/Users/hsipin/smux/smux.srcs/sim_1/new/test_smux.v

```
1  module test_smux;
2  wire OUT;
3  reg A,B,SEL;
4
5  smux U0(.out(OUT),.a(A),.b(B),.sel(SEL));
6
7  initial
8  begin
9    A=0;B=0;SEL=0;
10   #10 A=0;B=0;SEL=1;
11   #10 A=0;B=1;SEL=0;
12   #10 A=0;B=1;SEL=1;
13   #10 A=1;B=0;SEL=0;
14   #10 A=1;B=0;SEL=1;
15   #10 A=1;B=1;SEL=0;
16   #10 A=1;B=1;SEL=1;
```

Put your testbench here

Simulation (1/4)

smux - [C:/Users/hsipin/LD/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Run Help

Flow Navigator

- Project Manager
  - Project Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP Integrator
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- Simulation
  - Simulation Settings
  - Run Simulation
- RTL Analysis
  - Elaboration S
  - Open Elabora
- Synthesis
  - Synthesis Settings
  - Run Synthesis
  - Open Synthesized Desig
- Implementation
  - Implementation Settings
  - Run Implementation
  - Open Implemented Desig

Press and Select

Run Behavioral Simulation
Run Post-Synthesis Functional Simulation
Run Post-Synthesis Timing Simulation
Run Post-Implementation Functional Simulation
Run Post-Implementation Timing Simulation

Behavioral Simulation - Functional - sim_1 - test_smux

Sources
- Design Sources (1)
  - smux (smux.v)
- Constraints
- Simulation Sources (1)
  - sim_1 (1)
    - test_smux (test_smux.v) (1)
      - U0 - smux (smux.v)

Objects

Name	Value	Data Typ
OUT	1	Logic
A	1	Logic
B	1	Logic
SEL	1	Logic

smux.v | test_smux.v

C:/Users/hsipin/LD/smux/smux.srcs/sim_1/new/test_smux.v

```
1  module test_smux;
2  wire OUT;
3  reg A,B,SEL;
4
5  smux U0(.out(OUT),.a(A),.b(B),.sel(SEL));
6
7  initial
8  begin
9    A=0;B=0;SEL=0;
10   #10 A=0;B=0;SEL=1;
11   #10 A=0;B=1;SEL=0;
12   #10 A=0;B=1;SEL=1;
13   #10 A=1;B=0;SEL=0;
14   #10 A=1;B=0;SEL=1;
15   #10 A=1;B=1;SEL=0;
16   #10 A=1;B=1;SEL=1;
17 end
18
19 endmodule
```

```
# run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_smux_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:03 ; elapsed = 00:00:12 . Memory (MB): peak = 780.797 ; gain = 10.039
```

Type a Tcl command here

Tcl Console | Messages | Log

Vivado Simulator

Simulation (2/4)

smux - [C:/Users/hsipin/LD/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Run Help

Press maximize

Flow Navigator

- Project Manager
  - Project Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP Integrator
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- Simulation
  - Simulation Settings
  - Run Simulation
- RTL Analysis
  - Elaboration Settings
  - Open Elaborated Design
- Synthesis
  - Synthesis Settings
  - Run Synthesis
  - Open Synthesized Design
- Implementation
  - Implementation Settings
  - Run Implementation
  - Open Implemented Design

Behavioral Simulation - Functional - sim_1 - test_smux

Scopes

Name	Design Unit	Block Type
test_smux	test_smux	Verilog Module
U0	smux	Verilog Module
glbl	glbl	Verilog Module

Objects

Name	Value	Data Typ
OUT	1	Logic
A	1	Logic
B	1	Logic
SEL	1	Logic

smux.v | test_smux.v | Untitled 2

Name	Value
OUT	1
A	1
B	1
SEL	1

/test_smux/SEL

Tcl Console

```
# }
# run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_smux_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:06 . Memory (MB): peak = 799.906 ; gain = 0.000
```

Type a Tcl command here

Tcl Console | Messages | Log

Sim Time: 1 us

Simulation (3/4)

Behavioral Simulation - Functional - sim_1 - test_smux

smux.v | test_smux.v | Untitled 2

Scope | Objects

Name	Value
OUT	1
A	1
B	1
SEL	1

1,000,000 ps

1,000,000 ps | 1,000,001 ps | 1,000,002 ps | 1,000,003 ps

Use these to zoom in or zoom out

Tcl Console

Scroll this to the beginning

Simulation (4/4)

smux - [C:/Users/hsipin/LD/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Run Help

Flow Navigator

- Project Manager
  - Project Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP Integrator
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- Simulation
  - Simulation Settings
  - Run Simulation
- RTL Analysis
  - Elaboration Settings
  - Open Elaborated Design
- Synthesis
  - Synthesis Settings
  - Run Synthesis
  - Open Synthesized Design
- Implementation
  - Implementation Settings
  - Run Implementation
  - Open Implemented Design

Behavioral Simulation - Functional - sim_1 - test_smux

smux.v | test_smux.v | Untitled 2

Name	Value
OUT	0
A	0
B	0
SEL	0

0.000 ns

0 ns, 20 ns, 40 ns, 60 ns, 80 ns, 100 ns, 120 ns

Tcl Console

Sim Time: 1 us