

# HW4

1. (20%) Design a combinational circuit with three inputs, x (MSB), y, and z (LSB), and three outputs, A (MSB), B, and C (LSB). When the binary input is 0, 1, 2, or 3, the binary output is three greater than the input ( $xyz=001$  (1)  $\Rightarrow ABC=100$  (4),  $xyz=011$  (3)  $\Rightarrow ABC=110$  (6)). When the binary input is 4, 5, 6, or 7, the binary output is two less than the input ( $xyz=110$  (6)  $\Rightarrow ABC=100$  (4),  $xyz=100$  (4)  $\Rightarrow ABC=010$  (2)).

(a) Derive the truth table. (5%)

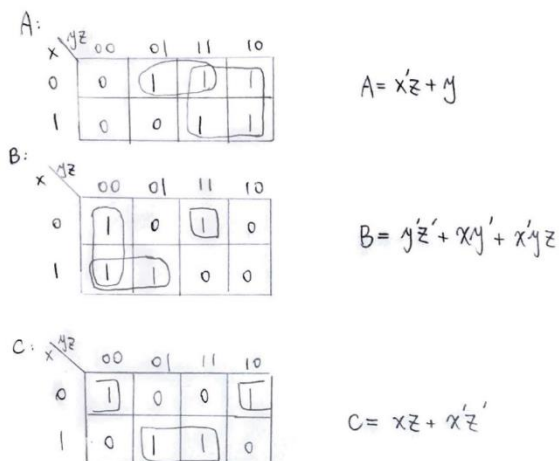
(b) Derive the simplified Boolean expressions for A, B, and C using maps. (10%)

(c) Draw the related logic diagram. (5%)

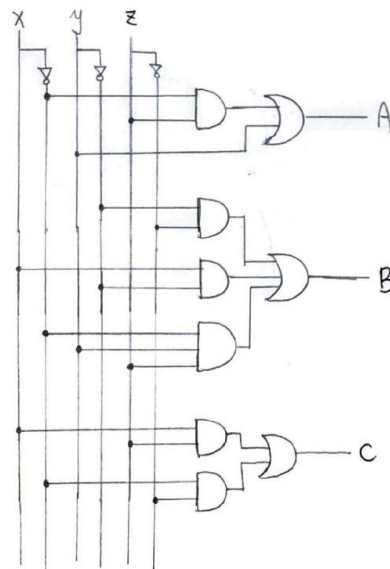
(a)

x	y	z	A	B	C
0	0	0	0	1	1
0	0	1	1	0	0
0	1	0	1	0	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	1	0	0
1	1	1	1	0	1

(b)



(c)



2. (10%) Design an excess-3-to-binary decoder using the unused combinations of the code as don't-care conditions.

e0	e1	e2	e3	b0	b1	b2	b3
0	0	0	0	x	x	x	x
0	0	0	1	x	x	x	x
0	0	1	0	x	x	x	x
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

$e_2e_3$ $e_0e_1$	00	01	11	10
00	x	x	0	x
01	0	0	0	0
11	1	x	x	x
10	0	0	1	0

$$b_0 = e_0e_1 + e_0e_2e_3$$

$e_2e_3$ $e_0e_1$	00	01	11	10
00	x	x	0	x
01	0	0	1	0
11	0	x	x	x
10	1	1	0	1

$$b_1 = e_1'e_2' + e_1e_3e_3 + e_1'e_3'$$

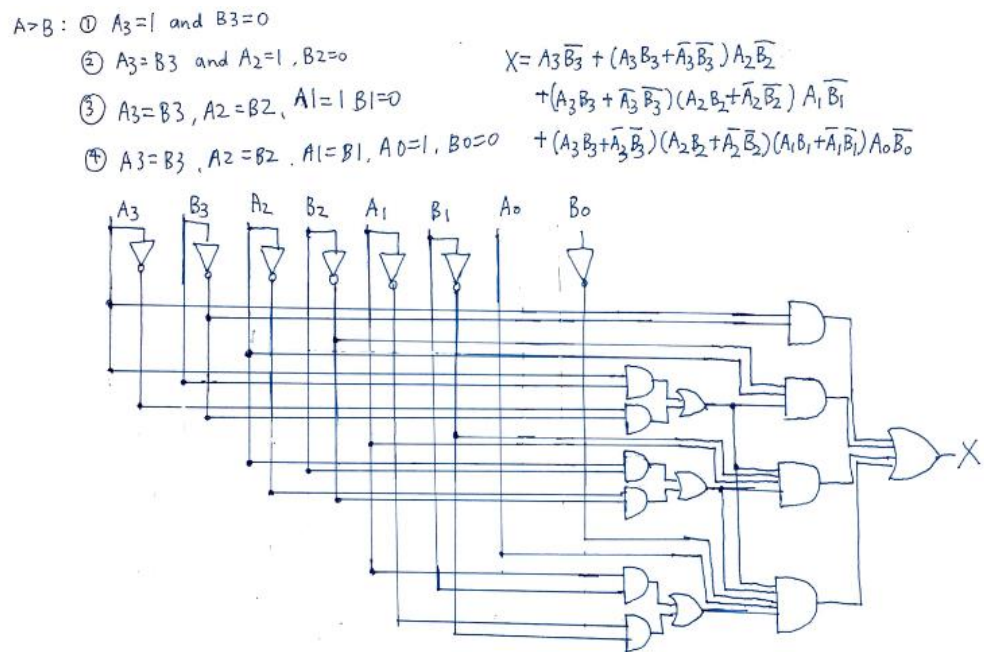
$e_2e_3$ $e_0e_1$	00	01	11	10
00	x	x	0	x
01	0	1	0	1
11	0	x	x	x
10	0	1	0	1

$$b_2 = e_2'e_3 + e_2e_3'$$

$e_2e_3$ $e_0e_1$	00	01	11	10
00	x	x	0	x
01	1	0	0	1
11	1	x	x	x
10	1	0	0	1

$$b_3 = e_3'$$

3. (10%) Design a combinational circuit that compares two 4-bit unsigned numbers A and B to see whether A is greater than B. The circuit has one output X, so that  $X = 0$  if  $A \leq B$  and  $X = 1$  if  $A > B$ .



4. (10%) Design a 3-bit absolute value calculator. ( $Z = |z|$ ).

以下提供兩種不同的做法供同學參考：

(I)

	$z_3$	$z_2$	$z_1$	$A_3$	$A_2$	$A_1$
0	0	0	0	0	0	0
1	0	0	1	0	0	1
2	0	1	0	0	1	0
3	0	1	1	0	1	1
-4	1	0	0	x	x	x
-3	1	0	1	0	1	1
-2	1	1	0	0	1	0
-1	1	1	1	0	0	1

$z_3 \backslash z_2$	00	01	11	10
0	0	0	0	0
1	x	0	0	0

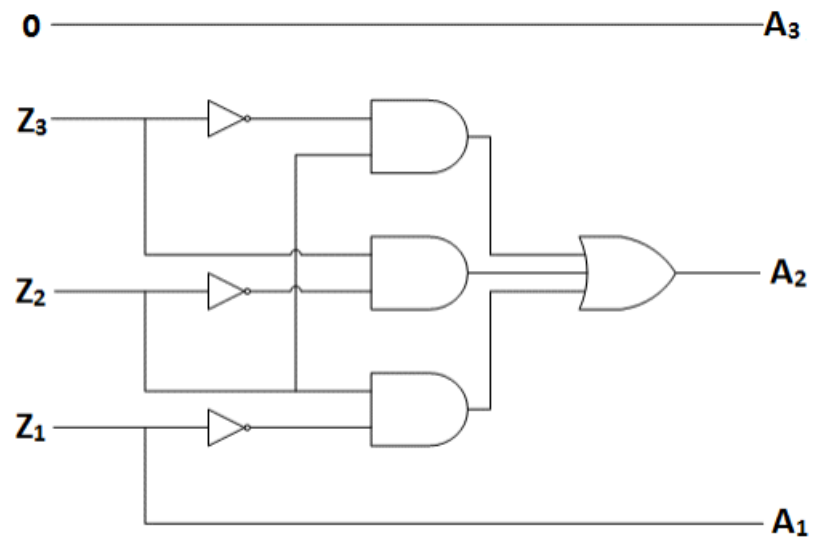
$A_3 = 0$

$z_3 \backslash z_2$	00	01	11	10
0	0	1	1	0
1	x	1	0	1

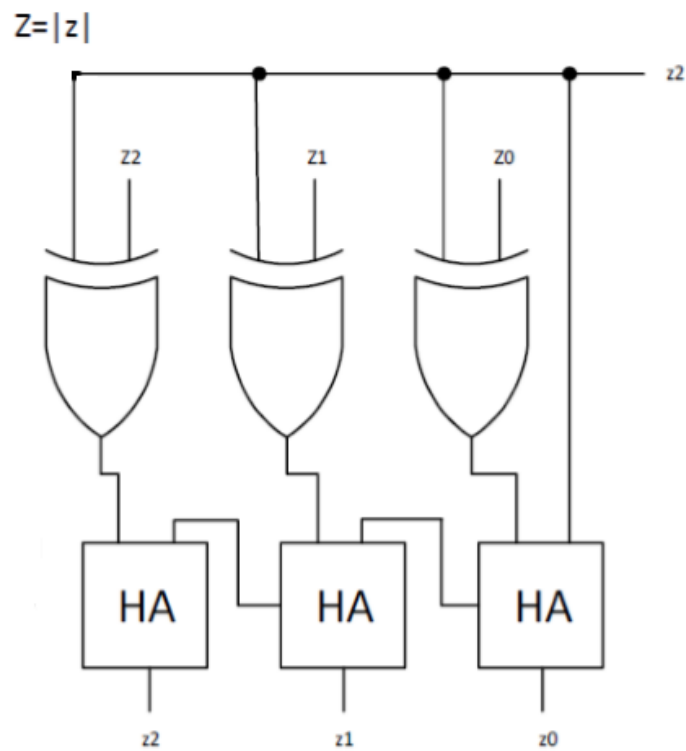
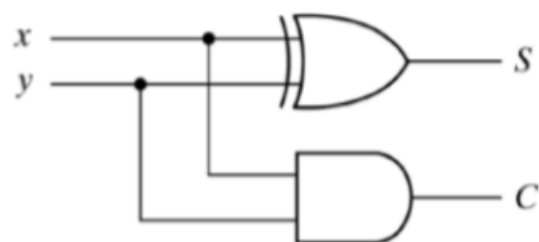
$A_2 = z_2 z_3' + z_1' z_3 + z_1' z_3$

$z_3 \backslash z_1$	00	01	11	10
0	0	0	1	1
1	x	0	1	1

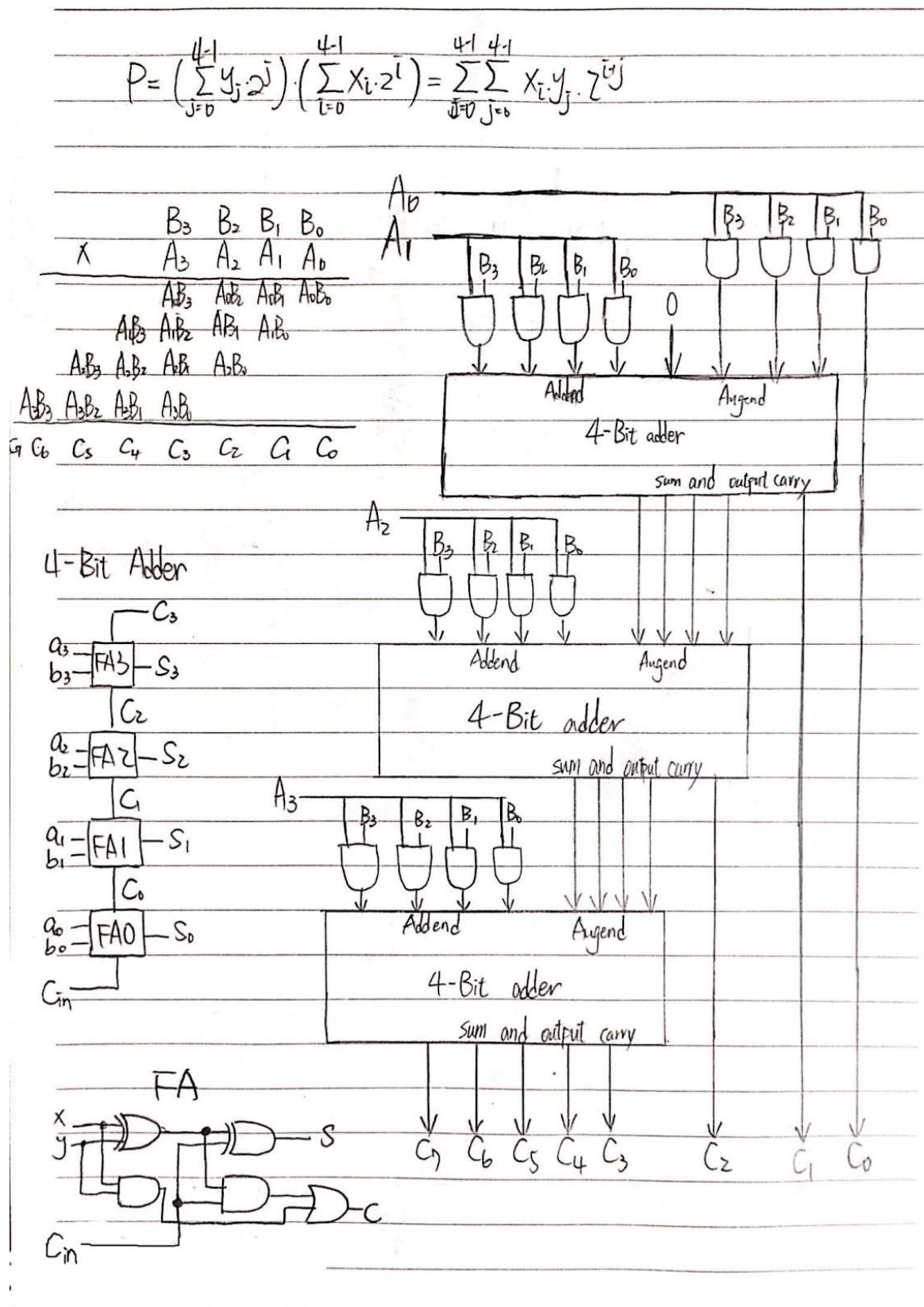
$A_1 = z_1$

**Logic Diagram**

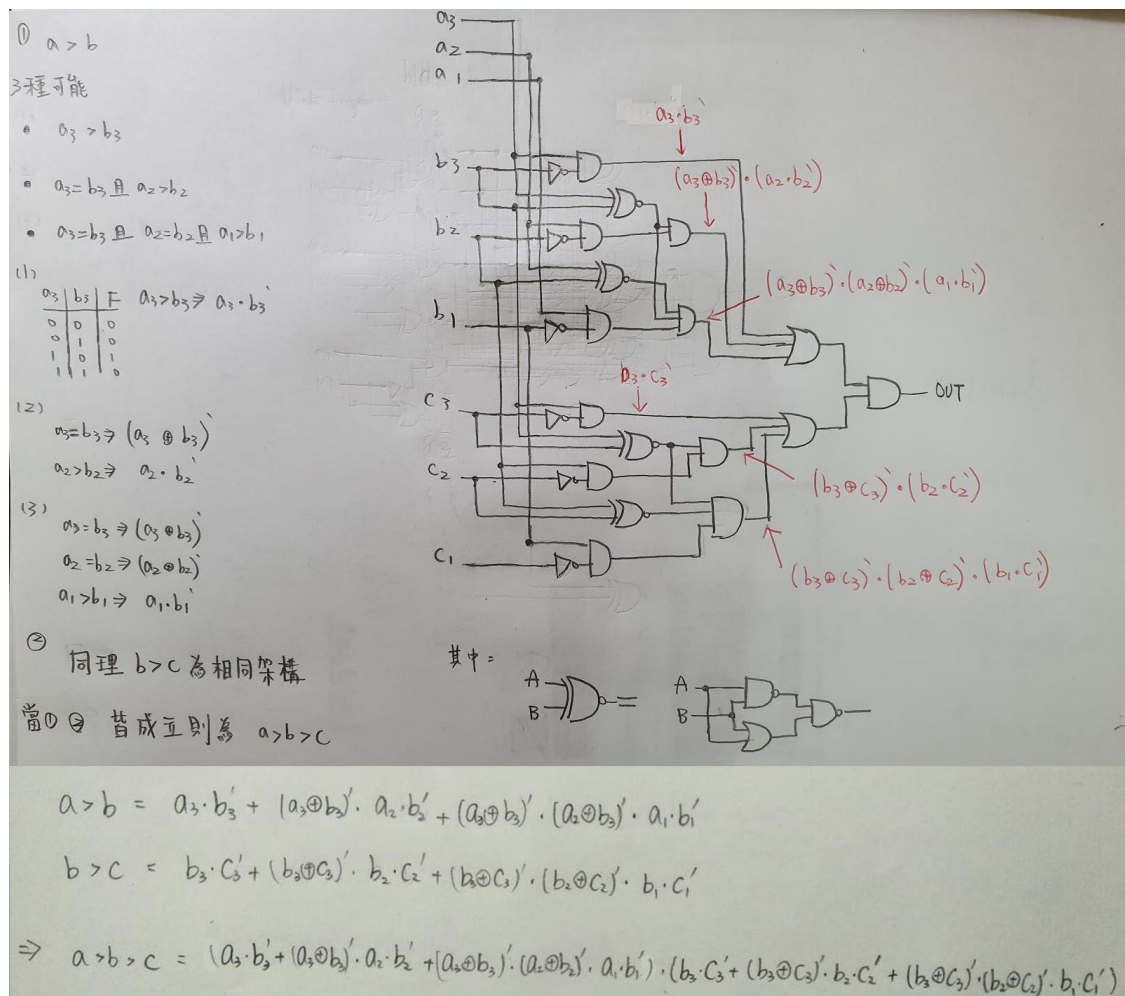
(II)

**Half adder**

5. (10%) Design a 4x4 multiplier using four-bit adders (Ripple-Carry adders) and other logic gates.



6. (20%) Design a three-way magnitude comparator that outputs true if its three inputs are in strict order:  $a > b > c$ .  $a$ ,  $b$ , and  $c$  are all three-bit unsigned numbers.





7. (10%) Design a 4→2 priority encoder with input D[3:0] and output A[1:0] where D<sub>0</sub> has the highest priority and D<sub>3</sub> has the lowest priority.

\* 本題需注意 valid (V) 為 priority encoder 的一部分，因此不能省略

7.

Inputs				Outputs		
D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	A <sub>1</sub>	A <sub>0</sub>	V
0	0	0	0	X	X	0
X	X	X	1	0	0	1
X	X	1	0	0	1	1
X	1	0	0	1	0	1
1	0	0	0	1	1	1

A<sub>1</sub>:

00	01	11	10
00	X		
01			
11			
10			

D<sub>3</sub> { 11, 10 } D<sub>2</sub> D<sub>0</sub>

A<sub>0</sub>:

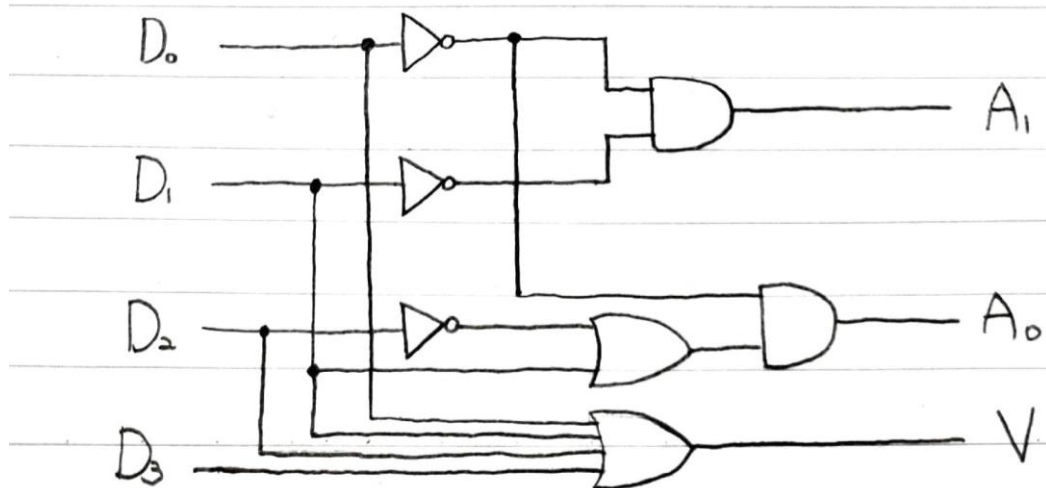
00	01	11	10
00	X		
01			
11			
10			

D<sub>3</sub> { 11, 10 } D<sub>2</sub> D<sub>0</sub>

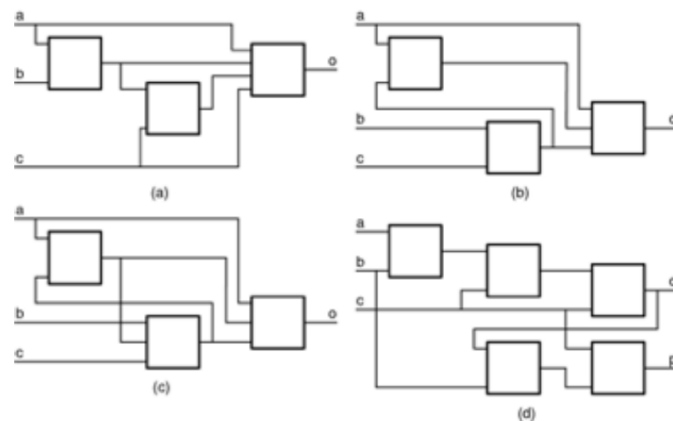
$$A_1 = D_1' D_0'$$

$$A_0 = D_1 D_0' + D_2' D_0' = D_0' (D_1 + D_2')$$

$$V = D_0 + D_1 + D_2 + D_3$$

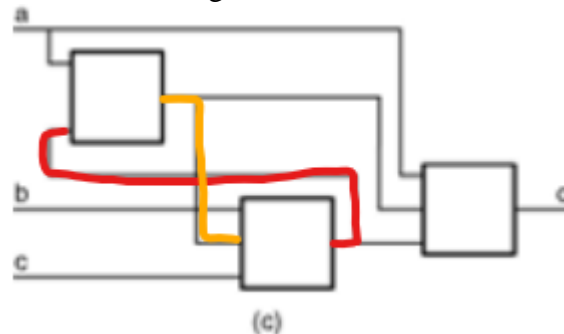


8. (10%) Which of the following circuits are combinational? Each box in the figure is itself a combinational circuit.



Ans : (a)(b)(d) are combinational.

參考老師上課講義 Combinational Logic P.6



(c) is a sequential logic circuit because the feedback variable can remember the history of the circuits .

(a)(b)(d) are combinational circuits whose outputs at any time are determined directly and only from the present input combination.