HW6

1. The content of a 4-bit shift register is initially 1011. The register is shifted five times to the left with the serial input 101110 (left bit is first input). What is the content of the register after *each shift*?

   initially :1011 input:101110

   shift 1 :0111

   shift 2 :1110

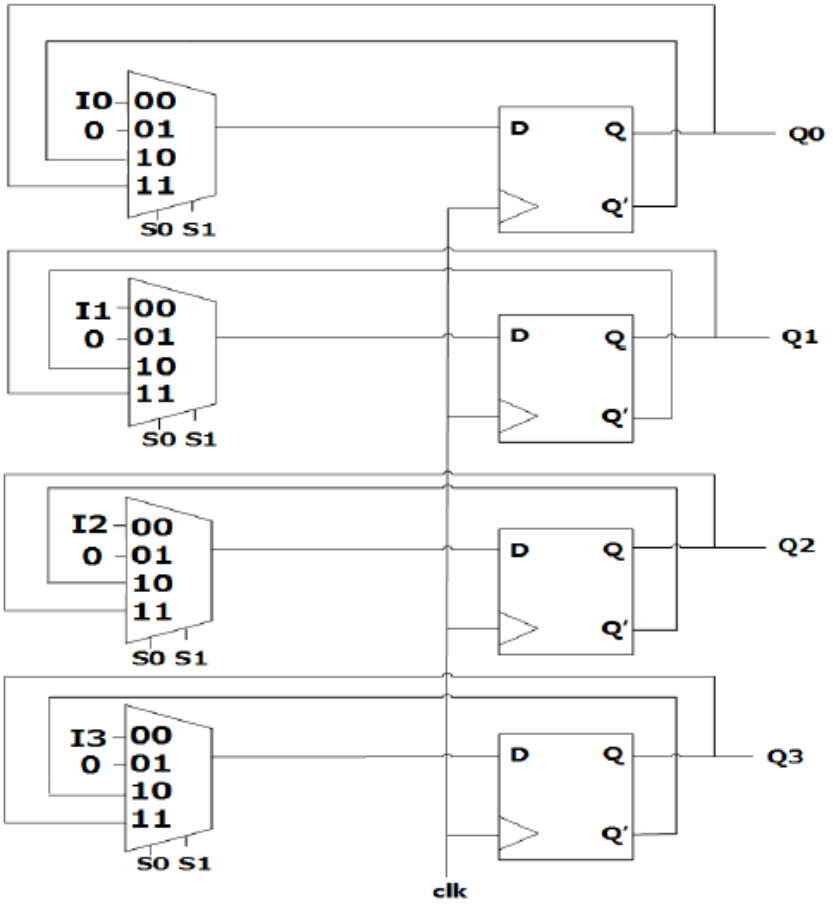
   shift 3 :1101

   shift 4 :1011

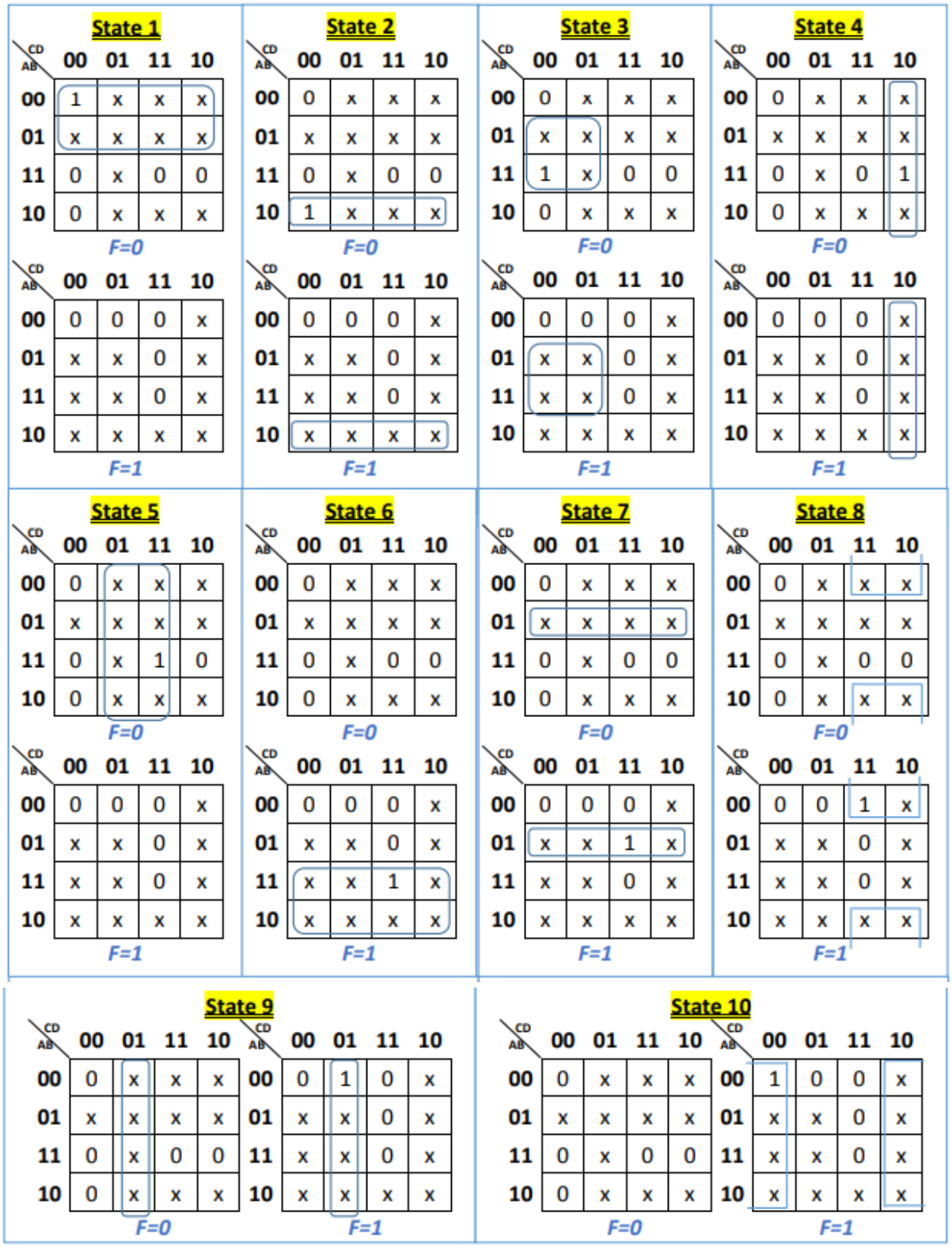
   shift 5 :0111

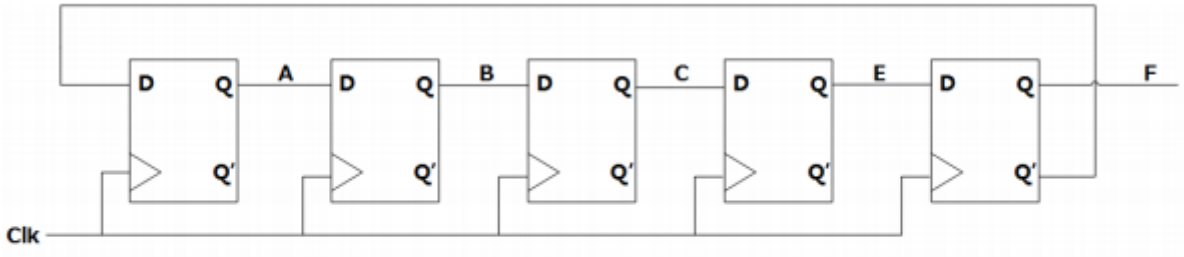
2. Draw the logic diagram of a four-bit register with four D flip-flops and four 4x1 multiplexers with mode selection S1 and S0. The register operates according to the following function table.

S1	S0	Register Operation
0	0	Load parallel data
0	1	Clear register to 0 (synchronous with the clock)
1	0	Complement the four outputs
1	1	No change



3. Show that a Johnson counter with n flip-flops produces a sequence of 2n states. List the 10 states produced with five flip-flops and the Boolean terms of each of the 10 AND gate outputs.

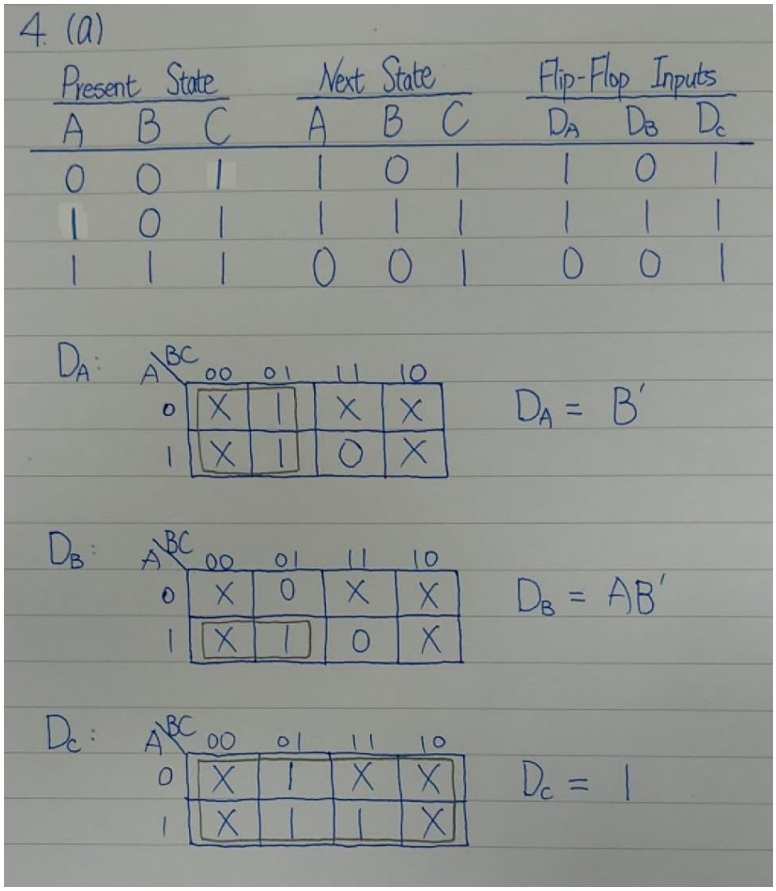




Sequence Number	A	B	C	E	F	AND gate for output
1	0	0	0	0	0	A'F'
2	1	0	0	0	0	AB'
3	1	1	0	0	0	BC'
4	1	1	1	0	0	CD'
5	1	1	1	1	0	DF'
6	1	1	1	1	1	AF
7	0	1	1	1	1	A'B
8	0	0	1	1	1	B'C
9	0	0	0	1	1	C'D
10	0	0	0	0	1	D'F

4. Use D flip-flops and gates to design a binary counter with each of the following repeated binary sequences:

   (a) 1, 5, 7



(b) 0, 2, 4, 6

Present state A	B	C	Next State A	B	C	Flip-Flop inputs D_A	D_B	D_C
0	0	0	0	1	0	0	1	0
0	1	0	1	0	0	1	0	0
1	0	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0	0

For D_A:

A \ BC	00	01	11	10
0	0	X	X	1
1	1	X	X	0

$D_A = AB' + A'B$

For D_B:

A \ BC	00	01	11	10
0	1	X	X	0
1	1	X	X	0

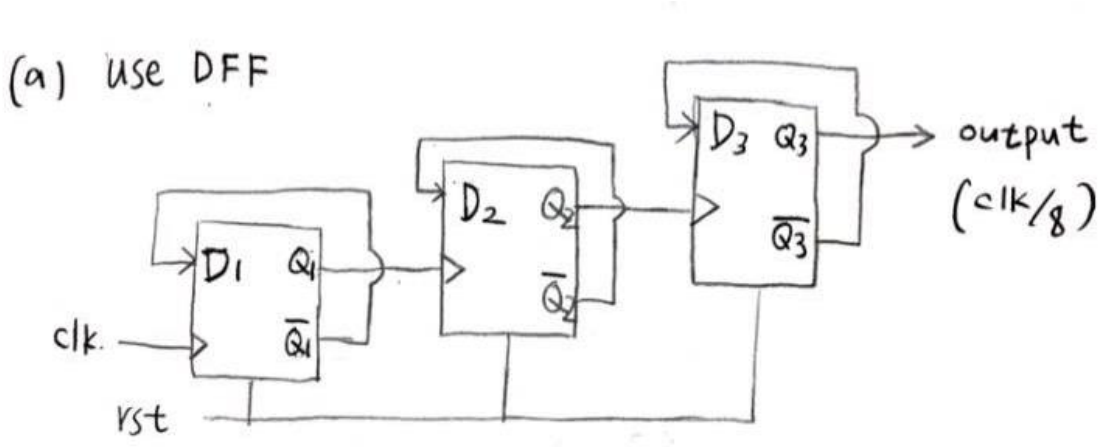
$D_B = B'$

For D_C:

A \ BC	00	01	11	10
0	0	X	X	0
1	0	X	X	0

$D_C = 0$

5. Frequency divider:
   (a) Design a frequency divider to provide the output signal with frequency as 1/8 of the that of the original signal.



(b) Design a frequency divider to provide the output signal with frequency as 1/6 of the that of the original signal.