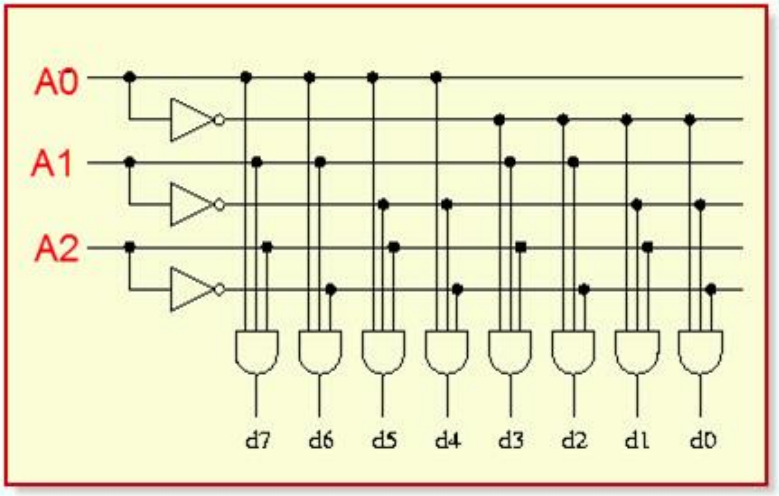
HW7

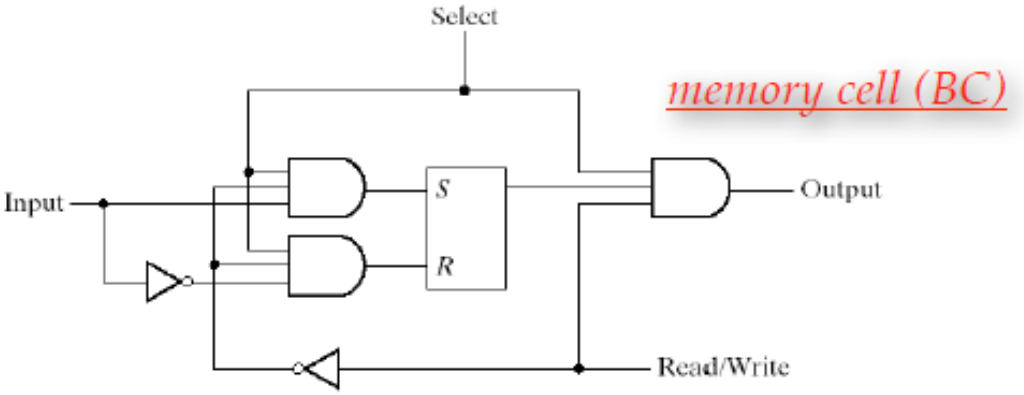
1. The memory units that follow are specified by the number of words times the number of bits per word. (1) How many address lines and input-output lines are needed in each case? (2) Give the number of bits stored in the memories in each case. (a) 2M x 16 (b) 2G x 8.

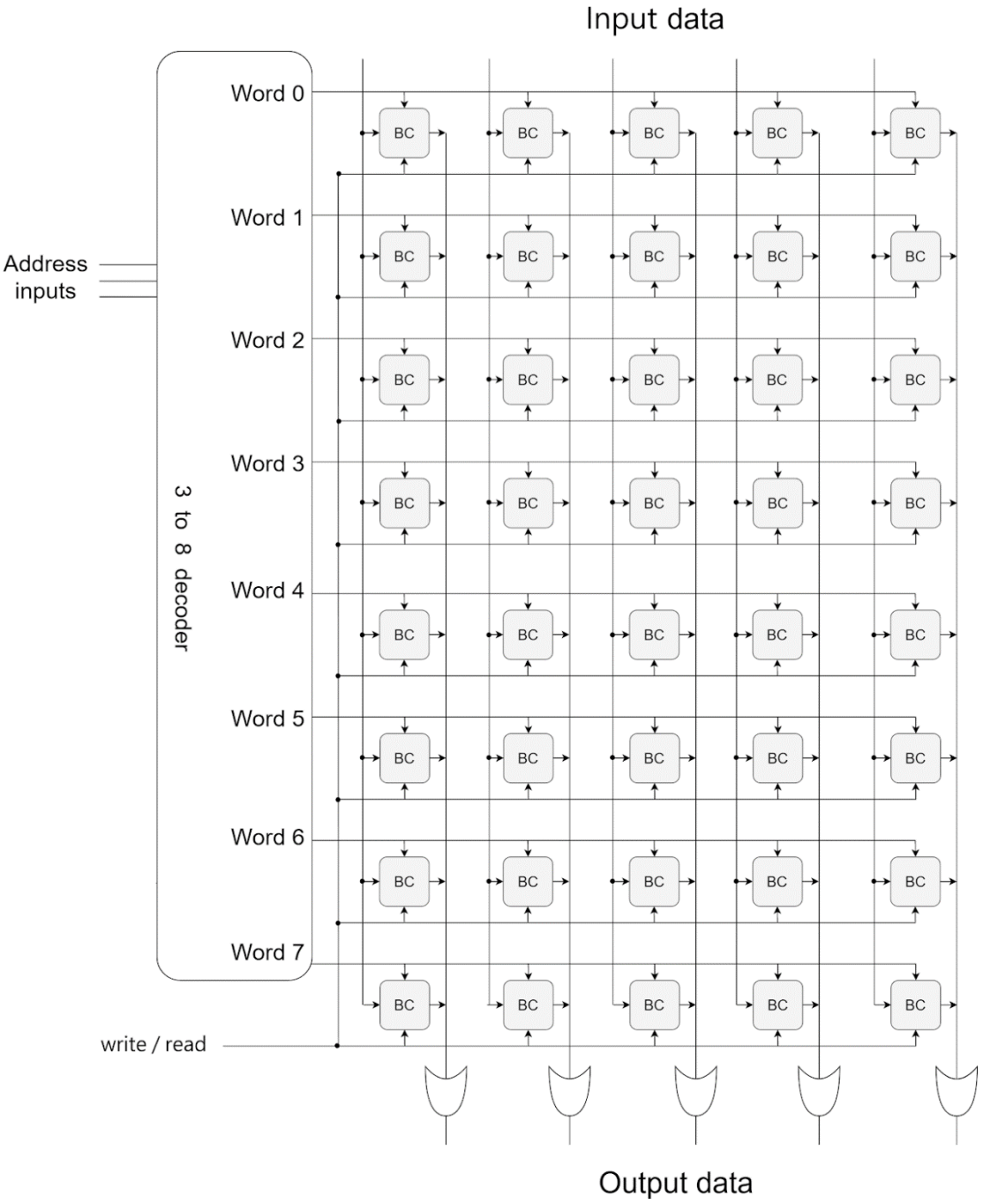
   (a)
   (1) 21 address lines,
   16 data input lines,
   16 data output lines.
   (2) 2^21 * 2^4 = 2^25bits

   (b)
   (1) 31 address lines,
   8 data input lines,
   8 data output lines.
   (2) 2^31 * 2^3 = 2^34bits

2. Design a 8x5 RAM.






Input data
Word 0
Word 1
Word 2
Word 3
Word 4
Word 5
Word 6
Word 7
Address inputs
3 to 8 decoder
write / read
BC
Output data

3. A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from the memory. What is the original 8-bit data word that was written into memory if the 12-bit word read out is as: (a) 011001000110 (b) 101110110100

3 (a) 011001000110

C_1 = XOR of bits (1, 3, 5, 7, 9, 11) = 0

C_2 = XOR of bits (2, 3, 6, 7, 10, 11) = 1

C_4 = XOR of bits (4, 5, 6, 7, 12) = 1

C_8 = XOR of bits (8, 9, 10, 11, 12) = 0

$C_8C_4C_2C_1 = (0110)_2 = (6)_{10}$ ⇒ No.6 bit is wrong

⇒ 011000000110

⇒ 01100000110 ⇒ 10000110

去除 parity bits

(b) 101110110100

C_1 = XOR (1, 3, 5, 7, 9, 11) = 0

C_2 = XOR (2, 3, 6, 7, 10, 11) = 1

C_4 = XOR (4, 5, 6, 7, 12) = 1

C_8 = XOR (8, 9, 10, 11, 12) = 0

$C_8C_4C_2C_1 = (0110)_2 = (6)_{10}$ ⇒ NO6 bit is wrong

⇒ 101111110100

⇒ 10111111100 ⇒ 11110100

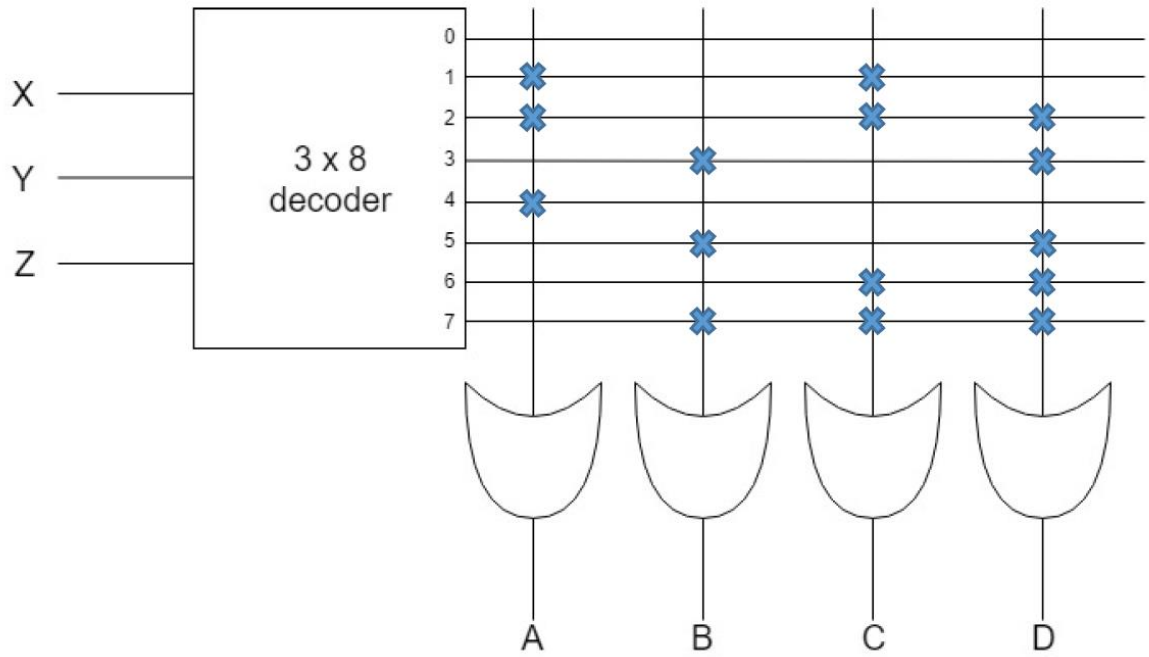
去除 parity bits

4. Tabulate the truth table for an 8x4 ROM that implements the Boolean functions.
   (a) A(X, Y, Z) = Σm(1, 2, 4)
   (b) B(X, Y, Z) = Σm(3, 5, 7)
   (c) C(X, Y, Z) = Σm(1, 2, 6, 7)
   (d) D(X, Y, Z) = Σm(2, 3, 5, 6, 7)

   Truth Table:

Inputs			Outputs			
X	Y	Z	A	B	C	D
0	0	0	0	0	0	0
0	0	1	1	0	1	0
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	0	0
1	0	1	0	1	0	1
1	1	0	0	0	1	1
1	1	1	0	1	1	1

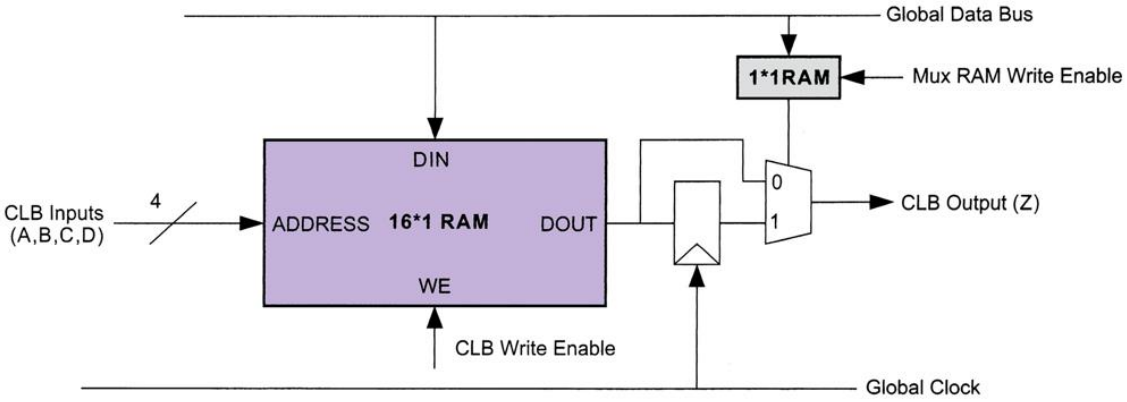
   ROM Configuration:



   (3x8 decoder 可參考第 2 題的設計)

5. FPGA: The logic cell has four inputs (A, B, C, D) and one output (Z).
   (a) Draw the logic diagram of a simple logic cell with 4-bit inputs and 1-bit outputs.
   (b) Explain how the logic cell can finish the sum function in a full adder. (Z=A+B+C)

(a)



若FPGA需要做Sequential Circuit，1*1 RAM內的data=1；反之若為Combinational Circuit，1*1 RAM內的data=0。

(b)

address	A	B	C	D	Dout
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	1
15	1	1	1	1	1

(sum function : Dout=A xor B xor C)
首先，CLB Write Enable=1，將以上的 LUT 資料存進 16*1 RAM 對應的；存完之後 CLB Write Enable=0，將資料藉由 CLB inputs 獲得 address，再將對應 address 的 data 讀出；而 1*1 RAM 的 data=0，因為 sum function 只需使用 Combination circuit 來實現。

