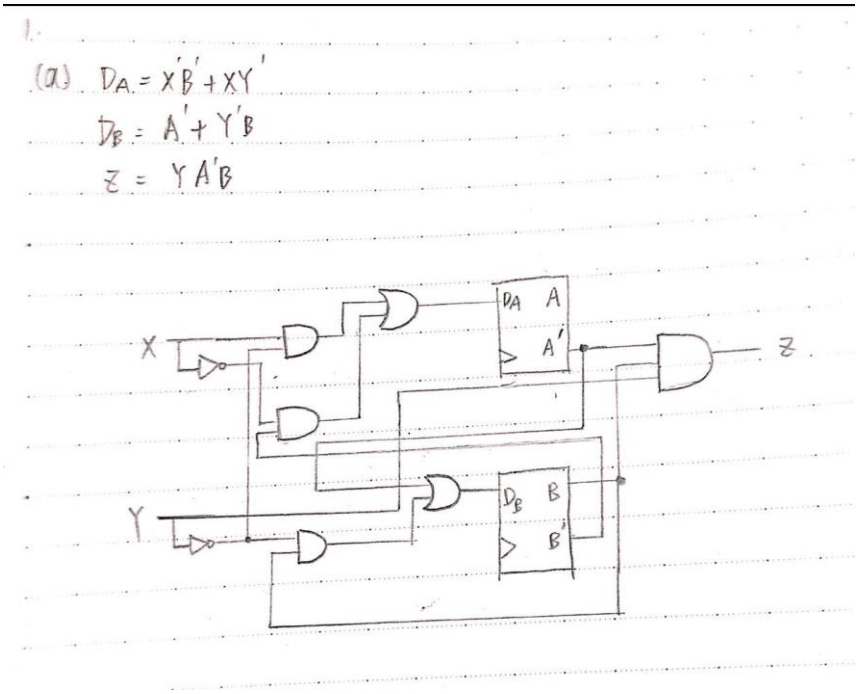
HW5

1. (15%) A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following input equations:

   D_A=X'B'+XY', D_B=A'+Y'B, Z=YA'B

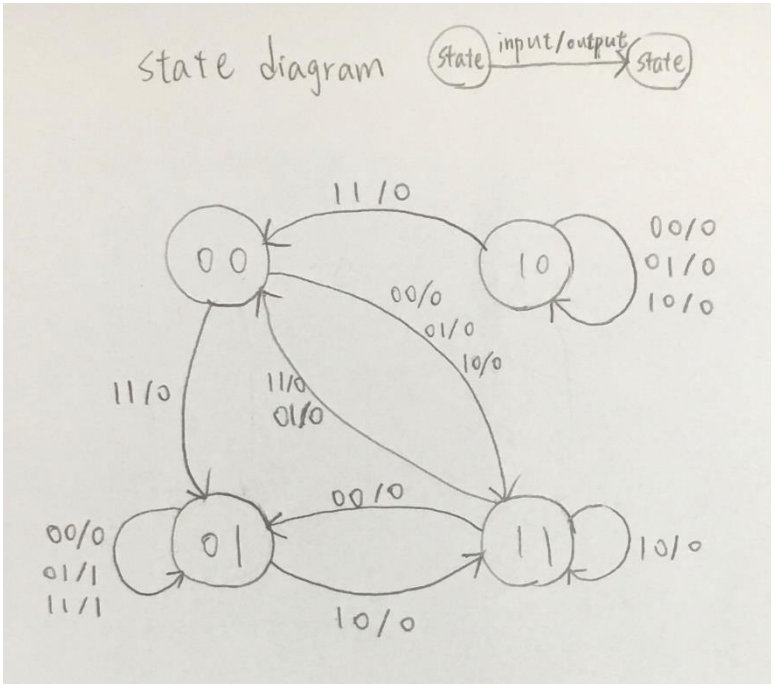
   (a) Draw the logic diagram of the circuit.



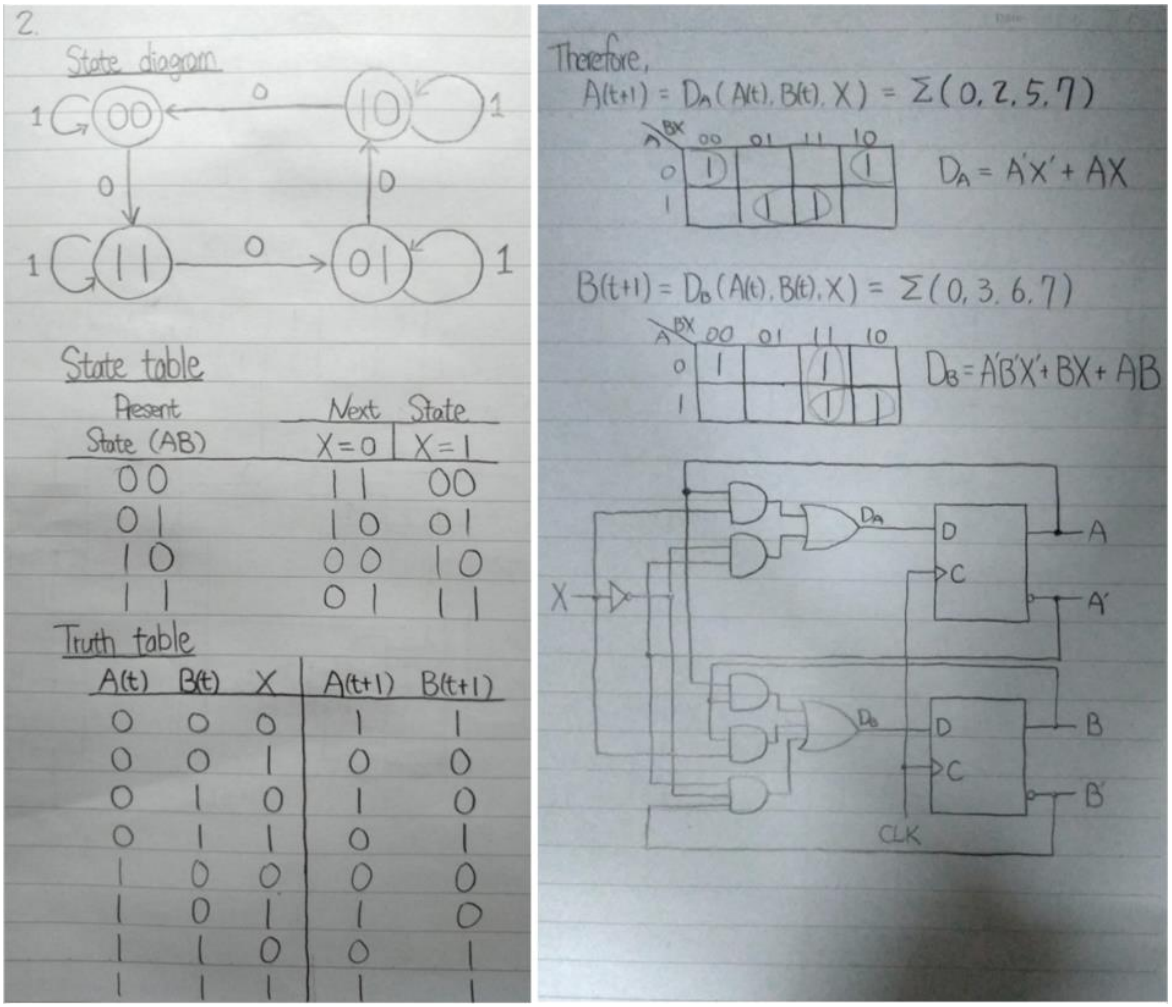
   (b) Derive the state table.

Present state		Input		Next state		Output
A(t)	B(t)	X	Y	A(t+1)	B(t+1)	Z
0	0	0	0	1	1	1
0	0	0	1	1	1	0
0	0	1	0	1	1	1
0	0	1	1	0	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	1	0
0	1	1	1	0	1	0
1	0	0	0	1	0	1
1	0	0	1	1	0	0
1	0	1	0	1	0	1
1	0	1	1	0	0	0
1	1	0	0	0	1	0
1	1	0	1	0	0	0
1	1	1	0	1	1	0
1	1	1	1	0	0	0

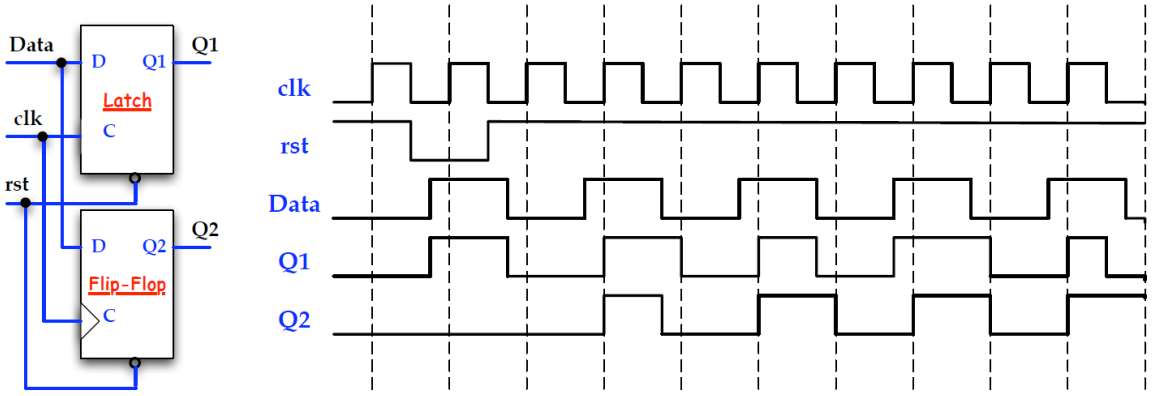
(c) Derive the state diagram.



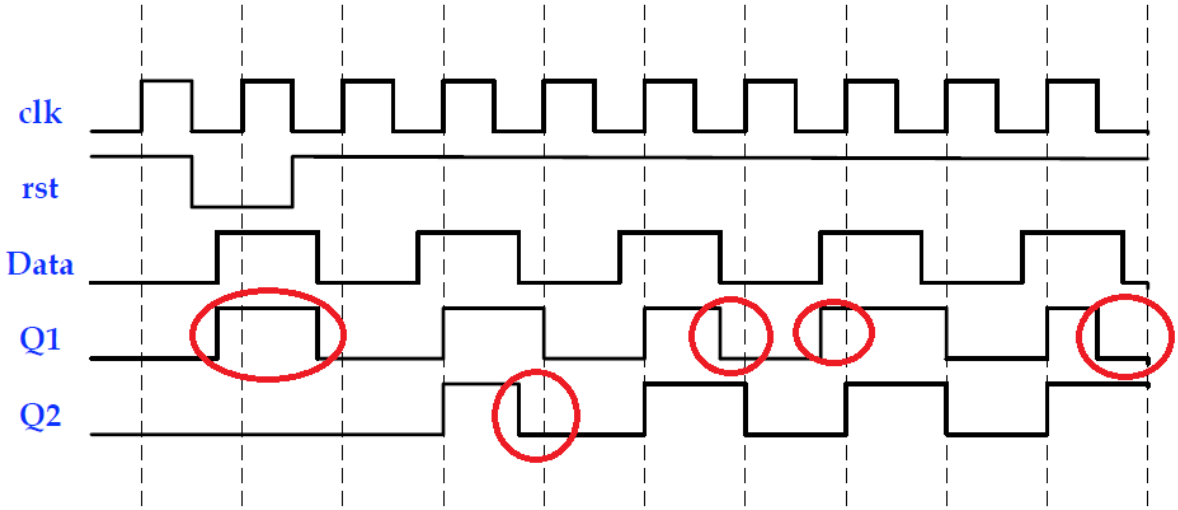
2. (10%) Design a sequential circuit with two D flip-flops A and B and one input X. When X = 1, the state of the circuit remains the same. When X = 0, the circuit goes through the state transitions from 00 to 11 to 01 to 10, back to 00, and then repeats.



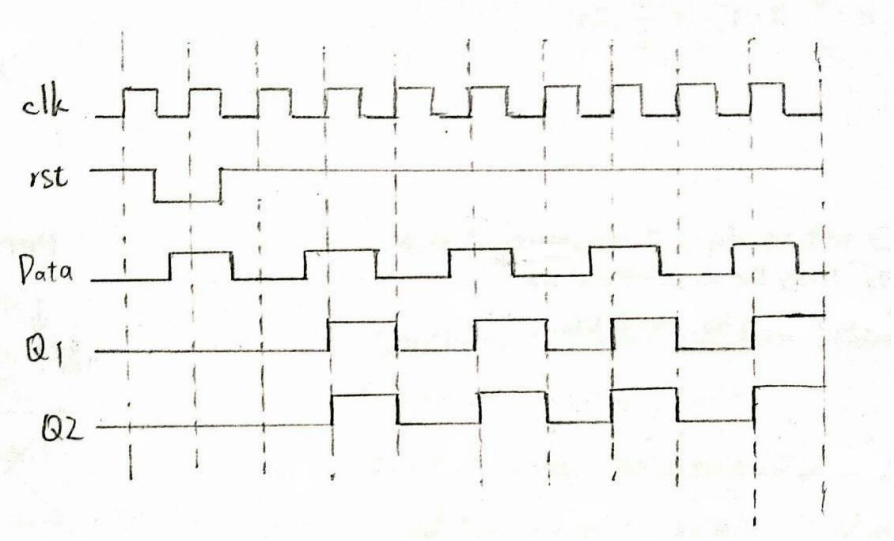
3. (20%) For the D-type positive edge-triggered flip-flop and D-type positive level-sensitive (level-triggered) latch with the same clock (clk), asynchronous reset signal (rst, active low), and input (Data) below. Assume the initial state of both the flip-flop and latch are '0', and both devices are with 0 D-to-Q delay. Point out the incorrect parts for Q1 and Q2 in the timing diagram and redraw the correct timing diagram.



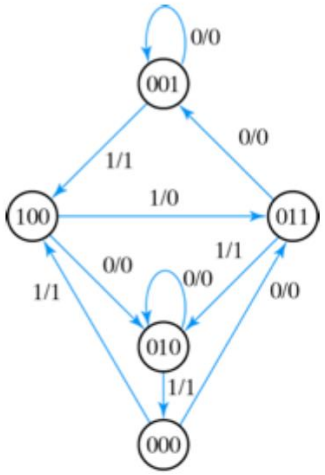
Incorrect parts:



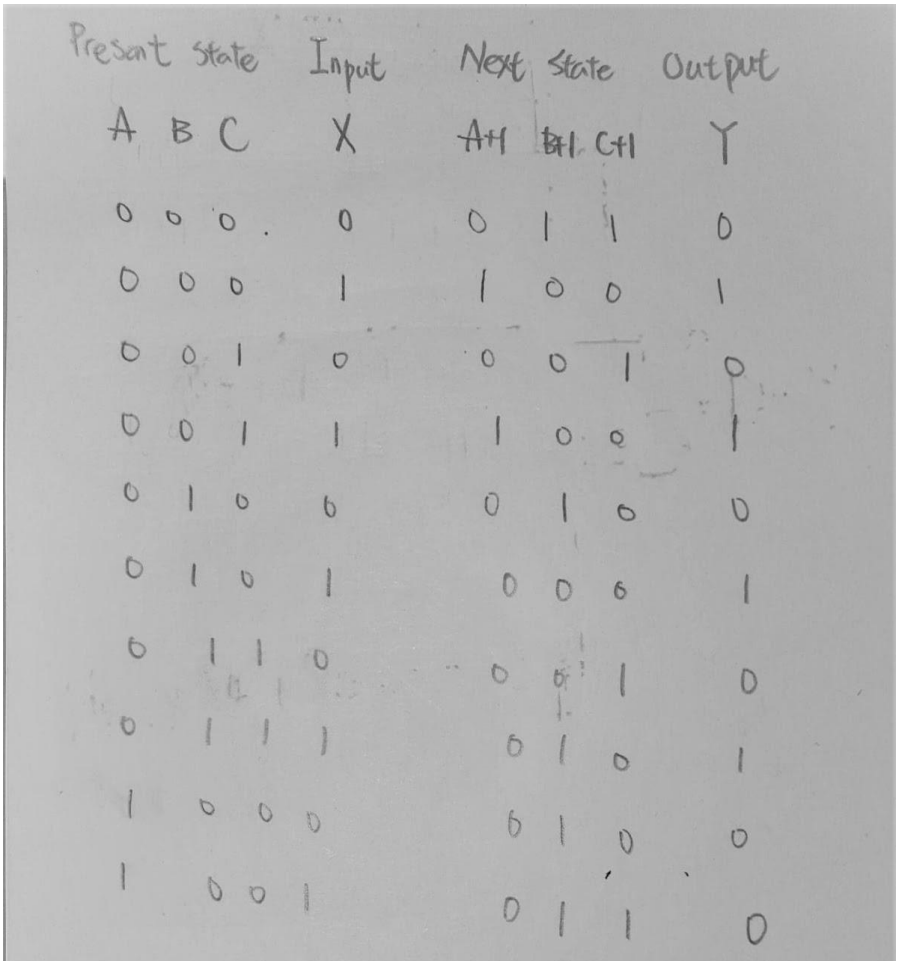
Correct timing diagram:

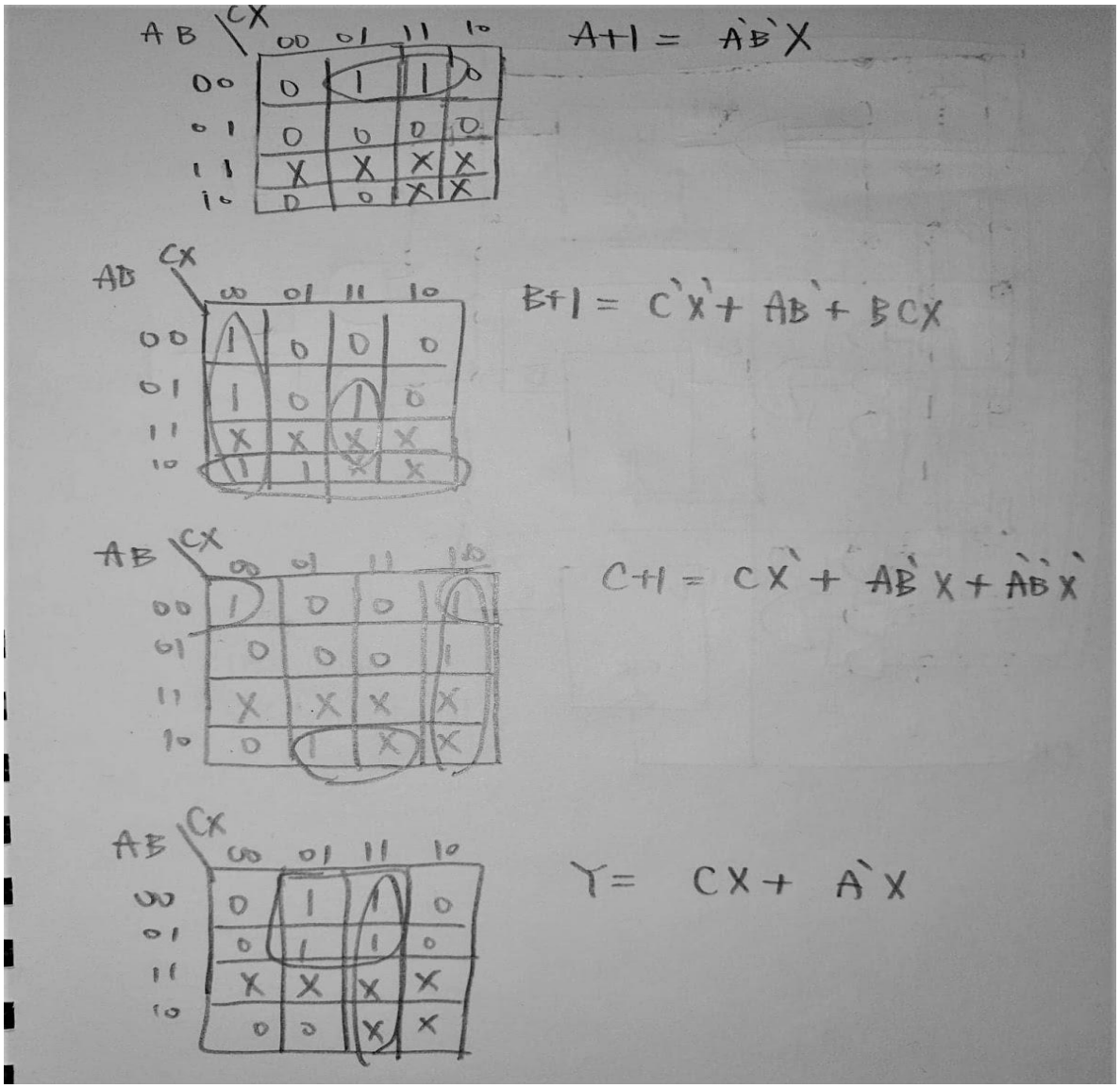


4. (10%) A sequential circuit has two flip-flops A and B, one input X, and one output Y. The state diagram is shown in figure below. Design the circuit with D flip-flops.

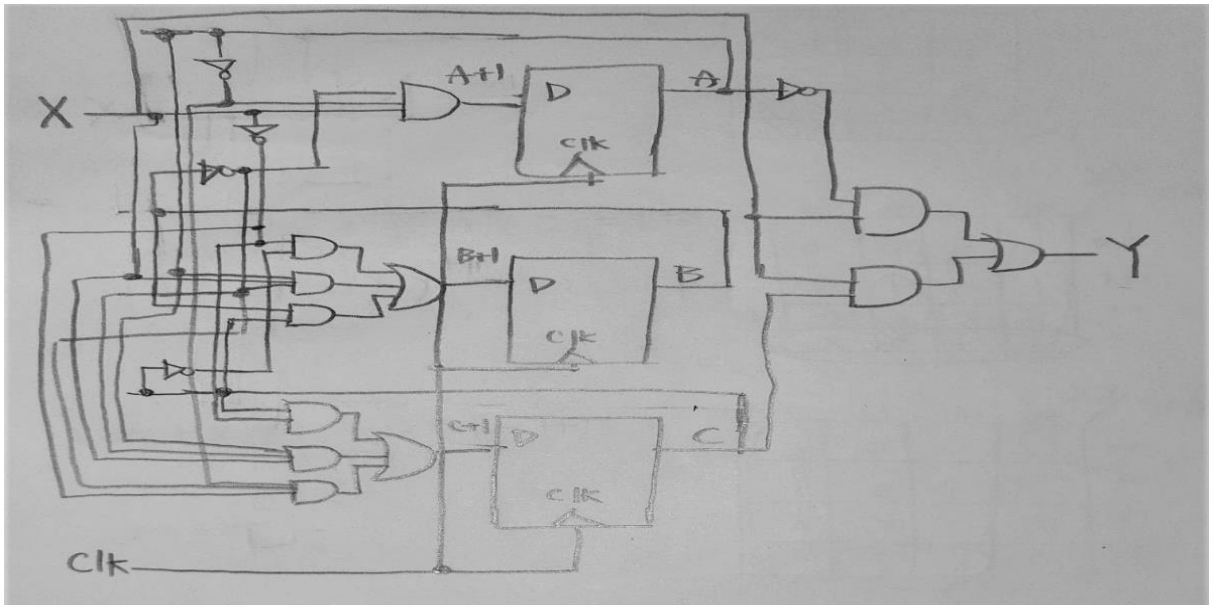


Ans:





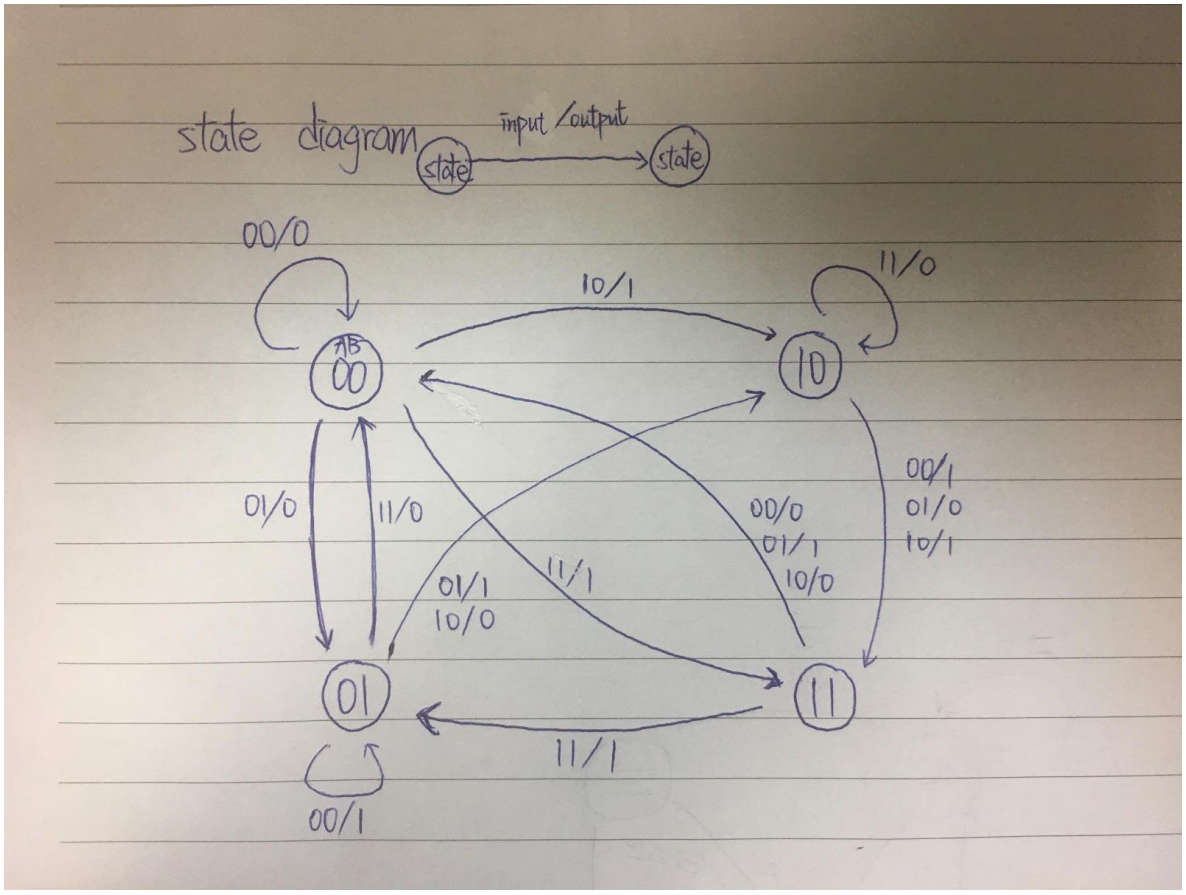
Logic Diagram (Optional):



5. (10%) Draw the state diagram of the sequential circuit specified by the following state table.

Present State		Inputs		Next State		Output
A	B	X	Y	A	B	Z
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	0	1	0	1	0	1
0	0	1	1	1	1	1
0	1	0	0	0	1	1
0	1	0	1	1	0	1
0	1	1	0	1	0	0
0	1	1	1	0	0	0
1	0	0	0	1	1	1
1	0	0	1	1	1	0
1	0	1	0	1	1	1
1	0	1	1	1	0	0
1	1	0	0	0	0	0
1	1	0	1	0	0	1
1	1	1	0	0	0	0
1	1	1	1	0	1	1

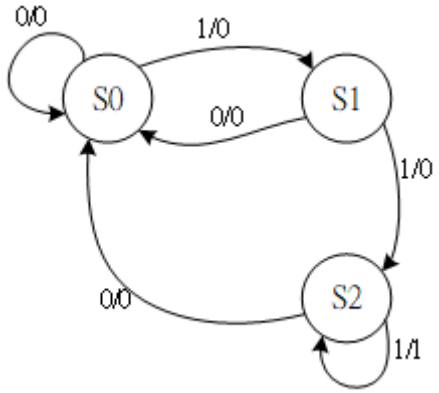
Ans:



6. (15%) Design a recognizer that recognizes an input sequence that has at least three 1's. The recognizer has a single input X, and a single output Y, and one asynchronous Reset input signal. The recognizer sets the output Y to 1 if the input signal X was equal to 1 in at least 3 clock cycles after reset. (a) Derive the state diagram. (b) Encode the states to minimize the combinational logic. (c) Draw the logic diagram using D flip-flops.

*本題使用 Moore Machine 或 Mealy Machine 皆可，解答以 Mealy Machine 為例

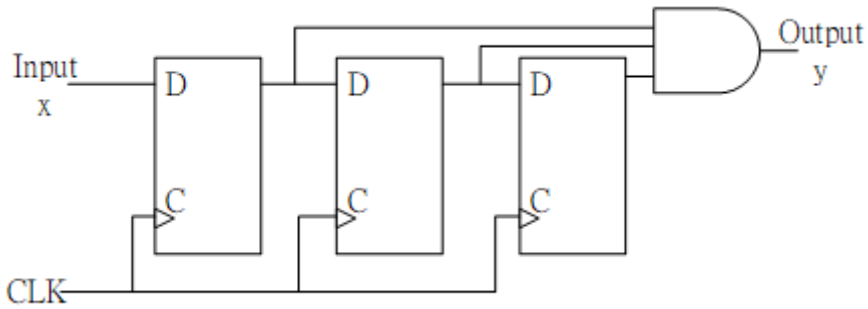
(a)



(b)

present state		next state x=0	next state x=1	output y x=0	output y x=1
S0	00	00	01	0	0
S1	01	00	10	0	0
S2	10	00	11	0	1

(c)



7. (20%) Reduce the number of states in the following state table and tabulate the reduced state table.

Present State	Next State x=0	Next State x=1	Output x=0	Output x=1
a	f	b	0	0
b	d	e	1	0
c	f	e	0	0
d	g	a	1	0
e	d	e	1	0
f	f	b	1	1
g	g	a	1	0
h	g	c	0	0

Show that the same output sequences are obtained for both the state table of the previous problem and the reduced state table from the previous problem. The state-circuit starts from state a, and the input sequence is 10110101001.

Ans:

1st turn

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	f	b	0	0
b	d	e b	1	0
c	f	e b	0	0
d	g	a	1	0
~~e~~	~~d~~	~~e~~	~~1~~	~~0~~
f	f	b	1	1
g	g	a	1	0
h	g	c	0	0

2nd turn

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	f	b	0	0
b	d	b	1	0
c	f	b	0	0
d	g d	a	1	0
f	f	b	1	1
~~g~~	~~g~~	~~a~~	~~1~~	~~0~~
h	g d	c	0	0

Reduced table

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	f	b	0	0
b	d	b	1	0
c	f	b	0	0
d	d	a	1	0
f	f	b	1	1
h	d	c	0	0

Brfore Reduced											
Time	1	2	3	4	5	6	7	8	9	10	11
Present state	a	b	d	a	b	d	a	f	b	d	g
Input	1	0	1	1	0	1	0	1	0	0	1
Next State	b	d	a	b	d	a	f	b	d	g	a
Output	0	1	0	0	1	0	0	1	1	1	0
After Reduced											
Time	1	2	3	4	5	6	7	8	9	10	11
Present state	a	b	d	a	b	d	a	f	b	d	d
Input	1	0	1	1	0	1	0	1	0	0	1
Next State	b	d	a	b	d	a	f	b	d	d	a
Output	0	1	0	0	1	0	0	1	1	1	0

