HW6a

1. Consider a 4-bit synchronous binary up counter.
   (a) Draw the logic diagram
   (b) Construct Verilog RTL representation for the logics with verification.

2. Use D flip-flops and gates to design a binary counter with each of the following repeated binary sequences:

   (a) 1, 5, 7
   (b) 0, 2, 4, 6

