EECS 207002
Logic Design Laboratory
邏輯設計實驗

黃元豪
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Department of Electrical Engineering
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Syllabus

- Credit : 3
- Instructor : Yuan-Hao Huang (黃元豪)
  - Room 953 Delta Building,
  - E-mail : yhhuang@ee.nthu.edu.tw
- Class Hours
  - 15:30~17:20 (R7,R8) Teaching at Delta Building Room 217 (class)
- TA Hours
  - 17:30~19:20 (R9,RA) Delta Building 2F 電子電路實驗室(lab)
  - 17:30~19:20 (M9,MA) Delta Building 2F 電子電路實驗室(lab)
    補demo 於 Prof. His-Pin Ma's TA Hours
- Course Notes : eLearn 數位學習平台
- Teaching Assistants:
  - 吳秉豐、陳思熙、江威霖、徐宜婕、陳成彬、周沛毅
  - Email : nthueecom626@gmail.com

Syllabus

- Reference Book
  - William J. Dally & R. Curtis Harting, *Digital Design – A System Approach*, Cambridge International Student Edition
  - M. Morris Mano & Charles R. Kime, Logic and Computer Design Fundamental, 4th ed. 2008, Pearson Prentice Hall.

- Grading
  - 70% : Experiments
  - 20% : Final Project
  - 10% : Final On-Site Examination

Schedule

Official Week	Date	Lecture	Lab
1	2/17	0 Introduction to Verilog RTL	Lab 0: Simple Verilog and Vivado Simulation
2	2/24	1 Verilog HDL I Combination Logic	Lab 1: Introduction to Verilog HDL
3	3/3	2. FPGA Emulation	Lab 1: Introduction to Verilog HDL
4	3/10	3. Verilog HDL II Sequential Logic	Lab 2: FPGA Emulation
5	3/17	4. Counters and Shift Registers	Lab 3: Counters and Shift Registers I
6	3/24	5. Finite State Machine / Button and Stopwatches	Lab 4: Counters and Shift Registers II
7	3/31	7_0. Communications Protocol	Lab 5: Timers and Stop Watches
8	4/7	7_1. Speaker	Lab 6: Electronic Clock
9	4/14	8 Keyboard	Lab 6: Electronic Clock
10	4/21	8 Keyboard	Lab 7: Speakers
11	4/28	9 Electronic Organ	Lab 8: Keyboard
12	5/5	10 VGA *final project proposal	Lab 8: Keyboard
13	5/12	10 VGA	Lab 9: VGA Display
14	5/19	Final Project	Lab 9: VGA Display
15	5/25	Final Project	
16	6/2	Final Exam	
17	6/9	Final Project	
18	6/16	Final Project Demo	

Experiments

- Pre-lab assignment
  - Upload simulation results and signed by TAs
- Course contents
  - ~40min instruction by instructor
- Lab Experiments
  - Rest of the lab hours with instructor & TAs
  - Demo by pm 19:20
- Lab Demo Report deadline
  - pm 11:59, Wednesday after lab work

Lab Evaluation

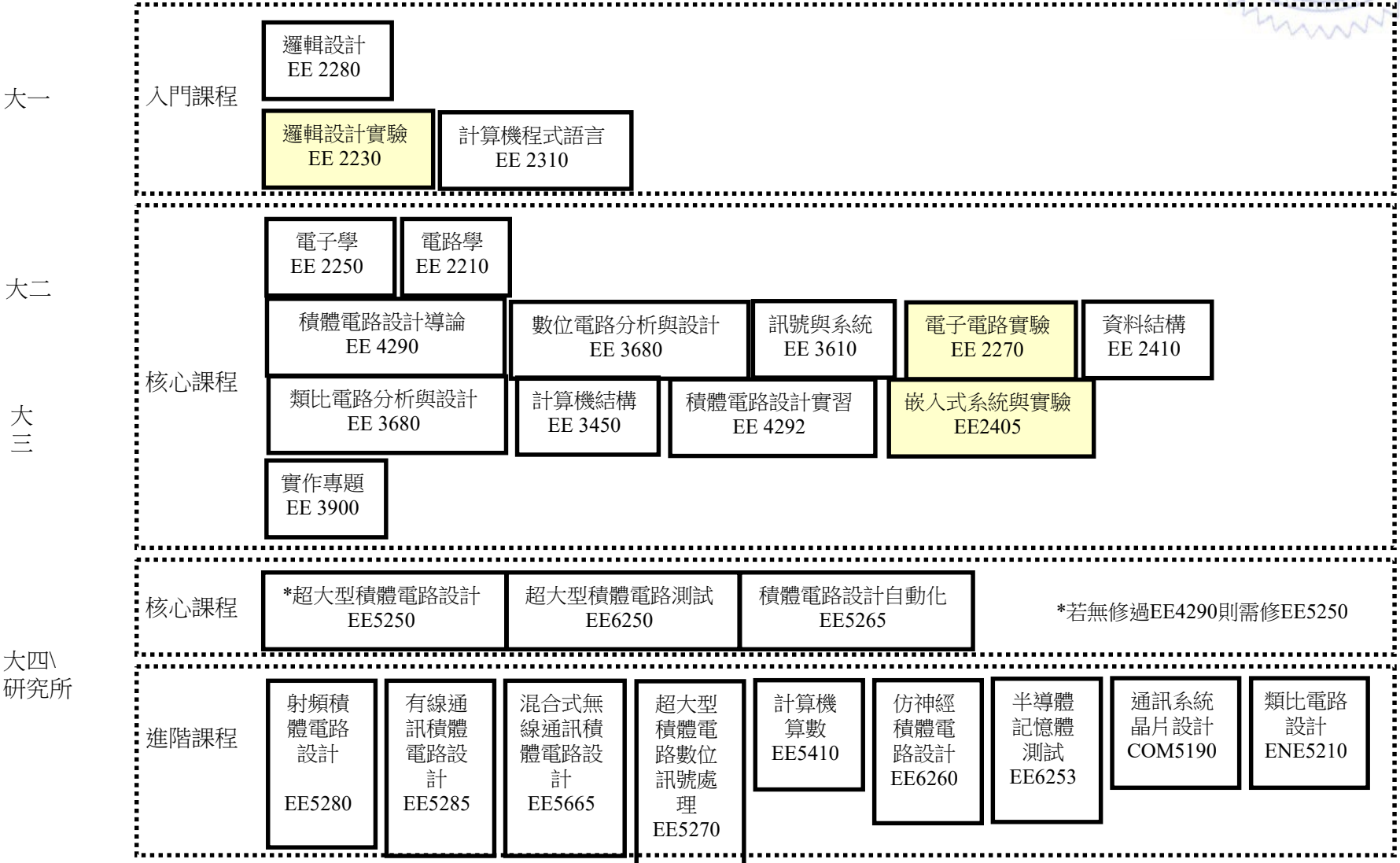
- Pre-lab
  - On time: 20% (-5%/week)
- Experiment
  - On time: 35% (-5%/week)
- Lab report
  - On time: 15% (-5%/week)
  - Report score: +20%
  - Bonus Problem: +10%

Software

- Vivado Installation
  - Verilog HDL Editor
  - Verilog Simulator
  - FPGA Design and Implementation Tool
- You can download the tool package (Vivado 2016.2) at elearn course website.
- You can apply the updated tool package (Vivado 2019.2) at http://www.Xilinx.com
  - Please read instruction in elearn course website.

電子電路設計學程

建議修課時程



- 一年級：電資院學士班、電機系、資工系、雙主修(電資、電機、資工)
- 四年級：電資院學士班、電機系、資工系、雙主修(電資、電機、資工)
- 三年級：電資院學士班、電機系、資工系、雙主修(電資、電機、資工)
- 二年級：電資院學士班、電機系、資工系、雙主修(電資、電機、資工)
- 大四：電資院、電機系、資工系第二專長
- 大三：電資院、電機系、資工系第二專長
- 大二：電資院、電機系、資工系第二專長