Lab 1: Introduction to Verilog HDL

Objective

- ✓ Review fundamental logic components.
- ✓ Introduce Verilog HDL modeling and verification.

Prerequisite

- ✓ Fundamentals of logic gates and Verilog HDL

Experiments

Design and verify a 4-bit binary-to-Gray-code converter (input: ***abcd***, output: ***wxyz***, ***a*** and ***w*** are the MSB).

1.1 Write the Boolean function/logic equation.
1.2 Draw the related logic diagram.
1.3 Construct the Verilog RTL code for the converter and use a testbench to simulate the logic behavior for verification.

2 Design a signed 4-bit binary adder/subtractor with input ***a*** ($\mathbf{a}_3\mathbf{a}_2\mathbf{a}_1\mathbf{a}_0$), ***b*** ($\mathbf{b}_3\mathbf{b}_2\mathbf{b}_1\mathbf{b}_0$), **m** as the operator control (0 for addition and 1 for subtraction); output ***s*** ($\mathbf{s}_3\mathbf{s}_2\mathbf{s}_1\mathbf{s}_0$), **v** as overflow indicator.

2.1 Derive the Boolean function/logic equation.
2.2 Draw the related logic diagram.
2.3 Construct the Verilog RTL code for the function and use a given testbench to simulate the logic behavior for verification.

3 (Bonus) For two 3-bit signed numbers ***a*** ($\mathbf{a}_2\mathbf{a}_1\mathbf{a}_0$) and ***b*** ($\mathbf{b}_2\mathbf{b}_1\mathbf{b}_0$), build a logic circuit to output ***o***($\boldsymbol{o}_2\boldsymbol{o}_1\boldsymbol{o}_0$) as the larger number and use a given testbench for verification.

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