Lab 4: Counters and Shift Registers II

Objective

- ✓ Review sequential circuits.
- ✓ Review counters and shift registers.

Prerequisite

- ✓ Fundamentals of logic gates.
- ✓ Clocking concepts
- ✓ Logic modeling in Verilog HDL.

Experiments

1 Construct a 4-bit synchronous binary up counter ($b_3b_2b_1b_0$) with the 1-Hz clock frequency from exp2 and use 4 LEDs for display.

I/O	$f_{crystal}$	b_3	b_2	b_1	b_0
Site	W5	V19	U19	E19	U16

2 Construct a single digit BCD up counter with the divided clock as the clock frequency and display on the seven-segment display.
- 2.1 Construct a BCD up counter.
- 2.2 Construct a BCD-to-seven-segment display decoder.
- 2.3 Combine the above two together.

3 Construct a single digit BCD down counter with the divided clock as the clock frequency and display on the seven-segment display.
- 3.1 Construct a BCD up counter.
- 3.2 Construct a BCD-to-seven-segment display decoder.
- 3.3 Combine the above two together.

4 (Bonus) Construct a 30 seconds count down timer (stop at 00).

TA: _____

