Submit Hierarchy

- StudentID_Lab3/
    - prelab/
      - prelab_1.v、prelab_1_tb.v、 prelab_2.v、prelab_2_tb.v
    - exp_1/
      - exp_1.v
    - exp_2/
      - exp_2.v
    - exp_3/
      - exp_3.v
    - exp_4/
      - exp_4.v
    - exp_5/
      - exp_5.v
    - StudentID_Lab3_report.pdf

- ➢ 請同學依照上述格式存放檔案並壓縮成 StudentID_Lab3.zip
- ➢ 報告請轉成 .pdf 檔
- ➢ 報告可重複上傳，第二次繳交請把舊檔案刪除。
- ➢ 請在時間內繳交至 eLearn，遲交每周會扣 5% 成績

Report 繳交內容參考:
  Prelab:
    1. logic diagram、simulation waveform
    2. simulation waveform
  experiment:
    1. specification of the frequency divider、block diagram、describe the design flow
    2. specification of the frequency divider、block diagram、describe the design flow
    3. block diagram、describe the design flow
    4. block diagram、describe the design flow
    5. block diagram、describe the design flow
  conclusion: