

## Lab 1: Verilog HDL

---

### Objective

- ✓ Review fundamental logic components.
- ✓ Introduce Verilog HDL modeling and verification.

### Prerequisite

- ✓ Fundamentals of logic gates and Verilog HDL.

### Experiments

- 1 Design and implement a full adder. ( $s + cout = x + y + cin$ )
  - 1.1 Write the logic equation.
  - 1.2 Draw the related logic diagram.
  - 1.3 Verilog RTL representation with verification.
- 2 Design a single digit decimal adder with input  $A(a_3a_2a_1a_0)$ ,  $B(b_3b_2b_1b_0)$ ,  $C_{in}(ci)$ , and output  $S(s_3s_2s_1s_0)$  and  $C_{out}(co)$ .
- 3 (Bonus) Design a 3-to-8-line decoder with enable (input  $in[2:0]$ , enable  $en$  and output  $d[7:0]$ ).
  - 3.1 Logic equation,
  - 3.2 Logic schematic,
  - 3.3 Verilog RTL representation with verification.

TA: \_\_\_\_\_