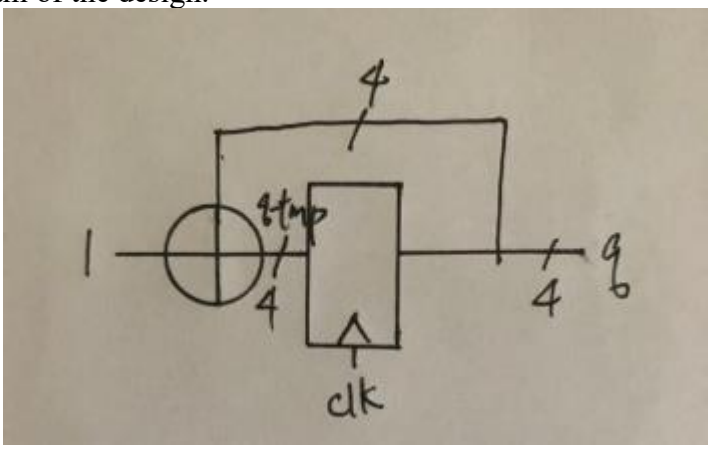
PreLab3_1

Design Specification

- ✓ For a counter:
  Input: clk, rst_n
  Output: q[3:0]
- ✓ Draw the block diagram of the design.



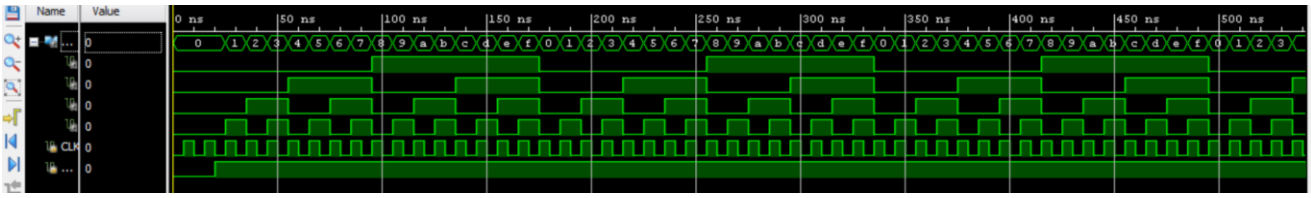
Design Implementation

- ✓ Truth table

input		q				output(q_next)			
rst	clk	q0	q1	q2	q3	q'0	q'1	q'2	q'3
0	X	X	X	X	X	0	0	0	0
1	1	0	0	0	0	0	0	0	1
1	1	0	0	0	1	0	0	1	0
1	1	0	0	1	0	0	0	1	1
1	1	0	0	1	1	0	1	0	0
1	1	0	1	0	0	0	1	0	1
1	1	0	1	0	1	0	1	1	0
1	1	0	1	1	0	0	1	1	1
1	1	0	1	1	1	1	0	0	0
1	1	1	0	0	0	1	0	0	1
1	1	1	0	0	1	1	0	1	0
1	1	1	0	1	0	1	0	1	1
1	1	1	0	1	1	1	1	0	0
1	1	1	1	0	0	1	1	0	1
1	1	1	1	0	1	1	1	1	0
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	1
1	0	0	0	1	0	0	0	1	0
1	0	0	0	1	1	0	0	1	1

1	0	0	1	0	0	0	1	0	0
1	0	0	1	0	1	0	1	0	1
1	0	0	1	1	0	0	1	1	0
1	0	0	1	1	1	0	1	1	1
1	0	1	0	0	0	1	0	0	0
1	0	1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0	1	0
1	0	1	0	1	1	1	0	1	1
1	0	1	1	0	0	1	1	0	0
1	0	1	1	0	1	1	1	0	1
1	0	1	1	1	0	1	1	1	0
1	0	1	1	1	1	1	1	1	1

- ✓ Logic
  Set q_tmp = q + 1
  If rst_n = 1, clk = 0, q_next <= q
  Else if rst_n = 1, clk = 1, q <= q_tmp
  Else if rst_n = 0, q = 0
- ✓ Simulation

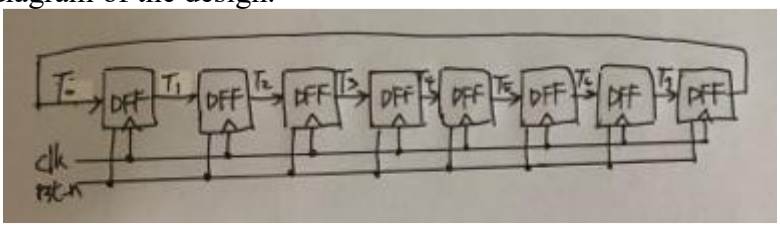


PreLab3_2

Design Specification

✓ For a 8-bit ring counter:
Input: clk, rst_n.
Output: t[3:0].

✓ Draw the block diagram of the design.



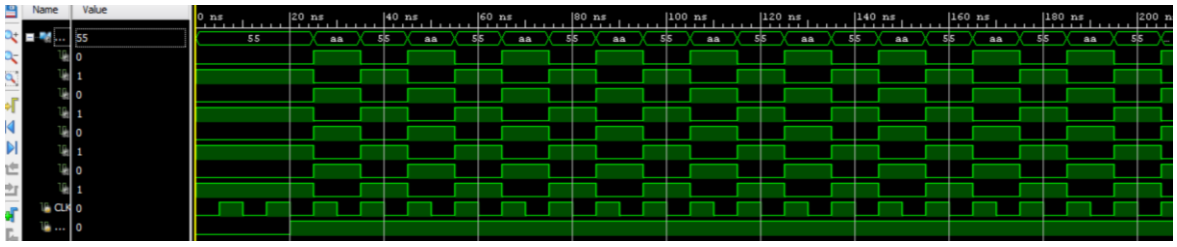
Design Implementation

✓ Truth table

clk	rst	t0	t1	t2	t3	t4	t5	t6	t7	t'0	t'1	t'2	t'3	t'4	t'5	t'6	t'7
X	0	X	X	X	X	X	X	X	X	0	1	0	1	0	1	0	1
1	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0
1	1	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

✓ Logic function
If rst_n = 1, t[0] <= t[1];
t[1] <= t[2];
t[2] <= t[3];
t[3] <= t[4];
t[4] <= t[5];
t[5] <= t[6];
t[6] <= t[7];
t[7] <= t[0];
If rst_n = 0, t = 01010101

✓ Simulation



Discussion

須注意 q 跟 q_next 的關聯，以及其切換條件，如 clk 和 rst_n 的設定會影響是否 trigger。另須注意其為 posedger 或 nenedger。

Conclusion

這次的 prelab 內容多為上學期課程，主要的問題是對於 verilog 語法不夠熟悉，上課也只有帶過一點點，大多都須看講義才知道要怎麼打 code。

