Lab 4: Counters and Shifters II

Objective

- ✓ Review sequential circuits.
- ✓ Review shift registers.

Prerequisite

- ✓ Fundamentals of logic gates.
- ✓ Clocking concepts
- ✓ Logic modeling in Verilog HDL.

Experiments

1 Construct a 4-bit synchronous binary down counter ($b_3b_2b_1b_0$) with the 1-Hz clock frequency from lab3 and use 4 LEDs for display.

I/O	$f_{crystal}$	b_3	b_2	b_1	b_0
Site	W5	V19	U19	E19	U16

2 Combine the 4-bit synchronous binary down counter from exp1 with a binary-to-seven-segment-display decoder (from lab2) to display the binary counting in 7-segment display.

3 Construct a single digit BCD **down** counter with a 0.5-Hz clock as the clock frequency and display on the seven-segment display.
- 3.1 Construct a BCD down counter.
- 3.2 Construct a BCD-to-seven-segment display decoder (from lab2).
- 3.3 Combine the above two together.

4 Construct a two-digit BCD **up** counter with a 1-Hz clock as the clock frequency and display on the seven-segment display.

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