**Lab2\_1**

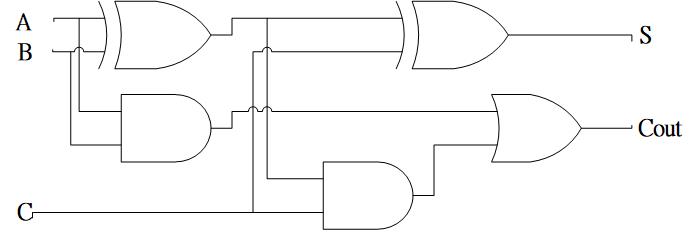
**Design Specification**

* For a full adder:

Input: a, b, cin.

Output: s, cout.

* Draw the block diagram of the design.

****

**Design Implementation**

* Truth table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| a | b | cin | s | cout |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

* Logic function

s = (a’．b’．cin) +(a’．b．cin’) +(a．b’．cin’) +(a．b．cin)

= a⊕b⊕cin

cout = a．b + b．cin + a．cin

* I/O pin

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| I/O | a | b | cin | s | cout |
| LOC | V17 | V16 | W16 | U16 | E19 |

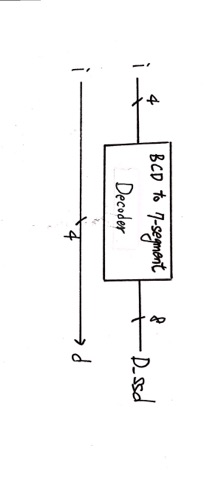
**Lab2\_2**

**Design Specification**

* Input: i[3:0]

Output: d[3:0], D\_ssd [7:0]

* Draw the block diagram of the design.



**Design Implementation**

* Truth table

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| input | | | | output | | | | | | | | | | | | | | | |
| i3 | i2 | i1 | i0 | D\_ssd7 | D\_ssd6 | D\_ssd5 | D\_ssd4 | D\_ssd3 | D\_ssd2 | D\_ssd1 | D\_ssd0 | d3 | d2 | d1 | d0 | D3 | D2 | D1 | D0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 2 | 2 | 2 | 2 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 3 | 3 | 3 | 3 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 4 | 4 | 4 | 4 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 5 | 5 | 5 | 5 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 6 | 6 | 6 | 6 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 7 | 7 | 7 | 7 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 8 | 8 | 8 | 8 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 9 | 9 | 9 | 9 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | F | F | F | F |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | F | F | F | F |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | F | F | F | F |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | F | F | F | F |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | F | F | F | F |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | F | F | F | F |

* Logic function

d = i

D = 4’ b0000

D\_ssd[7:0] are low – active

4'd0: D\_ssd = 8'b00000011;

4'd1: D\_ssd = 8'b10011111;

4'd2: D\_ssd = 8'b00100101;

4'd3: D\_ssd = 8'b00001101;

4'd4: D\_ssd = 8'b10011001;

4'd5: D\_ssd = 8'b01001001;

4'd6: D\_ssd = 8'b01000001;

4'd7: D\_ssd = 8'b00011111;

4'd8: D\_ssd = 8'b00000001;

4'd9: D\_ssd = 8'b00001001;

default: D\_ssd = 8'b01110001;

* I/O pin

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| I/P | i3 | i2 | i1 | i0 | d3 | d2 | d1 | d0 | D3 | D2 | D1 | D0 |
| VOC | W17 | W16 | V16 | V17 | V19 | U19 | E19 | U16 | W4 | V4 | U4 | U2 |
| I/P | D\_ssd7 | D\_ssd6 | D\_ssd5 | D\_ssd4 | D\_ssd3 | D\_ssd2 | D\_ssd1 | D\_ssd0 |  |  |  |  |
| VOC | W7 | W6 | U8 | V8 | U5 | V5 | U7 | V7 |  |  |  |  |

**Lab2\_3**

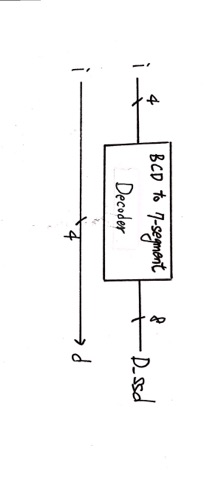
**Design Specification**

* I/P

Input: i[3:0]

Output: d[3:0], D\_ssd [7:0]

* Block diagram



**Design Implementation**

* Truth table

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| input | | | | output | | | | | | | | | | | | | | | |
| i3 | i2 | i1 | i0 | D\_ssd7 | D\_ssd6 | D\_ssd5 | D\_ssd4 | D\_ssd3 | D\_ssd2 | D\_ssd1 | D\_ssd0 | d3 | d2 | d1 | **d0** | D3 | D2 | D1 | D0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 2 | 2 | 2 | 2 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 3 | 3 | 3 | 3 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 4 | 4 | 4 | 4 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 5 | 5 | 5 | 5 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 6 | 6 | 6 | 6 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 7 | 7 | 7 | 7 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 8 | 8 | 8 | 8 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 9 | 9 | 9 | 9 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | F | F | F | F |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | F | F | F | F |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | F | F | F | F |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | F | F | F | F |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | F | F | F | F |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | F | F | F | F |

* Logic function

d = i

D = 4’ b0000

D\_ssd[7:0] are low – active

4'd0: D = 8'b00000011;

4'd1: D = 8'b10011111;

4'd2: D = 8'b00100101;

4'd3: D = 8'b00001101;

4'd4: D = 8'b10011001;

4'd5: D = 8'b01001001;

4'd6: D = 8'b01000001;

4'd7: D = 8'b00011111;

4'd8: D = 8'b00000001;

4'd9: D = 8'b00001001;

4'd10: D = 8'b00010001;

4'd11: D = 8'b11000001;

4'd12: D = 8'b01100011;

4'd13: D = 8'b10000101;

4'd14: D = 8'b01100001;

4'd15: D = 8'b01110001;

* I/O pin

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| * I/P | i3 | i2 | i1 | i0 | d3 | d2 | d1 | d0 | D3 | D2 | D1 | D0 |
| VOC | W17 | W16 | V16 | V17 | V19 | U19 | E19 | U16 | W4 | V4 | U4 | U2 |
| I/P | D\_ssd7 | D\_ssd6 | D\_ssd5 | D\_ssd4 | D\_ssd3 | D\_ssd2 | D\_ssd1 | D\_ssd0 |  |  |  |  |
| VOC | W7 | W6 | U8 | V8 | U5 | V5 | U7 | V7 |  |  |  |  |

**Lab2\_4**

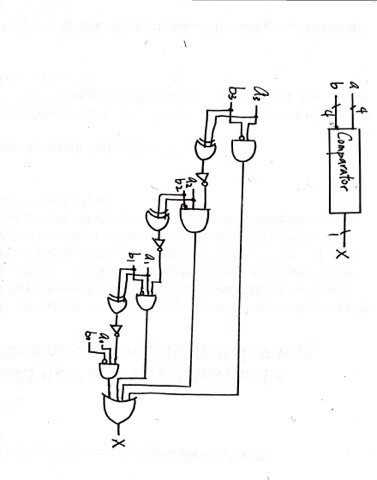
**Design Specification**

* I/P

Input: a[3:0], b[3:0]

Output: x, A[3:0]. B[3:0]

* Block diagram



**Design Implementation**

* Truth table

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| input | | | | | | | | output |
| a3 | a2 | a1 | a0 | b3 | b2 | b1 | b0 | x |
| 1 | X | X | X | 0 | X | X | X | 1 |
| 1 | 1 | X | X | 1 | 0 | X | X | 1 |
| 1 | 1 | 1 | X | 1 | 1 | 0 | X | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |

* Logic function

A = a

B = b

Set c[3:0], c = ( a & b’ | a’ & b )’

x = a[3] & b[3]’ | c[3]&a[2]&b[2]’ | c[3]&c[2]&a[1]&b[1]’ | c[3]&c[2]&c[1]&a[0]&b[0]’

* I/O pin

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| I/P | a3 | a2 | a1 | a0 | b3 | b2 | b1 | b0 |  |
| VOC | W19 | W16 | V16 | V17 | R2 | T1 | U1 | W2 |  |
| I/P | A3 | A2 | A1 | A0 | B3 | B2 | B1 | B0 | x |
| VOC | V19 | U19 | E19 | U16 | L1 | P1 | N3 | P3 | U14 |

**Discussion**

第二題與第三題須設計一個3 to 8 decoder，並將其結果顯示於7-segment display上。因此在設定了不同case會對應到不同的結果。須注意的是其為low-active，因此要注意對應關係，不然就會得到相反的結果。第四題為設計a與b的大小比較器，若a的較高位數皆大於b，即可得知a>b(由truth table可見)。

**Conclusion**

這次的實驗程式大多是上學期上課內容以及課堂上所教的，主要目的是讓我更熟悉FPGA板的使用。FPGA的pin腳有output跟input之分，如果看錯排就會很麻煩。