**Lab3\_1**

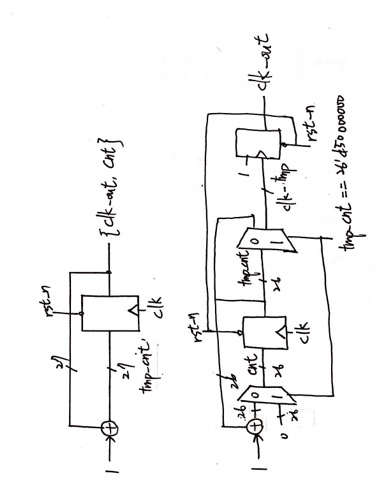
**Design Specification**

* For a 1/227 frequenc:

Input: rst\_n, clk

Output: clk\_out

* Draw the block diagram of the design.



**Design Implementation**

* 輸入的頻率F為100HZ，題目要求做出1/227頻率的除頻器，因此設立一個counter (cnt[25:0])。假設clk的頻率為F，則cnt[0]的頻率為F/2、cnt[1]的頻率為F/22、cnt[2]的頻率為F/23……cnt[25]的頻率為F/226、clk\_out的頻率為F/227，即符合題目要求。

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| clk\_out | cnt[25] | cnt[n-1] | cnt[2] | cnt[1] | cnt[0] | clk |
| 0 | 0 | … | 0 | 0 | 0 | 0 |
| 0 | 0 | … | 0 | 0 | 0 | 1 |
| 0 | 0 | … | 0 | 0 | 1 | 0 |
| 0 | 0 | … | 0 | 0 | 1 | 1 |
| 0 | 0 | … | 0 | 1 | 0 | 0 |
| 0 | 0 | … | 0 | 1 | 0 | 1 |
| 0 | 0 | … | 0 | 1 | 1 | 0 |
| 0 | 0 | … | 0 | 1 | 1 | 1 |
| 0 | 0 | … | 1 | 0 | 0 | 0 |
| 0 | … | …. | … | … | … | … |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| F/227 | F/226 | F/2n | F/8 | F/4 | F/2 | F |

* Logic function

當rst\_n為下緣或clk為上緣時，判斷若rst\_n = 0，則{clk\_out, cnt}歸零；否則{clk\_out, cnt}加1

* I/O pin

|  |  |  |  |
| --- | --- | --- | --- |
| I/O | clk | rst\_n | clk\_out |
| VOC | W5 | V17 | U16 |

**Lab3\_2**

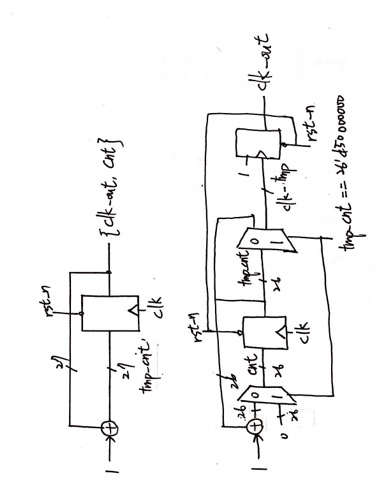
**Design Specification**

* For a 1/226 frequenc:

Input: rst\_n, clk

Output: clk\_out

* Draw the block diagram of the design.



**Design Implementation**

* 輸入的頻率F為100HZ，題目要求做出頻率為1HZ的除頻器，約等於1/226的除頻器。因此設立一個counter (cnt[24:0])。假設clk的頻率為F，則cnt[0]的頻率為F/2、cnt[1]的頻率為F/22、cnt[2]的頻率為F/23……cnt[24]的頻率為F/225、clk\_out的頻率為F/226，即符合題目要求。

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| clk\_out | cnt[24] | cnt[n-1] | cnt[2] | cnt[1] | cnt[0] | clk |
| 0 | 0 | … | 0 | 0 | 0 | 0 |
| 0 | 0 | … | 0 | 0 | 0 | 1 |
| 0 | 0 | … | 0 | 0 | 1 | 0 |
| 0 | 0 | … | 0 | 0 | 1 | 1 |
| 0 | 0 | … | 0 | 1 | 0 | 0 |
| 0 | 0 | … | 0 | 1 | 0 | 1 |
| 0 | 0 | … | 0 | 1 | 1 | 0 |
| 0 | 0 | … | 0 | 1 | 1 | 1 |
| 0 | 0 | … | 1 | 0 | 0 | 0 |
| 0 | … | …. | … | … | … | … |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| F/226 | F/225 | F/2n | F/8 | F/4 | F/2 | F |

* Logic function

當rst\_n為下緣或clk為上緣時，判斷若rst\_n = 0，則{clk\_out, cnt}歸零；否則當cnt等於26'd50000000時，cnt歸零，clk\_out = clk\_out’；否則{clk\_out, cnt}加1。

* I/O pin

|  |  |  |  |
| --- | --- | --- | --- |
| I/O | clk | rst\_n | clk\_out |
| VOC | W5 | V17 | U16 |

**Lab3\_3**

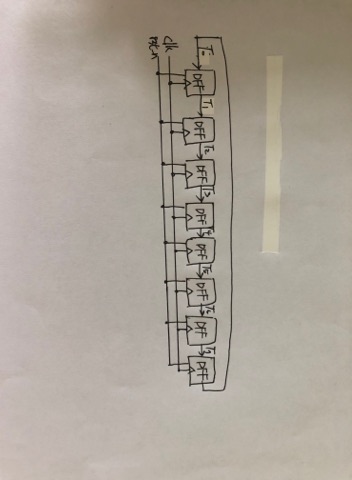
**Design Specification**

* I/P

Input: clk, rst\_n

Output: t[7:0]

* Block diagram



**Design Implementation**

* Truth table

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| clk | rst | t0 | t1 | t2 | t3 | t4 | t5 | t6 | t7 | t'0 | t'1 | t'2 | t'3 | t'4 | t'5 | t'6 | t'7 |
| X | 0 | X | X | X | X | X | X | X | X | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

* Logic function

將lab3-2的clk\_out作為此處的clk，當rst\_n為下緣或clk為上緣時，

If rst\_n = 1, t[0] <= t[1];

t[1] <= t[2];

t[2] <= t[3];

t[3] <= t[4];

t[4] <= t[5];

t[5] <= t[6];

t[6] <= t[7];

t[7] <= t[0];

If rst\_n = 0, t = 01010101

* I/O pin

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| I/O | t0 | t1 | t2 | t3 | t4 | t5 | t6 | t7 | clk | rst\_n |
| VOC | U16 | E19 | U19 | V19 | W18 | U15 | U14 | V14 | W5 | V17 |

**Discussion**

第一題與第二題基本上原理一樣，但第二題因為是要做1hz的除頻器，因此會多了一個判斷tmp\_cnt等於26’d50000000的步驟。兩題皆是透過加法器計算除頻次數，觀察附表可看出其規律。第三題則是結合第二題與prelab2，將第二題的clk\_out作為prelab的clk。

**Conclusion**

這次實驗的原理主要著重於除頻器的部分，如果沒搞懂其原理與flip flop的用法，會很容易出錯。接上電路板的 clk，其頻率所引起的訊號是有週期的，只是因為過快導致肉眼無法辨識，因此經過除頻後則可以看出其頻率。藉由不同counter與條件的搭配，可以做出不同的除頻器。