Frank Laterza

941-223-5298 | franklaterza@gmail.com | franklaterza.com | github.com/franklaterza | linkedin.com/in/laterzafrank
Software Engineer · UCF Computer Engineering Student

Education

University of Central Florida — Orlando, FL
Bachelor of Science in Computer Engineering — *Expected Graduation: Dec. 2025*

Technical Skills

Languages: C/C++, Python, Java, TypeScript, Objective-C, Swift, Verilog, VHDL
Hardware/Embedded: FPGA, PCB Design (Eagle CAD), Real-Time Systems (FreeRTOS), I2C, SPI, UART

Experience

Eta Space — Rockledge, FL
Software Engineer Lead — *June 2023 – Current*

- Led software development for a NASA-funded satellite mission, architecting a fault-tolerant, multithreaded flight software system in C++ to demonstrate lossless cryogenic liquid transfer.
- Engineered a robust embedded stack to control and monitor a network of sensors, heaters, valves, and pressure transducers, ensuring mission-critical system reliability.
- Designed a custom PCB and firmware with in-flight reprogramming capabilities, enabling remote system updates.
- Implemented an encrypted telemetry system integrated with Rocket Lab spacecraft, securing critical data transmission.
- Developed C++ GUI for ground-side testing, improving engineering interface efficiency with flight computer.

Apple — Cupertino, CA
Software Engineer Intern — *May 2025 – Aug. 2025*

- Prototyped first party feature for the Apple HomePod, utilizing Objective-C/Swift to seamlessly integrate with the Home ecosystem to enhance multi-device interaction.
- Optimized a lightweight Precision Time Protocol (PTP) algorithm for multi-room synchronization, reducing network overhead and improving timing accuracy across home devices.
- Architected a fault-tolerant distributed system framework for the HomePod, ensuring high availability and consistent state management for critical home automation tasks.

NVIDIA — Santa Clara, CA
GPU Firmware Engineer Intern — *May 2024 – Aug. 2024*

- Refactored security key-signing software to dynamically parse metadata, enabling secure client-side firmware updates for enterprise GPUs.
- Integrated static stack analysis into the GPU BIOS build system, proactively preventing critical stack overflow errors before deployment.
- Developed and released a client-facing diagnostic tool to expose I2C event logs, accelerating crash analysis for enterprise datacenter GPUs.

Projects

S.P.U.D (Custom RISC-V CPU) — Aug. 2025

- Designed and implemented a 5-stage pipelined 32-bit RISC-V CPU on an FPGA to drive a 64x64 RGB-LED matrix, including custom display driver logic with protected RAM buffers.
- Developed a C-based SDK for the S.P.U.D. processor, providing a hardware abstraction layer (HAL) and a simple graphics engine for 2D game development.

Dex (Self-Balancing Robot) — Dec. 2024

- Developed multicore real-time embedded software using FreeRTOS and the Pico SDK to control a self-balancing robot via Bluetooth (BTstack).
- Implemented a robust PID control system for real-time balancing, utilizing gyroscope/accelerometer data from an IMU.
- Designed a modular PCB in integrating a microcontroller, IMU, motor drivers, and power management circuits.