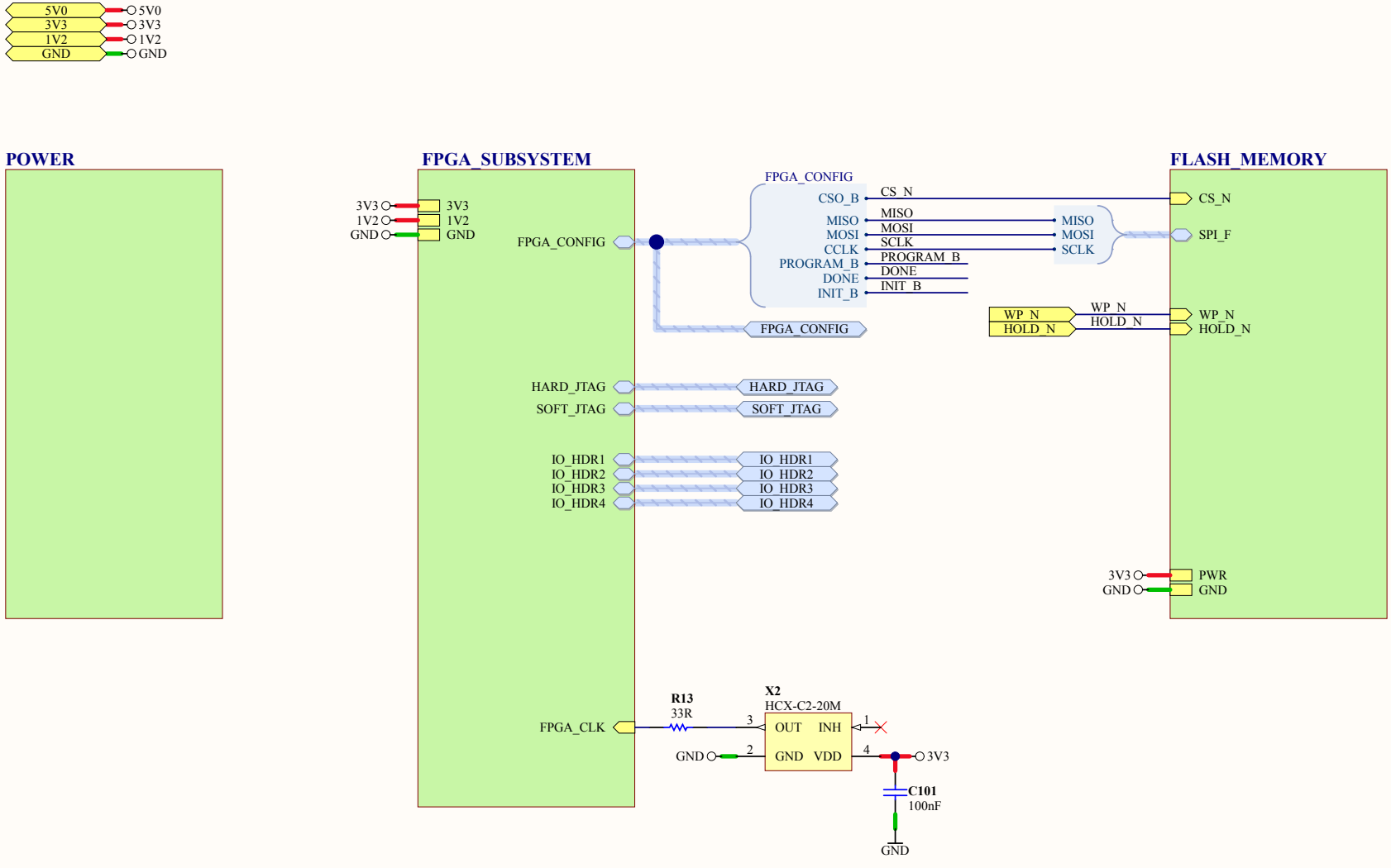
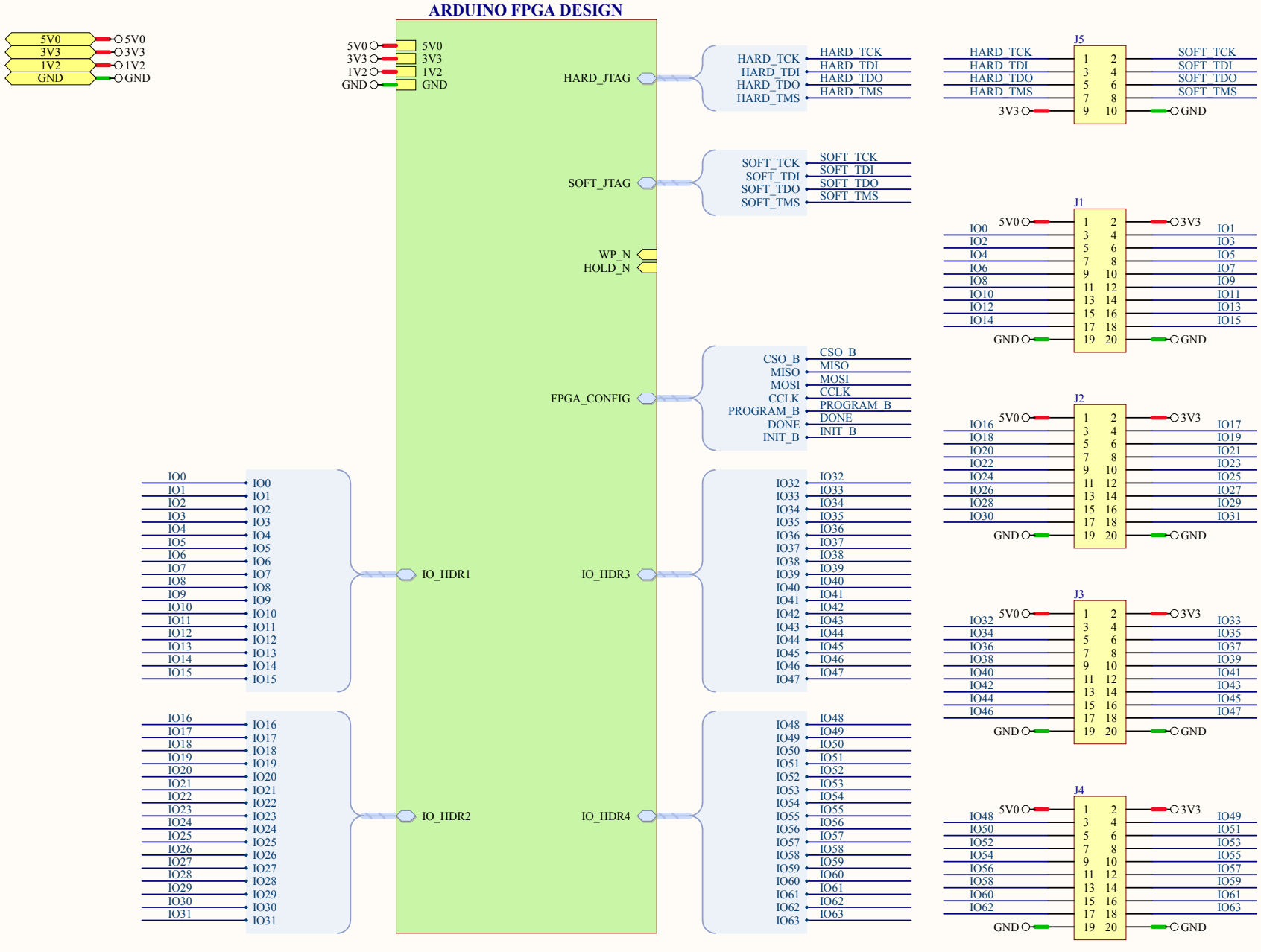
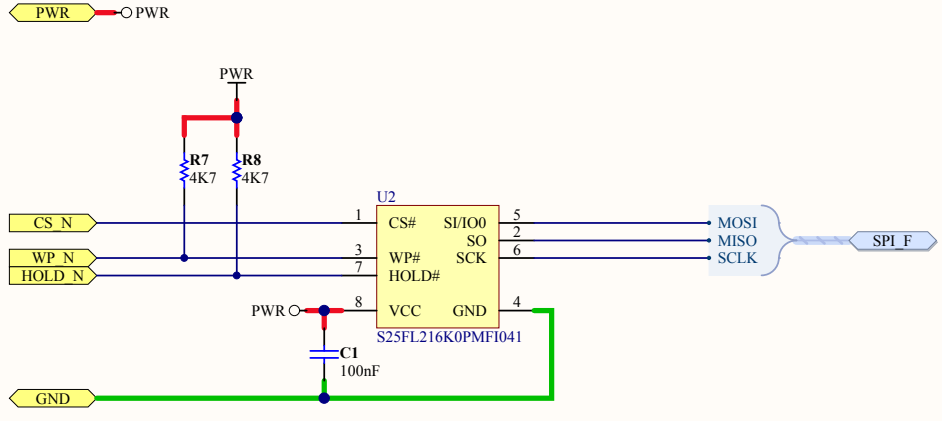

5V0
3V3
1V2
GND
POWER
FPGA_SUBSYSTEM
FLASH_MEMORY
FPGA_CONFIG
CSO_B
MISO
MOSI
CCLK
PROGRAM_B
DONE
INIT_B
CS_N
SPI_F
WP_N
HOLD_N
HARD_JTAG
SOFT_JTAG
IO_HDR1
IO_HDR2
IO_HDR3
IO_HDR4
PWR
FPGA_CLK
R13
33R
X2
HCX-C2-20M
OUT
INH
VDD
C101
100nF

TBD :)


ARDUINO FPGA DESIGN
5V0
3V3
1V2
GND
HARD_JTAG
SOFT_JTAG
WP_N
HOLD_N
FPGA_CONFIG
IO_HDR1
IO_HDR2
IO_HDR3
IO_HDR4
HARD_TCK
HARD_TDI
HARD_TDO
HARD_TMS
SOFT_TCK
SOFT_TDI
SOFT_TDO
SOFT_TMS
CSO_B
MISO
MOSI
CCLK
PROGRAM_B
DONE
INIT_B
J1
J2
J3
J4
J5

**Power Supply 2V4 to 3V7**




| | | |
|---|---|---|
| Title | | |
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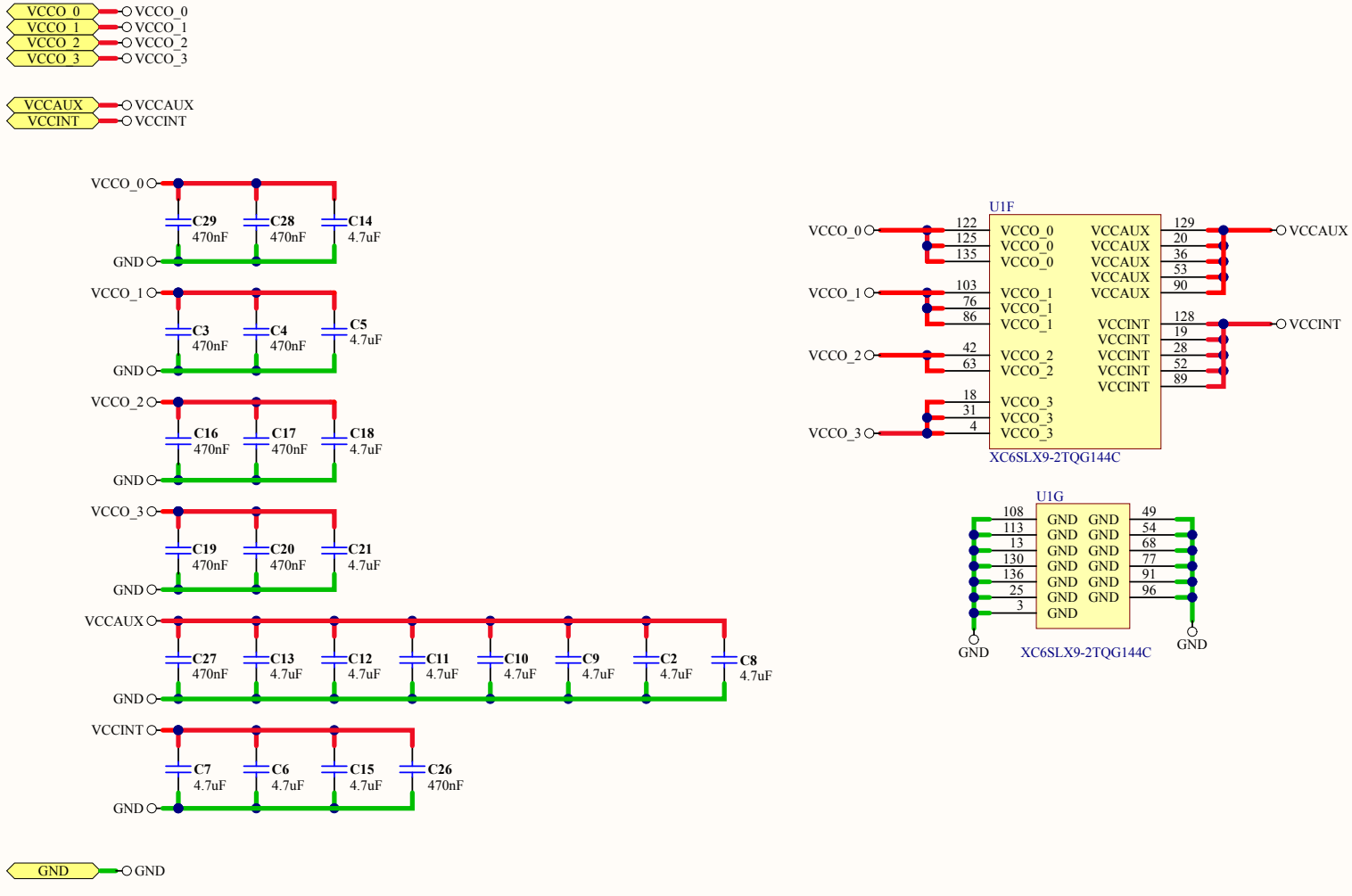
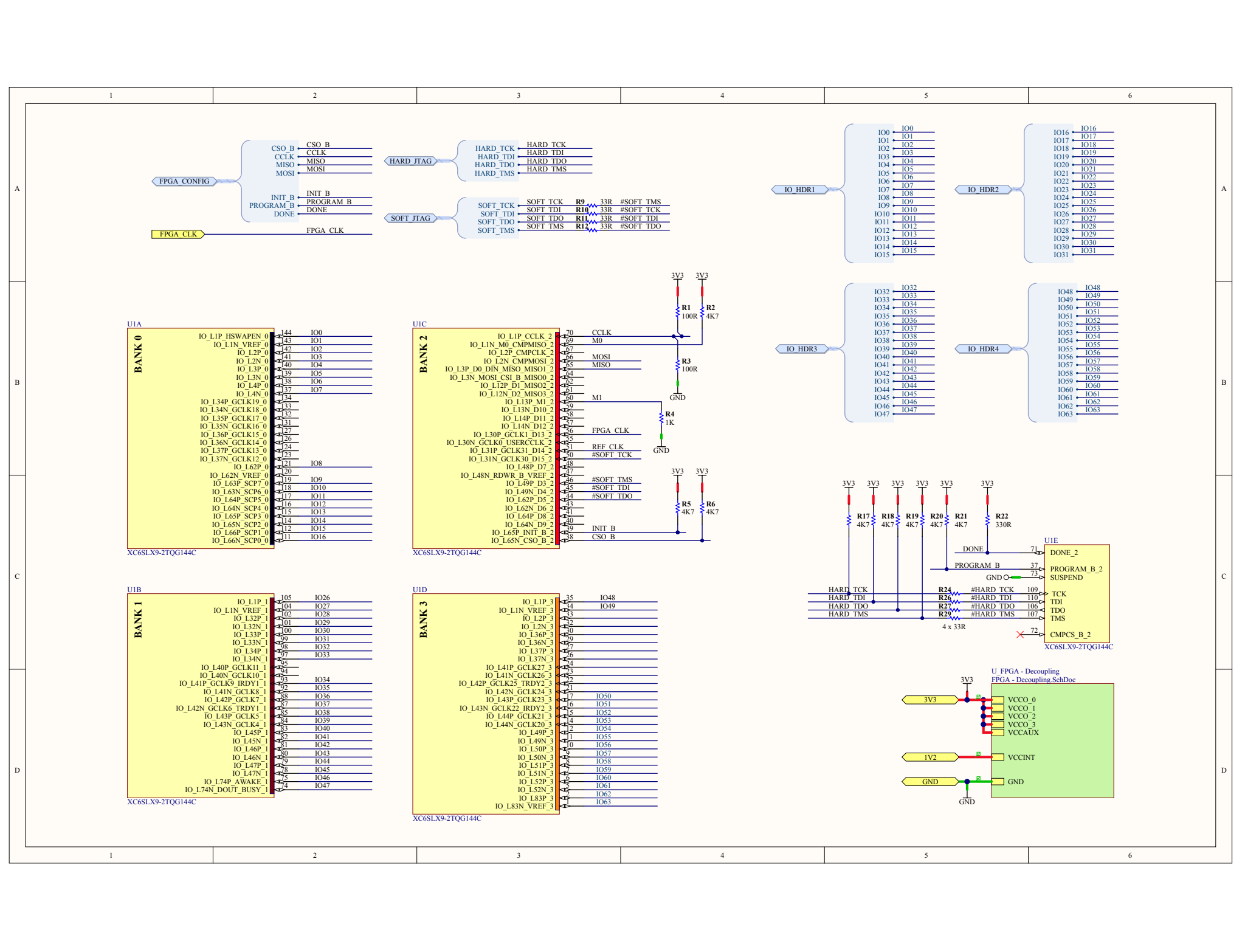
| Date: 3/1/2014 | Sheet of | |
| File: C:\Code\..\Flash - S25FL216K0PMFI041.SchDoc | Drawn By: | |


VCCO_0
VCCO_1
VCCO_2
VCCO_3
VCCAUX
VCCINT
GND
C29 470nF
C28 470nF
C14 4.7uF
C3 470nF
C4 470nF
C5 4.7uF
C16 470nF
C17 470nF
C18 4.7uF
C19 470nF
C20 470nF
C21 4.7uF
C27 470nF
C13 4.7uF
C12 4.7uF
C11 4.7uF
C10 4.7uF
C9 4.7uF
C2 4.7uF
C8 4.7uF
C7 4.7uF
C6 4.7uF
C15 4.7uF
C26 470nF
U1F
XC6SLX9-2TQG144C
U1G
XC6SLX9-2TQG144C


FPGA_CONFIG
CSO_B
CCLK
MISO
MOSI
INIT_B
PROGRAM_B
DONE
FPGA_CLK
HARD_JTAG
HARD_TCK
HARD_TDI
HARD_TDO
HARD_TMS
SOFT_JTAG
SOFT_TCK
SOFT_TDI
SOFT_TDO
SOFT_TMS
R9 33R #SOFT_TMS
R10 33R #SOFT_TCK
R11 33R #SOFT_TDI
R12 33R #SOFT_TDO
IO_HDR1
IO_HDR2
IO_HDR3
IO_HDR4
U1A
BANK 0
XC6SLX9-2TQG144C
U1C
BANK 2
3V3
R1 100R
R2 4K7
R3 100R
R4 1K
R5 4K7
R6 4K7
GND
U1B
BANK 1
U1D
BANK 3
R17 4K7
R18 4K7
R19 4K7
R20 4K7
R21 4K7
R22 330R
R24 #HARD_TCK
R26 #HARD_TDI
R27 #HARD_TDO
R29 #HARD_TMS
4 x 33R
U1E
DONE_2
PROGRAM_B_2
SUSPEND
TCK
TDI
TDO
TMS
CMPCS_B_2
U_FPGA - Decoupling
FPGA - Decoupling.SchDoc
VCCO_0
VCCO_1
VCCO_2
VCCO_3
VCCAUX
VCCINT
1V2