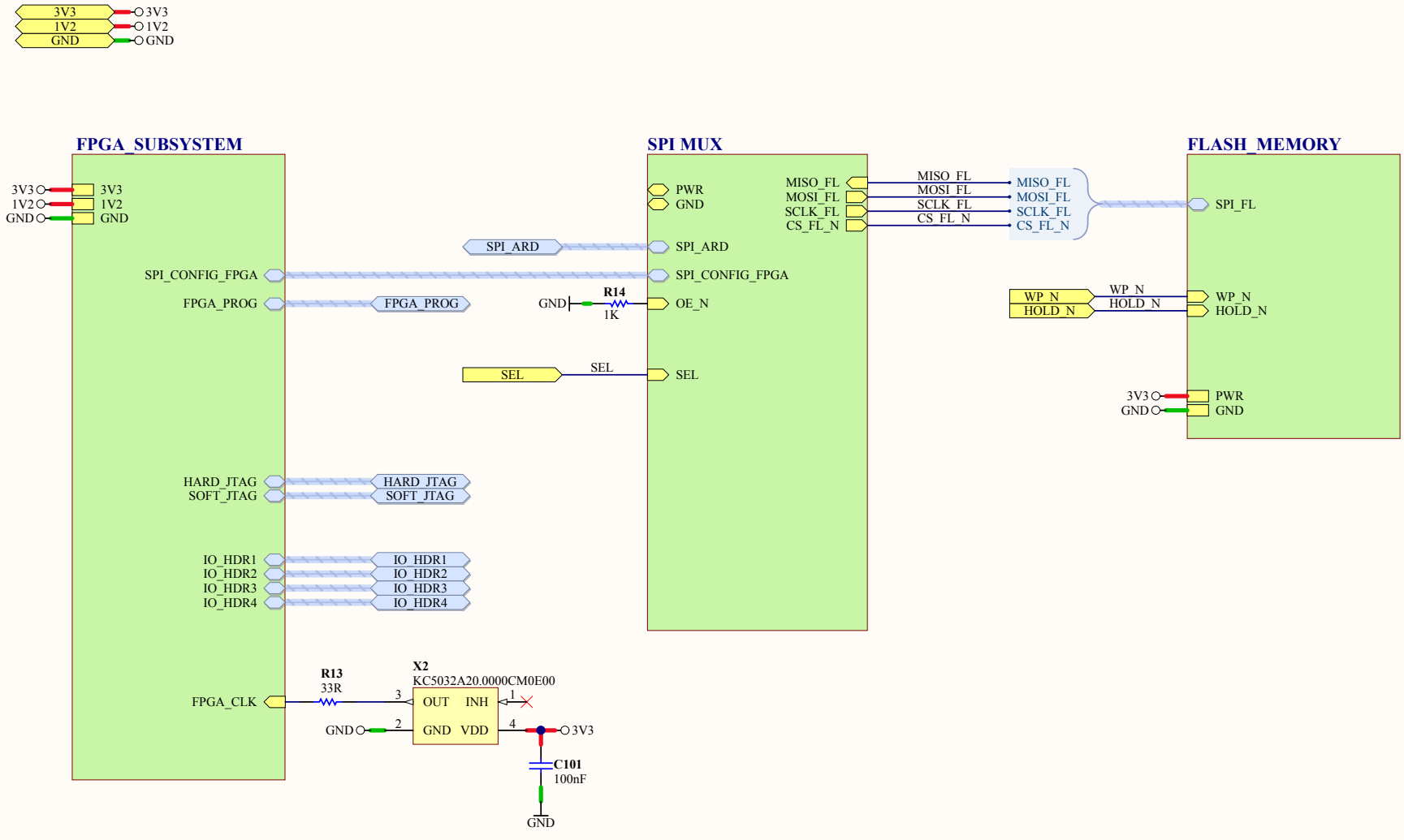
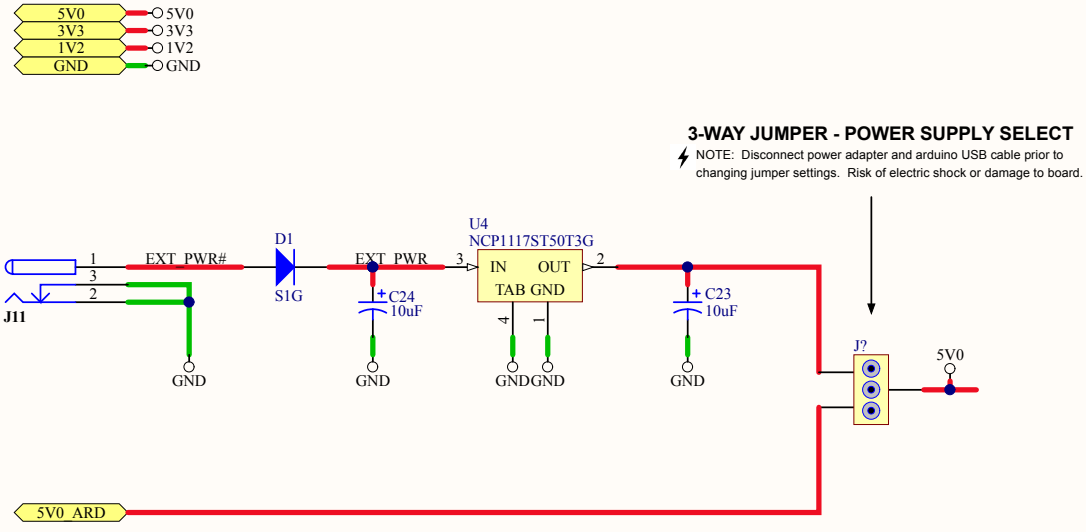
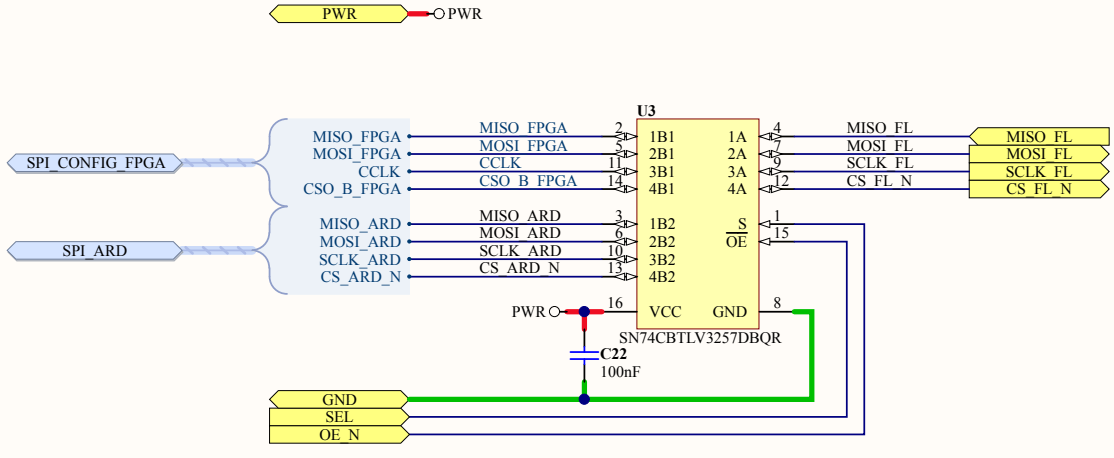
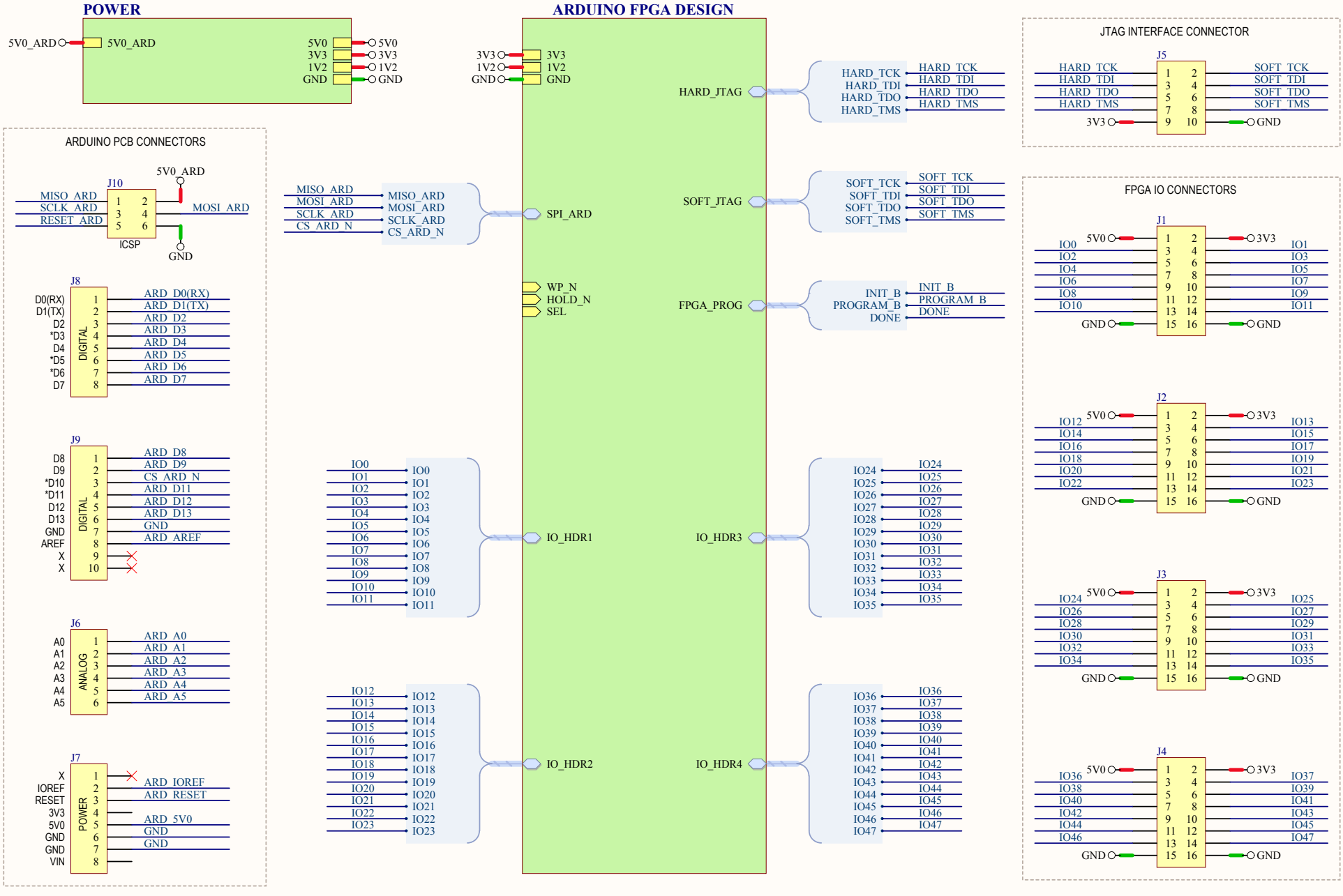
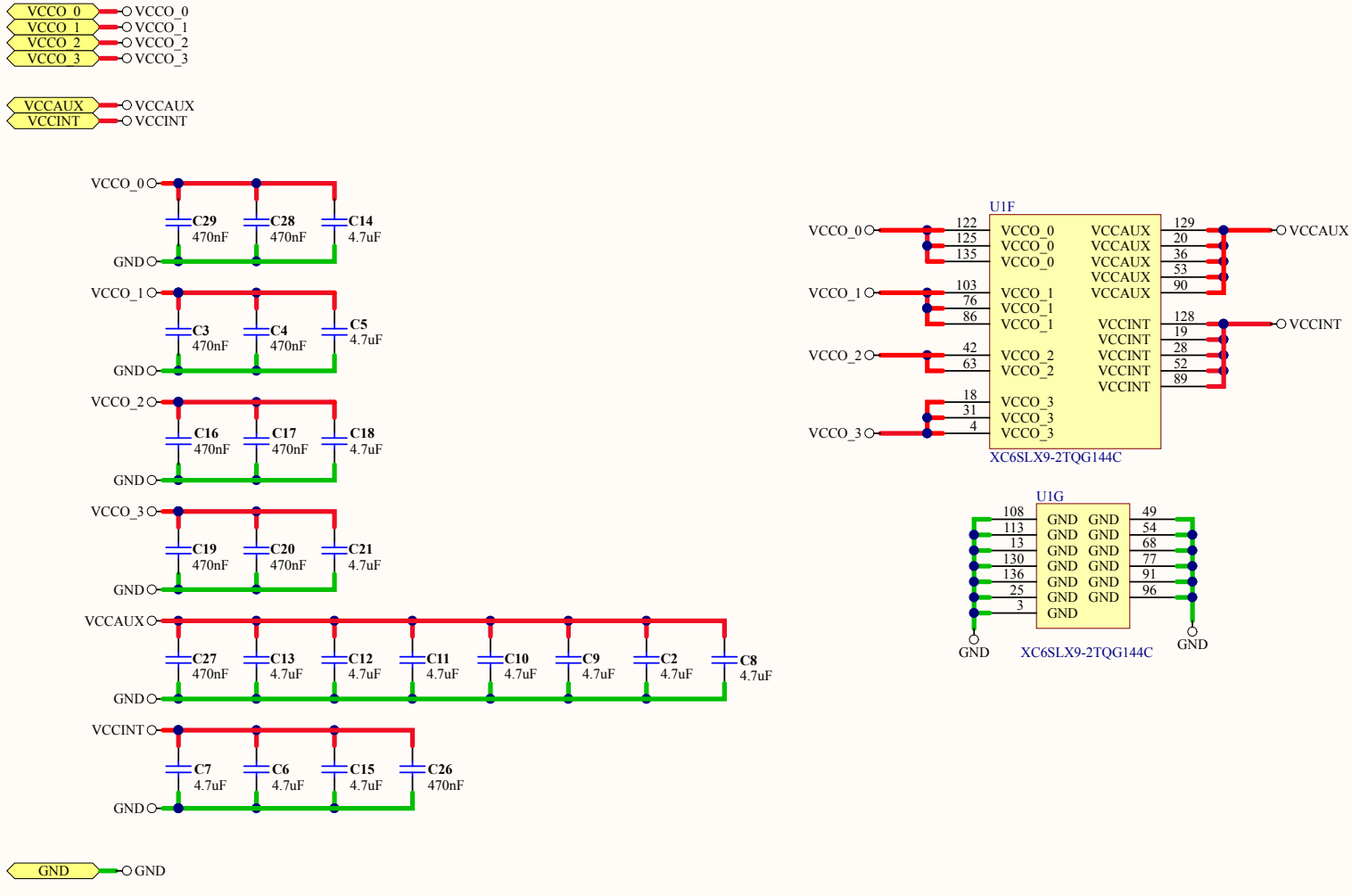
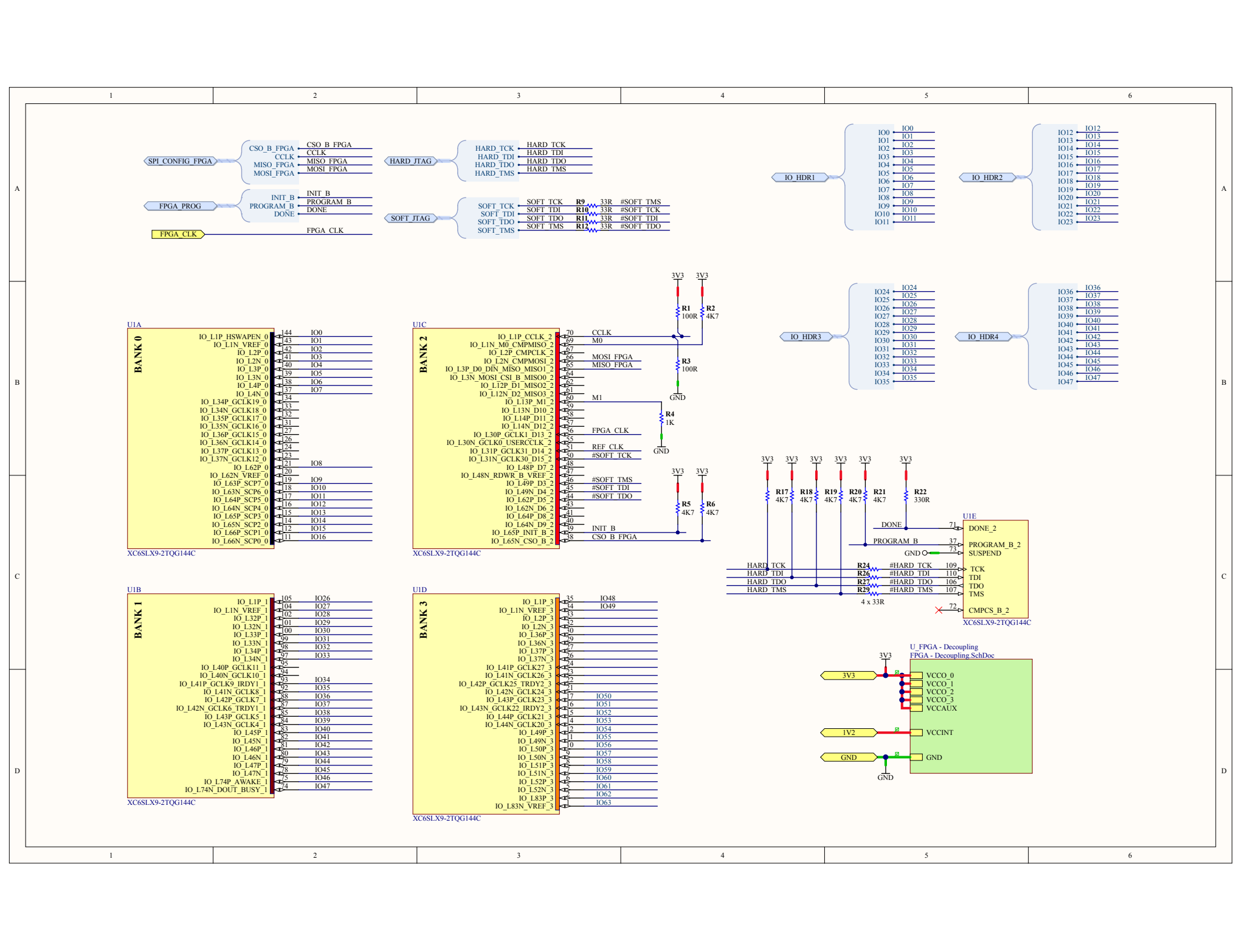

3V3
1V2
GND
3V3
1V2
GND
FPGA_SUBSYSTEM
SPI MUX
FLASH_MEMORY
SPI_CONFIG_FPGA
FPGA_PROG
SEL
HARD_JTAG
SOFT_JTAG
IO_HDR1
IO_HDR2
IO_HDR3
IO_HDR4
FPGA_CLK
SPI_ARD
PWR
OE_N
MISO_FL
MOSI_FL
SCLK_FL
CS_FL_N
WP_N
HOLD_N
R14
1K
R13
33R
X2
KC5032A20.0000CM0E00
OUT
INH
GND
VDD
C101
100nF

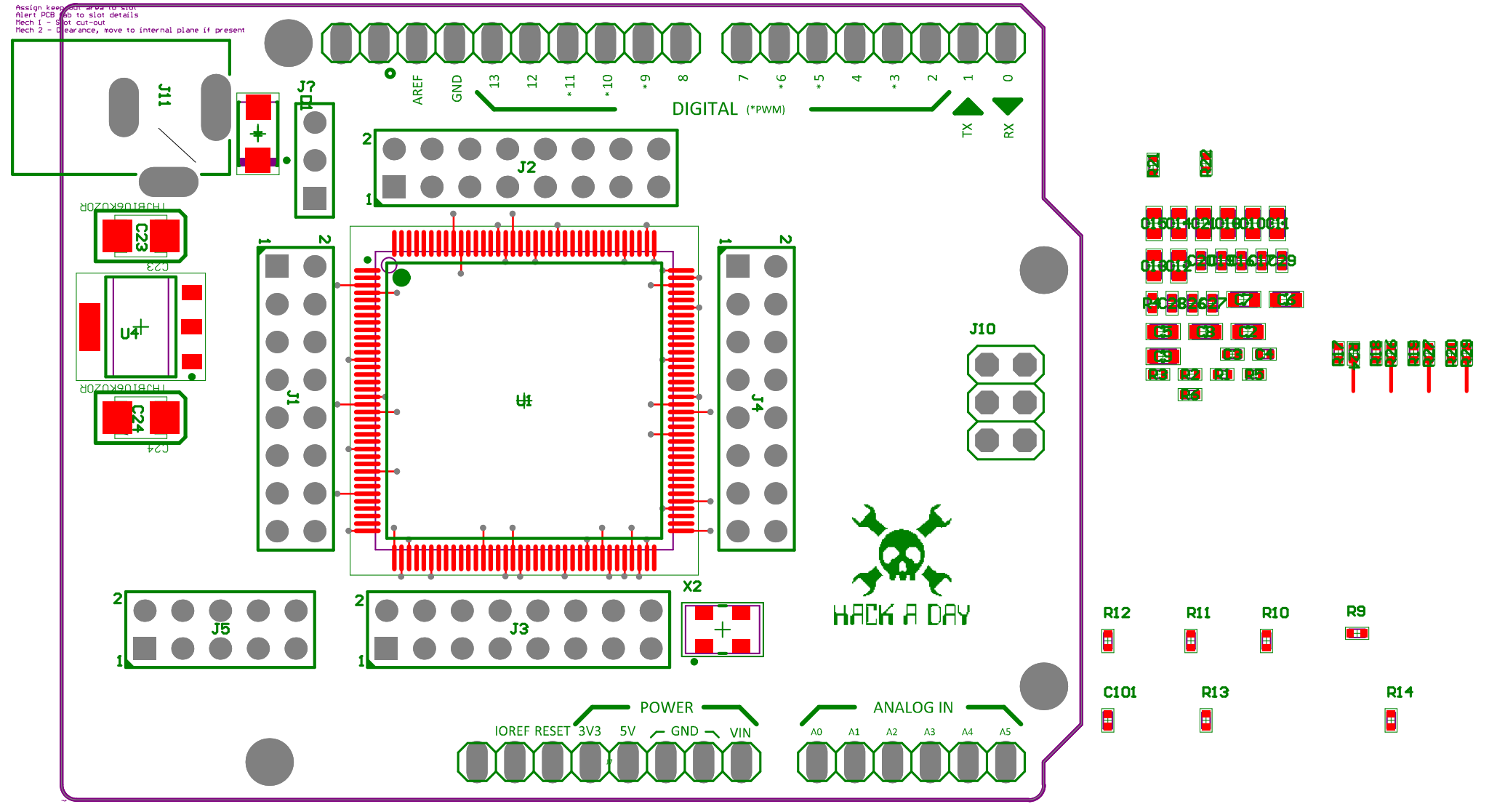

5V0
3V3
1V2
GND
5V0
3V3
1V2
GND
3-WAY JUMPER - POWER SUPPLY SELECT
NOTE: Disconnect power adapter and arduino USB cable prior to changing jumper settings. Risk of electric shock or damage to board.
J11
1
3
2
EXT_PWR#
D1
S1G
EXT_PWR
C24
10uF
U4
NCP1117ST50T3G
IN
OUT
TAB
GND
3
2
4
1
C23
10uF
J?
5V0
GND
GND
GND
GND
GND
5V0_ARD


PWR
PWR
U3
SPI_CONFIG_FPGA
MISO_FPGA
MOSI_FPGA
CCLK
CSO_B_FPGA
SPI_ARD
MISO_ARD
MOSI_ARD
SCLK_ARD
CS_ARD_N
MISO_FPGA 2
MOSI_FPGA 5
CCLK 11
CSO_B_FPGA 14
MISO_ARD 3
MOSI_ARD 6
SCLK_ARD 10
CS_ARD_N 13
1B1
2B1
3B1
4B1
1B2
2B2
3B2
4B2
1A
2A
3A
4A
S
OE
4
7
9
12
1
15
MISO_FL
MOSI_FL
SCLK_FL
CS_FL_N
MISO_FL
MOSI_FL
SCLK_FL
CS_FL_N
PWR
16
VCC
GND
8
SN74CBTLV3257DBQR
C22
100nF
GND
SEL
OE_N


POWER
5V0_ARD
5V0_ARD
5V0
3V3
1V2
GND
ARDUINO FPGA DESIGN
3V3
1V2
GND
HARD_JTAG
HARD_TCK
HARD_TDI
HARD_TDO
HARD_TMS
SOFT_JTAG
SOFT_TCK
SOFT_TDI
SOFT_TDO
SOFT_TMS
FPGA_PROG
INIT_B
PROGRAM_B
DONE
WP_N
HOLD_N
SEL
SPI_ARD
MISO_ARD
MOSI_ARD
SCLK_ARD
CS_ARD_N
IO_HDR1
IO_HDR2
IO_HDR3
IO_HDR4
JTAG INTERFACE CONNECTOR
J5
SOFT_TCK
SOFT_TDI
SOFT_TDO
SOFT_TMS
FPGA IO CONNECTORS
J1
J2
J3
J4
ARDUINO PCB CONNECTORS
J10
ICSP
MOSI_ARD
RESET_ARD
J8
DIGITAL
ARD_D0(RX)
ARD_D1(TX)
ARD_D2
ARD_D3
ARD_D4
ARD_D5
ARD_D6
ARD_D7
J9
ARD_D8
ARD_D9
CS_ARD_N
ARD_D11
ARD_D12
ARD_D13
ARD_AREF
J6
ANALOG
ARD_A0
ARD_A1
ARD_A2
ARD_A3
ARD_A4
ARD_A5
J7
POWER
ARD_IOREF
ARD_RESET
ARD_5V0


VCCO_0
VCCO_1
VCCO_2
VCCO_3
VCCAUX
VCCINT
GND
C29 470nF
C28 470nF
C14 4.7uF
C3 470nF
C4 470nF
C5 4.7uF
C16 470nF
C17 470nF
C18 4.7uF
C19 470nF
C20 470nF
C21 4.7uF
C27 470nF
C13 4.7uF
C12 4.7uF
C11 4.7uF
C10 4.7uF
C9 4.7uF
C2 4.7uF
C8 4.7uF
C7 4.7uF
C6 4.7uF
C15 4.7uF
C26 470nF
U1F
XC6SLX9-2TQG144C
U1G
XC6SLX9-2TQG144C


SPI_CONFIG_FPGA
CSO_B_FPGA
CCLK
MISO_FPGA
MOSI_FPGA
FPGA_PROG
INIT_B
PROGRAM_B
DONE
FPGA_CLK
HARD_JTAG
HARD_TCK
HARD_TDI
HARD_TDO
HARD_TMS
SOFT_JTAG
SOFT_TCK
SOFT_TDI
SOFT_TDO
SOFT_TMS
R9 33R #SOFT_TMS
R10 33R #SOFT_TCK
R11 33R #SOFT_TDI
R12 33R #SOFT_TDO
IO_HDR1
IO_HDR2
IO_HDR3
IO_HDR4
U1A
BANK 0
XC6SLX9-2TQG144C
U1B
BANK 1
XC6SLX9-2TQG144C
U1C
BANK 2
CCLK
M0
MOSI_FPGA
MISO_FPGA
M1
FPGA_CLK
REF_CLK
#SOFT_TCK
#SOFT_TMS
#SOFT_TDI
#SOFT_TDO
INIT_B
CSO_B_FPGA
R1 100R
R2 4K7
R3 100R
R4 1K
R5 4K7
R6 4K7
XC6SLX9-2TQG144C
U1D
BANK 3
XC6SLX9-2TQG144C
R17 4K7
R18 4K7
R19 4K7
R20 4K7
R21 4K7
R22 330R
R24 #HARD_TCK
R26 #HARD_TDI
R27 #HARD_TDO
R29 #HARD_TMS
4 x 33R
U1E
DONE_2
PROGRAM_B_2
SUSPEND
TCK
TDI
TDO
TMS
CMPCS_B_2
XC6SLX9-2TQG144C
U_FPGA - Decoupling
FPGA - Decoupling.SchDoc
VCCO_0
VCCO_1
VCCO_2
VCCO_3
VCCAUX
VCCINT
GND
3V3
1V2


Assign keepout area to slot
Alert PCB fab to slot details
Mech 1 - Slot cut-out
Mech 2 - Clearance, move to internal plane if present
J11
J?
AREF
GND
13
12
*11
*10
*9
8
7
*6
*5
4
*3
2
1
0
DIGITAL (*PWM)
TX
RX
J2
C23
U4
C24
J1
J4
J10
J5
J3
X2
HACK A DAY
POWER
IOREF RESET 3V3 5V GND VIN
ANALOG IN
A0 A1 A2 A3 A4 A5
R12
R11
R10
R9
C101
R13
R14