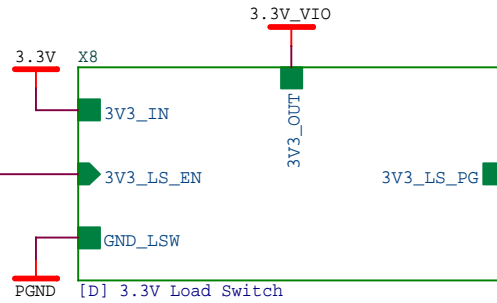
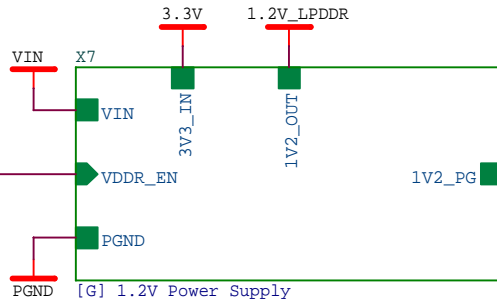
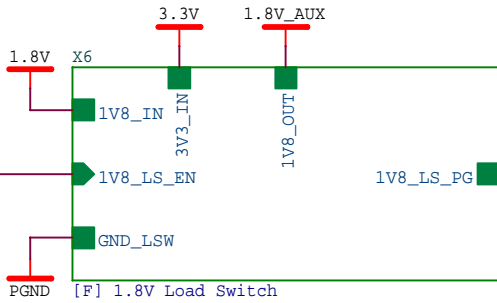
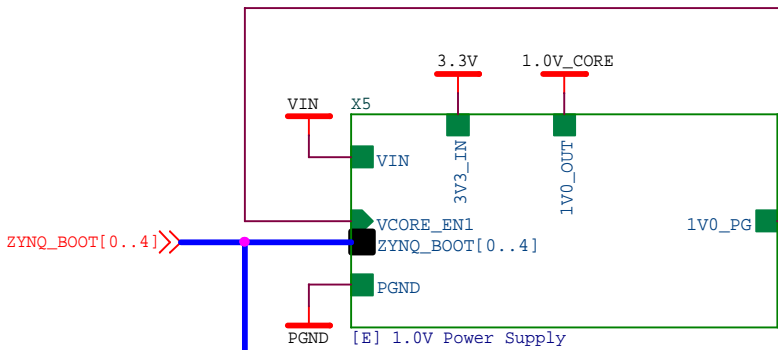
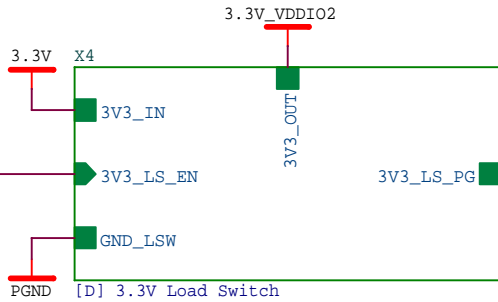
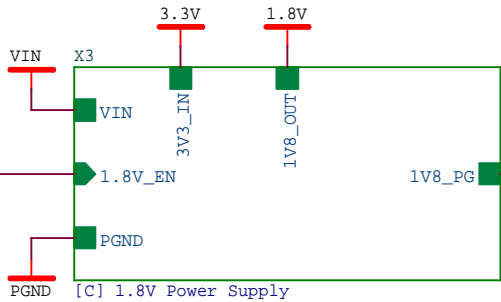
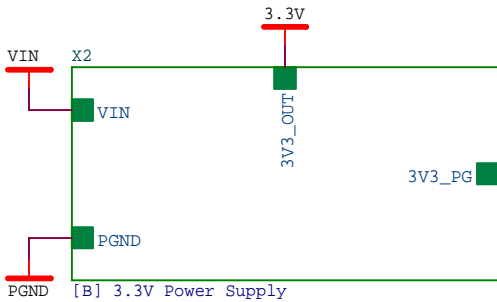
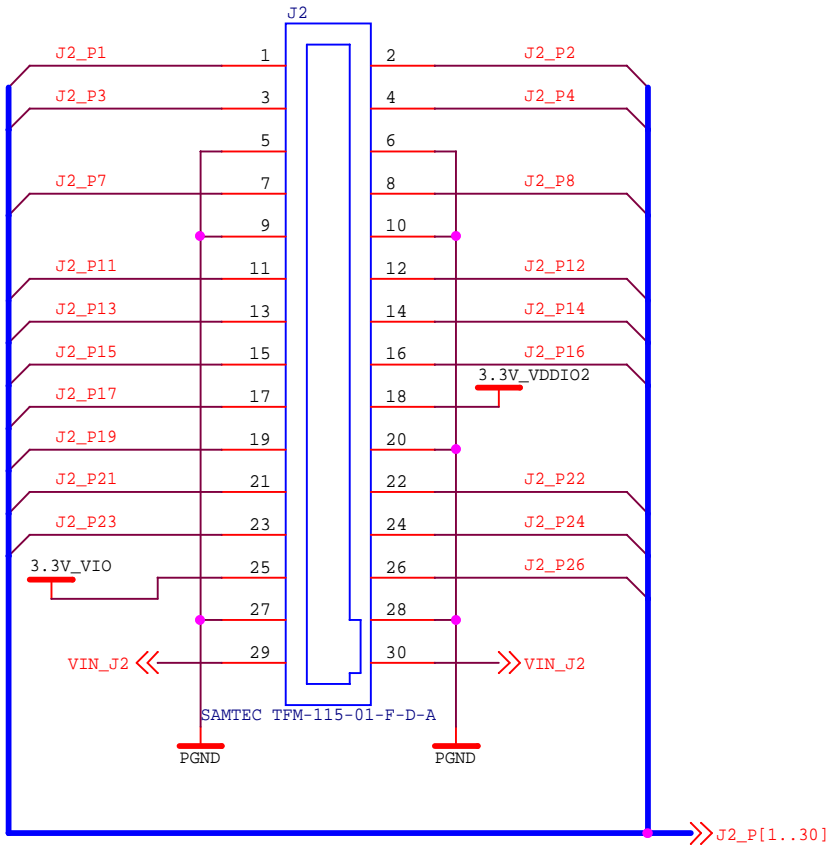
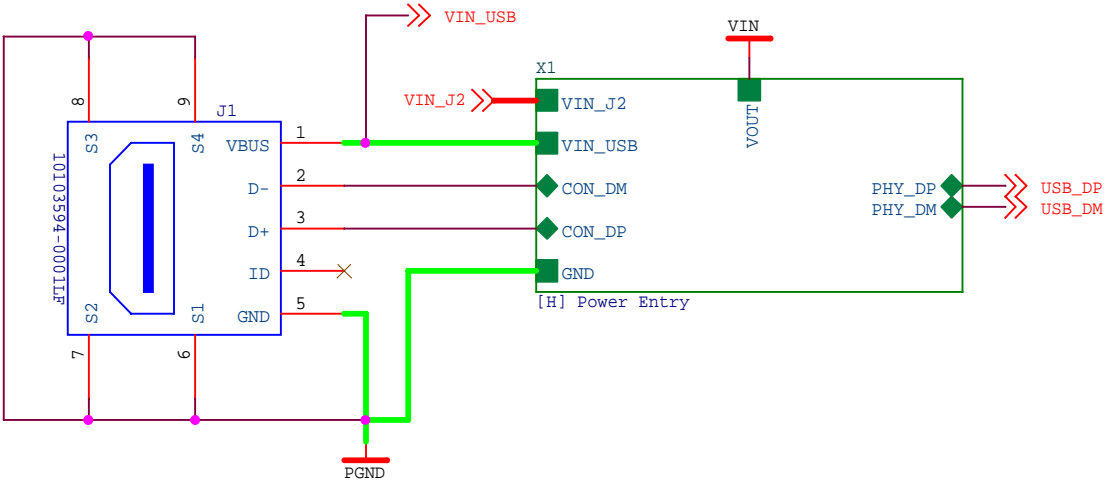


Rev.	Description	CO Number	Date	Approved By	Checked By
2	Alpha Prototype	00001	09/01/2015	JJW	BEH

Power/JTAG/SWD/BT Audio/I2C/DAC/ADC



Minimum Trace Ratings	
6000mA	Orange
4000mA	Red
2000mA	Green
1000mA	Purple
200mA	Pink

Minimum Plane Ratings	
+VIN	4000mA
+3.3V	4000mA
+1.8V	2000mA
+3.3V_VDDIO2	4000mA
+1.0V_CORE	6000mA
+1.8V_AUX	2000mA
+1.2V_LPDDR	2000mA
+3.3V_VIO	4000mA



krtkl inc.
350 Townsend Street
Suite 301A
San Francisco, CA 94107
+1 415 857 4857

TITLE snickerdoodle FPGA Module
PATH /
DESCRIPTION Top Level Block Diagram

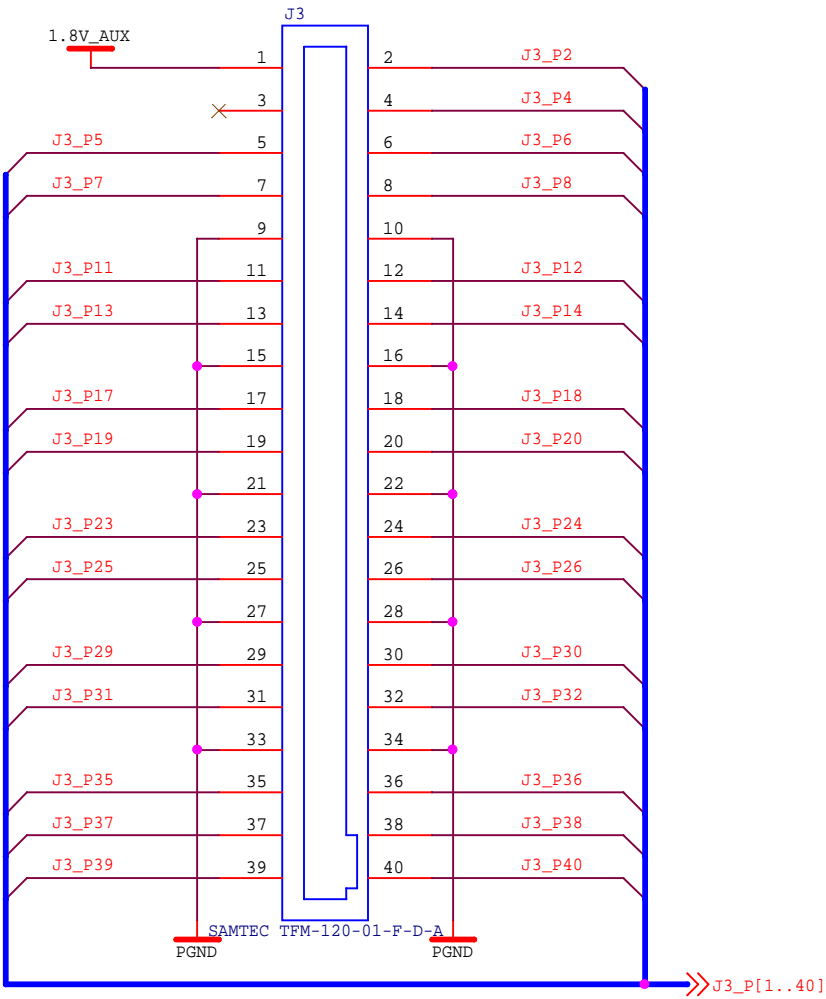


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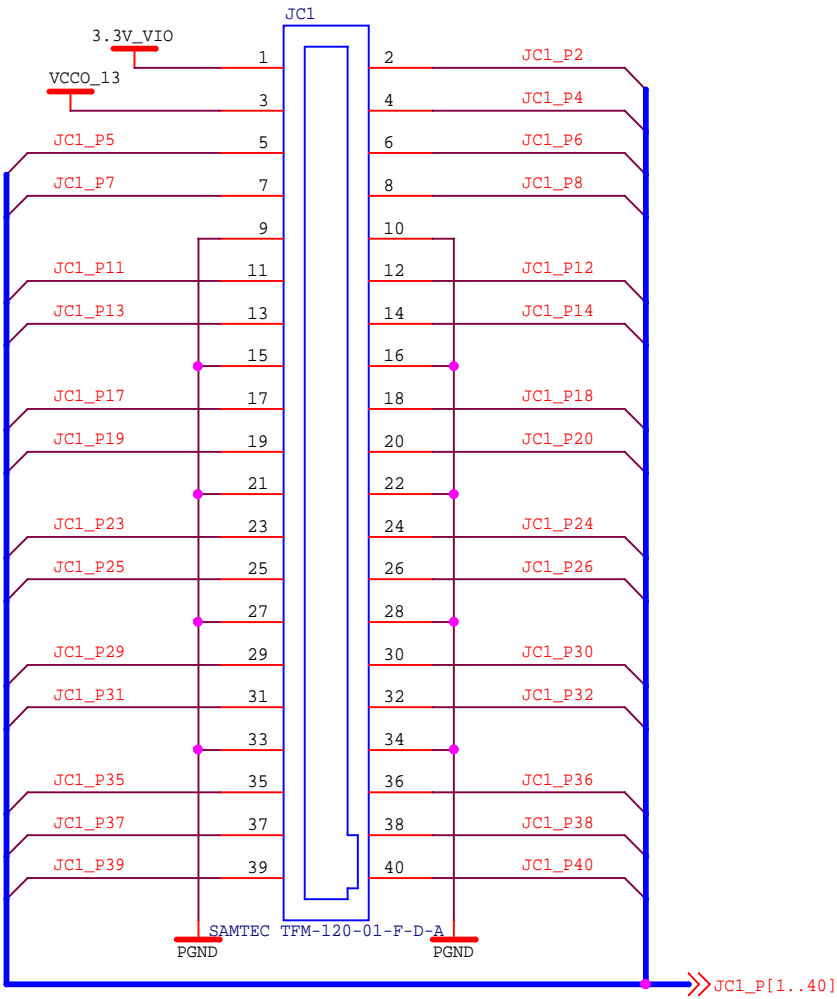
	NAME	DATE
DRAWN BY	J. Weatherbee	08/17/2015
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

SIZE	DRAWING NO.	REV
B	15081800-01	2
SHEET 1 OF 30		

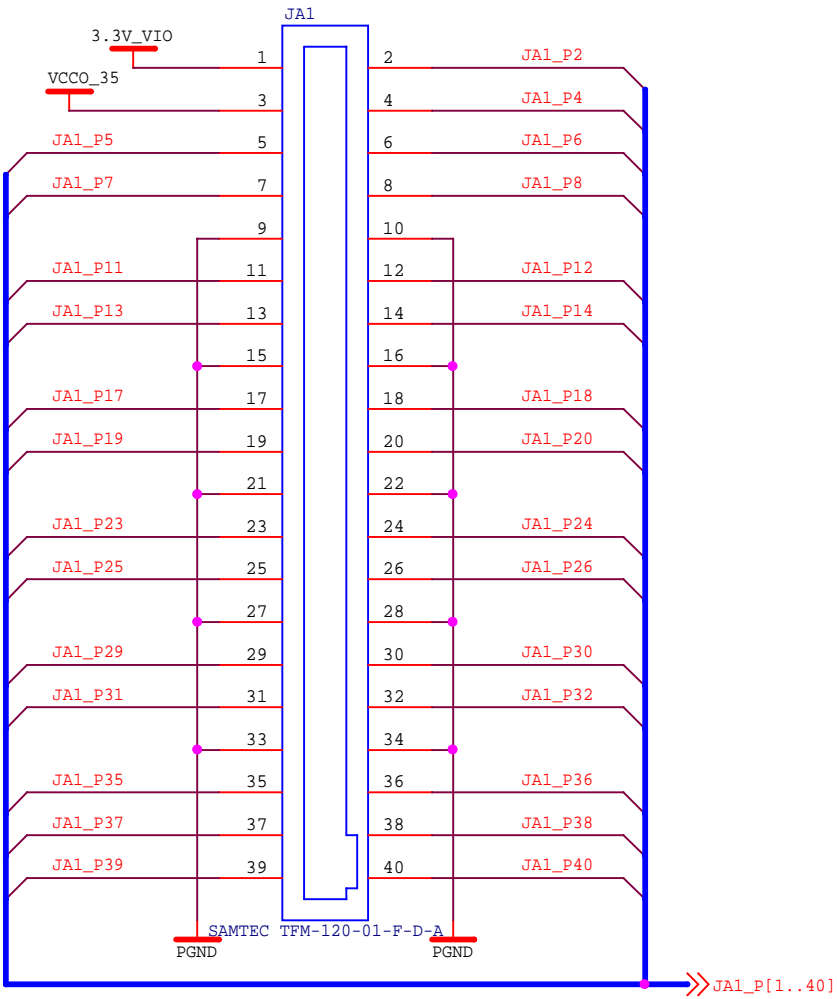
CPU GPIO/USB ULPI/GigE RGMII/SPI/I2C/UART/CAN

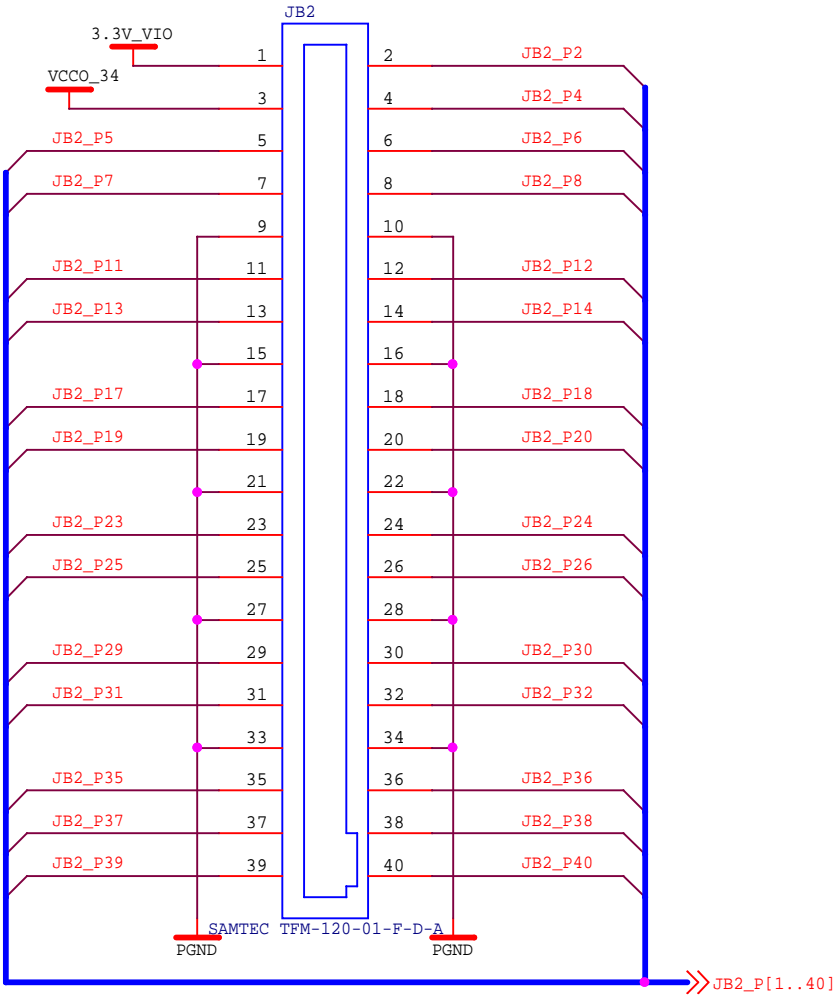
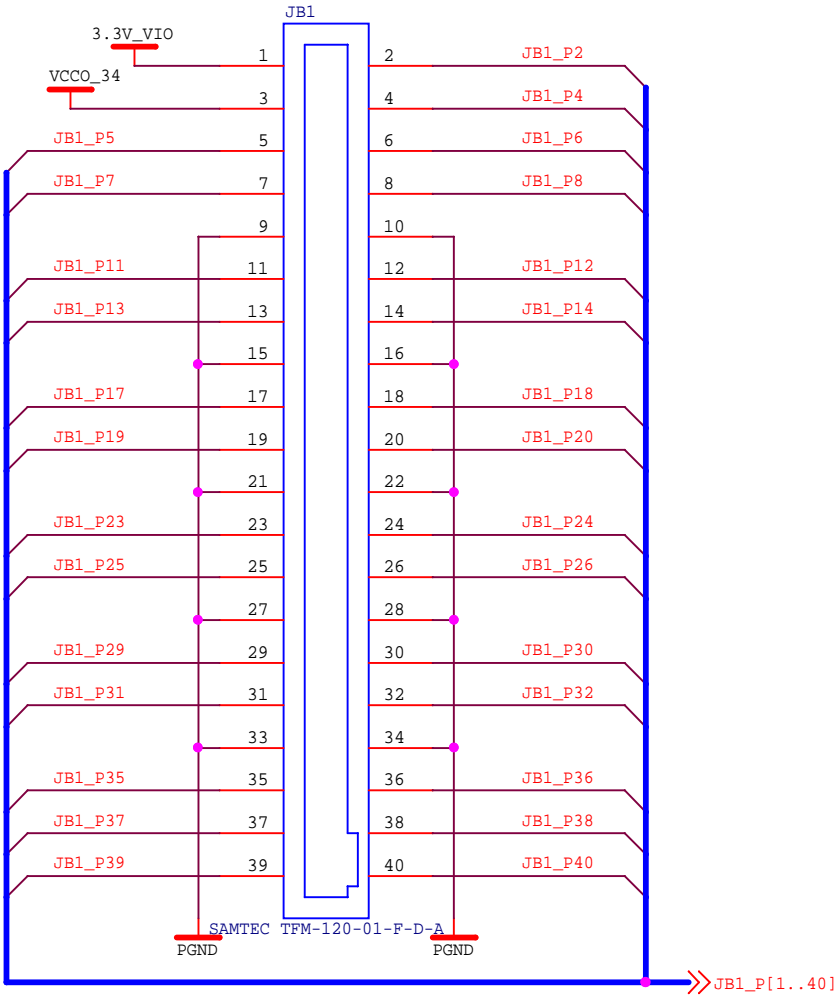
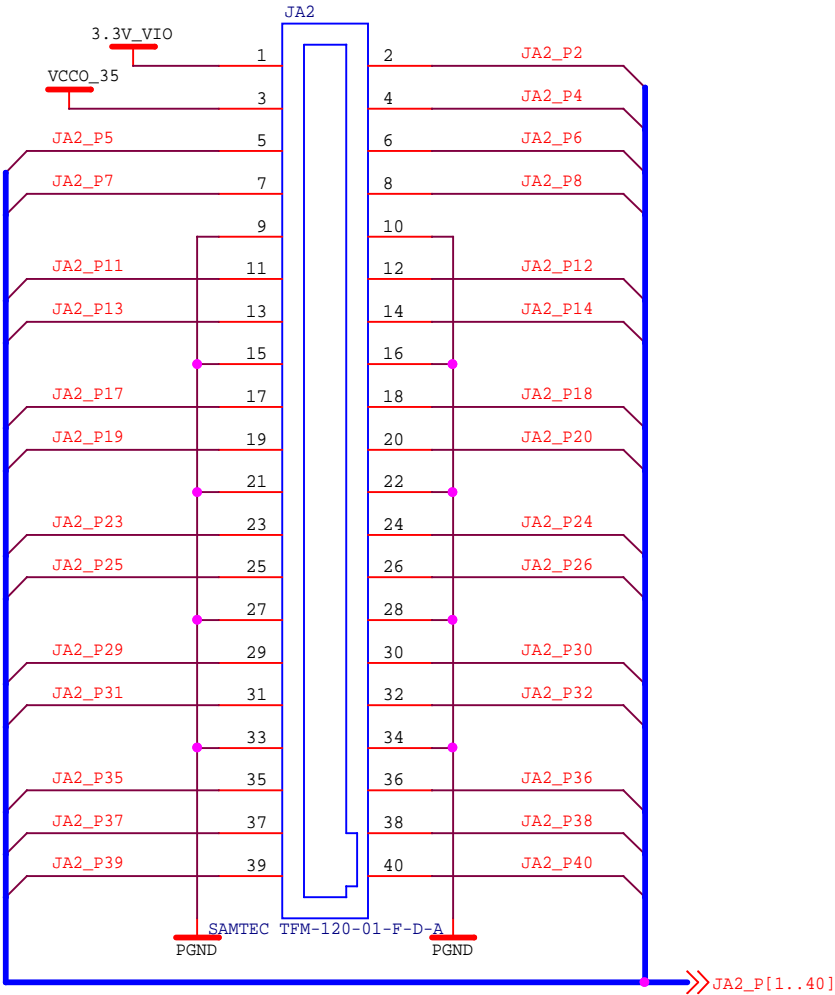


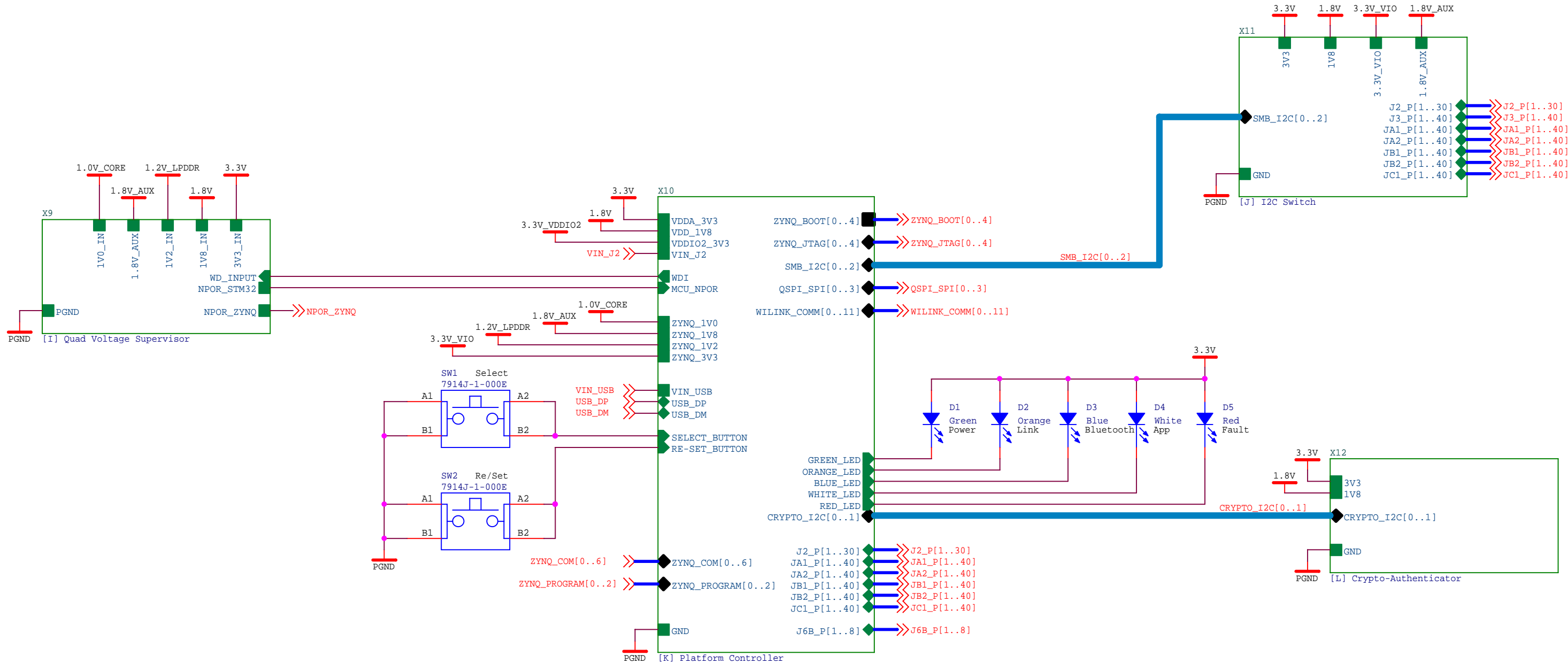
FPGA I/O

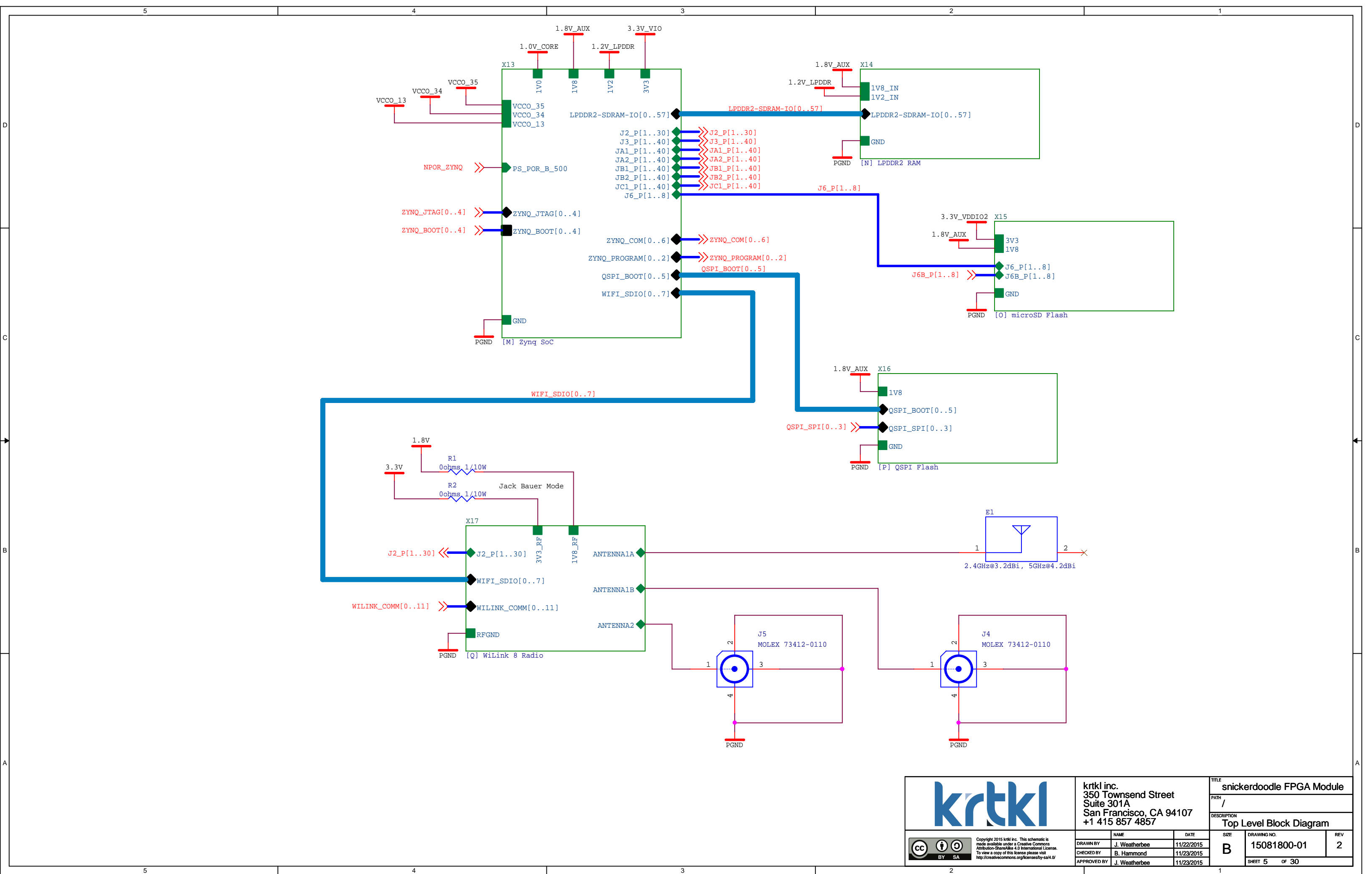


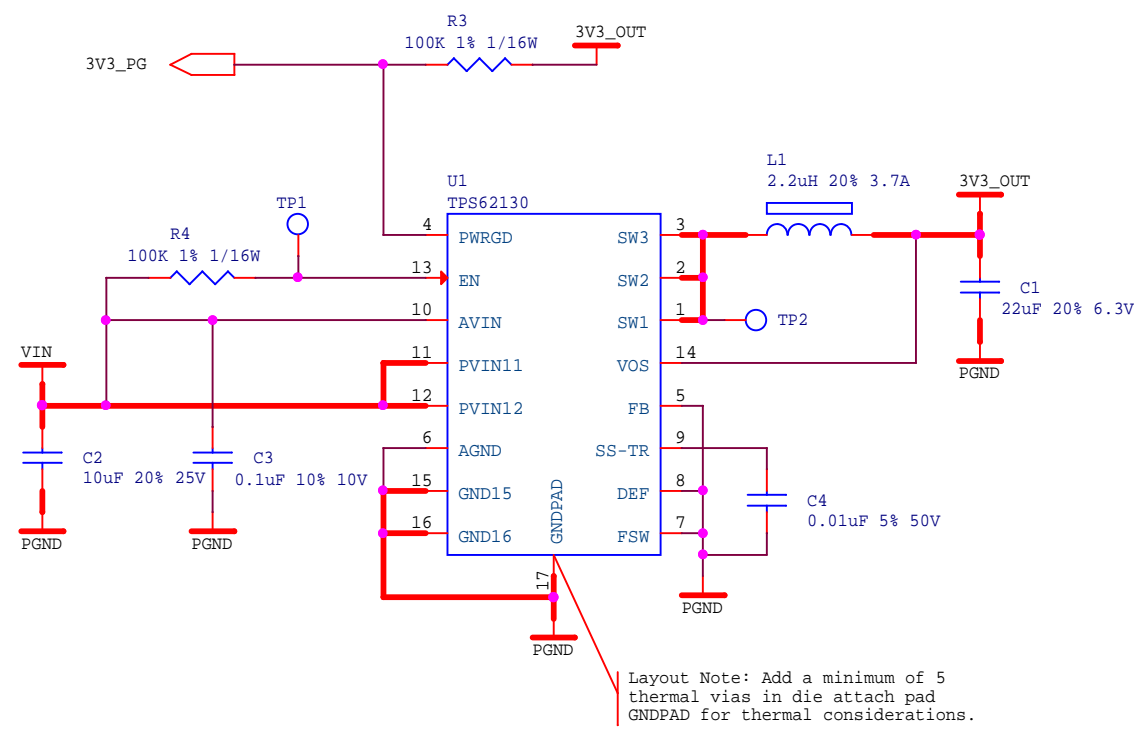
FPGA I/O



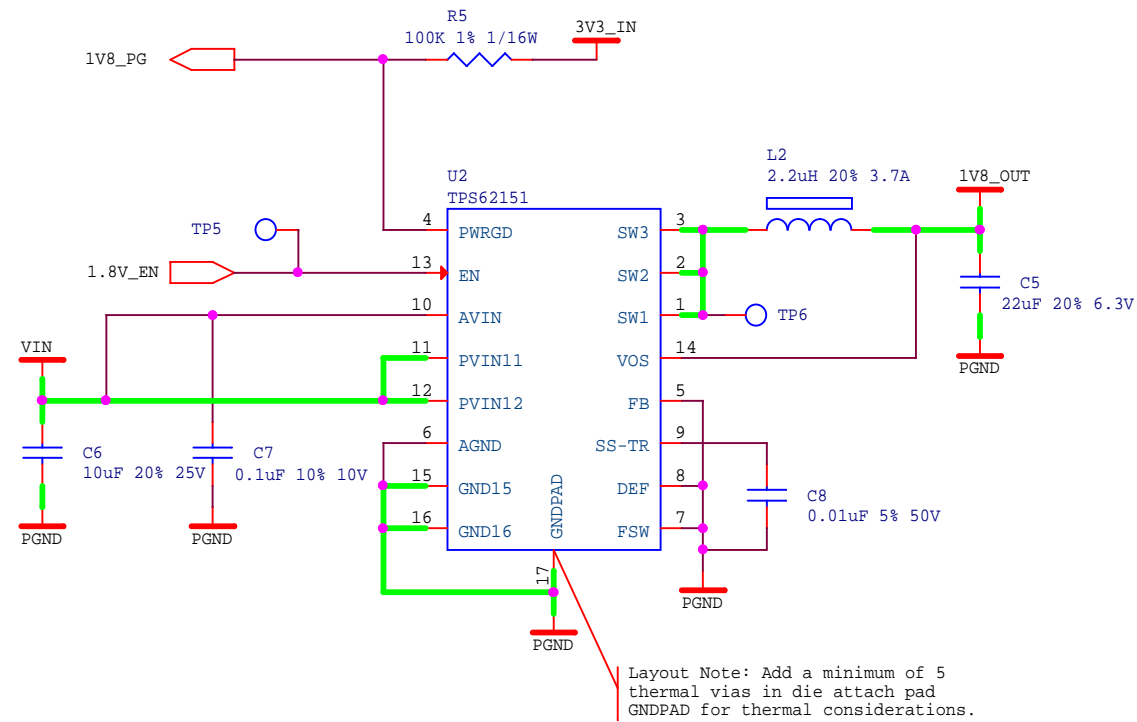




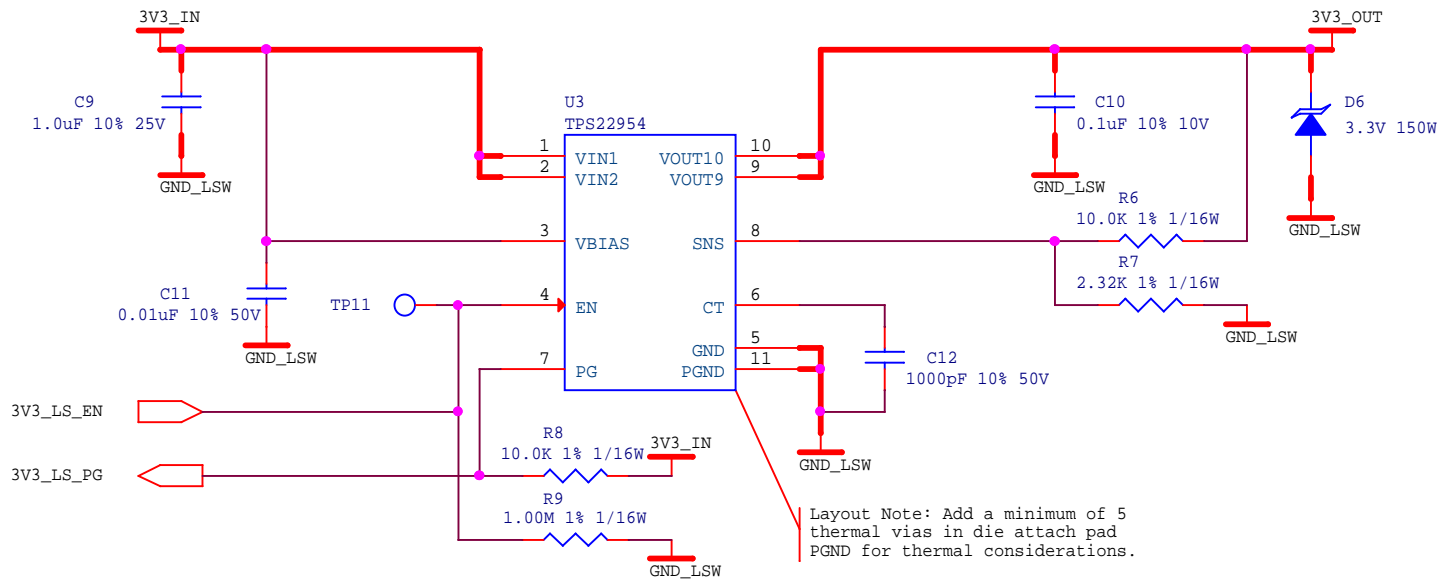




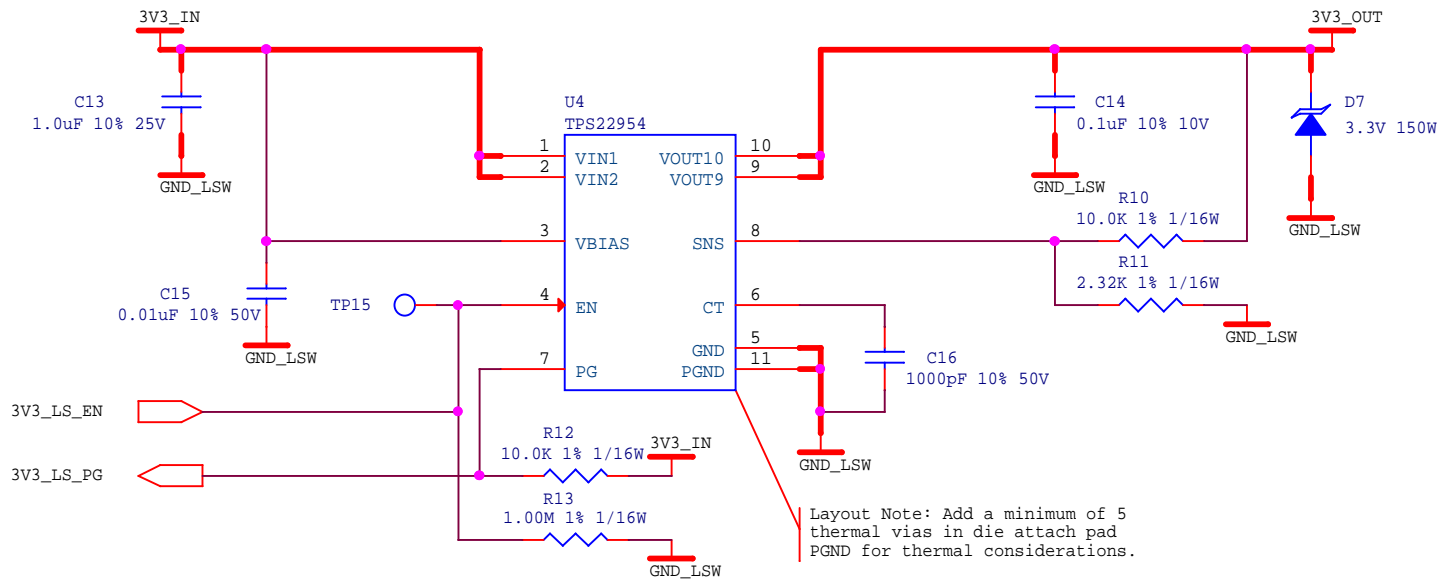
		krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857		TITLE snickerdoodle FPGA Module	
				PATH /X2	
				DESCRIPTION 3.3V Power Supply	
	DRAWN BY	B. Hammond	DATE	SIZE B	DRAWING NO. 15081800-01
	CHECKED BY	J. Weatherbee	11/23/2015		REV 2
	APPROVED BY	J. Weatherbee	11/23/2015		SHEET 6 OF 30



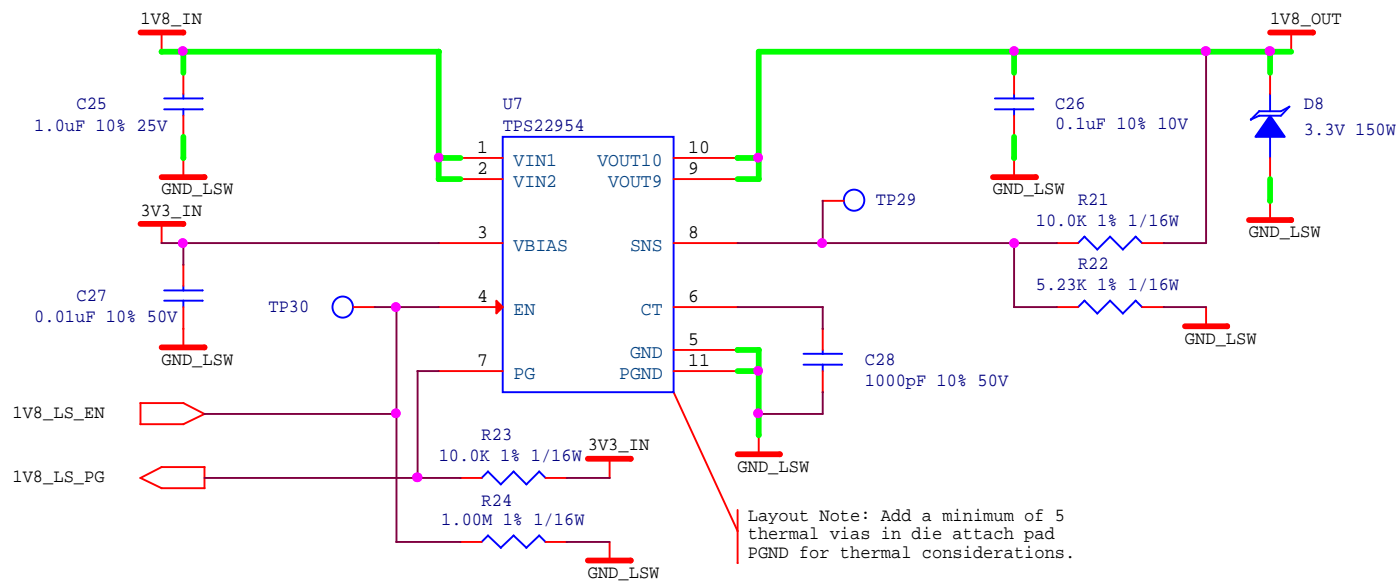
		krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857		TITLE snickerdoodle FPGA Module				
 Copyright 2015 krtkl inc. This schematic is made available under a Creative Commons Attribution-ShareAlike 4.0 International License. To view a copy of this license please visit http://creativecommons.org/licenses/by-sa/4.0/				PATH /X3				
				DESCRIPTION 1.8V Power Supply				
		NAME		DATE		SIZE B	DRAWING NO. 15081800-01	REV 2
		DRAWN BY B. Hammond		11/21/2015				
		CHECKED BY J. Weatherbee		11/23/2015				
		APPROVED BY J. Weatherbee		11/23/2015		SHEET 7 of 30		



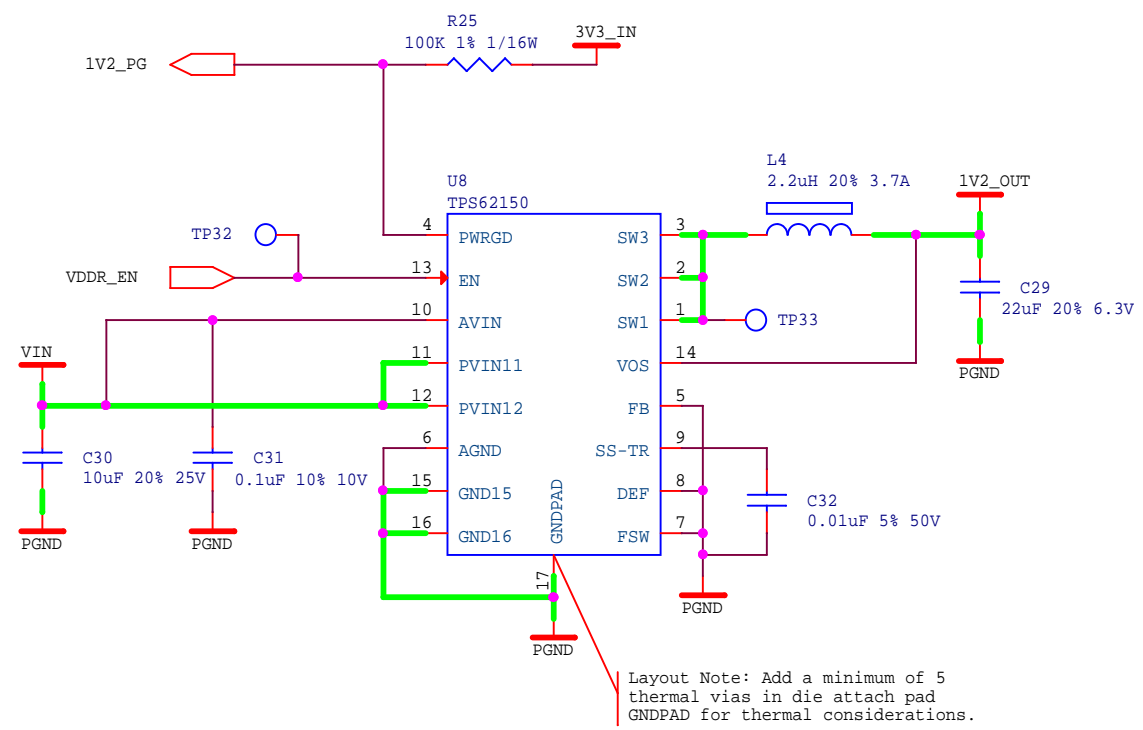
		krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857		TITLE snickerdoodle FPGA Module	
				PATH /X4	
		Copyright 2015 krtkl inc. This schematic is made available under a Creative Commons Attribution-ShareAlike 4.0 International License. To view a copy of this license please visit http://creativecommons.org/licenses/by-sa/4.0/		DESCRIPTION 3.3V Load Switch	
				SIZE B	REV 2
DRAWN BY B. Hammond		DATE 11/21/2015		DRAWING NO. 15081800-01	
CHECKED BY J. Weatherbee		DATE 11/21/2015		SHEET 8 OF 30	
APPROVED BY J. Weatherbee		DATE 11/21/2015			



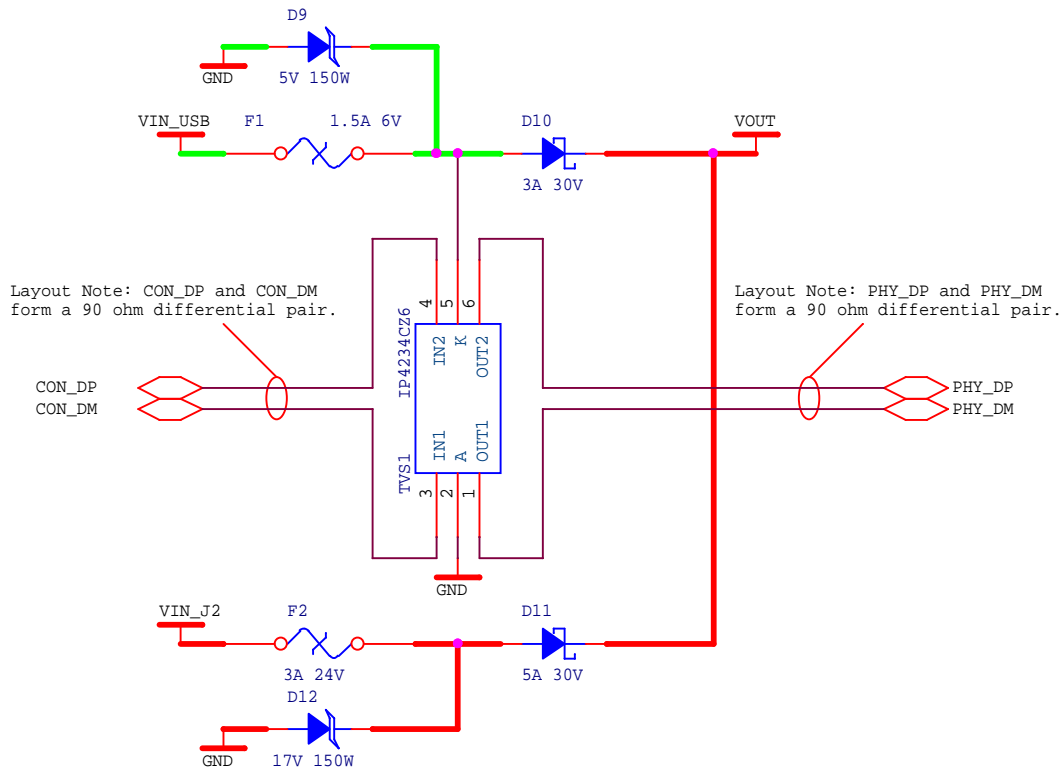
		krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857		TITLE snickerdoodle FPGA Module			
 <p>Copyright 2015 krtkl inc. This schematic is made available under a Creative Commons Attribution-ShareAlike 4.0 International License. To view a copy of this license please visit http://creativecommons.org/licenses/by-sa/4.0/</p>		NAME		DATE	PATH /X8		
		DRAWN BY B. Hammond		11/21/2015	DESCRIPTION 3.3V Load Switch		
		CHECKED BY J. Weatherbee		11/21/2015	SIZE B	DRAWING NO. 15081800-01	REV 2
		APPROVED BY J. Weatherbee		11/21/2015	SHEET 9 OF 30		



		krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857		TITLE snickerdoodle FPGA Module	
				PATH /X6	
				DESCRIPTION 1.8V Load Switch	
	DRAWN BY	B. Hammond	DATE	SIZE B	DRAWING NO. 15081800-01
	CHECKED BY	J. Weatherbee	11/23/2015		REV 2
	APPROVED BY	J. Weatherbee	11/23/2015		SHEET 11 OF 30



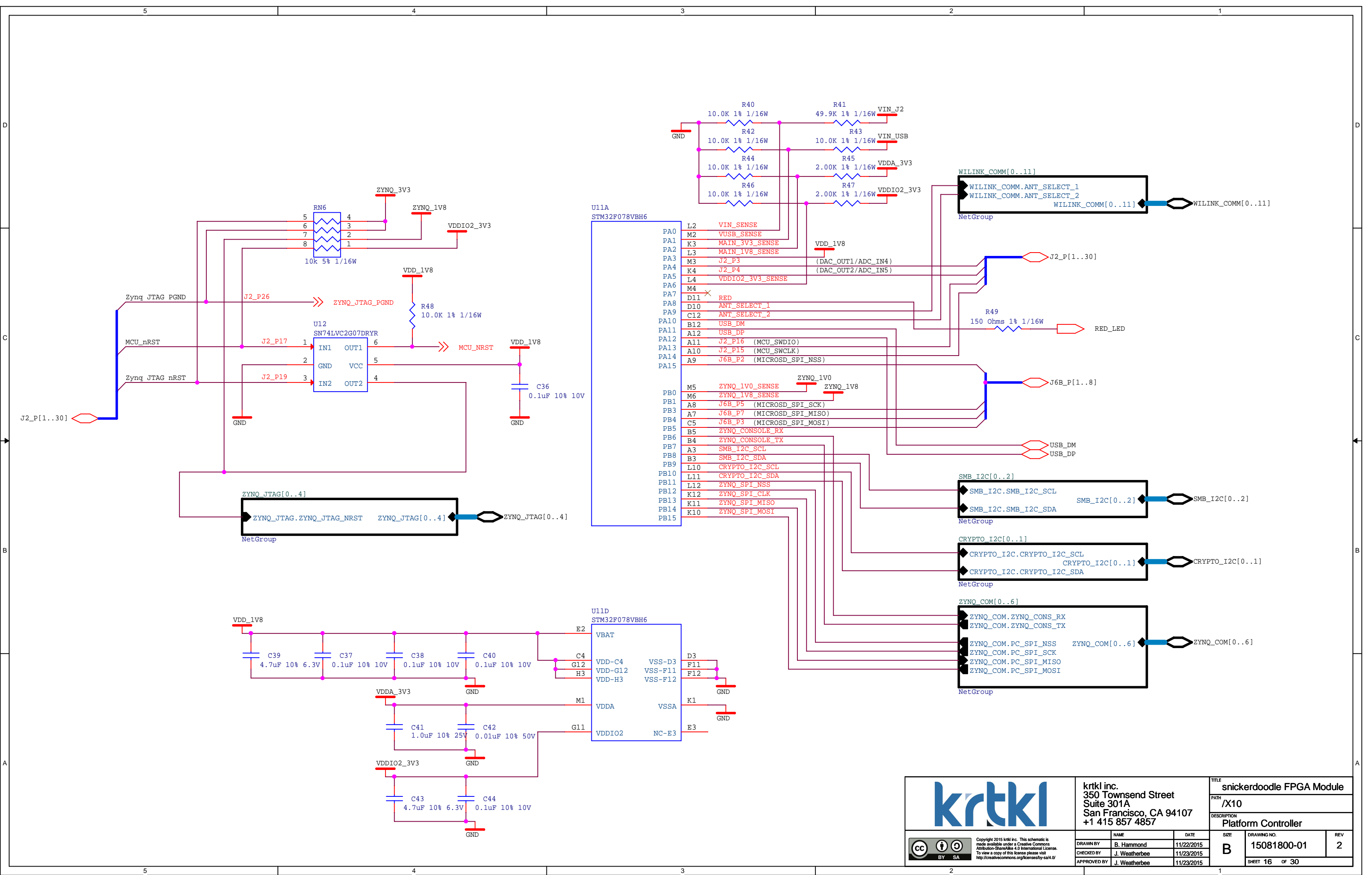
		krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857		TITLE snickerdoodle FPGA Module				
 Copyright 2015 krtkl inc. This schematic is made available under a Creative Commons Attribution-ShareAlike 4.0 International License. To view a copy of this license please visit http://creativecommons.org/licenses/by-sa/4.0/				PATH /X7				
				DESCRIPTION 1.2V Power Supply				
		NAME		DATE		SIZE B	DRAWING NO. 15081800-01	REV 2
		DRAWN BY B. Hammond		11/21/2015				
		CHECKED BY J. Weatherbee		11/23/2015				
		APPROVED BY J. Weatherbee		11/23/2015				
						SHEET 12 of 30		



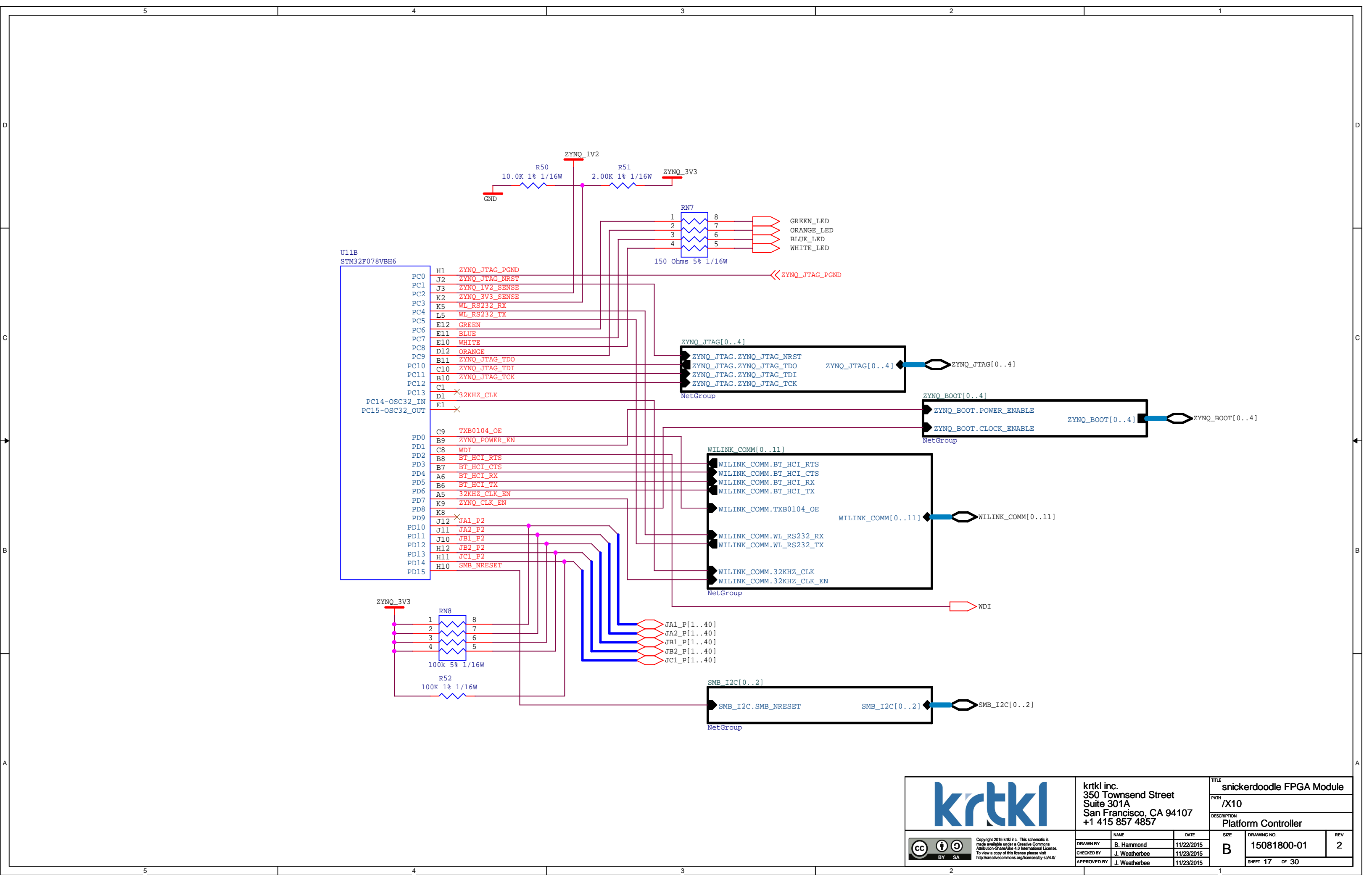
		<div>krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857</div>		TITLE snickerdoodle FPGA Module	
				PATH /X1	
				DESCRIPTION Power Entry	
				SIZE B	DRAWING NO. 15081800-01
		DRAWN BY B. Hammond	DATE 11/21/2015	REV 2	
		CHECKED BY J. Weatherbee	11/23/2015	SHEET 13 OF 30	
		APPROVED BY J. Weatherbee	11/23/2015		

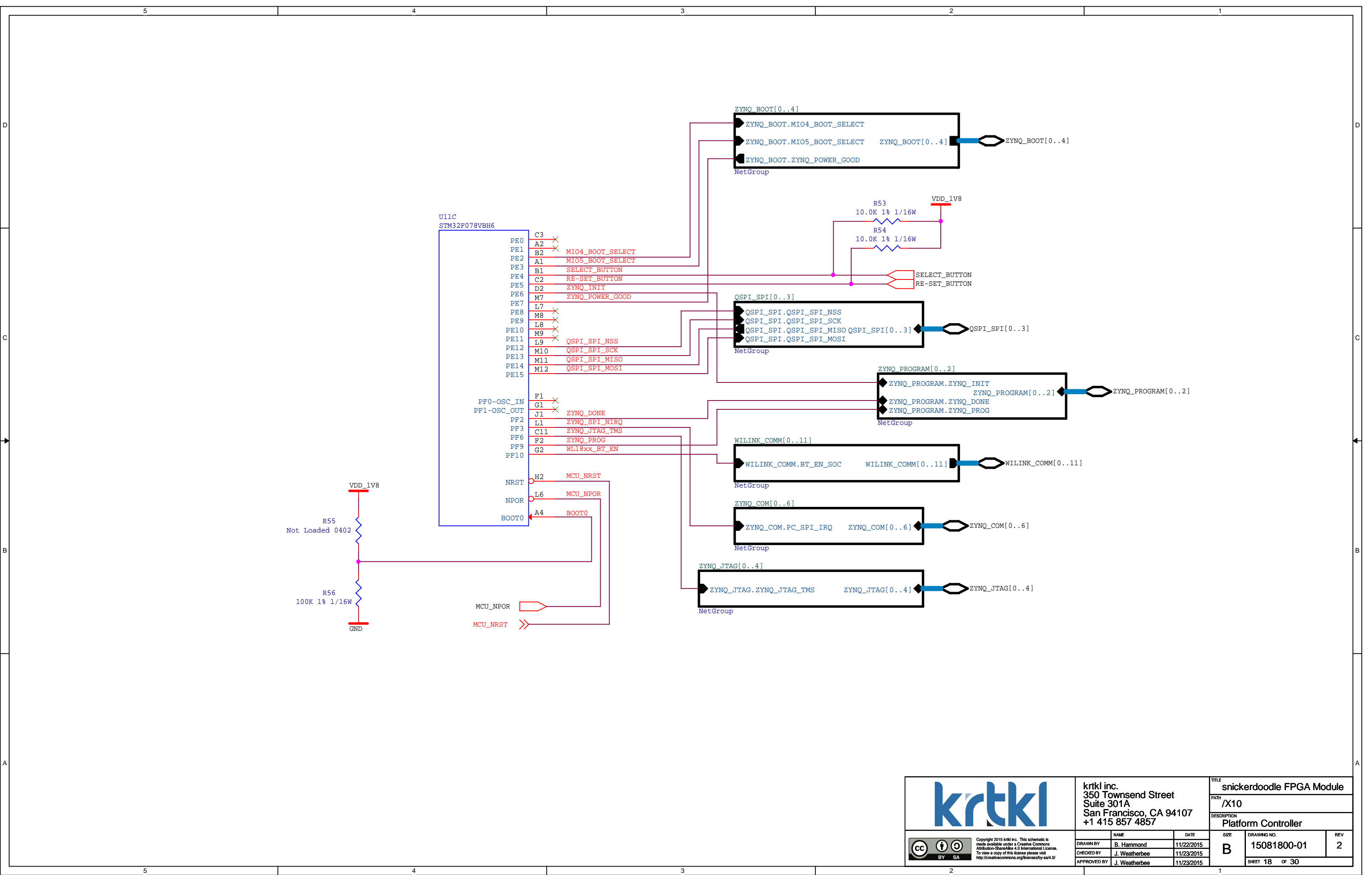


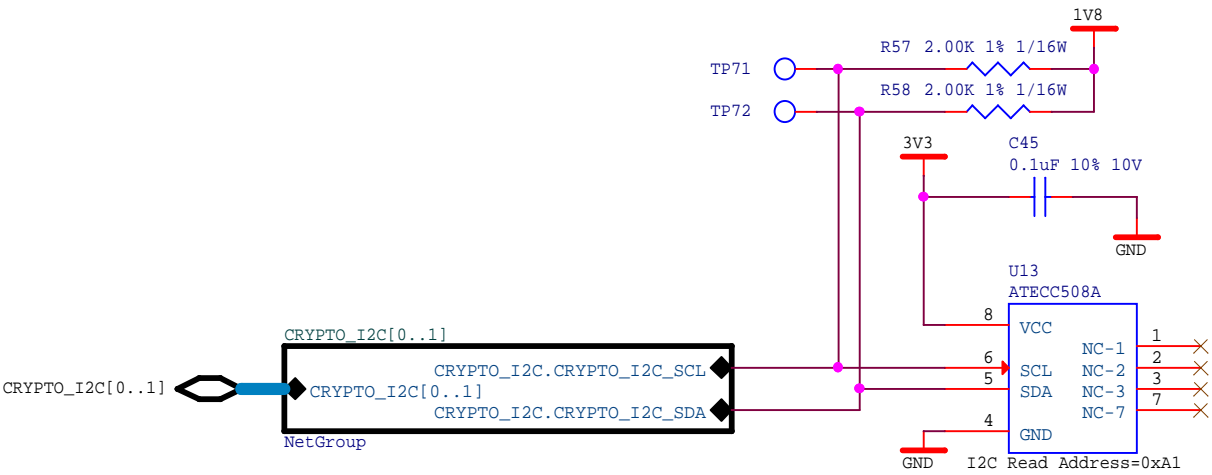




		krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857		TITLE snickerdoodle FPGA Module		
				PATH /X10		
				DESCRIPTION Platform Controller		
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		DRAWN BY B. Hammond	11/22/2015	B	15081800-01	2
		CHECKED BY J. Weatherbee	11/23/2015			
		APPROVED BY J. Weatherbee	11/23/2015			
				SHEET 16 OF 30		







		krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857		TITLE snickerdoodle FPGA Module			
				PATH /X12			
				DESCRIPTION Crypto-Authenticator			
 Copyright 2015 krtkl inc. This schematic is made available under a Creative Commons Attribution-ShareAlike 4.0 International License. To view a copy of this license please visit http://creativecommons.org/licenses/by-sa/4.0/			NAME	DATE	SIZE	DRAWING NO.	REV
		DRAWN BY	B. Hammond	11/22/2015	B	15081800-01	2
		CHECKED BY	J. Weatherbee	11/23/2015			
		APPROVED BY	J. Weatherbee	11/23/2015			
SHEET 19 OF 30							

D

D

C

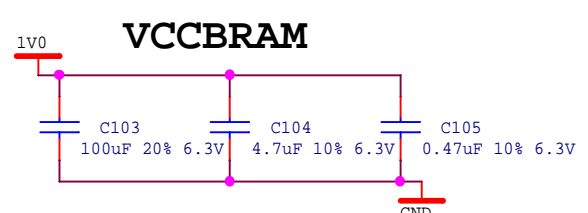
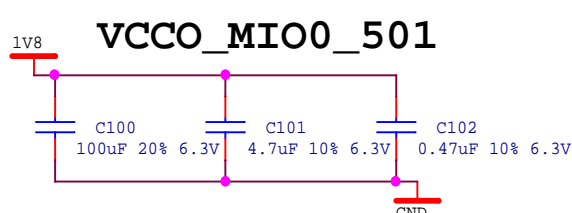
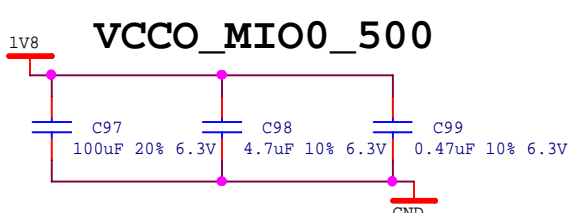
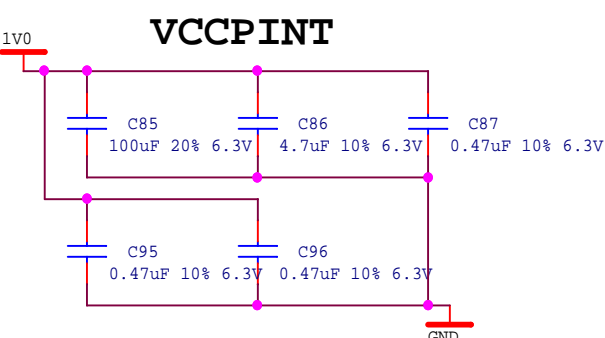
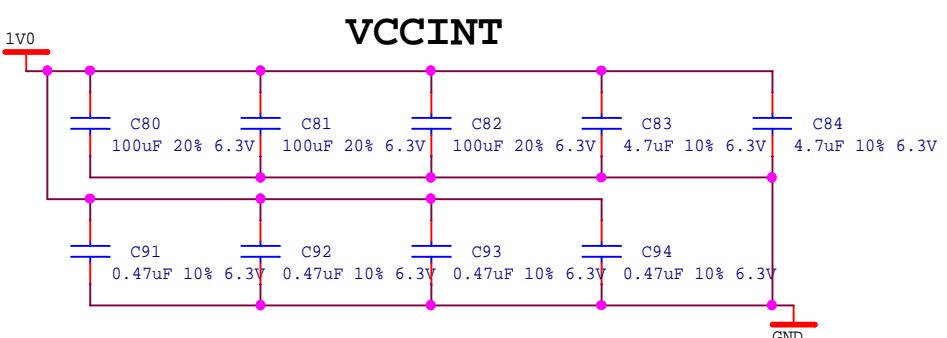
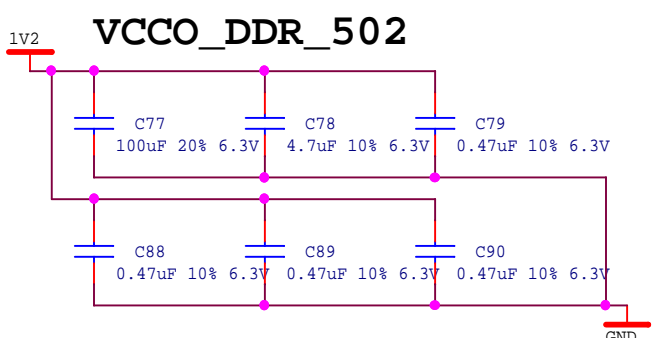
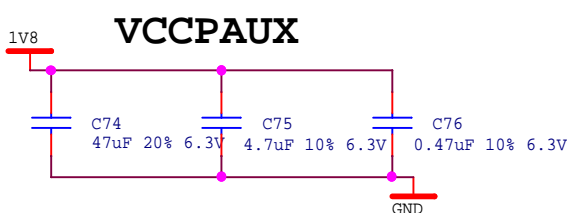
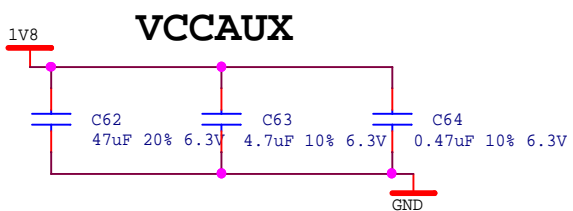
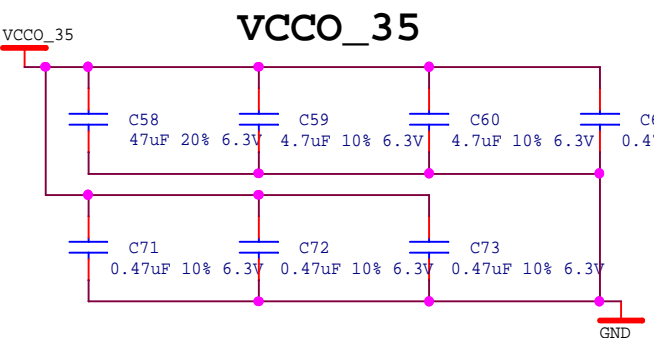
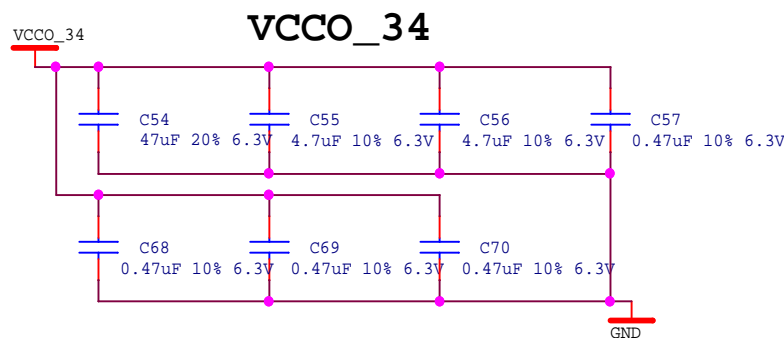
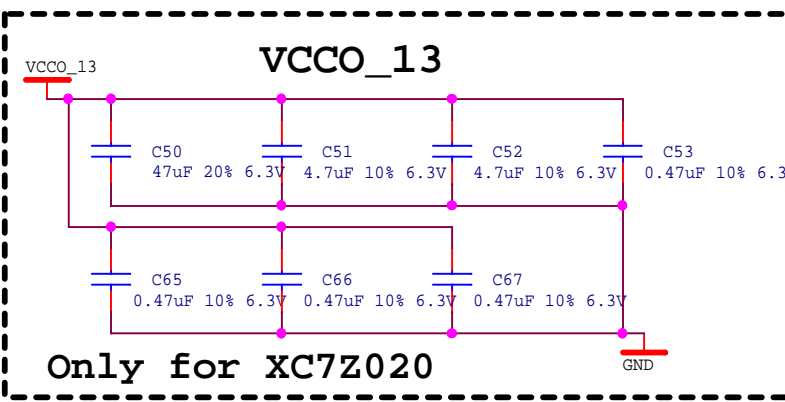
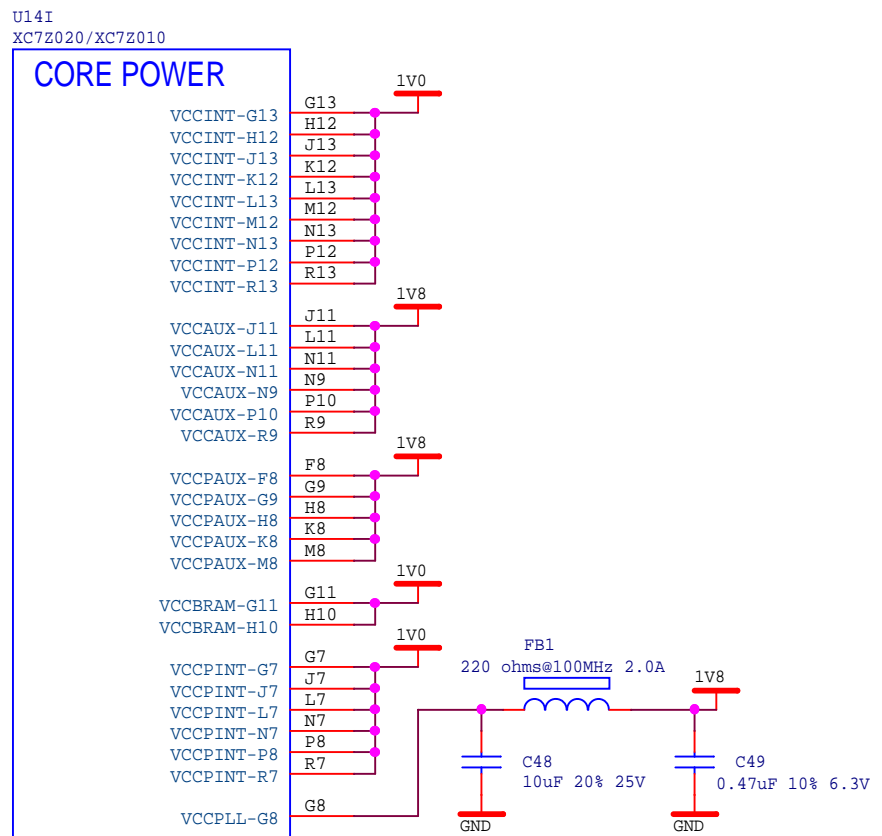
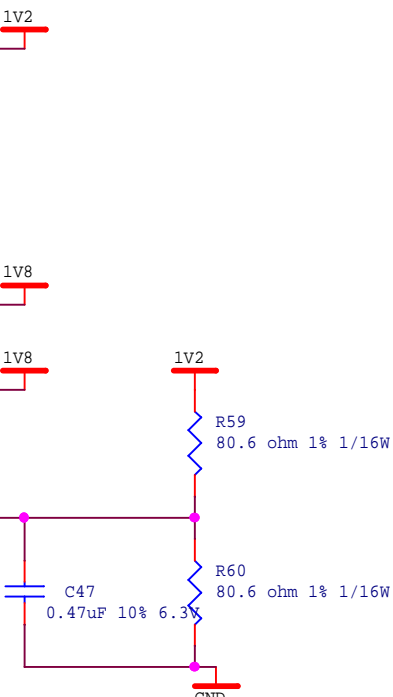
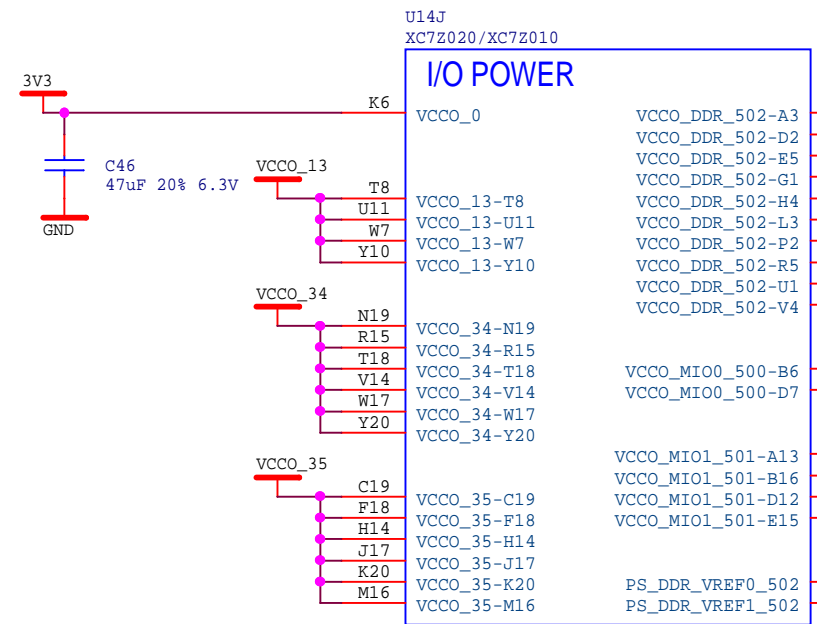
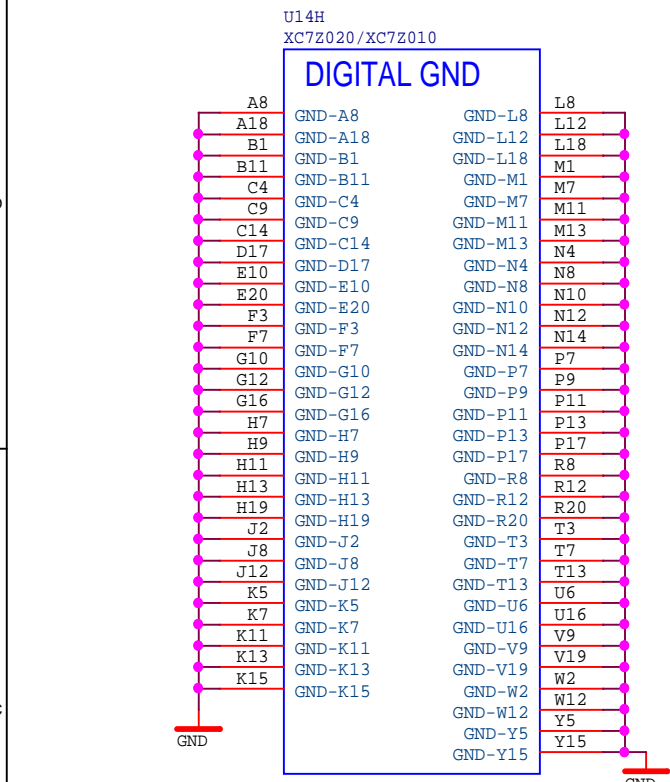
C

B

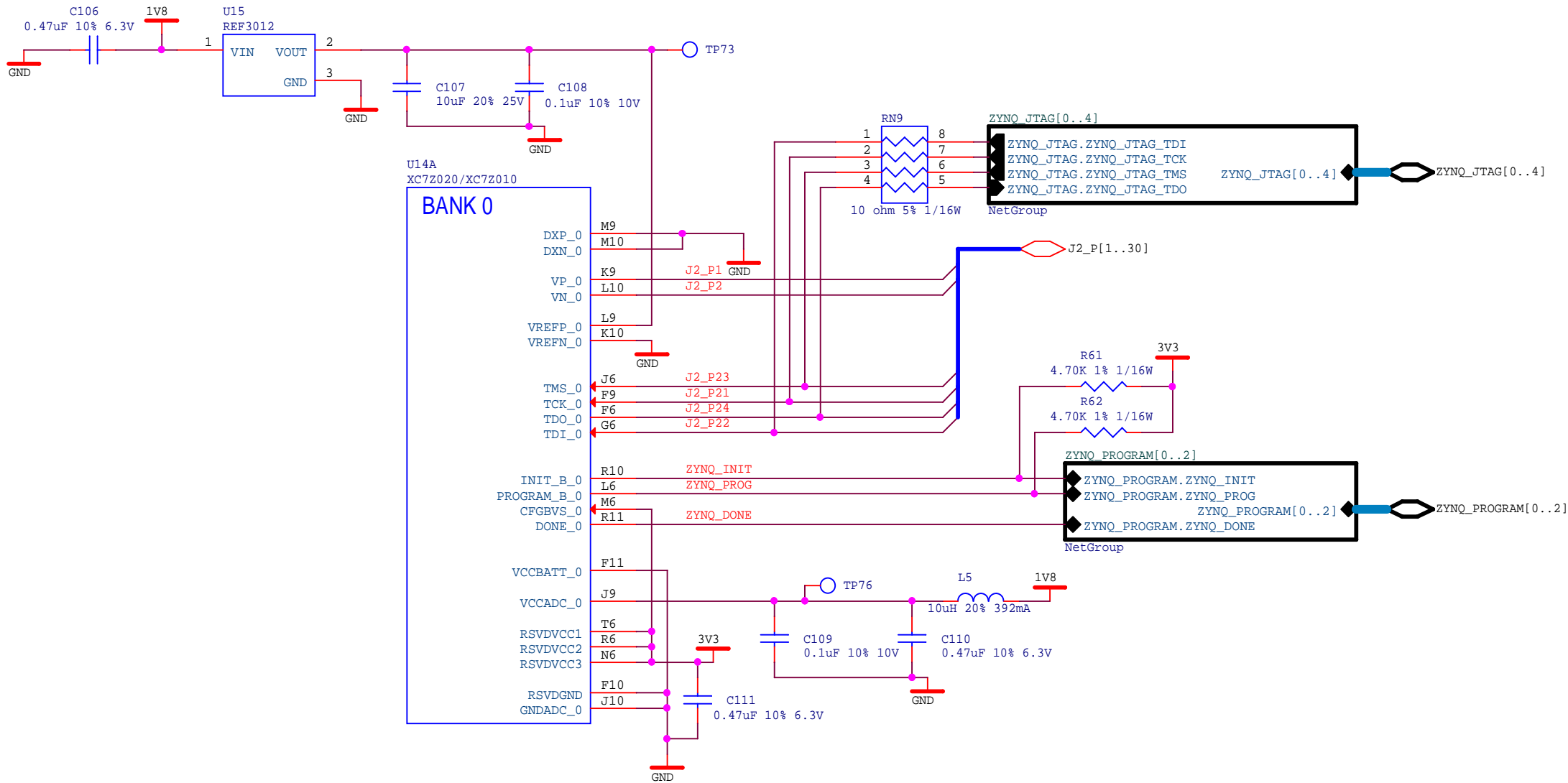
B

A

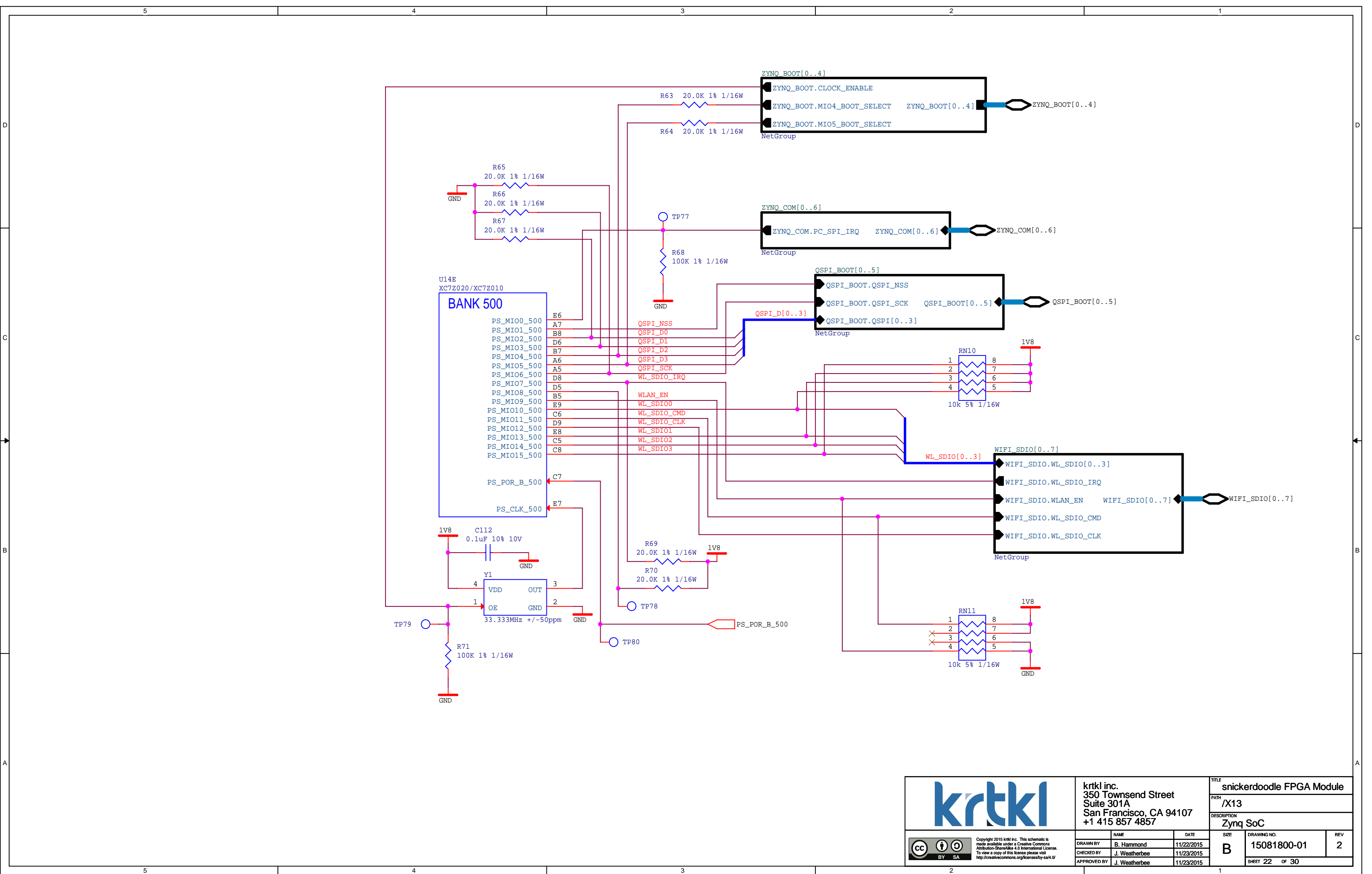
A



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	DRAWN BY	NAME	
	CHECKED BY	DATE	
	APPROVED BY	DATE	
krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857		TITLE snickerdoodle FPGA Module	
PATH /X13		DESCRIPTION Zynq SoC	
SIZE B	DRAWING NO. 15081800-01	REV 2	
SHEET 20 OF 30			



		krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857		TITLE snickerdoodle FPGA Module	
				PATH /X13	
		Copyright 2015 krtkl inc. This schematic is made available under a Creative Commons Attribution-ShareAlike 4.0 International License. To view a copy of this license please visit http://creativecommons.org/licenses/by-sa/4.0/		DESCRIPTION Zynq SoC	
				SIZE B	DRAWING NO. 15081800-01
DRAWN BY B. Hammond		DATE 11/22/2015		REV 2	
CHECKED BY J. Weatherbee		DATE 11/23/2015		SHEET 21 OF 30	
APPROVED BY J. Weatherbee		DATE 11/23/2015			



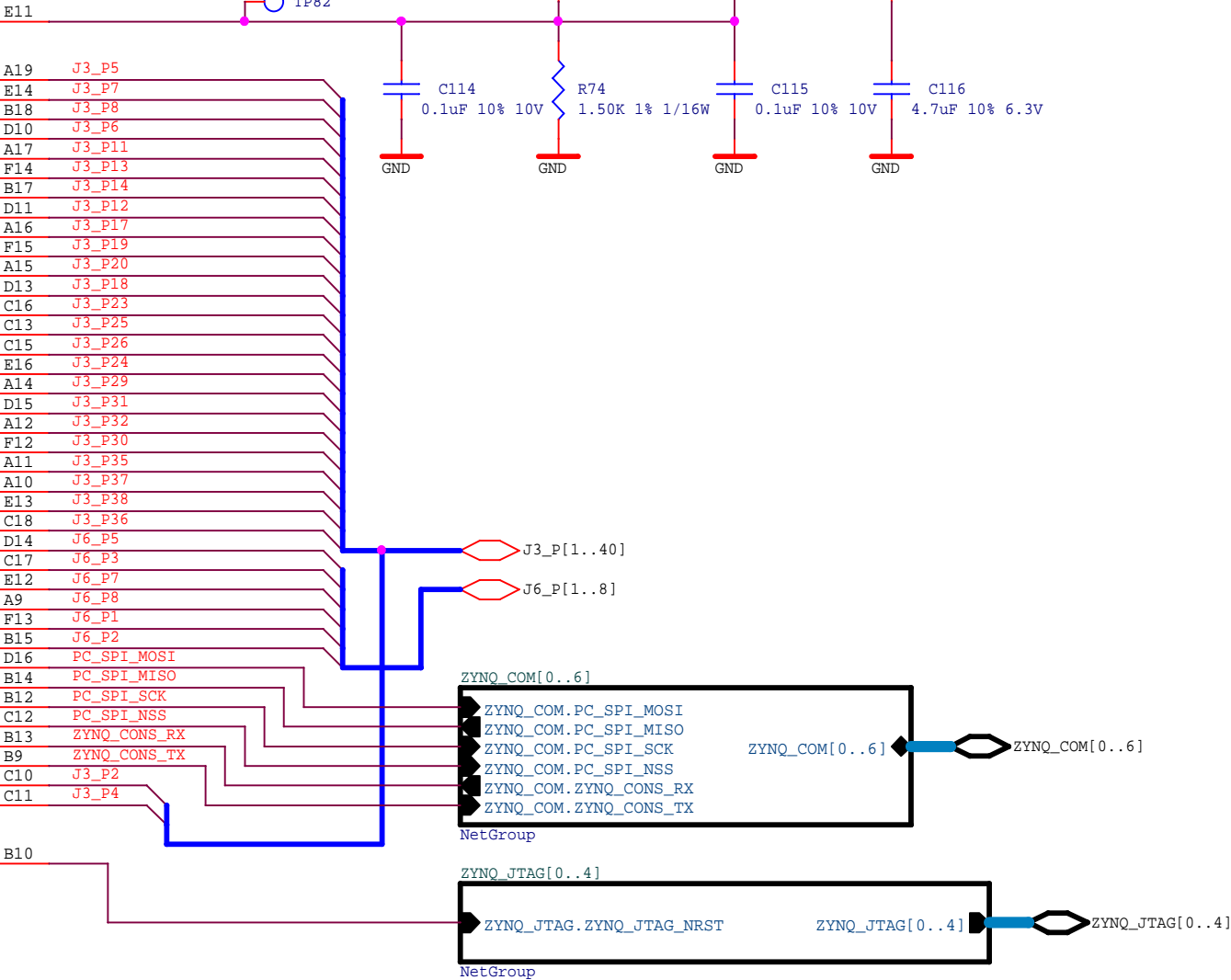
U14F
XC7Z020/XC7Z010

BANK 501

PS_MIO_VREF_501

- PS_MIO16_501
- PS_MIO17_501
- PS_MIO18_501
- PS_MIO19_501
- PS_MIO20_501
- PS_MIO21_501
- PS_MIO22_501
- PS_MIO23_501
- PS_MIO24_501
- PS_MIO25_501
- PS_MIO26_501
- PS_MIO27_501
- PS_MIO28_501
- PS_MIO29_501
- PS_MIO30_501
- PS_MIO31_501
- PS_MIO32_501
- PS_MIO33_501
- PS_MIO34_501
- PS_MIO35_501
- PS_MIO36_501
- PS_MIO37_501
- PS_MIO38_501
- PS_MIO39_501
- PS_MIO40_501
- PS_MIO41_501
- PS_MIO42_501
- PS_MIO43_501
- PS_MIO44_501
- PS_MIO45_501
- PS_MIO46_501
- PS_MIO47_501
- PS_MIO48_501
- PS_MIO49_501
- PS_MIO50_501
- PS_MIO51_501
- PS_MIO52_501
- PS_MIO53_501

PS_SRST_B_501



U14G
XC7Z020/XC7Z010

BANK 502

PS_DDR_DQ0_502
PS_DDR_DQ1_502
PS_DDR_DQ2_502
PS_DDR_DQ3_502
PS_DDR_DQ4_502
PS_DDR_DQ5_502
PS_DDR_DQ6_502
PS_DDR_DQ7_502
PS_DDR_DQ8_502
PS_DDR_DQ9_502
PS_DDR_DQ10_502
PS_DDR_DQ11_502
PS_DDR_DQ12_502
PS_DDR_DQ13_502
PS_DDR_DQ14_502
PS_DDR_DQ15_502
PS_DDR_DQ16_502
PS_DDR_DQ17_502
PS_DDR_DQ18_502
PS_DDR_DQ19_502
PS_DDR_DQ20_502
PS_DDR_DQ21_502
PS_DDR_DQ22_502
PS_DDR_DQ23_502
PS_DDR_DQ24_502
PS_DDR_DQ25_502
PS_DDR_DQ26_502
PS_DDR_DQ27_502
PS_DDR_DQ28_502
PS_DDR_DQ29_502
PS_DDR_DQ30_502
PS_DDR_DQ31_502

PS_DDR_A0_502
PS_DDR_A1_502
PS_DDR_A2_502
PS_DDR_A3_502
PS_DDR_A4_502
PS_DDR_A5_502
PS_DDR_A6_502
PS_DDR_A7_502
PS_DDR_A8_502
PS_DDR_A9_502
PS_DDR_A10_502
PS_DDR_A11_502
PS_DDR_A12_502
PS_DDR_A13_502
PS_DDR_A14_502

PS_DDR_DQS_P0_502
PS_DDR_DQS_N0_502
PS_DDR_DQS_P1_502
PS_DDR_DQS_N1_502
PS_DDR_DQS_P2_502
PS_DDR_DQS_N2_502
PS_DDR_DQS_P3_502
PS_DDR_DQS_N3_502

PS_DDR_CKP_502
PS_DDR_CKN_502

PS_DDR_BA0_502
PS_DDR_BA1_502
PS_DDR_BA2_502

PS_DDR_DM0_502
PS_DDR_DM1_502
PS_DDR_DM2_502
PS_DDR_DM3_502

PS_DDR_CS_B_502
PS_DDR_WE_B_502
PS_DDR_CAS_B_502
PS_DDR_RAS_B_502
PS_DDR_CKE_502
PS_DDR_ODT_502

PS_DDR_DRST_B_502

PS_DDR_VRP_502
PS_DDR_VRN_502

C3
B3
A2
A4
D3
D1
C1
E1
E2
E3
G3
H3
J3
H2
H1
J1
P1
P3
R3
R1
T4
U4
U2
U3
V1
Y3
W1
Y4
Y2
W3
V2
V3

N2
K2
M3
K3
M4
L1
L4
K4
K1
J4
F5
G4
E4
D4
F4

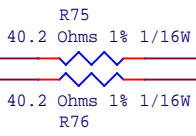
C2
B2
G2
F2
R2
T2
W5
W4

L2
M2
L5
R4
J5

A1
F1
T1
Y1

N1
M5
P5
P4
N3
N5

B4
H5
G5

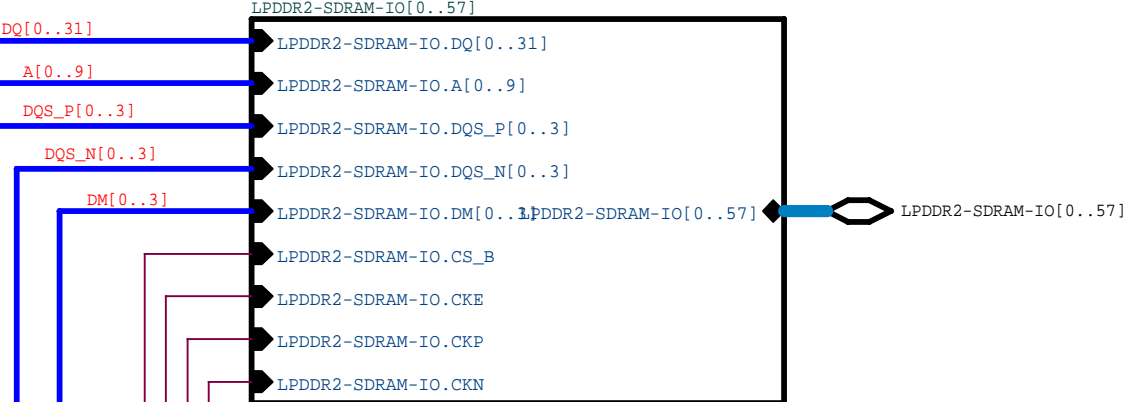


Match all signal trace lengths for DQ groups with a max deviation of ±50 mils and route on the same layer.

Route address and command signals on a different layer than the data and data mask signals.

Route clock on inner layers with outer-layer run lengths held to under 500 mils and maintain a 10-mil spacing from other nets. Length match clock traces within ±25 mils, with CKP and CKN traces matched within ±10 mils. Do not route CKP/CKN pair and CKE close to address signals.

Route address and command signals on a different layer than the data and data mask signals.





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DRAWN BY	B. Hammond	DATE	11/22/2015
CHECKED BY	J. Weatherbee	DATE	11/23/2015
APPROVED BY	J. Weatherbee	DATE	11/23/2015

snickerdoodle FPGA Module

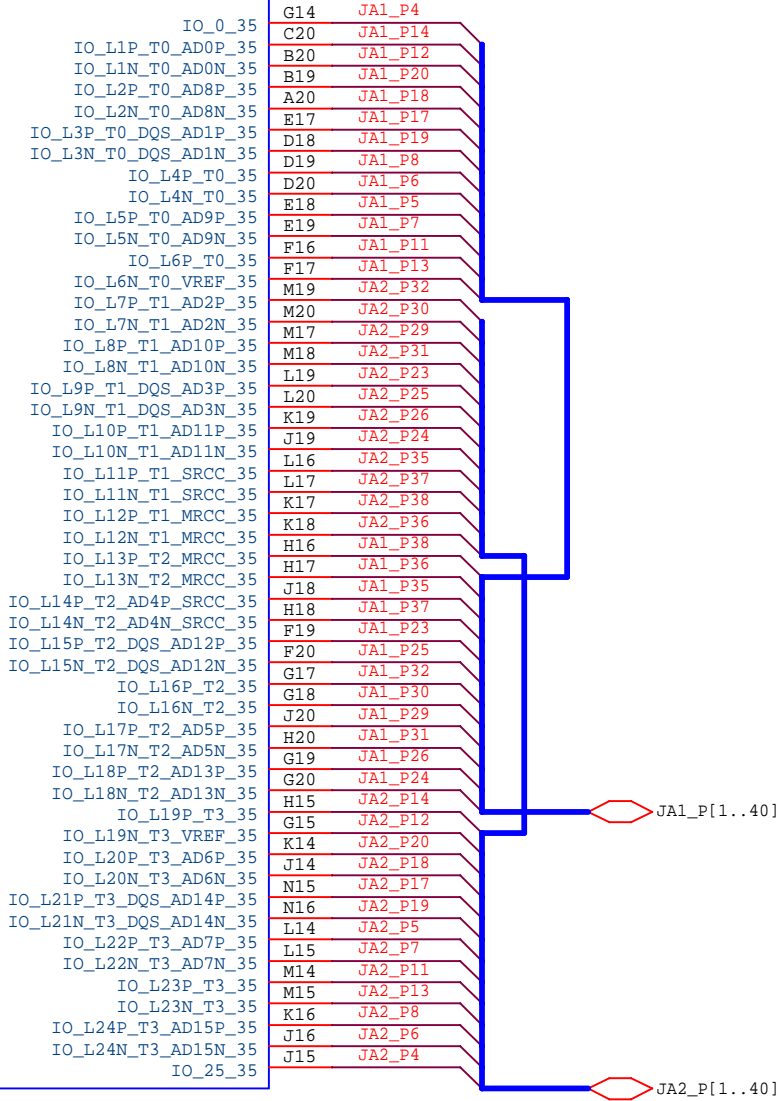
/X13

Zynq SoC

SIZE	DRAWING NO.	REV
B	15081800-01	2
SHEET 24 OF 30		

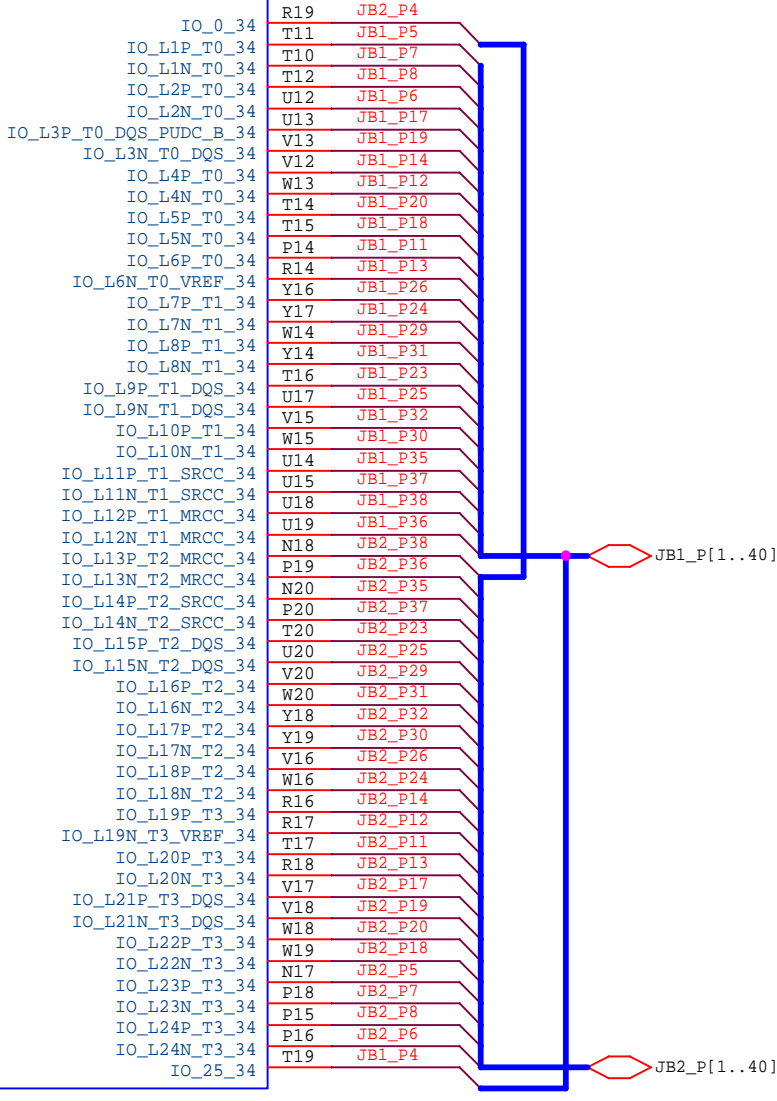
U14D
XC7Z020/XC7Z010

BANK 35



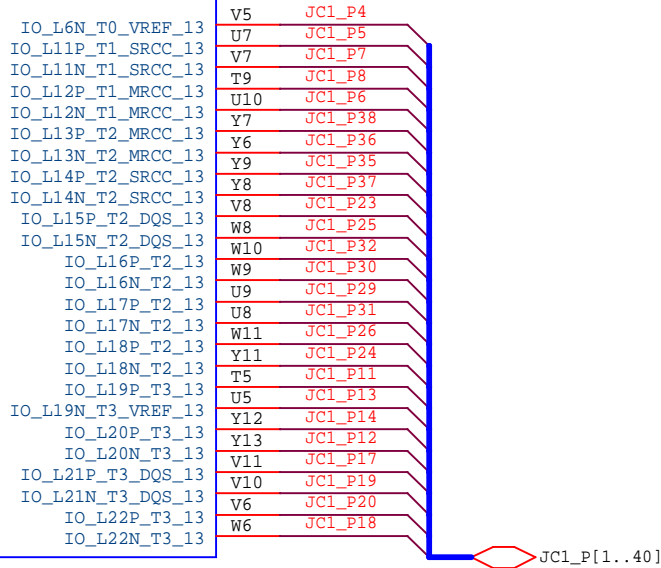
U14C
XC7Z020/XC7Z010

BANK 34



U14B
XC7Z020/XC7Z010

BANK 13



Only for XC7Z020

		krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857		TITLE snickerdoodle FPGA Module	
				PATH /X13	
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				SIZE B	DRAWING NO. 15081800-01
DRAWN BY B. Hammond		NAME B. Hammond		DATE 11/22/2015	
CHECKED BY J. Weatherbee		NAME J. Weatherbee		DATE 11/23/2015	
APPROVED BY J. Weatherbee		NAME J. Weatherbee		DATE 11/23/2015	
				SHEET 25	OF 30
				REV 2	

