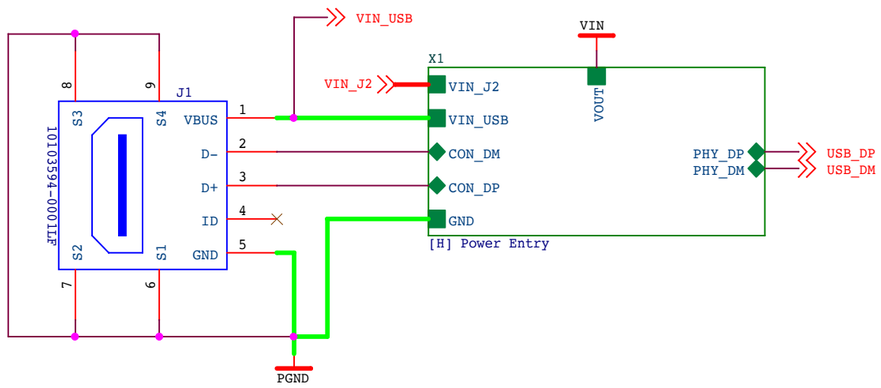
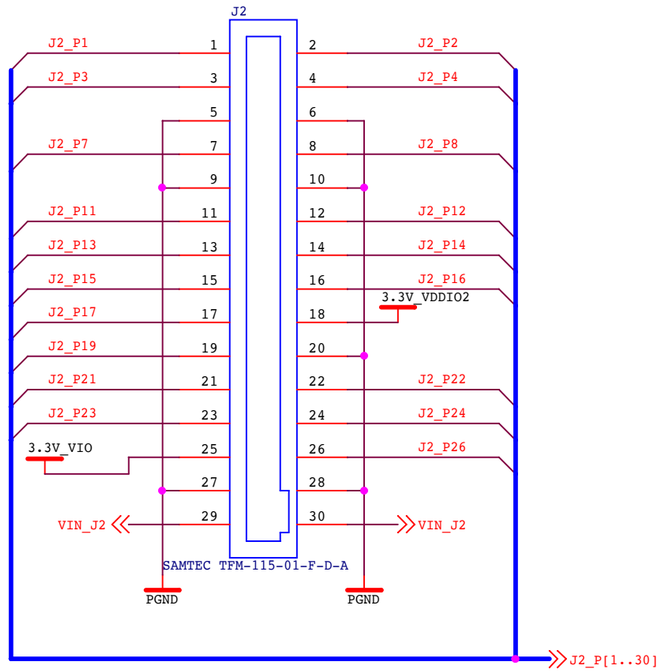
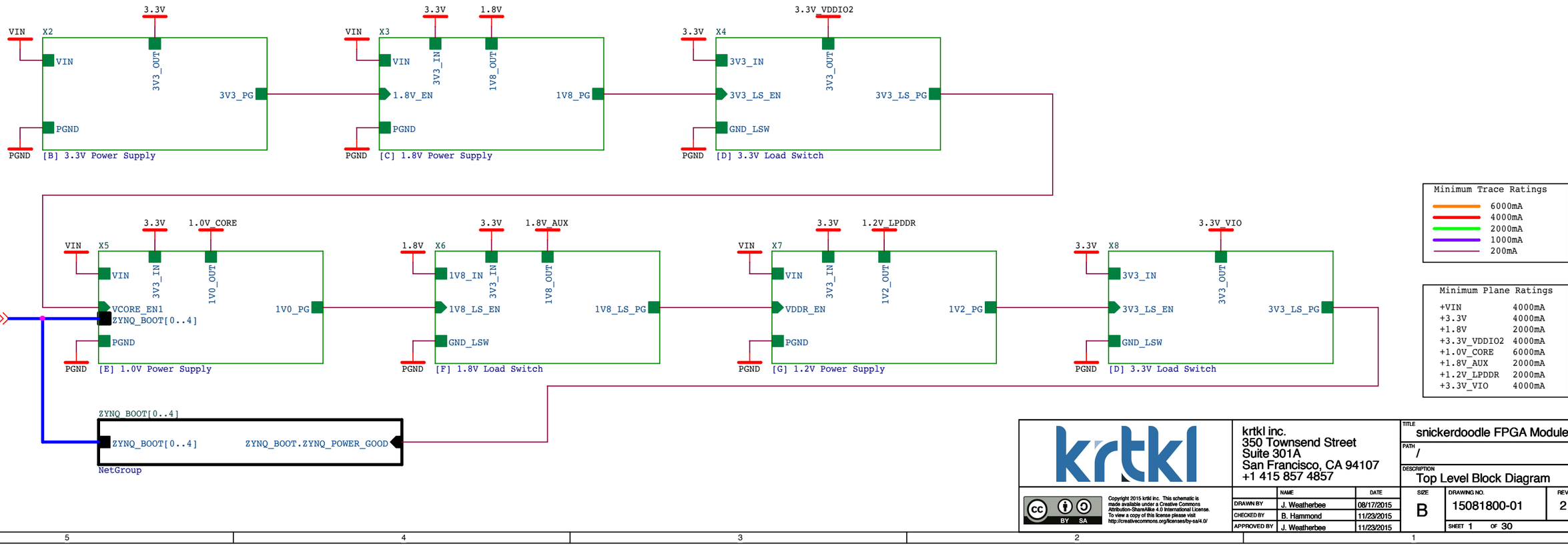
Rev.	Description	CO Number	Date	Approved By	Checked By
2	Alpha Prototype	00001	09/01/2015	JJW	BEH

Power/JTAG/SWD/BT Audio/I2C/DAC/ADC







Minimum Trace Ratings	
	6000mA
	4000mA
	2000mA
	1000mA
	200mA

Minimum Plane Ratings	
+VIN	4000mA
+3.3V	4000mA
+1.8V	2000mA
+3.3V_VDDIO2	4000mA
+1.0V_CORE	6000mA
+1.8V_AUX	2000mA
+1.2V_LPDDR	2000mA
+3.3V_VIO	4000mA

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	NAME	DATE
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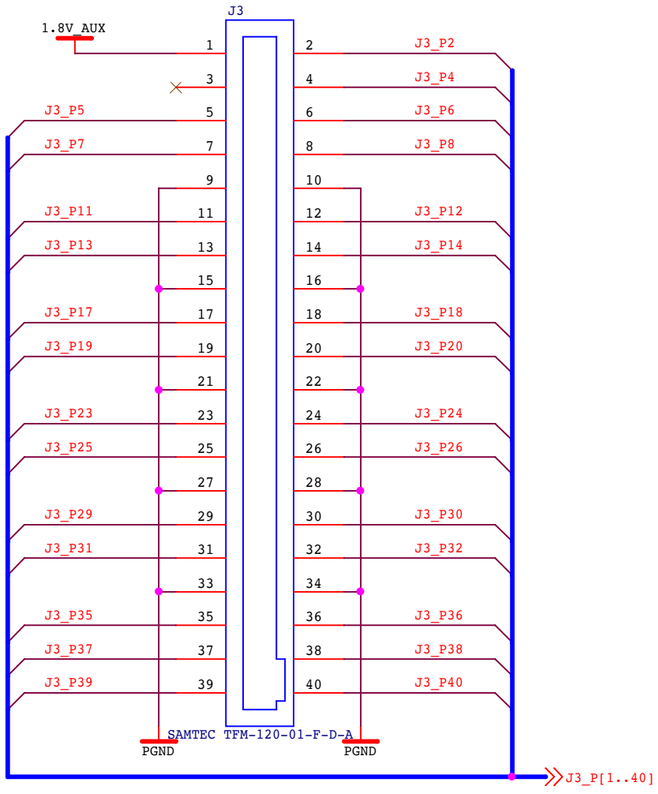
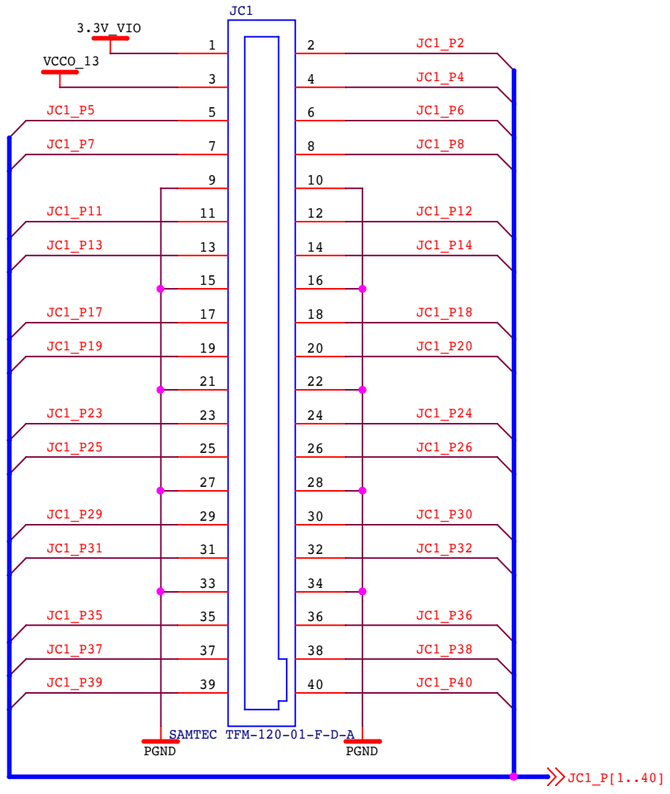
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 1 OF 30

CPU GPIO/USB ULPI/GigE RGMII/SPI/I2C/UART/CAN



FPGA I/O



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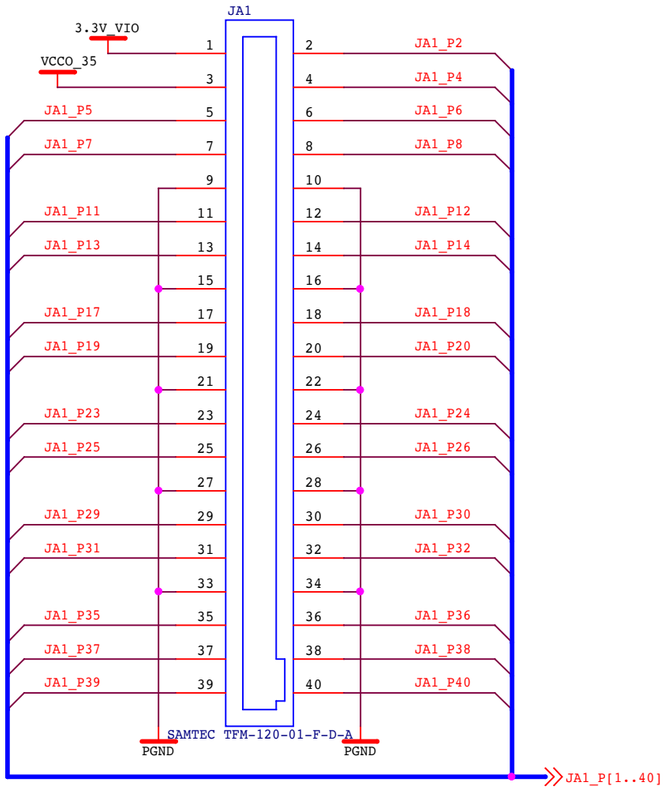

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DRAWN BY	J. Weatherbee	11/21/2015
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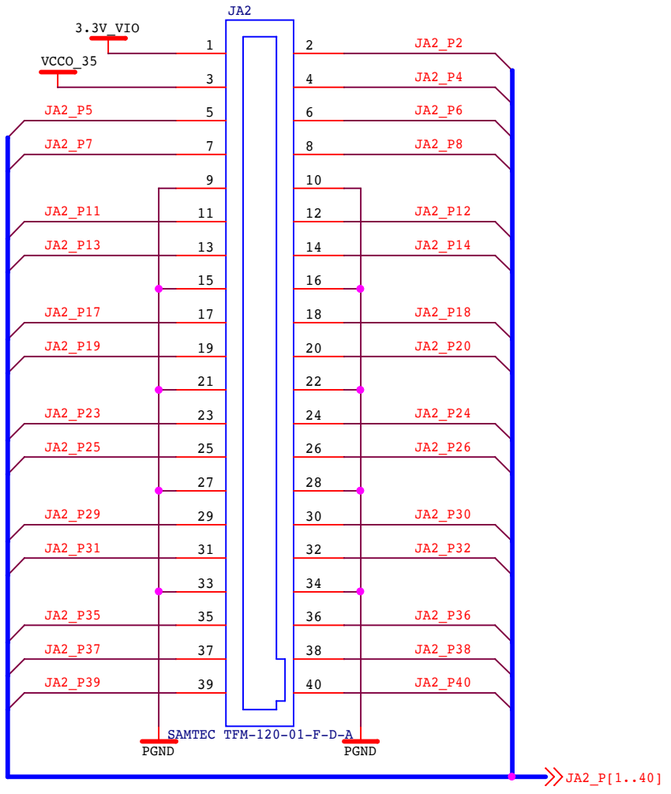
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 2 OF 30

FPGA I/O



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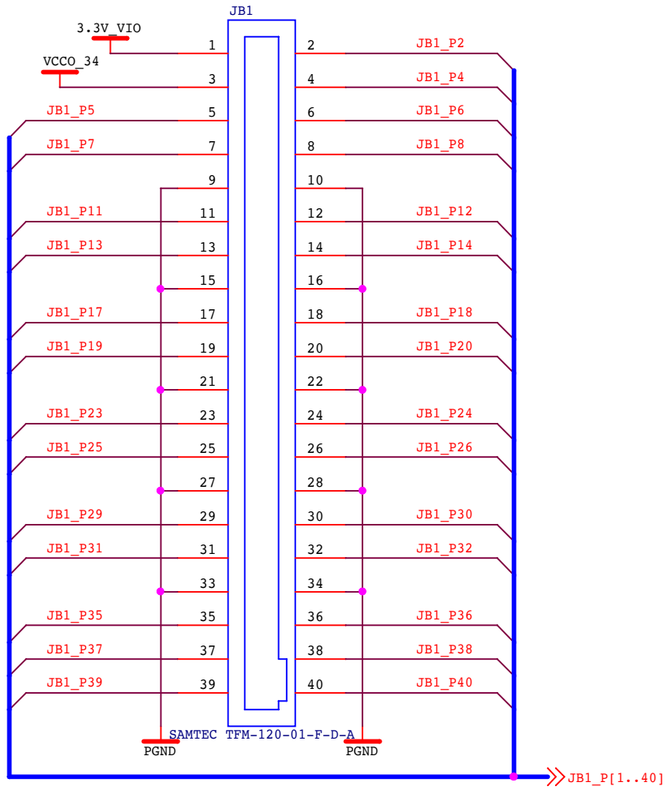
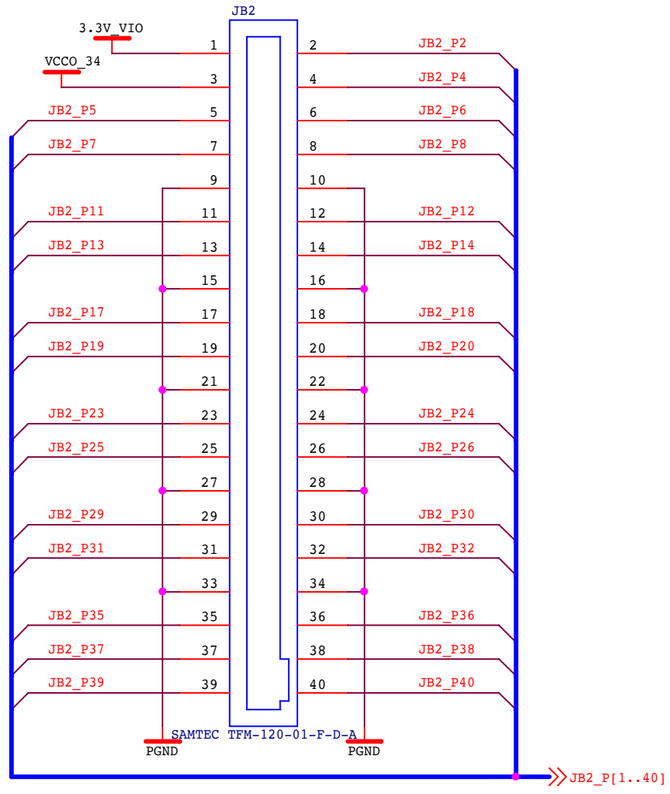


FPGA I/O



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	NAME	DATE
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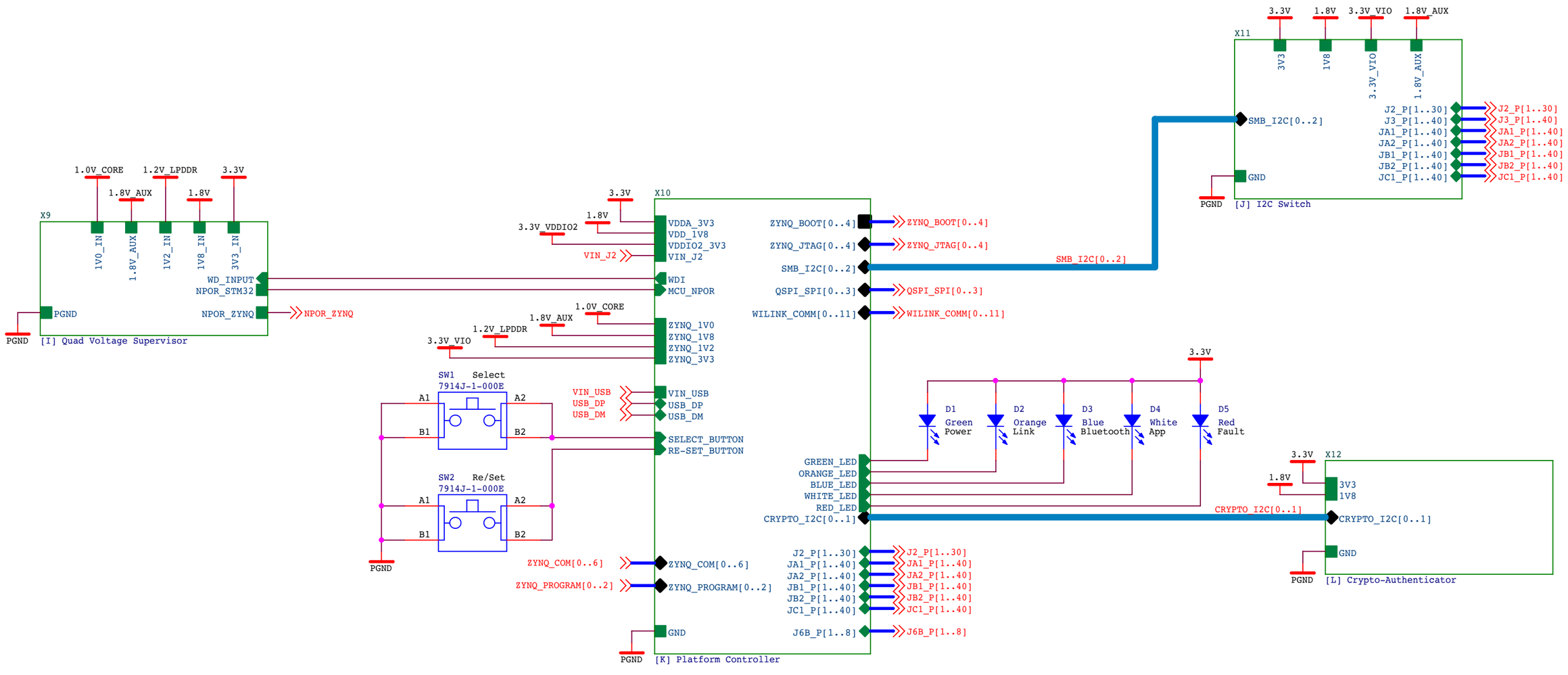
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 3 OF 30



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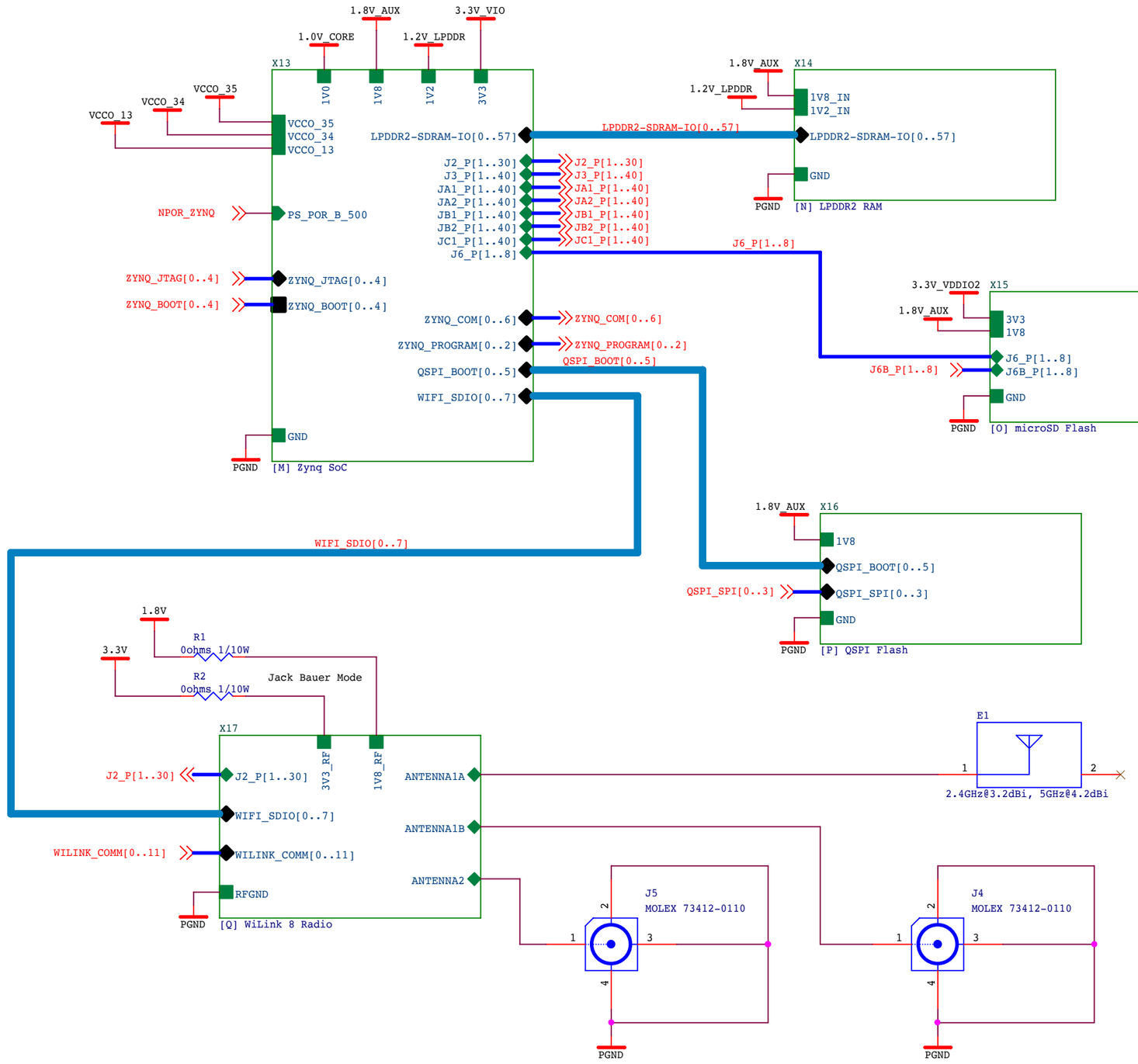
	NAME	DATE
DRAWN BY	J. Weatherbee	11/22/2015
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 4 OF 30



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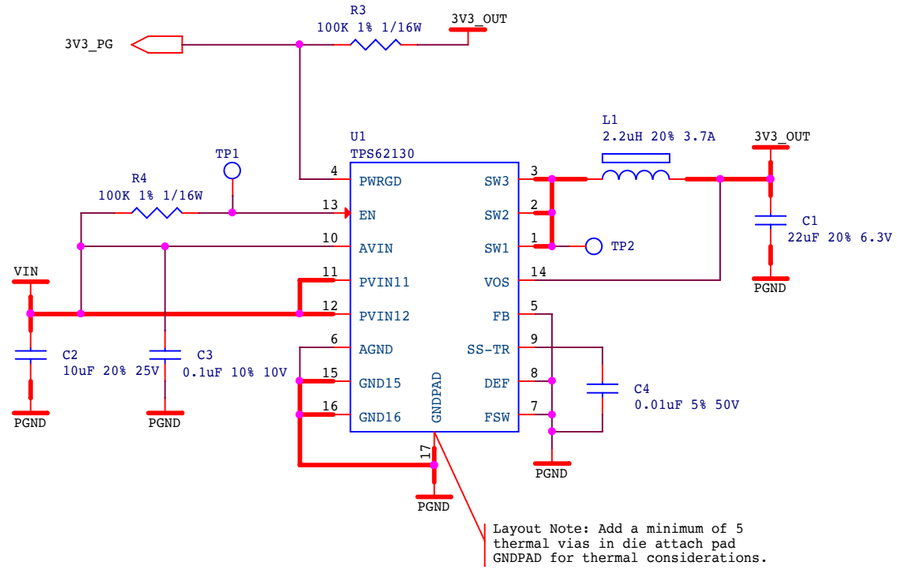
	NAME	DATE
DRAWN BY	J. Weatherbee	11/22/2015
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 5 OF 30



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DRAWN BY	B. Hammond	11/21/2015
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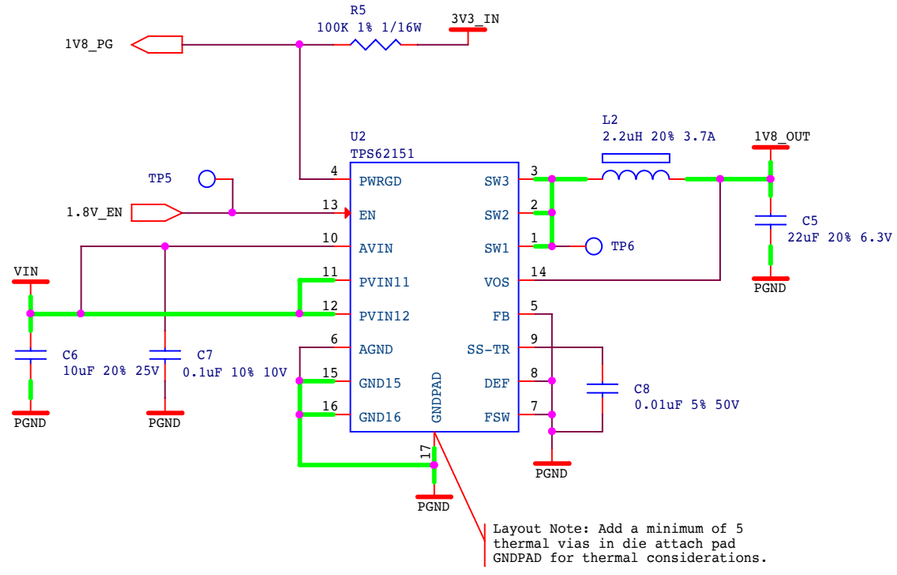
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X2
DESCRIPTION: 3.3V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 6 OF 30



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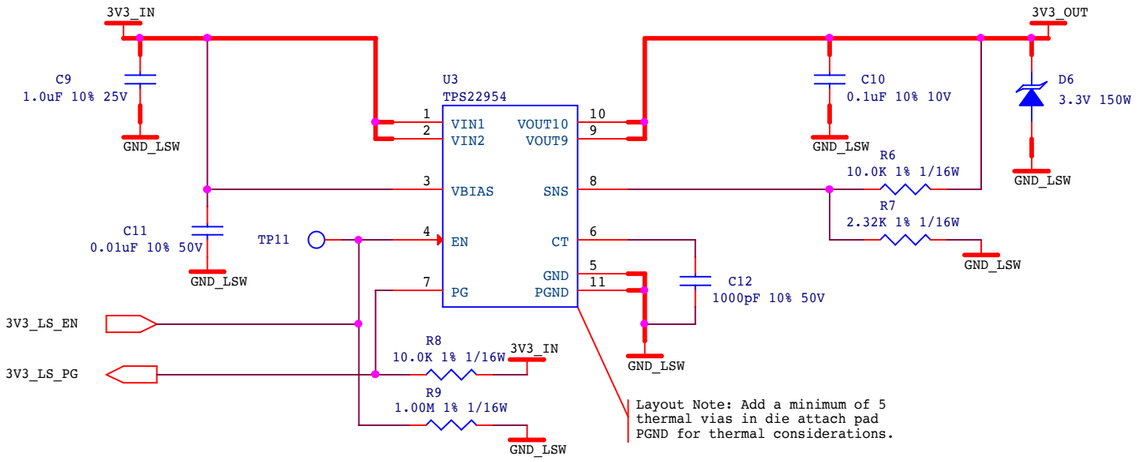
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X3
DESCRIPTION: 1.8V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 7 OF 30



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DRAWN BY	B. Hammond	11/21/2015
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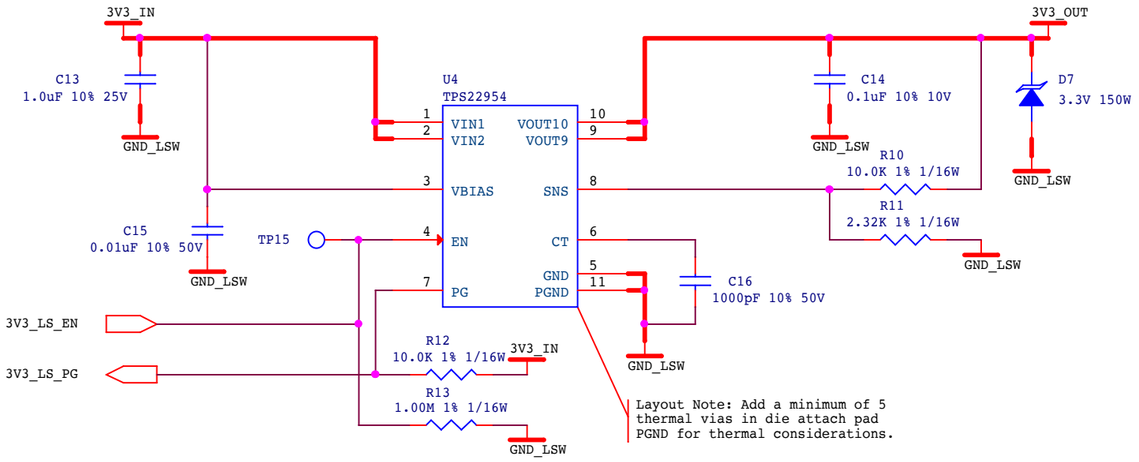
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X4
DESCRIPTION: 3.3V Load Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 8 OF 30



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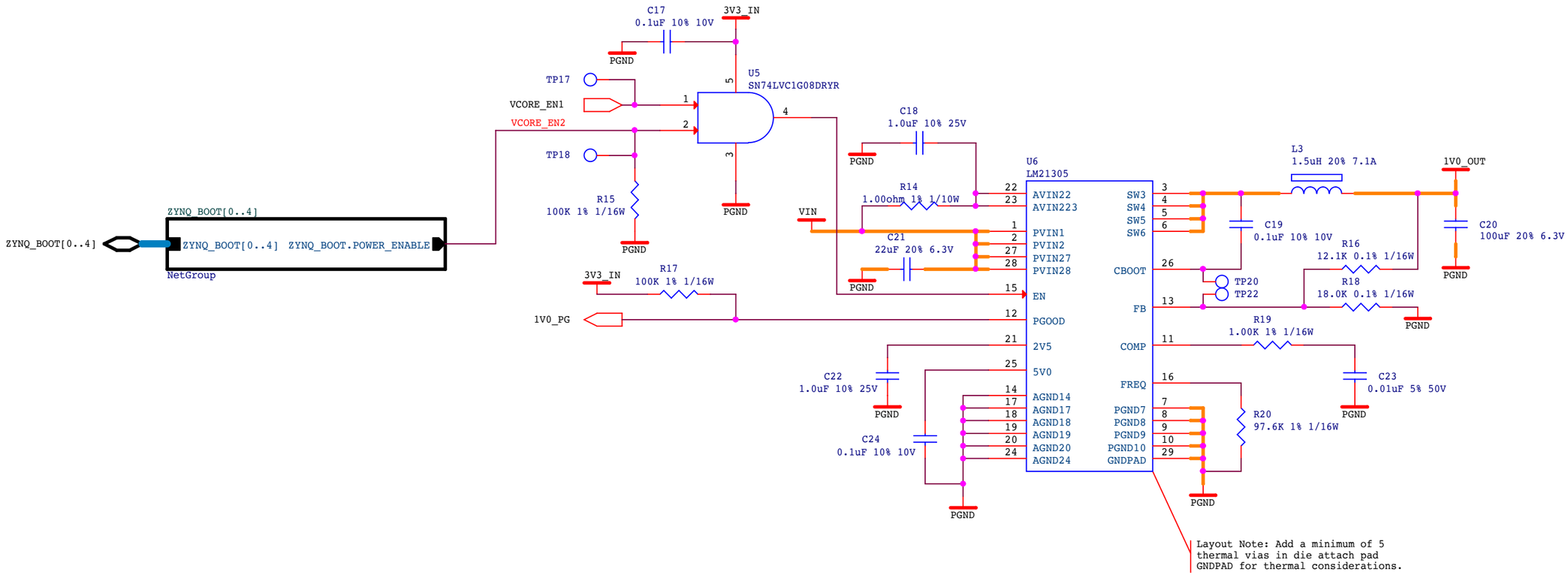
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X8
DESCRIPTION: 3.3V Load Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 9 OF 30



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DRAWN BY	B. Hammond	11/21/2015
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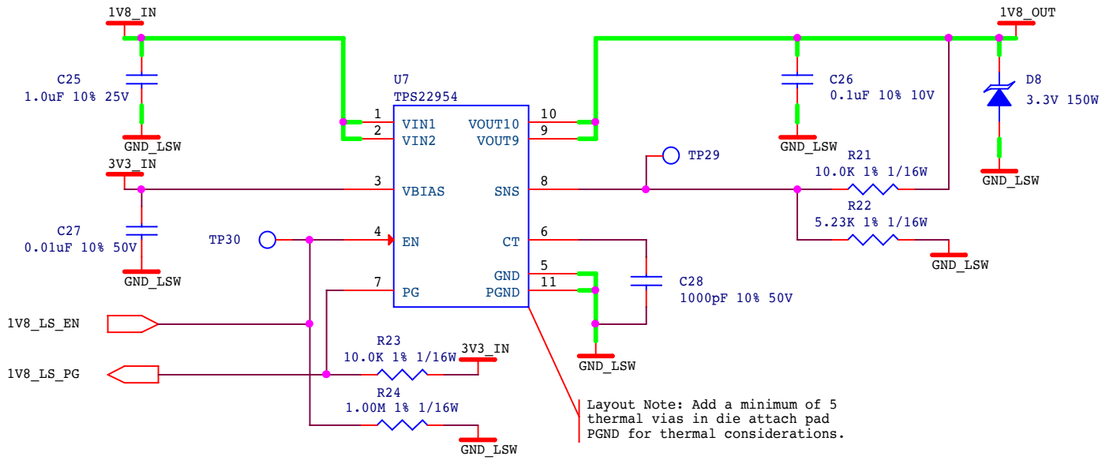
TITLE: snickerdoodle FPGA Module
PATH: /X5
DESCRIPTION: 1.0V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 10 OF 30



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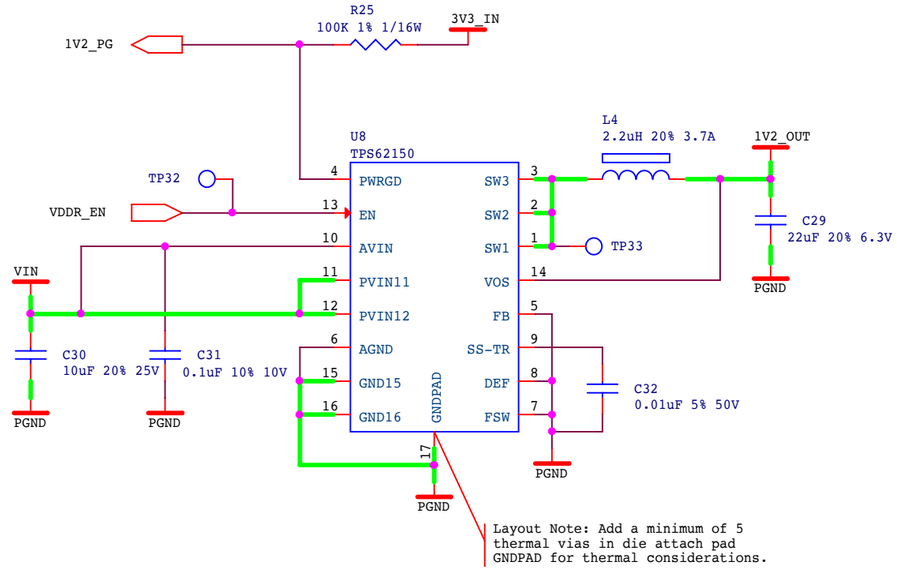
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X6
DESCRIPTION: 1.8V Load Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 11 OF 30



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DRAWN BY	B. Hammond	11/21/2015
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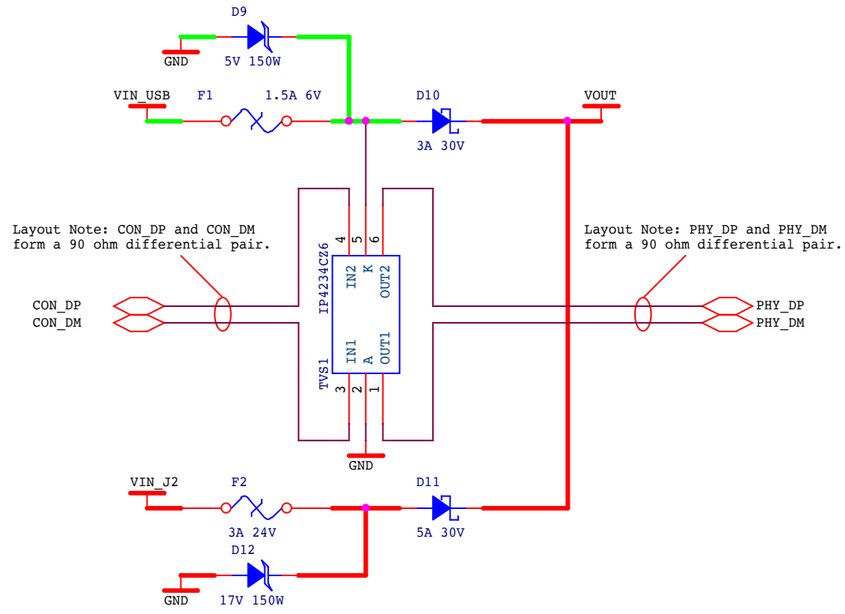
TITLE: snickerdoodle FPGA Module
PATH: /X7
DESCRIPTION: 1.2V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 12 OF 30



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DRAWN BY	B. Hammond	11/21/2015
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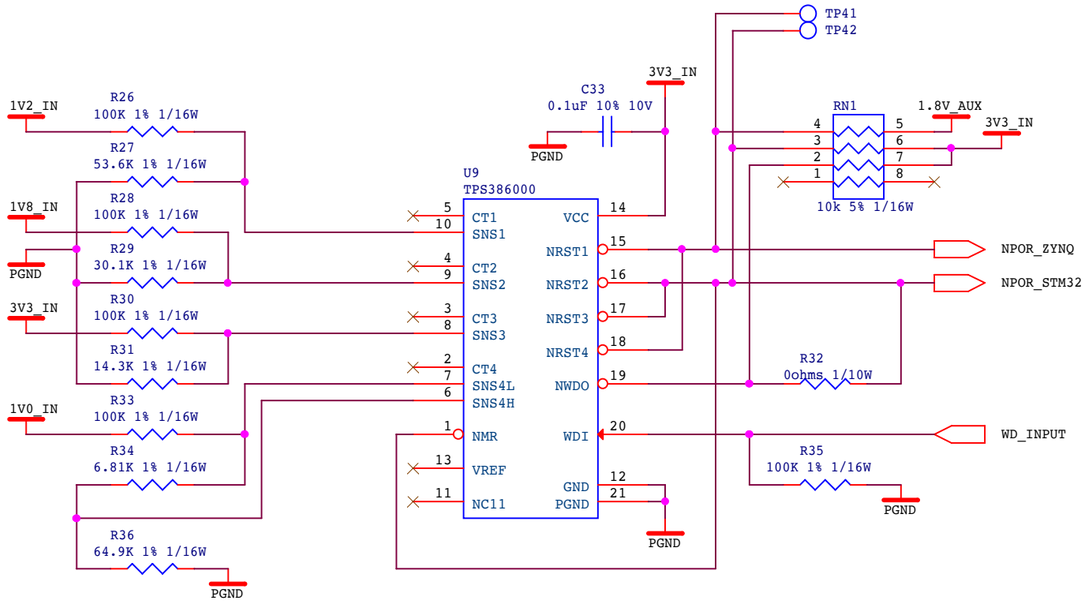
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X1
DESCRIPTION: Power Entry
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 13 OF 30



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DRAWN BY	B. Hammond	11/21/2015
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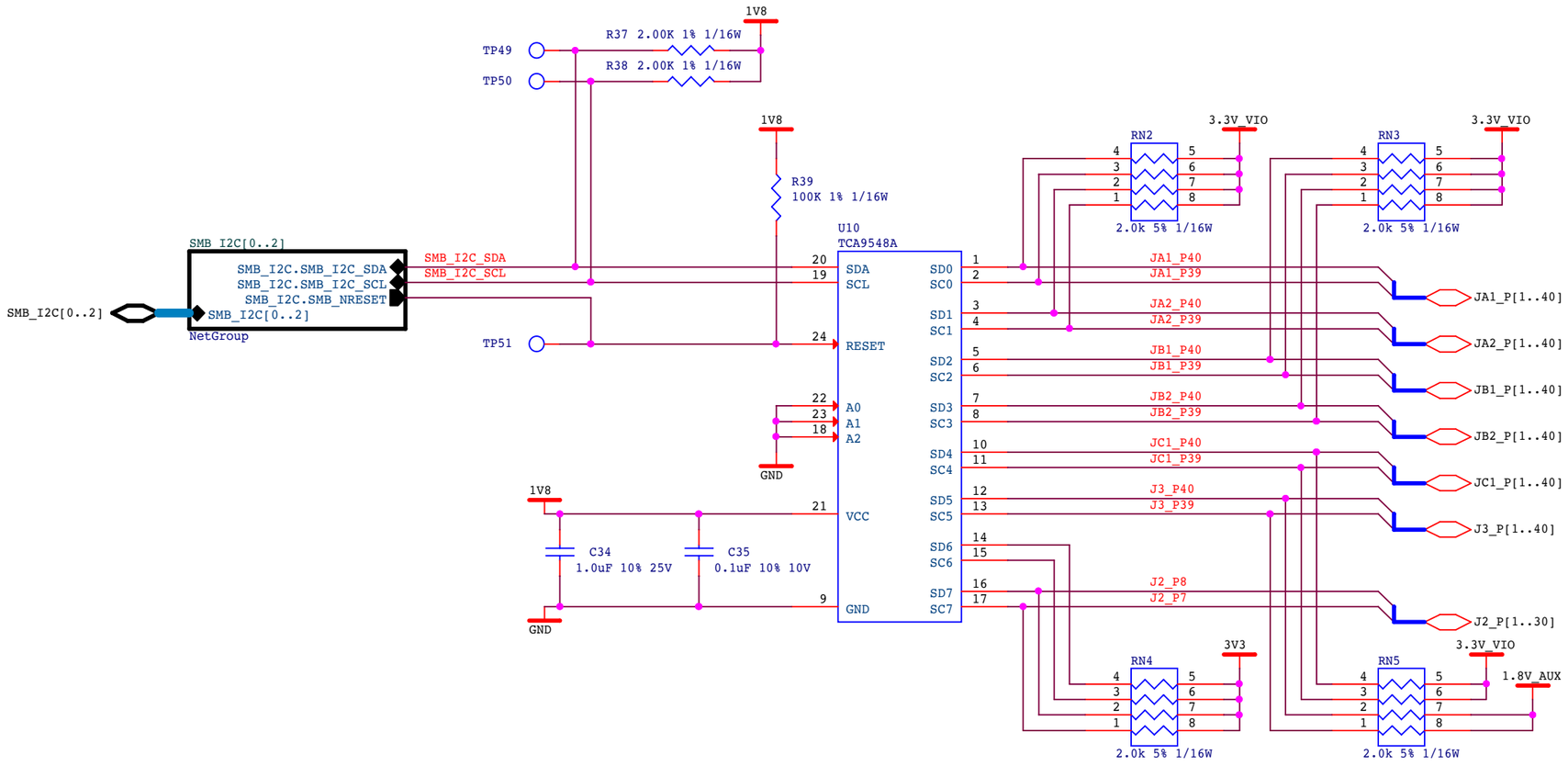
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X9
DESCRIPTION: Quad Voltage Supervisor
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 14 OF 30



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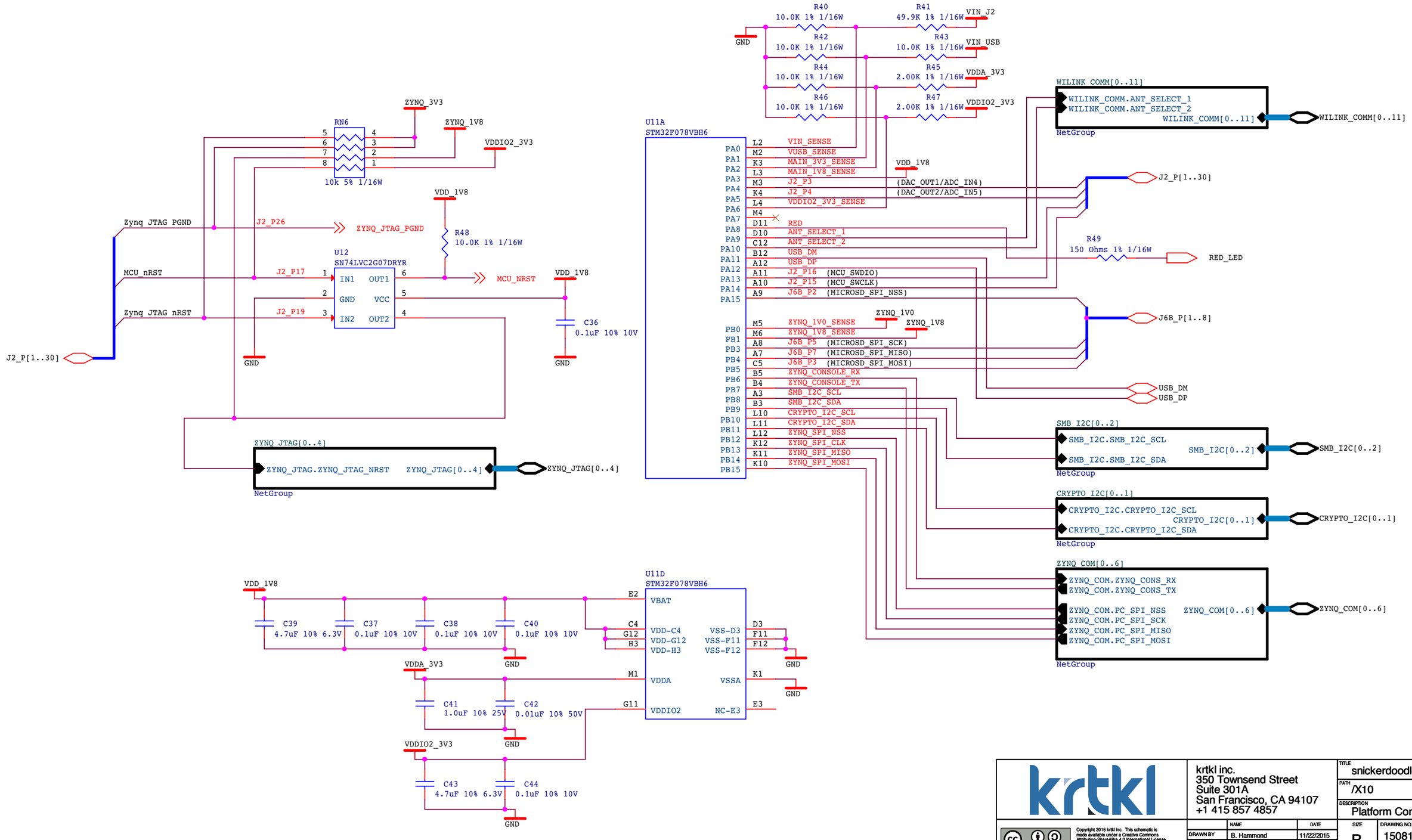
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X11
DESCRIPTION: I2C Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 15 OF 30



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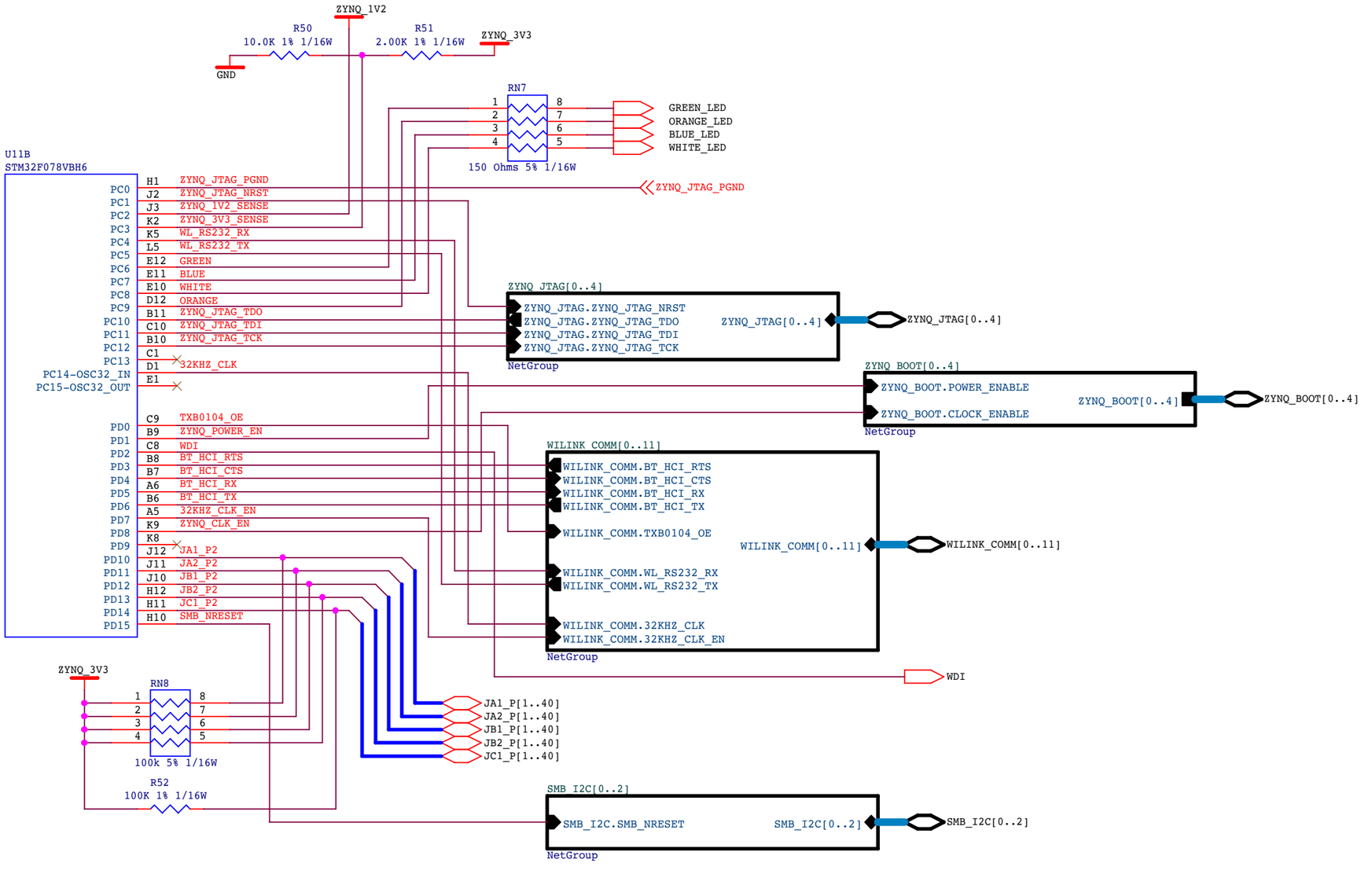
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X10
DESCRIPTION: Platform Controller
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 16 OF 30



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	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
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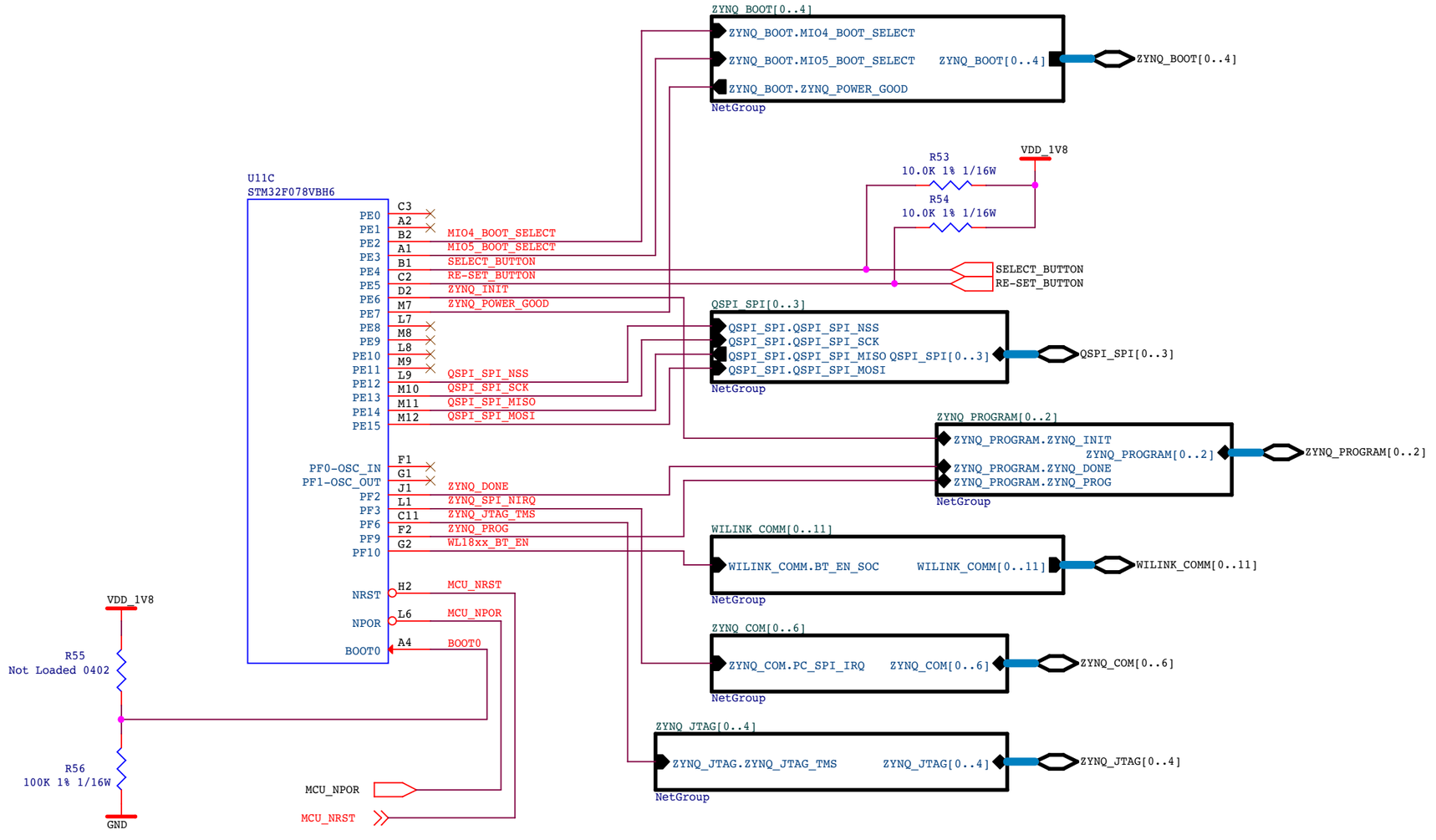
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X10
DESCRIPTION: Platform Controller
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 17 OF 30



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DRAWN BY	B. Hammond	11/22/2015
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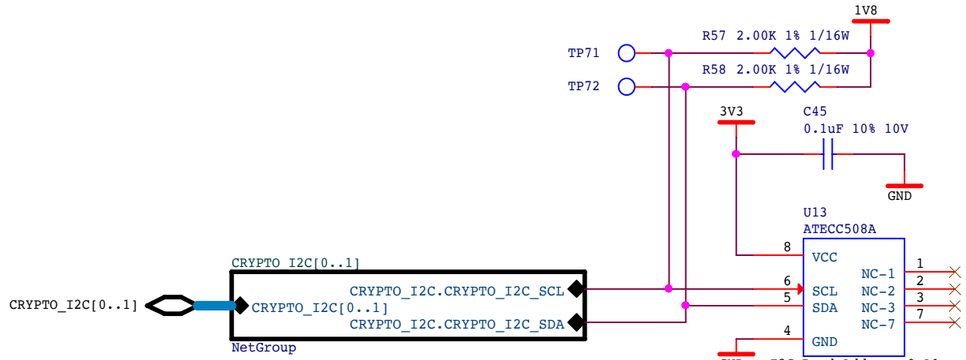
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X10
DESCRIPTION: Platform Controller
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 18 OF 30



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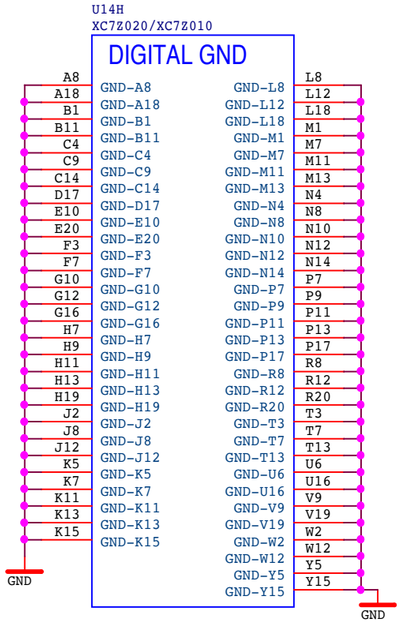
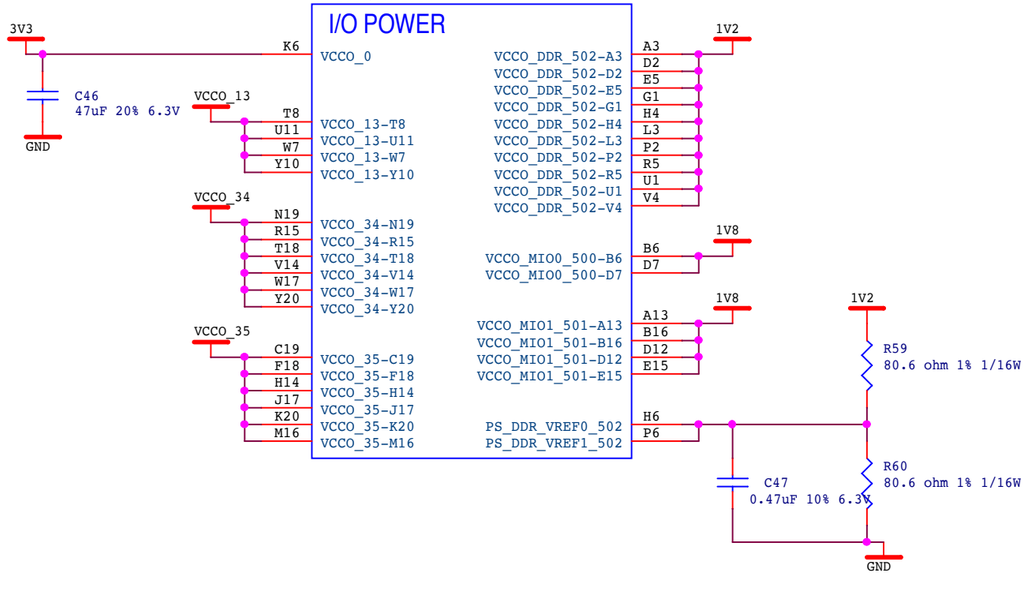
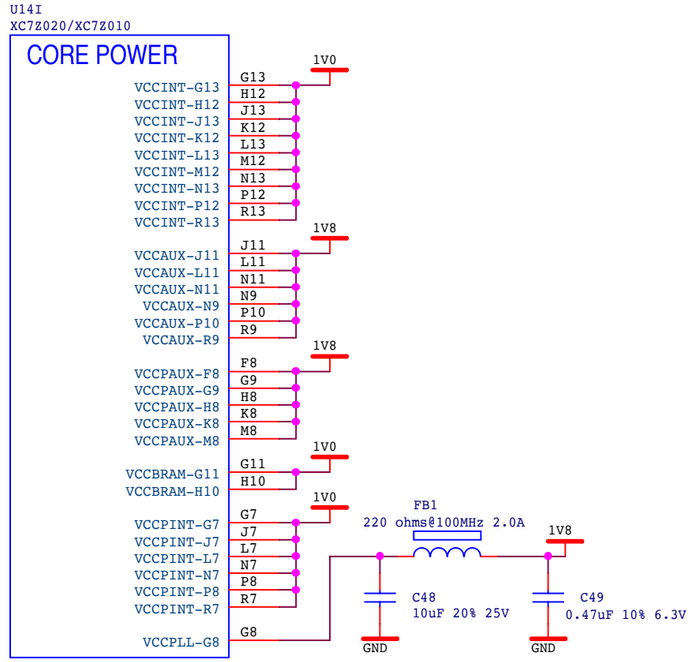
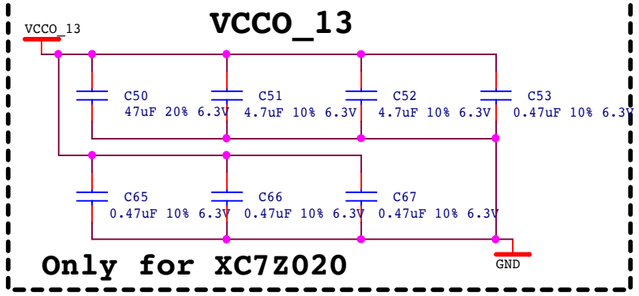
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

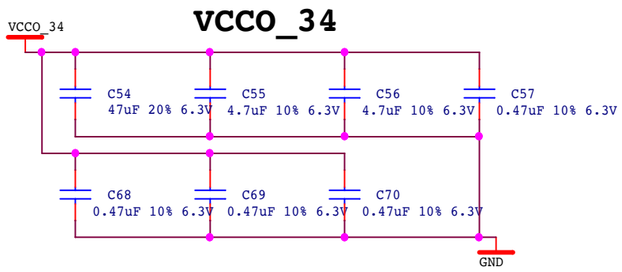
TITLE: snickerdoodle FPGA Module
PATH: /X12
DESCRIPTION: Crypto-Authenticator
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 19 OF 30

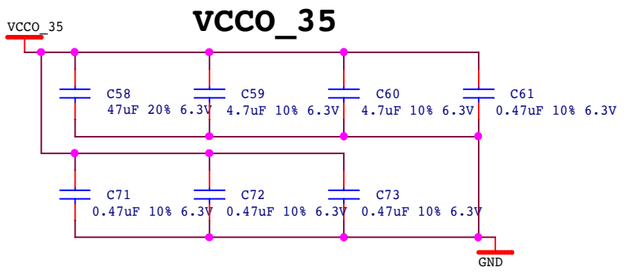


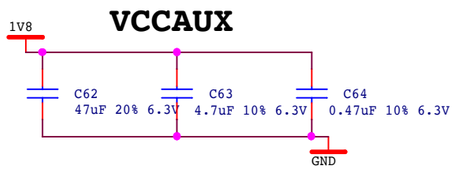


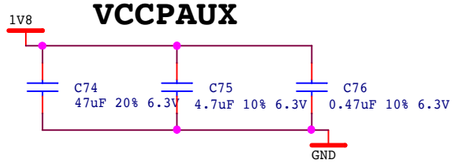


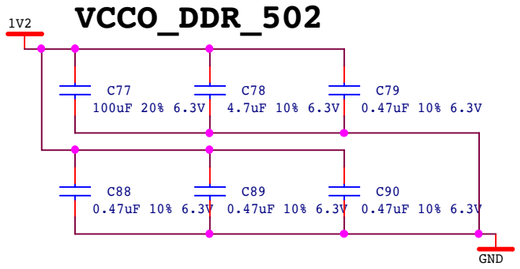


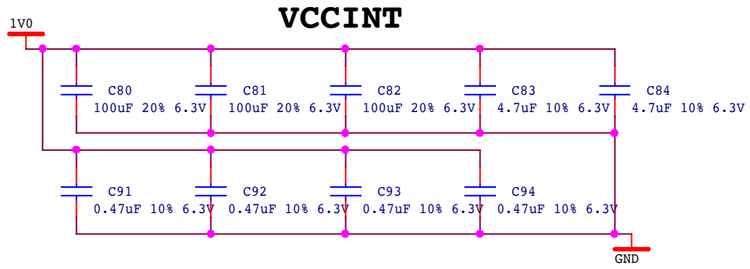


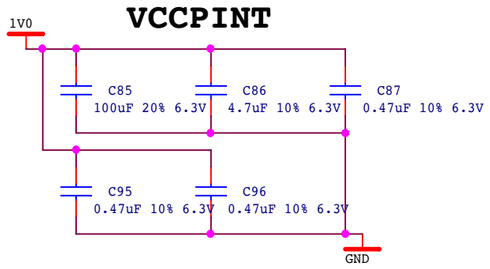


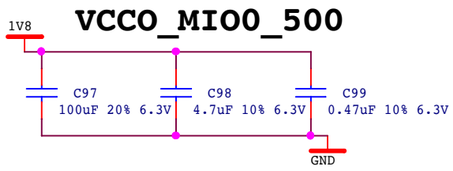


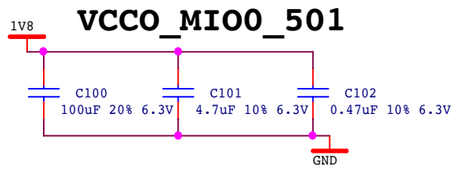


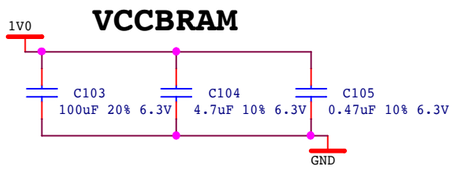












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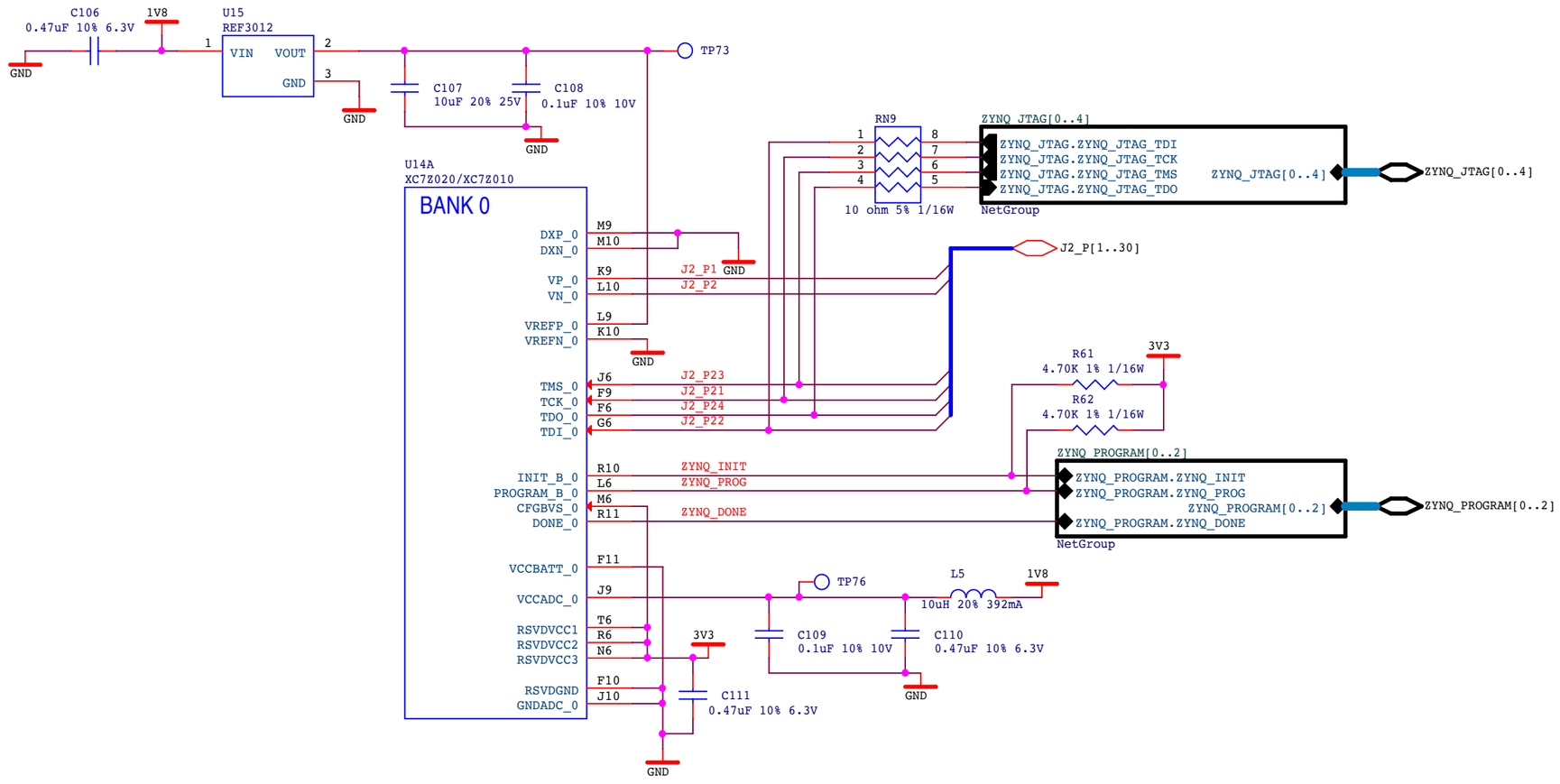
TITLE	snickerdoodle FPGA Module	
PATH	/X13	
DESCRIPTION	Zynq SoC	
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015
SIZE	B	
DRAWING NO.	15081800-01	
REV	2	
SHEET	20 OF 30	



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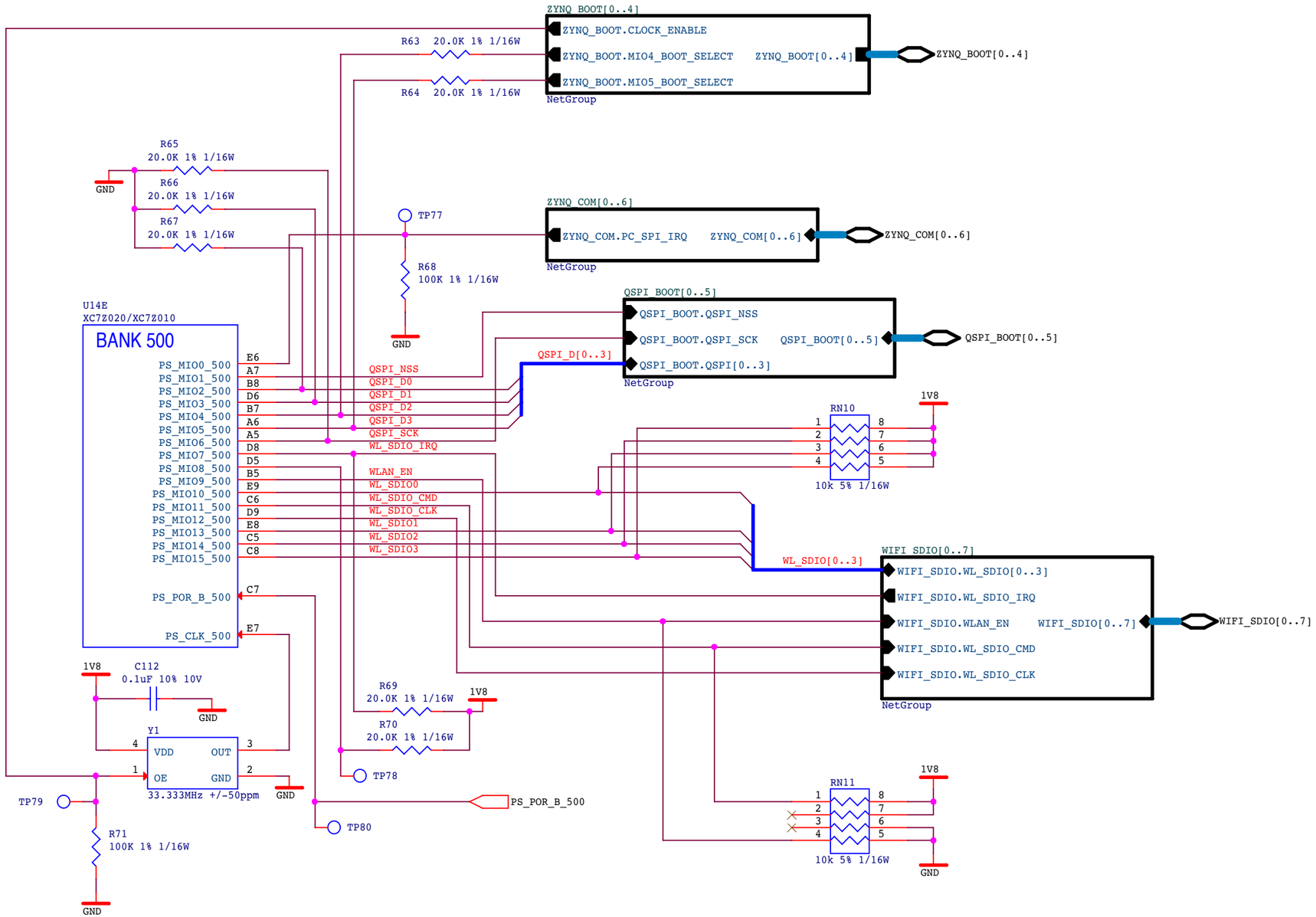
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 21 OF 30



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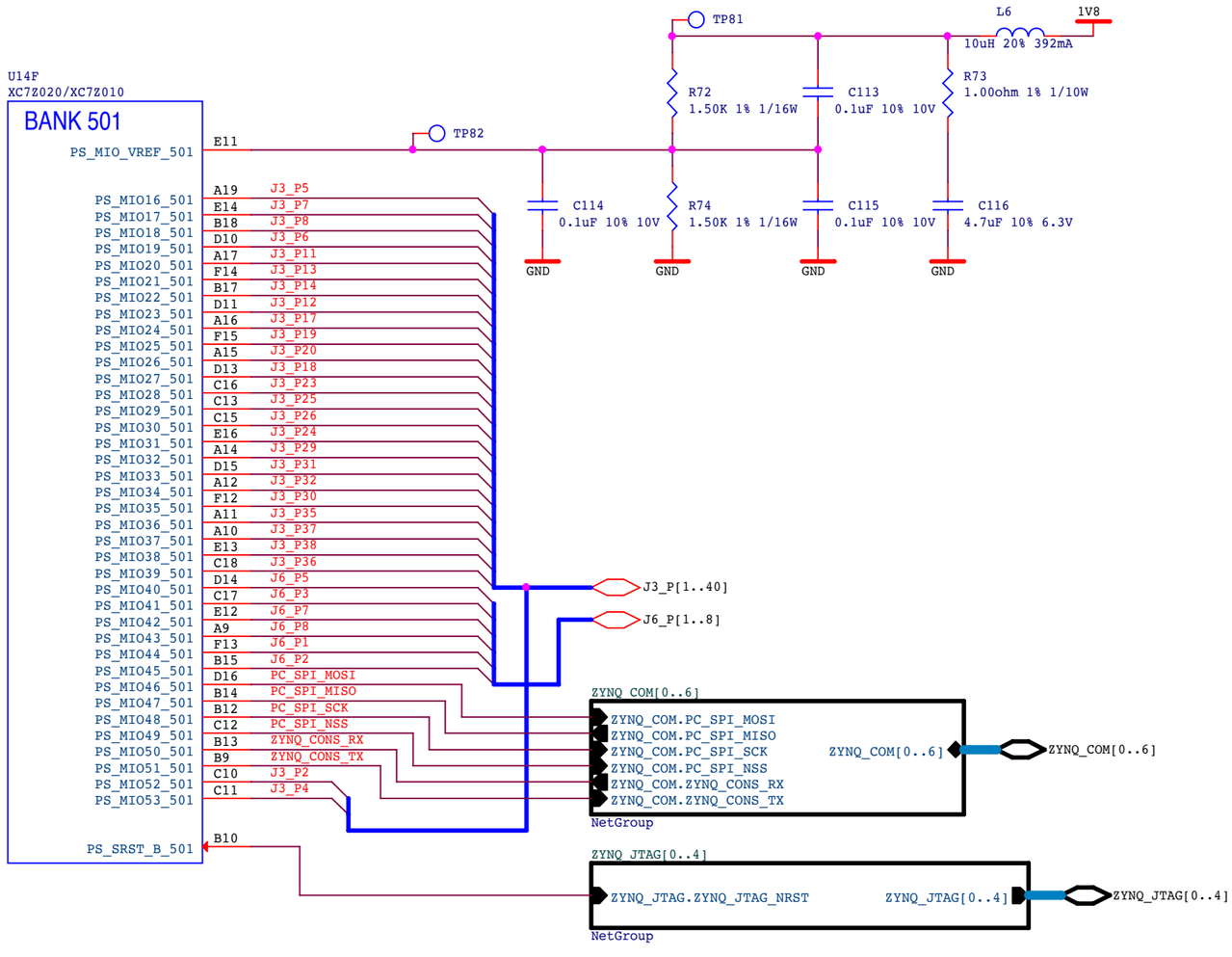
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 22 OF 30



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	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 23 OF 30

U14G
XC7Z020/XC7Z010

BANK 502

PS_DDR_DQ0_502	C3	DQ0
PS_DDR_DQ1_502	B3	DQ1
PS_DDR_DQ2_502	A2	DQ2
PS_DDR_DQ3_502	A4	DQ3
PS_DDR_DQ4_502	D3	DQ4
PS_DDR_DQ5_502	D1	DQ5
PS_DDR_DQ6_502	C1	DQ6
PS_DDR_DQ7_502	E1	DQ7
PS_DDR_DQ8_502	E2	DQ8
PS_DDR_DQ9_502	E3	DQ9
PS_DDR_DQ10_502	G3	DQ10
PS_DDR_DQ11_502	H3	DQ11
PS_DDR_DQ12_502	J3	DQ12
PS_DDR_DQ13_502	H2	DQ13
PS_DDR_DQ14_502	H1	DQ14
PS_DDR_DQ15_502	J1	DQ15
PS_DDR_DQ16_502	P1	DQ16
PS_DDR_DQ17_502	P3	DQ17
PS_DDR_DQ18_502	R3	DQ18
PS_DDR_DQ19_502	R1	DQ19
PS_DDR_DQ20_502	T4	DQ20
PS_DDR_DQ21_502	U4	DQ21
PS_DDR_DQ22_502	U2	DQ22
PS_DDR_DQ23_502	U3	DQ23
PS_DDR_DQ24_502	V1	DQ24
PS_DDR_DQ25_502	Y3	DQ25
PS_DDR_DQ26_502	W1	DQ26
PS_DDR_DQ27_502	Y4	DQ27
PS_DDR_DQ28_502	Y2	DQ28
PS_DDR_DQ29_502	W3	DQ29
PS_DDR_DQ30_502	V2	DQ30
PS_DDR_DQ31_502	V3	DQ31
PS_DDR_A0_502	N2	A0
PS_DDR_A1_502	K2	A1
PS_DDR_A2_502	M3	A2
PS_DDR_A3_502	K3	A3
PS_DDR_A4_502	M4	A4
PS_DDR_A5_502	L1	A5
PS_DDR_A6_502	L4	A6
PS_DDR_A7_502	K4	A7
PS_DDR_A8_502	K1	A8
PS_DDR_A9_502	J4	A9
PS_DDR_A10_502	F5	
PS_DDR_A11_502	G4	
PS_DDR_A12_502	E4	
PS_DDR_A13_502	D4	
PS_DDR_A14_502	F4	
PS_DDR_DQS_P0_502	C2	DQS_P0
PS_DDR_DQS_N0_502	B2	DQS_N0
PS_DDR_DQS_P1_502	G2	DQS_P1
PS_DDR_DQS_N1_502	F2	DQS_N1
PS_DDR_DQS_P2_502	R2	DQS_P2
PS_DDR_DQS_N2_502	T2	DQS_N2
PS_DDR_DQS_P3_502	W5	DQS_P3
PS_DDR_DQS_N3_502	W4	DQS_N3
PS_DDR_CKP_502	L2	CKP
PS_DDR_CKN_502	M2	CKN
PS_DDR_BA0_502	L5	
PS_DDR_BA1_502	R4	
PS_DDR_BA2_502	J5	
PS_DDR_DM0_502	A1	DM0
PS_DDR_DM1_502	F1	DM1
PS_DDR_DM2_502	T1	DM2
PS_DDR_DM3_502	Y1	DM3
PS_DDR_CS_B_502	N1	CS_B
PS_DDR_WE_B_502	M5	
PS_DDR_CAS_B_502	P5	
PS_DDR_RAS_B_502	P4	
PS_DDR_CKE_502	N3	CKE
PS_DDR_ODT_502	N5	
PS_DDR_DRST_B_502	B4	
PS_DDR_VRP_502	H5	
PS_DDR_VRN_502	G5	

R75
40.2 Ohms 1% 1/16W

R76
40.2 Ohms 1% 1/16W

1V2

GND

Match all signal trace lengths for DQ groups with a max deviation of ±50 mils and route on the same layer.

Route address and command signals on a different layer than the data and data mask signals.

DQ[0..31]
A[0..9]
DQS_P[0..3]
DQS_N[0..3]
DM[0..3]
CS_B
CKE

LPDDR2-SDRAM-IO[0..57]
LPDDR2-SDRAM-IO.DQ[0..31]
LPDDR2-SDRAM-IO.A[0..9]
LPDDR2-SDRAM-IO.DQS_P[0..3]
LPDDR2-SDRAM-IO.DQS_N[0..3]
LPDDR2-SDRAM-IO.DM[0..3]
LPDDR2-SDRAM-IO.CS_B
LPDDR2-SDRAM-IO.CKE
LPDDR2-SDRAM-IO.CKP
LPDDR2-SDRAM-IO.CKN
NetGroup

LPDDR2-SDRAM-IO[0..57]
LPDDR2-SDRAM-IO[0..57]

Route clock on inner layers with outer-layer run lengths held to under 500 mils and maintain a 10-mil spacing from other nets. Length match clock traces within ±25 mils, with CKP and CKN traces matched within ±10 mils. Do not route CKP/CKN pair and CKE close to address signals.

Route address and command signals on a different layer than the data and data mask signals.

krtkl

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+1 415 857 4857

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC

	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 24 OF 30

U14D
XC7Z020/XC7Z010

BANK 35

IO_0_35	G14	JA1_P4
IO_L1P_T0_AD0P_35	C20	JA1_P14
IO_L1N_T0_AD0N_35	B20	JA1_P12
IO_L2P_T0_AD8P_35	B19	JA1_P20
IO_L2N_T0_AD8N_35	A20	JA1_P18
IO_L3P_T0_DQS_AD1P_35	E17	JA1_P17
IO_L3N_T0_DQS_AD1N_35	D18	JA1_P19
IO_L4P_T0_35	D19	JA1_P8
IO_L4N_T0_35	D20	JA1_P6
IO_L5P_T0_AD9P_35	E18	JA1_P5
IO_L5N_T0_AD9N_35	E19	JA1_P7
IO_L6P_T0_35	F16	JA1_P11
IO_L6N_T0_VREF_35	F17	JA1_P13
IO_L7P_T1_AD2P_35	M19	JA2_P32
IO_L7N_T1_AD2N_35	M20	JA2_P30
IO_L8P_T1_AD10P_35	M17	JA2_P29
IO_L8N_T1_AD10N_35	M18	JA2_P31
IO_L9P_T1_DQS_AD3P_35	L19	JA2_P23
IO_L9N_T1_DQS_AD3N_35	L20	JA2_P25
IO_L10P_T1_AD11P_35	K19	JA2_P26
IO_L10N_T1_AD11N_35	J19	JA2_P24
IO_L11P_T1_SRCC_35	L16	JA2_P35
IO_L11N_T1_SRCC_35	L17	JA2_P37
IO_L12P_T1_MRCC_35	K17	JA2_P38
IO_L12N_T1_MRCC_35	K18	JA2_P36
IO_L13P_T2_MRCC_35	H16	JA1_P38
IO_L13N_T2_MRCC_35	H17	JA1_P36
IO_L14P_T2_AD4P_SRCC_35	J18	JA1_P35
IO_L14N_T2_AD4N_SRCC_35	H18	JA1_P37
IO_L15P_T2_DQS_AD12P_35	F19	JA1_P23
IO_L15N_T2_DQS_AD12N_35	F20	JA1_P25
IO_L16P_T2_35	G17	JA1_P32
IO_L16N_T2_35	G18	JA1_P30
IO_L17P_T2_AD5P_35	J20	JA1_P29
IO_L17N_T2_AD5N_35	H20	JA1_P31
IO_L18P_T2_AD13P_35	G19	JA1_P26
IO_L18N_T2_AD13N_35	G20	JA1_P24
IO_L19P_T3_35	H15	JA2_P14
IO_L19N_T3_VREF_35	G15	JA2_P12
IO_L20P_T3_AD6P_35	K14	JA2_P20
IO_L20N_T3_AD6N_35	J14	JA2_P18
IO_L21P_T3_DQS_AD14P_35	N15	JA2_P17
IO_L21N_T3_DQS_AD14N_35	N16	JA2_P19
IO_L22P_T3_AD7P_35	L14	JA2_P5
IO_L22N_T3_AD7N_35	L15	JA2_P7
IO_L23P_T3_35	M14	JA2_P11
IO_L23N_T3_35	M15	JA2_P13
IO_L24P_T3_AD15P_35	K16	JA2_P8
IO_L24N_T3_AD15N_35	J16	JA2_P6
IO_25_35	J15	JA2_P4

JA1_P[1..40]

JA2_P[1..40]

U14C
XC7Z020/XC7Z010

BANK 34

IO_0_34	R19	JB2_P4
IO_L1P_T0_34	T11	JB1_P5
IO_L1N_T0_34	T10	JB1_P7
IO_L2P_T0_34	T12	JB1_P8
IO_L2N_T0_34	U12	JB1_P6
IO_L3P_T0_DQS_PUDC_B_34	U13	JB1_P17
IO_L3N_T0_DQS_34	V13	JB1_P19
IO_L4P_T0_34	V12	JB1_P14
IO_L4N_T0_34	W13	JB1_P12
IO_L5P_T0_34	T14	JB1_P20
IO_L5N_T0_34	T15	JB1_P18
IO_L6P_T0_34	P14	JB1_P11
IO_L6N_T0_VREF_34	R14	JB1_P13
IO_L7P_T1_34	Y16	JB1_P26
IO_L7N_T1_34	Y17	JB1_P24
IO_L8P_T1_34	W14	JB1_P29
IO_L8N_T1_34	Y14	JB1_P31
IO_L9P_T1_DQS_34	T16	JB1_P23
IO_L9N_T1_DQS_34	U17	JB1_P25
IO_L10P_T1_34	V15	JB1_P32
IO_L10N_T1_34	W15	JB1_P30
IO_L11P_T1_SRCC_34	U14	JB1_P35
IO_L11N_T1_SRCC_34	U15	JB1_P37
IO_L12P_T1_MRCC_34	U18	JB1_P38
IO_L12N_T1_MRCC_34	U19	JB1_P36
IO_L13P_T2_MRCC_34	N18	JB2_P38
IO_L13N_T2_MRCC_34	P19	JB2_P36
IO_L14P_T2_SRCC_34	N20	JB2_P35
IO_L14N_T2_SRCC_34	P20	JB2_P37
IO_L15P_T2_DQS_34	T20	JB2_P23
IO_L15N_T2_DQS_34	U20	JB2_P25
IO_L16P_T2_34	V20	JB2_P29
IO_L16N_T2_34	W20	JB2_P31
IO_L17P_T2_34	Y18	JB2_P32
IO_L17N_T2_34	Y19	JB2_P30
IO_L18P_T2_34	V16	JB2_P26
IO_L18N_T2_34	W16	JB2_P24
IO_L19P_T3_34	R16	JB2_P14
IO_L19N_T3_VREF_34	R17	JB2_P12
IO_L20P_T3_34	T17	JB2_P11
IO_L20N_T3_34	R18	JB2_P13
IO_L21P_T3_DQS_34	V17	JB2_P17
IO_L21N_T3_DQS_34	V18	JB2_P19
IO_L22P_T3_34	W18	JB2_P20
IO_L22N_T3_34	W19	JB2_P18
IO_L23P_T3_34	N17	JB2_P5
IO_L23N_T3_34	P18	JB2_P7
IO_L24P_T3_34	P15	JB2_P8
IO_L24N_T3_34	P16	JB2_P6
IO_25_34	T19	JB1_P4

JB1_P[1..40]

JB2_P[1..40]

U14B
XC7Z020/XC7Z010

BANK 13

IO_L6N_T0_VREF_13	V5	JC1_P4
IO_L11P_T1_SRCC_13	U7	JC1_P5
IO_L11N_T1_SRCC_13	V7	JC1_P7
IO_L12P_T1_MRCC_13	T9	JC1_P8
IO_L12N_T1_MRCC_13	U10	JC1_P6
IO_L13P_T2_MRCC_13	Y7	JC1_P38
IO_L13N_T2_MRCC_13	Y6	JC1_P36
IO_L14P_T2_SRCC_13	Y9	JC1_P35
IO_L14N_T2_SRCC_13	Y8	JC1_P37
IO_L15P_T2_DQS_13	V8	JC1_P23
IO_L15N_T2_DQS_13	W8	JC1_P25
IO_L16P_T2_13	W10	JC1_P32
IO_L16N_T2_13	W9	JC1_P30
IO_L17P_T2_13	U9	JC1_P29
IO_L17N_T2_13	U8	JC1_P31
IO_L18P_T2_13	W11	JC1_P26
IO_L18N_T2_13	Y11	JC1_P24
IO_L19P_T3_13	T5	JC1_P11
IO_L19N_T3_VREF_13	U5	JC1_P13
IO_L20P_T3_13	Y12	JC1_P14
IO_L20N_T3_13	Y13	JC1_P12
IO_L21P_T3_DQS_13	V11	JC1_P17
IO_L21N_T3_DQS_13	V10	JC1_P19
IO_L22P_T3_13	V6	JC1_P20
IO_L22N_T3_13	W6	JC1_P18

JC1_P[1..40]

Only for XC7Z020

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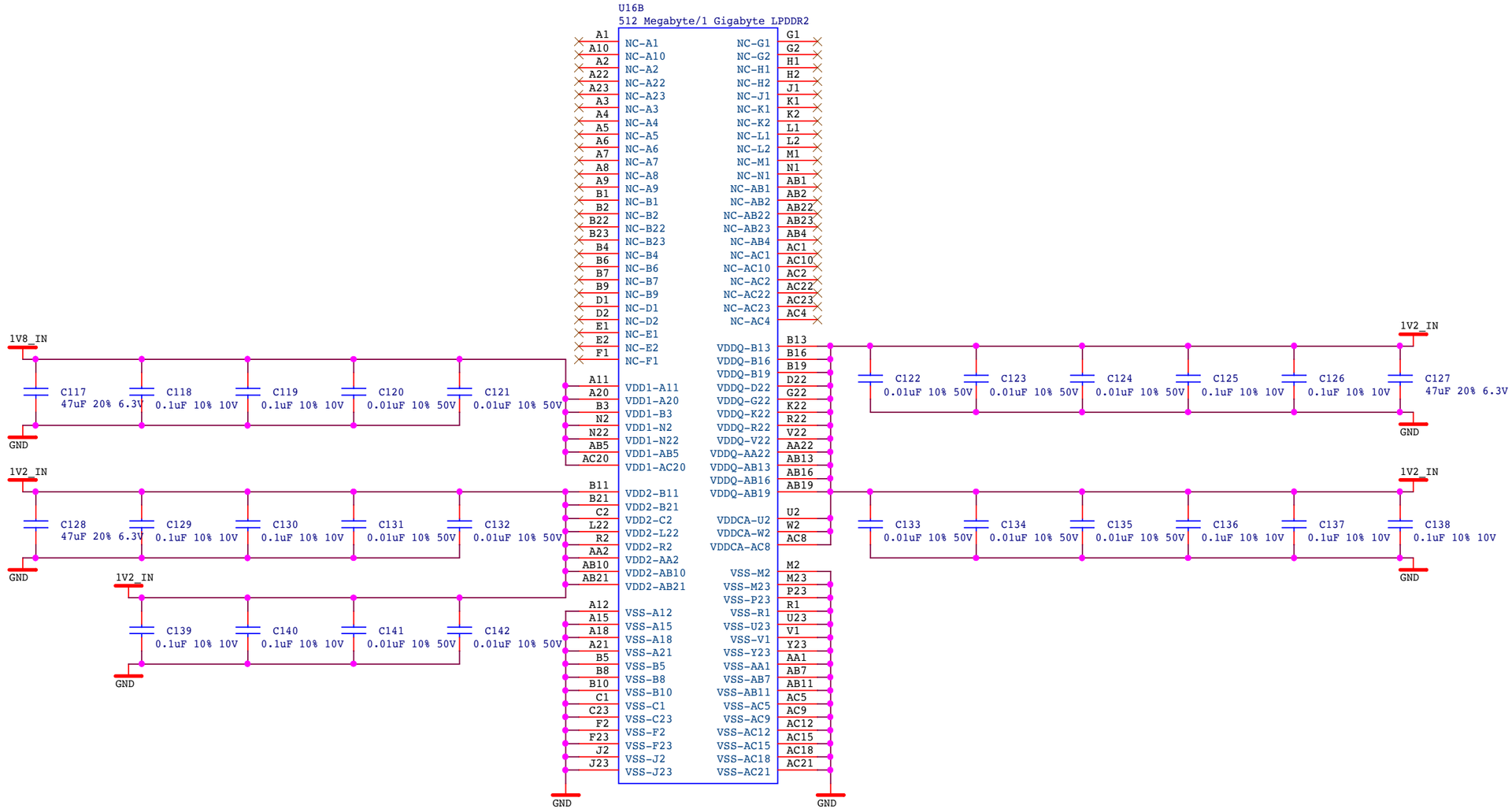
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 25 OF 30



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	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X14
DESCRIPTION: LPDDR2 RAM
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 26 OF 30

Route address and command signals on a different layer than the data and data mask signals.

Match all signal trace lengths for DQ groups with a max deviation of ±50 mils and route on the same layer.

LPDDR2-SDRAM-IO[0..57]

LPDDR2-SDRAM-IO[0..57]

LPDDR2-SDRAM-IO.DQ[0..31]
LPDDR2-SDRAM-IO.DQS_P[0..3]
LPDDR2-SDRAM-IO.DQS_N[0..3]
LPDDR2-SDRAM-IO.DM[0..3]
LPDDR2-SDRAM-IO[0..57]
LPDDR2-SDRAM-IO.CS_B
LPDDR2-SDRAM-IO.CKE
LPDDR2-SDRAM-IO.CKP
LPDDR2-SDRAM-IO.CKN
LPDDR2-SDRAM-IO.A[0..9]

NetGroup

DQ[0..31]
DQS_P[0..3]
DQS_N[0..3]
DM[0..3]
CS_B
CKE
CKP
CKN
A[0..9]

U16A
512 Megabyte/1 Gigabyte LPDDR2

DQS_P3	B18	DQS_P3	DQ31	B12	DQ31
DQS_P2	AB18	DQS_P2	DQ30	A13	DQ30
DQS_P1	J22	DQS_P1	DQ29	A14	DQ29
DQS_P0	R23	DQS_P0	DQ28	B14	DQ28
			DQ27	B15	DQ27
DQS_N3	A19	DQS_N3	DQ26	A16	DQ26
DQS_N2	AC19	DQS_N2	DQ25	A17	DQ25
DQS_N1	K23	DQS_N1	DQ24	B17	DQ24
DQS_N0	P22	DQS_N0	DQ23	AC17	DQ23
			DQ22	AB17	DQ22
DM3	B20	DM3	DQ21	AC16	DQ21
DM2	AB20	DM2	DQ20	AB15	DQ20
DM1	L23	DM1	DQ19	AC14	DQ19
DM0	N23	DM0	DQ18	AB14	DQ18
			DQ17	AC13	DQ17
CS_B	AB3	CS_B	DQ16	AB12	DQ16
CKE	AC3	CKE	DQ15	C22	DQ15
CKP	Y2	CKP	DQ14	D23	DQ14
CKN	Y1	CKN	DQ13	E23	DQ13
			DQ12	E22	DQ12
A9	T1	A9	DQ11	F22	DQ11
A8	T2	A8	DQ10	G23	DQ10
A7	U1	A7	DQ9	H23	DQ9
A6	V2	A6	DQ8	H22	DQ8
A5	W1	A5	DQ7	T23	DQ7
A4	AB9	A4	DQ6	T22	DQ6
A3	AB8	A3	DQ5	U22	DQ5
A2	AC7	A2	DQ4	V23	DQ4
A1	AB6	A1	DQ3	W23	DQ3
A0	AC6	A0	DQ2	W22	DQ2
			DQ1	Y22	DQ1
AC11		ZQ1	DQ0	AA23	DQ0
P1		ZQ0			
P2		VREFCA	VREFDQ	M22	

Route clocks on inner layers with outer-layer run lengths held to under 500 mils and maintain a 10-mil spacing from other nets. Length match all clock traces within ±25 mils, with CKP and CKN traces matched within ±10 mils. Do not route CKP/CKN pair and CKE close to address signals.

R77
240 ohm 1% 1/16W
R78
240 ohm 1% 1/16W
R79
4.70K 1% 1/16W

GND

Route address and command signals on a different layer than the data and data mask signals.

L7
10uH 20% 392mA
1V2_IN

L8
10uH 20% 392mA
1V2_IN

TP88
TP90

R80
1.00ohm 1% 1/10W
C143
0.1uF 10% 10V
R81
1.50K 1% 1/16W
VREFCA

R82
1.00ohm 1% 1/10W
C144
0.1uF 10% 10V
R83
1.50K 1% 1/16W
VREFDQ

C145
4.7uF 10% 6.3V
C146
0.1uF 10% 10V
R84
1.50K 1% 1/16W
C147
0.1uF 10% 10V
C148
0.1uF 10% 10V

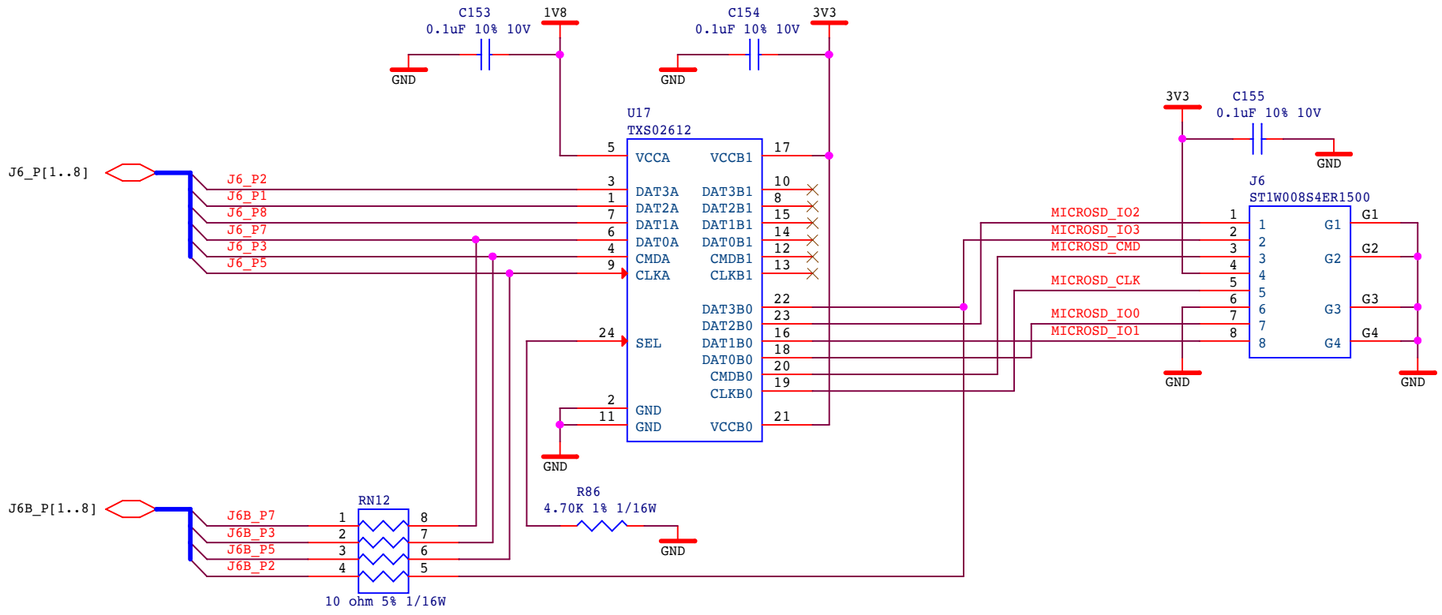
C149
4.7uF 10% 6.3V
C150
0.1uF 10% 10V
R85
1.50K 1% 1/16W
C151
0.1uF 10% 10V
C152
0.1uF 10% 10V

GND

krtkl inc.
350 Townsend Street
Suite 301A
San Francisco, CA 94107
+1 415 857 4857

	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X14
DESCRIPTION: LPDDR2 RAM
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 27 OF 30



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San Francisco, CA 94107
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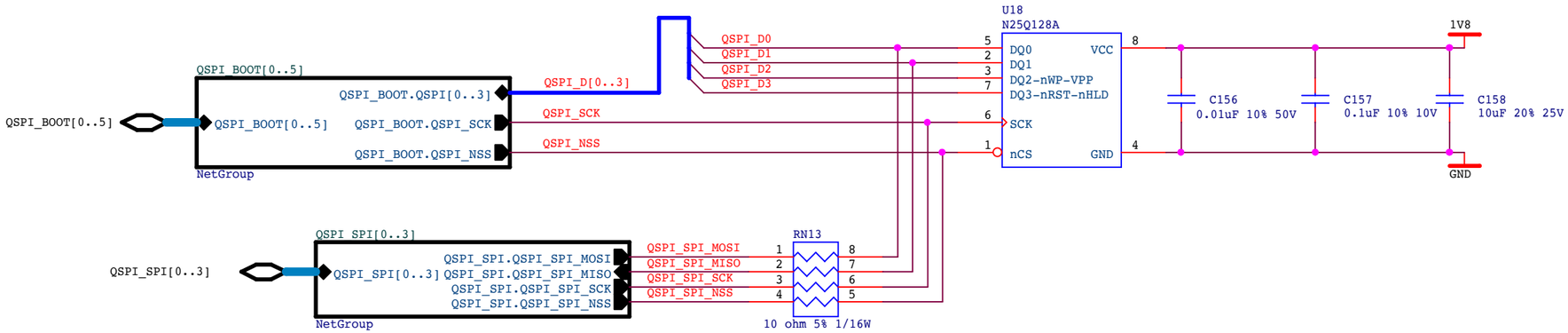
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/21/2015
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X15
DESCRIPTION: microSD Flash
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 28 OF 30



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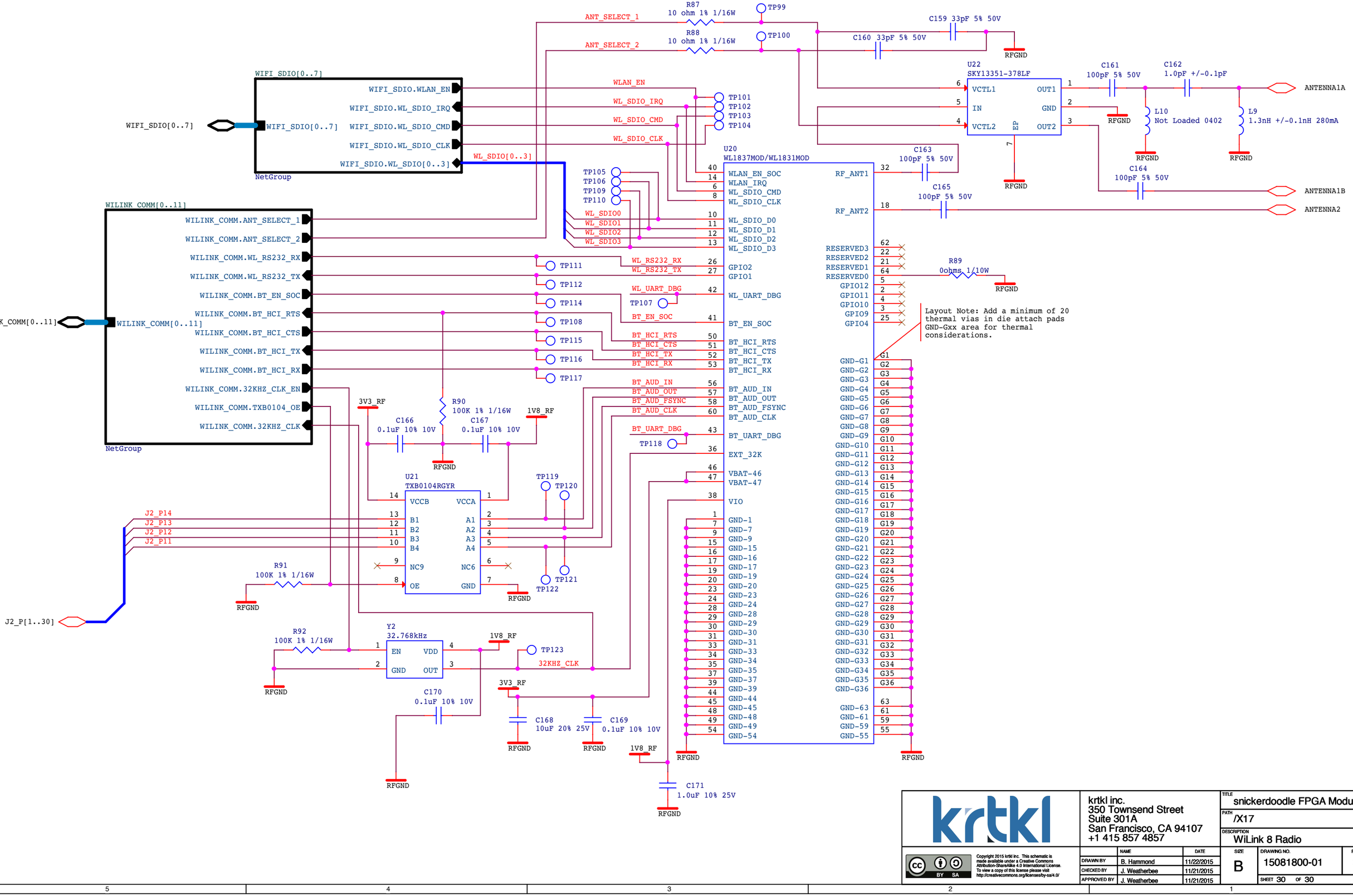
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/21/2015
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X16
DESCRIPTION: QSPI Flash
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 29 OF 30



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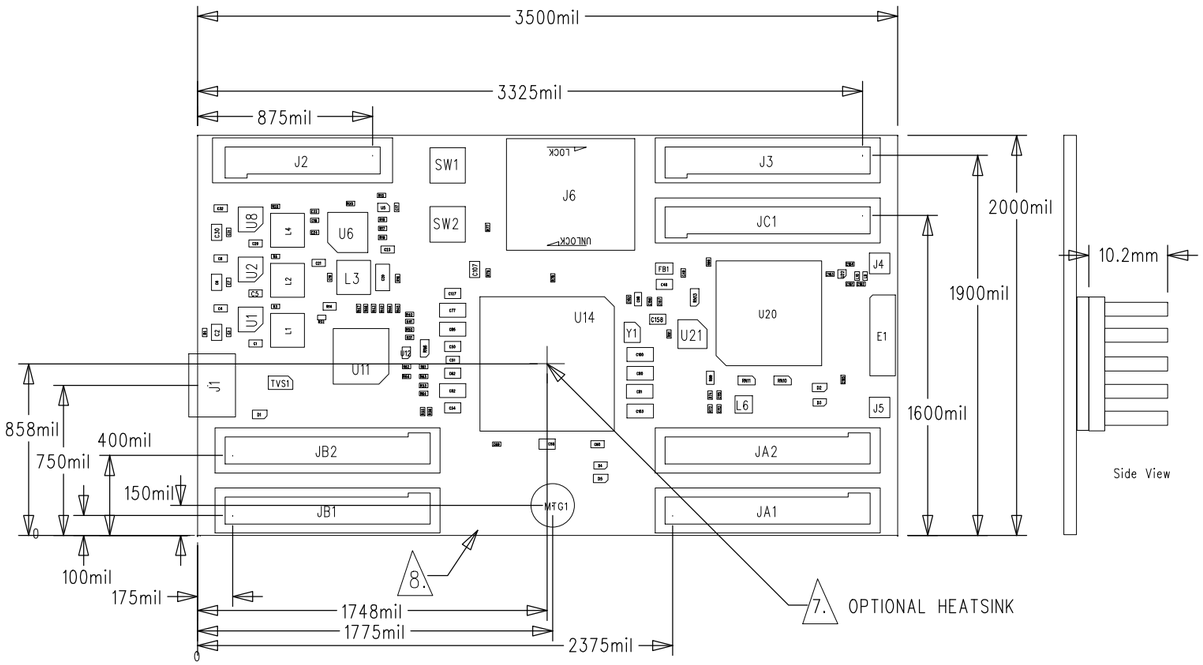
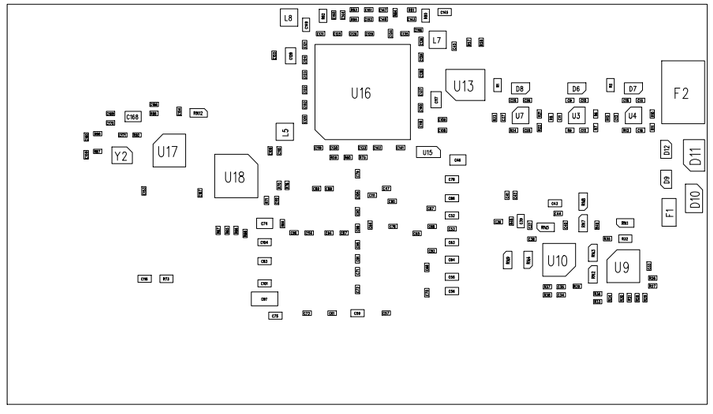
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/21/2015
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X17
DESCRIPTION: WiLink 8 Radio
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 30 OF 30

REV	DESCRIPTION	APPD BY	DATE
V1.0			08/01/15
V2.0			01/16/16





NOTES: UNLESS OTHERWISE SPECIFIED.

ALL SPECIFICATIONS REFERENCED SHALL BE OF THE LATEST REVISION.

1. CONTROLLING DIMENSIONS AND SUPPLIED DATA ARE IN MILLIMETERS. DIMENSIONS AND TOLERANCES PER ASME Y14.5M.
2. ASSEMBLE IN ACCORDANCE WITH IPC-A-610 CLASS 2.
3. ESD PRECAUTIONS DURING HANDLING AND ASSEMBLY TO BE IN ACCORDANCE WITH EIA JESD 625.
4. MAXIMUM LEAD PROTRUSION ON SECONDARY SIDE TO BE 1.5 MAX.
5. Use water soluble flux for SMT, and no clean flux for secondary solder steps if required
6. Board Cleaning: removal of flux residue is required after first pass SMT, hand solder and rework.

7. OPTIONAL HEATSINK (HS1)

8. SERIAL NUMBER TO BE APPLIED TO RAW PCB FAB PRIOR TO ASSEMBLY, AT LOCATION IDENTIFIED (TOP SIDE).

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- INTERPRET DRAWING IAW ASME Y14.100-2000
- DIMENSIONING & TOLERANCING IAW ASME Y14.5-1994
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- DIMENSIONS ARE IN MILLIMETERS (INCHES)
- TOLERANCES ARE: ANGLES 1.0
  1 PLACE DECIMAL .8 (.031)
  2 PLACE DECIMAL .25 (.010)
- SURFACE FINISH 63
- REMOVE ALL BURRS AND SHARP EDGES .25 RAD MAX.
- CONCENTRICITY MACHINED DIA: .05 FIM
- MACHINED TOOL MISMATCH .05 MAX.

DRAWING DESCRIPTION		
PCB Assembly Primary Side (TopLayer)		
DESIGNER	D. BEANE / J. COX	01AUG15
ENGINEER	J WEATHERBEE	16JAN16
CHECK BY	B HAMMOND	16JAN16
Q. A. BY	J WEATHERBEE	16JAN16

SECURITY LEVEL: CONFIDENTIAL - STEALTH MODE

DOCUMENT NUMBER: 15081800-06 REV. 2.0

TITLE: PCB, Snickerdoodle

SHEET 1 of 1 | SIZE C | SCALE 1:1

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CORP. NO. | SHT | REV