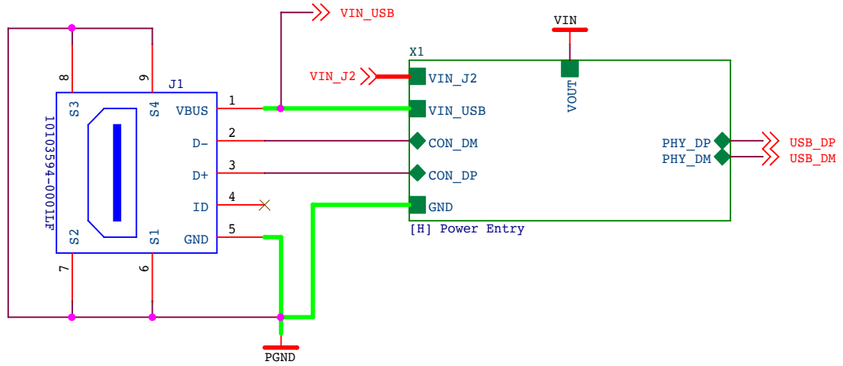
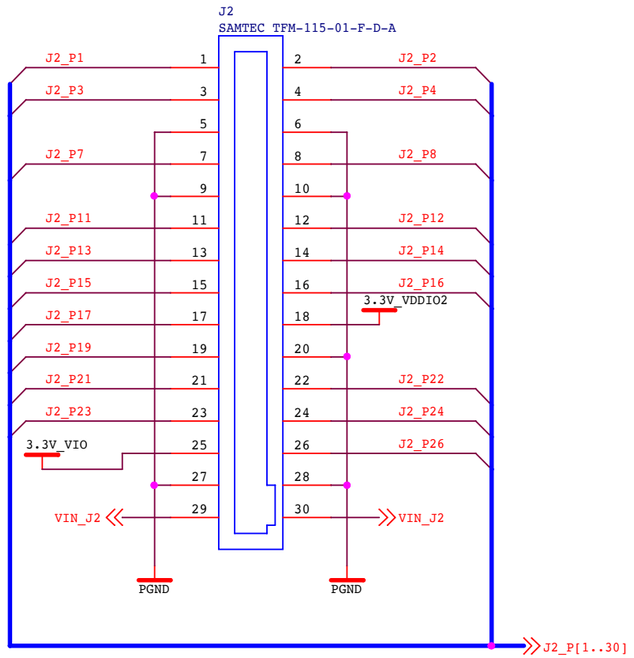
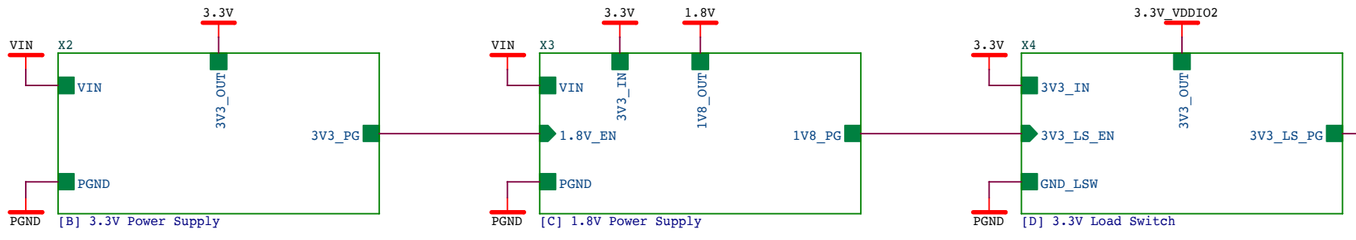
Rev.	Description	CO Number	Date	Approved By	Checked By
2	Alpha Prototype	00001	09/01/2015	JJW	BEH

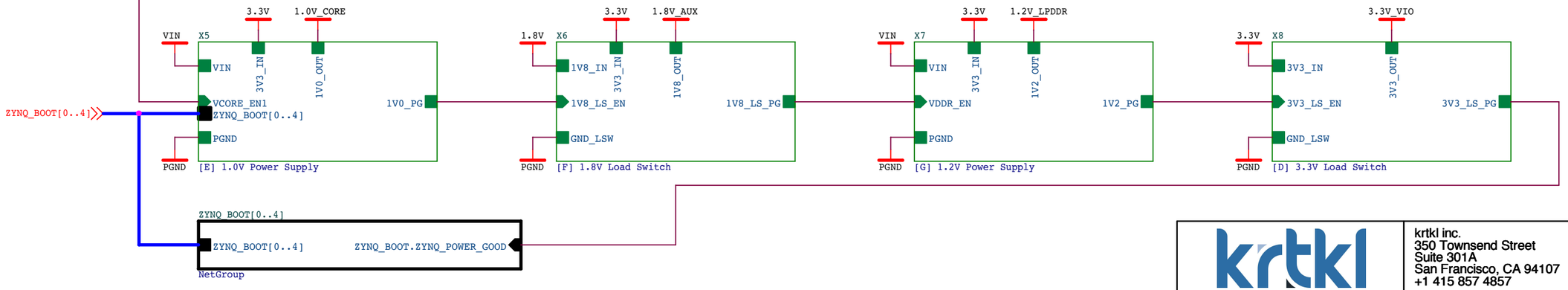
Power/JTAG/SWD/BT Audio/I2C/DAC/ADC





PRELIMINARY REVISION 2 ALPHA SCHEMATIC
NOT APPROVED FOR GENERAL PRODUCTION





Minimum Trace Ratings

6000mA	
4000mA	
2000mA	
1000mA	
200mA	

Minimum Plane Ratings

+VIN	4000mA
+3.3V	4000mA
+1.8V	2000mA
+3.3V_VDDIO2	4000mA
+1.0V_CORE	6000mA
+1.8V_AUX	2000mA
+1.2V_LPDDR	2000mA
+3.3V_VIO	4000mA

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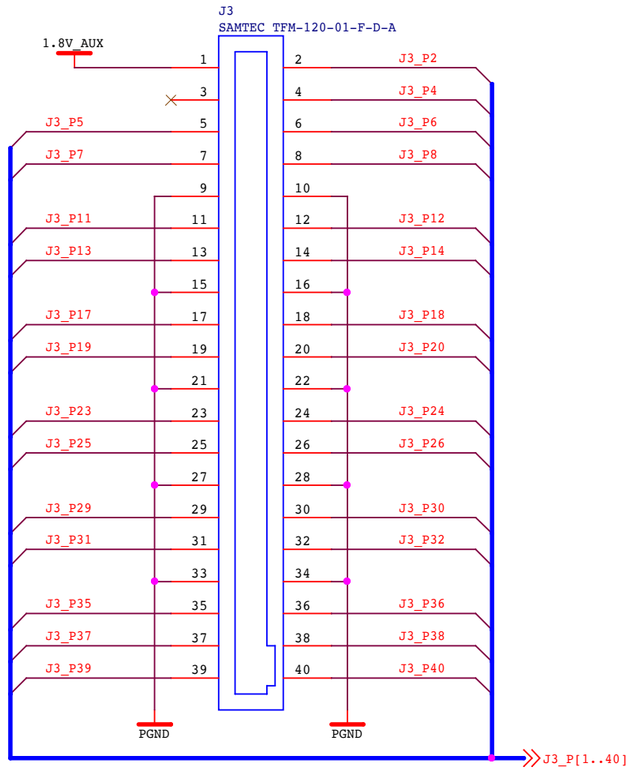
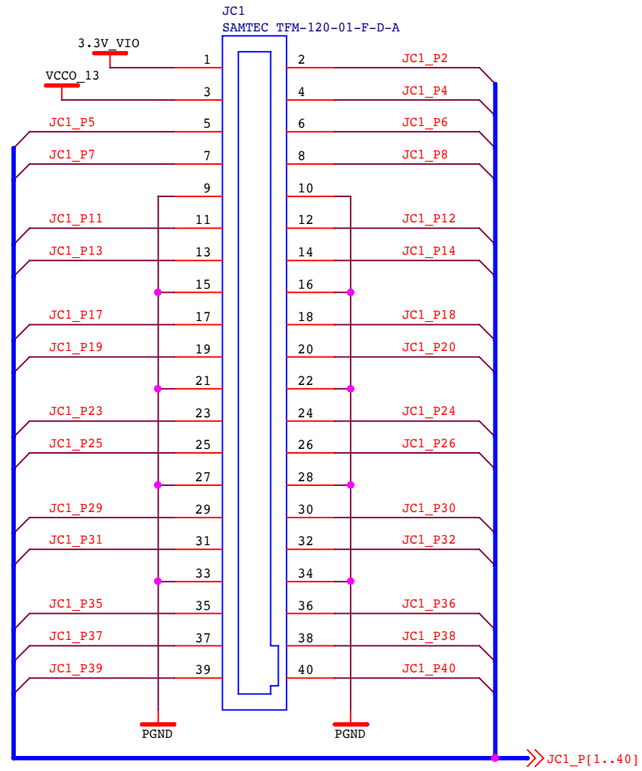
	NAME	DATE
DRAWN BY	J. Weatherbee	08/17/2015
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 1 OF 30

CPU GPIO/USB ULPI/GigE RGMII/SPI/I2C/UART/CAN



FPGA I/O



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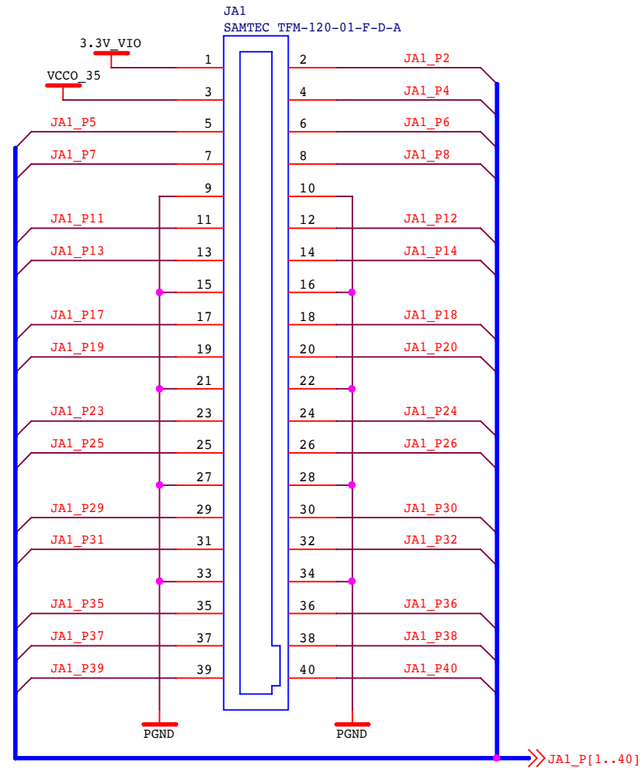

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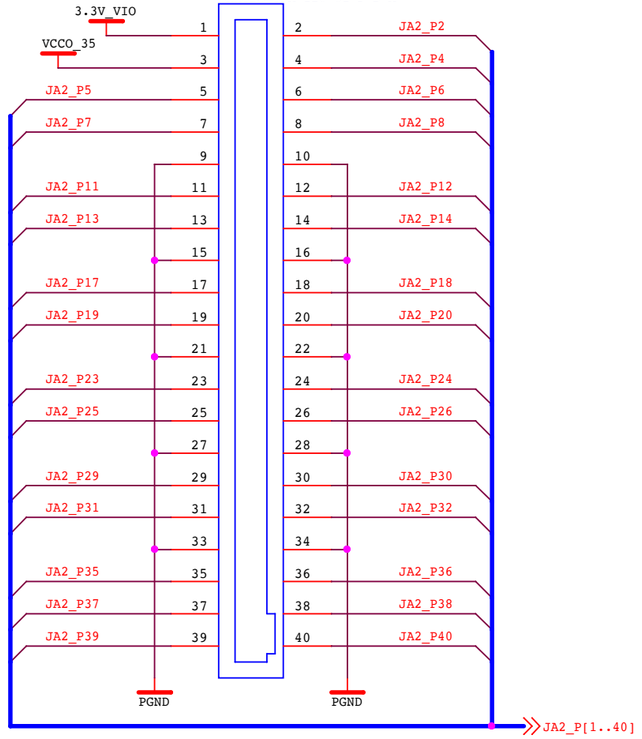
	NAME	DATE
DRAWN BY	J. Weatherbee	11/21/2015
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 2 OF 30

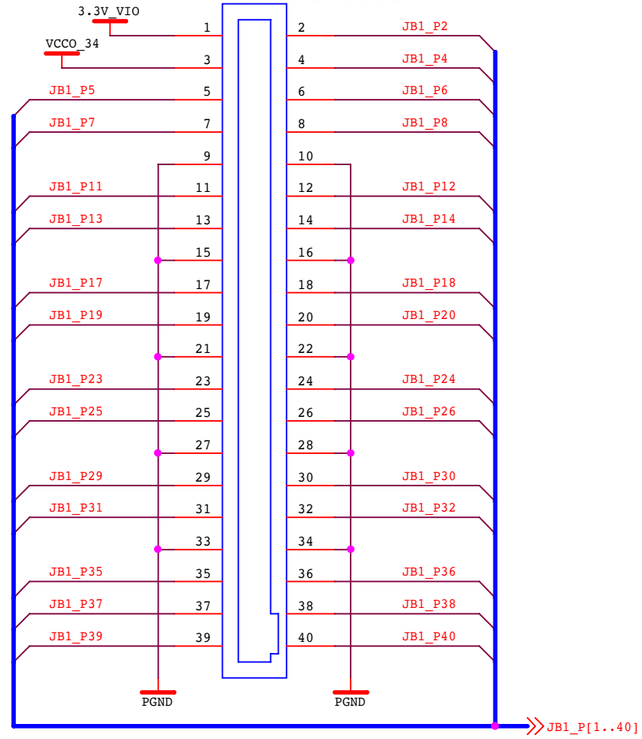
FPGA I/O

JA2
SAMTEC TFM-120-01-F-D-A



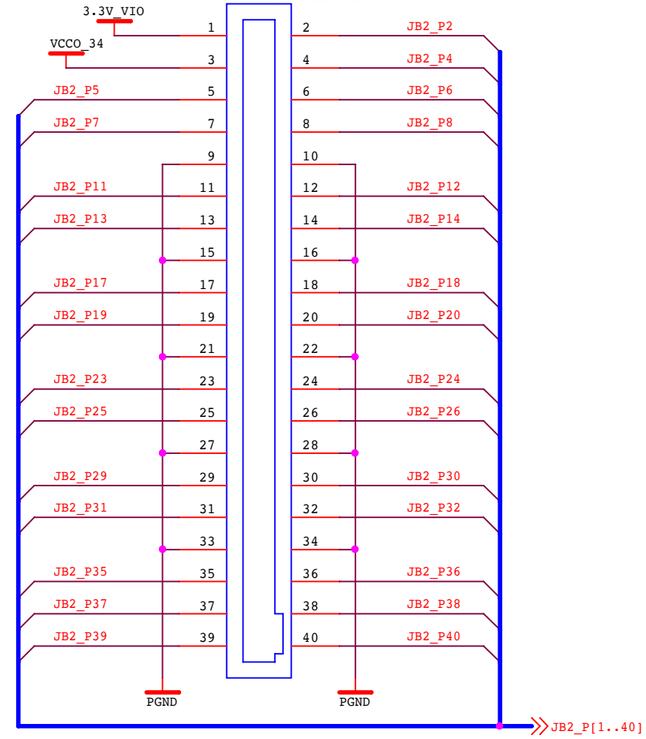
FPGA I/O

JB1
SAMTEC TFM-120-01-F-D-A



FPGA I/O

JB2
SAMTEC TFM-120-01-F-D-A



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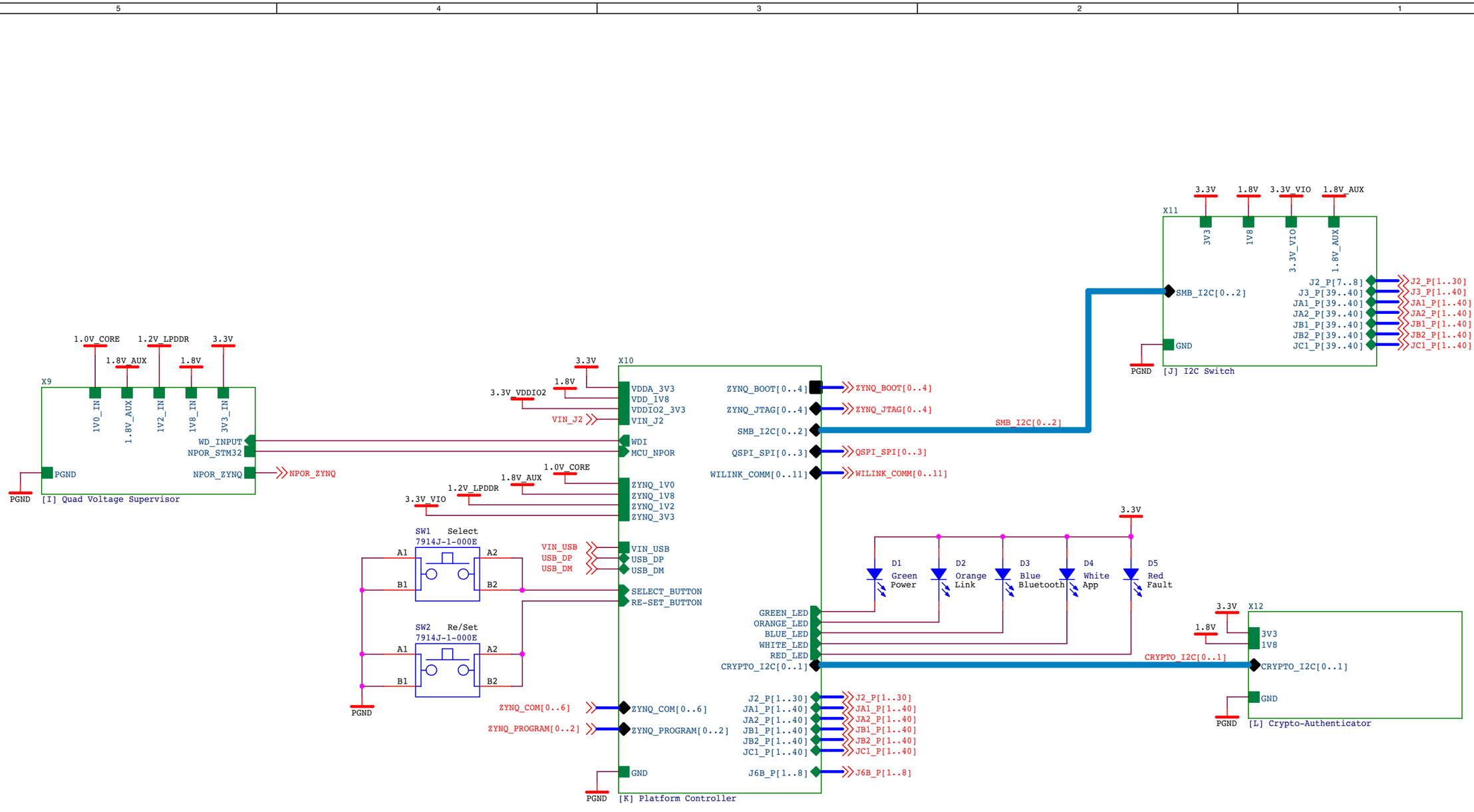
	NAME	DATE
DRAWN BY	J. Weatherbee	11/21/2015
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 3 OF 30



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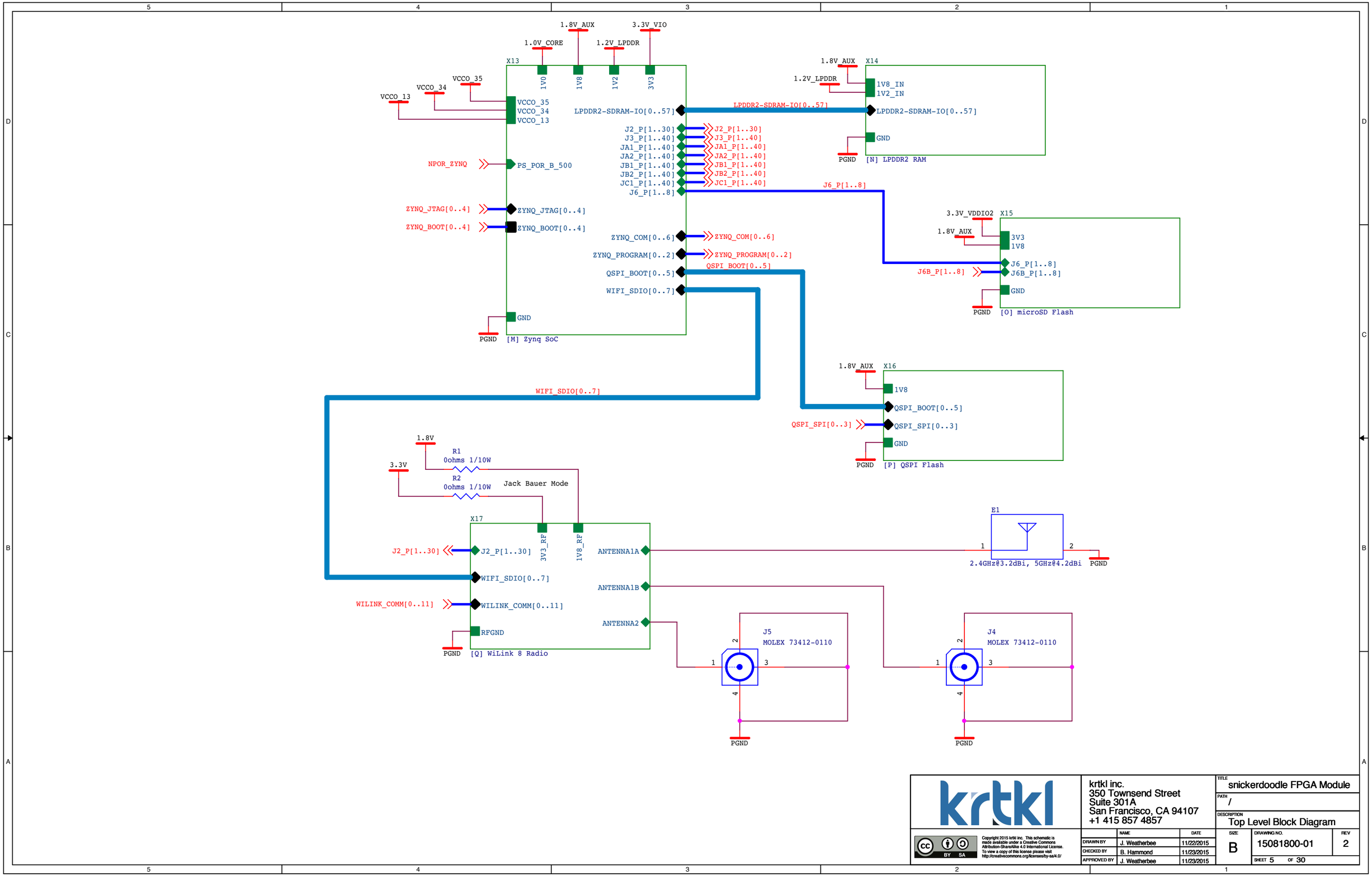
DRAWN BY	J. Weatherbee	11/22/2015
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 4 OF 30



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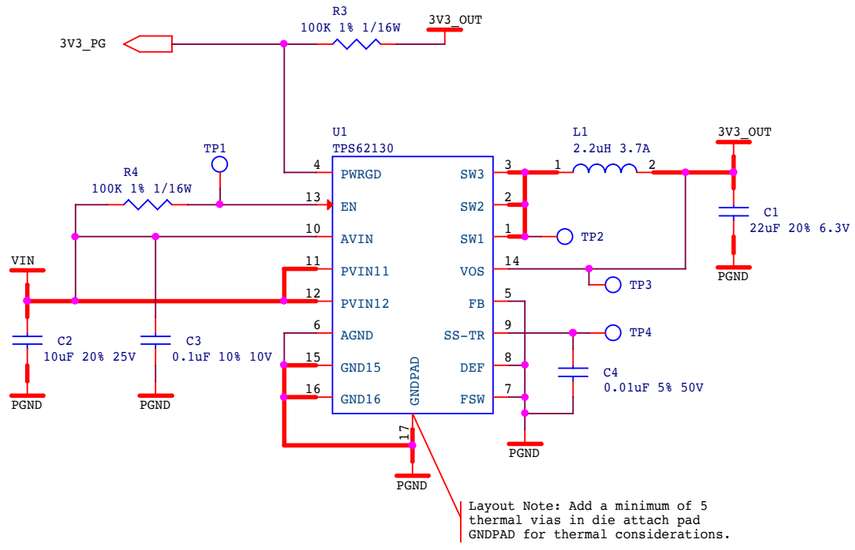
DRAWN BY	J. Weatherbee	11/22/2015
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE	snickerdoodle FPGA Module
PATH	/
DESCRIPTION	Top Level Block Diagram
SIZE	B
DRAWING NO.	15081800-01
REV	2
SHEET	5 OF 30



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DRAWN BY	B. Hammond	11/21/2015
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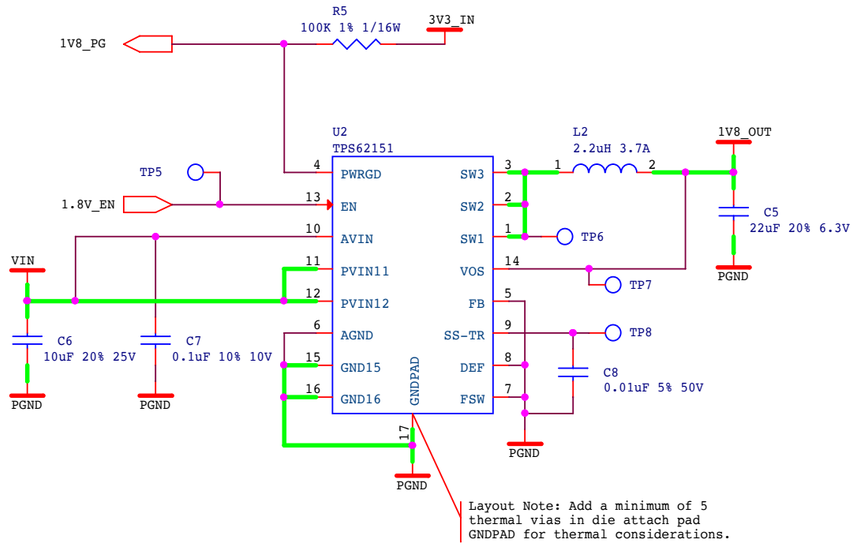
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X2
DESCRIPTION: 3.3V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 6 OF 30



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	NAME	DATE
DRAWN BY	B. Hammond	11/21/2015
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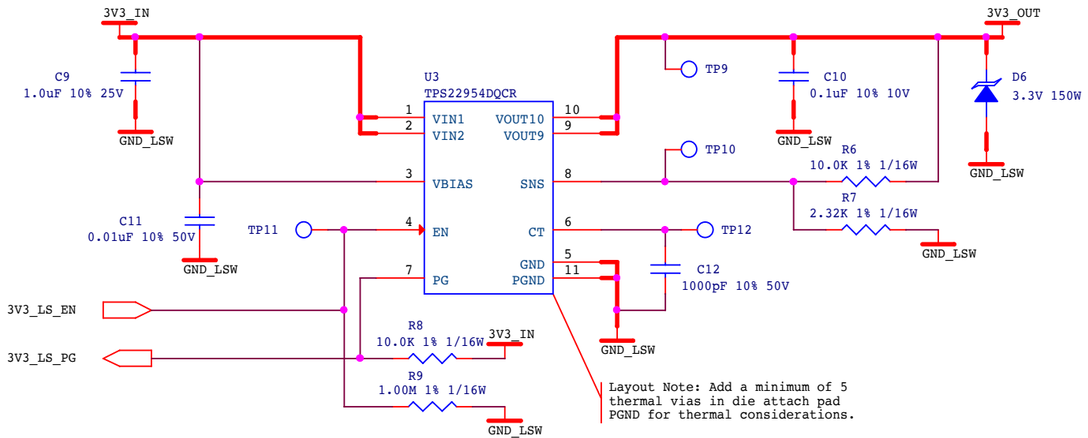
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X3
DESCRIPTION: 1.8V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 7 OF 30



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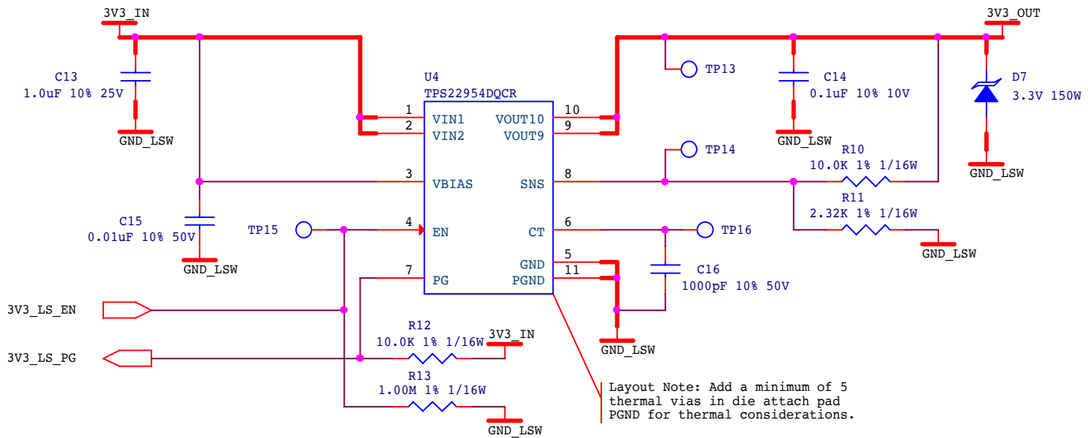
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/21/2015
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X4
DESCRIPTION: 3.3V Load Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 8 OF 30



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DRAWN BY	B. Hammond	11/21/2015
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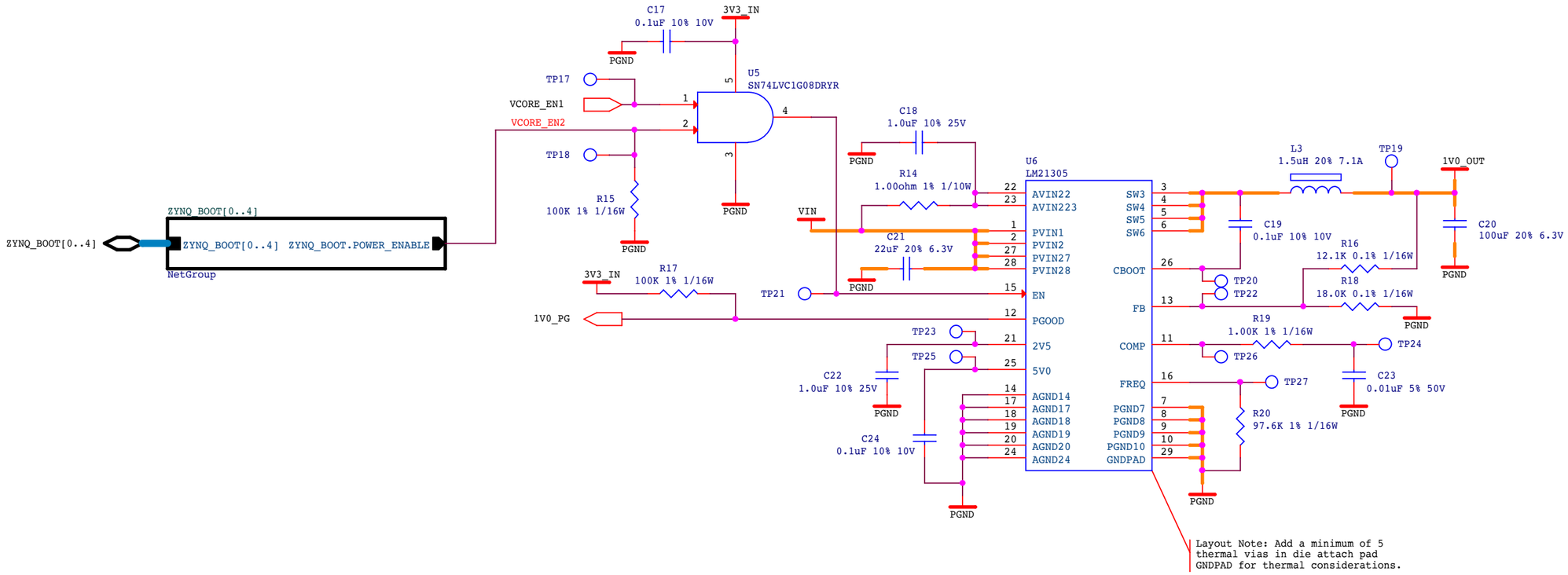
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X8
DESCRIPTION: 3.3V Load Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 9 OF 30



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DRAWN BY	B. Hammond	11/21/2015
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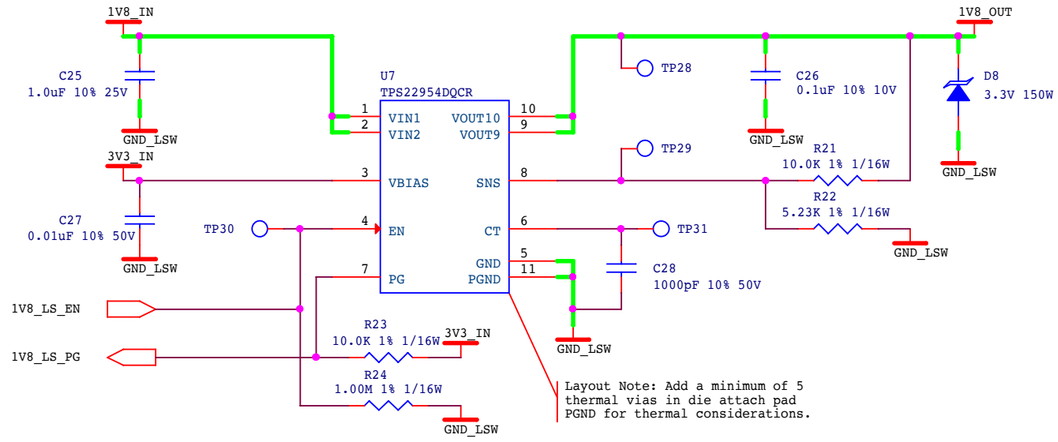
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X5
DESCRIPTION: 1.0V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 10 OF 30



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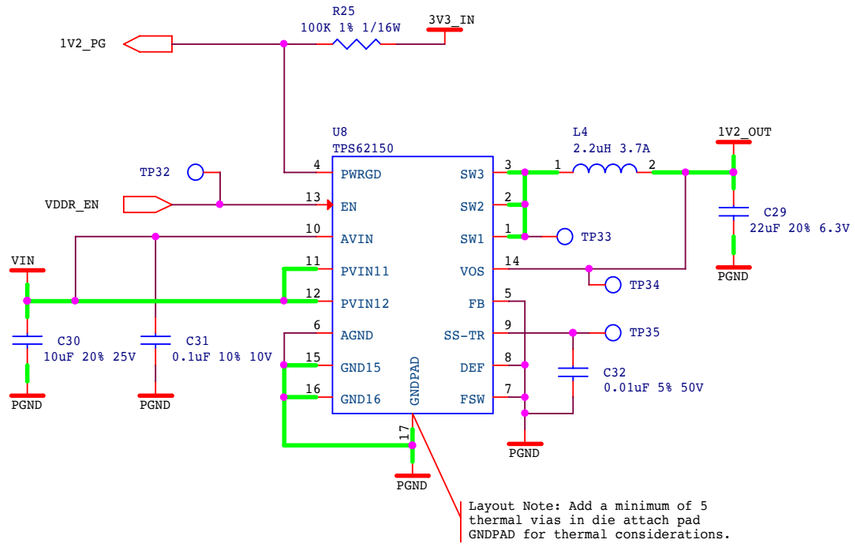
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X6
DESCRIPTION: 1.8V Load Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 11 OF 30



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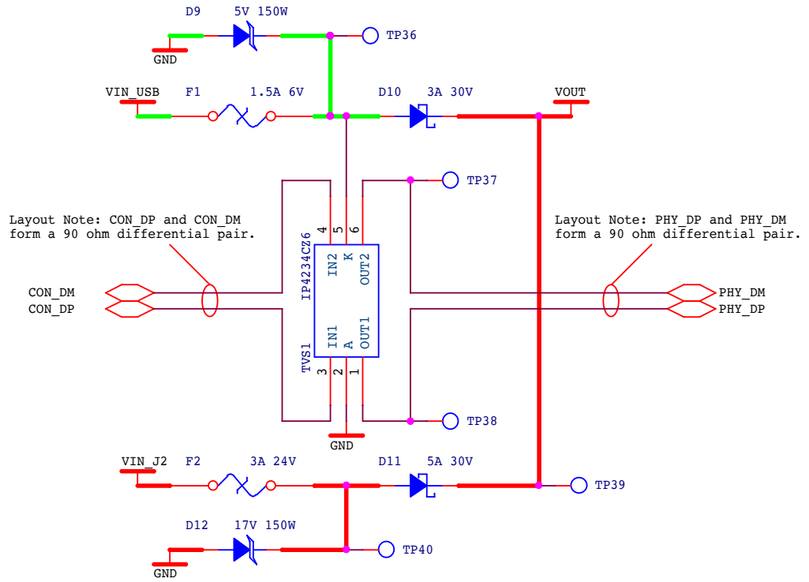
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X7
DESCRIPTION: 1.2V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 12 OF 30



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	NAME	DATE
DRAWN BY	B. Hammond	11/21/2015
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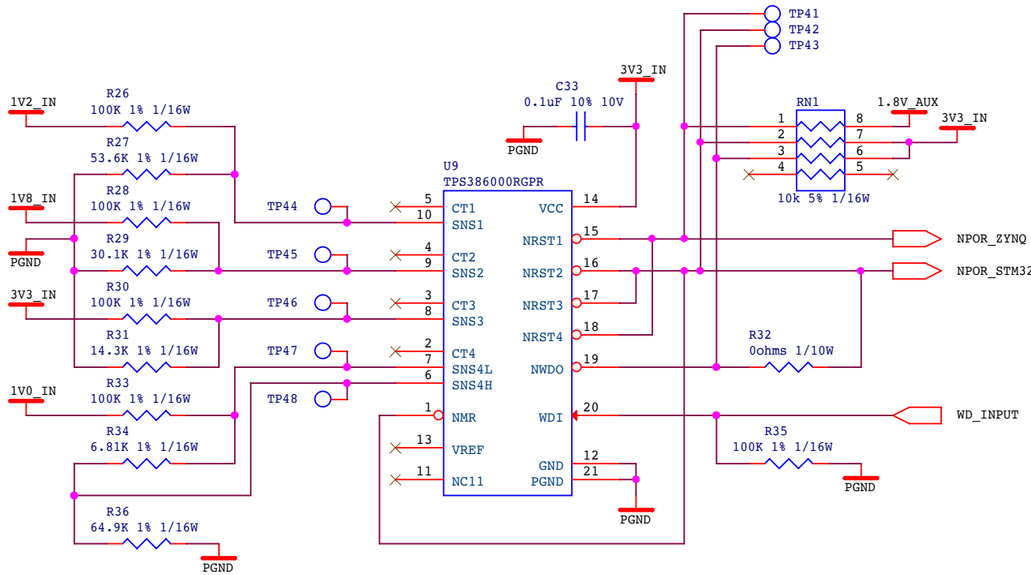
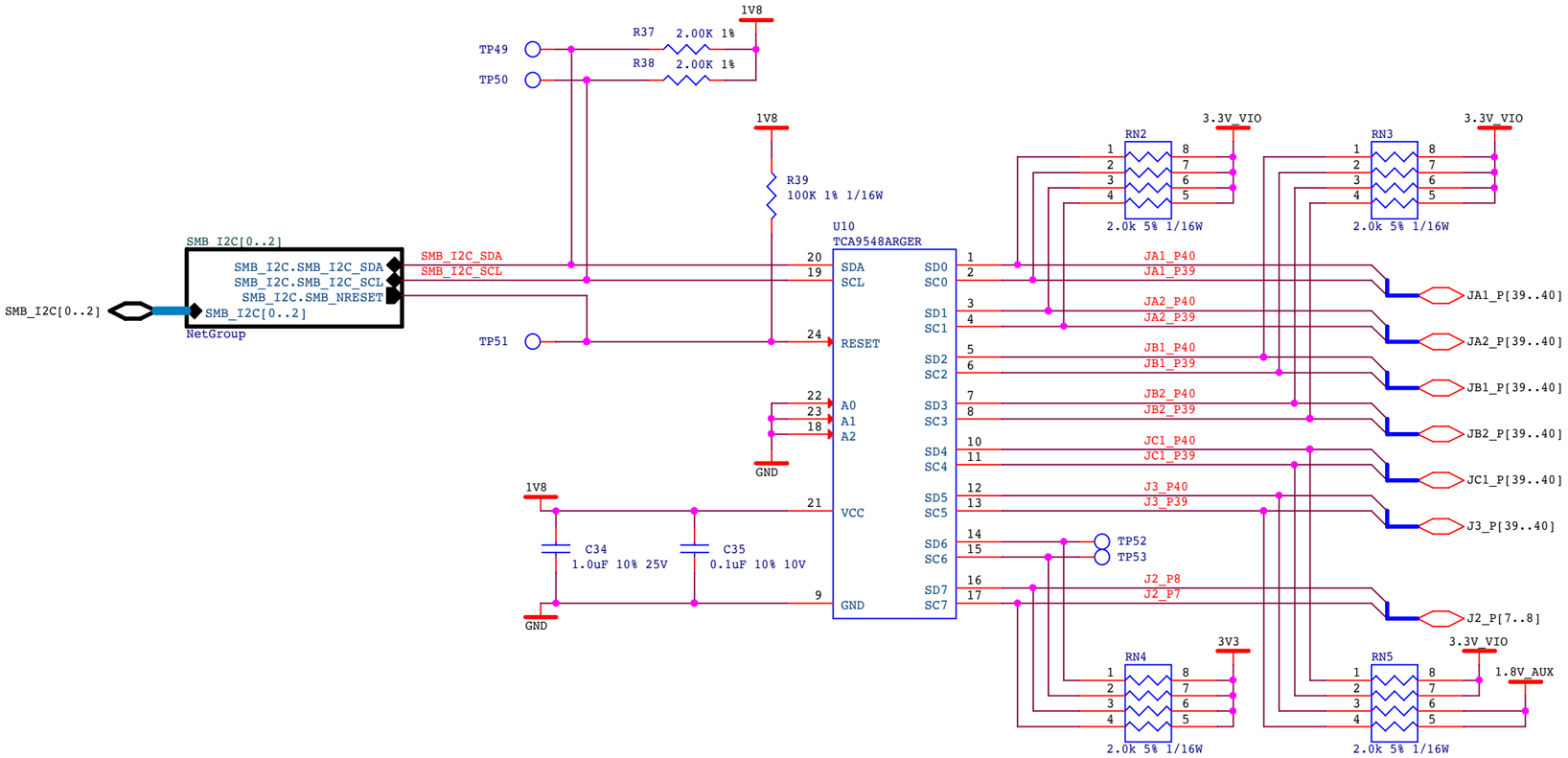
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X1
DESCRIPTION: Power Entry
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 13 OF 30



krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857	TITLE: snickerdoodle FPGA Module PATH: /X9 DESCRIPTION: Quad Voltage Supervisor	
	NAME / DATE	SIZE / DRAWING NO. / REV
DRAWN BY	B. Hammond / 11/21/2015	B / 15081800-01 / 2
CHECKED BY	J. Weatherbee / 11/23/2015	
APPROVED BY	J. Weatherbee / 11/23/2015	SHEET 14 OF 30



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DRAWN BY	B. Hammond	11/22/2015
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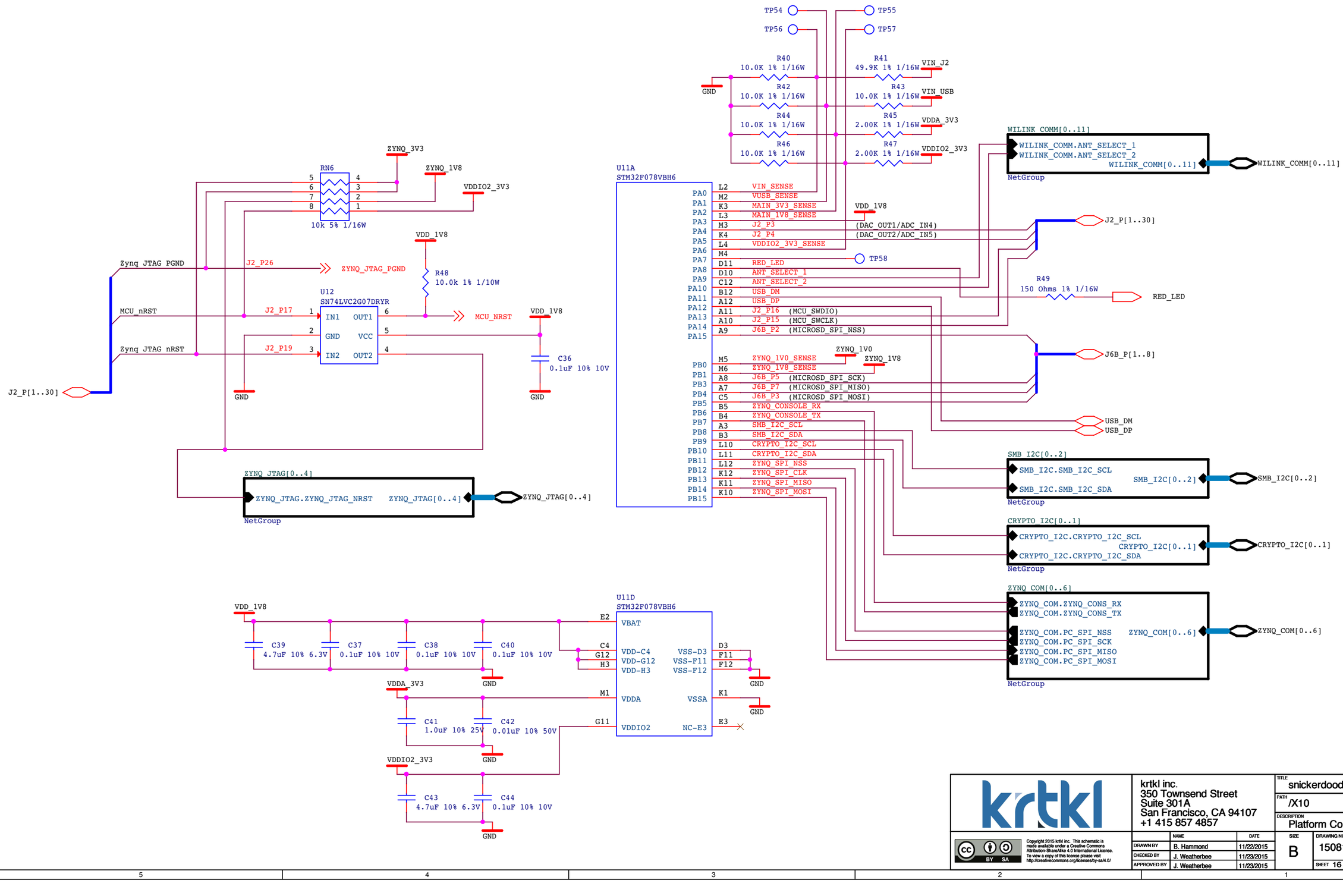
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X11
DESCRIPTION: I2C Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 15 OF 30



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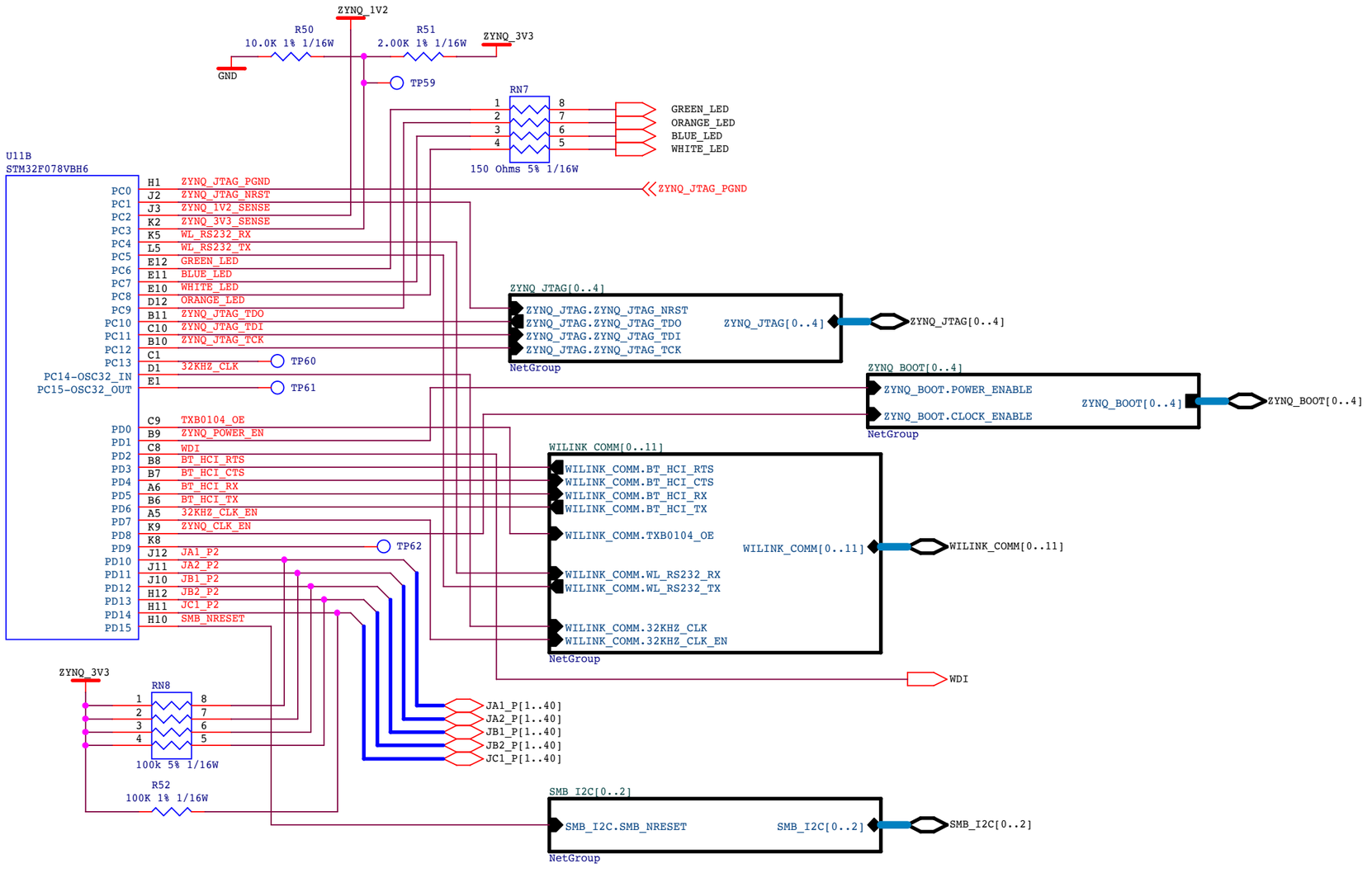
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X10
DESCRIPTION: Platform Controller
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 16 OF 30



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	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
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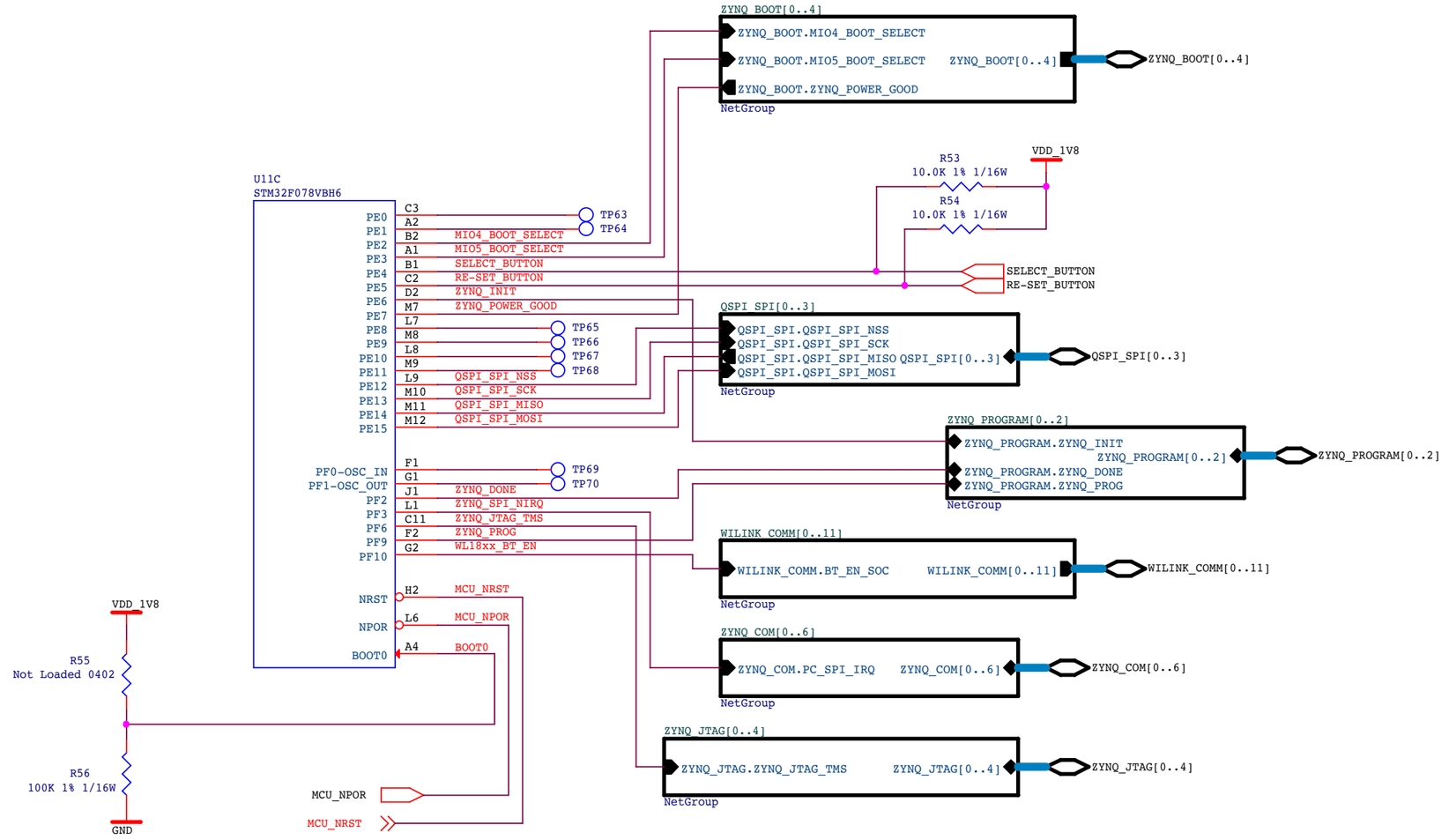
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X10
DESCRIPTION: Platform Controller
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 17 OF 30



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	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
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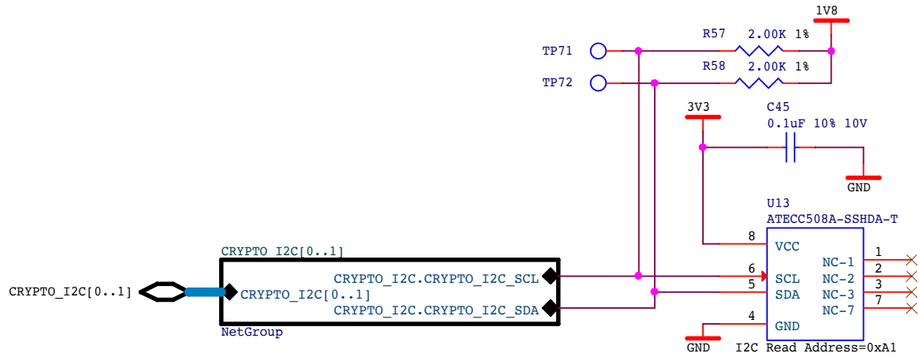
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X10
DESCRIPTION: Platform Controller
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 18 OF 30



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	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
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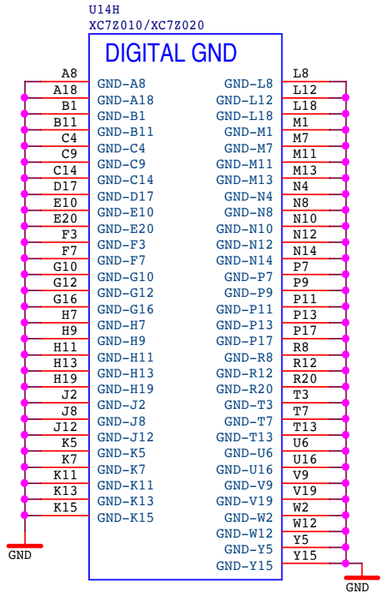
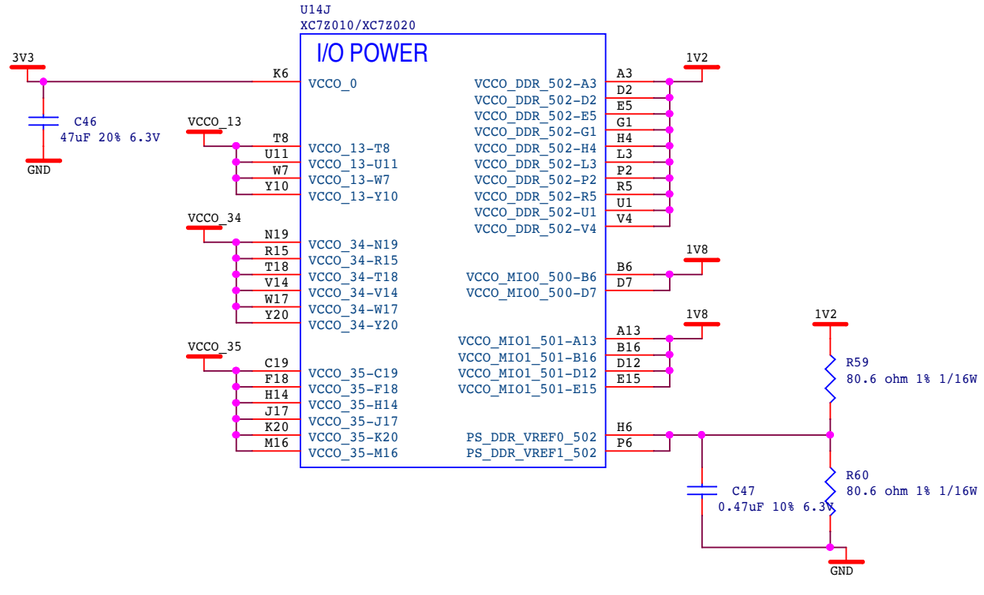
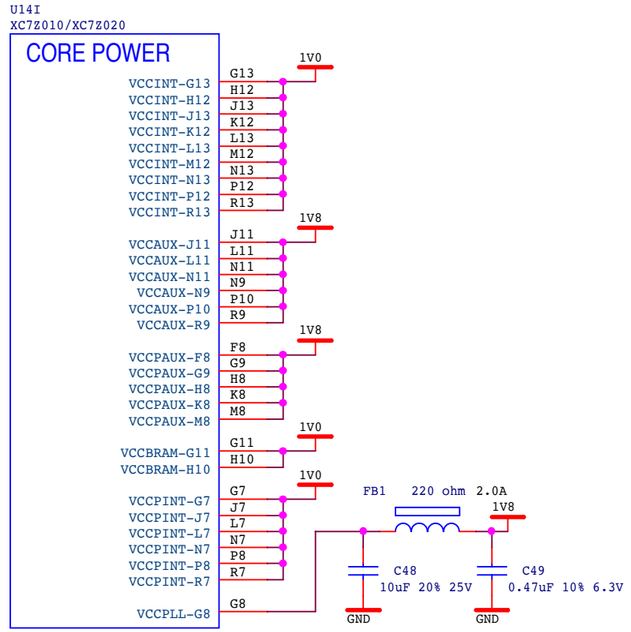
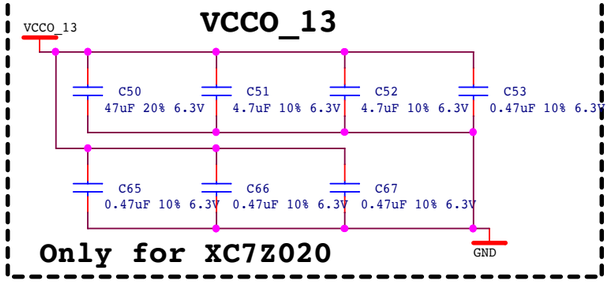
APPROVED BY	J. Weatherbee	11/23/2015

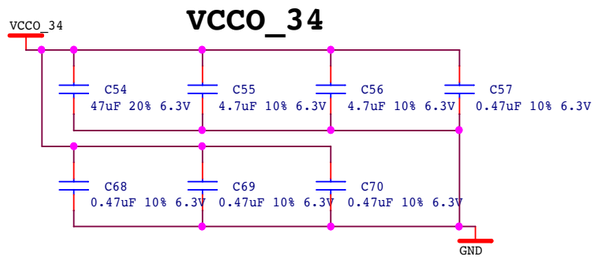
TITLE: snickerdoodle FPGA Module
PATH: /X12
DESCRIPTION: Crypto-Authenticator
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 19 OF 30

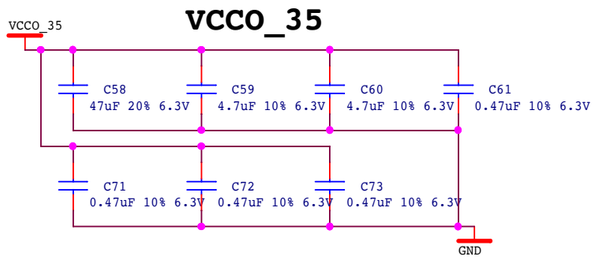


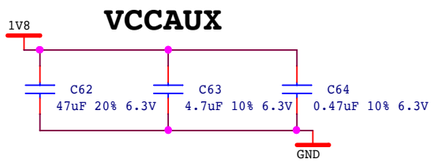


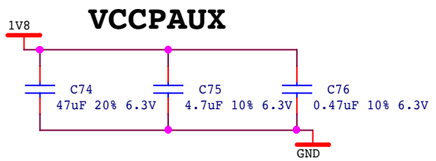


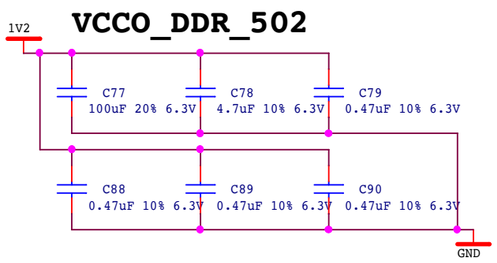


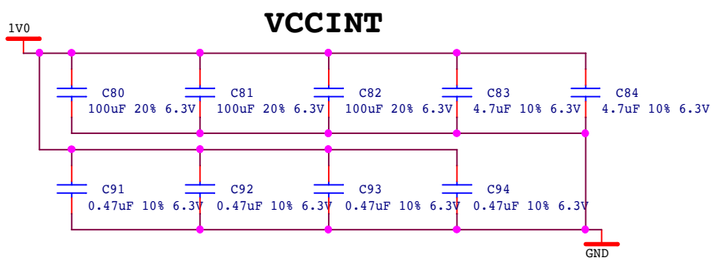


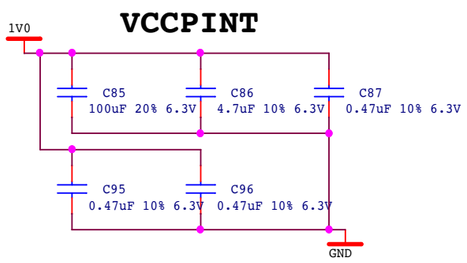


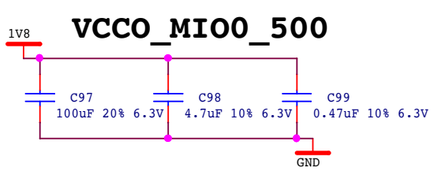


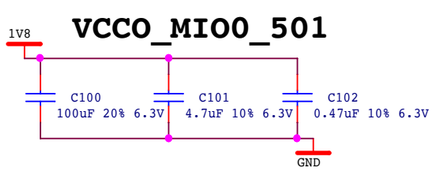


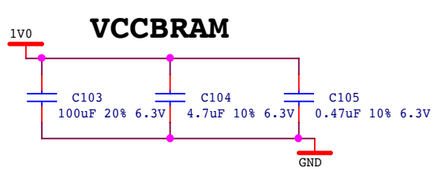












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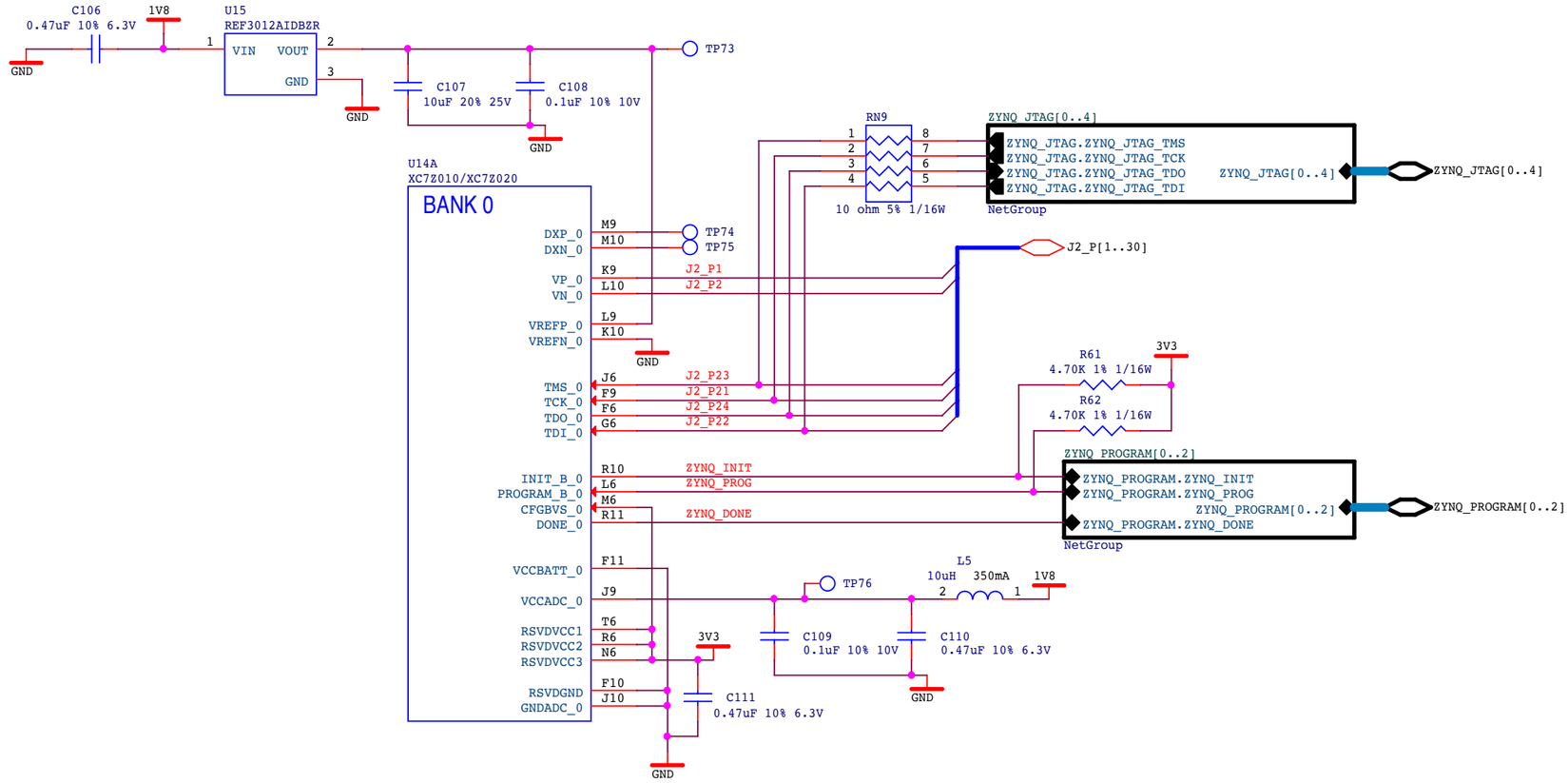
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE	snickerdoodle FPGA Module
PATH	/X13
DESCRIPTION	Zynq SoC
SIZE	B
DRAWING NO.	15081800-01
REV	2
SHEET	20 OF 30



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DRAWN BY	B. Hammond	11/22/2015
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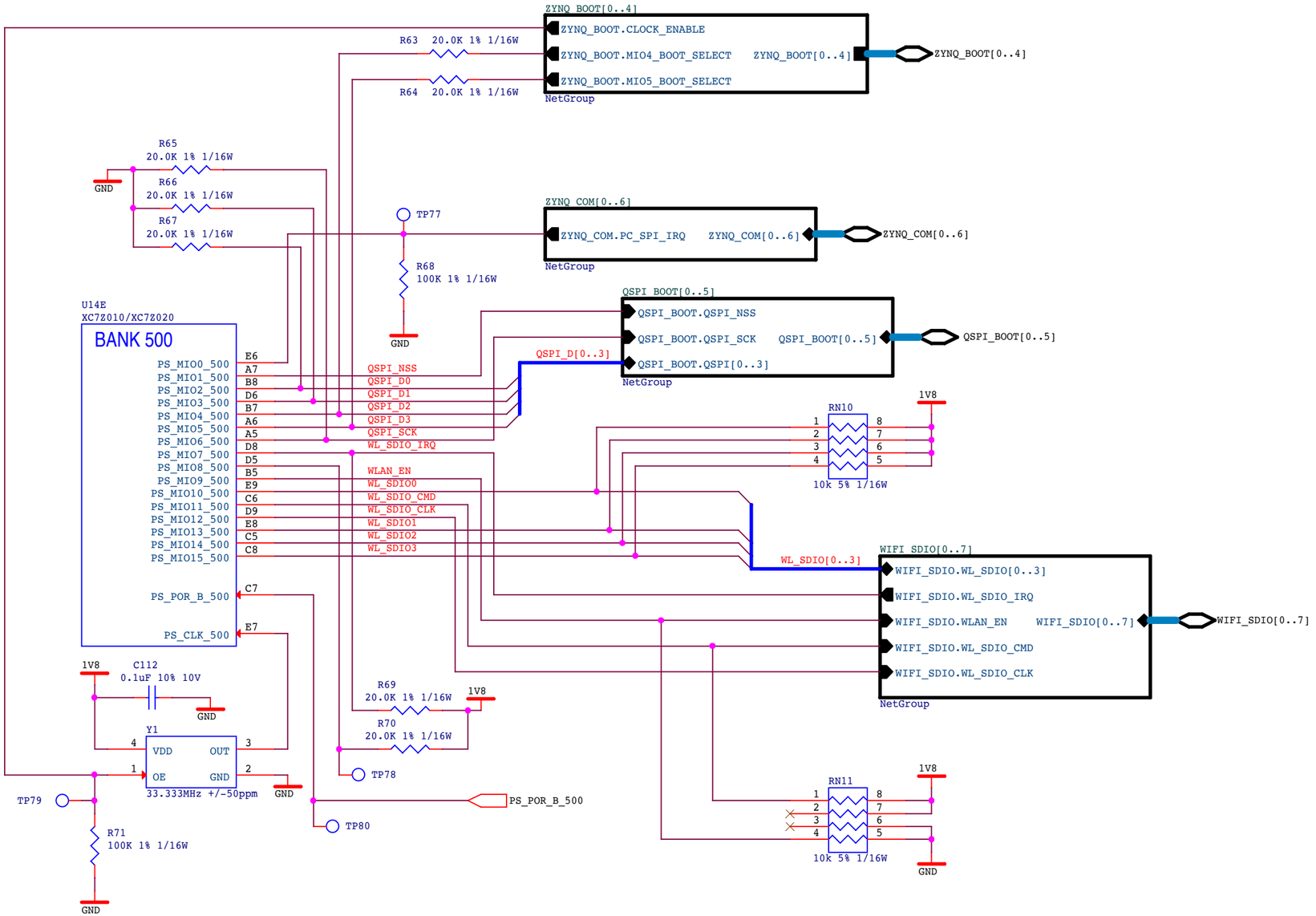
TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 21 OF 30



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	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
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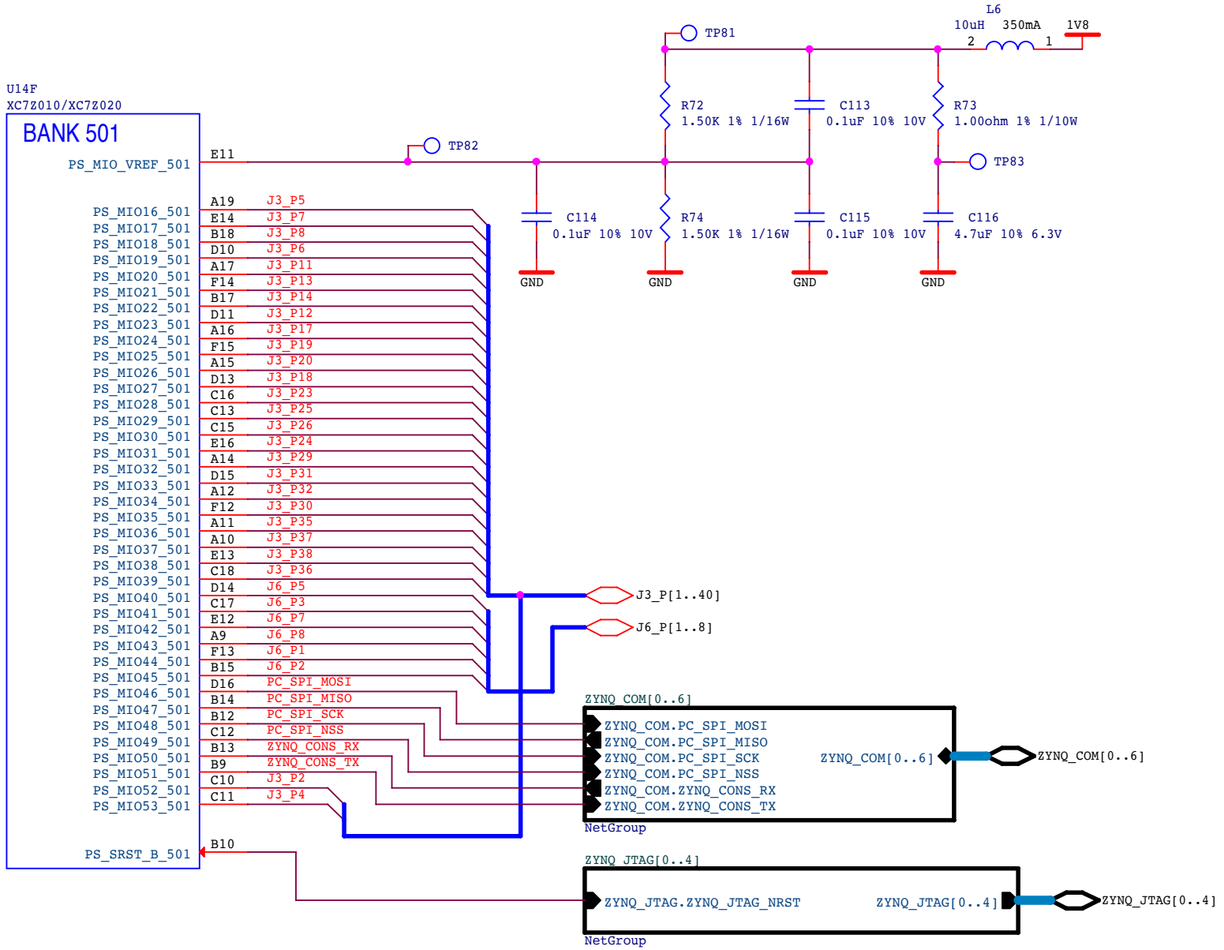
TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 22 OF 30



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TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 23 OF 30

U14G
XC7Z010/XC7Z020

BANK 502

PS_DDR_DQ0_502	C3	DQ0
PS_DDR_DQ1_502	B3	DQ1
PS_DDR_DQ2_502	A2	DQ2
PS_DDR_DQ3_502	A4	DQ3
PS_DDR_DQ4_502	D3	DQ4
PS_DDR_DQ5_502	D1	DQ5
PS_DDR_DQ6_502	C1	DQ6
PS_DDR_DQ7_502	E1	DQ7
PS_DDR_DQ8_502	E2	DQ8
PS_DDR_DQ9_502	E3	DQ9
PS_DDR_DQ10_502	G3	DQ10
PS_DDR_DQ11_502	H3	DQ11
PS_DDR_DQ12_502	J3	DQ12
PS_DDR_DQ13_502	H2	DQ13
PS_DDR_DQ14_502	H1	DQ14
PS_DDR_DQ15_502	J1	DQ15
PS_DDR_DQ16_502	P1	DQ16
PS_DDR_DQ17_502	P3	DQ17
PS_DDR_DQ18_502	R3	DQ18
PS_DDR_DQ19_502	R1	DQ19
PS_DDR_DQ20_502	T4	DQ20
PS_DDR_DQ21_502	U4	DQ21
PS_DDR_DQ22_502	U2	DQ22
PS_DDR_DQ23_502	U3	DQ23
PS_DDR_DQ24_502	V1	DQ24
PS_DDR_DQ25_502	Y3	DQ25
PS_DDR_DQ26_502	W1	DQ26
PS_DDR_DQ27_502	Y4	DQ27
PS_DDR_DQ28_502	Y2	DQ28
PS_DDR_DQ29_502	W3	DQ29
PS_DDR_DQ30_502	V2	DQ30
PS_DDR_DQ31_502	V3	DQ31
PS_DDR_A0_502	N2	A0
PS_DDR_A1_502	K2	A1
PS_DDR_A2_502	M3	A2
PS_DDR_A3_502	K3	A3
PS_DDR_A4_502	M4	A4
PS_DDR_A5_502	L1	A5
PS_DDR_A6_502	L4	A6
PS_DDR_A7_502	K4	A7
PS_DDR_A8_502	K1	A8
PS_DDR_A9_502	J4	A9
PS_DDR_A10_502	F5	
PS_DDR_A11_502	G4	
PS_DDR_A12_502	E4	
PS_DDR_A13_502	D4	
PS_DDR_A14_502	F4	
PS_DDR_DQS_P0_502	C2	DQS_P0
PS_DDR_DQS_N0_502	B2	DQS_N0
PS_DDR_DQS_P1_502	G2	DQS_P1
PS_DDR_DQS_N1_502	F2	DQS_N1
PS_DDR_DQS_P2_502	R2	DQS_P2
PS_DDR_DQS_N2_502	T2	DQS_N2
PS_DDR_DQS_P3_502	W5	DQS_P3
PS_DDR_DQS_N3_502	W4	DQS_N3
PS_DDR_CKP_502	L2	CKP
PS_DDR_CKN_502	M2	CKN
PS_DDR_BA0_502	L5	
PS_DDR_BA1_502	R4	
PS_DDR_BA2_502	J5	
PS_DDR_DM0_502	A1	DM0
PS_DDR_DM1_502	F1	DM1
PS_DDR_DM2_502	T1	DM2
PS_DDR_DM3_502	Y1	DM3
PS_DDR_CS_B_502	N1	CS_B
PS_DDR_WE_B_502	M5	
PS_DDR_CAS_B_502	P5	
PS_DDR_RAS_B_502	P4	
PS_DDR_CKE_502	N3	CKE
PS_DDR_ODT_502	N5	
PS_DDR_DRST_B_502	B4	
PS_DDR_VRP_502	H5	
PS_DDR_VRN_502	G5	

Match all signal trace lengths for DQ groups with a max deviation of ±50 mils and route on the same layer.

Route address and command signals on a different layer than the data and data mask signals.

DQ[0..31]
A[0..9]
DQS_P[0..3]
DQS_N[0..3]
DM[0..3]

LPDDR2-SDRAM-IO[0..57]
- LPDDR2-SDRAM-IO.DQ[0..31]
- LPDDR2-SDRAM-IO.A[0..9]
- LPDDR2-SDRAM-IO.DQS_P[0..3]
- LPDDR2-SDRAM-IO.DQS_N[0..3]
- LPDDR2-SDRAM-IO.DM[0..3]
- LPDDR2-SDRAM-IO.CS_B
- LPDDR2-SDRAM-IO.CKE
- LPDDR2-SDRAM-IO.CKP
- LPDDR2-SDRAM-IO.CKN

NetGroup

LPDDR2-SDRAM-IO[0..57]

Route clock on inner layers with outer-layer run lengths held to under 500 mils and maintain a 10-mil spacing from other nets. Length match clock traces within ±25 mils, with CKP and CKN traces matched within ±10 mils. Do not route CKP/CKN pair and CKE close to address signals.

Route address and command signals on a different layer than the data and data mask signals.

R75
40.2 Ohms 1% 1/16W
R76
40.2 Ohms 1% 1/16W
1V2
GND

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	NAME	DATE
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APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 24 OF 30

U14D
XC7Z010/XC7Z020

BANK 35

IO_0_35	G14	JA1_P4
IO_L1P_T0_AD0P_35	C20	JA1_P14
IO_L1N_T0_AD0N_35	B20	JA1_P12
IO_L2P_T0_AD8P_35	B19	JA1_P20
IO_L2N_T0_AD8N_35	A20	JA1_P18
IO_L3P_T0_DQS_AD1P_35	E17	JA1_P17
IO_L3N_T0_DQS_AD1N_35	D18	JA1_P19
IO_L4P_T0_35	D19	JA1_P8
IO_L4N_T0_35	D20	JA1_P6
IO_L5P_T0_AD9P_35	E18	JA1_P5
IO_L5N_T0_AD9N_35	E19	JA1_P7
IO_L6P_T0_35	F16	JA1_P11
IO_L6N_T0_VREF_35	F17	JA1_P13
IO_L7P_T1_AD2P_35	M19	JA2_P32
IO_L7N_T1_AD2N_35	M20	JA2_P30
IO_L8P_T1_AD10P_35	M17	JA2_P29
IO_L8N_T1_AD10N_35	M18	JA2_P31
IO_L9P_T1_DQS_AD3P_35	L19	JA2_P23
IO_L9N_T1_DQS_AD3N_35	L20	JA2_P25
IO_L10P_T1_AD11P_35	K19	JA2_P26
IO_L10N_T1_AD11N_35	J19	JA2_P24
IO_L11P_T1_SRCC_35	L16	JA2_P35
IO_L11N_T1_SRCC_35	L17	JA2_P37
IO_L12P_T1_MRCC_35	K17	JA2_P38
IO_L12N_T1_MRCC_35	K18	JA2_P36
IO_L13P_T2_MRCC_35	H16	JA1_P38
IO_L13N_T2_MRCC_35	H17	JA1_P36
IO_L14P_T2_AD4P_SRCC_35	J18	JA1_P35
IO_L14N_T2_AD4N_SRCC_35	H18	JA1_P37
IO_L15P_T2_DQS_AD12P_35	F19	JA1_P23
IO_L15N_T2_DQS_AD12N_35	F20	JA1_P25
IO_L16P_T2_35	G17	JA1_P32
IO_L16N_T2_35	G18	JA1_P30
IO_L17P_T2_AD5P_35	J20	JA1_P29
IO_L17N_T2_AD5N_35	H20	JA1_P31
IO_L18P_T2_AD13P_35	G19	JA1_P26
IO_L18N_T2_AD13N_35	G20	JA1_P24
IO_L19P_T3_35	H15	JA2_P14
IO_L19N_T3_VREF_35	G15	JA2_P12
IO_L20P_T3_AD6P_35	K14	JA2_P20
IO_L20N_T3_AD6N_35	J14	JA2_P18
IO_L21P_T3_DQS_AD14P_35	N15	JA2_P17
IO_L21N_T3_DQS_AD14N_35	N16	JA2_P19
IO_L22P_T3_AD7P_35	L14	JA2_P5
IO_L22N_T3_AD7N_35	L15	JA2_P7
IO_L23P_T3_35	M14	JA2_P11
IO_L23N_T3_35	M15	JA2_P13
IO_L24P_T3_AD15P_35	K16	JA2_P8
IO_L24N_T3_AD15N_35	J16	JA2_P6
IO_25_35	J15	JA2_P4

JA1_P[1..40]

JA2_P[1..40]

U14C
XC7Z010/XC7Z020

BANK 34

IO_0_34	R19	JB2_P4
IO_L1P_T0_34	T11	JB1_P5
IO_L1N_T0_34	T10	JB1_P7
IO_L2P_T0_34	T12	JB1_P8
IO_L2N_T0_34	U12	JB1_P6
IO_L3P_T0_DQS_PUDC_B_34	U13	JB1_P17
IO_L3N_T0_DQS_34	V13	JB1_P19
IO_L4P_T0_34	V12	JB1_P14
IO_L4N_T0_34	W13	JB1_P12
IO_L5P_T0_34	T14	JB1_P20
IO_L5N_T0_34	T15	JB1_P18
IO_L6P_T0_34	P14	JB1_P11
IO_L6N_T0_VREF_34	R14	JB1_P13
IO_L7P_T1_34	Y16	JB1_P26
IO_L7N_T1_34	Y17	JB1_P24
IO_L8P_T1_34	W14	JB1_P29
IO_L8N_T1_34	Y14	JB1_P31
IO_L9P_T1_DQS_34	T16	JB1_P23
IO_L9N_T1_DQS_34	U17	JB1_P25
IO_L10P_T1_34	V15	JB1_P32
IO_L10N_T1_34	W15	JB1_P30
IO_L11P_T1_SRCC_34	U14	JB1_P35
IO_L11N_T1_SRCC_34	U15	JB1_P37
IO_L12P_T1_MRCC_34	U18	JB1_P38
IO_L12N_T1_MRCC_34	U19	JB1_P36
IO_L13P_T2_MRCC_34	N18	JB2_P38
IO_L13N_T2_MRCC_34	P19	JB2_P36
IO_L14P_T2_SRCC_34	N20	JB2_P35
IO_L14N_T2_SRCC_34	P20	JB2_P37
IO_L15P_T2_DQS_34	T20	JB2_P23
IO_L15N_T2_DQS_34	U20	JB2_P25
IO_L16P_T2_34	V20	JB2_P29
IO_L16N_T2_34	W20	JB2_P31
IO_L17P_T2_34	Y18	JB2_P32
IO_L17N_T2_34	Y19	JB2_P30
IO_L18P_T2_34	V16	JB2_P26
IO_L18N_T2_34	W16	JB2_P24
IO_L19P_T3_34	R16	JB2_P14
IO_L19N_T3_VREF_34	R17	JB2_P12
IO_L20P_T3_34	T17	JB2_P11
IO_L20N_T3_34	R18	JB2_P13
IO_L21P_T3_DQS_34	V17	JB2_P17
IO_L21N_T3_DQS_34	V18	JB2_P19
IO_L22P_T3_34	W18	JB2_P20
IO_L22N_T3_34	W19	JB2_P18
IO_L23P_T3_34	N17	JB2_P5
IO_L23N_T3_34	P18	JB2_P7
IO_L24P_T3_34	P15	JB2_P8
IO_L24N_T3_34	P16	JB2_P6
IO_25_34	T19	JB1_P4

JB1_P[1..40]

JB2_P[1..40]

U14B
XC7Z010/XC7Z020

BANK 13

IO_L6N_T0_VREF_13	V5	JC1_P4
IO_L11P_T1_SRCC_13	U7	JC1_P5
IO_L11N_T1_SRCC_13	V7	JC1_P7
IO_L12P_T1_MRCC_13	T9	JC1_P8
IO_L12N_T1_MRCC_13	U10	JC1_P6
IO_L13P_T2_MRCC_13	Y7	JC1_P38
IO_L13N_T2_MRCC_13	Y6	JC1_P36
IO_L14P_T2_SRCC_13	Y9	JC1_P35
IO_L14N_T2_SRCC_13	Y8	JC1_P37
IO_L15P_T2_DQS_13	V8	JC1_P23
IO_L15N_T2_DQS_13	W8	JC1_P25
IO_L16P_T2_13	W10	JC1_P32
IO_L16N_T2_13	W9	JC1_P30
IO_L17P_T2_13	U9	JC1_P29
IO_L17N_T2_13	U8	JC1_P31
IO_L18P_T2_13	W11	JC1_P26
IO_L18N_T2_13	Y11	JC1_P24
IO_L19P_T3_13	T5	JC1_P11
IO_L19N_T3_VREF_13	U5	JC1_P13
IO_L20P_T3_13	Y12	JC1_P14
IO_L20N_T3_13	Y13	JC1_P12
IO_L21P_T3_DQS_13	V11	JC1_P17
IO_L21N_T3_DQS_13	V10	JC1_P19
IO_L22P_T3_13	V6	JC1_P20
IO_L22N_T3_13	W6	JC1_P18

JC1_P[1..40]

Only for XC7Z020

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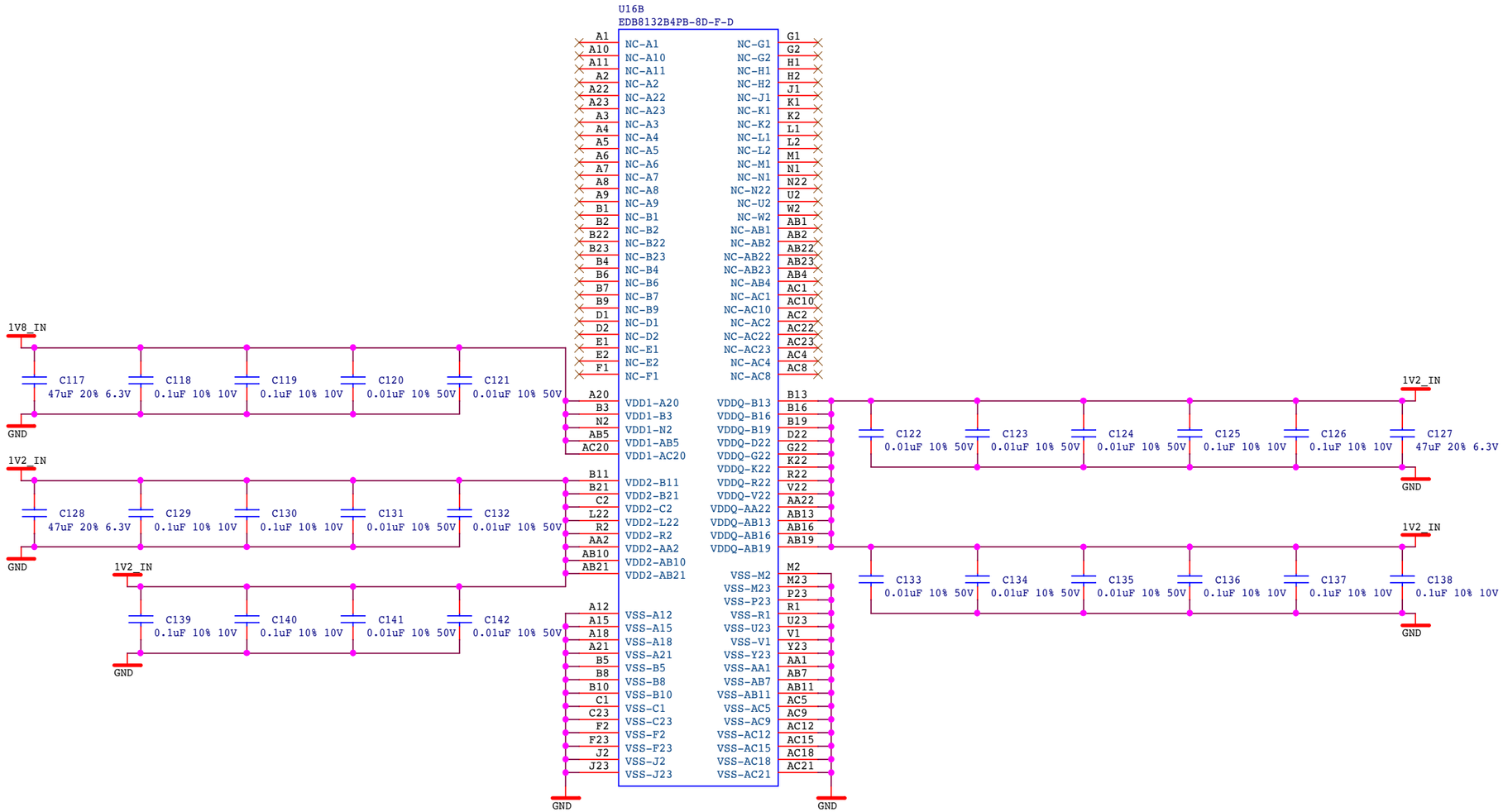
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 25 OF 30



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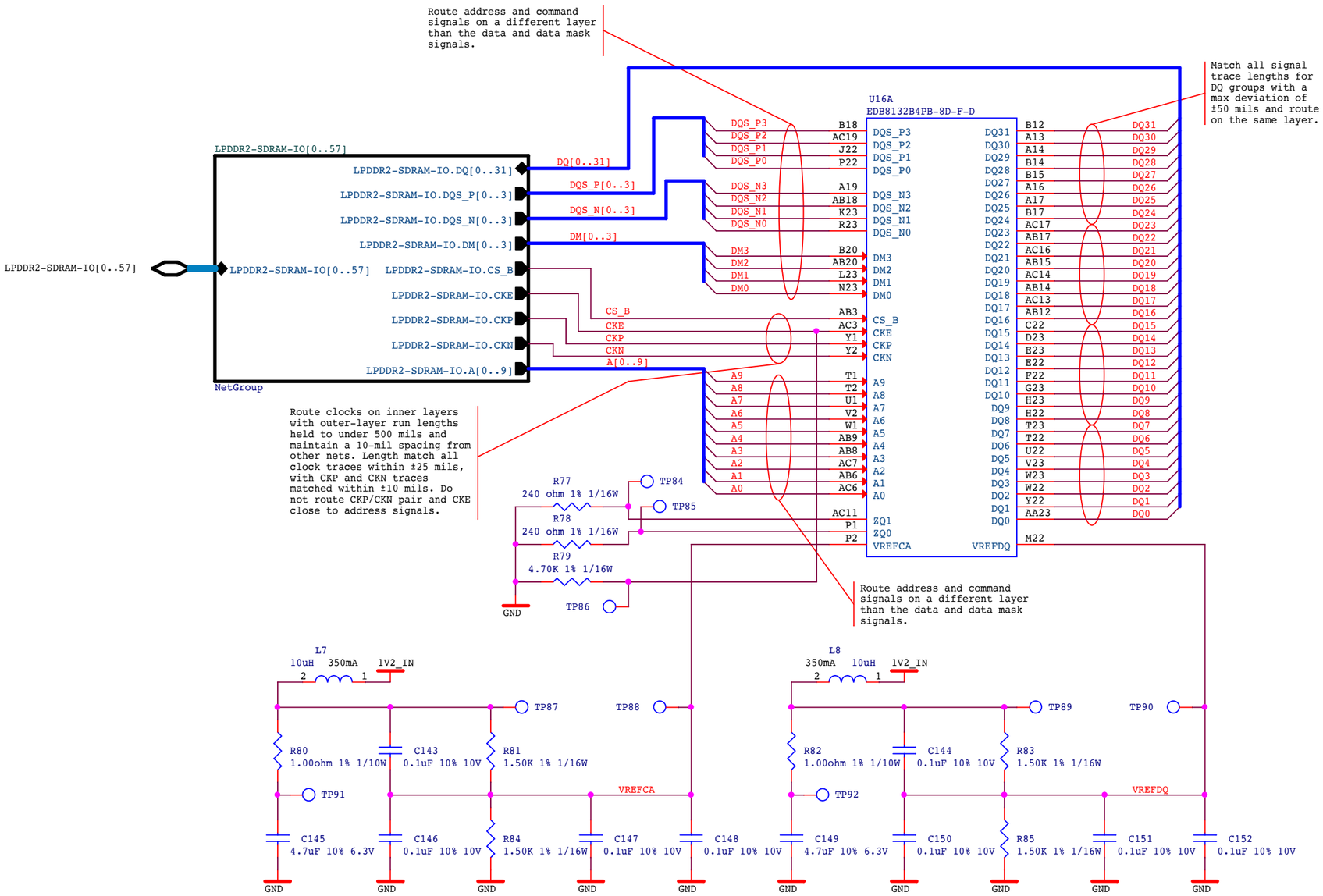
TITLE: snickerdoodle FPGA Module
PATH: /X14
DESCRIPTION: LPDDR2 RAM
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 26 OF 30



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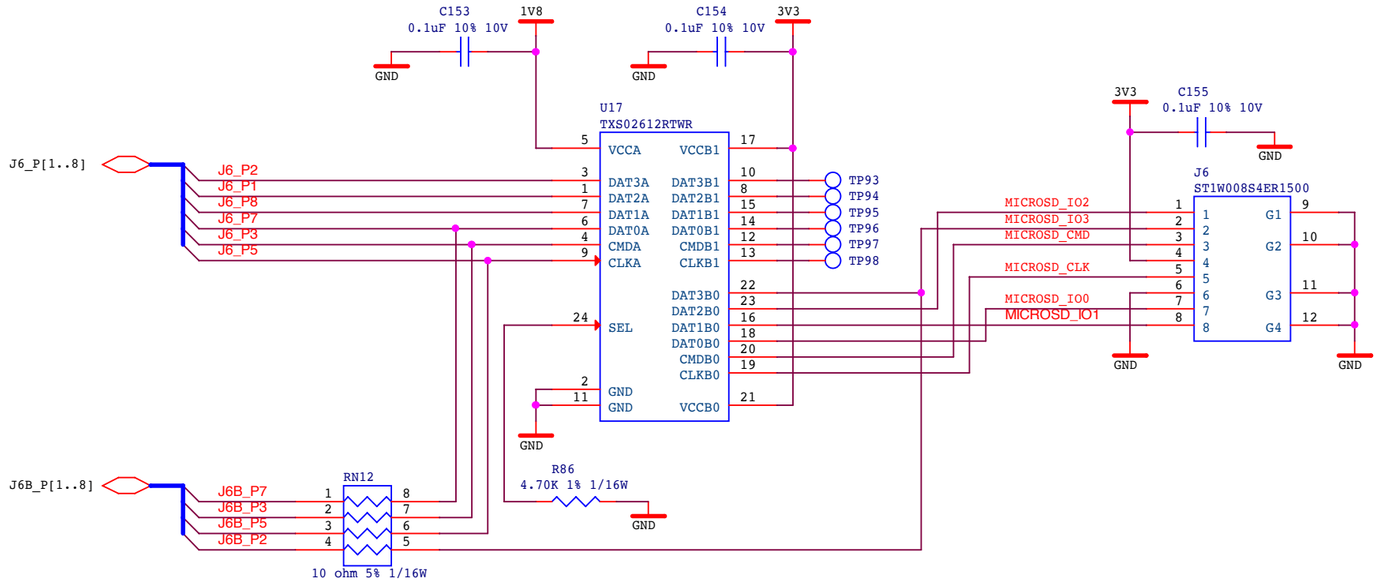
TITLE: snickerdoodle FPGA Module
PATH: /X14
DESCRIPTION: LPDDR2 RAM
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 27 OF 30



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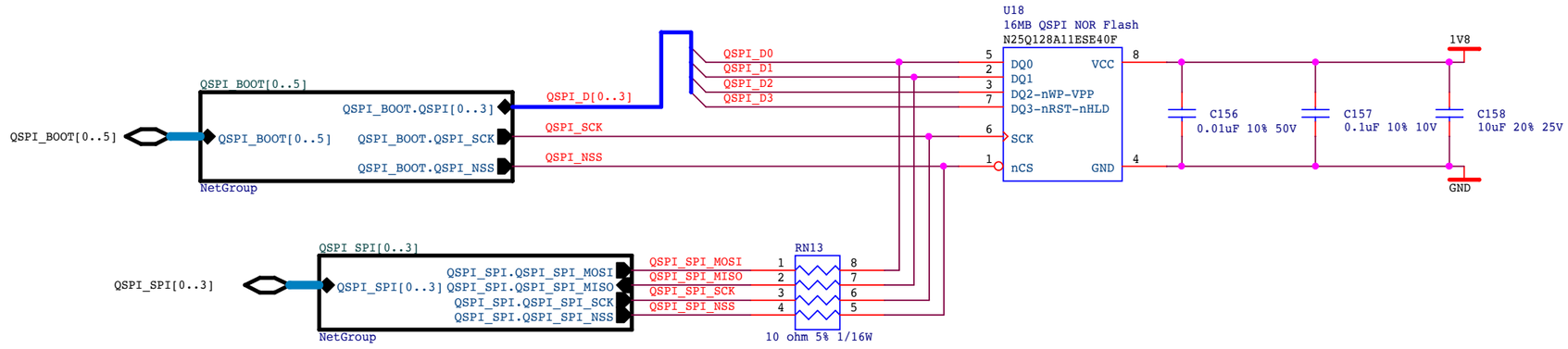
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/21/2015
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X15
DESCRIPTION: microSD Flash
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 28 OF 30



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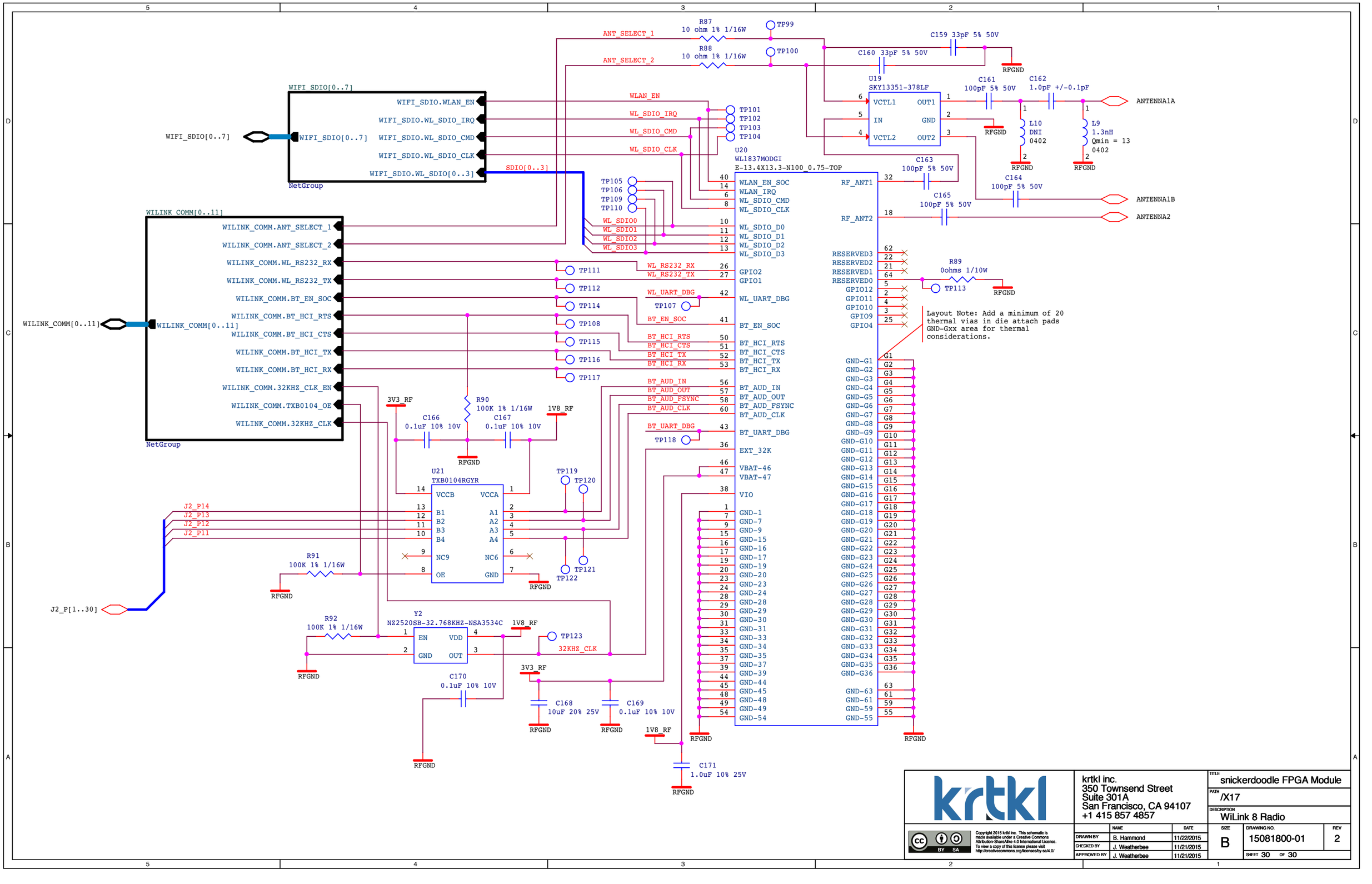
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/21/2015
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X16
DESCRIPTION: QSPI Flash
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 29 OF 30



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	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/21/2015
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X17
DESCRIPTION: WiLink 8 Radio
SIZE: B
DRAWING NO.: 15081800-01
REV: 2
SHEET 30 OF 30