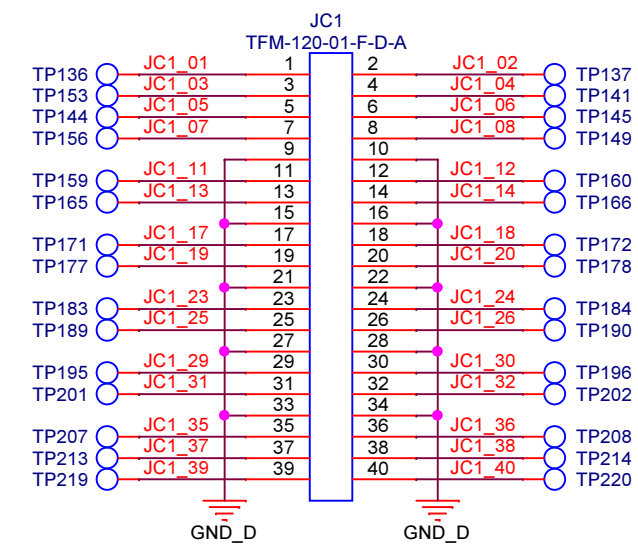
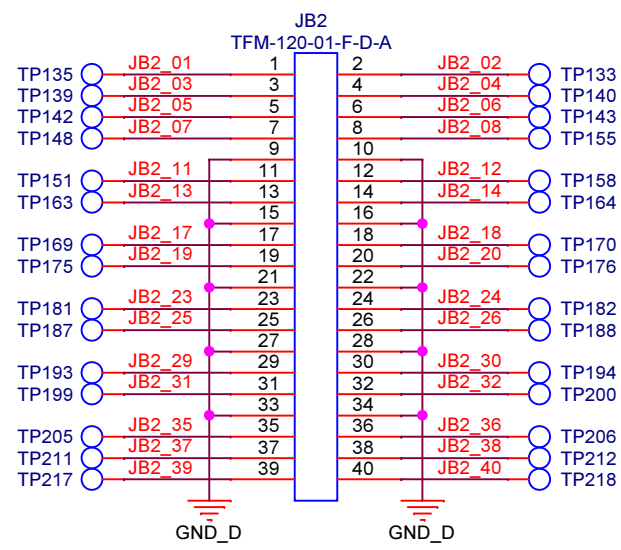
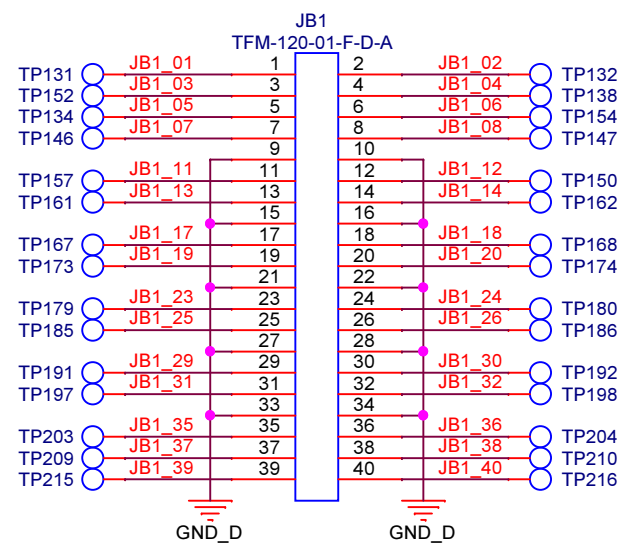
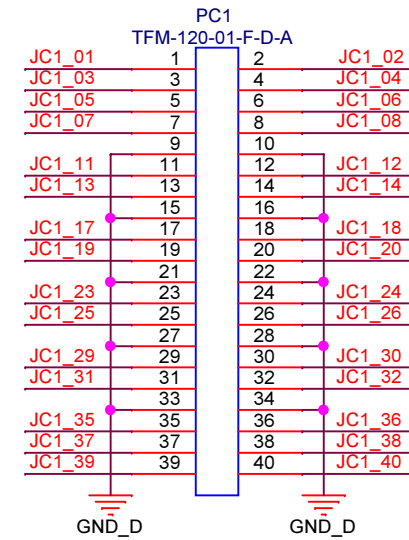
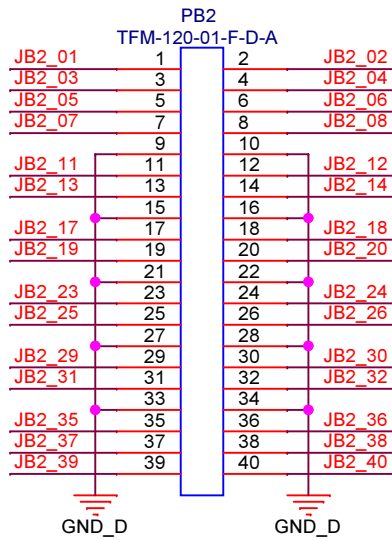
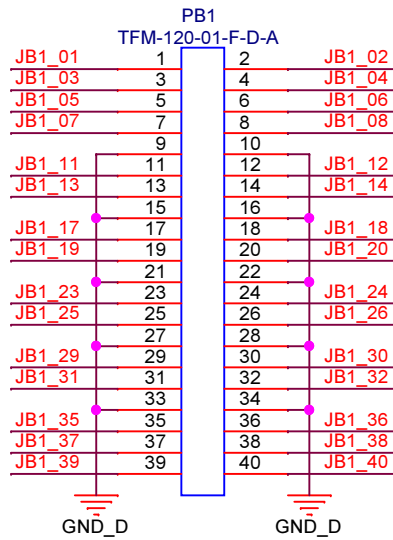


NOTES:  
 1 Place decoupling capacitors as close to IC pins as possible.

		krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857		TITLE <b>giggleBit</b>	
		PATH /		DESCRIPTION <b>Main Interconnect</b>	
DRAWN BY <b>B. Hammond</b>		DATE <b>10/16/2015</b>		SIZE <b>B</b>	
CHECKED BY <b>J. Weatherbee</b>		DATE <b>10/23/2015</b>		DRAWING NO. <b>15101401-01</b>	
APPROVED BY <b>R. Cousins</b>		DATE <b>10/23/2015</b>		REV <b>1.1</b>	
				SHEET 2 OF 6	

Copyright 2015 krtkl inc. This schematic is made available under a Creative Commons Attribution-ShareAlike 4.0 International License. To view a copy of this license please visit <http://creativecommons.org/licenses/by-sa/4.0/>



NOTES:



krtkl inc.  
350 Townsend Street  
Suite 301A  
San Francisco, CA 94107  
+1 415 857 4857

Copyright 2015 krtkl inc. This schematic is made available under a Creative Commons Attribution-ShareAlike 4.0 International License. To view a copy of this license please visit <http://creativecommons.org/licenses/by-sa/4.0/>

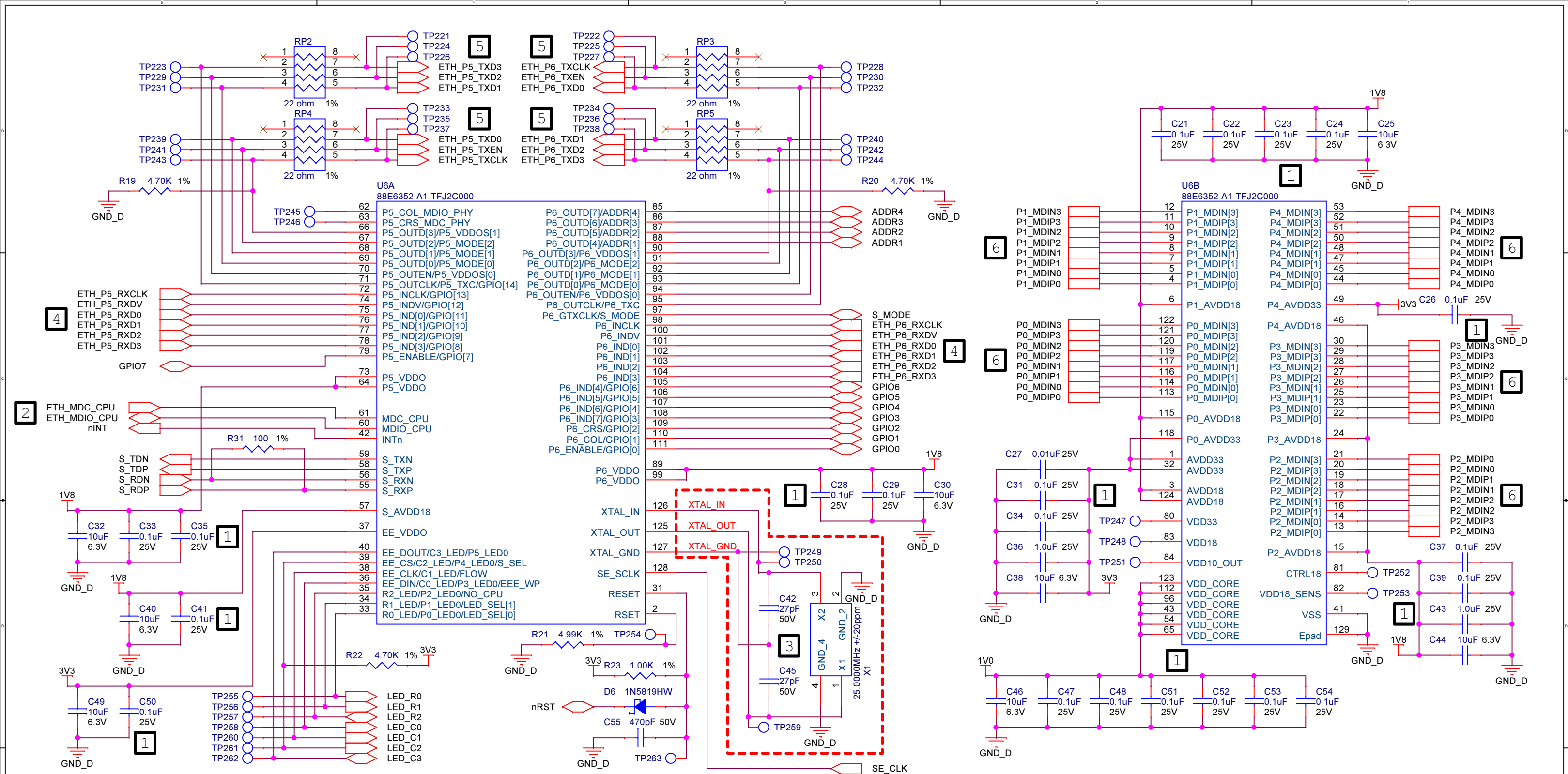
DRAWN BY	B. Hammond	DATE	10/16/2015
CHECKED BY	J. Weatherbee	DATE	10/23/2015
APPROVED BY	R. Cousins	DATE	10/23/2015

TITLE  
giggleBits

PATH  
/

DESCRIPTION  
Main Interconnect 2

SIZE B	DRAWING NO. 15101401-01	REV 1.1
SHEET 3 OF 6		



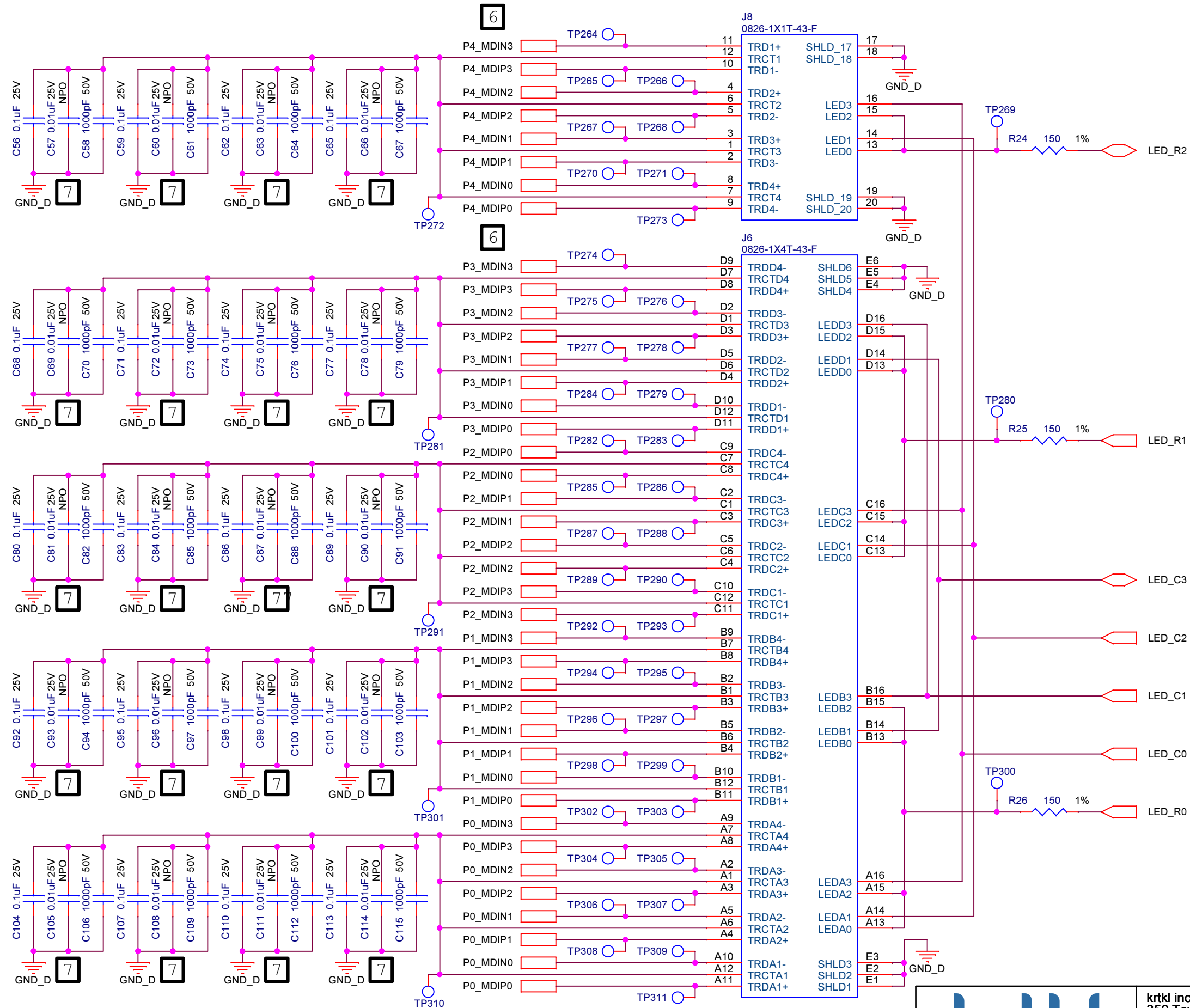
# NOTES:

- 1 Place decoupling capacitors as close to IC pins as possible.
- 2 High speed signal traces should be length matched to within 50mils for each set of grouped signals.
- 3 Minimize capacitance between the crystal drive signals by shielding with the local crystal ground. Also minimize coupling of these signals to other signal lines.

- 4 U6 RGMII inputs ETH\_Px\_RXxx: match trace lengths from connector P3 such that data bit to data bit skew is between -500ps and +500ps, and data bits to clock skew is between 1.0ns and 2.6ns.
- 5 U6 RGMII outputs ETH\_Px\_TXxx: match trace lengths from connector P3 such that data bit to data bit skew and data bits to clock skew is between -500ps and +500ps.

- 6 Route signal pairs with 50ohm single, 100ohm differential impedance.

		<b>krtkl inc.</b> 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857		<b>giggleBits</b> PATH / DESCRIPTION <b>Gigabit Ethernet Switch</b>	
		DRAWN BY <b>B. Hammond</b>	DATE 10/16/2015	SIZE <b>B</b>	DRAWING NO. 15101401-01
CHECKED BY <b>J. Weatherbee</b>		DATE 10/23/2015		REV 1.1	SHEET 4 OF 6
APPROVED BY <b>R. Cousins</b>		DATE 10/23/2015			



# NOTES:

**6** Route signal pairs with 50ohm single, 100ohm differential impedance.

**7** Place each set of three decoupling capacitors as close to Ethernet connector pins as possible.



krtkl inc.  
350 Townsend Street  
Suite 301A  
San Francisco, CA 94107  
+1 415 857 4857

TITLE  
giggleBits  
PATH  
/  
DESCRIPTION  
Gigabit Ethernet Connectors

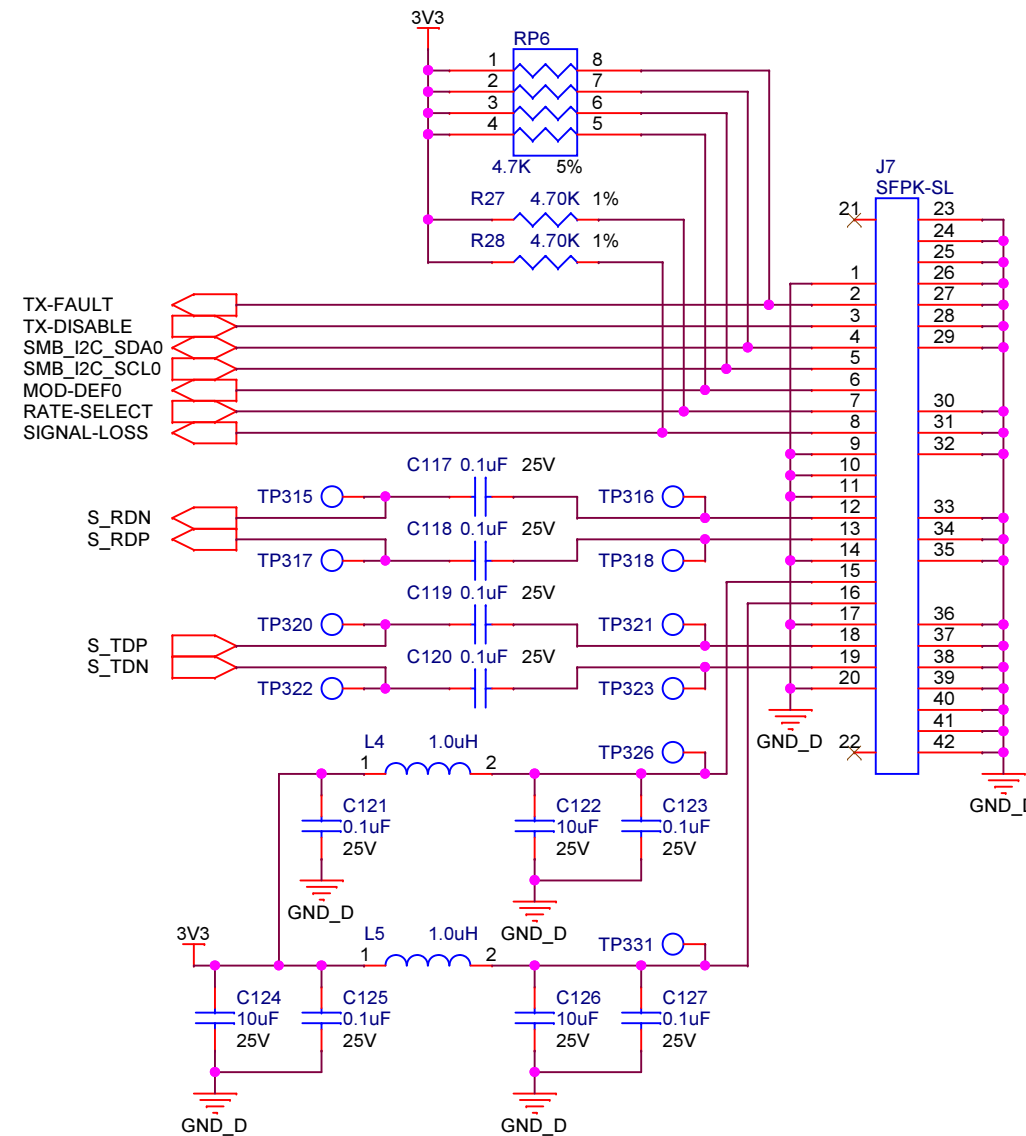
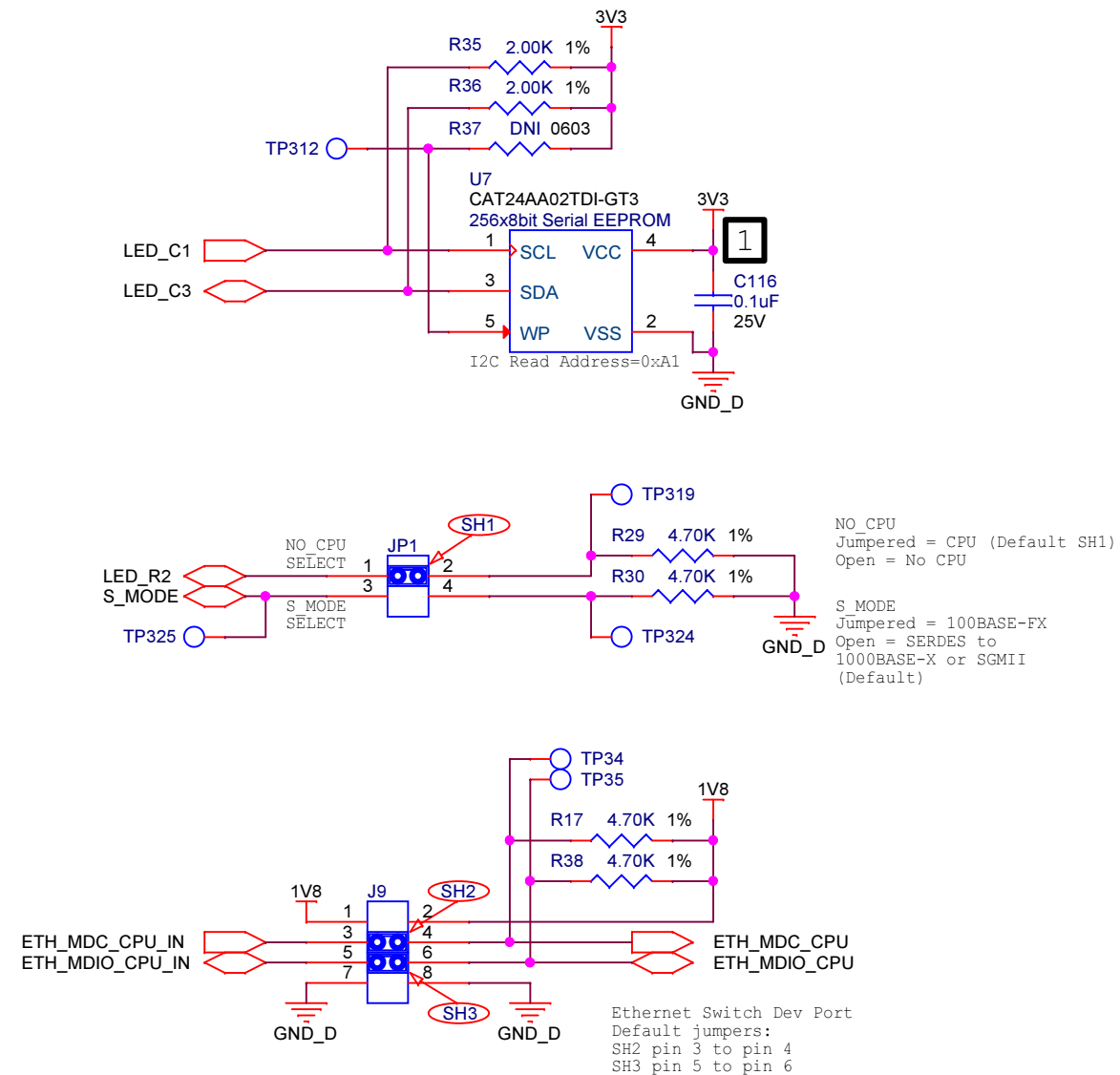


Copyright 2015 krtkl inc. This schematic is made available under a Creative Commons Attribution-ShareAlike 4.0 International License. To view a copy of this license please visit <http://creativecommons.org/licenses/by-sa/4.0/>

NAME	DATE
DRAWN BY B. Hammond	10/16/2015
CHECKED BY J. Weatherbee	10/23/2015
APPROVED BY R. Cousins	10/23/2015

SIZE	DRAWING NO.	REV
B	15101401-01	1.1
SHEET 5		OF 6





NOTES:

1 Place decoupling capacitors as close to IC pins as possible.