Assignment 5: Datapath Design

Task 1

In Figure 1. the microarchitecture of the Datapath and the control unit is shown.

Figure 1. Microarchitecture of Mega Adder

In the diagram there are different bit sizes for the wires, the detail is shown in Table 1.

Color	Size
Black	1
Red	2
Blue	3
Purple	32
Yellow	96
Green	128

Table 1. Bit Size of wires

Task 2

In Figure 2., it can be seen that the input values for a and b are:

```
a: x00000000_00000010_00000020_00000030
b: x00000000_00000001_00000002_00000003
```

From Figure 3., it is seen that the output value of y is:

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y: x00000000_00000011_00000022_00000033
```

This value is clearly correct and the Figure 2 and Figure 3, it is also shown that the valid/ready handshake was carried correctly.
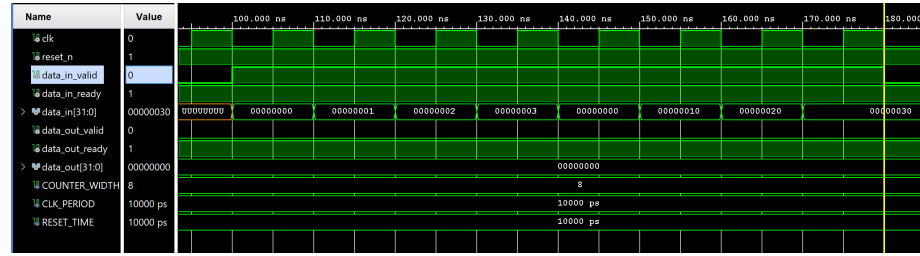

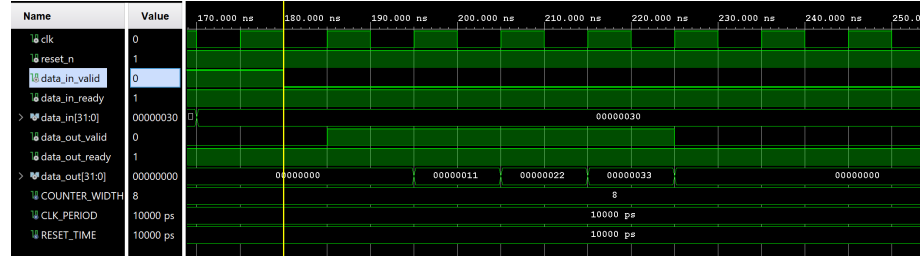*Figure 2. Waveform of Input values for MegaAdder*

Figure 3. Waveform of output values for MegaAdder

Task 3

In the Design (Datapath and Control Unit) 391 FFs were identified, and the detailed count is listed in Table 2.

Signal	Number of FFs
input_shift_cnt	3
output_shift_cnt	2
result_ready_r	1
output_reg_load_r	1
a_r	128
b_r	128

2

Signal	Number of FFs
y_r	128

Table 2. Detailed Count of Number of FFs

The result obtained after running the synthesis tool is found in Figure 4. Based on this results, it can be concluded that the number of FFs calculated are correct.

Resource	Estimation	Available	Utilizatio...
LUT	136	53200	0.26
FF	391	106400	0.37
IO	70	200	35.00
BUFG	1	32	3.13

Figure 4. Post-Synthesis Results

Task 4

The timing contraints were changed, and a clock period of 10ns was set, which implies setting a target frequency of 100MHz. After running the synthesis tool again, the timing report indicates that the timing constraints were met. The Timing report is shown in Figure 5.

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.986 ns	Worst Hold Slack (WHS):	0.140 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	487	Total Number of Endpoints:	487	Total Number of Endpoints:	392

Figure 5. Timing Report of MegaAdder after changes

Task 5

According to the timing report the critical path is located on input of the register *y_r* and the details are shown in Figure 6. After analyzing the signal at the input of this register *y_nxt*, a change on the microarchitecture is proposed as it is indicated in Figure 7.

Name	⤷ Path 1
Slack	-1.014ns
Source	🗋 u_adder_datapath/y_r_reg[32]/C (rising edge-triggered cell FDCE clocke
Destination	🗋 u_adder_datapath/y_r_reg[125]/D (rising edge-triggered cell FDCE clock
Path Group	clk
Path Type	Setup (Max at Slow Process Corner)
Requirement	5.000ns (clk rise@5.000ns - clk rise@0.000ns)
Data Pa... Delay	5.910ns (logic 4.962ns (83.959%) route 0.948ns (16.041%))
Logic Levels	33 (CARRY4=32 LUT4=1)
Clock ... Skew	-0.145ns
Clock U...tainty	0.035ns

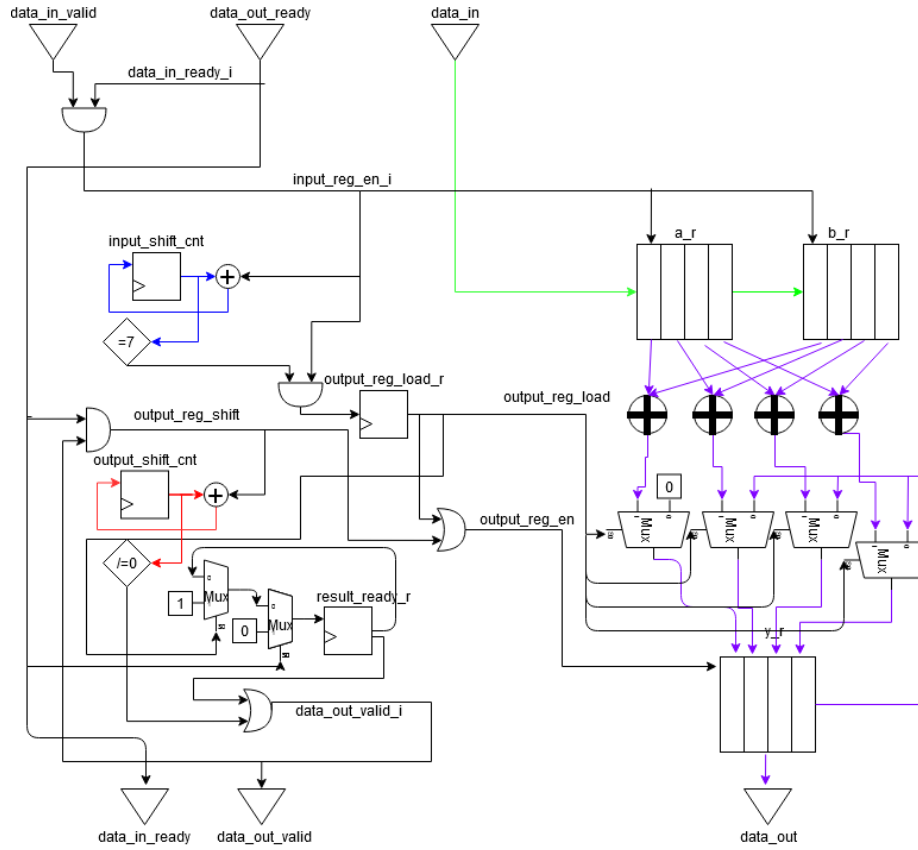*Figure 6. Timing details of the critical path*

Figure 7. Proposed new microarchitecture

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Task 6

The testbench was run, and the testcases were successful. Besides, in Figure 8., the timing report with the new microarchitecture is presented, and it can be seen that the timing constraints are met.

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	1.103 ns	Worst Hold Slack (WHS):	0.140 ns	Worst Pulse Width Slack (WPWS):	2.000 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	487	Total Number of Endpoints:	487	Total Number of Endpoints:	392

All user specified timing constraints are met.

Figure 8. Timing Report with new microarchitecture